Master's thesis

NTNU
Norwegian University of Science and Technology
Faculty of Information Technology and Electrical Engineering
Department of Electronic Systems

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Design of a fully-differential amplifier in 130nm technology for In-Probe Ultrasound Imaging Systems

Master's thesis in Electronic Systems Design and Innovation
Supervisor: Trond Ytterdal
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Abstract

The design of two different fully-differential current-mirror amplifiers for In-probe Ultrasound Imaging Systems is covered in this master thesis. Both amplifiers are designed in 130nm CMOS technology. The first design consists of an inverter input stage and a NMOS current-mirror output. The second design is also an inverter input stage but with a PMOS current-mirror output.

Corner simulations, noise and stability analysis are done for analysing the circuits. A capacitive load of 1pF is used at the output of the amplifier for all simulations. The power supply is set to 1.5V. For the design with a NMOS current-mirror output, a gain of 70.7dB and a unity-gain frequency of 582MHz is reached. The input-referred white noise achieves a result of $4.46nV/Hz^{0.5}$ for the typical corner simulation. In this thesis flicker noise will not be dealt with. This will be handled on system level. A phase margin of 50.2° is received. The power consumption is 1.59mW. Over all corners, gain, unity-gain frequency and noise specifications can be achieved. The specifications for the phase margin can not be achieved over all corner.
For the design with the PMOS current-mirror output, the simulation shows a gain of 65dB. The unity-gain frequency achieves a result of 610MHz. The input-referred white noise is $3.63nV/Hz^{0.5}$ and the phase margin is 56.8°. The power consumption of the design is 2.43mW. Over all corners the gain, unity-gain frequency, noise and phase margin specifications can be achieved.

Sammedrag

Denne masteroppgaven dekker design av to ulike fullt differensielle strømspeilforsterkere for In-probe ultralydavbildningssystemer. Begge forsterkerne er implementert i 130nm CMOS-teknologi. Det første designet består av et inverterbasert inngangstrinn og en NMOS strømspeilutgang. Det andre designet har også et inverter-basert inngangstrinn, men med en PMOS strømspeilutgang.

For å analysere kretsene er det gjort hjørnesimuleringer, støy- og stabilitetsanalyser. En kapasitiv last på 1pF brukes ved utgangen av forsterkeren i alle simuleringene. Strømforsyningen er satt til 1.5V. For implementasjonen med NMOS strømspeilutgang oppnås en forsterkning på 70.7dB og en unity-gain frekvens på 582MHz. Den inngangsrefererte hvite støyen oppnår et resultat på $4.46nV/Hz^{0.5}$ for den typiske hjørnesimuleringen. I denne oppgaven vil flimmerstøy ikke bli behandlet. Dette vil bli håndtert på systemnivå. En fasemargin på 50.2° oppnås. Strømforbruket er 1.59mW. Spesifikasjonene for forsterkning, unity-gain frekvens og støy oppnås i alle hjørner. Spesifikasjonene for fasemargin oppnås ikke for alle hjørner.
For designet med PMOS strømspeilutgang viser simuleringen en forsterkning på 65dB. Unity-gain frekvensen oppnår et resultat på 610MHz. Den inngangsrefererte hvite støyen er $3.63nV/Hz^{0.5}$, og fasemarginen er 56.8°. Strømforbruket til implementasjonen er 2.43mW. Spesifikasjonene for forsterkning, unity-gain frekvens, støy og fasemargin oppnås for alle hjørner.

Preface

This master thesis has been completed at the Department of Electronic Systems at the Norwegian University of Science and Technology in Trondheim during spring of 2024.

I would like to thank my supervisor Professor Trond Ytterdal for the support and help throughout my thesis. I learnt a lot during this project.

I also would like to thank my family for supporting me throughout my studies.

Trondheim, 10. June 2024
Alicia Göbel

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Chapter 1

Introduction

Ultrasound has a wide usage in medicine. During World War II the first use of ultrasound in medicine started all around the world [1]. Most common is ultrasound in gynecologic examinations. But ultrasound is also used for other applications for example to examine the heart of a patient after a heart attack or for examinations on the lung [1].

During an ultrasound examination, high frequency waves are sent into the body of the patient while echos are received [2]. The echos are converted by a receiver into an image which can be analysed [1]. The conversion of the echos is done with the help of an analog-to-digital converter (ADC) [3]. The analog signal received will be converted with an ADC in a digital signal. The digital signal is then used to create an image. In ultrasound in-probe devices, used for medical examinations today, there is a large number of ADC used.

One of the sustainable goals from the United Nations (UN) is to ensure a healthy life and the promotion of well-being for all over the world and at all ages [4]. For achieving this goal it is necessary to ensure the possibility for medical examinations all around the world. One important question for achieving this goal is how it can be realized that all persons around the world, not only in areas with high population, have the possibility for medical examinations like for example ultrasound examinations. A lot of research is done regarding wireless ultrasound in-probe technology and digital ultrasound probes. With this technology it is possible to do ultrasound examination at home without the physical help of medical personal. One point for wireless ultrasound probes is the importance to reduce the number of ADCs in the ultrasound receiver. The ADC has some specifications which needs to be considered while designing it.

Power consumption is for example one important value. It should be minimized as much as possible. This is necessary since high power consumption results in more heat of the probes. This causes problems since the probes are touching the skin of the patient [3]. ADCs comprises of a number of amplifiers which need to be designed properly to ensure a good performance. The amplifier designed in this thesis will be used as the receiving amplifier which is the first amplifier of an ADC.

In this master thesis two different fully-differential current-mirror amplifiers with an inverter-based input stage are designed. For the design a commercially available 130nm CMOS technology is used. A load capacitance of 1 pF is employed on the positive and negative output of the fully-differential amplifier. With respect to noise analysis, only white noise is considered. Flicker noise will be dealt with at system level. All specifications are shown below summarized in table 2. The unity-gain frequency is described with f_{ug}. VDD describes the supply voltage, which drives the amplifier. The gain of the amplifier is defined with A. A_{dB} describes the gain of the amplifier declared in dB. V_n describes the input-referred white noise.

Table 1.1: Specifications for the amplifier

Technology	130nm
f_{ug}	$>$ 500 MHz
VDD	1.5 V
A_{dB}	$>$ 60 dB
A	$>$ 1000
V_n	$< 6nV/Hz^{0.5}$
Load	1 pF capacitance
Phase margin	$> 50°$

1.1 Thesis outline

This thesis is structured as followed:

Chapter 2 - Theory The relevant background theory is described in this chapter. A special focus is given to different operational transconductance amplifier architectures as well as current-mirror circuits and the g_m/I_d - design method.

Chapter 3 - Comparison This chapter covers the comparison of different amplifier designs. Different amplifier designs using current-reuse technique are introduced. Besides this, other techniques like for example feedforward-compensation or folded cascode amplifiers are presented.

Chapter 4 - Design In this chapter the design of the amplifiers is described in more detail. A special focus is done to the design and sizing of two different circuits, as well as calculations regarding gain, unity-gain frequency and the second pole frequency.

Chapter 5 - Results and Discussion Simulation results concerning open-loop simulations, as well as noise and stability analysis for both designs are described in this chapter. After that the results from both designs are discussed in more detail.

Chapter 6 - Conclusion In this chapter, a final conclusion is done. For improvements on the designed amplifiers, future work is presented here as well.

Chapter 2

Theory

In this chapter relevant background theory is discussed in more detail. First a special focus is done to different operational transconductance amplifier architectures. After that the basics of current-mirror circuits will be looked into in more detail since the amplifiers designed in this thesis are predicated on a current-mirror circuit. At the end, the g_m/I_d - design methodology is introduced in more detail. This methodology is important for sizing of the transistors when doing amplifier design.

2.1 Operational transconductance amplifier architectures

There are a lot of different operational transconductance amplifier (OTA) architectures which could be used when designing a differential amplifier. For deciding, which of these possibilities is the best solution for the given specifications, it is important to know about the advantages and disadvantages of the different architectures.

One of the easiest possibility to design an OTA is a five transistor differential pair. This architecture is also the basis for other, more complex, OTA architectures [5]. In this architecture the gain is limited by the finite output impedance of the transistor. Therefore other architectures are needed to be found to improve the output impedance of the transistors [5].

An improvement of the five transistor differential pair architecture is a telescopic folded OTA. Here four additional transistors are added which results in a higher gain [5]. One disadvantage of this architecture is that the output swing is small [5]. The reason for this is that the transistors need overdrive voltage so that they work in saturation region [5].

This problem can be solved with a folded cascode OTA architecture. Here the output swing can be increased by not having a drawback in a smaller gain [5]. The decoupled input and output common-mode voltages are also advantageous for this architecture [5]. Another advantage of the folded cascode OTA architecture is that there is typically no compensation needed since the poles at the low impedance nodes are already at high frequencies [5]. This is due to the fact that the current converted by the input differential pair transistors is taken through low impedance nodes. Besides advantages, this architecture has also disadvantages. The architecture results for example in an increased power and noise [5].

Another possibility to achieve a high gain is to use a current-mirror based OTA. This architecture will be discussed in more detail in chapter 2.2. Current-mirror OTAs achieve a high gain with the help of increasing the number of fingers in the current-mirror. This results in a higher bias current which causes also higher power consumption [6].

Another technique for achieving high gain is to use a folded cascode OTA as described above and build that as two stage OTA. This architecture has the advantage that it can achieve high gain while also having low noise [5]. One disadvantage of this architecture is that due to the internal high impedance node at the cascade a low frequency pole appears which needs to be compensated [5].

An overview and comparison between these different architectures is done in table 2.1 below [5].

(a) is the five transistor differential pair solution, (b) the telescopic folded amplifier, (c) the folded cascode OTA architecture, (d) the current-mirror amplifier and (e) the two-stage OTA. This comparison apply to all the architectures with identical power supply and when being designed in the same technology [5].

Table 2.1: Comparison of different OTA architectures

	(a)	(b)	(c)	(d)	(e)
Output swing	+	-	++	+++	+++
Freq. response	+++	++	+	++	-
Gain	-	++	++	+	+++
Noise	-	-	+++	+	-

It can be seen that there is no architecture which achieves the best results for all parameters. For that reason it needs to be found the best solution for each problem individually with having drawbacks in some areas. As it can be seen in table 2.1 the solution with the folded cascode design and the current-mirror architecture gives overall the best results.

2.2 Current-mirror circuits

A simple CMOS current-mirror is a fundamental block when designing an amplifier. An ideal CMOS current-mirror is shown in figure 2.1.

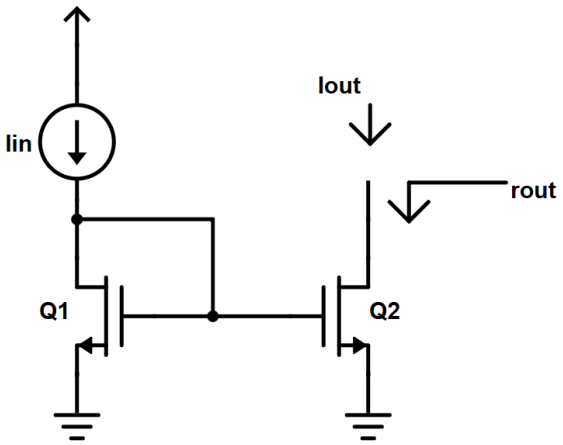

Figure 2.1: Circuit of CMOS current-mirror

For this simplified current-mirror an input current I_{in} generates an output current I_{out}, which is the same size as the input current [6]. This applies to the circuit when assuming that the transistors Q1 and Q2 have the same sizes. For an ideal current-mirror both transistors should be in active region [6]. A transistor is in active region when the drain-source voltage of the transistor is higher than the difference between the gate-source voltage of the transistor and the threshold voltage. The input resistance of a simple CMOS current-mirror can be described with $r_{in} = 1/g_{m1}$, the output resistance of the small-signal model is described with $r_{out} = r_{ds2}$ [6]. When designing current-mirrors, it is necessary to size the transistors properly. For reducing errors due to side-diffusion of the source and drain areas, the transistors should have the same length [7].

This current-mirror circuit as seen in figure 2.1 is the basis for building a current-mirror operational transconductance amplifier (OTA). A high output impedance can be achieved when using an amplifier with a current-mirror. A higher output impedance results in a higher gain [6]. A disadvantage of a current-mirror amplifier compared to for example a folded-cascode design is the increase in the thermal noise. This is due to the fact that the input transistors have a smaller transconductance due to a lower biasing of the total bias current [6].

2.3 The g_m/I_d - methodology

A design methodology often used when doing amplifier design is the g_m/I_d - method. This method is especially useful when sizing transistors since it can be used as calculating tool. The first time, this methodology was introduced was in paper [8] in 1996. Using the g_m/I_d - method results in some advantages compared to the square-law model [9]. The g_m/I_d - method can model at weak and moderate inversion and helps to point to the operating region of an amplifier [10]. Another disadvantage of the square-law model is that it does not include effects of scaling [9]. Due to the fact that the g_m/I_d - methodology uses measurable values of the transistors, it is a very accurate tool [8]. Both parameters, the transconductance and the drain current are connected to the performance of a circuit [8]. Because of a good compromise between speed and power consumption, the g_m/I_d - method is especially used for low power circuits [8]. The size of g_m/I_d determines the gain and speed of a design. A small g_m/I_d results in a high speed and a large V_{dsat} [9]. By contrast to this, a large g_m/I_d results in low power, low speed and a small V_{dsat} [9].

Chapter 3

Comparison of high gain and low noise amplifiers

This chapter covers the comparison of different designs of high gain and low noise amplifiers. A special focus is done to designs using the current-reuse technique. Other designs like for example feedforward-compensated amplifier or folded cascode amplifier are introduced and compared as well.

The goal for this thesis is to design a fully-differential operational transconductance amplifier which achieves a high gain while having a low input-referred noise and a high unity-gain frequency. As already described in chapter 2.1 there are different architectures to design an amplifier. In the last years a lot of different possible solutions to design a high gain, low noise amplifier have been presented in different papers. In the following some of these solutions will be presented to get an overview over the state of the art of amplifiers.

The current-reuse technique is one possible solution. Table 3.1 shows an overview over published papers which all are using current-reuse technique.

The unity-gain frequency is described with f_{ug}, PM represents the phase margin.

Table 3.1: Comparison of amplifier designs using current-reuse technique

Paper	[11]	[12]	[13]	[14]	[15]
Supply voltage	0.8V	1.35V	0.5V	1.2V	0.8V
Load	2pF	200fF	17pF	5pF	200fF
Gain [dB]	62	46.5	70.13	113	54.1dB
f_{ug}	160MHz	280MHz	25kHz	6.6MHz	229MHz
Noise [nV/Hz$^{0.5}$]	17	19	192	41.3	22.3
PM	67°	NA	56°	92°	NA
Power	250μW	55μW	0.337μW	1.3μW	4.91μW
Technology	180nm	180nm	180nm	90nm	22nm

Besides the current-reuse technique there are a couple of other possible solutions to design an amplifier with high gain and low noise like folded cascode amplifiers or feedforward-compensated amplifiers. Some examples from different papers will be discussed in the following as well. A summary of these are shown in table 3.2. As well as before, f_{ug} describes the unity-gain frequency while PM represents the phase margin.

Table 3.2: Comparison of amplifier designs using other techniques

Paper	[16]	[17]	[18]
Supply voltage	1.2V	1.25V	2V
Load	3pF	12pF	1pF
Gain [dB]	70	94	53.3
f_{ug}	70MHz	250MHz	81.4MHz
Noise [nV/Hz$^{0.5}$]	0.35	10.3	4.42
PM	77°	74°	95°
Power	NA	14mW	100μW
Technology	130nm	0.5μm	130nm

An important value when comparing the performance of different amplifiers is the figure of merit (FOM). There are different ways to define this value but it always contains important parameters of an amplifier like for example unity-gain frequency, power dissipation, load capacitance but also gain and input-referred noise. The figure of merit defined in this thesis will be discussed in more detail in chapter 5.3.

3.1 Low voltage, low power current-mirror OTA with near rail-to-rail output

Paper [11], published in 2007, introduces a current-mirror CMOS operational transconductance amplifier (OTA) which uses low voltage and low power. The amplifier architecture described in this paper is based on a current-mirror amplifier with current-reuse technique. The amplifier has a push-pull output stage to increase the voltage gain [11]. Another advantage for that, described in the paper, is the fact that biasing of the output stage will be simplified [11]. Since a fully-differential amplifier is introduced, a common-mode feedback (CMFB) circuit is needed. This paper uses two large resistors, an error amplifier and two transistors to build this circuit [11]. With a load of 2pF, this design achieves a gain of 62dB [11]. A drawback of the design is the low unity-gain frequency and the high noise compared to the specification given for this thesis. The unity-gain frequency of the design in paper [11] is 160MHz. In this paper there is no figure of merit introduced for the designed amplifier.

3.2 Low power current-reuse low noise amplifier

In paper [12], published in 2021, and paper [13], published in 2023, current-reuse operational low noise amplifiers (LNA) are described. In paper [12] a fully-differential amplifier is designed while in paper [13] the amplifier is single-ended. These amplifiers are designed for low power and low noise applications. A low noise amplifier (LNA) can be designed in different ways [12]. Possible solutions could be based on trans-impedance amplifier, current-mirror operational amplifier, inverter-based input stage amplifier, stacked inverter-based OTA, current-reuse amplifier or inverter stacking current-reuse amplifier [12]. The amplifiers described in the papers use an inverter-based input stage and a current-reuse technique. Since the amplifier in paper [13] is single-ended, there is no common-mode feedback circuit needed. The common-mode feedback circuit (CMFB) in [12] is based on two main common-mode feedback technologies and uses a continuous-time common-mode feedback circuit in terms of two resistors and a switched-capacitor CMFB. With a load of 200fF the amplifier described in paper [12] achieves a gain of 46.5dB. The unity-gain frequency is 280MHz. The gain and the unity-gain frequency are slightly lower compared to the specifications for the design in this thesis.

The amplifier designed in paper [13] achieves a gain of 70.13dB with an output load capacitance of 17pF. The unity-gain frequency is with 25kHz very low compared to other designs. The figure of merit calculated in paper [12] for the designed circuit is 0.32 $\frac{GHz^{1.5}}{pWV}$. The figure of merit calculated in paper [13] is 1261.12 $\frac{kHz \cdot pF}{uW}$.

3.3 Cascode current-reuse amplifier

The amplifier introduced in paper [14] from 2023 describes a similar design as the papers in the chapter before. The difference here is that a cascode current-reuse amplifier with four transistors at the input is used. This design makes it possible to achieve higher output resistances which results in a higher gain since the gain is direct proportional to the output resistance [14]. The design uses also current-mirror with cross-coupling transistors in the second stage for increasing the swing [14]. With this design and a load capacitance of 5pF a gain of 113dB can be achieved. The unity-gain frequency is at a very low level with 6.6MHz. The figure of merit is not indicated in this design.

3.4 Fully-differential inverter-based current-reuse OTAs

In paper [15] from 2022, a similar design as in paper [12] is used as basis for designing operational transconductance amplifiers. The difference in this paper is, that four different designs are developed. All designs have an inverter as input stage. The first circuit introduced in this paper is an OTA with a NMOS output current-mirror. The second design is an amplifier with a PMOS output current-mirror. The other alternatives introduced in this paper are cross-coupled versions of both designs with a NMOS and PMOS output current-mirror.
For the version with the NMOS output current-mirror, the highest gain of 41.3dB is achieved with a current gain of K = 3. The unity-gain frequency for this K is 222MHz. The FOM for this setup is 9 $\frac{GHz^{1.5}}{fWV}$ which is very low compared to the setups with the cross-coupling architecture. Here the highest gain is achieved with a K = 7. The drawback with this K is that the unity-gain frequency is lower than having smaller K. With a higher K, a unity-gain frequency of 191MHz is achieved. Despite that the figure of merit is very high with 36.4 $\frac{GHz^{1.5}}{fWV}$.

Another setup which is introduced in this report is the design with a PMOS output current-mirror. Here the highest gain could be achieved with K = 3. The gain of 42.1dB is slightly higher than with the NMOS output current-mirror. The unity-gain frequency achieved in this setup is 219MHz. As a result a FOM of 7.6 $\frac{GHz^{1.5}}{fWV}$ can be calculated. For the architecture with the cross-coupled version, a gain of 56.4dB is achieved with K = 7. The unity-gain frequency is 165MHz and the corresponding figure of merit is 32.9 $\frac{GHz^{1.5}}{fWV}$. With the cross-coupled setup and the PMOS output current-mirror a higher figure of merit can achieved with a current gain of 5. Then the FOM increases to 34.1$\frac{GHz^{1.5}}{fWV}$.

3.5 High gain and low noise folded cascode OTA

As described before there are also other techniques to design a high gain, low noise amplifier. A possible solution is described in paper [16] from 2017. Here a folded cascode OTA is designed. Folded cascode amplifiers have the advantage that they can achieve high gain and low noise together with a high unity-gain frequency [16]. For biasing, a bias scheme for this amplifier is introduced in the paper as well as the results in power savings compared to conventional bias schemes. This amplifier achieves a gain of 70dB with a load capacitance of 3pF. The unity-gain frequency is 70MHz. For this design, there is no figure of merit calculated.

3.6 Two stage single-ended amplifier with feed-forward compensation

Another possibility which is described in paper [17] from 2003 is an amplifier using a no-capacitor feedforward compensation scheme. Feedforward compensation has some advantages compared to Miller compensation scheme [17]. The positive phase shift of the left half plane zeros is used to compensate the negative phase shift due to the poles in feedforward compensation. These left half plane zeros are created by the feedforward path [17]. Feedforward compensation allows to design an amplifier with high gain and fast response [17]. The amplifier designed in the paper [17] is a single-ended two stage amplifier. The paper describes some design considerations which needs to be followed.

Some of these considerations are for example that the second and feedforward stage should not have any non-dominant pole before the unity-gain frequency or that pole-zero cancellation should occur at high frequencies [17]. Especially the last point is important to achieve a good settling time performance. The amplifier achieves a gain of 94dB with an output load capacitance of 12pF. The unity-gain frequency is 250MHz which is high compared to most of the other designs discussed before. A drawback of this design is that a feedforward compensated amplifier needs to be designed properly to achieve the given results [17]. Especially a big focus needs to be done to the poles and zeros of the amplifier. This results in a complex design progress. A figure of merit is not indicated in this paper.

3.7 Low noise CMOS inverter-based amplifier

Paper [18], published in 2019, describes the design of an amplifier which is based on an inverter topology. The amplifier achieves a low noise and power consumption. The design in [18] is a fully-differential amplifier with two CMOS branches. The OTA is a self-bias inverter stage with two pairs of cross-coupled NMOS and PMOS voltage-combiners [18]. The advantage of using voltage-combiners is that a high gain can be achieved as well as an improvement in the energy-efficiency of the amplifier [18]. The amplifier is designed in a 130nm CMOS technology and a supply-voltage of 2V is used [18]. The design in paper [18] achieves a gain of 53.3dB with a load capacitance of 1pF. The unity-gain frequency of the design is 81.4MHz. The FOM of this amplifier is calculated to 1628 $\frac{MHz \cdot pF}{mA}$.

Chapter 4

Design

The next chapters cover the design process of the operational transconductance amplifier. A special focus is done on the design of the amplifier. Here two different designs are introduced. The first solution is a current-mirror amplifier with a NMOS current-mirror at the output. The second solution is build up of the same current-mirror amplifier but it has a PMOS current-mirror at the output. After that calculations are discussed in more detail as well as the sizing of the transistors.

4.1 Amplifier design

In this master thesis a fully-differential current-mirror operational transconductance amplifier is designed using a commercial available 130nm CMOS technology. After literature research and comparison of different design techniques and solutions, a good starting point for the design needed to be found. Here the main focus is done to achieve the specifications as good as possible while having a design which is as simple as possible. Therefore the choice is done to design a circuit similar to that one described in paper [12] and [15]. These two papers base on a similar design, both achieve a high gain while having a high unity-gain frequency and a low noise.

In [15] two different versions of the circuit are presented. The first possibility is to use a NMOS current-mirror at the output of the inverter. Another solution is a PMOS output current-mirror. Both solutions will be introduced and compared in this thesis.

In [15] there is a design introduced using cross-coupled OTA with an output current-mirror. This design will not be considered more in this thesis.

The designed amplifier is shown in figure 4.1. The fully designed circuit can be seen in appendix A.

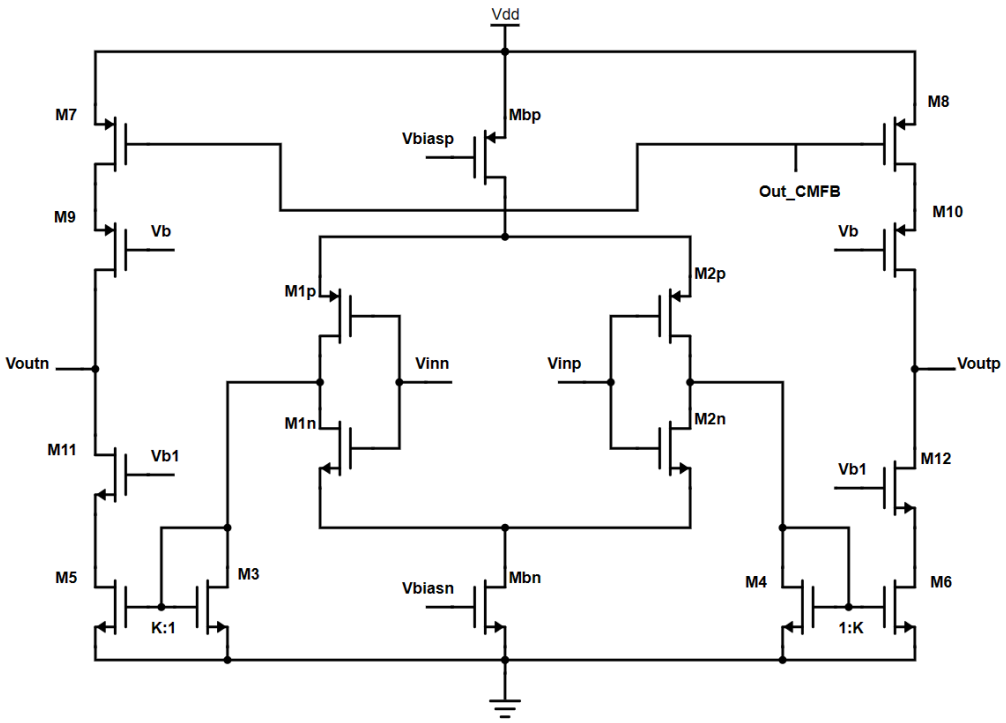

Figure 4.1: Circuit of amplifier with NMOS current-mirror

The amplifier consists of an inverter-based current-mirror OTA with a NMOS current-mirror at the output of the inverter input stage. It also uses current-reuse technique as described in chapter 3. The use of inverter leads to some advantages. One of them is that an inverter increases linearity [5]. Inverter used in OTA design lead to a decreased input-referred noise [5]. Since in this work, the input-referred noise is supposed to be as low as possible, using an inverter stage results in a great benefit.

The inverter-based input stage is build through the transistors M1p, M1n, M2p and M2n. The current-reuse technique is build with transistor M3 and M4. Current-reuse technique as well as inverter-based technique are used to decrease the input capacitance of the amplifier [12]. This can be done by decreasing the transconductance of the input transistors.

The transistors M3, M4, M5 and M6 build the current-mirror. This current-mirror at the output of the inverter input stage helps to achieve a high current without increasing the power usage. The bias current is divided into four branches, the drain currents of the NMOS input transistors M1n and M2n and to the transistors of the current-mirror M3 and M4 [12]. The currents through the transistors M3 and M4 are mirrored further through M5 and M6.

The transistors building the current-mirror are supposed to have the same width and length and only differ in the current gain K. M7 and M8 are the input transistors of the common-source amplifier which has the current-mirror as active load [12]. For achieving the gain and unity-gain frequency specified at the beginning as well as for having a stable amplifier with a phase margin higher than 50° it is necessary to cascode the transistors M5 and M7 at the output.

The amplifier with PMOS current-mirror output has a similar structure as the design with the NMOS setup. The transistors M3, M4, M7 and M8 are building the current-mirror at the output of the inverter stage and are used as active load. In this design, the transistors M3 and M4 are PMOS transistors. The transistors of the current-mirror differ only in the current gain K.
The amplifier with PMOS output current-mirror can be seen in figure 4.2. The fully designed circuit can be seen in appendix B.

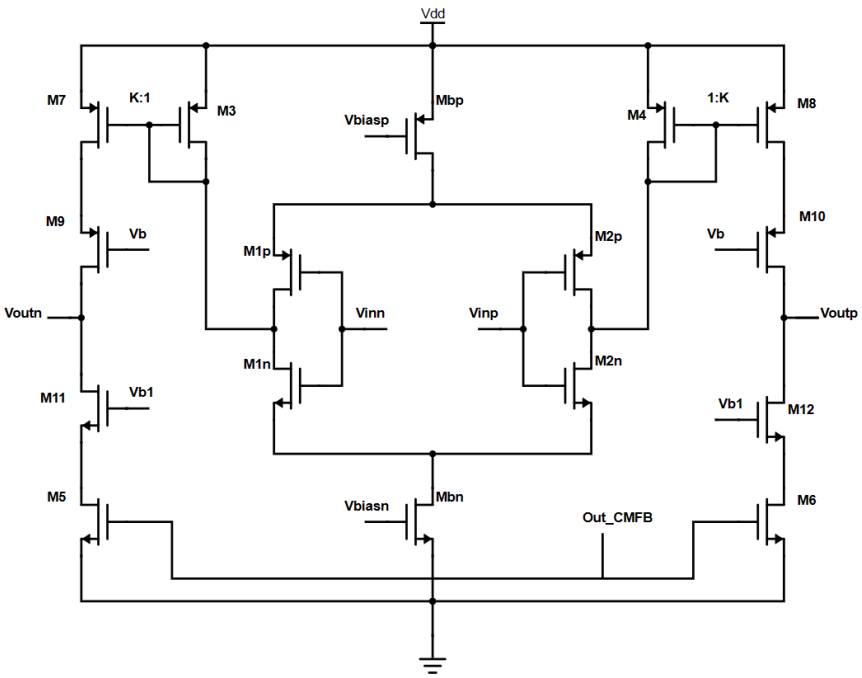

Figure 4.2: Circuit of amplifier with PMOS current-mirror

In fully-differential amplifiers, a common-mode feedback circuit is needed for controlling the common-mode voltage of the amplifier. For this common-mode feedback circuit a simplified model in terms of an ideal OTA is used. The proper design of a common-mode feedback circuit is complex and therefore not part of this thesis.

For biasing the amplifier, a bias circuit with two current-mirrors is used. These current-mirrors are driving the bias transistors Mbn and Mpn. Figure 4.3 shows the bias circuit used in both designs.

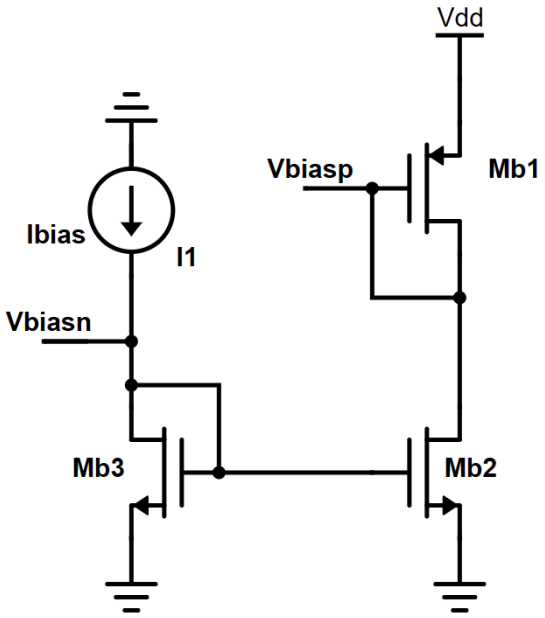

Figure 4.3: Bias circuit

4.2 Calculations

During amplifier design, calculations are done regarding gain and unity-gain frequency. This is used for transistor sizing as well as to compare with the results from the simulations. Since the circuit is assumed to be symmetric, all calculations need to be done for the half circuit only.

First, the gain will be looked into in more detail. When doing low frequency small signal analysis, it can be found an equation 4.1 for the gain of the output of the amplifier.

$$A_o = \frac{v_{out}}{v_1}\frac{v_1}{v_{in}} = \frac{v_{out}}{v_{in}} \tag{4.1}$$

In this equation v_{out} describes the output voltage and v_{in} the input voltage of the amplifier. The output voltage of the inverter input stage is defined as v_1.

The input voltage of the amplifier can be found with equation 4.2:

$$v_{in} = \frac{v_1}{g_{m1} r_{in}} \tag{4.2}$$

g_{m1} describes the transconductance of the inverter input stage, r_{in} is the output resistance of the inverter input stage. The transconductance g_{m1} of the inverter input stage is the amount of both the transconductance of NMOS and PMOS transistor, so that $g_{m1} = g_{m1n} + g_{m1p}$. The input resistance can be calculated with equation 4.3.

$$r_{in} = r_{ds1} || r_{ds3} || (1/g_{m3}) \tag{4.3}$$

The sum of the drain-source voltage of the two input transistors M1n and M1p is described with r_{ds1}. The drain-source voltage of the transistor M3 which builds the current-mirror is described with r_{ds3}. g_{m3} describes the transconductance of the transistor M3 of the current-mirror.

Due to the assumption that $r_{ds1} || r_{ds3} >> 1/g_{m3}$, the input resistance can be calculated with $r_{in} = 1/g_{m3}$.

As well as for the input voltage, an equation for the output voltage of the amplifier can be found with equation 4.4.

$$v_{out} = g_{m5} r_{out} v_1 \tag{4.4}$$

In this equation g_{m5} describes the transconductance of the transistor M5. r_{out} is the output resistance of the amplifier.

With the equation for the input and output voltage, the gain of the amplifier can be calculated with equation 4.5.

$$A_o = \frac{v_{out}}{v_{in}} = g_{m1} r_{in} g_{m5} r_{out} = \frac{g_{m1}}{g_{m3}} g_{m5} r_{out} \tag{4.5}$$

The transistors M3 and M5 are building a matched current-mirror and only differ in the current gain K. Therefore the following relation can be found for the transconductance of the transistor M5:

$$g_{m5} = K g_{m3} \tag{4.6}$$

With equation 4.5 and equation 4.6, the gain can be written to:

$$A_o = g_{m1} K r_{out} \tag{4.7}$$

With this equation it can be seen that the gain is only dependent on the transconductance g_{m1} of the inverter, the factor K and the output resistance of the amplifier.

Besides low frequency small signal analysis, high frequency small signal analysis can be done to achieve an equation for the unity-gain frequency. For finding the unity-gain frequency it is important to know where the dominant pole is located. This can be found with equation 4.8.

$$w_{out} = \frac{1}{r_{out} C_{L,eff}} \tag{4.8}$$

In this equation r_{out} describes the output resistance of the amplifier. $C_{L,eff}$ is the effective load capacitance at the output. It consists of the load capacitance and the parasitic capacitance of the output transistors M5/M6, M7/M8, M9/M10 and M11/M12. For now it is assumed that only the load capacitance is dominant and that the parasitic capacitances are much smaller so that they can be neglected.

With that the unity-gain frequency can be found with equation 4.9.

$$f_{ug} = \frac{A_o w_{out}}{2\pi} = \frac{K g_{m1}}{2\pi C_L} \tag{4.9}$$

In this equation, C_L represents the load capacitance. It can be seen that both, the gain and the unity-gain frequency are dependent on K. A higher K results in a higher gain and also a higher unity-gain frequency but with the trade-off of lowering the phase margin [6]. In practice K is often smaller than 5 [6]. With a high K the second pole is moved to lower frequencies [6].

A second pole frequency lower than the unity-gain frequency influences the stability of the circuit and decreases the phase margin [6]. If the second pole dominates, this results in a decrease in the unity-gain frequency. Then it is necessary to increase the load capacitance to ensure stability of the circuit [6]. The load capacitance for this design is a fixed value, which can not be changed. Because of this, it is important to have a second pole frequency which is higher than the unity-gain frequency. This second pole frequency can be calculated to ensure that this requirement is fulfilled for the design.

The equation for the frequency f_{p2} can be described with:

$$f_{p2} = \frac{w_{p2}}{2\pi} \tag{4.10}$$

w_{p2} is the angular frequency of the second pole and can be calculated with equation 4.11.

$$w_{p2} = \frac{g_{m3}}{C_{tot}} \tag{4.11}$$

The transconductance of the transistor M3, which builds the current-mirror, is described with g_{m3}. C_{tot} is the total capacitance and can be calculated with equation 4.12.

$$C_{tot} = C_{db1} + C_{db3} + C_{gs3} + C_{gs5} \tag{4.12}$$

Here C_{db1} is the sum of the drain-bulk capacitances of the inverter transistors, C_{db3} describes the drain-bulk capacitance and C_{gs3} the gate-source capacitance of the transistor M3. C_{gs5} is the gate-source capacitance of the transistor M5 of the current-mirror.

4.3 Transistor sizing

For finding the sizes of the transistors the g_m/I_d - method is used as well as calculations for gain and unity-gain frequency. The inverter input stage is designed to have at least a g_m/I_d from 10 since large g_m/I_d results in a lower power. The inverter input stage should also be designed to have an output voltage of around 750mV, which is half of the supply voltage.

The unity-gain frequency can be calculated with equation 4.9. Due to the specifications, the unity-gain frequency should be higher than 500MHz. The load capacitance C_L is defined to be 1pF.

The transconductance g_{m1} of the input inverter stage can be calculated with equation 4.13:

$$g_{m1} > \frac{2\pi C_L f_{ug}}{K} \tag{4.13}$$

With the values of the specifications, the transconductance of the inverter stage g_{m1} is calculated to be higher than $1571 \cdot 10^{-6}$ for a K = 2. For a K = 3, the transconductance g_{m1} needs to be higher than $1048 \cdot 10^{-6}$.

After these calculations the transistors can be sized. The sizing of all transistors is also done with attention to the minimal and maximal sizes for this technology. The designed amplifier is used in the implementation of an analog-to-digital converter. For that reason, the specification is to not have gate fingers which are longer than 8μm. Therefore the number of gate fingers is used, as it can be seen in the tables.

The sizes for the bias transistors are identified experimentally under consideration that all transistors are in active region. This is important to ensure a good performance. The bias transistors Mb1, Mb2 and Mb3 are similar in both designs. The values for the bias circuit can be seen in table 4.1.

Table 4.1: Transistor dimensions for bias circuit

Name	Type	Width [um]	Length [nm]	Multiplier	Finger
Mb1	PMOS	49.98	130	1	7
Mb2, Mb3	NMOS	40	200	1	5

The table below shows the dimensions for the transistors of the design with the NMOS current-mirror load. The current gain K in this design is chosen to be three.

Table 4.2: Transistor dimensions of circuit with NMOS current-mirror

Name	Type	Width [um]	Length [nm]	Multiplier	Finger
M1p, M2p	PMOS	50	250	1	8
M1n, M2n	NMOS	25	400	1	5
M3, M4	NMOS	3.6	200	1	1
M5, M6	NMOS	3.6	200	K	1
M7, M8	PMOS	24.99	850	K	7
M9, M10	PMOS	33	400	1	5
M11, M12	NMOS	0.95	300	9	1
MPb	PMOS	18.795	130	1	3
MNb	NMOS	3	170	3	1

The sizing for the circuit with a PMOS current-mirror load is done similar to the sizing of the circuit with a NMOS current-mirror. As described in chapter 4.1 the transistors M3, M4, M7 and M8 are building the current-mirror part in this design. The dimensions of all transistors can be seen in table 4.3. The current gain K in this design is set to two.

Table 4.3: Transistor dimensions of circuit with PMOS current-mirror

Name	Type	Width [um]	Length [nm]	Multiplier	Finger
M1p, M2p	PMOS	50	250	1	8
M1n, M2n	NMOS	35	220	1	8
M3, M4	PMOS	14	180	1	2
M5, M6	NMOS	40	630	1	5
M7, M8	PMOS	14	180	K	2
M9, M10	PMOS	19.4	200	5	5
M11, M12	NMOS	20	500	10	8
MPb	PMOS	2.7	130	2	1
MNb	NMOS	35	200	1	5

Chapter 5

Results and Discussion

The following chapter presents the results of different simulations done after the design of both amplifiers. Open-loop simulations are done as well as stability analysis to ensure that all specifications are achieved and to verify that the circuit is stable. Similar simulations are done for both designs. At the end of this chapter, a comparison of the results of both designs will be done to highlight advantages and disadvantages of the circuits.

As already described in chapter 4.1 two different circuits are designed. Both designs use the same testbenches for simulations ensuring that the amplifier achieves the specified unity-gain frequency and gain as well as the input-referred noise and phase margin. For both simulations a special focus is done to transistor process corner simulations.

The simulations are done in Cadence Virtuoso. A load capacitance of $C_L = 1pF$ is used at the fully-differential outputs. The supply voltage is set to 1.5V. The common-mode voltage is defined to 750mV.

Open-loop simulations are done with both designs using the testbench shown in figure 5.1. The full testbench can be found in appendix C.

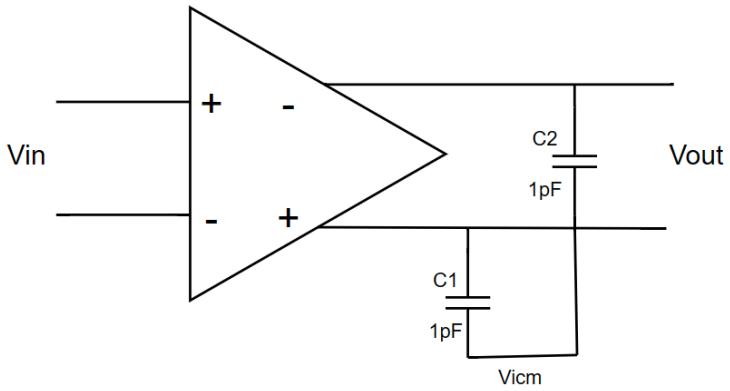

Figure 5.1: Testbench for open-loop simulations

For ensuring that the designed circuit is stable and for simulating the phase margin, the testbench shown in figure 5.2 is used. The full testbench can be found in appendix D.

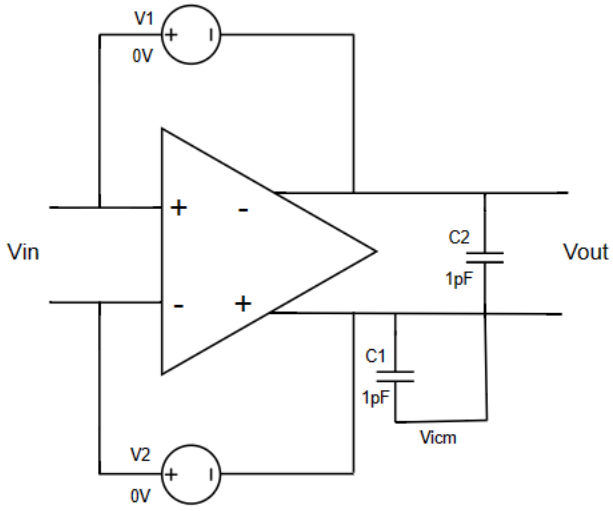

Figure 5.2: Testbench for stability analysis

An ideal OTA is used as simplified model for the common-mode feedback circuit, which can be seen in figure 5.3. The gain of the ideal amplifier is set to 10^6. As seen in the figure, the common-mode input of the amplifier is set to ground while the negative input is connected to the common-mode voltage. The positive input is connected to two resistors, which have a size of $1G\Omega$.

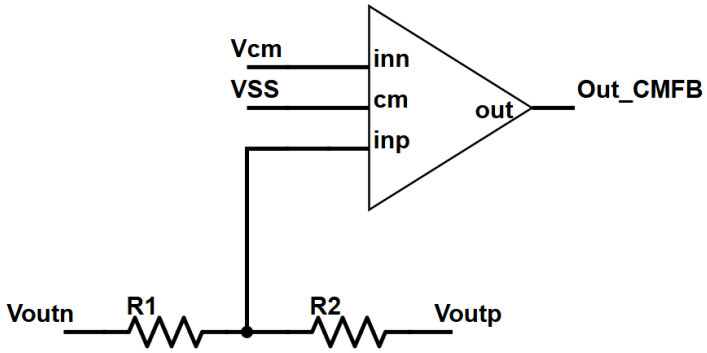

Figure 5.3: Model for common-mode feedback circuit

A common-mode feedback circuit needs to be designed properly that it works as expected. The design of a whole common-mode feedback is not part of this work.

5.1 Simulation of amplifier with NMOS current-mirror output

The simulations for the amplifier with a NMOS current-mirror load are done similarly to the simulations for the design with a PMOS current-mirror. The bias current for the bias circuit, which is build with Mbn, Mbp, Mb1, Mb2 and Mb3, is set to 485uA. Due to the cascoding structure at the output of the amplifier, two additional voltage sources are needed. For the voltage source at the cascoded PMOS transistor M9/M10, a voltage of 450mV is used. The voltage at the cascoded NMOS transistor M11/M12 is set to 1.2V. These voltages are found experimentally under consideration to achieve the specified gain, unity-gain frequency, noise and phase margin.

As input signal of the amplifier V_{in} a sine wave is used. The frequency is set to 10MHz and it has an AC magnitude of 1V. The input common-mode voltage is set to 750mV, which correspond to half of the supply voltage.

The load capacitance is connected to both differential outputs and to the common-mode voltage V_{icm} as seen in figure 5.1 and figure 5.2.

As described in chapter 4.3, a current gain of K = 3 is used for the design with a NMOS current-mirror load. As seen in chapter 4.2, K is proportional to the gain and unity-gain frequency. A high K results also in a decreased phase margin as described in chapter 4.2. It is therefore always necessary to have a trade-off between a high gain and a high unity-gain frequency on the one side and a high phase margin on the other side.

Table 5.1 shows the drain currents of the transistors and the transconductance for the circuit as well as the calculated value for g_m/I_d.

Table 5.1: Drain current and transconductance for typical corner

Transistor	Transconductance	Drain current [uA]	g_m/I_d
M1P/M2P	1.1m	70.9	15.5
M1N/M2N	669u	33.5	20
M3/M4	478u	37.4	12.8
M5/M6	1.4m	109	12.8
M7/M8	1.04m	109	9.54
M9/M10	1.01m	109	9.27
M11/M12	1.09m	109	10

The drain currents of the four transistors M5/M6, M7/M8, M9/M10 and M11/M12 at the output of the amplifier are identical as expected.

As it can be seen in table 5.1, the goal of having a g_m/I_d higher than 10 for the input inverter stage can be reached. The g_m/I_d of the transistors M3/M4 and M5/M6, which are building the current-mirror, is also higher than 10. Comparing the calculated value for the transconductance g_{m1} in chapter 4.3 with the value from the simulations, it can be seen that it is higher than the minimum transconductance with a value of $1769 \cdot 10^{-6}$.

Open-loop simulations over different process corners are done. There are four different process corners, fast-fast (FF), slow-slow (SS), fast-slow (FS) and slow-fast (SF). The results for this can be seen in table 5.2.

The unity-gain frequency is described with f_{ug}, PM is the phase margin.

Table 5.2: Simulation results with NMOS current-mirror for all corners

Corner	Gain [dB]	f_{ug} [Hz]	Noise $[nV/Hz^{0.5}]$	PM
Typical	70.7dB	582M	4.46	50.2°
FF	67dB	631M	4.30	51.1°
SS	74dB	503M	4.66	48.1°
FS	70.3dB	545M	4.46	46.4°
SF	69.7dB	590M	4.48	52.3°

For the typical simulation, a gain of 70.7dB is achieved with the design. The gain of the simulations over the corners varies between 67dB for the FF corner and 74dB for the SS corner. The unity-gain frequency for the typical corner is 582MHz. Over the different corners the unity-gain frequency differs between 503MHz for the SS corner and 631MHz for the FF corner.

Figure 5.4 shows the simulation result of the gain and phase response for the open-loop simulations. The blue graph represents the gain, while the red graph shows the phase response.

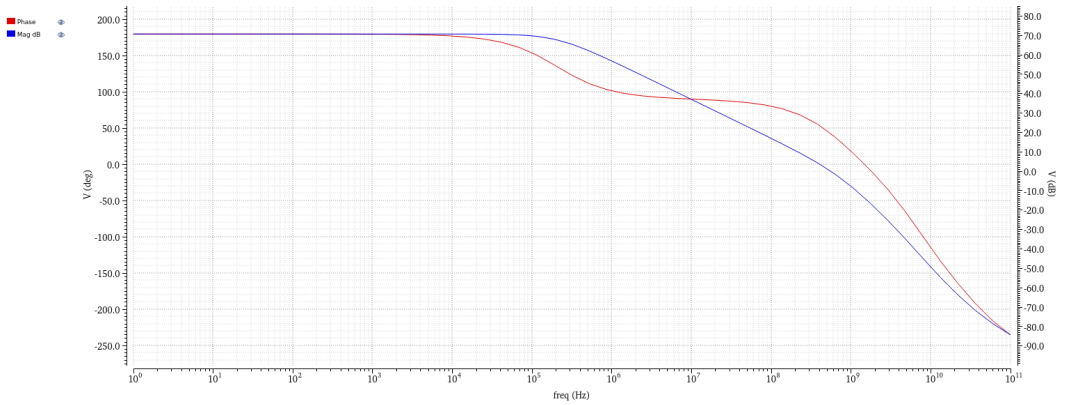

Figure 5.4: Simulation results for typical corner

As described in chapter 4.2 it is important that the second pole frequency is higher than the unity-gain frequency. For this reason, the second pole frequency f_{ug2} of the circuit is calculated. From extracting the second pole frequency from the graph, it is assumed that it is located at around 1GHz. The second pole frequency can be calculated with equation 5.3 where w_{p2} is described with equation 4.11. From the simulations g_{m3} is received to be 478u. The total capacitance can be calculated with 4.12 and is around 49fF for the typical simulation.

With this f_{p2} can be calculated to:

$$f_{p2} = \frac{g_{m3}}{2\pi C_{tot}} = \frac{478 \cdot 10^{-6}}{2\pi \cdot 49 \cdot 10^{-15}} = 1.55GHz \tag{5.1}$$

The calculations confirm the second pole frequency at 1.55GHz as assumed from the visual extraction.

The results for the input-referred noise can be found in the table 5.2 above as well. The input-referred noise for the typical corner is $4.46nV/Hz^{0.5}$. Over the different corners, the input-referred noise varies between $4.30nV/Hz^{0.5}$ for the FF corner and $4.66nV/Hz^{0.5}$ for the SS corner. Figure 5.5 shows the graph of the noise simulations for the typical corner. The input-referred noise can be read off the constant part between 10^7 and 10^8.

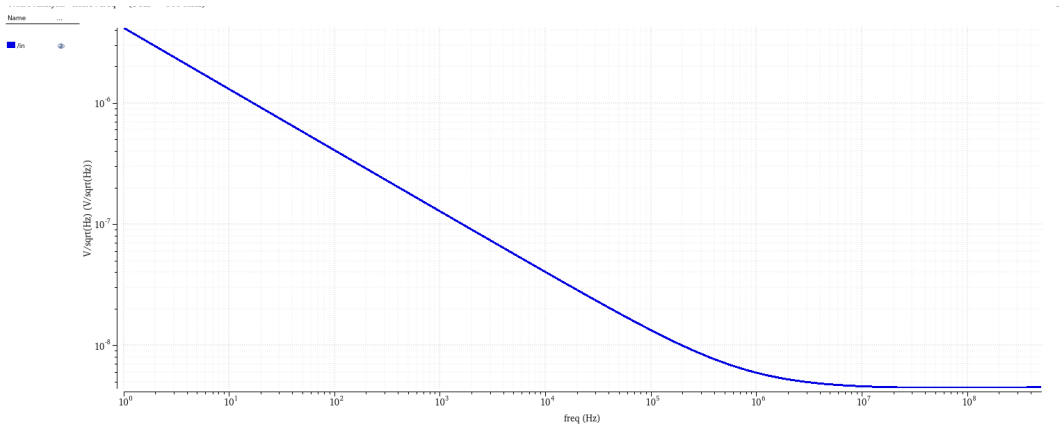

Figure 5.5: Simulation results for noise for typical corner

For the simulation of the phase margin and for ensuring stability of the design, stability analysis is done. As described before the testbench shown in figure 5.2 is used for this simulation. As it can be seen in table 5.2 a phase margin of 50.2° for the typical corner is achieved. Over the different corner, the phase margin varies between 46.4° for the FS corner and 52.3° for the SF corner. In figure 5.6 the results from the stability analysis are shown. The blue graph shows the loop gain, the red graph represents the loop phase.

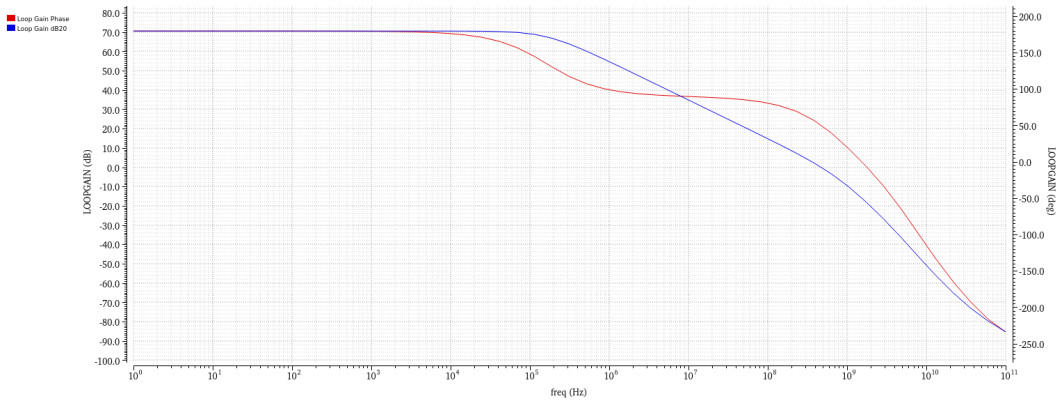

Figure 5.6: Graph of loop gain and phase of the NMOS current-mirror

Comparing the results received in the open-loop simulations and the stability analysis with the specifications, it can be seen that most requirements are accomplished. The gain is higher than 60dB over all corners. The unity-gain frequency achieves over all corner a result higher than 500MHz. The noise is supposed to be smaller than $6nV/Hz^{0.5}$. This requirement is also achieved over all corners. For ensuring a stable amplifier, a phase margin between 45° and 90° is required, typically it should be higher than 50° [6]. If the phase margin is too small, undesirable behavior in frequency response for the closed-loop amplifier can occur. The goal in this thesis is to design an amplifier with a phase margin higher than 50°. This goal could not be achieved over all corners for the design with the NMOS current-mirror load. A reason for that could be, that the output voltage of the inverter input stage is much smaller than half of the supply voltage. Table 5.3 shows the output voltages over all corners.

Table 5.3: Output voltages of inverter stage

Corner	V_{out} in [mV]
Typical	624
FF	567
SS	670
FS	525
SF	711

It can be seen, that for all corners the output voltage of the inverter input stage is much lower than 750mV. Especially in the FS corner the deviation is high. This could be one reason that causes smaller phase margin, especially in this corner.

Another observation which could be done during corner simulation is that in the SS corner and the FS corner not all transistors are in active region. For both corners the bias transistors Mbp are in triode region. This could also be the reason for not achieving the required phase margin.

A consideration, which is done during calculations for the unity-gain frequency in chapter 4.2 before, is that the parasitic capacitances of the output transistors M5/M6, M7/M8, M9/M10 and M11/M12 can be neglected and that only the load capacitance C_L is dominant. With the results in the simulations, $C_{L,eff}$ can be calculated with equation 5.2 to ensure, that this assumption is fulfilled in the real design.

$$C_{L,eff} = \frac{Kg_{m1}}{2\pi f_{ug}} = \frac{3 \cdot 1769 \cdot 10^{-6}}{2\pi \cdot 582 \cdot 10^{6}} = 1.45pF \tag{5.2}$$

With this, it can be seen, that the assumption that the load capacitance C_L dominates over the parasitic capacitances of the output transistors is almost fulfilled.

5.2 Simulation of amplifier with PMOS current-mirror output

As already described in chapter 4.1 two different circuits are designed in this thesis. For comparing the performance of both designs afterwards, open-loop and stability simulations are done similar to them described in the chapter before. The bias current for the bias circuit is set to 485uA, similarly to the setup with the NMOS current-mirror output. As explained in chapter 5.1, two additional voltage sources are needed for the cascoding structure at the output of the amplifier. The voltage source at the cascoded PMOS transistor M9/M10 is set to 300mV. The voltage at the cascoded NMOS transistor M11/M12 is set to 1.1V. The values for the voltages are found experimentally under consideration to achieve all specifications.

The input signal is similar to the setup for the NMOS current-mirror output.

For the PMOS design, a current gain of K = 2 is used since it came out that this K results in the best performance for the design. The table 5.4 shows the drain currents and trandsconductances of the transistors as well as the calculated value for g_m/I_d.

Table 5.4: Results for transconductance and drain current for typical corner

Transistor	Transconductance	Drain current [uA]	g_m/I_d
M1P/M2P	424u	21.1	20.1
M1N/M2N	2.87m	180	15.9
M3/M4	1.24m	159	7.8
M5/M6	3.11m	299	10.4
M7/M8	2.36m	299	7.9
M9/M10	3.74m	299	12.5
M11/M12	5.65m	299	18.9

As it can be seen for the design with a NMOS current-mirror, the drain currents of the four output transistors M5/M6, M7/M8, M9/M10 and M11/M12 are equal here as well.

The goal to have a g_m/I_d higher than 10 for the transistors of the inverter input stage is achieved as well. It can be seen, that except of the transistors of the current-mirror, all values for g_m/I_d are higher than 10. As described in chapter 4.3 the transconductance g_{m1} should be higher than $1571 \cdot 10^{-6}$. The sum of the transconductance of M1P and M1N can be calculated to $3294 \cdot 10^{-6}$ and is much higher than the minimum transconductance calculated in chapter 4.3.

Open-loop simulations over different process corners are done to verify all specifications for gain, unity-gain frequency and input-referred noise. These simulations are similar to these explained in chapter 5.1. Table 5.5 shows the results for unity-gain frequency, gain and noise of the amplifier with a PMOS current-mirror output over different process corners. There are four different process corners, fast-fast (FF), slow-slow (SS), fast-slow (FS) and slow-fast (SF).

Table 5.5: Simulation results with a PMOS output stage for all corners

Corner	Gain [dB]	f_{ug} [Hz]	Noise $[nV/Hz^{0.5}]$	PM [°]
Typical	65dB	610M	3.63	56.8°
FF	61.9dB	655M	3.49	56.5°
SS	65.8dB	565M	3.82	57.6°
FS	64.5dB	605M	3.62	57.5°
SF	62.7dB	603M	3.69	56.7°

The unity-gain frequency is described with f_{ug}, the phase margin with PM. As it can be seen in table 5.5, a gain of 65dB is achieved in the typical corner. Over the different corners the gain varies between 61.9dB for the FF corner and 65.8dB for the SS corner.
The unity-gain frequency is 610MHz in the typical corner and varies between 565MHz for the SS corner and 655MHz for the FF corner.

The graph of the gain and phase response for the open-loop simulations for the typical corner can be seen in the figure 5.7 below. The blue graph shows the gain response while the pink graph represents the phase response.

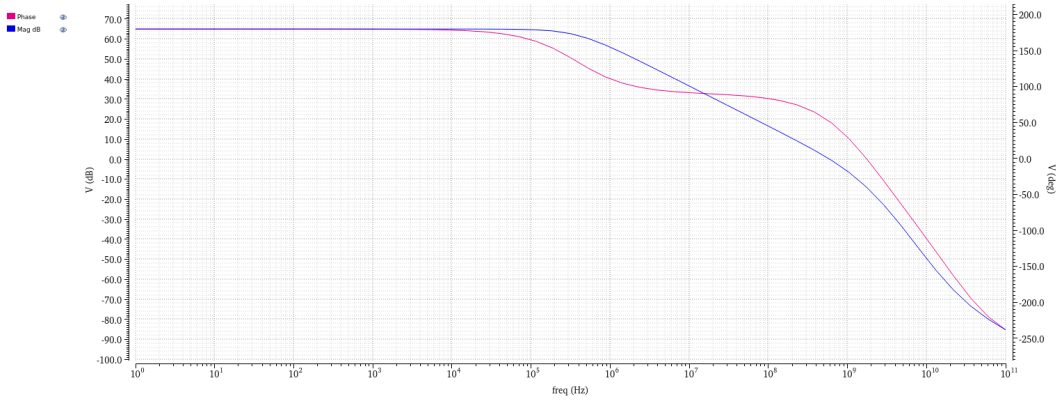

Figure 5.7: Graph for gain and phase response for open-loop simulations

As well as in chapter 5.1, the second pole frequency is calculated to ensure, that it is higher than the unity-gain frequency. When extracting the second pole frequency from the graph, it is assumed that the pole is located at around 2GHz. The second pole frequency f_{p2} can be calculated with equation 5.3. From the simulations a transconductance g_{m3} of 1.24m is received. The total capacitance can be calculated with equation 4.12 and is around 89.8fF. With that f_{p2} can be calculated to:

$$f_{p2} = \frac{g_{m3}}{2\pi C_{tot}} = \frac{1.24 \cdot 10^{-3}}{2\pi \cdot 89.8 \cdot 10^{-15}} = 2.2GHz \tag{5.3}$$

This result correspond to the result from visual extraction of the second pole frequency from the graph.

The results for the input-referred noise can also be found in table 5.5. For the typical corner the input-referred noise is $3.63nV/Hz^{0.5}$. Over the different corners the input-referred noise varies between $3.49nV/Hz^{0.5}$ for the FF corner and $3.82nV/Hz^{0.5}$ for the SS corner. In figure 5.8 the graph for the input-referred noise of the typical corner is shown. As seen before when discussing the circuit with the NMOS current-mirror output, the graph is as expected. The constant part between 10^7 and 10^8 represents the input-referred noise.

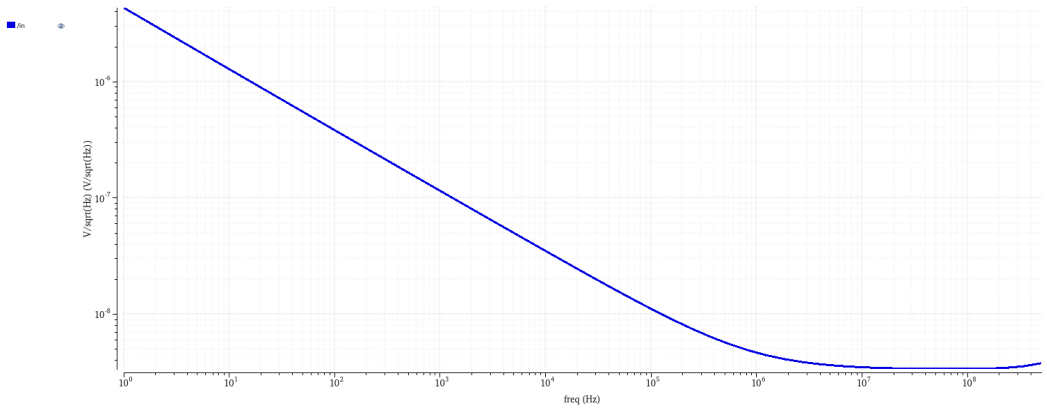

Figure 5.8: Graph for noise for open-loop simulations

Besides the open-loop simulations, stability analysis is done to ensure the stability of the amplifier as well as that the phase margin can be achieved. The results of the phase margin over all corners can be seen in table 5.5. In the typical corner, a phase margin of 56.8° can be achieved. Over the different corner the phase margin differs between 56.5° for the FF corner and 57.6° for the SS corner. One observation which can be done is that the phase margin does not vary so much. The difference between the worst and the best corner is only 1.1°. Figure 5.9 shows the results from the stability analysis. The pink graph represents the loop phase. The blue graph shows the loop gain.

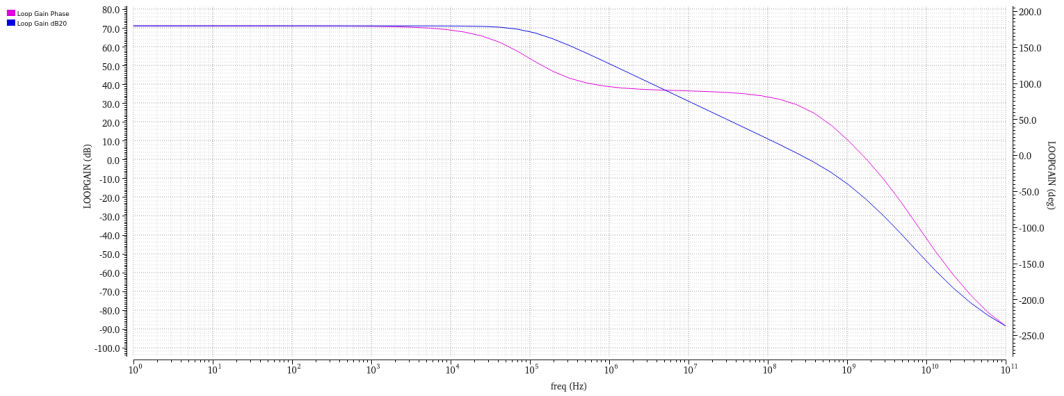

Figure 5.9: Graph for stability analysis

The result from the open-loop simulations and stability analysis can be compared with the specifications. Over all corners, a gain higher than 60dB is achieved. The unity-gain frequency reaches a result which is higher than 500MHz for all process corners. Also the requirement for noise and phase margin could be achieved.

Table 5.6 shows the output voltages of the inverter input stage. Optimally, a voltage higher than 750mV should be achieved here. This corresponds to half of the supply voltage. As it can be seen in the table, this requirement can almost be achieved for all corners. Only two corners have a slightly lower output voltage.

Table 5.6: Output voltages of inverter stage

Corner	V_{out} in [mV]
Typical	792
FF	865
SS	722
FS	703
SF	883

With all the results from the simulations above, calculation can be done to verify if the assumption of having an effective load capacitance of 1pF is right. For doing this, the transconductance g_{m1} and the unity-gain frequency for the typical corner are used to calculate the effective capacitance with equation 5.4.

$$C_{L,eff} = \frac{Kg_{m1}}{2\pi f_{ug}} = \frac{2 \cdot 3294 \cdot 10^{-6}}{2\pi \cdot 610 \cdot 10^{6}} = 1.72pF \tag{5.4}$$

With the result from the simulations, an effective load capacitance of 1.72pF can be calculated. This is close to the 1pF assumed before when doing calculations.

5.3 Comparison of both designs

After doing simulations, the results will be compared to find advantages and disadvantages of the both designs. In table 5.7 the results of all simulations are presented for the typical corner. The unity-gain frequency is described with f_{ug}, the phase margin is described with PM.

Table 5.7: Summary of the designed amplifiers

Design	Gain [dB]	f_{ug} [Hz]	Noise $[nV/Hz^{0.5}]$	PM	Power [mW]
NMOS	70.7dB	582M	4.46	50.2°	1.59
PMOS	65dB	610M	3.63	56.8°	2.43

It can be seen, that both designs achieve all specifications defined at the start. The gain of the design with the NMOS current-mirror is with 70.7dB slightly higher than the gain of the design with the PMOS current-mirror. But in contrast the unity gain frequency is with 610MHz for the PMOS design higher than for the NMOS design. An obvious difference can be seen in the input-referred noise. A noise of $4.46nV/Hz^{0.5}$ is achieved with the NMOS current-mirror output. The noise achieved with the PMOS current-mirror is with $3.63nV/Hz^{0.5}$ lower compared to the NMOS setup. The phase margin of the PMOS design is slightly higher compared to the NMOS design. Here the results differ between 50.2° for the NMOS setup and 56.8° for the setup with the PMOS current-mirror output. In respect of the phase margin, the NMOS current-mirror setup has a disadvantage compared to the PMOS design. The reason for that is the fact, that not all corners achieve the specified value of 50° for the phase margin. A big drawback of the design with the PMOS current-mirror is the power consumption. Here the NMOS design achieves a much better result with a power consumption of 1.49mW. The power consumption of the circuit with the PMOS current-mirror output is 2.43mW which is almost double of the power consumption of the NMOS.

Another observation which can be done when comparing table 5.3 and 5.6 is that the output voltage of the inverter input stage of the NMOS current-mirror design is much lower than 750mV over all corners. This could also be one of the reasons why the phase margin is not high enough over all corners.

For comparing the performance of an amplifier, the figure of merit (FOM) plays an important role. The figure of merit can be defined by equation 5.8 [12]. This equation contains the most important parameters of an amplifier.

$$FOM = \frac{A_0 f_{ug} C_L}{P V_n C_{in}} \tag{5.5}$$

Here A_0 describes the open-loop gain of the operational transconductance amplifier, f_{ug} is the unity-gain frequency of the OTA. C_L describes the load capacitance at the output of the amplifier and C_{in} the input capacitance of the amplifier. P is the power dissipation of the OTA and V_n the input-referred white noise. Since for the design in this thesis, the input capacitance is not considered, the figure of merit will be defined to equation 5.6. This equation is similar to the FOM used in literature [12] and [15]:

$$FOM = \frac{A_0 f_{ug}}{P V_n} \tag{5.6}$$

The goal during amplifier design is to achieve a high figure of merit. To get this, the gain and unity-gain frequency should be as high as possible, while having a small power and a small input-referred white noise.

With using the values from table 5.7, the FOM for both designs can be calculated. For the design with the NMOS current-mirror, a FOM_N of $281\frac{GHz^{1.5}}{pWV}$ can be calculated.

$$FOM_N = \frac{3428 \cdot 582 \cdot 10^6}{1.59 \cdot 10^{-3} \cdot 4.46 \cdot 10^{-9}} = 281\frac{GHz^{1.5}}{pWV} \tag{5.7}$$

For the design with the PMOS current-mirror, a FOM_P of $123\frac{GHz^{1.5}}{pWV}$ can be calculated.

$$FOM_P = \frac{1778 \cdot 610 \cdot 10^6}{2.43 \cdot 10^{-3} \cdot 3.63 \cdot 10^{-9}} = 123\frac{GHz^{1.5}}{pWV} \tag{5.8}$$

Under consideration to achieve a high FOM, the design with the NMOS current-mirror output achieves better results. Here the FOM is double compared to the FOM of the PMOS design.

After all, both designs have advantages and disadvantages. The PMOS design achieves better results for the corner simulations with the drawback of having a higher FOM. The NMOS design achieves better results for the FOM with the drawback of not achieving a output voltage at the inverter input stage that is high enough. This results in a worse phase margin over the corners.

Chapter 6

Conclusion

In this master thesis two different fully-differential current-mirror amplifiers were designed. The first design was done with an inverter input stage and a NMOS current-mirror at the output. The second amplifier designed in this thesis was based on an inverter input stage and a PMOS current-mirror at the output. The amplifier designed in this thesis is based on the implementations in the papers [12] and [15] which was chosen after comparing different design architectures.

The design with the NMOS current-mirror output had a current gain of K = 3. The design achieved a gain of 70.7dB and a unity-gain frequency of 582MHz for typical simulations. The input-referred noise was $4.46nV/Hz^{0.5}$. The stability analysis showed a phase margin of 50.2°. The power consumption of the circuit was 1.59mW. The figure of merit could be calculated to $281\frac{GHz^{1.5}}{pWV}$. The results from corner simulations pointed out that the specified phase margin could not be achieved over all corners. All other specifications could be achieved over all corner.

For the implementation with the PMOS current-mirror output a current gain of K = 2 was used. The design achieved a gain of 65dB and a unity-gain frequency of 610MHz. The input-referred noise was $3.63nV/Hz^{0.5}$ and a phase margin of 56.8° was achieved during stability analysis. The power consumption was 2.43mW. The FOM was calculated to $123\frac{GHz^{1.5}}{pWV}$. The results achieved during all simulations showed that the specifications could be reached for all corners.

Comparison between both designs showed that both circuits have advantages but also drawbacks which needs to be considered.

6.1 Future work

Future work on the design includes improvements in the design of the circuit with NMOS current-mirror output. Here as special focus needs to be done to achieve a high enough phase margin over all corners. This is necessary before starting with doing layout.

Another focus needs to be done to the output voltage of the inverter input stage. This should be around 750mV. So it is necessary to increase it over all corners. Here investigation should be done to the transistors which builds the inverter as well as the current-mirror. Increasing the output voltage of the inverter input stage, could also increase the phase margin.

Investigation also needs to be done to have all transistors in active region over all corner to ensure a proper work of the amplifier.

Another work, which could be done is the modification of the design with the PMOS current-mirror output to achieve a higher figure of merit. Here a good starting point could be to decrease the power consumption of the design.

In this thesis, no focus was done on the common-mode feedback circuit. For simplification, an ideal OTA was used as simplified model. For the future, a common-mode feedback circuit could be designed to compare the results between an ideal and a real circuit.

When all simulations are done and ensured, that all specifications can be reached layout needs to be done, as well as post-layout simulations.

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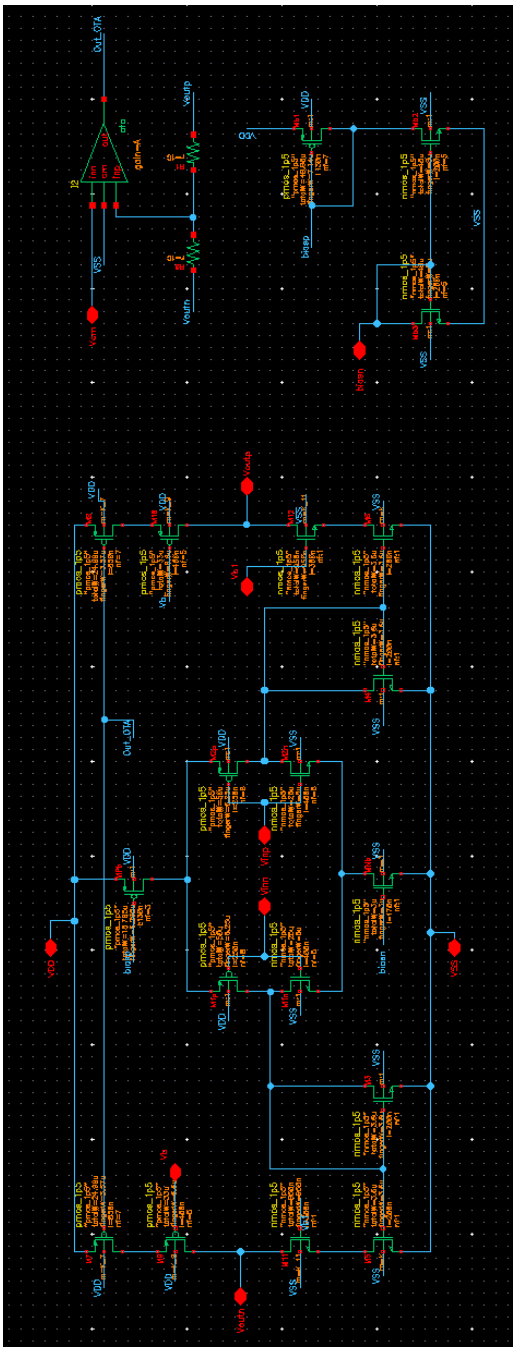
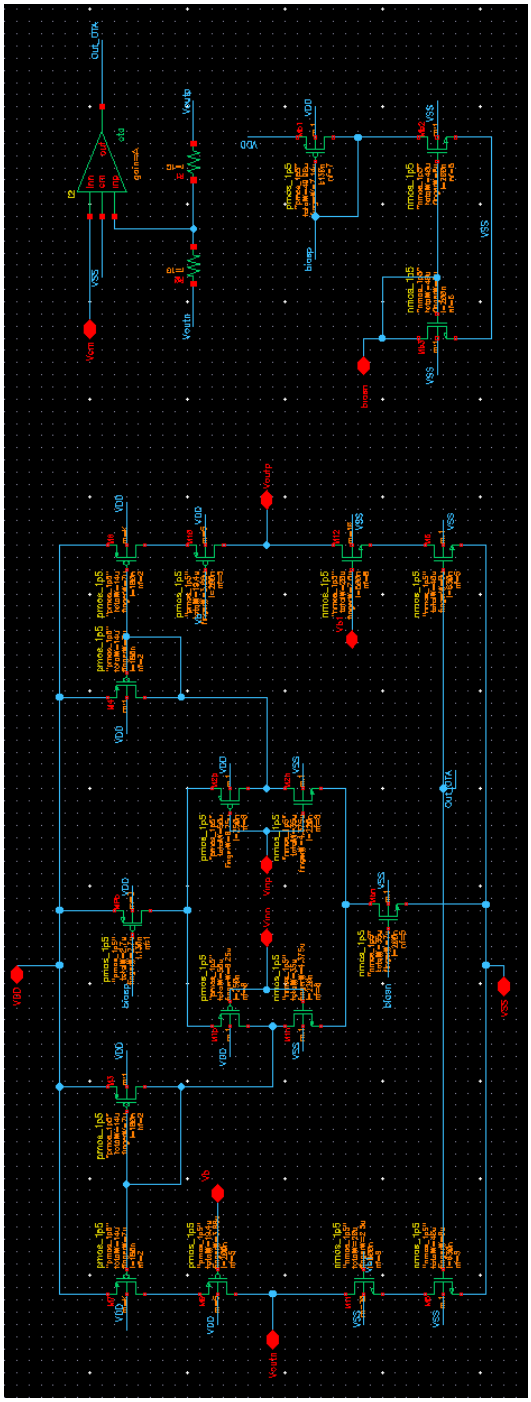
Appendix

A Amplifier with NMOS current-mirror output



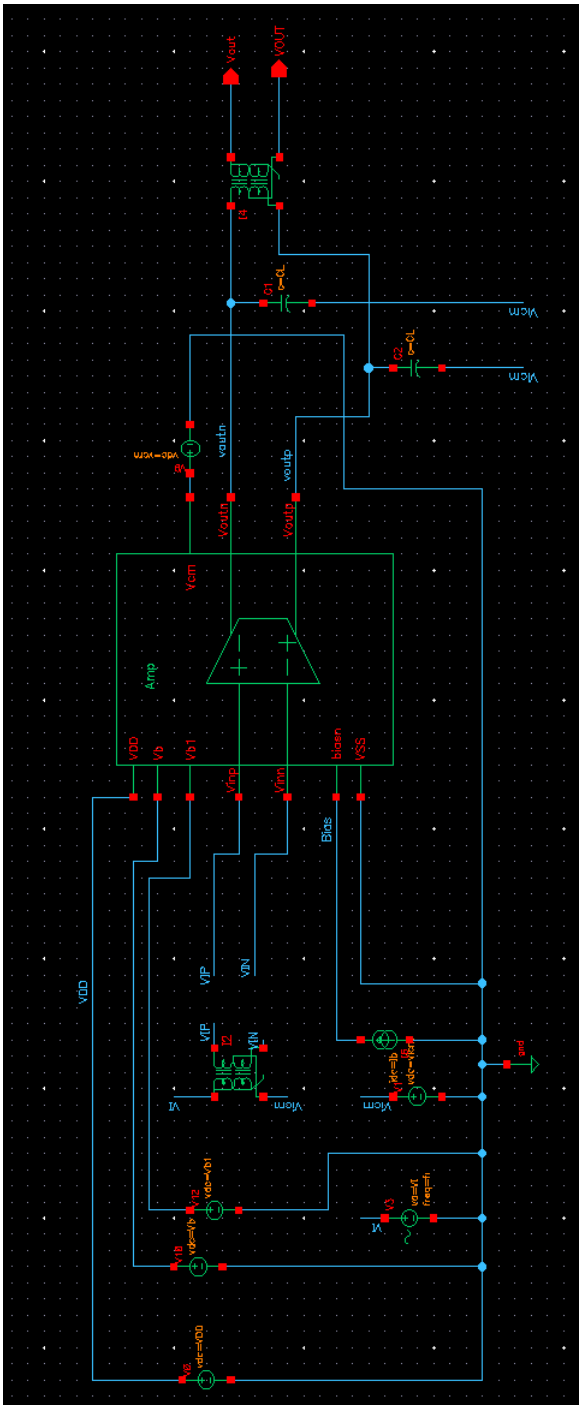
Virtuoso Schematic of the NMOS current-mirror output amplifier

B Amplifier with PMOS current-mirror output



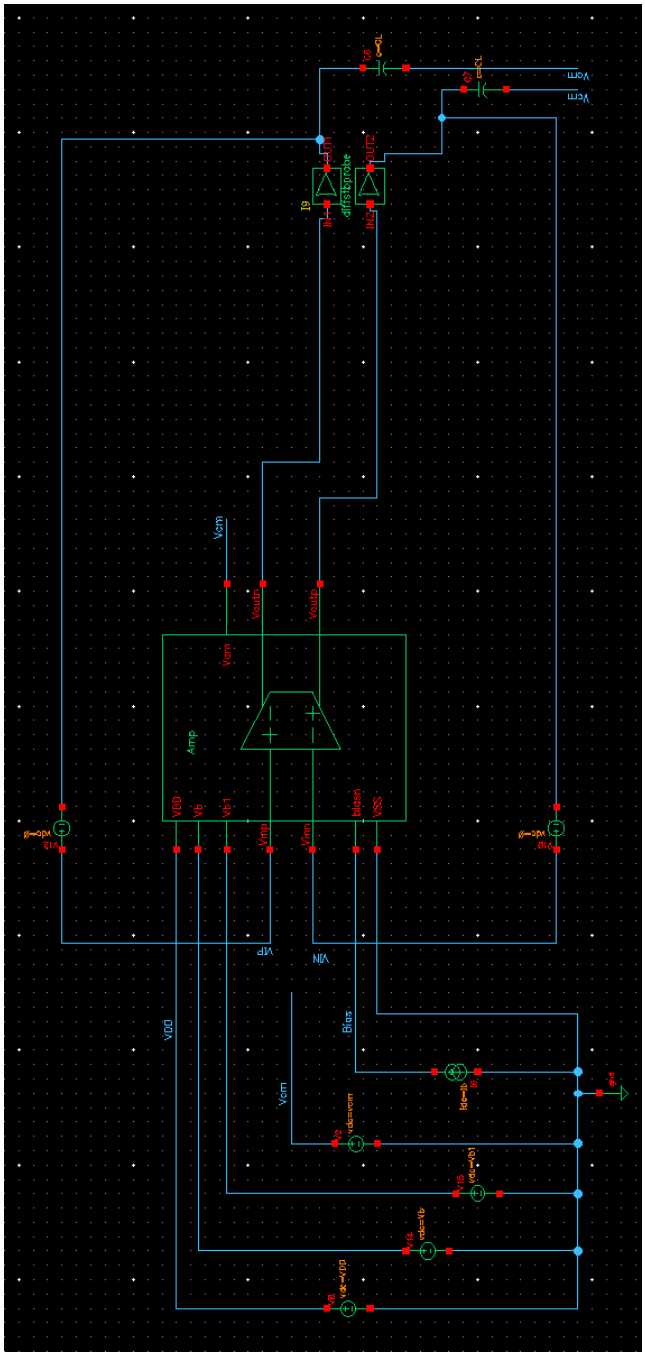
Virtuoso Schematic of the PMOS current-mirror output amplifier

C Virtuoso testbench for the open-loop simulations

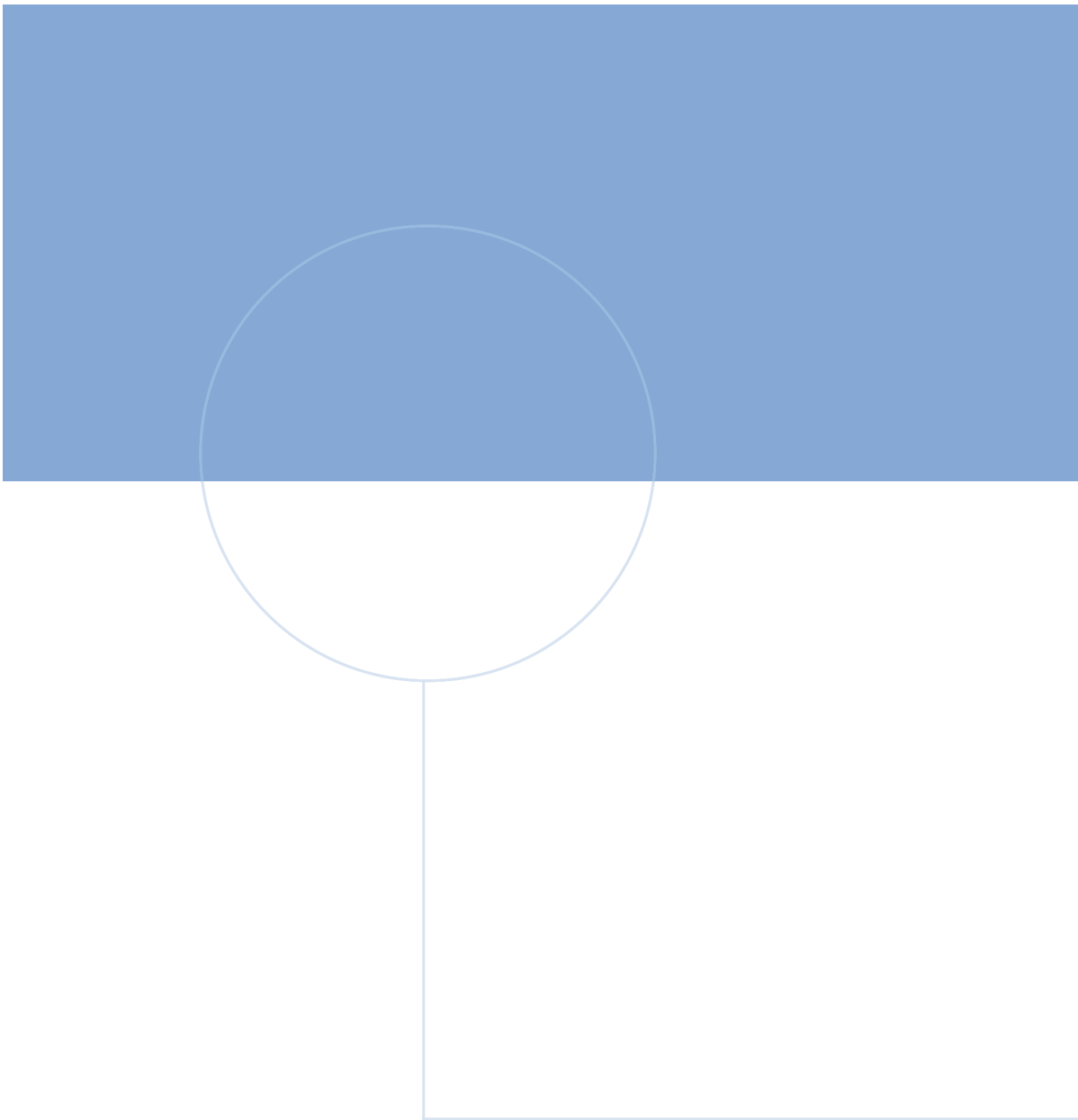


Virtuoso Schematic of the testbench for the open-loop simulations

D Virtuoso testbench for the stability simulations



Virtuoso Schematic of the testbench for the stability simulations



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