Discharge-based condition monitoring for electrolytic DC-link capacitors

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***Abstract*—Electrolytic capacitors are among the most vulnerable components in power electronic converters, risking their efficient and electrically stable operation. This is due to the decreasing capacitance under long-term stress. Thus, monitoring of the capacitance is imperative for ensuring proper converter's operation. This paper proposes a low-invasive method for condition monitoring of the health-status of DC-link electrolytic capacitors. The proposed method is based on the estimation of the remaining capacitance by analyzing the DC-link voltage decay during the shut-down phase of the power converter. In the proposed condition monitoring method, the temperature dependency and the physical behaviour of the electrolytic capacitors are investigated and compensated in the developed state of health estimation model. The proposed method has been validated experimentally using a full-scale power converter rated at 200 kW. The experimental validation includes accelerated degradation tests of capacitors under various temperature and pre-charge operating conditions, as well as field data from 153 converters, which are analyzed with the proposed method.**

***Index Terms*—Condition monitoring, dc-link capacitor, electrolytic capacitor, accelerated degradation test, field data analysis**

I. Introduction

DC-LINK capacitors are crucial components in power converters enabling not only voltage stabilization, but also fulfilling short-time energy storage requirements, either by serving load peaks or recovery energy in regeneration mode. Electrical energy supply to electromagnets at CERN is a typical power electronic converter application requiring both of these characteristics [1].

Electrolytic capacitors are among the most suitable technologies for DC-links due to their high volumetric and gravimetric capacitance density, as well as their cost-effectiveness. However, together with power semiconductors, electrolytic capacitors are the most vulnerable components of a power converter [2], [3]. Degradation of electrolytic capacitors is caused by the converter operating conditions, environmental conditions, and component quality. The most critical failure mechanism of electrolytic capacitors is evaporation of the liquid electrolytic. This has the effect of a reduced capacitance impacting the expected converter's electrical operation, but also of an increased equivalent series impedance (ESR) that results in higher losses. The degradation rate of electrolytic capacitors depends on the operating voltage and the operating temperature conditions [4]. In particular, the capacitor temperature is influenced by the ambient temperature and the internal temperature rise caused by the inner losses due to the ESR. The majority of degradation processes in electrolytic capacitors have some self-accelerating effects. If the ESR increases, the losses increase, thus having a flow-on effect on an elevated temperature which will increase the degradation rate. In addition to these two degradation mechanisms, capacitor failures might be caused by manufacturing errors and also by violating the maximum rated parameters during operation. Therefore, it is imperative to develop condition monitoring methodologies for assessing the health status of electrolytic capacitors in order to enable predictive maintenance for increasing the converter's reliability. Various methods have been proposed for condition monitoring (CM) of electrolytic capacitors.

Based on the data acquisition method for estimating the state of health (SOH), the CM methods can be classified as online [5]–[13], offline [14] and quasi-offline [4], [15], [16]. In online CM, critical data for assessing the SOH is acquired during the normal operation of the converter. On the contrary, offline CM is based on data measurements when the converter operation is stopped. Online CM has the advantage of providing information continuously without the need for stopping the converter's operation. However, a challenge is that additional sensors are required, which increase the overall system's complexity. Moreover, online measurements will be less accurate due to the impact of the semiconductor switching noise. On the other hand, offline CM might require disconnection of the power converter from the source and loads or even disassembling of converter's components for measurements. However, in critical applications these approaches might entail complicated procedures and extensive down-times. Still, in offline CM there is no requirement for placing sensors in the converter permanently. This allows a wide range of measurement options after the capacitor's disconnection. However, the acquired data is often processed manually, which imposes longer and costly SOH assessment procedures. An alternative approach to these measurement-based CM methods is to develop mathematical models that can estimate the SOH of capacitors under various accumulated stress conditions [17], [18]. More complex models have also been developed that are based on physics-informed modeling for estimating the remaining electrolyte's lifetime [3], [19]. However, stress accumulating methods can only estimate the degree of degradation, while they do not monitor the SOH of the actual components. The actual capacitor component can be influenced by manufacturing tolerances, which a mathematical lifetime model might not be able to represent accurately.

A solution to overcome the challenges of the online and offline methods is to develop quasi-offline CM methodologies (also referred as quasi-online) [20]. Quasi-offline methods are based on utilizing automated measurement procedures during

regular operation breaks of the converters. These measurements are performed using the existing sensors that are already incorporated in the converter for control and safety purposes, thus eliminating the need for increasing complexity. Quasi-offline CM methods are less sensitive to switching noise on the measured signals, since the measurements are acquired during shut-down stages of the converters. A quasi-offline CM method for monitoring the SOH of DC-link capacitor banks in accelerator power converters have been developed by the authors [21]. However, the impacts of temperature and charge history which are crucial for the accurate SOH detection have not been investigated. The contribution of this paper is on the development of a quasi-offline and non-invasive CM methodology of electrolytic capacitors. The proposed CM methodology incorporates modelling of the temperature and charge history in order to compensate for these effects on the measured capacitance, and to represent the SOH accurately.

The paper is organized as follows. Section II presents the different measurement techniques for CM in electrolytic capacitors. Then, the proposed optimal sampling methodology is analyzed in Section III and the converter for the evaluation is introduced in Section IV. Section V analyzes the non-linearity of electrolytic capacitors and the proposed compensation methodology is introduced in Section VI. The accelerated tests for verifying the proposed CM methodology are presented in Section VII. The results are presented and analyzed in Section VIII and further discussed in Section IX. Finally, the conclusions are summarized in Section X.

II. Capacitance Measurement Techniques for Detecting Degradation

At first sight, failures detection in capacitors can be performed through periodic visual inspections for mechanical destruction, deformation which indicates increased pressure, open pressure release vents or critical pollution levels. In addition, monitoring the weight of the capacitors can be used as an indication for loss of electrolyte [22]. However, even when all of these aspects look fine, the electrical performance may have been degraded. End of life (EOL) of an electrolytic capacitor is typically reached when the capacitance has dropped by 20% or the ESR has increased by 100% [8], [15], [23]. Which of these criteria is most critical depends on the application. Hence, it is imperative to measure either of these two electrical characteristics of the capacitors in order to assess the SOH. Electrical characterization of capacitors can be done by either injecting an alternating current (AC) or direct current (DC) as a test signal and measure the voltage response for estimating the capacitance and ESR.

A. AC Measurements

Due to the voltage polarity constraints in electrolytic capacitors, the AC test signal is superimposed to the DC voltage bias, while in some cases, the ripple of the regular operation can also be used as a test signal [9], [24]. However, the voltage ripple contains several harmonic components, and thus, it is more accurate to use a pure sinusoidal test signal to estimate the capacitor's complex impedance. In this case, the capacitor is connected to the test signal having a frequency f, and the complex impedance $\underline{Z}_C$ can be calculated from the measured voltage $\underline{V}_C$ and current $\underline{I}_C$ according to Eq. 1.

$$\underline{Z}_C = \frac{\underline{V}_C}{\underline{I}_C} = \mathrm{ESR} - i \cdot \frac{1}{2 \cdot \pi \cdot f \cdot C} \tag{1}$$

The real part of $\underline{Z}_C$ represents the ESR according to Eq. 2 while the capacitance can be calculated from the imaginary part according to Eq. 3.

$$\mathrm{ESR} = \Re(\underline{Z}_C) \tag{2}$$

$$C = \frac{1}{2 \cdot \pi \cdot f \cdot \Im(\underline{Z}_C)} \tag{3}$$

This equation represents how a commercial RLC-meter (Resistance Inductance Capacitance) can be used to measure the capacitance. Additionally, for this method, it should be noted that the frequency f of the test signal has an impact on the result, because at higher frequencies, the parasitic inductance of the capacitors becomes dominant.

For CM, the AC test signal is generated by an additional circuit or the converter itself. The way that this test signal is generated, depends on the converter topology [25]. For the different converter topologies $\underline{V}_C$ and $\underline{I}_C$ can be measured in a different way as well. For example, in the case of a modular multi-level converter, the phase load current is equal to the capacitor current and, hence, there is no need for additional current sensors [24]. For other converter topologies there is usually no sensor to measure the capacitor current.

B. DC Measurements

An alternative method to enable CM in capacitors, is to measure the capacitance using a DC test signal. In this method, a capacitor is charged or discharged with a constant current, I, for a time period t in order to add or subtract a certain amount of charge Q. With the measured voltage V the capacitance C can be calculated according to Eq. 4.

$$C = \frac{Q}{V} = \frac{I \cdot t}{V} \tag{4}$$

In practice, situations in which the DC-link capacitors are charged with DC, will occur at each startup sequence of the converter, while a discharging of the capacitors will happen at the turn off sequence. Therefore, such DC based methods are predesignated for quasi-offline CM. If the charging or discharging procedure is realised with constant current (e.g. due to a current limitation circuit) the capacitance can be estimated by Eq. 4. Moreover, the capacitor's charge and discharge with a resistor can be used for CM. The discharge voltage $V_C(t)$ is expressed by Eq. 5, where t is the time, V_0 the start voltage and τ the time constant. τ represents the capacitance C and the discharging resistor R.

$$V_\mathrm{C}(t) = V_0 \cdot e^{\frac{-t}{\tau}}; \quad \tau = R \cdot C \tag{5}$$

Rearranging Eq. 5 yields Eq. 6, from which τ can be calculated and C is derived.

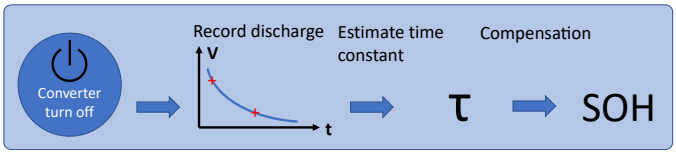

Fig. 1. Proposed CM principle

$$\tau = -\frac{t_2 - t_1}{ln(\frac{V_2}{V_1})}; \quad C = \frac{\tau}{R} \tag{6}$$

The resistance R represents the equivalent lump sum resistance in the capacitor's discharging path. This means that R also includes the ESR of the capacitor and possible other parasitic resistive components in the circuit. A method to decouple the ESR from the other resistors in the discharging path and estimate its value can be realized by activating different discharging paths [15].

Even though there are several powerful methods for DC-link capacitor CM as presented above, the goal is to implement the CM scheme by utilizing the existing hardware (e.g., sensors) of the power converter, to achieve better reliability with a similar cost factor. The authors propose using the existing set of sensors (for sensing voltage, current and temperature) that are primarily used for control and protection purposes in a power converter. Therefore, the need for additional sensors, which increase the design complexity of the system, is eliminated. In a typical converter design, there is one voltage sensor for measuring the DC-link voltage across the DC-link capacitors and there is no current sensor employed in the capacitor path. The main focus of this paper is to evaluate the CM potential of identifying the health status of the DC-link capacitors by monitoring the capacitor's discharge voltage decay during a controlled shut-down state of a power converter. By processing these voltage decay data, the time constant τ is estimated at regular time intervals, which can be used as a health status indication for the capacitance degradation.

The proposed CM method is applicable for all converters' DC-link capacitors which are discharged with resistors during the shut-down process. Due to this principle of the quasi-offline CM method, operation breaks of the converters are required. In most of the power converter applications, such operation interrupts will appear often enough for CM. For instance, in the case of a photovoltaic converter the SOH of the DC-link capacitor could be estimated each evening after sunset.

The proposed CM method estimates the SOH of the DC-link capacitor, by analyzing the discharge voltage decay after turn-off of the converter as depicted in Fig. 1.

With this straight forward approach according to Eq. 6, it is possible with only two voltage samples (i.e., red crosses in Fig. 1) to estimate the remaining capacitance. An optimal choice of the sampling time instants for the decaying voltage is crucial for improving measurement accuracy (Section III). Even under optimal sampling conditions, the capacitance estimation of electrolytic capacitors also depends on ionisation effects and temperature as will be analyzed in Section V. Therefore, in order to estimate the SOH, a compensation for temperature and ionisation effects is required, which will be presented in Section VI.

III. Proposed Optimal Sampling Method

In order to apply the CM methodology that was presented in the previous Section, it is vital to optimize the selection of the time-voltage pairs to minimizes the τ estimation error. In particular, the goal of the proposed approach is to minimize the impact of the limited accuracy and resolution of the voltage sensor used to measure the DC-link voltage discharge. The aim is to find the best time instants (i.e., time stamps) to sample the voltage during the discharge for calculating τ using Eq. 6. According to this equation, it is sufficient to acquire only two samples S_1 and S_2 with the voltages V_1 and V_2 and the corresponding time stamps t_1 and t_2, where the index 1 indicates the earlier sample. From the mathematical point-of-view, the voltage decay Eq. 5 is a memory-less function, which means that the two samples can be taken randomly within the discharging time period. It is crucial to investigate which is the best sample pair in order to minimise the error impact on τ estimation.

The timestamp $t_{\text{timestamp}}$ represents the sampling time in the dataset. However, the timestamp can also contain some errors due to filtering, analogue-to-digital conversion, network latency and the impact of preemptive multi-tasking systems. For this investigation, these errors are distinguished between a constant time shift t_{shift} which is equal among all samples and a random time error t_{jitter}. Both errors distort the real sampling time $t_{\text{samplepoint}}$ according to Eq. 7.

$$t_{\text{timestamp}} = t_{\text{samplepoint}} + t_{\text{shift}} + t_{\text{jitter}} \tag{7}$$

To analyze the failure impact of the time errors ($t_{\text{samplepoint}}$ and t_{shift}) the basic Eq. 6 is considered. In Eq. 6 the timestamps are used to calculate a time difference $t_2 - t_1$. Therefore, a constant time shift t_{shift} which will be equal at both samples will have no impact, whereas the jitter t_{jitter} will have. In a similar way, the voltage measurement is also analysed. The voltage sample V_{sample} which represents the real voltage V_{real} will contain a linear voltage error Err_{Lin} and an additive error V_{ErrAdd} according to Eq. 8.

$$V_{\text{sample}} = (V_{\text{real}} + V_{\text{ErrAdd}}) \cdot (1 - \text{Err}_{\text{Lin}}) \tag{8}$$

The linear error in the voltage measurement, Err_{Lin}, is caused by tolerances of voltage dividers and incorrect amplification factors, whereas the additive error, V_{ErrAdd}, is due to offset, quantification noise and further noise sources impacting the measurement. The two voltage samples are used for calculating the quotient V_2/V_1 according to Eq. 6. This means that a linear voltage error Err_{Lin} does not affect the measurement accuracy. Therefore, by incorporating the various error contributions, Eq. 6 can be extended to Eq. 9.

$$\tau_{\text{WithErr}} = -\frac{t_2 - t_1 + t_{\text{jitter}}}{ln(\frac{V_2 + V_{2\text{ErrAdd}}}{V_1 + V_{1\text{ErrAdd}}})} \tag{9}$$

The jitter is simplified to one t_{jitter} for both samples. It should be noted that the same error variance in both samples

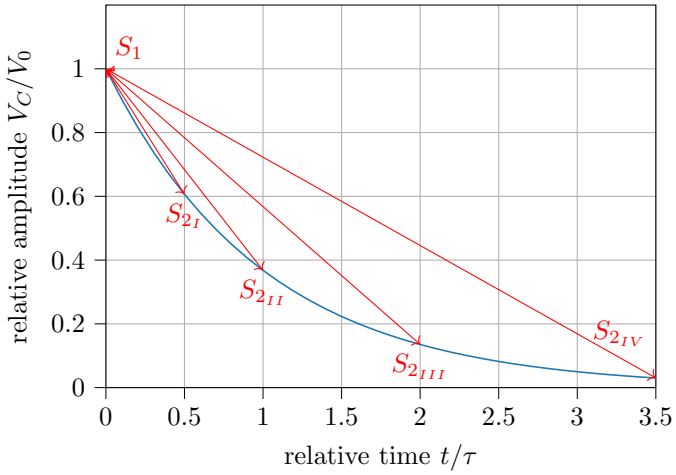

Fig. 2. Graphical illustration of the sampling options for the second voltage sample.

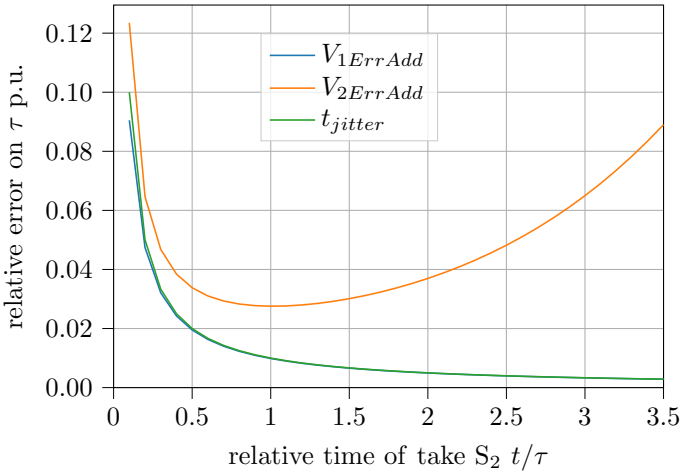

Fig. 3. Numerical results showing the impact of the errors on τ estimation by applying an error of 1% to different failure types.

is expected, because these errors come from the same sensing circuit. According to the nominator in Eq. 9, the impact of t_{jitter} becomes less relevant when the time difference between $t_2 - t_1$ is large. The noise level V_{ErrAdd} will not change during the discharge, but it will be more significant at late samples with lower voltage values. Therefore, the best approach is to acquire the first sample S_1 as early as possible at the beginning of the discharging process. However, the best choice for the second sample S_2 is not trivial. A certain time difference is required to get a significant voltage quotient V_2/V_1, but on the other hand, low voltages can only be measured with lower accuracy. The solution must, therefore, be based on a trade-off. The search of possible sample pairs is visualized in Fig. 2. In order to develop a general solution the voltage decay is plotted by using the relative voltage V/V_0 and the relative time t/τ.

To find this trade-off for the optimal S_2 sample, a simple numerical simulation on the errors has been conducted. The basis for this simulation is an ideal discharge voltage decay as shown in Fig. 2 according to Eq. 5 with a defined time constant of τ_{correct}. From this ideal voltage decay, the error-influenced time constant, $\tau_{withErr}$, is calculated according to Eq. 9 for different choices of the second sample S_2 (S_1 is always taken at $t = 0$). For each error assessment, only one error type is analyzed ($V_{1\text{ErrAdd}}$, $V_{2\text{ErrAdd}}$, t_{jitter}) by setting the two other types of errors to zero. In order to assess the voltage signal error ($V_{1\text{ErrAdd}}$, $V_{2\text{ErrAdd}}$), a constant offset error of 1% of the starting voltage V_0 was added, while for the time signal error assessment, an error of 1% of τ_{correct} was applied to t_{jitter}. From this τ_{withErr}, a relative error is calculated according to Eq. 10 and plotted in Fig. 3 for each error type.

$$\text{RelativeError} = \frac{|\tau_{\text{withErr}} - \tau_{\text{correct}}|}{\tau_{\text{correct}}} \tag{10}$$

From this plot, the most interesting observation is the sensitivity of the voltage error of the second voltage sample, $V_{2ErrAdd}$, that is visualized with the orange waveform in Fig. 3. This error has its minimum value for a time stamp equals to one τ. Thus, it makes sense to wait for at least one τ for taking the second sample. For samples taken later than one τ, Jitter t_{jitter} and additive voltage errors on the first sample $V_{1ErrAdd}$ have a smaller impact, while the additive error on the second sample $V_{2ErrAdd}$ becomes more significant again. It should be highlighted that the voltage error of both samples will have the same variance. If, in the specific application, the Jitter is significant compared to the voltage error, the optimal τ can be chosen a bit later to minimize this impact. In general, small deviations from the optimum sampling point will still deliver good results because the error impact function (according to Fig. 3) remains quite flat around the optimum sampling region. The negative impact on measurement accuracy due to an inadequate choice of sample pairs is not limited.

In addition to the presented optimal sampling method for the time and voltage pairs, filtering approaches can be applied. A digital low-pass filter of the DC-link voltage should be avoided because the shape of the decay will be distorted. Therefore, it is better to calculate the τ value first and filter it afterwards. For this purpose, several voltage samples at the very beginning and several samples around one τ should be taken to calculate several τ values. From these τ values the median is taken to be most insensitive to out-liners.

IV. Experimental Converter Test Setup

This section presents the design and operating principle of the power converter type for which the CM method has been developed. At the CERN complex, a large number of power converters of the same type comprise a converters family and they are used to energize the magnets of the transfer lines in CERN's accelerator complex. Transfer lines are used to connect accelerators or deliver beam to fixed target experiments. Electromagnets in these lines guide the beam to the upstream accelerator. The current in the electromagnets is supplied by high-power electronic converters. One example of such power converter is the SIRIUS converters family (Power **S**ystem for rap**I**d **R**egulation with **I**nternal controlled **U**nit of energy **S**torage) [1]. A typical SIRIUS converter (Fig. 4) consists of a grid connection through a transformer, a diode rectifier, a DC/DC boost stage for controlling the DC-link

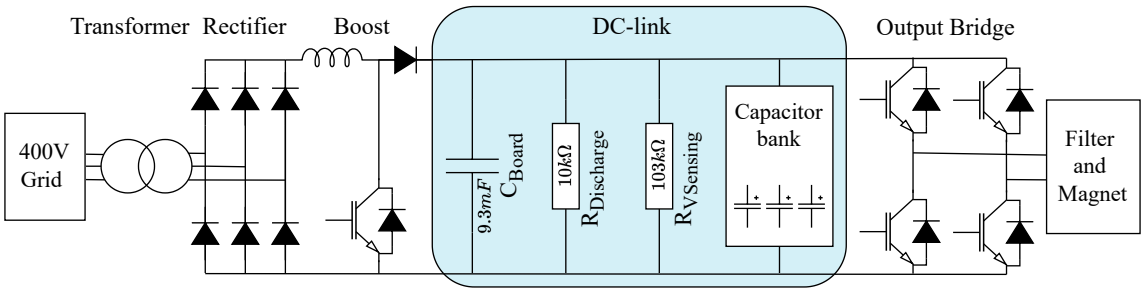

Fig. 4. Schematic of the SIRIUS accelerator converter with marked DC-link

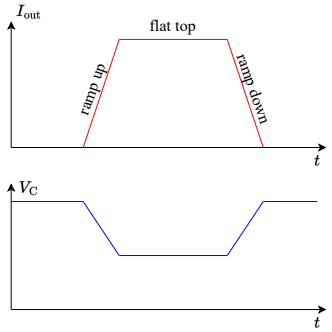

Fig. 5. Visualisation of the waveform of output current and DC-link capacitors

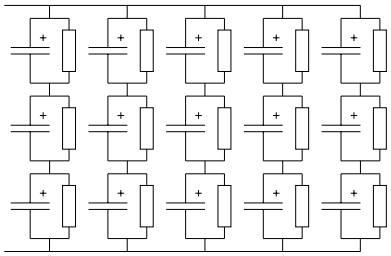

Fig. 6. Schematic of the capacitor bank. Each capacitor have a nominal capacitance of 29mF with a balancing resistor of 27k

voltage and a full-bridge converter stage which supplies high-precision current to the electromagnet through low-pass filters. Of particular importance is the DC-link capacitors bank that is able to supply and recover energy during operation. A film capacitor C_{Board} and a discharging resistor $R_{\mathrm{Discharge}}$ are connected close to the converter's current commutation path. Finally, a voltage divider to measure the voltage (modelled as R_{VSensing}) is also employed in SIRIUS.

In the transfer lines of the accelerators, the particle beam is only passing for a short time period. For this reason, it is only required to supply the high-precision direct current during the beam's transfer by magnetizing the electromagnets. The rest of the time the stored energy in the electromagnets is recovered by de-energizing them. A typical current profile supplied to the electromagnets through the SIRIUS power converters is shown in the top plot of Fig. 5. As shown from this figure, the current ramps up from zero to the flat top value causing a drop in the DC-link voltage, maintains a high-precision DC value for a certain time (flat top), and it finally ramps down by recovering the energy stored in the magnets. For the ramp-up

TABLE I
DATA OF THE ELECTROLYTIC CAPACITOR

Nominal capacitance	29 mF
Capacitance tolerance	0+30%
Typical ESR	5 mΩ
Nominal voltage	400 V
Maximal temperature	85 °C

process a high power, supplied by the converter is required, while during the ramp-down phase a significant amount of this energy is recovered and transferred to the capacitors. The energy recovered is reduced by the resistive losses in the converter and adjacent circuit components. This cycle is repeated every few seconds.

During the operation of the SIRIUS converters, the DC-link voltage, V_C, exhibits a significant drop in order to supply the required energy to the electromagnet, as shown in the bottom plot of Fig. 5.

This feature also dictates the need for employing a relatively large capacitive storage element on the DC-link. In the case of the SIRIUS this encompasses five pairs of three series-connected electrolytic capacitors as illustrated in Fig. 6 (see details of the capacitors in Table I).

Balancing resistors are required to balance the voltage across the series-connected capacitors. In practice, the grid side boost converter charges the capacitor bank to a DC-link voltage of 900 V, while the output full-bridge feeds the magnet with a current of up to 450 A. The pulse energy is delivered from the DC-link capacitors, with the effect of dropping down the voltage to 450 V.

The SIRIUS converter is a modular system which can consist of up to four sub-converters, namely bricks, which operate in parallel or series to enable reliable supply of the required output current [26]. Based on the operating constraints of specific electromagnets, each DC-link can be built with up to seven parallel capacitor banks in order to increase the energy storage capability. For the experimental validation of the proposed CM methodology in this paper, only the simplest configuration with only one brick and one connected capacitor bank has been utilized. With this, the DC-link can be simplified to a total capacitance of 57.6 mF connected in parallel with a discharging resistor of 6.04 kΩ. For the healthy case, a τ of 348 s is expected. In the case of several bricks, each brick has his own DC-link which is not connected with the other brick's DC-link. Therefore, each

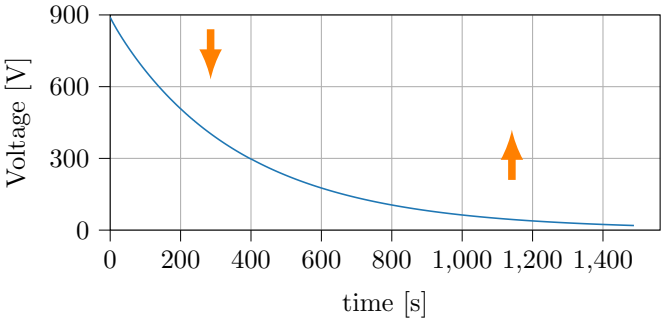

Fig. 7. Experimental measurements of the voltage discharge using the converter test setup that demonstrates the deviation of the decay form from the regular discharge according to expected behaviour (see Eq. 5)

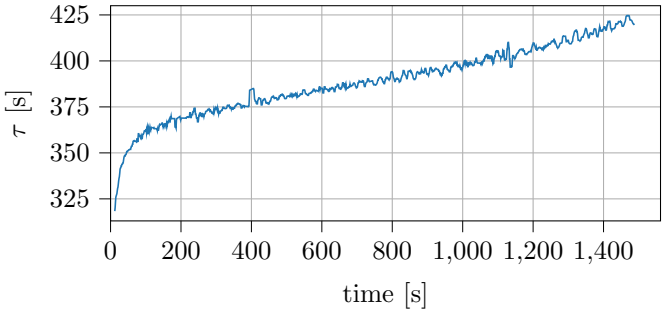

Fig. 8. Calculation of a local τ during the voltage decay to demonstrate the variation of the discharging rate

brick is monitored individually. A higher number of connected capacitor banks could be monitored in the same way, with the caveat that the expected τ will be different.

V. Behaviour of the Electrolytic DC-Link Capacitors

This section analyses the behaviour of the electrolytic capacitors during regular discharge through a resistor, and the impact of the operating and environmental conditions on the discharging process. The first subsection explains the general non-linearity of the voltage decay and the second subsection presents the experimental verification of the impact of temperature and charge history.

A. Non-linearity of discharge voltage decay

In this subsection, the validity of the voltage decay expression given by the common formula given in Eq. 5 is assessed. For this purpose, a simple experiment was performed in order to record the voltage decay of the SIRIUS converter. The converter was turned on with the effect that the DC-link was charged to 900 V. Then the converter was turned off again to initiate the regular discharge of the capacitors. The DC-link voltage was recorded with a sampling rate of 1 Hz using a FLUKE 289 multimeter. By analyzing the recorded data, it became clear that the discharge voltage decay could not be fully described by the common discharging formula (Eq. 5). The real discharging process is quicker at the first moments and slows down later on, as depicted in Fig. 7.

The linear discharge deviation can be analyzed by calculating local τ values for specific time periods of the voltage decay. The resulting τ development is plotted in Fig. 8. The time axis in Fig. 8 describes the time when the second sample, S_2 for τ calculation was taken (S_1 was taken 10 s earlier). That is the reason why no values are available at the beginning of the graph. This plot shows that during the discharging process, the discharging rate decreases (corresponds to increasing τ values in Fig. 8). The values for τ increase further for later sample pairs than plotted here. This is not relevant because the corresponding low voltages cannot be measurable accurately enough, as explained in Section III.

The main reason for this behaviour is the ion distribution in the electrolytic capacitor. The electrode surface inside the electrolyte of the capacitor is made of a very porous material in order to create a big active surface. This is the basic principle of electrolytic capacitors that enables a high capacitance density. Charge is stored in the form of ions on the outer surface but also in the holes of the porous electrodes material. The charge exchange (i.e., during charging or discharging of the capacitor) appears on the outer surfaces of the porous material and the ion's movement in the pores will be initiated with a delay. This ionic inertia explains why the discharge is first quicker and then slower than expected [27]. This time variant behaviour of electrolytic capacitors has also been described by the authors of [28] where they develop models to explain this behaviour in the time and frequency domain for the short term effects.

In the perspective of CM this ion-distribution has further side effects. In particular, the discharge voltage decay is no longer a memory-less function as stated above. The choice of the sample pair delivers different results for the same discharge voltage decay. Moreover, the ion distribution before the discharge becomes relevant, as the ion distribution itself depends on the charge history. In a practical application, the ion distribution depends on the time period that the converter has been in operation before the discharge starts. The deviations of the capacitor voltage during operation has an impact on the discharge voltage decay. Additionally the capacitance depends on temperature [4], [29].

B. Laboratory setup to verify the discharge behaviour

In order to verify the impact of the temperature and charge history on the discharging process of the capacitors, the SIRIUS converter presented in Section IV has been used. The goal of this experimental procedure is to verify the existence of these effects, and to quantify their relevance for CM. A limitation of the experimental procedure is that it will not be possible to measure exactly the inner temperatures of the capacitors and to use the full charge history of the capacitors in the application, which is in principle infinitely long. Therefore, a simplification has been adopted for the test setup. To emulate the temperature and charge history, the ambient temperature of the capacitors is adjusted by placing the capacitors bank in a thermal chamber (Memmert TTC 256). Instead of a detailed charge history, for a constant DC-link voltage of 900 V the on-time of the converter was also varied before the discharge starts.

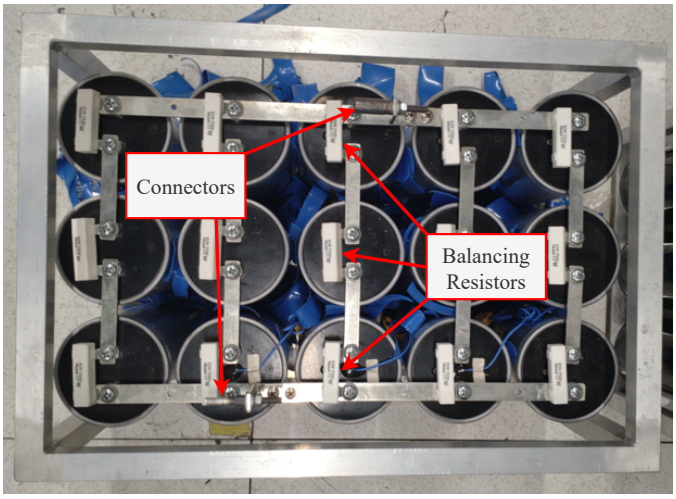

Fig. 9. Capacitor bank with connected balancing resistors

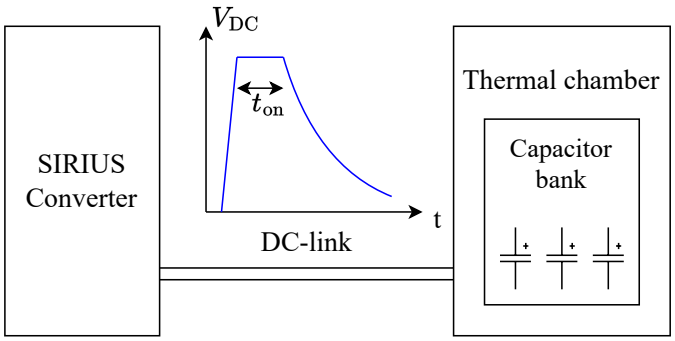

Fig. 10. Block diagram of the experimental setup to verify the temperature and on-time dependency.

For these experiments, only the grid side of the SIRIUS converter (Fig. 4) was used. The grid side (i.e., transformer, diode rectifier and DC/DC boost converter) was used to charge the capacitors to the nominal DC-link voltage of 900 V and kept it constant until the converter was turned off. Then the capacitors were discharged through the discharging and balancing resistors. The output full-bridge converter of SIRIUS remained connected but it was kept inactive and, thus, did not influence the tests. The capacitors bank itself (Fig. 9) was placed in a thermal chamber to adjust the ambient temperature as depicted in Fig. 10. Fig. 11 shows the SIRIUS converter and the thermal chamber. The voltage is measured with resistors and a LEM LV25-P/SP5 current sensor, in the same way as it is realized in the field application. Additionally, to acquire more accurate data, the voltage was recorded with a FLUKE 289 multimeter. For both measurement methods, the sampling frequency was set to 1 Hz.

The goal of these experiments was to emulate the field conditions as closely as possible. Therefore, the test temperature range exceeds slightly the expected field temperatures to achieve a good coverage. Very excessive test temperatures should be avoided because they will cause significant degradation of the capacitors.

Thus, the test was conducted at internal chamber temperatures of 10 °C, 25 °C and 50 °C. These three temperatures were chosen to reproduce the ambient temperature conditions of the application. It is a good compromise to check if the temperature dependency is linear. To guarantee a uniform temperature distribution, the air circulation functionality of the thermal chamber was activated. Before the tests, to ensure that the entire capacitor reached the set temperature after a temperature step, a series of discharges were captured, until the discharge voltage decay did not change anymore. At that point, it was assumed that the capacitors had reached the desired temperature. For the given capacitor under test, this preconditioning lasted for several hours.

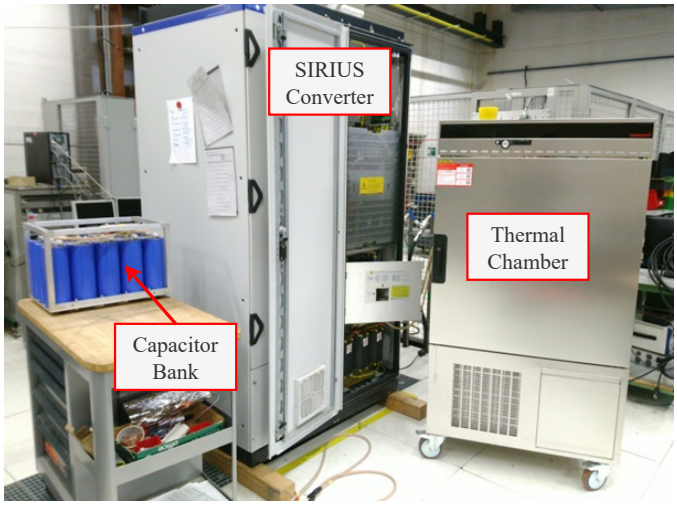

Fig. 11. Laboratory setup with SIRIUS converter, thermal chamber and capacitor bank. For the experiments the capacitor bank is placed inside the thermal chamber and connected with the converter's DC-link.

To emulate the charging history effect, discharging experiments with different on-times for the capacitors' pre-charging were performed. These on-times vary from several seconds to several hours. To simplify the big amount of data from the voltage decays, a single τ value was calculated according to the method of optimal τ (Section III). Some information will be lost by processing the decays in this way, but it enables a graphical representation of on-time and temperature dependency as shown in Fig. 12 with one τ value per discharge. The temperatures are represented with different colours. On the x-axis, the on-time in logarithmic scale is shown and on the y-axis the τ value in linear scale.

From this plot, it is observed that the τ increases with temperature and the dependency is quite linear. On the other hand, the on-time have a logarithmic impact on τ. Moreover, it becomes clear that there is some saturation effect on τ for very long on-times.

There is an alternative way to explain the on-time dependency. The on-time is just a representation of the more complex charge history. The discharge behaviour of a capacitor is mainly dependent on the voltage just before the discharge starts. In the case of electrolytic capacitors also the time before the discharge is relevant. Therefore, it is paramount to assess the impact that each part of the charge history has on the τ calculation. This analysis is also supported with the

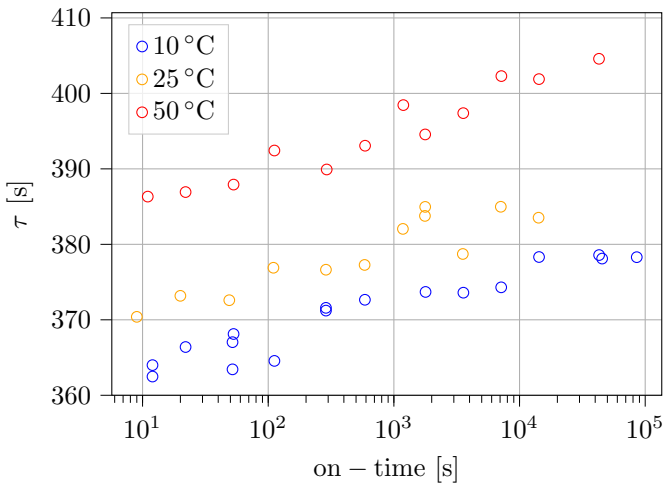

Fig. 12. Visualisation of the measured on-time and temperature dependency of τ for capacitors without degradation.

TABLE II
IMPACT OF CHARGE HISTORY ON τ ESTIMATION FOR A CAPACITOR TEMPERATURE OF 10 °C

on-time [s]		τ [s]	relτ	Δ on-time [s]	rel$\Delta\tau$
12		364.0	96.1%	12	96.1%
53	≈ 1 min	368.1	97.2%	41	1.1%
288	≈ 5 min	371.6	98.2%	235	0.9%
1787	≈ 30 min	373.7	98.7%	1499	0.6%
14296	≈ 4 h	378.3	99.9%	12509	1.2%
42976	≈ 12 h	378.6	100%	28680	0.1%

experimental results, which are presented in Table II for the temperature of 10 °C. In this table, the calculated τ is listed for various on-times. Then τ gets normalized rel$\Delta\tau$ with the maximal reached τ (=378.6s in 12h on-time = 100%) as shown in Table II).

From the analysis presented in Table II, it is possible to calculate which on-time period is responsible for which percentage of τ. As it can be seen, the last 12 s before the discharge commences have the most significant impact on the τ value (96.1%). The impact of the previous 41 s will have a contribution of 1.1% on τ, while the previous 4 min will contribute by 0.9%. It can also be done in a cumulative way as it is done in column $rel\tau$. Here it should be noted that the results shown in Table II are just approximations because they only depend on a subset of the data created by removing outliers, and assume that the maximum ion saturation is reached after 12 h of operation at 10 °C.

The knowledge of the impact of the charge history is of relevance for CM in different aspects. Firstly, it demonstrates which part of the charge history is relevant for accurate CM. Additionally, it shows that changes in the DC-link voltage shortly before the discharge starts will have the most significant impact on the discharge decay. This is especially critical when there was a failure which lets the converter trip and the discharge decay is recorded. Such converter trip might therefore provide data that cannot be applied with the proposed CM methodology. This issue will be discussed further in Section VIII-B.

VI. PROPOSED COMPENSATION METHODOLOGY OF CHARGE HISTORY AND TEMPERATURE EFFECT

Due to the significant impact of temperature and charge history on the discharge decay, it is vital to develop a compensation methodology for these effects in order to estimate τ accurately. With the use of CM, the main goal is only to detect capacitance decrease due to degradation, independently of the operating and environmental conditions. Thus, it is imperative to represent the SOH of the capacitor bank with a temperature and on-time compensated τ. A compensation function which compensates the temperature T and on-time t_{on} effects on the measured value τ_{measured} shall be developed so that a corrected $\tau_{\text{corrected}}$ can be calculated according to Eq. 11.

$$\tau_{\text{corrected}} = \tau_{\text{measured}} \cdot \text{Correction}(T, t_{on}) \tag{11}$$

Instead of directly searching for the correction function $\text{Correction}(T, t_{on})$, a function to predict the values of τ from temperature and on-time should be developed. The aim is to calculate the expected time constant $\tau_{\text{predicted}}$ from a constant τ_{nominal} value for a given on-time t_{on} and temperature T combination according to Eq. 12.

$$\tau_{\text{predicted}} = \tau_{\text{nominal}} \cdot \text{Predictionfactor}(T, t_{on}) \tag{12}$$

The prediction function $\text{Predictionfactor}(T, t_{on})$ is estimated from the plotted values in Fig. 12. The temperature can be represented with a linear temperature coefficient Coeff_T. The on-time dependency is estimated in the logarithmic pane. It can be represented with a linear function (defined with the parameter $\text{Coeff}_{t_{on}}$) which saturates at t_{on_max} for increased values. This saturated on-time t_{on_sat} parameter is given by Eq. 13. The Prediction factor can now be expressed as Eq. 14.

$$t_{on\_sat} = \min(t_{on}, t_{on\_max}) \tag{13}$$

$$\begin{aligned}\text{Predictionfactor}(T, t_{on\_sat}) = 1 &+ \text{Coeff}_T \cdot (T - T_{ref}) \\ &+ \text{Coeff}_{t_{on}} \cdot \big(\log_{10}(t_{on\_sat}) \\ &- \log_{10}(t_{on\_max})\big)\end{aligned} \tag{14}$$

The coefficients are estimated from the measurement data and presented in Table III. The estimation of the coefficients was done manually. The temperature of 10 °C was chosen as the reference temperature T_{ref} (other temperatures would also be feasible). Then the maximal reached value for τ at the reference temperature was chosen as the nominal time constant τ_{nominal}. According to Fig. 12 the maximal on-time t_{on_max} when the τ values become constant was derived. From this saturation point t_{on_max} the gradient $\text{Coeff}_{t_{on}}$ in the logarithmic pane was estimated to cover the on-time dependency for on-times $t_{on} < t_{on\_max}$. Finally, the temperature coefficient Coeff_T was estimated from different τ values with different temperatures but equal on-time.

With Eq. 12, Eq. 14 and the coefficients summarized in Table III, it is possible to predict the τ values for given on-time and temperature combinations. The predicted and measured values of τ are plotted in Fig. 13, which demonstrates the validity of this prediction.

TABLE III
COEFFICIENTS FOR TEMPERATURE AND ON-TIME COMPENSATION

Coefficient	value	unit
T_{ref}	10	°C
τ_{nominal}	378.3	s
$t_{on\ max}$	14296 ≈ 4 h	s
$\text{Coeff}_{t_{on}}$	0.01263	$1/\log_{10}(\text{s})$
Coeff_T	0.001575	1/°C

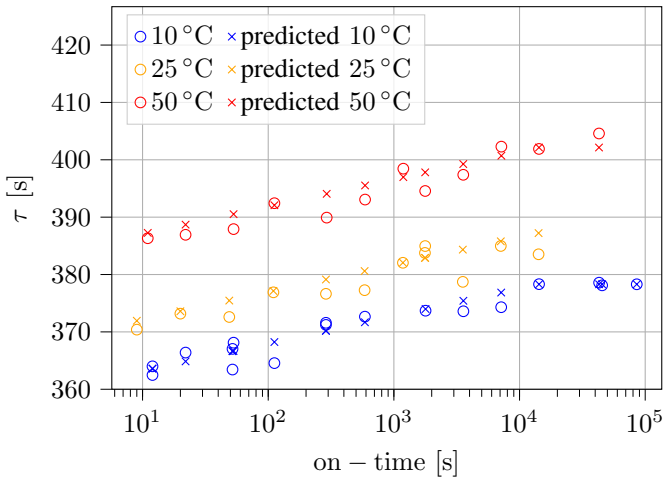

Fig. 13. Comparison of the measured and predicted values of τ

However, the goal is to find a correction function $\text{Correction}(T, t_{on})$ to compensate the temperature and on time effects. This can now be realized in a straight forward way by using the reciprocal value of the prediction factor. With this, Eq. 11 evolves into Eq. 15.

$$\tau_{\text{corrected}} = \tau_{\text{measured}} \cdot \frac{1}{\text{Predictionfactor}(T, t_{on})} \tag{15}$$

Therefore, it is considered accurate to compensate the temperature and the on-time using Eq. 15. With this correction effort, the capacitance-related SOH can now be represented with $\tau_{corrected}$. This compensation is applied to the data acquired from the experiments at 50 °C and 10 °C and plotted together with the uncompensated data in Fig. 14. In this plot, the τ values are normalised to 100%, which represents the capacitance of a healthy capacitor bank. Alternatively, it is possible to use this $\tau_{corrected}$ value and calculate a percent value. For example, if the EOL criterion has been set to 80% of the capacitance at the beginning of the useful capacitor's lifetime, this will correspond to 0% of SOH. However, the specific EOL criterion depends on the application that requires a certain capacitance.

It has been demonstrated that the proposed compensation methodology can take into account the on-time and temperature dependencies. Yet, for the compensated data points no temperature and on-time dependency are visible anymore. This compensation factor method is a versatile tool that can be applied to different capacitor bank sizes or to capacitors from different manufacturers in the same manner. The temperature compensation is implemented by considering the temperature difference with respect to a reference temperature, according

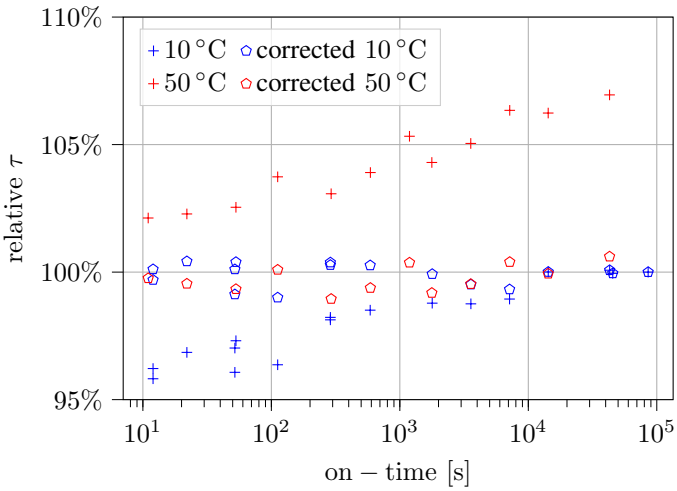

Fig. 14. Example of normalized capacitance with and without compensation

to Eq. 14. This reference temperature represents an operating temperature of the capacitor. Therefore, the temperature coefficient becomes less sensitive on possible production tolerances compared to a temperature coefficient which is estimated based on the absolute temperature.

VII. ACCELERATED DEGRADATION TEST

To verify the CM method experimentally with real data, an accelerated degradation test was performed. In particular, the full-size capacitors bank was degraded in order to repeat the same verification tests with the converter as they had been done for the healthy case in Section V-B. In the first part of this Section, the designing criteria for an accelerated degradation test are analyzed followed by the presentation of the implemented degradation test.

A. Designing the accelerated degradation test of electrolytic capacitors

Degradation of capacitors is developed under long-term converter's operation in the field. However, relying on long-term operation of converters to acquire degradation data test is usually impractical, especially for recently commissioned converters. A solution for assessing the feasibility of CM methodologies is to conduct accelerated degradation tests in order to degrade capacitors within shorter times. An alternative way to do this is to utilize historical data of capacitors degradation from the SIRIUS converters. However, such data is not available for these converters hence considering an accelerated degradation test.

In general, these tests are classified into accelerated degradation tests within or out of manufacturer specifications. The aim of triggering degradation within the manufacturer's specifications is to get the most realistic representation of performance decrease over time. The manufacturer provides a likelihood of failures under these conditions for a defined time. Because of its low likelihood the imposed stress level needs to be applied for a longer time period before a failure occurs or an EOL criterion is reached. Therefore, it is desired to exceed the load level over the specified ratings by the

manufacturer in order to see significant degradation or failure in the capacitor within a reasonable test time. In general, it is a trade-off between finding an appropriate stress level to shorten the test duration and triggering the desired type of degradation. For this, it is required to understand the effect of stress on the component.

The lifetime of electrolytic capacitors depends on the operating voltage and temperature, where the temperature itself depends on the ambient temperature and the electrical losses in the capacitor. Usually, the expected lifetime, L_{expected}, is estimated according to Eq. 16 [30], [31].

$$L_{\text{expected}} = L_0 \cdot \left(\frac{V_{\text{Design}}}{V_C}\right)^n \cdot 2^{\left(\frac{T_{\text{Design}} - T_C}{10}\right)} \tag{16}$$

The expected lifetime L_{expected} depends on the basic lifetime L_0, a voltage term and a temperature term. The voltage dependency is determined by the operating voltage V_C, the designed rated voltage V_{Design}, and a form factor n, which is dependent on the construction of the capacitor (usually in the range of 0 .. 2.5). The temperature term is defined by the designed maximum temperature T_{Design} and the operating temperature T_C. Eq. 16 demonstrates that the lifetime halves when the temperature increases by $10\,^{\circ}\text{C}$. In general Eq. 16 is only valid for approximations under the designed operating conditions and thus it is not applicable for discharged capacitors with $V_C \approx 0$, which does however still degrade.

An example of an accelerated degradation test for electrolytic capacitors within specifications is presented in [32]. In this case, the EOL criteria were not reached during the 5000 hours of the test for all samples. Instead, a slight, almost linear, increase of ESR was measured. In the first 1000 hours of the test the capacitance had still increased and started to decrease only after 3000 hours.

Alternatively, the test can also be performed under very highly accelerated conditions, as it is studied by [31], where the test duration is shortened down to 250 hours by increasing the temperature with the effect that all samples reached an EOL criterion. In this test, the capacitance drops very quickly in the first hours after which it falls slower and almost linearly. Only after 150 hours the capacitance drop rate increases again.

Another example of an out-of-specifications test is presented in [3]. In this case, the applied thermal stress was chosen lower while an almost linear decrease of the capacitance of approximately 10% was detected after 3500 hours.

By comparing the above results, it becomes clear that a different degradation mode was triggered in all tests. Due to the very high temperatures, the highly accelerated test has mainly triggered electrolyte vaporisation with the effect of quick capacitance drop. In the within-specifications test, first an increased capacitance is observed, before the electrolyte loss has become the dominant degradation mechanism. An alternative way to shorten the required test time is to puncture the capacitors before the accelerated ageing test to increase the electrolyte vaporisation rate even more [30].

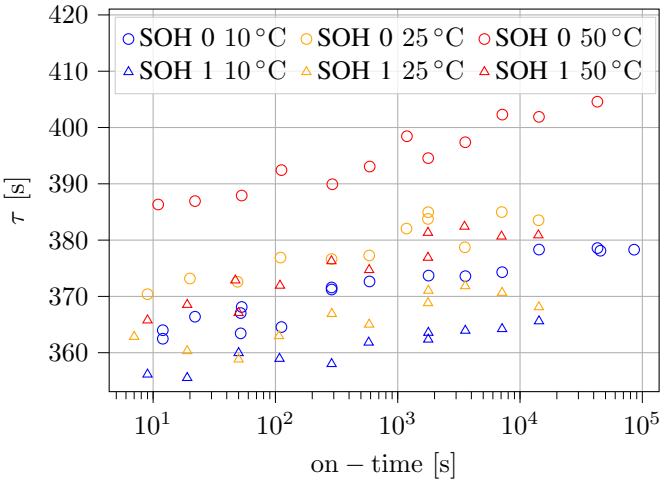

Fig. 15. Measurement results of τ as a function of on-time and at various temperatures under the accelerated degradation tests (SOH 1) compared with the healthy data (SOH 0).

B. Utilized accelerated degradation test

The highly accelerated test method was chosen because the proposed CM method is only sensitive to capacitance decrease. The puncturing method was not used to avoid electrolyte loss (i.e., changing SOH) during the verification test. The exact loss of SOH was not that relevant for this test. The goal of the accelerated tests was to collect data in order to compare the capacitance decrease after a degradation step with the healthy condition.

For this test, the capacitors bank was placed in the same thermal chamber as it was used for the characterization of the capacitors. The degradation was realized by exposing capacitors designed for maximal $85\,^{\circ}\text{C}$ for several hours to temperatures of up to $150\,^{\circ}\text{C}$. The capacitors bank has remained connected to the converter and supplied with a DC voltage of $900\,\text{V}$ while applying the thermal stress. In this way a series of discharges have been conducted in order to monitor the changes in capacitance during the test. With this, the capacitors were additionally exposed to a small voltage stress. The self-heating effect due to the current which is flowing during charging and discharging is negligible. After this thermal degradation, the characterisation test was repeated as described in Section V-B. The data of the degraded capacitor bank (index SOH 1) can now be compared with the healthy capacitor bank (index SOH 0) as illustrated in Fig. 15.

This plot shows again that the τ has decreased for all temperature and on-time cases, which means that the thermal stress had triggered electrolyte vaporisation with the effect of a reduced capacitance. The difference between the healthy capacitors and the capacitors after exposed to thermal stress is more significant at higher temperatures. Moreover, the results show that information about the temperature and on-time is relevant for distinguishing the data of degraded and healthy capacitors.

VIII. Results

This section presents and analyzes all the results by applying the proposed CM method to the accelerated ageing test data,

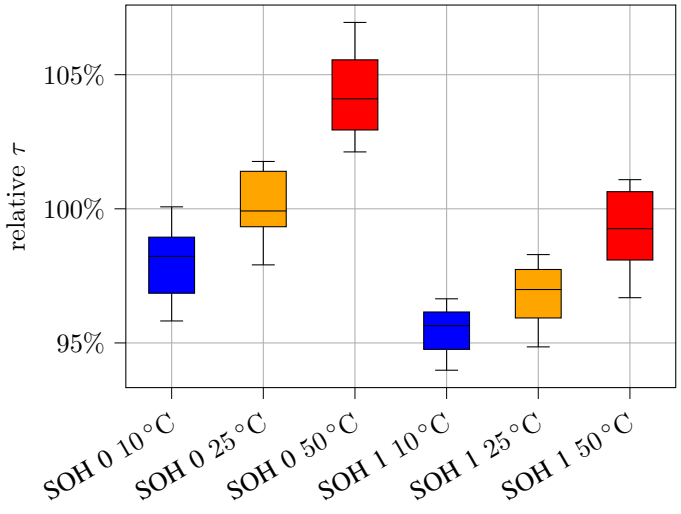

Fig. 16. Box plot of the healthy (SOH 0) and degraded (SOH 1) normalized τ data without applying the temperature and on-time compensation.

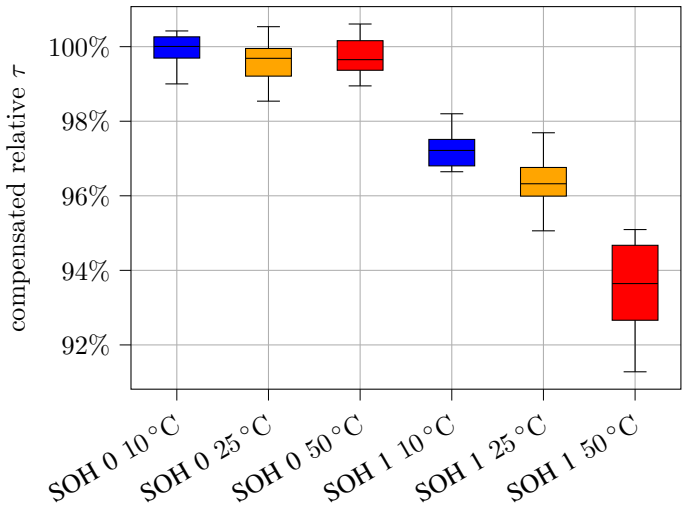

Fig. 17. Box plot of the healthy (SOH 0) and degraded (SOH 1) normalized and corrected τ data when applying the temperature and on-time compensation.

as well as field data.

A. Verification with accelerated degradation data

This subsection presents the results on applying the compensation method to the recorded data with the degraded capacitors bank. This means that the corrected τ value shall represent only the SOH of the capacitor independently of on-time and temperature. In Fig. 14 of Section VI the application of the compensation method has been presented for healthy data. This compensation is now applied to all data of the healthy and degraded capacitors. To increase the visibility of the high amount of data points a box plot is used, where each batch contains all on-times for a given temperature and SOH combination. For comparison clarity, the results are first presented without compensation in Fig. 16 and with applying the compensation in Fig. 17.

As shown in Fig. 17, for the healthy case (i.e., SOH 0) the compensation works very well and not much scattering is remaining on the data. In the case of degradation (i.e., SOH 1) the compensation performance is reduced. However, according to this plots the CM system is now able to clearly distinguish between data of the healthy and degraded capacitor banks for all temperatures and on-times successfully. All compensated relative τs of the degraded capacitors are of lower value than the healthy ones.

B. Verification of the CM method with field data

At CERN 153 SIRIUS converters with a total number of 251 bricks are employed. With the proposed CM method, the SOH of the capacitor banks employed in all these SIRIUS converters have been monitored. To achieve this, a data acquisition script runs continuously and records the discharge voltage decays every time a converter trips or is regularly shut down. Additionally, the converter status and temperatures of some auxiliary circuits are recorded. The capacitor ambient temperature is measured with sensors installed on an auxiliary circuit with negligible self-heating. The status data allow to reconstruct the on-time and discern between converter trips and a regular shutdown. This is relevant because in the case of a converter's trip, a failure might have occurred which might cause significant charge exchange with the capacitor bank. This will influence the charge history at the most sensitive time before the discharge starts (see Section V-A). Therefore, only data from regular shut downs should be considered for CM. The converter's status data also contain data of very short operation interruptions, in which the DC-link capacitors are just discharged partially until the converter is turned-on again. In this case, the discharge is sometimes not deep enough to calculate an optimal τ using the proposed CM methodology. Such partial discharges will impact the charge history in an unclear way. Therefore, it is decided to only use data when the last discharge was almost complete (i.e., voltage reached $<20\,\mathrm{V}$) or the on-time of the capacitors bank was at least longer than $>12\,\mathrm{h}$.

In the first step just the optimal τ value is calculated from the discharge voltage decay if the discharge was deep enough. These uncompensated τ values are plotted in the top graph of Fig. 18. In the bottom plot the data is on-time and temperature compensated and the cases with unclear charge history as described above are removed. In this plot the turn-off cases are plotted in brown and the trip cases are shown in violet.

In the bottom plot of Fig. 18 a slight trend for decreasing capacitance seems to be visible. However, for most of the converters, no clear trend is visible yet, since the converters are still in the early phase of their lifetime. In some cases, the corrected τ value still increases. Increasing capacitance in the first period of the lifetime might be possible. This effect was also recognized for several samples in the within-specifications test according to [32], which was discussed in Section VII-A. It is expected from the converter design that in these 3 years of operation not much degradation should occur. One of the reasons is the underrated usage of the converters in order to increase their reliability. However, the data acquisition is still in operation and degradation will become visible in the future, making imperative the use of the proposed CM methodology. In particular, a decreasing trend in the observed compensated

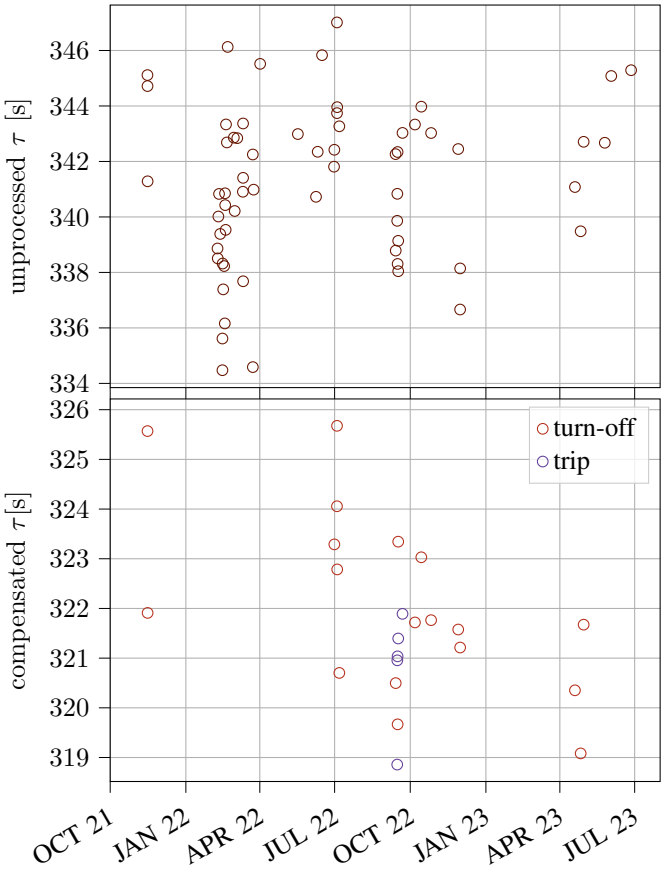

Fig. 18. Example of field data for one specific converter. The upper plot shows the unprocessed τ values while the lower plot shows the corrected τ values categorised for regular power converter turn-offs and power converter trips. It should be noted that some data points are excluded from the lower plot; the reason being that they do not fulfill the criteria of usable records primarily because they have been obtained during partial capacitors' discharges which do not start from the nominal voltage.

τ values in the bottom plot of Fig. 18 will become visible. As stated in Section II, an EOL criterion in terms of capacitance decrease can be set by the converter operator to, for example, 20% compared to the healthy capacitor.

IX. Discussion

In this section the CM method is discussed with its strengths, weaknesses and the proceeded tests.

A. Impact of the converter

Because all of the tests have been conducted with the converter itself, it needs to be verified that the results are not influenced by further undesired effects due to various other components of the converter. There are different components connected to the DC-link as described in Section IV. It is for instance possible that leakage currents of the semiconductors or voltage measurement circuits can influence the result. It is very obvious that the board capacitor C_{Board} shown in Fig. 4 will have an impact on the measured τ. The C_{Board} consists of eight parallel connected film capacitors which are assumed ideal without the described ionisation effects of electrolytic capacitors. To ensure that there are no undesired effects from the

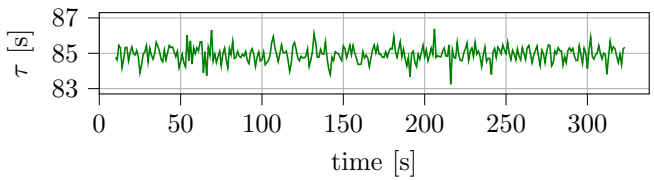

Fig. 19. Measured τ when only the board capacitors, C_{Board}, are connected with early (left-side) and late (right side) sample pairs.

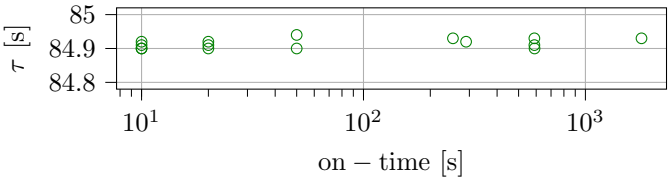

Fig. 20. On-time dependency of τ for the case with only the board capacitors, C_{Board} connected.

converter, tests of the converter without a connected capacitors bank have been performed. The balancing resistors are part of the capacitor bank and, therefore, will also be disconnected. Thus, only the board capacitor C_{Board}, voltage measurement R_{VSensing} and the main discharging resistor $R_{\mathrm{Discharge}}$ are kept connected for these tests. A linear discharge according to Eq. 5 with a τ of 85.17 s is expected. The same linearity check as it was done in Fig. 8 of Section V-A is repeated for a discharge voltage decay without the capacitors bank being connected. The result of this linearity check is plotted in Fig. 19.

The very low scattering of the result shown in Fig. 19 is assumed to be a result of noise and limited measurement accuracy. In addition, tests with different on-times without the electrolytic capacitors bank were conducted. In the results shown in Fig. 20 no on-time dependency is investigated.

These measurements with the disconnected capacitors bank show that only the electrolytic capacitors cause the non-linearity in the voltage decay proving that the presented results are not influenced by this side effect of the converter.

B. Impact of discharge resistor

According to Section IX-A, for the SIRIUS converter no side effects of the discharge resistor are recognized. However, in other converters the discharge resistors might have an impact on the measured τ. In the ideal case, resistors have just constant resistance under rated operated conditions. Nonetheless, it is possible that they can have a positive (PTC) or negative temperature coefficient (NTC). Due to self-heating effect of the resistors, this can add further non-linearity to the regular voltage decay. This effect should be distinguished between the case with always-connected discharging resistors and discharging resistors which are switched on after the converter's turn-off. This means that the discharge can start when the resistor is in cold or hot condition. In addition, during the discharge the resistor temperature depends on the decreasing power dissipation during the discharge, and also the heat exchange with ambient and thermal capacitance of the resistor. To apply this method, discharging resistors of good

thermal stability needs to be chosen, even when this is not a requirement for the regular converter's operation.

In other converter designs, the discharging resistor might be of different type and value, thus resulting in different time constants. Still, permanent connected discharging and/or balancing resistors are required for a safe operation of the converter but they cause additional losses. Therefore, the time constants are quite long to minimize them. The influence of different resistance values and their implications on the proposed CM method have not investigated in this paper, but it is expected that the proposed CM method will still be valid, provided that a calibration of the DC-link capacitors is performed at the beginning of their useful lifetime. The calibration process has been analyzed in Section IX-F

C. Optimal Sampling

This paragraph discusses the improvements and limitations that are implied regarding the optimal sampling in the field application. The SIRIUS converter uses a 10bit analogue-to-digital conversation (ADC) system. That means that the voltage is measured in steps of approximately $1\,\mathrm{V}$. Additionally, there is a typical voltage offset in the range of $2\,\mathrm{V}$. This corresponds to $3\,\mathrm{V}$ noise on the voltage signal. With the optimal τ approach (see Section III), it is feasible to minimize the impact on the τ measurement. In the case of SIRIUS converters, a 0.3% voltage error results in a τ difference of 0.52%. If the resolution would be reduced to 8bits, τ would be impacted by 1% error. With a good choice of sample points, the best performance out of the limited sensor accuracy can be achieved. Yet, the negative impact of an inadequate choice of sample pairs is not limited. According to Fig. 3 small deviations from the optimum will have a minor impact. Linear errors in the voltage measurement will not have an impact on the τ calculation at all. This makes tolerances in voltage dividers to measure the voltage irrelevant. Because of the non-linearity of electrolytic capacitors, it is important to always keep the same samples even when the measured τ decreases due to degradation, in order to keep the data comparable.

D. Compensation of temperature and on-time

The proposed CM method and the compensation approach present a way to use the regular discharges which will appear under different temperatures and after different usage of the converter. However, there are further impacts of the charge history when the converter is operating. Data from converter trips and partial discharges can be filtered out. Still, uncertainties of the charge history due to capacitor voltage changes will remain. These are the regular voltage drops according to Fig. 5 to enable the strong current pulses. Further it is expected that the previous operation of the converter can have an impact as well, when the converter operation interruption was only for a short time period.

The capacitor temperature will also be difficult to estimate. Due to the converter operation, the ripple current losses in the capacitor can influence the temperature in a relevant way. Because of the high thermal capacitance of the capacitors, ambient temperature changes will impact the capacitor temperature with some delay. To emulate this delay a low pass filter can be used on the measured ambient temperature. Finally, the temperature estimation also depends on the application, for example, if significant temperature deviation will appear and compensation is required. For the investigated healthy capacitors bank a temperature change from $10\,^{\circ}\mathrm{C}$ to $50\,^{\circ}\mathrm{C}$ will change the τ value by 6% which requires compensation for a meaningful CM.

For each DC-link capacitor type a calibration is required (see Section IX-F). However, tolerances in the production process of capacitors from the same manufacturer might be expected. Additionally to capacitance and ESR, also the compensation coefficients (see Table III) might have changed slightly. Variations in the ESR will not be relevant for the proposed CM method, because the high resistance value of the discharging resistor, usually in the$\mathrm{k}\Omega$ range, will be dominant compared to the capacitor's ESR, which is usually in the $\mathrm{m}\Omega$ range. Initial variations of the capacitance will be detected and will be integrated in initial estimation of the time constant. More critical are tolerances in the temperature and on-time dependency, which are expected to be low as long as the same design and materials are used by the manufacturer. By using Eq. 14, the temperature coefficient is defined based on a reference temperature which represents a typical temperature for the field application. Therefore, it is less sensitive compared to a temperature coefficient which is referred to the absolute temperature due to the fact that only the temperature difference is used.

Alternatively, it is also possible during longer off-times of the converter to charge and discharge the DC-link capacitors only for performing CM. In this way, charge history effects due to converter's operation can be widely avoided. These extra discharges for CM can be done when the temperature is out of an extreme value to reduce the need for temperature compensation. This alternative kind of quasi-offline CM will provide better results but it will consume some additional energy and increase the number of circuit breaker switching procedures.

E. Data processing

The proposed CM methodology can be implemented on the converter's controller itself since the data processing does not require high computing power. Due to the quasi-offline operation, it will not require sensing and computing resources during the operation of the converter. However, it needs to be ensured that the controller and sensors will be powered until the capacitors are discharged to enable the recording. This can be an issue for some applications, but it can be overcome by using short-term energy storage like a supercapacitor or a battery to keep the controller powered for the short time of the testing. Data exchange over a network using for example an Internet of Things (IoT) device is beneficial for collecting data from all converters, but the method can also be implemented standalone on the converter controller.

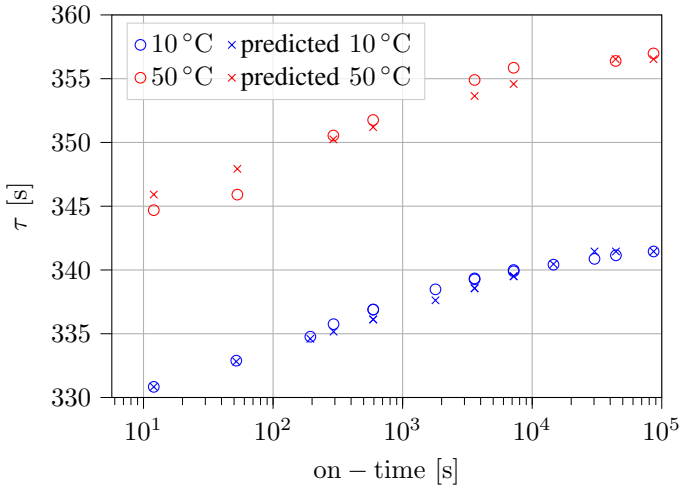

Fig. 21. Measured temperature and on-time dependency for alternative capacitor type including the predicted values for verification of the compensation method.

F. Calibration requirements

To enable this CM method several parameters are required. These are temperature coefficient and on-time dependency (see Table III). All of these parameters are usually not available from the manufacturer and require an extensive pre-characterization and calibration. However, it is sufficient to perform these procedures with just one converter and use the coefficients for all others, provided that they are of the same type and built with the same type of components.

G. Validation of the proposed CM method with an alternative capacitor

To verify the feasibility of the proposed CM method, a test with capacitors from a different manufacturer has been performed. This additional test focuses on the verification of the on-time and temperature dependency. The test setup remains the same as explained in Section V-B. The alternative capacitor has the same nominal data (29 mF, 400 V, maximal temperature 85 °C) as the original capacitor. However, the typical ESR value is higher (16 mΩ instead of 5 mΩ) and the tolerance in capacitance is different (+/- 20% instead of 0+30%) compared to the initial capacitor.

The measured τ values for different on-times at 10 °C and 50 °C using the alternative capacitors type, are presented in Fig. 21. The shape of the curve remains similar to the measurements of the original capacitor (Fig. 12). With this measurement data a new set of compensation coefficients has been calculated, which are summarized in Table IV. For verification of the proposed procedure for these alternative capacitors, the expected τ values are estimated and plotted in Fig. 21.

The measurement with the alternative capacitor type proves that the method can also be applied for a different type of DC-link capacitor. As it is described in Section IX-F, a calibration is always required to compensate with the correct coefficients.

TABLE IV
COEFFICIENTS FOR TEMPERATURE AND ON-TIME COMPENSATION FOR THE ALTERNATIVE CAPACITOR TYPE

Coefficient	value	unit
T_{ref}	10	°C
τ_{nominal}	341.5	s
$t_{on\ max}$	30263 ≈ 8.4 h	s
$\text{Coeff}_{t_{on}}$	0.009141	$1/\log_{10}(\text{s})$
Coeff_{T}	0.001104	1/°C

H. Comparison with other CM methods for capacitors

The proposed CM method is limited to detect capacitance drop. According to accelerated ageing tests with different stress levels [31], [32], it is not possible to estimate ESR directly form the capacitance. This paper focuses on CM methods for electrolytic DC-link capacitors with the restriction that only a voltage sensor at the DC-link is available and it can be implemented without hardware changes to an existing converters family.

With this limitation in mind, a periodical manual offline CM [14] can be an alternative to the proposed CM method. In this case, the offline CM should be performed always at the same temperature to avoid distortion of the results. Manual inspections can be grouped with other preventive maintenance actions, but would require the use of external instrumentation and disconnection of the capacitors, which can introduce risks like contact issues in the reassembling phase. Manual inspections can, on the other hand, offer a deeper understanding of individual capacitor ESR and capacitance state.

Another alternative method can also be to run load-profile-based degradation simulations using a mathematical lifetime model of the capacitor [3], [17]. These methods provide information about the expected degradation level and the results can be used for planning offline CM rather than for monitoring the actual SOH.

Methods that involve additional circuits and/or sensors to monitor the ESR in addition to the capacitance may yield advantages in SOH monitoring and may also operate as online CM methods. These methods can have additional requirements for current and voltage sensors to allow AC measurements (see Section II-A). In these methods the injected current into the capacitor bank can be an AC signal with a small DC component which is flowing through the balancing resistors. The voltage sensor will sense a significant DC-link voltage superimposed with a relatively low ripple voltage or test signal, which is relevant for CM. Aspects related to voltage sensing for better utilization of the voltage resolution have been discussed in [16]. An alternative way to measure capacitance and ESR is to introduce a switchable additional discharge resistor instead of a current sensor [15]. This quasi-offline CM method uses the voltage resolution quite well.

As described above and in Section II the most suitable CM method depends on the converter topology and the requirements of the application. It is a conceptual decision if additional hardware for CM is feasible and can be tolerated by the design and operating constraints of the converter and

if operation interruptions can be tolerated for quasi-offline or even offline CM.

X. Conclusion

This paper has presented a low-invasive and quasi-offline CM methodology for electrolytic capacitors employed in large converters' installations at CERN. The investigations show that this low-invasive CM methodology can be implemented seamlessly even for an existing converter system without any hardware changes. The CM runs in quasi-offline mode and will therefore not impact the converter's operation or use additional resources of the converter's controller. The basic approach of investigating the regular discharge after each discharge can only be used to detect very significant capacitance degradation. Therefore, it is essential to combine this data with temperature and charge history for compensation. An optimal sampling method is proposed with a view of acquiring the best data from limited sensor resolution and accuracy.

It has been shown that for the healthy capacitor bank the deviation due to temperature and on-time of 7% can be reduced to 1% uncertainty with the proposed compensation method. This makes it feasible to detect and distinguish between healthy and degraded capacitor banks. This method requires a large dataset to estimate the coefficients. Once the coefficients are estimated, then the results can be used for all converters of the same type. With information about the converter status, the CM can focus on data which is best suitable by sorting out inappropriate records.

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