Gate-Drive Circuits for Adaptive Operation of SiC MOSFETs

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***Abstract*—This paper presents two novel adaptive gate driving concepts for Silicon Carbide (SiC) metal oxide semiconductor field-effect transistors (MOSFETs). The first concept is based on the adaptive over-driving principle and implemented either as a novel adaptive voltage-source over-driver (AVSOD) or as the conventional adaptive current-source over-driver. The adaptive over-drivers are capable of independently controlling turn-on and turn-off delay times, switching times and switching energy, as well as device dv/dt and di/dt. The second concept is a novel variable-voltage source multi-level gate driver (VVSMGD) with integrated synchronous buck converter, which is able to adjust the gate driving voltage. This driver is capable of adaptively manipulating turn-off delay times, turn-off times and switching energy, device voltage and current overshoots, voltage and current harmonic spectrum during switching transients. Furthermore, this driver can also adjust the conduction loss of the MOSFET by manipulating the on-state resistance through the gate-source voltage. The presented gate drivers are experimentally validated on a 3.3 kV/750 A high-power SiC MOSFET power module. It has been shown that the AVSOD reduces the turn-on and turn-off switching energies up to 55% and 68%, respectively, while the VVSMGD can reduce the drain-source voltage overshoot by 45%.**

***Index Terms*—Silicon Carbide MOSFETs, Silicon Carbide power module, High-Voltage Silicon Carbide MOSFETs adaptive gate drivers**

I. Introduction

Silicon carbide (SiC) metal-oxide semiconductor field-effect transistors (MOSFETs) are becoming the most attractive wide-bandgap (WBG) semiconductor technology to replace silicon (Si) based insulated-gate bipolar transistors (IGBTs) commonly deployed in high-voltage high-current power electronics systems. Even though high-voltage (> 3.3kV) SiC MOSFETs are yet to reach the market, the available devices (≤ 3.3kV) are considered as potential replacements of the well established Si IGBTs in applications such as medium-voltage (MV) drives and medium- and high-voltage (HV) direct-current (DC) grids [1]–[9].

Gate drivers are the key components to exploit the fast-switching capabilities of SiC MOSFETs and ensure safe operation when employed in power electronic converters. Adapting the conventional totem-pole voltage source gate driver (CVSGD) technology used for Si IGBTs, poses limitations in exploiting the fast-switching characteristics of SiC MOSFETs. Even though fast switching unlocks the utilization of higher switching frequencies due to lower switching energies, it causes overvoltages (i.e., due to high di/dt) that might be severe for the safe operation of SiC MOSFETs. Besides, reducing deadtimes in half-bridge circuits in order to decrease conduction of antiparallel diodes and thus reduce losses necessitates the minimization of turn-on and turn-off delay times. In case of dual active bridge (DAB) converters, extensive deadtimes can trigger unwanted effects such as voltage reversal, phase drift, increased reflow power, and voltage sag [10]. Therefore, the drive circuits for SiC MOSFETs should not only perform optimal turn-on and turn-off transients and exhibiting the lowest possible switching energies, but also ensure safe operation of the devices. These challenges become more prominent under varying load current and blocking voltage conditions of the SiC MOSFETs, where optimal tuning of the CVSGD for the entire range of operating points is not possible. CVSGD have a fixed design and parameters choice, which are determined during the converter's design phase. A solution to this, is the utilisation of adaptive gate drivers which are able to continuously optimise their operation based on the loading conditions.

Adaptive gate drivers are able to manipulate the movement of gate charge in a more flexible way than the CVSGDs, both during the switching transients and during conduction phase. Adaptability during the switching transient allows for both manipulation of the switching loss and switching time parameters. The switching loss can either be minimized to optimize efficiency or adapted in a way to minimize device junction temperature variations and thus improving reliability. The turn-on and turn-off delay times can be manipulated to accommodate optimal system deadtime conditions, as well as device di/dt and dv/dt control for complying with electromagnetic interference requirements. Furthermore, by adjusting the on-state gate driver voltage supply values, $v_{GS} = V_H$, the device on-state drain-source resistance, $r_{DS(on)}(v_{GS})$, can be manipulated.

Adaptive current-source gate drivers (ACSGD) are implemented either as inductor-less or inductor-based topologies. The *inductor-less* ACSGDs are typically current-mirror based circuit topologies [11]–[15]. On the other hand, inductor-based ACSGDs utilize a single or multiple inductors as an energy storing element in the gate driving circuitry. The inductor-based ACSGDs can be categorized into continuous (CCS) and discontinuous (DCS) current source drivers [16], depending on whether the current through the driver inductor is continuous or discontinuous [16]. The CCS typically needs a larger inductor value and higher driver losses than the DCS for the same gate drive current [16], [17]. On the other hand, DCS typically

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have a circuit topology with higher component count, with more drive switches and higher control complexity. For CCS-based ACSGDs, the drive circuit is typically implemented as a full-bridge type used in synchronous converter applications for driving both converter switches [18]–[24]. ACSGDs with DCS are typically implemented as a full-bridge type [25]–[32]. Another possibility is to realize them as pure half-bridge circuits or half-bridge type hybrid circuit with additional blocking switches and resonance circuitry [33]–[39]. An ACSGD capable of multi-functional switching transient adaptability has been proposed by the authors in [40], [41]. This driver is capable of independently control the device's turn-on/off delays, as well as di/dt and dv/dt. In all these ACSGD concepts, the peak value of the gate current is always kept lower than the critical value which excites oscillations in the gate loop [41]. However, allowing the gate current to exceed the oscillation-excited current and by well-controlling this value, speeding-up the switching transients becomes possible. The first contribution of this paper is the design and operation of a traditional ACSGD in over-driving mode for improving switching speed of SiC MOSFETs. The term over-driving refers to the supply of a peak gate current that exceeds the corresponding gate current that can be supplied by using a CVSGD with zero gate resistance.

The second family of adaptive gate drivers, namely adaptive voltage source gate drivers, can control the gate current either by adjusting the voltage source supply level or the impedance seen by the gate path. Variable impedance drivers are most commonly implemented as variable gate resistance or variable input capacitance circuits [42]. Variable resistance drivers simply vary the applied gate resistance seen by the device, thus enabling control of the gate current and consequently the device switching transient [43]–[47]. Variable capacitance drivers regulate the switching transients by controlling the input capacitance C_{iss}, for example by controlling the Miller capacitance C_{gd} or the gate-source capacitance C_{gs} [48], [49].

Variable voltage source drivers are commonly implemented as multi-level voltage source circuits or two-level circuits with voltage level controllability, e.g. using a buck converter [50]–[58]. By adjusting the gate-source voltage, v_{GS}, level prior to the switching transient, the turn-on and turn-off delays can be controlled. Besides, by adjusting the value of v_{GS} during the switching transients, switching parameters such as di/dt, dv/dt, total switching time, as well as v_{DS} and i_D overshoot values can be controlled. However, none of these gate driver concepts has explored the possibility for slightly over-driving the gate in order to achieve faster switching performance. Besides, the combination of over-driving features with adaptive functionalities for manipulating switching parameters has not been studied either. Finally, none of the presented gate drivers are capable of adjusting switching and conduction power losses simultaneously.

The second contribution of this paper is the development of a voltage-source gate driver with over-driving functionalities both in the positive and negative gate voltages, for improving the switching performance of SiC MOSFETs. Finally, the

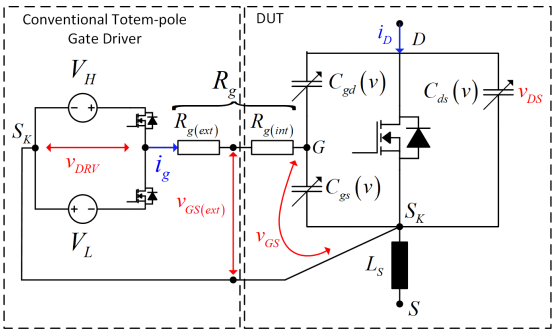


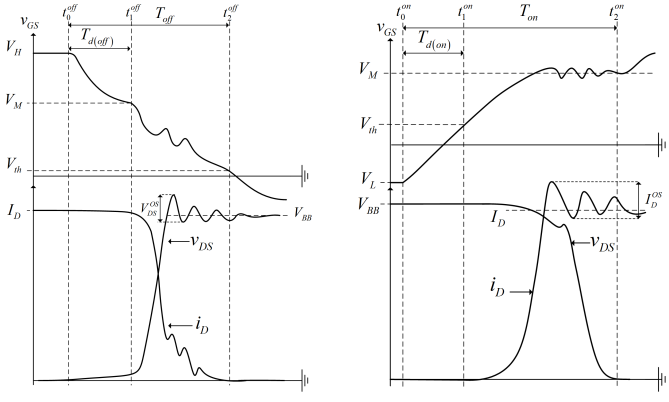
Fig. 1. Circuit schematic of the totem-pole based CVSGD connected to the equivalent SiC MOSFET circuit.

third contribution of the paper is a novel variable voltage-source multi-level gate driver that incorporates a synchronous DC/DC buck converter for online adjustment of switching and conducting characteristics of SiC MOSFETs by incorporating an adjustable intermediate positive gate voltage. An extensive theoretical and experimental performance evaluation of the three gate driver concepts is shown in the paper.

The paper is organized as follows. Section II presents the switching characteristics of SiC MOSFETs and the limitations using CVSGDs. Section III shows the design and operation of adaptive over-drivers, while in Section IV the proposed variable-source, multilevel gate driver is presented. A thorough experimental validation of the gate drivers is shown in Section V. Discussion of the findings is included in Section VI and the conclusions are drawn in Section VII.

II. Switching Characteristics of SiC MOSFETs and Performance Limitations using the CVSGD

The schematic diagram of a CVSGD is shown in Fig. 1. The CVSGD supplies the driving voltage, v_{DRV} that can switch between a positive, V_H, and a negative value, V_L. The gate current is governed by the values of V_H and V_L, as well as by the value of the resistance, R_g in the gate path.



(a) Theoretical turn-off waveforms. (b) Theoretical turn-on waveforms. .

Fig. 2. Theoretical switching waveforms of SiC MOSFETs.

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Theoretical switching waveforms are shown in Fig. 2 and the parameters depicted are determined as follows. The turn-on time $T_{on} = t_2^{on} - t_0^{on}$ is defined as the time duration from the time instant that the gate drive voltage v_{DRV} changes from the off-state voltage level V_L until the device has reached linear region, i.e. $v_{DS} \leq (v_{GS} - V_{th})$. The turn-on delay time $T_{d(on)} = t_1^{on} - t_0^{on}$ is defined as the time duration from the time point when v_{DRV} changes from V_L until the device starts conducting (i.e. $v_{GS} > V_{th}$ and $i_D > 0$). The turn-on switching energy E_{on} is the switching energy incurred by the device from the time instant that i_D starts rising until $v_{DS} \leq (v_{GS} - V_{th})$

$$E_{on} = \int_{t_1^{on}}^{t_2^{on}} i_D \cdot v_{DS}\, dt \tag{1}$$

Similarly, for turn-off, the turn-off time $T_{off} = t_2^{off} - t_0^{off}$ is the time duration from when v_{DRV} changes from the positive driver supply level V_H until $v_{GS} \leq V_{th}$. Finally, the turn-off delay time $T_{d(off)} = t_2^{off} - t_0^{off}$ is defined as the time duration from the time instant that v_{DRV} changes from V_H until the device reaches the saturation region (i.e., $v_{DS} \geq (v_{GS} - V_{th})$. The turn-off switching energy is thus defined as

$$E_{off} = \int_{t_1^{off}}^{t_2^{off}} i_D \cdot v_{DS}\, dt \tag{2}$$

The drain current i_D can be approximated in the saturation region (i.e. for $v_{DS} \geq (v_{GS} - V_{th})/P_{vf}$ while $v_{GS} \geq V_{th}$, where P_{vf} is a parameter defining the sharpness of transition between ohmic and saturation region) considering its transfer characteristics as [59], [60]

$$i_D \approx g_s(v_{GS} - V_{th})^x(1 + \lambda v_{DS}) \tag{3}$$

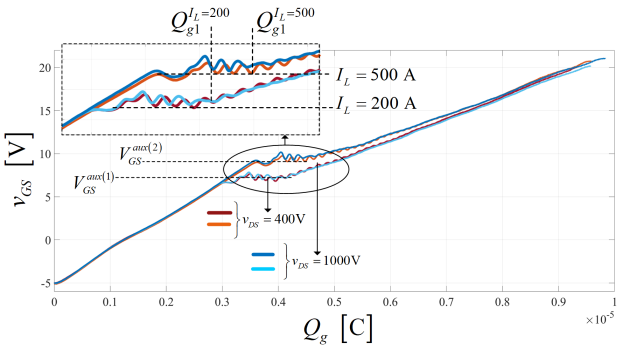
where g_s is the MOSFET's transconductance, x is a fitting parameter to be adjusted to the specific device used and λ is the channel modulation index, with the value of v_{DS} being the device's blocking voltage.

The manipulation of *switching loss* is limited when using CVSGDs, as they have limited design parameters available for shaping the switching transients. The values for the positive and negative driver supplies, V_H and V_L, are limited by the voltage rating of the gate $[V_{GS}^{max}, V_{GS}^{min}]$, which are usually in the range of $[20\text{V}, -20\text{V}]$ for SiC MOSFETs. The lower value of R_g is generally limited by the device's internal resistance $R_{g(int)}$. For a CVSGD, the gate current i_g is given by

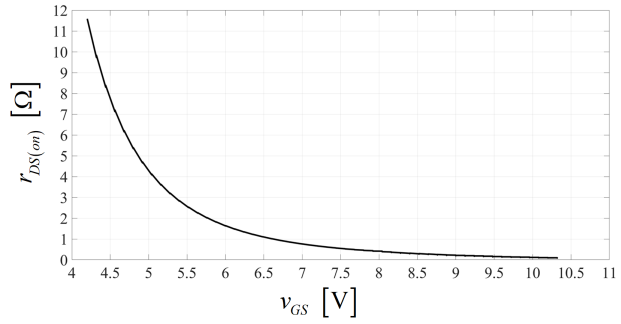
$$i_g = \frac{(V_{HL} - v_{GS})}{R_g} = \frac{V_{HL}}{R_g} e^{-t/\tau_{iss}} \tag{4}$$

where $R_g = R_{g(ext)} + R_{g(int)}$, $V_{HL} = V_H - V_L$, $C_{iss} = C_{gs} + C_{gd}$ and $\tau_{iss} = C_{iss} R_g$. The time duration of which the CVSGD can move the amount of charge Q_{g_1} is given by

$$T_{g_1} = -\tau_{iss} \cdot \ln\left(\frac{Q_{g_1}}{C_{iss} V_{HL}}\right) \tag{5}$$



(a) The FMF750DC-66A $Q_g(v_{GS})$ characteristics.



(b) $r_{DS(on)}$ vs. v_{GS}. Measured $r_{DS(on)}$ on-state v_{GS} dependency of the FMF750DC-66A.

Fig. 3. (a) Gate charge as a function of V_{gs} (b) and on-state drain-source resistance on-state gate-source voltage dependency of the Mitsubishi FMF750DC-66A SiC MOSFET half-bridge power module used as device under test (DUT) using the B1505A Power Device Analyser.

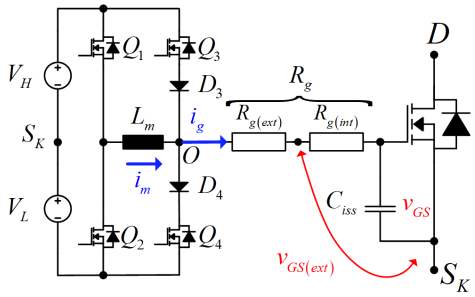
Considering the turn-on process, the device is considered turned on when the output capacitance $C_{oss} = C_{gd} + C_{ds}$ is discharged. That is, when Q_{g_1} has been moved from the driver to the gate at the given device operating point, as seen in Fig. 3a. Thus, the only configurable design parameters available for the CVSGD is the V_H/V_L values and R_g.

As seen in Fig. 3b, the on-state resistance of SiC MOSFETs, $r_{DS(on)}$, is dependent on the value of v_{GS}. Adjusting the value of v_{GS} allows for conduction loss

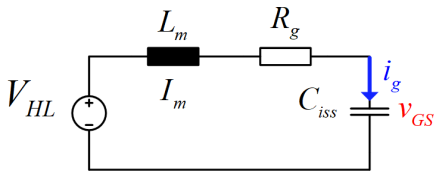
$$p_{cond} = r_{DS(on)}(v_{GS}) \cdot i_D^2 \tag{6}$$

manipulation during operation in power converters in order to, for example, achieve active thermal control.

Since the CVSGD drive strength is fixed by its driving voltages and total gate resistance, the switching performance using CVSGD can only be altered by changing the hardware of the system (i.e. the external DUT gate resistance and driving voltages), and will only have one optimal gate drive design for a particular converter operating point. The presented adaptive gate drivers allows manipulating the switching performance and conduction performance online during converter operation, and are thus not limited by fixed hardware parameters.

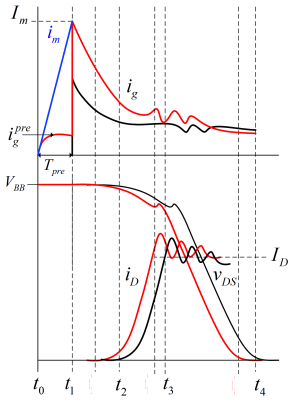


(a) ACSOD circuit schematic.

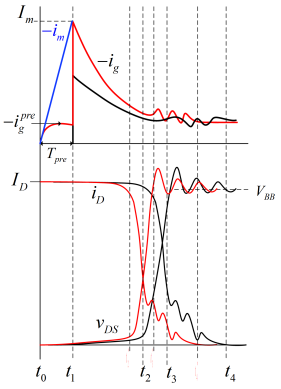


(b) ACSOD equivalent RLC-circuit schematic.

Fig. 4. The adaptive current source over-driver (ACSOD).



(a) ACSOD turn-on transition.



(b) ACSOD turn-off transition.

Fig. 5. ACSOD theoretical switching waveforms (red) and CVSGD theoretical switching waveforms (black).

III. Adaptive Over-Drivers

This section introduces a class of adaptive gate drivers termed *over-drivers*. The *over-drive* concept is defined as adaptive gate drivers capable of supplying a higher peak current I_g than the corresponding gate current using the CVSGD, i.e.

$$I_g = \frac{V_{HL}}{R_g} \tag{7}$$

Two approaches of achieving over-drive capabilities are discussed in the following. The first over-driving principle is based on the full-bridge current source topology and presented in subsection III-A, while a novel over-driver based on a voltage-source topology is presented in subsection III-B.

A. Adaptive Current Source Over-Driver

The circuit schematic of the adaptive current-source over-driver (ACSOD) is shown in Fig. 4a with its equivalent RLC-circuit illustrated in Fig. 4b. The driver topology utilizes 4 discrete switches (Q_1-Q_4) configured in a full-bridge with an energy storing inductor, L_m. This type of full-bridge inductor-based current source gate driver is utilized for high switching frequency operation of synchronous converter topologies, and for individual-switch driving [18]–[23], [25]–[32], [61]. The operating principle of the ACSOD is based on charging L_m to a peak current I_m via the voltage sources V_H and V_L. The charged current i_m is then injected into the gate at turn-on and sunk from the gate at turn-off process. By adjusting the magnitude I_m, the switching energies E_{on}/E_{off} and switching times can be controlled.

The procedure for the turn-on transition is illustrated with the red waveforms in Fig. 5a and for the turn-off in Fig. 5b.

1) Pre-charge Interval: The ACSOD operation is initiated by the pre-charge interval. At turn-on, the current i_m is charged to an amplitude of I_m by V_{HL} through L_m, by turning Q_1 and Q_4 on for the time duration $T_{pre} = t_1 - t_0$, as seen in Fig. 5a. Due to on-state resistance of the discrete switches (Q_1-Q_4) and blocking diodes (D_3/D_4), R_{ls} comprising the driver and a stray inductance L_{ls} in the lower path between Q_2 and Q_4, a current divider is formed between the path through $R_g \rightarrow C_{iss} \rightarrow V_L$ and the path through $Q_4 \rightarrow V_L$, as illustrated in Fig. 6a-6b. Thus, a current, i_g^{pre} flows into the gate between t_0 and t_1, as illustrated theoretically in Fig. 6c and measured as seen in Fig. 7. This current charges the gate-source voltage, v_{GS}, to a pre-charge value V_{GS}^{pre}. An in-depth explanation and mathematical derivation of the pre-charge interval is given in [41].

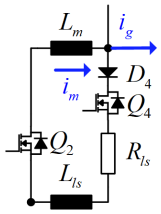
2) Turn-on: The inductor current i_m having an amplitude I_m is then injected into the gate at the time instant t_1 by turning Q_4 off while keeping Q_1 on, realising the equivalent circuit illustrated in Fig. 4b.

3) Turn-off: For the turn-off process, the current i_m is similarly charged to an amplitude of I_m by turning Q_2 and Q_3 on at the time point t_0 and keeping them on for a time interval T_{pre}. The inductor current i_m with the amplitude I_m is then sunk from the gate at t_1 by turning Q_3 off while keeping Q_2 on. Similarly as for the turn-on, a pre-charge current $-i_g^{pre}$ is sunk from the gate during the T_{pre} interval at turn-off, causing v_{GS} to slightly decrease below V_H prior to the turn-off instant t_1.

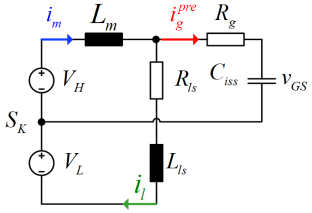
4) ACSOD Design: The energy storing element, L_m, yields significant benefits in terms of switching speed flexibility. Considering the equivalent RLC circuit of the ACSOD given in Fig. 4b and using Kirchhoff's laws, the evolution of v_{GS} can be described by the following differential equation

$$\frac{d^2 v_{GS}}{dt^2} + \frac{R_g}{L_m}\frac{dv_{GS}}{dt} + \frac{v_{GS}}{C_{iss}L_m} = \frac{V_{HL}}{C_{iss}L_m} \tag{8}$$

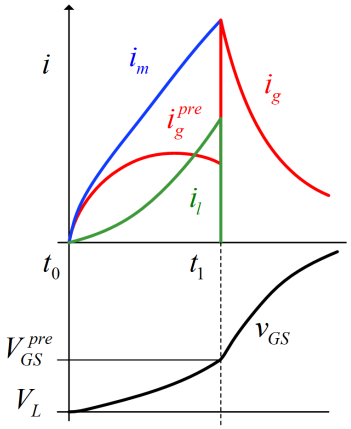
Equation "(8)" is written in the Laplace domain as



(a) Lower part of the ACSOD circuit during pre-charge interval.



(b) Equivalent circuit during pre-charge interval.



(c) Current waveforms during pre-charge interval

Fig. 6. Pre-charge interval.

$$v_{GS}(s)\left(s^2+2\alpha_s s+\omega_{0_s}^2\right)= \left(\frac{V_H\omega_{0_s}^2}{s}+sV_L+\frac{I_m}{C_{iss}}+\frac{R_g}{L_m}V_L\right) \qquad (9)$$
$$\alpha_s=\frac{R_g}{2L_m},\ \omega_{0_s}^2=\frac{1}{C_{iss}L_m}$$

A critically damped response yields the fastest response in v_{GS} to stimuli from i_g. Thus, the damping of the RLC equivalent circuit must be $\zeta_s=\alpha_s/\omega_{0_s}=1$, and L_m then be chosen as

$$L_m=C_{iss}\left(\frac{R_g}{2}\right)^2 \qquad (10)$$

for a given C_{iss} and R_g to preserve a damping of 1. With the response of v_{GS} being critically damped, $v_{GS}(s)$ have a single pole $s_s=-\alpha_s$, and the time response of $v_{GS}(t)$ is described as

$$v_{GS}(t)=V_H+\underbrace{e^{-\alpha_s t}}_{e(t)}\cdot\underbrace{\left(k_{s_1}^v t+k_{s_2}^v\right)}_{l(t)} \qquad (11)$$
$$k_{s_1}^v=\frac{I_m}{C_{iss}}+\alpha_s k_{s_2}^v,\ k_{s_2}^v=-V_{HL}$$

and the gate current i_g given by

TABLE I
ACSOD PASSIVE LOAD TEST PARAMETERS

V_H[V]	V_L[V]	C_L[nF]	R_g[Ω]	L_m[μH]	I_m^{OS}[A]
20	−5	300	3.7	∼ 1	13.5

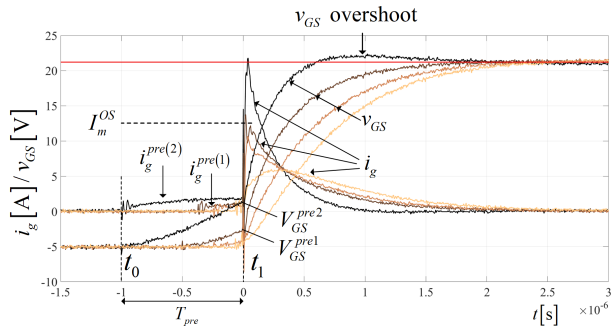


Fig. 7. Measured gate current i_g and gate-source voltage v_{GS} waveforms showing the effect of $I_m > I_m^{OS}$.

$$i_g(t)=C_{iss}\frac{dv_{GS}}{dt}=C_{iss}e^{-\alpha_s t}\cdot\left(k_{s_1}^i t+k_{s_2}^i\right) \qquad (12)$$
$$k_{s_1}^i=-\alpha_s k_{s_1}^v,\ k_{s_2}^i=k_{s_1}^v-\alpha_s k_{s_2}^v$$

Even though the response of v_{GS} is critically damped, the evolution of $v_{GS}(t)$ may still overshoot the voltage source value of V_H if the energy stored in L_m at the turn-on instant is greater than the energy capacity of C_{iss}. Thus, overshoot in v_{GS}, i.e. $v_{GS}(t) > V_H,\ t \geq t_1$, occurs if the magnetic field energy E_L of L_m is greater than the electric field energy capacity E_C of the C_{iss}, according to the following criterion:

$$E_L=\frac{L_m I_m^2}{2}>E_C=\frac{C_{iss}V_{HL}^2}{2} \qquad (13)$$

For a value of I_m greater than the overshoot value I_m^{OS}, v_{GS} overshoots, hence the peak pre-charge value I_m of i_m should not exceed I_m^{OS}

$$I_m^{OS}=V_{HL}\sqrt{\frac{C_{iss}}{L_m}} \qquad (14)$$

The overshoot is visualized in Fig. 7, where the ACSOD is tested on a capacitive passive load C_L in the same range as the input capacitance of the 3.3 kV/750 A SiC MOSFET power module (Mitsubishi FMF750DC-66A) that is used for the experimental validation in this paper. The parameters of the driver for the passive test are summarized in Table I. As seen in Fig. 7, for values of $I_m > I_m^{OS}$, an overshoot occurs in v_{GS}.

The energy dissipation of the gate driver is given by

$$E_D=\int_0^\infty R_g i_g^2 dt \qquad (15)$$

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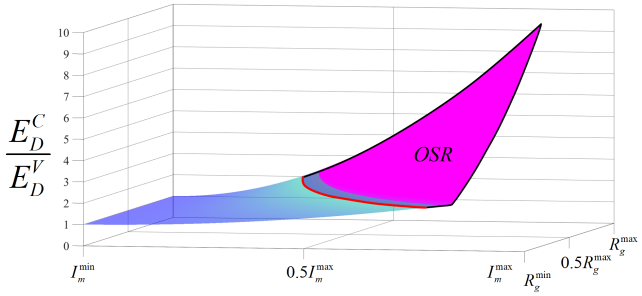


Fig. 8. Gate driver energy comparison of the ACSOD E_D^C and CVSGD E_D^V. The boundary of I_m^{OS} is marked with the red line.

The energy dissipation of the gate driver's total gate resistance R_g is the major contributor of the driver's overall energy use, as compared to the efficiency of driver's on-board DC/DC converters and other ICs such as signal isolators and discrete switch drivers, both in active and quiescent state. The ideal energy dissipation of the CVSGD is constant and given by

$$E_D^V = 0.5 C_{iss} V_{HL}^2 \tag{16}$$

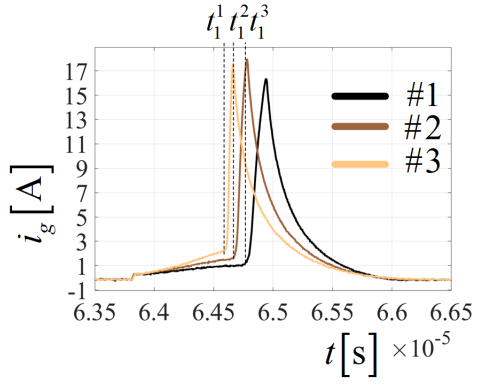
with "(4)" used in "(15)". The energy dissipation of the ACSOD depends on the value of I_m as given in "(12)". Similarly, by using "(12)" in "(15)" with the condition $I_m = I_m^{OS}$ yielding $k_{s_1}^1 = 0$ and $\alpha_s = 2/(R_g C_{iss})$ for $\zeta_s = 1$, the energy dissipation of the ACSOD is given by

$$E_D^{C(max)} = \frac{\alpha_s R_g (V_{HL} C_{iss})^2}{2} = C_{iss} V_{HL}^2 = 2E_D^V \tag{17}$$

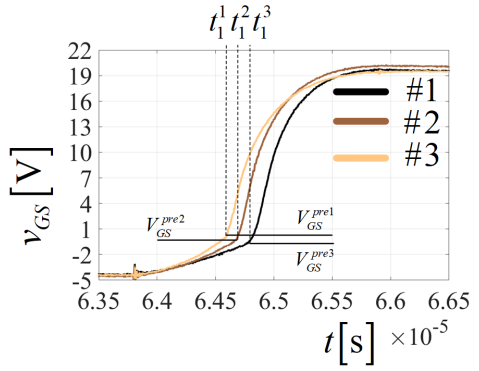
Therefore, using the maximum I_m given by "(14)" with the ACSOD results in twice the energy dissipation compared to the CVSGD. This is illustrated in Fig. 8, where the energy use of the ACSOD driver is compared to that of the CVSGD for different values of R_g and I_m. The red line marks the I_m^{OS} boundary for a critically damped driver, where I_m values larger than I_m^{OS} yields v_{GS} overshoot for the given R_g.

A comparison of estimated v_{GS} rise times during the turn-on between the CVSGD and the ACSOD, that is v_{GS} traversing from the off-state voltage level $v_{GS} = -5$V to an approximation of the Miller plateau voltage (i.e. an estimation of the turn-on time) for different values of I_m and R_g is provided in [41]. A higher I_m results in faster v_{GS} rise times at the cost of higher gate driver energy use.

5) Practical ACSOD Design Considerations: The effect of R_{ls} on the pre-charge current i_g^{pre} can be adjusted by the proper choice of the discrete switches $(Q_1 - Q_4)$ that is of low-voltage Silicon MOSFET type. Choosing components for a gate driver (and general power electronic systems) is generally a compromise between price, size, thermal requirements and device characteristics. A comparison between 3 discrete low-voltage Silicon MOSFET switches with different electrical characteristics is given in Table II. The i_g and v_{gs} responses by employing these 3 MOSFET types in the ACSOD gate driver are shown in Fig. 9. It can be seen that the choice of



(a) i_g.



(b) v_{GS}.

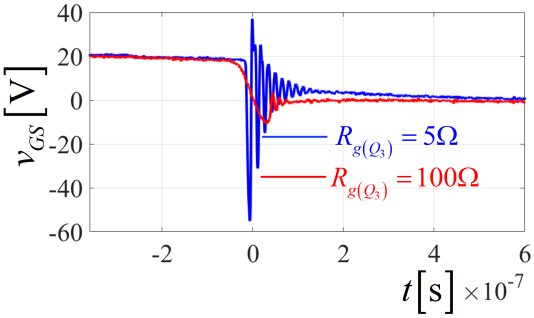
Fig. 9. Comparing i_g and v_{GS} measured waveforms of the ACSOD driver using the 3 discrete gate driver MOSFET switches of Table II. Test performed on a passive load C_L similar to the C_{iss} of the FMF750DC-66A DUT.

TABLE II
GATE DRIVER DISCRETE SWITCH RATED PARAMETERS

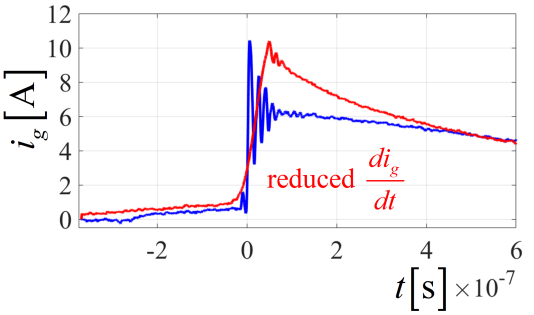
#	Device	V_{BB}	$r_{DS(on)}$	C_{oss}	Package
1	DMN10H220LVT	100V	250mΩ	22pF	TSOT-26-6
2	DMN10H170SVT	100V	115mΩ	36pF	TSOT-26-6
3	DMN6040SVTv	60V	44mΩ	57pF	TSOT-26-6

discrete driver switches impacts the response of the driver, and consequently the response of the driven device i_g and v_{GS}. Their varying values of the device equivalent capacitances impact the di/dt and dv/dt values of the discrete switches – and consequently the slew rate of i_g and v_{GS} – while their $r_{DS(on)}$ impacts the pre-charge current flowing into the gate prior to turn-on and the obtained maximum value I_m, as described in [41].

The gate resistors of $Q_1 - Q_4$, $R_{g(Q_{1-4})}$ also impact the di/dt and dv/dt of the discrete driver switches. A low $R_{g(Q_{1-4})}$ results in a high di/dt and dv/dt, which impact the response of v_{GS} and i_g to the applied i_m. Considering the turn-off instant at t_1 when i_g is sunk from the gate, the discrete driver switch Q_3 is turned off while Q_2 is on, forcing i_g to be sunk from the driver as L_m resists its change in current. Due to



(a) Measured v_{GS} comparing $R_{g(Q_3)} = 5\Omega$ to $R_{g(Q_3)} = 100\Omega$.



(b) Measured i_g comparing $R_{g(Q_3)} = 5\Omega$ to $R_{g(Q_3)} = 100\Omega$.

Fig. 10. Effect of increased v_{GS} comparing $R_{g(Q_3)}$ on di_g/dt and gate oscillations.

TABLE III
ACSOD DISCRETE COMPONENTS RATED PARAMETERS

Component	MPN	Parameter	Package
L_m	IHLP-4040DZ-11	$DCR = 2.5\text{m}\Omega$	10.16x10.16x4mm
$D_{3/4}$	SDT5A100SB-13	$v_F = 600\text{mV}$	DO-214AA

unavoidable stray inductances L_{GS} in the PCB tracks between the node O and S_K, the value of di/dt of the current though switch Q_3 directly determines the di/dt of the sunk i_g. The interaction between the rapidly changing i_g and L_{gs} causes voltage transients and oscillations in v_{GS}. This is seen in Fig. 10 where a simple turn-off instant is performed with different $R_{g(Q_3)}$ values. Increased $R_{g(Q_3)}$ reduces switch di/dt, hence reducing oscillations and voltage overshoots in v_{GS}.

Furthermore, using discrete gate driver switches with higher $r_{DS(on)}$ adds to the total gate drive resistance of the driver and consequently to the total gate driver power losses. During T_{pre}, i_m flows through two of the driver switches and one diode (Q_1/Q_4 and D_4 at turn-on, Q_2/Q_3 and D_3 at turn-off) and L_m. Assuming that R_{ls} and L_{ls} are small compared to the gate impedance, i_g^{pre} is ignored and the current i_m can be estimated as

$$i_m = \frac{I_m}{T_{pre}} \cdot t \tag{18}$$

Thus, during this interval, the energy dissipated in the two gate drivers switches and the DC resistance (DCR) of L_m is

$$\begin{aligned} E_{D(ON)}^{pre} &= \int_0^{T_{pre}} \underbrace{(2r_{DS(on)(Q)} + r_{L_M})}_{r_{ON(pre)}} \cdot i_m^2 dt \\ &= r_{ON(pre)} \cdot T_{pre} \cdot \frac{I_m^2}{3} \end{aligned} \tag{19}$$

where the $r_{DS(on)(Q)}$ is the drain-source on-state resistance of the gate driver switches (see Table II) and r_{L_M} is the DC resistance (DCR) of L_M (see Table III). Calculating the conduction losses for a single switch during the pre-charge interval, $E_{D(Q)}^{pre}$ Similarly, the voltage drop of the diodes causes the energy dissipation

$$\begin{aligned} E_{D(D)}^{pre} &= \int_0^{T_{pre}} v_F \cdot i_m dt \\ &= v_F \cdot T_{pre} \cdot \frac{I_m}{2} \end{aligned} \tag{20}$$

assuming a constant diode forward voltage drop v_F. When the ACSOD driver has charged its desired current I_m after T_{pre}, the current i_m is injected into the gate as described in Sections III-A2 and III-A3. Since only one of the gate drive switches is on during the turn-on/off, the conduction losses induced in these switches can be described by Eq. (15) replacing R_g with $r_{DS(on)(Q)}$. The gate driver discrete switch conduction losses can be included in the total gate driver losses described by Eq. (15) by including $r_{DS(on)(Q)}$ in R_g.

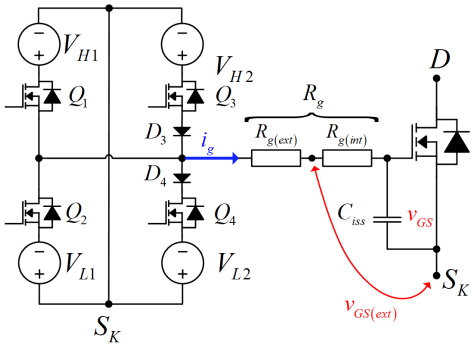
TABLE IV
ACSOD DISCRETE COMPONENTS POWER LOSSES
$L_M = 1\mu\text{H}$, $V_{HL} = 25\text{V}$, $R_g = 3.7\Omega$, $C_{iss} = 300 \cdot 10^{-9}\text{F}$
DEVICE #3

I_m	$E_{D(ON)}^{pre}$	$E_{D(Q)}^{pre}$	$E_{D(D)}^{pre}$	$E_{D(Q)}^{on}$	E_D^{on}
5A	0.39μJ	0.19μJ	0.30μJ	3.46μJ	115μJ
10A	3.10μJ	1.53μJ	1.20μJ	4.59μJ	152μJ
15A	10.46μJ	5.15μJ	2.70μJ	6.48μJ	215μJ

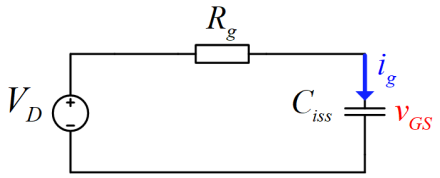
Table IV gives a breakdown over the discussed component losses across different values of I_m at turn-on with a passive load as illustrated in Fig. 4b. The imposed energy losses during the pre-charge interval are small compared to the the total gate driver energy losses E_D^{on}. It is seen that the ACSOD switches exhibit a higher energy loss during the pre-charge interval for higher values of I_m than the diode, while the difference is reduced at lower values of I_m due to the assumption of constant v_F and hence the diode's linear loss relationship with I_m. Furthermore, it is seen that the ACSOD switch energy loss $E_{D(Q)}^{on}$ constitutes a small percentage of the total ACSOD loss E_D^{on}, and is equal to the ratio of $r_{DS(on)Q)}$ to R_g.

B. Adaptive Voltage Source Over-Driver

This section presents a novel adaptive voltage-source over-driving circuit concept (AVSOD). The circuit schematic of the



(a) AVSOD circuit schematic.



(b) AVSOD equivalent RLC-circuit schematic.

Fig. 11. The adaptive voltage source over-driver (AVSOD).

AVSOD is shown in Fig. 11a with its equivalent RLC-circuit illustrated in Fig. 11b. The voltage sources V_{H1} and V_{H2} are used for turn-on, while the voltage sources V_{L1} and V_{L2} are used for the turn-off process. For the configuration presented in this paper, the voltages V_{H1} and V_{L1} are used as over-drive voltages, i.e. $V_{H1} > V_{H2}$ and $V_{L1} > V_{L2}$, while V_{H2} and V_{L2} are kept at a fixed level corresponding to conventional V_H and V_L driving levels. By controlling the switches Q_1 and Q_3, the voltage V_D in Fig. 11b, takes either the value of V_{H1} or V_{H2} at turn-on, while it either takes the voltage V_{L1} or V_{L2} at turn-off. Depending on when the voltage source is applied to the gate during the switching transients, different switching properties can be achieved, as is explained below.

1) Turn-on Modes: The driver's operation for the different main modes during turn-on switching transients is presented in the following subsections. It should be specified that the driver can operate in different ways and versions of the 5 presented modes, e.g. i_D overshoot reduction or frequency spectrum control (as it will be shown for the VVSMGD in Section IV).

a) Turn-on Full Over-Drive Mode: The overall turn-on time T_{on} and turn-on switching energy E_{on} can be controlled by applying the turn-on full over-drive mode. As illustrated in Fig. 12a, by applying V_{H1} with a higher voltage level than V_H, T_{on} can be reduced. The full over-drive mode is initiated by applying the voltage source V_{H1} to the gate at the time instant t_0 by turning Q_1 on, while turning Q_4 off. At the time instant t_3^*, the voltage level V_{H2} is applied to the gate by turning Q_3 on while turning Q_1 off, removing V_{H1} from the gate. This results in the reduced turn-on time $T_{on}^* = t_3^* - t_0$, as well as reduced turn-on delay time $T_{d(on)}$ and switching energy, E_{on}.

b) Turn-on Delay Control Mode: The turn-on delay time $T_{d(on)}$ can be manipulated by applying the voltage source V_{H1} in the time-range $[t_0^{on}, t_1^{on}]$ (see Fig. 2b). As illustrated in Fig. 12b, by applying V_{H1} with a higher voltage level than V_H, $T_{d(on)}$ can be reduced. Assuming the device is in the off-state, the turn-on delay control mode is initiated by applying the voltage source V_{H1} to the gate at time instant t_0 by turning Q_1 on, while turning Q_4 off. At time instant t_1^*, the voltage level V_{H2} is applied to the gate by turning Q_3 on while turning Q_1 off, removing V_{H1} from the gate. This results in the reduced turn-on delay time $T_{d(on)}^* = t_1^* - t_0$, as well as reduced T_{on} and E_{on}.

c) Turn-on di/dt Control Mode: The device di/dt can be controlled with the turn-on di/dt control mode. By applying V_{H1} with a higher voltage level than V_H during i_D rise time, di/dt can increase, without significantly affecting the device dv/dt, as illustrated in Fig. 12c. The turn-on is initiated by turning Q_3 on while turning Q_4 off, applying V_{H2} to the gate. The mode is initiated by applying the voltage source V_{H1} to the gate at time instant t_1 by turning Q_1 on, while turning Q_3 off. At time instant t_2^*, the voltage level V_{H2} is again applied to the gate by turning Q_3 on while turning Q_1 off, removing V_{H1} from the gate. Thus, the device's di/dt increases, while dv/dt is the same. This operating mode will also reduce T_{on} and E_{on}.

d) Turn-on dv/dt Control Mode Mode: The device dv/dt can be controlled with the turn-on dv/dt control mode. By applying V_{H1} with a higher voltage level than V_H during v_{DS} fall time after i_D has reached the load current value I_D, the $|dv/dt|$ can increase, as illustrated in Fig. 12d. The turn-on is initiated by turning Q_3 on while turning Q_4 off, applying V_{H2} to the gate. This mode is initiated by applying the voltage source V_{H1} to the gate at t_2 by turning Q_1 on, while turning Q_3 off. At t_3^*, the voltage level V_{H2} is applied to the gate by turning Q_3 on again while turning Q_1 off, removing V_{H1} from the gate. Therefore, $|dv/dt|$ can increase, while keeping di/dt the same. This mode will reduce T_{on} and E_{on}.

e) Turn-on di/dt and dv/dt Control Mode: The device di/dt and dv/dt can be controlled with the turn-on di/dt and dv/dt control mode. If V_{H1} with a higher voltage level than V_H is applied during i_D rise time and v_{DS} fall time, di/dt and $|dv/dt|$ can increase, as depicted in Fig. 12e. The turn-on is initiated by turning Q_3 on while turning Q_4 off, applying V_{H2} to the gate. The mode is initiated by applying the voltage source V_{H1} to the gate at t_1 by turning Q_1 on, while turning Q_3 off. At t_3^*, the voltage level V_{H2} is applied to the gate by turning Q_3 on while turning Q_1 off, removing V_{H1} from the gate. This results in increased device di/dt and $|dv/dt|$ while maintaining $T_{d(on)}$. This mode will also reduce T_{on} and E_{on}.

2) Turn-off Modes: The driver operation for the different operating modes during turn-off switching transients is presented in the following subsections.

a) Turn-off Full Over-drive Mode: The overall turn-off time T_{off} and turn-off switching energy E_{off} can be controlled by applying the turn-off full over-drive mode. As illustrated in Fig. 13a, by applying V_{L1} with a lower voltage level than V_L, T_{off} can be reduced. The full over-drive mode is initiated by applying the voltage source V_{L1} to the gate at t_0 by turning Q_2 on, while turning Q_3 off. At t_3^*, the voltage level

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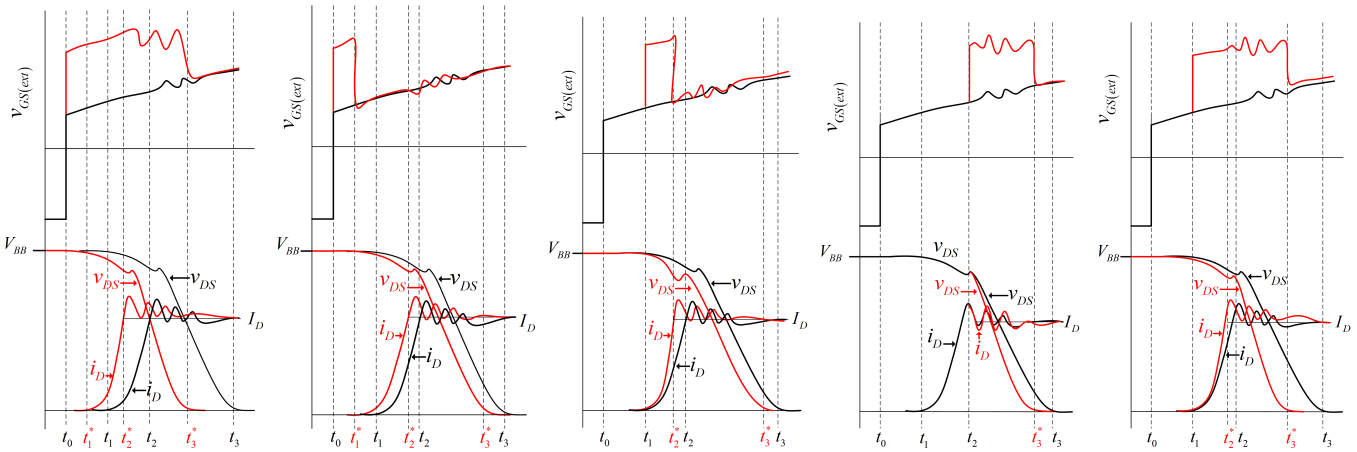
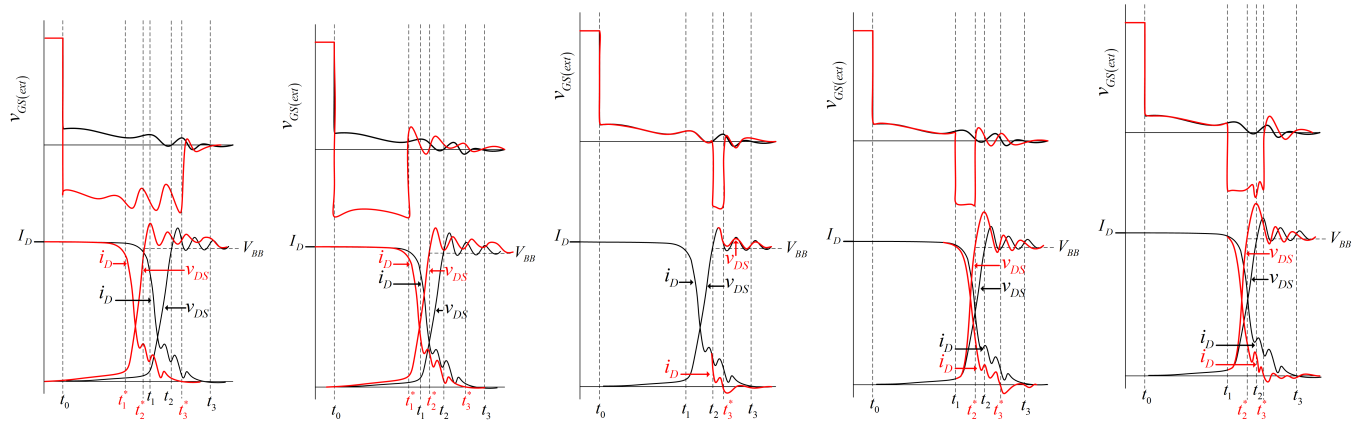


(a) Turn-on full over-drive mode theoretical waveforms. (b) Turn-on delay control mode theoretical waveforms. (c) Turn-on di/dt control mode theoretical waveforms (d) Turn-on dv/dt control mode theoretical waveforms. (e) Turn-on di/dt and dv/dt control mode theoretical waveforms.

Fig. 12. The adaptive voltage source over-driver (AVSOD) 5 key operation modes theoretical waveforms during turn-on transition.



(a) Turn-off full over-drive mode theoretical waveforms. (b) Turn-off delay control mode theoretical waveforms. (c) Turn-off di/dt control mode theoretical waveforms. (d) Turn-off dv/dt control mode theoretical waveforms. (e) Turn-off di/dt and dv/dt control mode theoretical waveforms.

Fig. 13. The adaptive voltage source over-driver (AVSOD) 5 key operation modes theoretical waveforms during turn-off transition.

V_{L2} is applied to the gate by turning Q_4 on while turning Q_2 off, removing V_{HL1} from the gate. This results in the reduced turn-on time $T^*_{off} = t^*_3 - t_0$, as well as reduced $T_{d(off)}$ and E_{off}.

b) Turn-off Delay Mode: The turn-off delay time $T_{d(off)}$ can be manipulated by applying the voltage source V_{L1} in the time-range $[t_0^{off}, t_1^{off}]$ (see Fig. 2a). As illustrated in Fig. 13b, by applying V_{L1} with a lower voltage level than V_L, $T_{d(off)}$ can decrease. Assuming the device is in the on-state, the turn-off delay control mode is initiated by applying V_{L1} to the gate at t_0 by turning Q_2 on, while turning Q_3 off. At t^*_1, V_{L2} is applied to the gate by turning Q_4 on and Q_2 off, removing V_{L1} from the gate. This results in the reduced turn-off delay time $T^*_{d(off)} = t^*_1 - t_0$, as well as reduced T_{off} and E_{off}.

c) Turn-off di/dt Control Mode: The device di/dt can be controlled during turn-off with the turn-off di/d control mode. If $V_{L1} < V_{L2}$ is applied during i_D fall time, $|di/dt|$ can increase, without affecting the device dv/dt, as illustrated in Fig. 13c. At t_0, V_{L2} is applied to the gate by turning Q_4 on while turning Q_3 off, initiating the turn-off transient. The mode is initiated by applying V_{L1} to the gate at t_2 by turning Q_2 on and Q_4 off. At t^*_3, V_{L2} is again applied to the gate by turning Q_4 on while turning Q_2 off, removing V_{L1} from the gate. Thus, $|di/dt|$ can increase while dv/dt is kept the same. This mode will also reduce T_{off} and E_{off}.

d) Turn-off dv/dt Control Mode Mode: The device's dv/dt can be controlled with the turn-off dv/dt control mode. By applying V_{L1} during v_{DS} rise time, dv/dt can increase, as illustrated in Fig. 13d. The turn-off transient is initiated at t_0 by turning Q_4 on and Q_3 off, applying V_{L2} to the gate. At t_1, V_{L1} is supplied to the gate by turning Q_2 on and Q_4 off, removing V_{L2} from the gate. V_{L2} is again applied to the gate at t^*_3, removing V_{L1} from the gate, by turning Q_4 on and Q_2 off. This results in increased device $|dv/dt|$, and as a result,

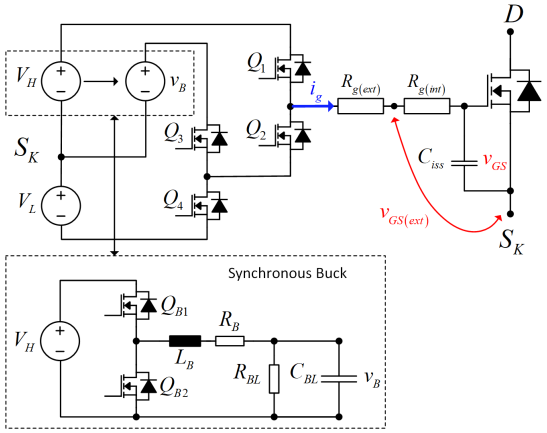


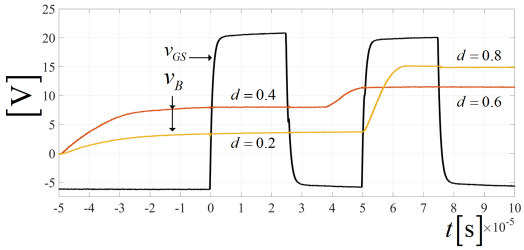
Fig. 14. The variable voltage source multi-level gate driver (VVSMGD) circuit schematic showing the 4-switched $Q_1 - Q_4$ driver circuit with the integrated synchronous buck converter with the switches Q_{B1} and Q_{B1}.

increased di/dt. This mode will reduce T_{off} and E_{off}.

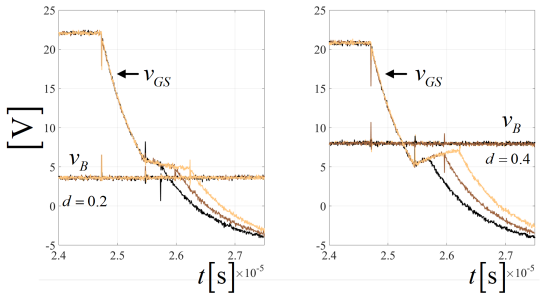
e) Turn-off di/dt and dv/dt Control Mode: The device's di/dt and dv/dt can be controlled with the turn-off di/dt and dv/dt control mode. By applying V_{L1} during v_{DS} rise time and i_D fall time, $|di/dt|$ and dv/dt can increase, as illustrated in Fig. 13e. The turn-off is initiated by turning Q_4 on while turning Q_3 off, applying V_{L2} to the gate. The mode is initiated by applying V_{L1} to the gate at t_1 by turning Q_2 on and Q_4 off. At t_3^*, V_{L2} is applied to the gate by turning Q_4 on while turning Q_2 off, removing V_{L1} from the gate. This results in increased device dv/dt and $|di/dt|$ while keeping $T_{d(off)}$ the same. This mode will reduce T_{off} and E_{off}.

IV. Variable Voltage Source Multi-level Gate Driver

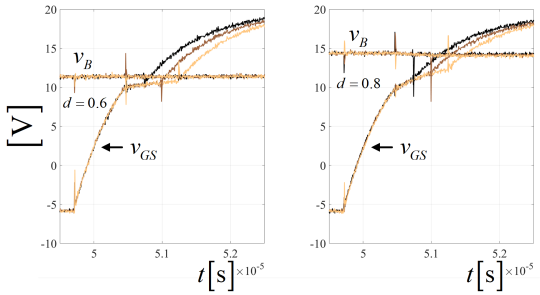
This section presents a novel voltage-source gate driver topology with variable voltage source and multi-level voltage driving capabilities. The variable voltage source multi-level gate driver (VVSMGD) circuit schematic is shown in Fig. 14 and it is based on the circuit topology introduced by Zhao et al. [56], [57], [62], [63]. The driver utilises three voltage sources $V_H > v_B > V_L$ where the fixed voltage V_H is the highest voltage level, v_B is the variable middle voltage and derived from V_H and the fixed V_L is the lowest off-state voltage level. The voltage sources provide the gate current i_g to the MOSFET gate through the gate resistors $R_g = R_{g(ext)} + R_{g(int)}$. The multi-level driving capability is achieved by the two half-bridge circuits comprising Q_1/Q_2 and Q_3/Q_4 and by introducing a buck converter in the circuit, the variable mid-level voltage is achieved. The intermediate voltage v_B is controlled by adjusting the duty-cycle d of the buck converter through the expression $v_B = d \cdot V_H$, where V_H is the high state, positive gate driver voltage. The varying behavior of v_B can also be seen from the experimental results in Fig. 15. With the proposed VVSMGD, the intermediate voltage v_B can vary in real-time based on the driving needs, which is a limitation with the fixed intermediate voltage in the multi-level gate driver introduced in [56].



(a) Double pulse testing of the VVSMGD on a passive load with duty cycle d changes.



(b) Turn-off test with $d = 0.2$ and $d = 0.4$ with different t_n^{vos} timing values.



(c) Turn-on test with $d = 0.6$ and $d = 0.8$ with different t_n^{ios} timing values.

Fig. 15. VVSMGD test on passive RC-load.

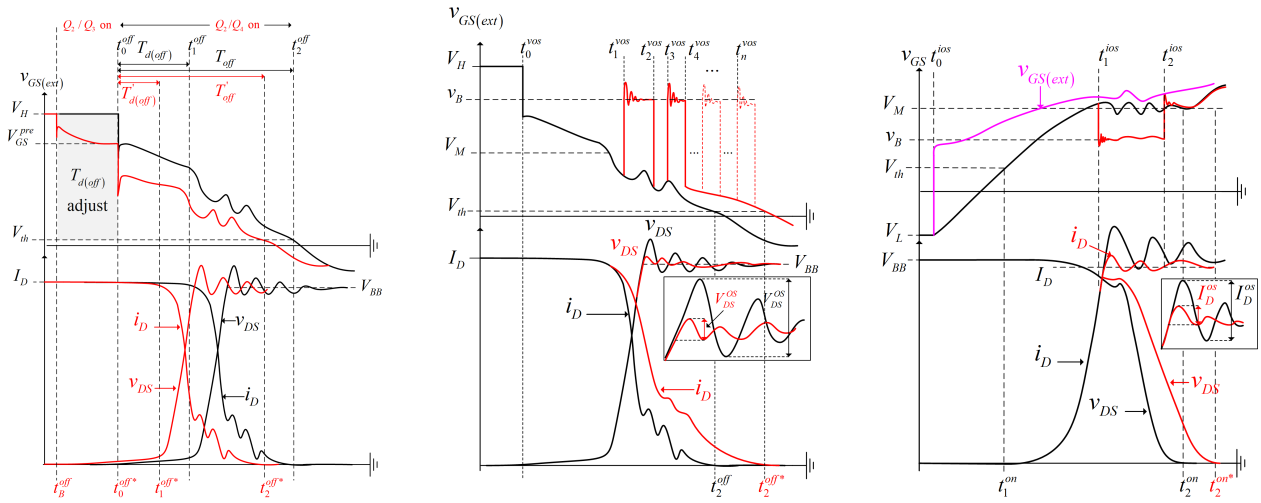
The VVSMGD has several operating modes which can be used separately or together and they are described in the following subsections.

A. Turn-off Delay Manipulation

The device turn-off delay time $T_{d(off)}$ can be manipulated by providing the variable voltage source v_B to the gate prior to the actual turn-off instant, as illustrated in Fig. 16a. By adjusting the duty-cycle d of the buck converter, v_B can be set to a pre-defined voltage level $v_B = V_{GS}^{pre}$. Turning Q_2 and Q_3 on at t_B^{off}, applies v_B to the gate to adjust the turn-off delay time and turn-off time of the DUT. The turn-off transition is then initiated by turning Q_3 off at $t_0^{off^*}$, while turning Q_4 on, applying V_L to the gate. Thus, $T_{d(off)}$ and T_{off} can be adjusted depending on the value V_{GS}^{pre}.

B. Turn-off Voltage Overshoot Manipulation

By controlling v_{GS} during v_{DS} overshooting oscillatory behaviour, the magnitude of the overshoot V_{DS}^{OS} and frequency spectrum of the oscillations can be manipulated. Due to the



(a) Turn-off delay manipulation theoretical waveforms.

(b) Turn-off voltage overshoot manipulation and frequency spectrum control theoretical waveforms.

(c) Turn-on current overshoot and frequency spectrum manipulation theoretical waveforms.

Fig. 16. Theoretical waveforms of the variable voltage source multi-level gate driver (VVSMGD) shown in red color and compared to theoretical waveforms using the CVSGD (black lines).

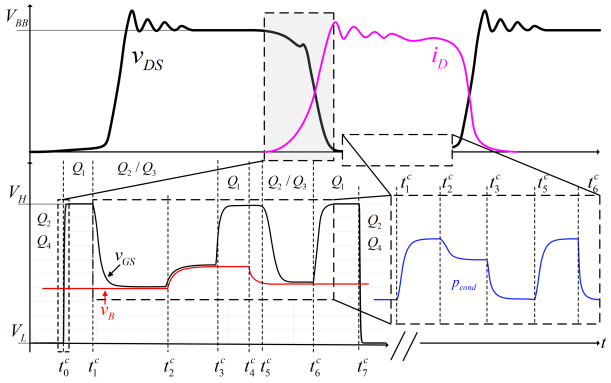


Fig. 17. Theoretical waveform of the conduction loss manipulation.

falling i_D and the unavoidable parasitic inductance L_{eq} of the power module layout and power circuit loop, the anticipated voltage overshoot approximately equals to

$$V_{DS}^{OS} = L_{eq}\frac{di_D}{dt} \tag{21}$$

By manipulating v_{GS} while the MOSFET is in the saturation region, the slope of i_D can be adjusted (as seen from "(3)"). Thus, the overshoot and oscillatory behaviour of v_{DS} can be controlled, as illustrated in Fig. 16b.

C. Turn-on Current Overshoot Manipulation

Similarly to the turn-off voltage overshoot manipulation, by controlling v_{GS} during i_D peak time (i.e. when v_{GS} reaching the Miller plateau and v_{DS} is falling) the i_D peak value can be manipulated as illustrated in Fig. 16c.

Both turn-off voltage overshoot manipulation (Section IV-B) and turn-on current overshoot manipulation cause both the v_{DS} and i_D slew rate to reduce, hence increasing the switching loss.

D. Conduction Loss Manipulation

By manipulating v_{GS} during DUT conduction, the value of the drain-source on-state resistance $r_{DS(on)}$ can be adjusted, based on the $r_{DS(on)} - (v_{GS})$ plot shown in Fig. 3b. Thus, the drain-source voltage $v_{DS(on)} = r_{DS(on)} \cdot i_D$ is controllable and consequently the instantaneous conduction loss

$$p_{cond} = v_{DS(on)} \cdot i_D \tag{22}$$

can also be adjusted.

By applying v_B to the gate during conduction phase and adjusting v_B, p_{cond} can be controlled. The driver switches Q_2 and Q_3 are turned on while Q_1 and Q_4 are turned off, and by adjusting the buck converter duty-cycle d, $p_{cond}(d)$ can be controlled to a desired value.

An illustration of theoretical conduction loss manipulation concept is shown in Fig. 17. The DUT is turned on at $t = t_0^c$ by turning Q_1 on. At t_1^c, the synchronous buck voltage v_B is applied to the gate by turning Q_1 off while turning Q_2 and Q_3 on. The voltage v_B can be varied according to the duty-cycle of the synchronous buck, as seen at time t_2^c and t_4^c. The applied gate voltage can be varied between V_H and v_B, as is illustrated at time instants t_3^c and t_5^c. The DUT is turned off at t_7^c by turning Q_1 and Q_3 off, while turning Q_2 and Q_4 on. This constitute a variable conduction loss p_{cond}, as illustrated ith blue waveforms color in Fig. 17.

The load capacitance value on the synchronous buck, C_{BL} is chosen as a compromise between minimal voltage variation in v_B during application of v_B to the gate, and the ability of v_B to change value within certain time periods as response to change in the duty cycle, d. The applied on-pulses from the

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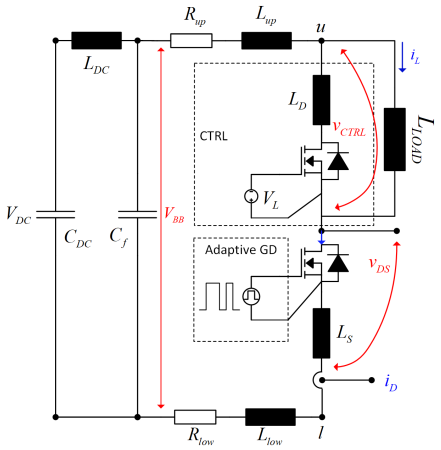
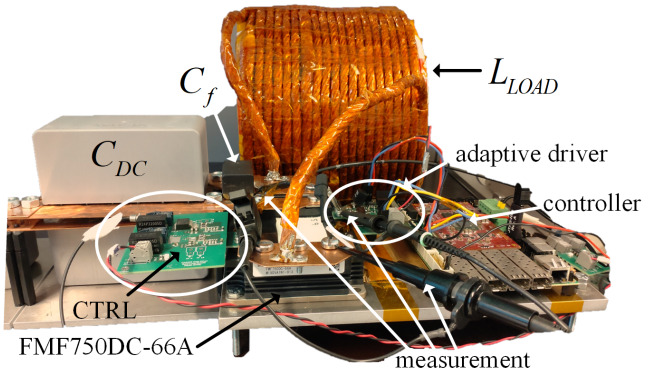


(a) Double pulse test (DPT) equivalent circuit schematic.



(b) Photo of the experimental setup.

Fig. 18. Double pulse test (DPT) setup.

buck converter, draw or inject current depending on whether v_B is higher or lower than v_{GS} at the time of applying v_B. The current drawn from C_{BL} when applying v_B at the gate is given by

$$i_{C_{BL}} = \frac{v_B - v_{GS}}{R_g} \tag{23}$$

To confine v_B within a certain voltage variation Δv_B, the capacitance of C_{BL} should then be chosen as

$$C_{BL} = T_{\Delta}^{VOS}\left(\frac{i_{C_{BL}}}{\Delta v_B}\right) \tag{24}$$

where T_{Δ}^{VOS} is the time duration of applying v_B, i.e. $T_{\Delta}^{VOS} = t_n^{VOS} - t_{n-1}^{VOS}$ in Fig. 16b. Having chosen the desired value of C_{BL}, the other passive components of the synchronous buck are calculated to obtain a critically damped response in v_B, i.e., $R_B = 2\sqrt{(L_B/C_B)}$. The synchronous buck switching frequency is chosen as a compromise between the capability of the circuit components and controller, size of passive components and bandwidth of the synchronous buck.

V. Experimental Results

The performance of the proposed adaptive gate drivers was experimentally validated on a double-pulse test (DPT) circuit

TABLE V
Double Pulse Test Circuit Parameters

L_D	L_S	L_{up}	L_{low}	L_{LOAD}	C_f	C_{DS}
7nH	7nH	20nH	20nH	80μH	10μF	800μF

TABLE VI
Measurement Equipment

Scope	Tektronix MSO 5104	$f_{bw} = 1$GHz, 10GS/s.
Voltage Probe v_{DS}	Tektronix P5100A	$f_{bw} = 500$MHz
Voltage Probe $v_{GS(ext)}$	Tektronix TPP0500B	$f_{bw} = 500$MHz
Current Probe i_D	PEM CWTUM	$f_{bw} = 30$MHz

as illustrated in Fig. 18a with a photo of the experimental setup shown in Fig. 18b. The setup employs a high-voltage 3.3 kV, 750 A SiC MOSFET half-bridge power module (Mitsubishi FMF750DC-66A) connected to an inductive load. The electrical parameters of the DPT are listed in Table V. The busbar inductances L_{up} and L_{low} as well as the load inductance L_{LOAD} have been measured using the Keysight E4990A Impedance Analyser. Table VI summarizes the measurement equipment used during testing. The PicoZed 7030 (xc7z30sbg485-1) SOM's FPGA is used for the controller and adaptive driver signals generation. The FPGA has a maximum clock frequency of $f_{clk} = 250$MHz yielding a minimum signal pulse-width of 4ns. Moreover, for the practical implementation of the active switches on the circuit boards of the three adaptive gate drivers, (i.e., Q_1, Q_2, Q_3, Q_4 and also Q_{B1}, Q_{B2} for the DC/DC buck in the VVSMGD), the Silicon MOSFET #3 (DMN6040SVT) from Table II in the manuscript has been chosen. This device has voltage rating of 60 V and a continuous current rating of 4.3 A at 25^{o}C, with a peak current rating of 30 A. Driving the low-voltage Silicon MOSFETs is done by utilizing an integrated drive circuit (LM25101AMX), which is driven through a signal isolator (ISO7420MD).

A. Adaptive Current Source Over-Driver

A photograph of the printed circuit board (PCB) shown in Fig. 19. Experimental results of the ACSOD (section III-A) for varying pre-charged peak current ($I_m = 6 - 16$A) are shown in Fig. 20 for the turn-on transient and in Fig. 21 for the turn-off transient. For both cases, the maximum value of the pre-charged current i_m amplitude $I_{m(max)}$ is estimated by "(14)". The lowest testing I_m current corresponds to the gate current that would be supplied in case of a CVSGD. From these measurements, it is observed that by varying I_m, the turn-on and turn-off delay times, as well as turn-on and turn-off switching energies can be manipulated. Table VII presents the numerical results of these three parameters for the experimental results shown in these two figures. From this table, it is observed that a reduction of 61.76% in $T_{d(on)}$ is achieved for a peak I_m of 16A. Similarly, the turn-on

TABLE VII
TURN-ON AND TURN-OFF EXPERIMENTAL DATA USING THE ACSOD FOR $I_D = 300$A AND $V_{BB} = 800$V.

	I_m[A]	5	7.5	10	12.5	16
$T_{d(on)}$	val [ns]	330	280	230	190	130
	% ↓	2.94	17.64	32.59	44.11	61.76
T_{on}	val [ns]	850	750	670	560	360
	% ↓	2.29	12.64	22.98	35.63	58.62
E_{on}	val [mJ]	47.9	45.7	42.5	37.3	24.1
	% ↓	1.23	5.77	12.37	23.09	50.31
$E_{D(on)}$	val [μJ]	76.1	83.8	93.1	105.9	136.6
	% ↑	−1	9.0	21.1	37.7	77.6
$T_{d(off)}$	val [ns]	870	795	705	595	345
	% ↓	3.33	11.67	21.7	33.89	61.67
T_{off}	val [ns]	1403	1313	1211	1097	812
	% ↓	11.2	16.89	23.35	30.56	48.60
E_{off}	val [mJ]	25.62	22.42	21.91	20.9	15.63
	% ↓	4.22	16.19	18.13	21.86	41.57
$E_{D(off)}$	val [μJ]	111.2	117.6	125.8	136.2	165.0
	% ↑	0.7	6.5	13.9	23.4	49.5

time, T_{on} is reduced by 58.62% and the switching energy by 50.31%. The corresponding decrease for turn-off transients are 61.67%, 48.6% and 41.57%. It should be noted that the percentage reduction values are compared to CVSGD with $R_{g(ext)} = 1.2\Omega$.

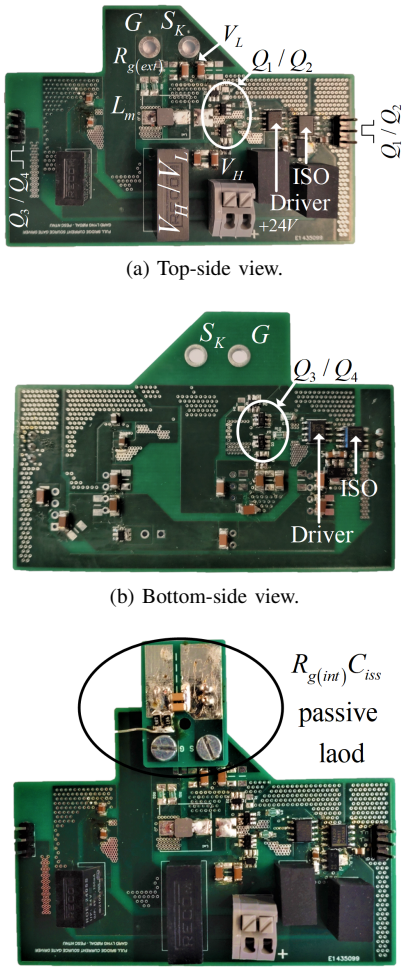
B. Adaptive Voltage Source Over-Driver

The PCB of the AVSOD is shown in Fig. 22. Experimental results of the turn-on and turn-off switching transients are presented in the following subsections.

1) Turn-on Full Over-Drive Mode: Experimental results of the AVSOD showing the turn-on full over-drive mode (section III-B1a) under various values of V_{H1} are shown in Fig. 23. Key performance data of the AVSOD for this mode of operation have been extracted from the experimental measurements and are presented in Table VIII. It is observed that by increasing V_{H1} to 40V, the turn-on delay time, $T_{d(on)}$ can be reduced by 41%, the turn-on time, T_{on} by 46% and turn-on energy, E_{on} by 50%.

2) Turn-on Delay Control Mode: Experimental results of the AVSOD showing the turn-on delay control mode (section III-B1b) for different values of V_{H1} are illustrated in Figs. 24a-24b, while Table IX summarizes key data extracted from the measurements. It can be seen that for $V_{H1} = 40$V, $T_{d(on)}$ can be reduced by 41%, whereas the reduction of T_{on} is lower compared to mode 1 of the AVSOD.

3) Turn-on di/dt Control Mode: Experimental results of the AVSOD showing the turn-on di/dt control mode (section III-B1c) for various values of V_{H1} are shown in Figs. 24c-24d. Table X summarizes key experimental data of di/dt and E_{on}

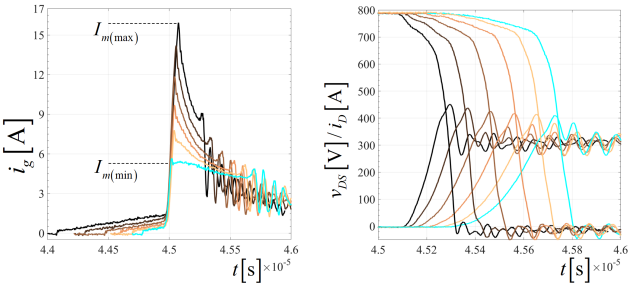


(a) Top-side view.

(b) Bottom-side view.

(c) Top-side view with passive RC-load.

Fig. 19. Photograph of the ACSOD printed circuit board (PCB).



(a) Gate current i_g.

(b) Drain-source voltage v_{DS} and drain current i_D.

Fig. 20. ACSOD turn-on waveforms for varying values of I_m.

control as V_{H1} varies. From these plots, it is seen that dv/dt is approximately constant and equals $dv/dt \approx 5.5$V/ns across all V_{H1} levels, while di/dt can be adjusted in a range between 23% to 93% and E_{on} up to 33%.

4) Turn-on dv/dt Control Mode: Figs. 24e-24f illustrate experimental results of the turn-on dv/dt control mode (section III-B1d) using the AVSOD, where as shown in Table XI dv/dt can vary up to 57% when $V_{H1} = 40$V. Using this mode

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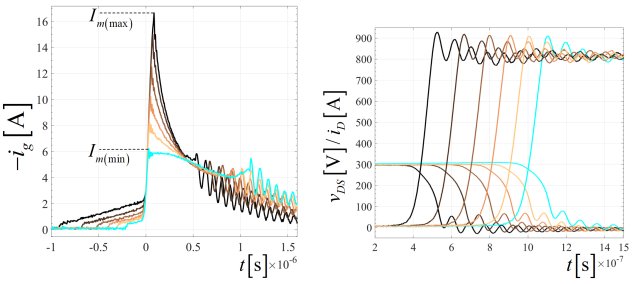
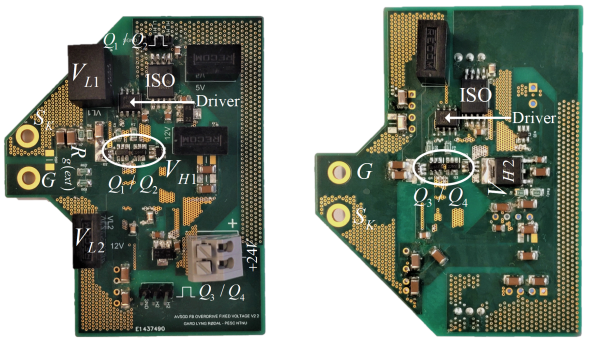


(a) Gate current i_g. (b) Drain-source voltage v_{DS} and drain current i_D.

Fig. 21. ACSOD turn-off waveforms for varying values of I_m.



(a) Top-side view. (b) Bottom-side view.

Fig. 22. Photograph of the AVSOD printed circuit board (PCB).

of operation, di/dt is kept constant at $di/dt \approx 0.85$A/ns across all V_{H1} levels.

5) Turn-on di/dt and dv/dt Control Mode: Controlling dv/dt and di/dt simultaneously also becomes possible with the proposed AVSOD, as shown in the turn-on experimental results of Figs. 24g-24h. For a value of $V_{H1} = 40$V, dv/dt can increase by 57%, while di/dt increases by 178% (Table XII). It is worth mentioning that with this control mode of the AVSOD, the peak value of the drain current $\hat{I}_D$ can also be controlled.

TABLE VIII
TURN-ON EXPERIMENTAL DATA USING THE AVSOD IN FULL OVER-DRIVE MODE FOR $I_D = 300$A AND $V_{BB} = 800$V.

	V_{H1}[V]	20	25	30	35	40
$T_{d(on)}$	val [ns]	340	320	270	230	200
	% ↓		5.88	20.58	32.35	41.17
T_{on}	val [ns]	870	810	660	550	470
	% ↓		6.89	24.13	36.78	45.97
E_{on}	val [mJ]	48.5	44.6	34.6	28.5	24.2
	% ↓		8.04	28.65	41.23	50.10
$E_{D(on)}$	val [μJ]	76.9	87.3	107.1	124.8	143.0
	% ↑		13.5	37.3	62.3	86.0

TABLE IX
TURN-ON DELAY CONTROL EXPERIMENTAL DATA USING THE AVSOD FOR $I_D = 300$A AND $V_{BB} = 800$V.

	V_{H1}[V]	20	25	30	35	40
$T_{d(on)}$	val [ns]	340	320	270	230	200
	% ↓		5.88	20.58	32.35	41.17
T_{on}	val [ns]	870	850	780	740	710
	% ↓		2.29	10.34	14.94	18.39
E_{on} [mJ]		48.5	48.3	47.9	48.0	48.8

TABLE X
TURN-ON di/dt CONTROL MODE EXPERIMENTAL DATA USING THE AVSOD FOR $I_D = 300$A AND $V_{BB} = 800$V.

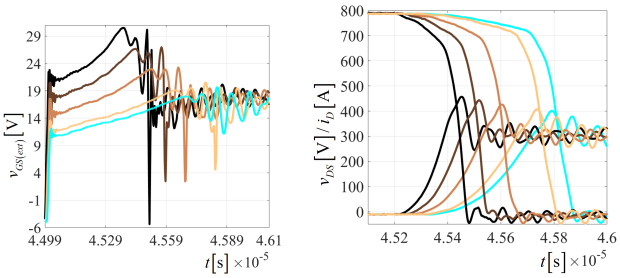
	V_{H1}[V]	20	27.5	30	35	40
di/dt	val [A/ns]	0.85	1.04	1.16	1.40	1.63
	% ↑		23.4	37.24	65.91	92.69
E_{on}	val [mJ]	48.5	42.0	39.2	34.4	32.6
	% ↓		13.40	19.17	29.07	32.78

TABLE XI
TURN-ON dv/dt CONTROL MODE EXPERIMENTAL DATA USING THE AVSOD FOR $I_D = 300$A AND $V_{BB} = 800$V.

	V_{H1}[V]	20	30	35	40
$\lvert dv/dt \rvert$	val [V/ns]	5.45	6.67	7.50	8.57
	% ↑		22.22	37.50	57.14
E_{on}	val [mJ]	48.50	47.85	47.04	45.05
	% ↓		1.32	2.99	7.11

TABLE XII
TURN-ON di/dt AND dv/dt CONTROL MODE EXPERIMENTAL DATA USING THE AVSOD FOR $I_D = 300$A AND $V_{BB} = 800$V.

	V_{H1}[V]	20	27.5	30	35	40
di/dt	val [A/ns]	0.85	1.28	1.42	1.92	2.35
	% ↑		51.01	67.82	127.0	178.1
I_D^{OS}	$\hat{I}_D$[A]	400	417	428	441	456
	% ↑		17	28	41	56
$\lvert dv/dt \rvert$	val [V/ns]	5.45	5.71	6.0	6.67	8.57
	% ↑		4.76	10.0	22.22	57.14
E_{on}	val [mJ]	48.5	38.79	34.35	28.23	24.14
	% ↓		20.02	29.17	1.79	50.22



(a) $v_{GS(ext)}$ mode 1) turn-on. (b) v_{DS}/i_D mode 1) turn-on.

Fig. 23. The adaptive voltage source over-driver (AVSOD) turn-on operation mode 1) as described in section III-B for $I_D = 300A$ and $V_{BB} = 800V$.

TABLE XIII
TURN-OFF FULL OVER-DRIVE MODE EXPERIMENTAL DATA USING THE AVSOD FOR $I_D = 300$A AND $V_{BB} = 800$V.

	V_{L1}[V]	-5	-15	-24
$T_{d(off)}$	val [ns]	880	530	400
	% ↓		39.77	54.54
T_{off}	val [ns]	1580	870	710
	% ↓		44.93	55.06
E_{off}	val [mJ]	26.75	13.25	9.74
	% ↓		50.46	63.58
$E_{D(off)}$	val [μJ]	110.4	155.8	204.5
	% ↑		41.2	85.2

6) Turn-off Full Over-Drive Mode: Experimental results of the AVSOD showing the turn-off full over-drive mode (section III-B2a) are shown in Fig. 25. From the analysis of the experimental results, it is revealed that the turn-off delayed time, $T_{d(off)}$, can be reduced by 54%, the turn-off time, T_{off}, by 55% and the turn-off energy, E_{off} by 63%, when $V_{L1} = -24$V (Table XIII).

7) Turn-off Delay Control Mode: The turn-off delay control mode of the AVSOD (section III-B2b) is experimentally shown in Figs. 26a-26b, while from Table XIV it is observed that by applying $V_{L1} = -24$V to the external gate circuit, $T_{d(off)}$ can be reduced by 54% and T_{off} by 42%.

8) Turn-off di/dt Control Mode: Experimental results of the AVSOD showing the turn-off di/dt control mode (section III-B2c) are presented in Figs. 26c-26d. Based on these results, it is clear that di/dt is able to increase by approximately 81% for $V_{L1} = -24$V resulting in a 18% reduction of E_{off} value (Table XV). For this mode of AVSOD's operation, dv/dt is approximately constant at $dv/dt \approx 4$V/ns.

TABLE XIV
TURN-OFF DELAY CONTROL MODE EXPERIMENTAL DATA USING THE AVSOD FOR $I_D = 300$A AND $V_{BB} = 800$V.

	V_{L1}[V]	-5	-15	-24
$T_{d(off)}$	val [ns]	880	530	400
	% ↓		39.77	54.54
T_{off}	val [ns]	1580	1150	910
	% ↓		27.21	42.40
E_{off} [mJ]		26.75	26.60	24.91

TABLE XV
TURN-OFF di/dt CONTROL MODE EXPERIMENTAL DATA USING THE AVSOD FOR $I_D = 300$A AND $V_{BB} = 800$V.

	V_{L1}[V]	-5	-15	-24
$\lvert di/dt \rvert$	val [A/ns]	0.461	0.795	0.838
	% ↑		72.22	81.53
E_{off}	val [mJ]	26.75	22.30	21.90
	% ↓		16.48	17.98

TABLE XVI
TURN-OFF dv/dt CONTROL MODE EXPERIMENTAL DATA USING THE AVSOD FOR $I_D = 300$A AND $V_{BB} = 800$V.

	V_{L1}[V]	-5	-15	-24
dv/dt	val [V/ns]	4.05	5.5	7.0
	% ↑		35.71	72.72
$\lvert di/dt \rvert$	val [A/ns]	0.46	0.96	1.42
	% ↑		109.6	209.5
E_{off}	val [mJ]	26.75	15.77	11.10
	% ↓		41.04	58.50

9) Turn-off dv/dt Control Mode: The turn-off dv/dt control mode of the AVSOD (section III-B2d) is experimentally shown in Figs. 26e-26f, while the numerical results of dv/dt, di/dt and E_{off} manipulation are given in Table XVI. In particular, for $V_{L1} = -24$V, dv/dt increases by 72%, di/dt increases by 210%, leading to a 58% decrease of E_{off}.

10) Turn-off di/dt and dv/dt Control Mode: Finally, experimental results of the AVSOD showing the turn-off di/dt and dv/dt control mode (section III-B2e) are shown in Figs. 26g-26h. As summarized in Table XVII, dv/dt can increase by approximately 73% and di/dt by 219% when $V_{L1} = -24$V. Moreover, the controllability of V_{DS}^{OS} is also shown in this table.

C. Adaptive Current Source and Voltage Source Over-Drive Comparison

To assess the ACSOD and AVSOD performance in terms of turn-on/off delay time, turn-on/off time and turn-on/off switching energy, the drivers in over-drive mode have been tested across a set of load currents and blocking voltages. The over-drive performance of the ACSOD with varying values of the current i_m amplitude I_m is shown in Fig. 28a while the over-drive performance of the AVSOD with varying values of the V_{H1} is shown in Fig. 28b. The same performance metrics are evaluated at turn-off in Fig. 29a for the ACSOD and Fig. 29b for the AVSOD, all compared to the CVSGD.

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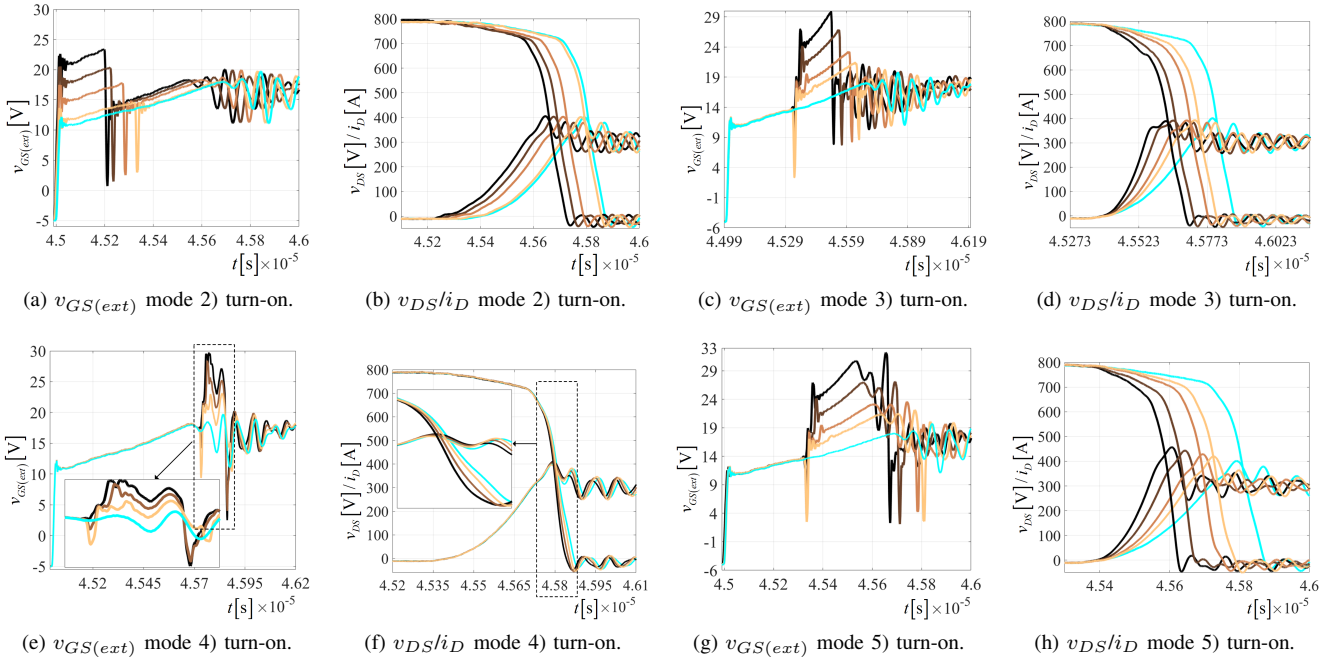
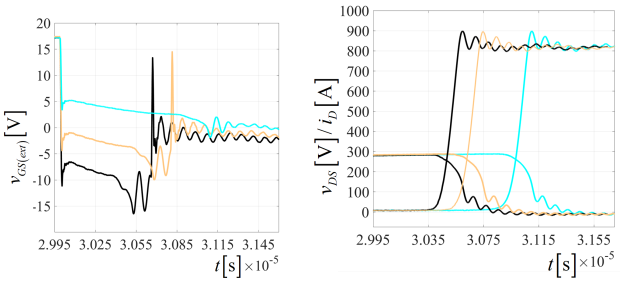


(a) $v_{GS(ext)}$ mode 2) turn-on. (b) v_{DS}/i_D mode 2) turn-on. (c) $v_{GS(ext)}$ mode 3) turn-on. (d) v_{DS}/i_D mode 3) turn-on.

(e) $v_{GS(ext)}$ mode 4) turn-on. (f) v_{DS}/i_D mode 4) turn-on. (g) $v_{GS(ext)}$ mode 5) turn-on. (h) v_{DS}/i_D mode 5) turn-on.

Fig. 24. The adaptive voltage source over-driver (AVSOD) turn-on operation modes 2)-5) as described in section III-B for $I_D = 300$A and $V_{BB} = 800$V.



(a) $v_{GS(ext)}$ mode 6) turn-off. (b) v_{DS}/i_D mode 6) turn-off.

Fig. 25. The adaptive voltage source over-driver (AVSOD) turn-off operation mode 6) as described in section III-B for $I_D = 300$A and $V_{BB} = 800$V.

TABLE XVII
TURN-OFF di/dt AND dv/dt CONTROL MODE EXPERIMENTAL DATA USING THE AVSOD FOR $I_D = 300$A AND $V_{BB} = 800$V.

	V_{L1}[V]	-5	-15	-24
dv/dt	val [V/ns]	4.05	5.5	7.0
	% ↑		35.71	72.72
V_{DS}^{OS}	$\hat{V}_{DS}$[V]	898	936	956
	% ↑		38.77	59.18
$\lvert di/dt \rvert$	val [A/ns]	0.46	1.07	1.47
	% ↑		133.3	219.3
E_{off}	val [mJ]	26.75	13.72	9.99
	% ↓		48.72	62.66

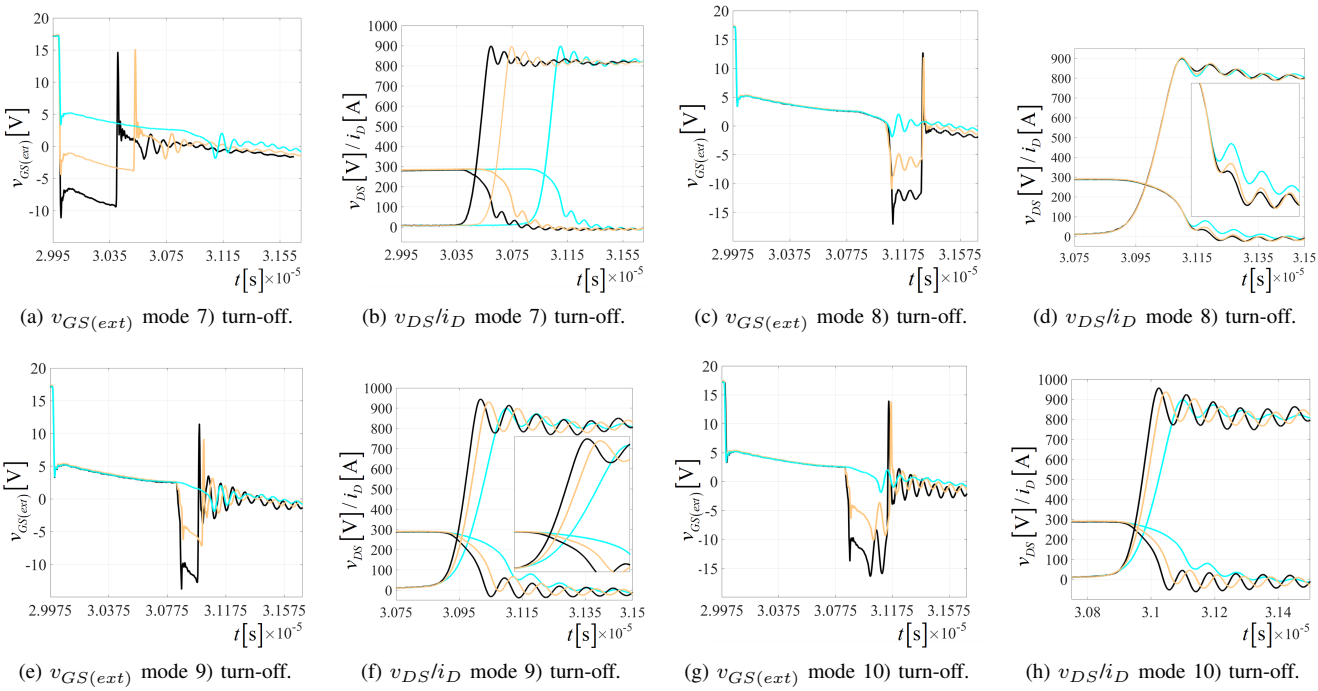
From Fig. 28, it can be seen that the controllability window becomes wider when utilising the ACSOD, where the values of $T_{d(on)}$ can be manipulated from 0% to approximately 80%, the value of T_{on} between 0% to approximately 70% and finally E_{on} can vary from 0% to approximately 60%, compared to 5-45%, 10-50% and 10-55% when using the AVSOD. Similarly, for the turn-off process, the controllability window for the turn-off delay time, $T_{d(off)}$, is wider for ACSOD compared to that one of the AVSOD as shown in Fig. 29, even though the manipulation range for T_{off} and E_{off} are approximately the same for ACSOD and AVSOD. However, as it is illustrated in Fig. 27, the cost for the larger manipulation window is the higher gate drive energy use from the ACSOD compared to AVSOD.

A way to decide which over-driver concept should be utilised in a power converter that exhibits adaptive operation through the adjustment of switching energies can be seen in Fig. 30. This figure shows a comparison between the turn-on energy by using the ACSOD with $I_{m(max)}$, i.e. $E_{on(I_{m(max)})}^{ACSOD}$, and when using the AVSOD with $V_{H1} = 40$V, i.e. $E_{on(V_{H1}=40\text{V})}^{AVSOD}$, and $V_{H1} = 30$V, i.e. $E_{on(V_{H1}=30\text{V})}^{AVSOD}$ (Fig. 30a). The same comparison of the turn-off energy between the ACSOD with $I_{m(max)}$, i.e. $E_{off(I_{m(max)})}^{ACSOD}$, and AVSOD with $V_{L1} = -24$V, i.e. $E_{off(V_{L1}=-24\text{V})}^{AVSOD}$, and $V_{L1} = -15$V, i.e. $E_{off(V_{H1}=-15\text{V})}^{AVSOD}$, is shown in Fig. 30b.

D. Variable Voltage Source Multi-level Gate Driver

Experimental results of the different operating modes of the VVSMGD are given in the following subsections, with a photograph of the printed circuit board (PCB) shown in Fig. 31.

1) Turn-off Delay Manipulation: Experimental results verifying the effect of the turn-off delay manipulation are shown



(a) $v_{GS(ext)}$ mode 7) turn-off. (b) v_{DS}/i_D mode 7) turn-off. (c) $v_{GS(ext)}$ mode 8) turn-off. (d) v_{DS}/i_D mode 8) turn-off.

(e) $v_{GS(ext)}$ mode 9) turn-off. (f) v_{DS}/i_D mode 9) turn-off. (g) $v_{GS(ext)}$ mode 10) turn-off. (h) v_{DS}/i_D mode 10) turn-off.

Fig. 26. The adaptive voltage source over-driver (AVSOD) turn-off operation modes 7)-10) as described in section III-B for $I_D = 300$A and $V_{BB} = 800$V.

TABLE XVIII
VVSM GATE DRIVER PARAMETERS

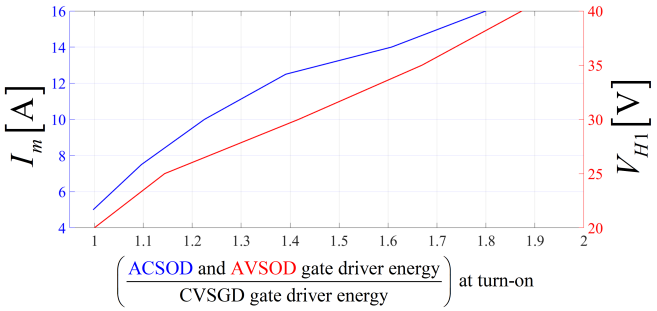
L_B	R_B	R_{BL}	C_{BL}	f_{sw_B}	$R_{g(ext)}$
3.3μH	1.4Ω	5kΩ	6.8μF	2MHz	1.2Ω

in Fig. 32. The effect of applying a variable voltage v_B to the gate prior to turn-off is clear, with a maximum reduction of 88.9% in $T_{d(off)}$, 51.7% in T_{off} and 6.7% in E_{off} comparing the maximum delay manipulation with $v_B = V_{GS}^{pre} = 9$V to no delay manipulation (marked in light blue color Fig. 32).

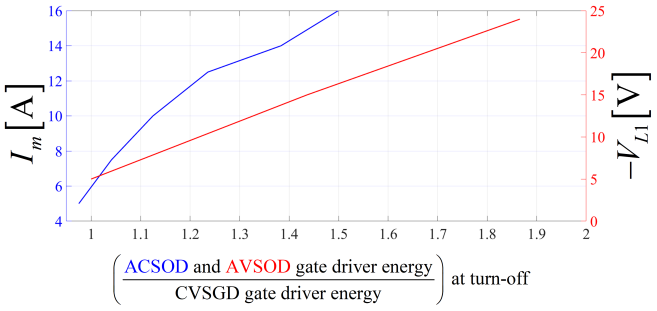
2) Turn-off Voltage Overshoot Manipulation: Experimental results demonstrating the voltage overshoot manipulation are shown in Figs. 33 and 34. In Fig. 33a, a single-pulse operation mode with two different buck voltage v_B levels is shown, resulting in different reduction in V_{DS}^{OS}. Fig. 33b presents the percentage reduction in V_{DS}^{OS} and the resulting percentage increase in the turn-off energy E_{off} over a set of v_B values compared to no overshoot manipulation (red waveforms in Fig. 33a) while operating as in Fig. 33a. Using no overshoot manipulation yields an overshoot value of $V_{DS}^{OS} = 185$V, while using a single-pulse operation mode with $v_B = 9$V yields $V_{DS}^{OS} = 103$V, i.e. a $\sim 44\%$ reduction. Using no overshoot manipulation yields a turn-off energy of $E_{off} = 0.0517$J, while using a single-pulse operation mode with $v_B = 9$V results in $E_{off} = 0.1056$J, i.e. a $\sim 104\%$ increase. Fig. 34a shows the multi–pulse operation mode of the VVSMGD with a buck voltage value of $v_B = 13$V. From these measurements, it is revealed that using a multi–pulse operation allows for both reduction in V_{DS}^{OP} as well as manipulation of the frequency spectrum imposed by v_{DS}, as seen in Fig. 34b.

3) Turn-on Current Overshoot Manipulation.: The experimental results validating the manipulation of the drain current overshoot are shown in Fig. 35. The i_D overshoot is clearly adjustable by applying v_B to the gate during the time interval where i_D reaches the peak value. As seen in Fig. 35b, using no i_D overshoot manipulation yields an overshoot of approximately $I_D^{OS} \approx 75$A at a load current level $I_D \approx 300$A and this overshoot is reduced to $I_D^{OS} \approx 20$A overshoot with $v_B = 9$V. The turn-on energy with no i_D overshoot manipulation is $E_{on} \approx 0.103$J and is increased to $E_{on} \approx 0.187$J using $v_B = 9$V. The controllability window for various values of v_B is shown in Fig. 35b, where it is observed that I_D^{OS} can be reduced up to 73% when $v_B = 9$V at a cost of 45% higher E_{on}.

4) Conduction Loss Manipulation: Exemplary experimental results showing the conduction loss manipulation mode are shown in Fig. 36. At $t = t_0^c$, the DUT is turned on with $v_{DRV} = V_H = 20$V applied to the gate. At $t = t_1^c$, Q_2 and Q_3 are turned on while Q_1 is turned off, applying $v_B = 9$V to the gate. Thus, as $v_{GS} \to v_B$, $r_{DS(on)}$ increases as observed in Fig. 3b, affecting v_{DS}. At $t = t_2^c$, v_B is still applied to the gate, but a change in the duty cycle of the buck converter from $d = 0.4 \to d = 0.6$ is performed, resulting in $v_B \to 11$V, reducing $r_{DS(on)}$ and v_{DS}. At $t = t_3^c$, V_H is applied to the gate, further reducing $r_{DS(on)}$ and v_{DS}. Again, at $t = t_4^c$, $v_B = 11$V is applied to the gate and $r_{DS(on)}$ and v_{DS} increase. The drain current i_D (red waveform) and instantaneous power loss $p = i_D \cdot v_{DS}$ (blue waveform) are shown in the lower

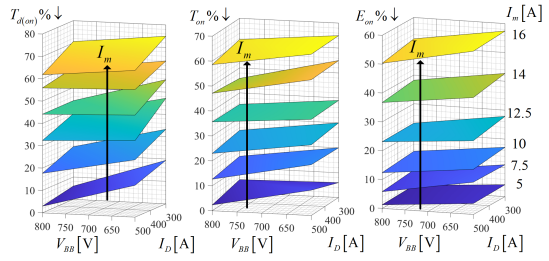


(a) Turn-on ACSOD (blue) and AVSOD (red) gate drive energy ratio to CVSGD gate driver energy for different values of I_m and V_{H1}.

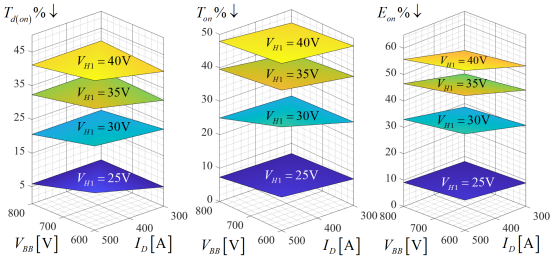


(b) Turn-off ACSOD (blue) and AVSOD (red) gate drive energy ratio to CVSGD gate driver energy for different values of I_m and V_{L1}.

Fig. 27. ACSOD and AVSOD over-drive mode gate drive energy ratio to CVSGD gate driver energy for $R_{g(ext)} = 1.2\Omega$.



(a) Turn-on over-drive ACSOD values for different I_m.

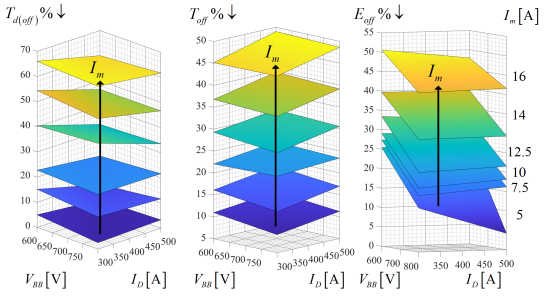


(b) Turn-on over-drive AVSOD values for different V_{H1}.

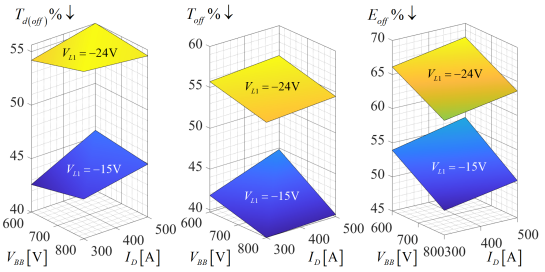
Fig. 28. Comparison of turn-on over-drive performance in terms of $T_{d(on)}$, T_{on} and E_{on} between ACSOD and AVSOD.

plot in Fig. 36, and it is clear how manipulating v_{GS} results in fine-grained control of the conduction power loss, p.

5) Control reference for adaptive gate drivers: Manipulating key operating parameters of the SiC MOSFETs, necessitates the control of the proposed adaptive gate drivers through their independent control variables (e.g., I_m in ACSOD, v_B in

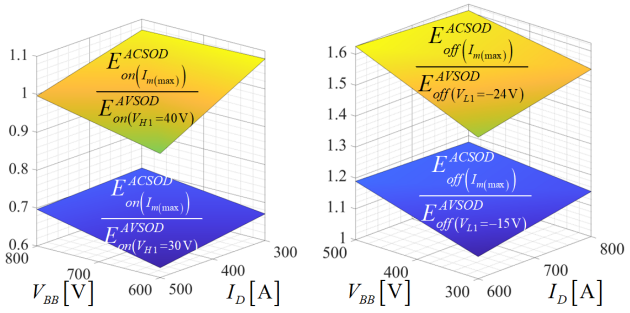


(a) Turn-off over-drive ACSOD values for different I_m.



(b) Turn-off over-drive AVSOD values for different V_{L1}.

Fig. 29. Comparison of turn-off over-drive performance in terms of $T_{d(off)}$, T_{off} and E_{off} between ACSOD and AVSOD.

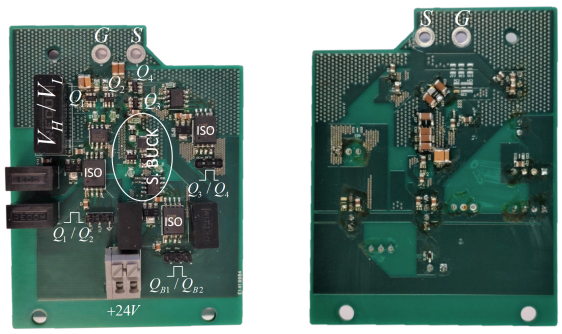


(a) E_{on} comparison between ACSOD and AVSOD for maximum levels of I_m vs. $V_{H1} = 40$V and $V_{H1} = 30$V.

(b) E_{off} comparison between ACSOD and AVSOD for maximum levels of I_m vs. $V_{L1} = -24$V and $V_{L1} = -15$V.

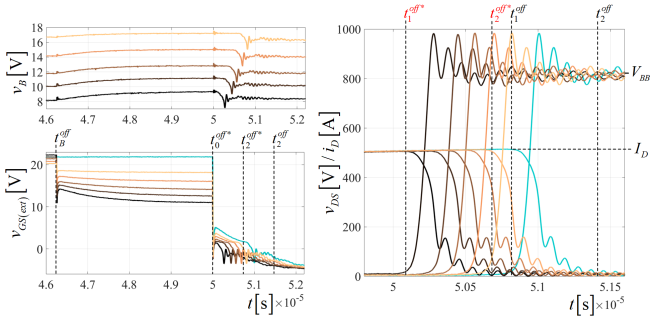
Fig. 30. Ratio > 1 means ACSOD is resulting in a higher $E_{on/off}$ value than AVSOD.

VVSMGD etc.). One way to set the desired control references and identify the switching instants of $Q_1 - Q_4$ in case, for instance, of the ACSOD is to utilize the pre-characterization of the specific adaptive gate driver combined with the SiC MOSFET power module, as shown in Figs. 28, 29 and 33. An alternative way is to utilize a device model that can run in real-time, receives measured signals (e.g., load current and/or voltage) and provide the desired control reference to the gate driver. An example is a discrete-time SiC MOSFET model that is implemented in FPGA processor and is capable of running in real time [64], [65]. The switching instants can also be determined in an open-loop control scheme by employing mathematical models of the DUT. Thus, the switching instants can be derived from the mathematical model of the trajectories of v_{GS}, i_D and v_{DS}. The switching instants can for example

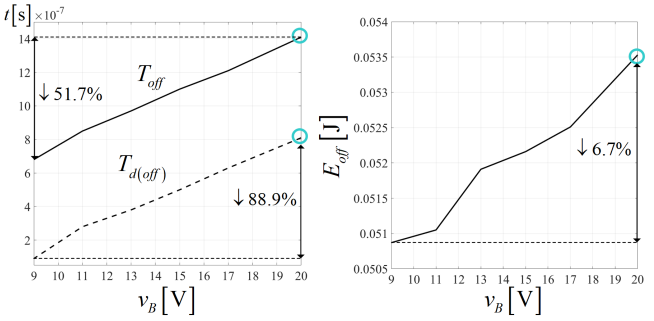


(a) Top-side view. (b) Bottom-side view.

Fig. 31. Photograph of the variable voltage source multi-level gate driver (VVSMGD) printed circuit board (PCB).



(a) v_B, $v_{GS(ext)}$ and i_D/v_{DS} waveforms.



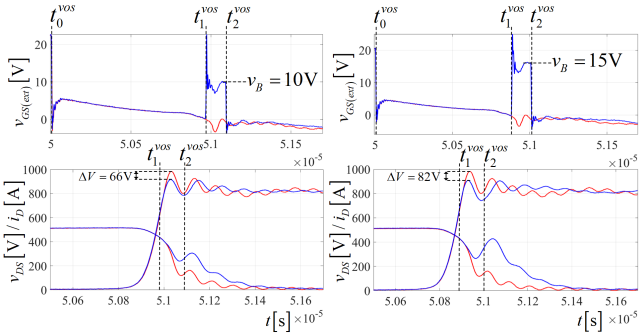
(b) $T_{d(off)}$, T_{off} and E_{off} reduction.

Fig. 32. VVSMGD turn-off delay manipulation.

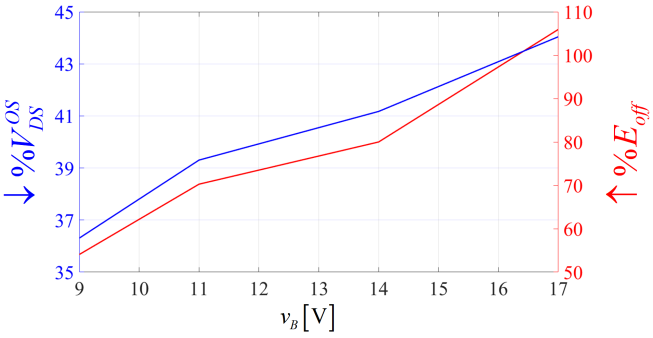
be pre-programmed in the digital controller's look-up tables depending on load and source conditions, and desired operating modes of the adaptive gate drivers.

VI. Discussion

The ACSOD is seen to be able to control the overall $T_{d(on/off)}$, $T_{(on/off)}$ and $E_{on/off}$ by adjusting the pre-charge current amplitude I_m. For $V_{BB} \in [600, 800]$V and $I_D \in [300, 500]$A of the SiC MOSFET power module, the ACSOD achieves a maximum reduction of $50-55\%$ in E_{on}, a $60-65\%$ reduction in T_{on} and a $60-75\%$ reduction in $T_{d(on)}$ for turn-on, while a maximum $40-50\%$ reduction in E_{off}, a $45-50\%$ reduction in T_{off} and a $60-65\%$ reduction in $T_{d(off)}$ is achieved at turn-off given the I_m^{OS} constraint.



(a) $v_B = 10$V (left) and $v_B = 15$V (right) in blue waveforms compared to no overshoot manipulation shown in red waveform color.



(b) V_{DS}^{OS} reduction and E_{off} increase.

Fig. 33. Single-pulse VVSMGD turn-off voltage overshoot V_{DS}^{OS} manipulation.

The presented AVSOD has been shown to be able to independently control $T_{d(on/off)}$, $T_{(on/off)}$ and $E_{on/off}$, as well as device dv/dt and di/dt. For $V_{BB} \in [600, 800]$V and $I_D \in [300, 500]$A, the AVSOD achieves a maximum $50-55\%$ reduction in E_{on}, a 48% reduction in T_{on} and a 40% reduction in $T_{d(on)}$ for turn-on using the over-drive mode with $V_{H1} = 40$V, while a maximum $60-68\%$ reduction in E_{off}, a 55% reduction in T_{off} and a $53-57\%$ reduction in $T_{d(off)}$ is achieved at turn-off using the over-drive mode with $V_{L1} = -24$V. As can be seen in Fig. 30, using the AVSOD in over-drive mode with $V_{H1} = 40$V yields a similar E_{on} values as using the ACSOD with $I_{m(max)} \approx I_m^{OS} \approx 16$A. For turn-off, using the AVSOD in over-drive mode with $V_{L1} = -15$V yields marginally lower E_{off} as using the ACSOD with $I_{m(max)} \approx I_m^{OS} \approx 16$A, while using $V_{L1} = -24$V yields a lower E_{off} than using the ACSOD with $I_{m(max)} \approx I_m^{OS}$ with a factor of $1:1.6$.

The AVSOD shows a higher degree of control capabilities compared to the ACSOD with the same number of discrete driver switches. While the AVSOD is capable of independently increasing or decreasing the DUT switching parameters E_{on}/E_{off}, T_{on}/T_{off}, $T_{d(on)}/T_{d(off)}$, di/dt and dv/dt by controlling the length, timings and magnitude of the applied voltages, the ACSOD may only adjust the amplitude of I_m, hence dependently reducing or increasing the DUT switching parameters compared to the previous switching instant. A caveat to this – an operating point of the ACSOD which

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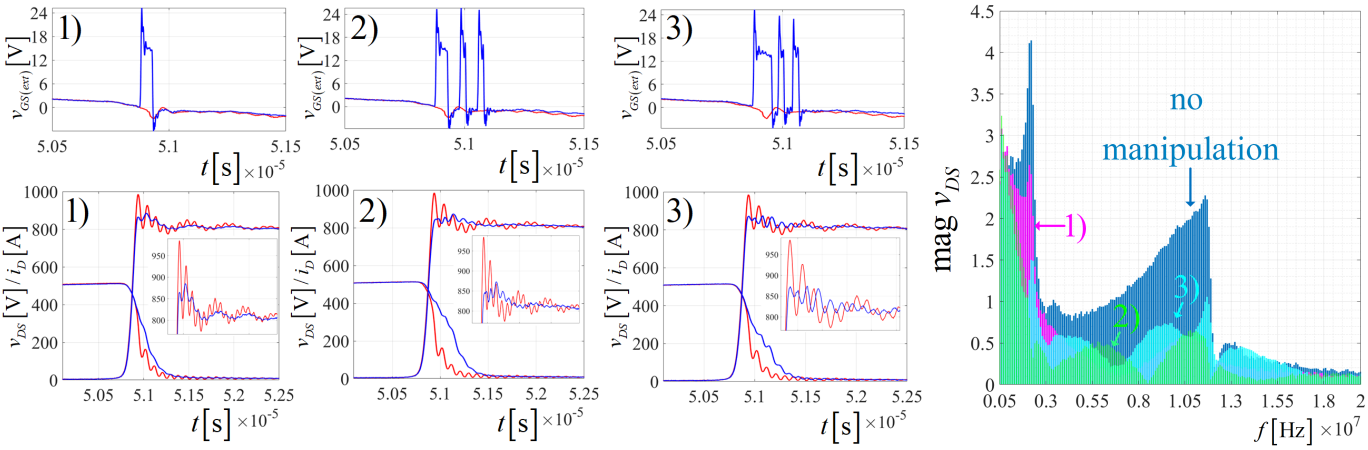
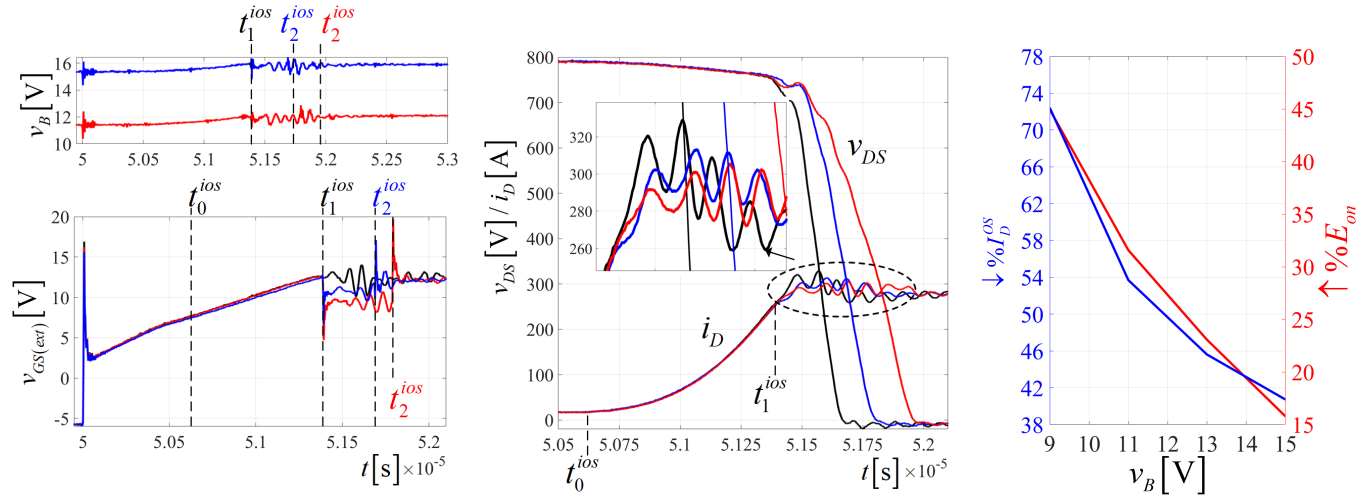


(a) $v_{GS(ext)}$ with $v_B = 15$V upper figures and i_D/v_{DS} lower figures.

(b) Frequency spectrum of the v_{DS} oscillations.

Fig. 34. Multi-pulse VVSMGD turn-off voltage overshoot V_{DS}^{OS} manipulation.



(a) Drain current i_D overshoot manipulation with $v_B = 15$V (blue waveform color), $v_B = 11$V (red waveform color) compared to no manipulation (black waveform color).

(b) I_D^{OS} reduction and E_{on} increase.

Fig. 35. Turn-on current overshoot I_D^{OS} manipulation.

is not shown in this paper, but addressed in [41] – is the ACSOD ability to reduce dv/dt and di/dt by commutating i_g away from the gate at a specified time instant during the switching interval. For instance, during turn-on, the increase of dv/dt is accomplished by turning Q_4 on for a given time period after injecting i_m into the gate, hence commutating i_g into V_L (i.e. V_L is effectively applied to the gate), reducing dv/dt and increasing E_{on}. The same can be accomplished for turn-off by turning Q_3 on for a certain time period after the turn-off is initiated by turning Q_2 on. Turning Q_3 on after v_{DS} rise will effectively reduce di/dt, which will increase E_{off}. Furthermore, while the ACSOD is limited in L_m driving energy by the internal gate resistance $R_{g(int)}$ and the critical damping criterion (which one may move away from, however, proper driver design considering the effective RLC circuit must be done to ensure safe operation and avoid excessive v_{GS} voltages), there is no restriction on the AVSOD over-drive levels V_{H1}/V_{L1}. However, strict safety considerations must be adhered to (e.g. hard-coded maximum on-time of the AVSOD Q_1/Q_2 for a given DUT and V_{H1}/V_{L1}) when using high over-drive voltages to ensure that v_{GS} does not exceed its safe operating limits.

A summary of the capabilities of the discussed gate driver topologies is given in Table XIX. The presented capabilities include gate over-driving (OD), controlling turn-on/off delay time $T_{d(on)}/T_{d(off)}$, controlling turn-on/off partial switching time $T_{p(on)}/T_{p(off)}$, controlling dv/dt and di/dt at turn-on and turn-off and conduction loss (CL) manipulation. The symbol $\times$ indicates that the driver lacks the ability to control the corresponding parameter. The symbol Y^i indicates that the driver can independently control the parameter without significantly affecting the other parameters. The symbol Y^c

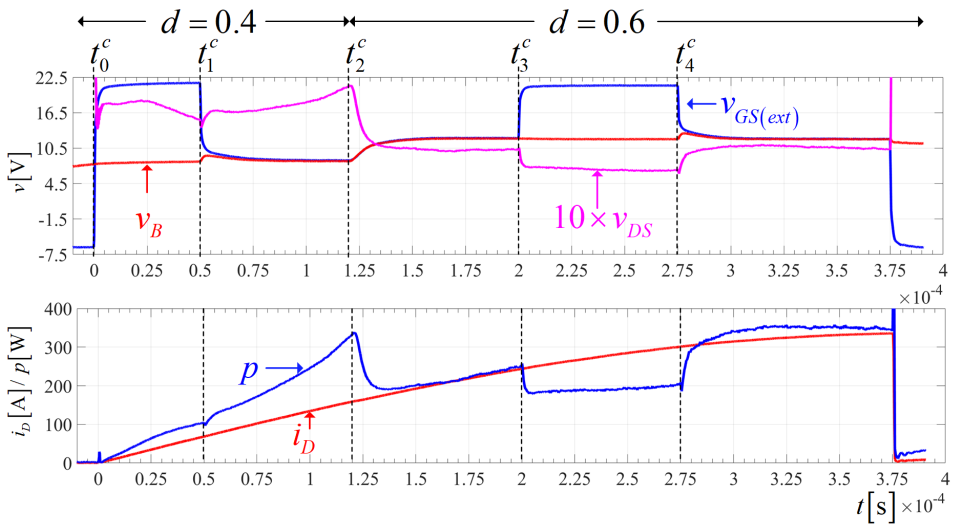


Fig. 36. Single pulse test showing the conduction loss manipulation operation. Upper figure shows v_{GS} (blue waveform), v_B (red waveform) and $10 \cdot v_{DS}$ (magenta waveform) with the buck converter duty-cycle d changes. The lower figure shows the drain current i_D (red waveform) and the instantaneous power loss of the device $p = i_D \cdot v_{DS}$.

TABLE XIX
GATE DRIVER SUMMARY
* VARYING dv/dt DURING THE TURN-OFF CAUSES A VARYING DISCHARGE CURRENT OF THE BLOCKING DIODE, HENCE AFFECTING DUT'S di/dt. THE MOSFET IS IN SATURATION REGION AND v_{GS} GOES BELOW THE MILLER PLATEAU, HENCE ANY CHANGE IN APPLIED GATE DRIVING VOLTAGE AFFECTS i_D.
** VARYING di/dt DURING THE TURN-ON AFFECTS DUT dv/dt DUE TO POWER LOOP STRAY INDUCTANCE.

	CVSGD	CCSGD	ACSOD	AVSOD	VVSMGD
OD	×	Y	Y	Y	×
$T_{d(on)}$	P	Y^c	Y^c	Y^i	Y^i
$T_{d(off)}$	P	Y^c	Y^c	Y^i	Y^i
dv/dt_{on}	P	Y^c	Y^i	Y^i	$Y^i_\downarrow$
dv/dt_{off}	P	Y^c	Y^{c^*}	Y^{c^*}	$Y^{c^*}_\downarrow$
di/dt_{on}	P	Y^c	$Y^{c^{**}}$	$Y^{c^{**}}$	$Y^{c^{**}}_\downarrow$
di/dt_{off}	P	Y^c	Y^i	Y^i	$Y^i_\downarrow$
CL	×	×	×	×	Y

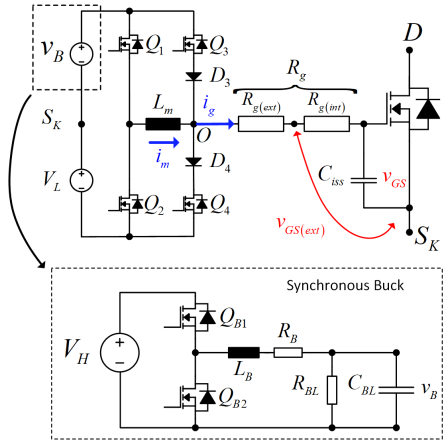
indicates that the driver can control the parameter, but it will affect some of the other parameters. The symbol $Y_\downarrow$ means the driver has the ability only to reduce the parameter, as is the case with the VVSMGD. As this driver incorporates a buck converter from the on-state voltage V_H, the driver may only reduce dv/dt and di/dt parameters during the partial switching transient. The symbol P indicates that the driver can passively control the parameter, e.g. through hardware interference changing the gate resistance R_g.

Both the ACSOD and AVSOD can be further modified to include the proven adaptive capabilities of the VVSMGD. By including the synchronous buck into the ACSOD and AVSOD high-side voltage source, the conduction loss and T_{on}/$T_{d(on)}$ manipulation capabilities of the VVSMGD can be included in the over-drivers, yielding an even higher degree of adaptability. Inclusion of these capabilities in the ACSOD and AVSOD drivers is shown in Fig. 37.

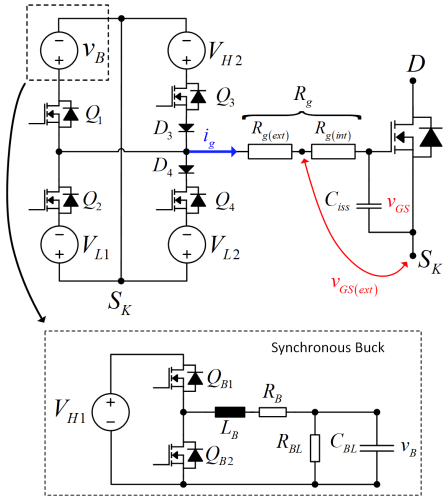
Using the turn-off delay manipulation as described in Section IV-A includes reduction of v_{GS} prior to actual turn-off. Evidently, this leads to an increase in device $r_{DS(on)}$, as seen from Fig. 3b. Thus, the instantaneous conduction loss p_{cond} will slightly increase during $T_{d(off)}$ adjustment (Fig. 16a). However, as seen from Fig. 3b, significant increase in $r_{DS(on)}$ occurs for decreasing v_{GS} below 10V, hence keeping V_{GS}^{pre} below such level keeps the increase in p_{cond} low during this time interval. Furthermore, $T_{d(off)}$ adjustment should be significantly lower than the PWM on-time, hence the increase in instantaneous p_{cond} is low on the average conduction loss.

On the other hand, the VVSMGD can also be utilized for adjusting the conduction power losses of the SiC MOSFET during load current conduction. This is, in particular, advantageous in active thermal control applied to soft-switching power converters, where junction temperature control is only possible through manipulation of conduction power losses. Still, using the proposed VVSMGD design, it is only possible to adjust the positive gate voltage to values lower than $V_H = 20V$, which is defined by the device manufacturer. Thus, it is only feasible to generate conduction losses higher than the minimum value obtained for $V_H = 20V$.

Table XX presents a qualitative and quantitative comparison of the AVSOD and VVSMGD with adaptive voltage-source gate driver concepts that have been shown in literature. For the quantitative comparison, % variations have been used, in order to harmonize the testing conditions. It is observed that the AVSOD exhibits the highest reduction of E_{on}, T_{on}, E_{off} and T_{off} among the existing concepts, while it also enables



(a) Modified ACSOD.



(b) Modified AVSOD.

Fig. 37. ACSOD and AVSOD with the capabilities of VVSMGD.

increase of dv/dt and di/dt, as denoted with the symbol ↑ in Table XX. Similarly, the VVSMGD shows a comparable reduction of I_D^{OS} as in [50] at a cost of a lower increase of E_{on}. In addition, using the VVSMGD, the V_{DS}^{OS} can be reduced by 45%, while exhibiting the lowest increase of E_{off} among all other concepts. Finally, the VVSMGD is also able to control the conduction power losses as the gate driver presented in [57] does.

The proposed adaptive gate drivers are beneficial for various power electronics applications operating under varying load conditions. Such varying conditions might be load current variations, such as electric motor torque variations, or voltage variations, such as lithium-ion batteries voltage variations with state-of-charge (SOC). An active slew rate control can be integrated with EV battery management systems (BMS), as Texas Instruments discuss in [66] using their variable gate resistance UCC5880-Q1 gate driver to optimize gate driving for various SOC conditions, as shown in a typical battery voltage versus SOC plot in Fig. 38. In the latter case, a CVSGD is optimally tuned at a fixed operating point, where the anticipated overvoltage in v_{DS} is the highest. However, at lower SOC values, the safety margin to reach the maximum overvoltage is larger, thus there is room for further minimizing switching losses. Using an adaptive gate driver, it becomes possible to control di/dt of the SiC MOSFET in real time, and therefore, always minimizing the switching losses by respecting the maximum overvoltage limits at device turn-off. This has been experimentally validated using the proposed VVSMGD as shown in Fig. 33. and Fig. 34a, the AVSOD as shown in Fig. 26 and the ACSOD in Fig. 21.

Other examples potentially benefiting from active slew rate control are inverter-based applications, where the load varies in a sinusoidal manner. Considering a three-phase inverter supplying a three-phase load, e.g. grid interfacing converters, the switch currents in the respective bridge leg are highest at the sinusoidal peak. Hence, the v_{DS} overshoot amplitude will vary in a sinusoidal manner following the load current. For such an application, where the load frequency is known, the adaptive capability can be programmed to follow the grid frequency. Furthermore, the grid load is typically predictable with load peaks in mornings and late afternoons, hence the adaptive gate driver control can be adapted for the load variations.

Typically, the adaptive gate drivers can optimize the operation of power electronic systems in closed-loop control. Closed loop control of switching loss for increasing efficiency, dv/dt or di/dt for controlling EMI is possible by employing measurements of the driven device's dv/dt or di/dt. The closed loop control allows for real-time control of these parameters and can adapt the SiC MOSFETs power module's parameters to a specific application based on a control input, for example the pre-charge time of the gate current, T_{pre}^*, in the case of the ACOSD driver. An example of a closed-loop dv/dt control scheme is illustrated in Fig. 39, with a typical dv/dt measurement circuit shown in Fig. 40a. The error between the reference and measured dv/dt is provided to the PI-controller which provides the command T_{pre}^* for ACSOD peak charge current I_m^*. The resulting change in I_m manipulates the device dv/dt, with resulting changes in device switching loss p_{sw}.

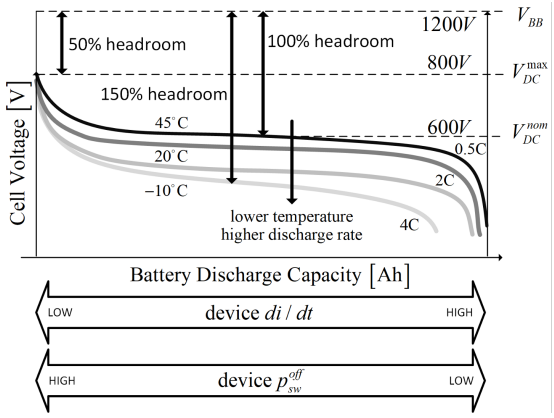


Fig. 38. Battery cell voltage versus discharge curves for different temperatures and discharge rates (C-rates).

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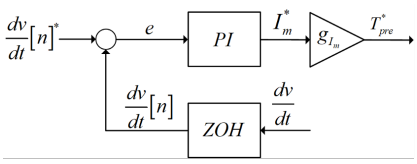
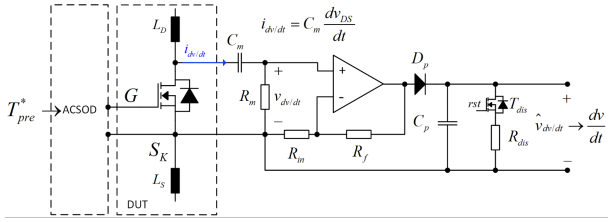
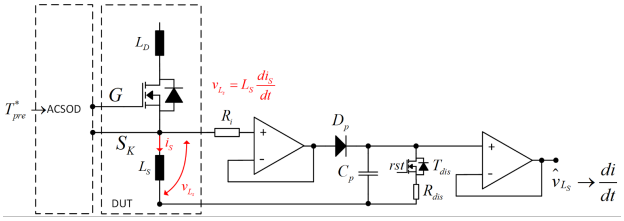


Fig. 39. Block diagram illustration of closed-loop dv/dt control.



(a) Circuit schematic of dv/dt measurement circuit employed with closed-loop dv/dt control.



(b) Circuit schematic of di/dt measurement circuit employed with closed-loop di/dt control.

Fig. 40. dv/dt and di/dt measurement circuits.

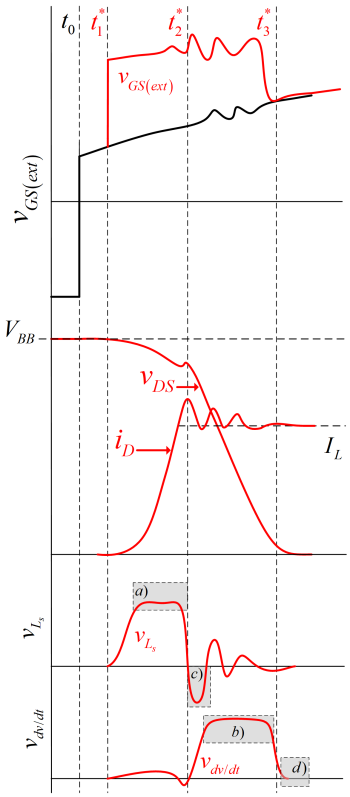


Fig. 41. AVSOD in over-drive mode with corresponding di/dt and dv/dt measurement voltages.

The voltage measured across the device source stray inductance L_s, $v_{L_s} = L_s \cdot di_s/dt$, will vary according to the instantaneous value of the device di/dt, as illustrated in Fig. 41. This is also the case for measurement of the device v_{DS} dv/dt, where the measured current $i_{dv/dt}$ varies with the device dv/dt and its capacitances. For example, when v_{L_s} crosses a certain value, that will correspond to a certain device di/dt, and the di/dt control can then be initiated in zone a) Fig. 41, adjusting di/dt according to the value of v_{L_s}. The di/dt control can be stopped when v_{L_s} is measured negative (zone c) Fig. 41), corresponding to i_D reaching fully turned on device current. Similar closed-loop control can be performed for the dv/dt using the measurement circuit in Fig. 40a. The AVSOD dv/dt control can be initiated in zone b) as shown in Fig. 41 and ended when the measured dv/dt reaches zero again, i.e. in zone d) in Fig. 41. Hence, for the control of the AVSOD, one can then use the v_{L_s} and $v_{dv/dt}$ amplitudes to determine the switching instants of $Q_1 - Q_4$.

Continuous operation of the proposed adaptive gate drivers imposes the need for effective heat dissipation from the driver circuit board. This phenomenon is pronounced at higher switching frequencies. Although this aspect is crucial to allow continuous operation of the drivers, this paper only focused on presenting the topologies, operating principles and capabilities of the proposed gate drivers.

Increasing the power ratings of converters, is usually done by parallel-connecting power modules, as shown in [67] for an active neutral point clamp (ANPC) converter employing 3.3 kV SiC power modules. This practice requires gate drivers capable of delivering higher gate currents, while at the same time compensating for possible electrical and thermal behavior mismatches. The proposed AVSOD and ACSOD are able to not only supply a higher gate current to the parallel modules for enabling fast switching transients, but also to compensate in real time for possible mismatches in temperature distribution causing uneven loss performance, and mismatches in v_{DS} overvoltages due to the unsymmetrical inductive layout.

VII. Conclusion

This paper presented two novel adaptive voltage source gate drivers, namely the adaptive voltage source over-driver (AVSOD) and the variable voltage source multi-level gate driver (VVSMGD). The paper introduced the concept of gate over-driving and compares the over-driving capabilities of the AVSOD with an adaptive current source over-driver (ACSOD) based on a full-bridge driver topology. The working principles of the presented drivers are accurately described, and their operating modes verified experimentally on the FMF750DC-66A SiC MOSFET half-bridge power module using a double pulse test setup.

The presented AVSOD is seen to be able to independently control the DUT's switching losses, turn-on/off time and turn-on/off delay times, as well as di/dt and dv/dt. The over-driving capability of the AVSOD is able to reduce E_{on} up to

TABLE XX
COMPARISON OF THE AVSOD AND VVSMGD WITH EXISTING GATE DRIVER CONCEPTS IN LITERATURE

Ref.	E_{on}	T_{on}	I_D^{OS}	E_{off}	T_{off}	V_{DS}^{OS}	$\lvert dv/dt \rvert$	$\lvert di/dt \rvert$	p_{cond} ctrl
[57]	-20%	-25%	11%	-	-	-11.5% (+350% E_{off})	$\downarrow$ / $\uparrow_{on}$	$\downarrow$ / $\uparrow_{on}$	yes
[53]	-41%	-21%	-	-31.1%	-33%	-	$\downarrow$	$\downarrow$	no
[50]	-	-	-85% (+80% E_{on})	-	-	-6.6% (+300% E_{off})	$\downarrow$	$\downarrow$	no
[51]	-	-18%	-	-	-29%	-	$\uparrow$	$\uparrow$	no
[68]	-	-	-21.5% (+44% E_{on})	-	-	-16.7% (+10% E_{off})	$\downarrow$	$\downarrow$	no
[69]	-	-	-30%(+300% E_{on})	-	-	-3.1% (+300% E_{off})	$\downarrow$	$\downarrow$	no
AVSOD	-55%	-48%	-	-68%	-55%	-	$\uparrow$	$\uparrow$	no
VVSMGD	-	-	-70%(+45% E_{on})	-6.5%	-51.7%	-45% (+110% E_{off})	$\downarrow$	$\downarrow$	yes

55% and E_{off} by 68% in over-drive mode with the utilised driver voltage levels, while the over-driving capability of the ACSOD is able to reduce E_{on} up to 58% and E_{off} by 50% in over-drive mode with the given $I_{m(max)}$ values.

The presented VVSMGD has shown to control turn-off delay times and consequently turn-off times, turn-off v_{DS} overshoots and turn-on i_D overshoots of the switched DUT. From experiments, it has been shown that by using the VVSMGD, the voltage overshoot on v_{DS} can be reduced by 44%. Furthermore, by manipulating the duty-cycle of the integrated buck converter, the driver can accurately adjust the DUT conduction loss through the dynamic adjustment of $r_{DS(on)}$.

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