Graduate thesis

NTNU
Norwegian University of Science and Technology
Faculty of Information Technology and Electrical Engineering
Department of Electronic Systems

Muhammad Naseer ud Din

Ultra low voltage arithmetics- Schmitt trigger based vs Static CMOS

Graduate thesis in Electronic Systems Design (MSELSYS)
Supervisor: Snorre Aunet
Co-supervisor: Trond Ytterdal
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TFE4930 - Master thesis

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.

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Abstract

The demand for low-power and energy-efficient digital systems has increased in recent years for various applications. Ultra-low-voltage circuits have become popular in low-power applications but face performance degradation. This report analyzes the operation of static CMOS and Schmitt trigger (ST) CMOS-based full adders, full adders connected as ring oscillators, and ripple carry adders in the subthreshold region. Full adder implementation using Schmitt trigger CMOS XOR can save 50% average power as compared to full adder implementation using static CMOS XOR, while full adder implementation using Schmitt trigger CMOS NAND gate can save 31% average power as compared to full adder implementation using static CMOS NAND gate at TT corner, 0.18V and 27°C. Additionally, the report provides a complete DC voltage transfer analysis with analytical expressions for the NM_H and NM_L. A comparison between the ST CMOS and static CMOS adders reveals the relative benefits, such as a high and stable noise margin, with the temperature rise, while presenting drawbacks, such as larger size requirements of each in ULV applications. Propagation delay is higher for Schmitt trigger CMOS full adders than static CMOS full adders for all process corners at 0.18V and 27°C. Furthermore, the study includes a thorough investigation of measured propagation delay, average power, power delay product, and energy-delay product of the circuit when full adders are connected in the ring configurations and also in the ripple carry adders configuration. In-ring oscillators at TT corner, 0.18V and 27°C, ST CMOS NAND save 16% average power than static CMOS NAND, ST CMOS XOR save 66% average power than static CMOS XOR configuration. In the RCAs at TT corner, 0.18V and 27°C, ST CMOS NAND saves 43% average power than static CMOS NAND, ST CMOS XOR saves 53% average power than static CMOS XOR configuration.

Keywords: Schmitt trigger, Static, Subthreshold, CMOS, NM_H, NM_L, delay, Power, PDP, EDP, Ring, RCA.

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1 Introduction

In recent years, the research community and marketplace have shown increasing interest in ultra-low power VLSI (Very Large Scale Integration) circuits[1]. There has been a rising demand for low-power and energy-efficient digital systems, particularly in portable and battery-powered gadgets. These applications include wireless sensor networks, biomedical apparatuses, ambient intelligence, wearable computing, smart grids, air quality tracking, plant observation, smart warehouses, and more[1].

At the same time, there have been significant advancements in overall electronics, leading to a notable improvement in the functionalities of various kinds of equipment. This progress has resulted in the development of more sophisticated and advanced systems for communication, data processing, entertainment, ubiquitous computing, sensor networks, and healthcare facilities[2]. Generally, the main emphasis is on autonomous applications that rely on either small batteries or utilize ambient energy harvesting techniques. While some devices may operate without the need for batteries and stay connected to an electrical outlet, any technique that reduces their energy consumption would be advantageous[2]. Ultralow voltage methods play a crucial role in battery-operated applications such as embeddable devices, hearing assistance gadgets, and environmental sensors. These techniques are essential for extending battery life and reducing the need for challenging interventions or excursions, especially in remote forest locations[2]. The disposal of a substantial number of batteries is a concern as the environment is unable to deal with the volume of waste they generate[2].

Ambient energy-harvesting sources can be an important source of power, several produce a low voltage level, typically less than 100 mV. For example, thermo-electric generators (TEGs) that utilize bismuth telluride (Bi2Te3) [3] and operate based on the temperature difference between the human body and the environment, typically generate a voltage output between 50 and 75 mV[2], due to the small temperature difference of 1-3 K. In dark office environments, photovoltaic cells have the potential to produce a voltage output of several hundred millivolts [4]. Ultralow voltage operation is marked by the condition where the supply voltage of digital circuits is significantly decreased to a level of tens of millivolts, which results in notable deviations of the output voltages corresponding to logic levels '0' and '1' from the supply rails[2].

Due to voltage limitations in low-power applications, ultra-low-voltage circuits have become a popular choice[5]. Scaling down the supply voltage is the deterioration of performance that comes with it, as stated in [6]. This performance degradation typically follows a linear trend with the voltage above the absolute value of threshold Vt (the point at which the device is nominally turned on) and exponentially as the device operates in subthreshold (when the device is nominally off) [6]. The exponential relationship between current and voltage in the subthreshold regime makes the performance of devices sensitive to process, voltage, and temperature (PVT)variations, which can lead to considerable performance degradation. This variation is a crucial factor that has contributed to the voltage scaling[6].

Operating digital logic in the subthreshold regime requires different design optimizations compared to those used in strong inversion. The first proposal for Pseudo-NMOS logic to operate in the subthreshold regime was presented in [7]. The main drawback of pseudo-NMOS logic is that it requires an always-on PMOS transistor, which acts as an active load. The logic function is determined by a series/parallel array of NMOS transistors. While this logic family has lower delays and power-delay product (PDP) than static CMOS in subthreshold operation, it is less efficient in terms of total energy per cycle [2].

Sub-Domino logic is a dynamic and dual-phase logic for ultralow voltage applications that uses a clock signal to control precharge and evaluate phases [8]. Depending on the input signal pattern, the output node can be charged or discharged during the precharge phase, resulting in a high-activity output signal and higher energy dissipation compared to static logic. However, Sub-Domino logic has drawbacks such as requiring an inverter for cascading, being highly sensitive to noise[8], and the potential for leakage currents to cause logic errors during the evaluation phase [2].

In the sub-threshold region, Static CMOS is the most common logic used due to its robustness [9]. In the subthreshold region of operation, the power consumption is reduced due to reduced Vdd of

the circuit[10]. It operates without the need for a clock or differential signals, has reliable static noise margins, does not have any dynamic nodes, and can be conveniently cascaded. So, static logic is considered the most suitable general-purpose choice in subthreshold technology compared to other techniques like sub-Domino logic and Pseudo-NMOS logic[2].

However, with reduced supply voltage, MOS transistors often have to operate in the subthreshold regime, where Vdd is below the threshold voltage. In such scenarios, the standard CMOS Schmitt trigger circuit [11] is highly valued for its adaptability and ability to serve both analog and digital purposes[5]. The static noise margin of the Schmitt Trigger is greater than that of a conventional inverter under similar conditions.[2].

In VLSI applications, arithmetic operations hold significant importance, and they include addition, subtraction, multiplication, and accumulation. The 1-bit full adder (FA) cell serves as the fundamental building block for most implementations of these operations [12].

The main goal of this thesis is to compare and contrast the ST CMOS-based and static CMOS adders for ULV applications. The comparison will be carried out through simulation studies using AIM SPICE tools. The results of this study will provide insights into the relative benefits and drawbacks of the two ULV logic families(Schmitt trigger CMOS and static CMOS), The outcome will assist in the design of energy-efficient electronic systems.

Notably, this study reveals several key trends that clearly show the different behaviors and efficiencies of these technologies. In static CMOS full adders, an increase in temperature leads to a decrease in NM_H and an increase in NM_L. However, in Schmitt trigger CMOS full adders, both NM_H and NM_L remain relatively constant with the temperature rise. Propagation delay is higher in Schmitt Trigger CMOS full adders as compared to Static CMOS full adders. The average power of Schmitt trigger CMOS full adders is less than static CMOS full adders for all process corners at 0.18V and 27°C.

Chapter 2 (Methods), provides an overview of the different circuit designs and topologies, specifically focusing on Schmitt trigger and Static CMOS circuits. The chapter proceeds to the theory of noise margins, and propagation delay, followed by the description of test benches for various circuits. It also explores simulation and analysis, including the utilization of various software and scripts to generate the desired outputs. Chapter 3 (Results), includes the results of the static CMOS full adder and Schmitt trigger CMOS full adder, ring oscillator, and RCA. Chapter 4 is dedicated to the discussion and analysis of these results. The chapter ends with final thoughts, conclusions, and future work based on the study.

2 Methods

The methods section provides a comprehensive overview of the implementation of static CMOS and Schmitt trigger CMOS full adder, aiming to gain a thorough understanding of their behavior and performance. The full adder design is designed in two ways. First is a direct XOR gate setup. Second, it is designed using XOR functionality based on a NAND gate. Both types are further explored in Static CMOS and Schmitt trigger CMOS ways. This results in four distinct types of full adders: 1) Full adder Implementation using Static CMOS NAND gates, 2) Full adder Implementation using Schmitt Trigger CMOS NAND gates, 3) Full adder Implementation using Static CMOS XOR gate, 4) Full adder Implementation using Schmitt Trigger CMOS XOR gates.

Each type of full adder contributes to creating a specific ring oscillator, providing insights into how they work together in this oscillating system. The study combines the four types of Full Adders into the 4bit Ripple Carry Adder design. The goal is to see how well they fit and affect the overall performance.

2.1 Circuit Topologies:

A full adder adds three binary digits A, B, and a carry input (Cin). It produces a sum output and a carry output. This circuit is designed using NAND and XOR gates. Sum is designed using two XOR gates.
Expression for sum:

$$\text{SUM} = A \oplus B \oplus \text{Cin}$$

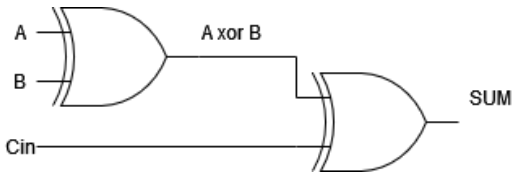


Figure 1: SUM

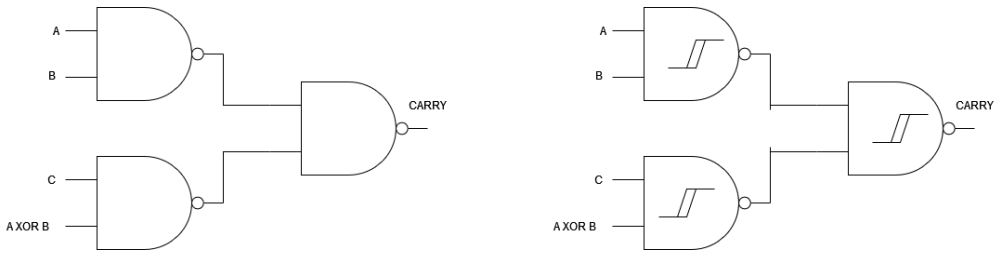
Carry is designed using three NAND gates. In Static CMOS design, carry is achieved using static CMOS NAND gates, while in Schmitt trigger CMOS configuration, carry is established using the Schmitt trigger NAND gates.

Expression for Carry:

$$CARRY = AB + C(AxorB)$$

$$CARRY = \overline{\overline{AB + C(AxorB)}}$$

$$CARRY = \overline{\overline{AB}.\overline{C(AxorB)}}$$



(a) (b)

Figure 2: (a) carry; (b) Schmitt trigger carry

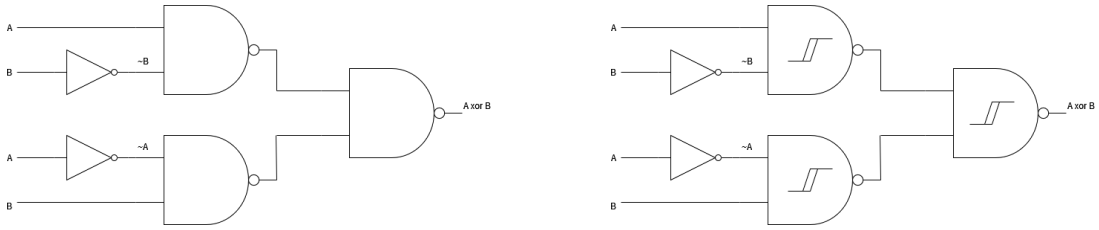
2.1.1 Topology1: Full Adder Implementation using Static CMOS vs Schmitt Trigger CMOS NAND gates:

The full adders are designed using XOR gates. For the full adder Implementation using Static CMOS NAND gates: XOR gate is designed by using static CMOS NAND gates and Static CMOS Inverters. For the full adder Implementation using Schmitt Trigger CMOS NAND gates: XOR gate is designed by using Schmitt Trigger CMOS NAND gates and stacked Static CMOS Inverters.

The main motivation to use static CMOS NAND and Schmitt trigger CMOS NAND is that the robustness was checked in the report [1].

Simplified expression for XOR gate.

$$\text{XOR} = \text{A}\overline{B} + \overline{A}\ \text{B}$$
$$\text{XOR} = \overline{\overline{A\overline{B}} + \overline{\overline{A}B}}$$
$$\text{XOR} = \overline{A\overline{B}}.\overline{\overline{A}B}$$



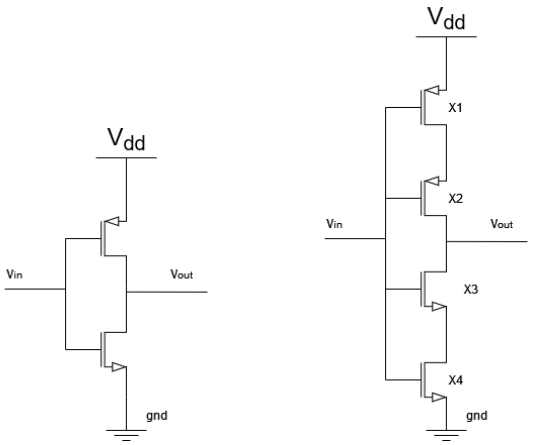
(a) (b)

Figure 3: (a) XOR using static CMOS NAND gates and Inverters; (b) XOR gate using Schmitt trigger CMOS NAND gates and Inverters

The static CMOS inverter consists of a pull-up network, represented by (a PMOS transistor) and a pull-down network (an NMOS transistor). The gates of both the PMOS and NMOS transistors are interconnected which are driven by the input voltage. Similarly, their drains are also interconnected, serving as the output voltage point. The source of the PMOS transistor is connected to VDD while the source of the NMOS transistor is connected to the ground. Figure 4a shows the resulting circuit [1].

The stacked CMOS inverter consists of two PMOS transistors and two NMOS transistors. Two PMOS transistors, X1, and X2, form a series connection between the VDD and the output node, while two NMOS transistors, X3, and X4, are similarly connected in series between the output node and ground. The gates of these four transistors are linked to the input voltage. The stacking of four transistors (X1-X2-X3-X4) plays a crucial role in ensuring the proper functioning of the circuit, the technique of transistor stacking has been employed in references to significantly mitigate leakage currents. Furthermore, the reference asserts that transistor stacking can lead to a tenfold reduction in leakage current [1].

[1] TFE4590-Specialization project[2023], [Muhammad Naseer ud din], [Ultra low voltage logic- Schmitt trigger based vs Static CMOS].



(a) (b)

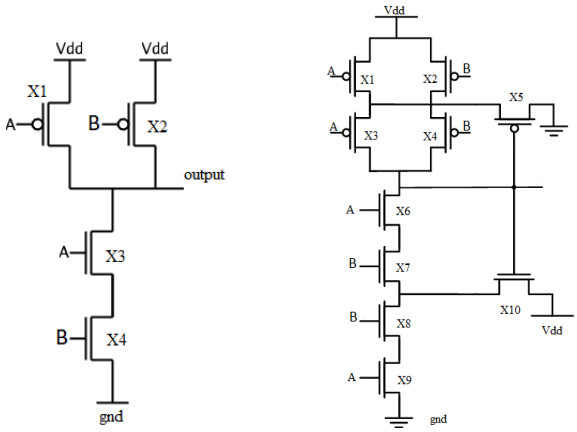
Figure 4: (a) CMOS Inverter; (b) Stacked CMOS Inverter

Source: [13].

The static CMOS NAND2 gate is configured using two PMOS transistors and two NMOS transistors. The sources and drains of both PMOS transistors(X1, X2) are connected to the VDD and output node respectively. On the other hand, the NMOS transistors(X3, X4) are connected in series such that the drain of the first NMOS transistor is connected to the output terminal while its source is connected to the drain of the second NMOS transistor. The source of the second NMOS transistor(X4) is connected to the ground. The gates of the first PMOS(X1) and the first NMOS transistors(X3) are connected to form one input, while the gates of the second PMOS(X2) and the second NMOS(X4) transistors are connected to the other input. The circuit can be seen in Figure 5a [1].

The Schmitt trigger CMOS NAND2 gate consists of 10 transistors: 5 PMOS and 5 NMOS. In the pull-up network, two pairs of PMOS transistors (X1 and X3, X2 and X4) are connected in series between VDD and the output terminal. These two branches are then connected in parallel. The midpoint of each pair is connected to the source of a corresponding feedback PMOS transistor (X5), whose drain connects to the ground, and gate to the output node. The pull-down network utilizes 4 NMOS transistors connected in series from the output terminal to the ground terminal. The mid-point of this network is connected to the source of a feedback NMOS transistor (X10), with its source connected to the VDD, and the gate to the output terminal. The resulting circuit is shown in Figure 5b. [1]

[1]TFE4590-Specialization project[2023], [Muhammad Naseer ud din], [Ultra low voltage logic- Schmitt trigger based vs Static CMOS].



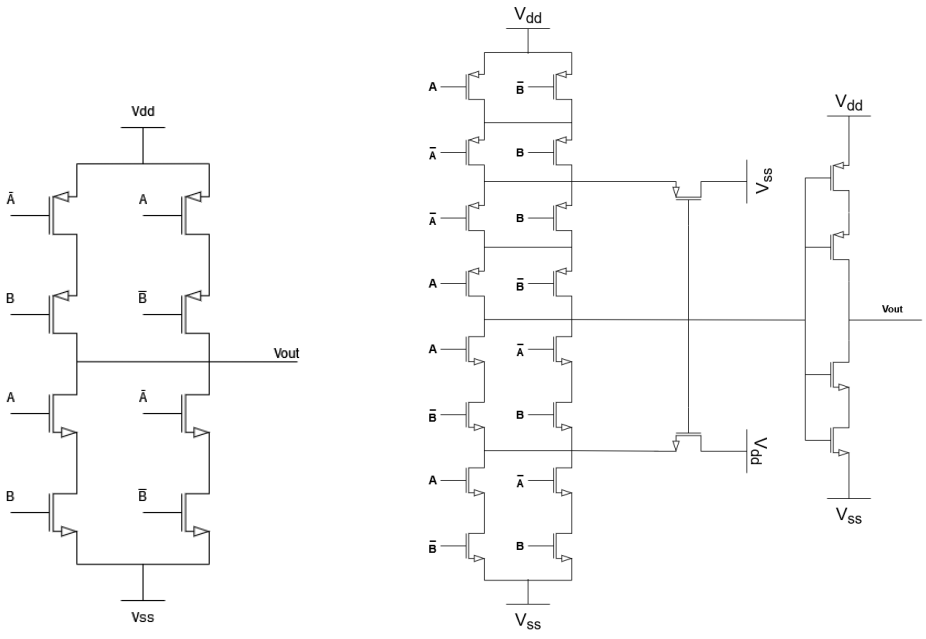
(a) (b)

Figure 5: (a) Static CMOS NAND gate; (b) Schmitt trigger CMOS NAND gate.

Source: With modification[13].

2.1.2 Topology2: Full Adder Implementation using Static CMOS vs Schmitt Trigger CMOS XOR gates:

The full adder is designed using XOR gates in both static CMOS and Schmitt trigger CMOS XOR gates configurations. The Static CMOS-based FA is designed by using the static CMOS XOR gate 6a and static CMOS inverter 4a. While ST FA is configured with the ST XOR gate as in the figure 6b and stacked Inverter as in the figure4b. The Sum of FA is designed as in the expression and the figure1. For static CMOS Xor full adder, the carry the same expression and figure is used as in the 2a. For Schmitt trigger CMOS Xor full adder, the carry the same expression and figure is used as in the 2b.



(a) (b)

Figure 6: (a) Static CMOS XOR gate; (b) Schmitt trigger CMOS XOR gate.

Source: With modification[14].

2.1.3 Connectivity of Full Adders as Ring oscillator:

For the ring oscillator, three full adders of the same type are connected in a ring as in the figure 7. Input A is connected to a low voltage (ground), input B to a high voltage (Vdd), and input C to the sum output of the preceding full adder in the ring. Full adder could be any type for example Static CMOS or Schmitt trigger CMOS.

The choice of full adder is versatile, allowing for either Static CMOS or Schmitt trigger CMOS. One ring oscillator uses three FA with Static CMOS NAND gates, while another goes for three FA with Schmitt trigger CMOS NAND gates. In an alternative setup, a ring oscillator employs three FA with Static CMOS XOR gates, while another scenario employs three FA with Schmitt trigger CMOS XOR gates.

An initial condition is required for simulation. Initial conditions may vary depending on the specific circuit type and Vdd.
.ic v(Sum3)= 0.18

Table 1: Ring Oscillator Using Full Adders

Inputs			Outputs	
A	B	C	SUM	$CARRY$
0	1	0	1	0
0	1	1	0	1

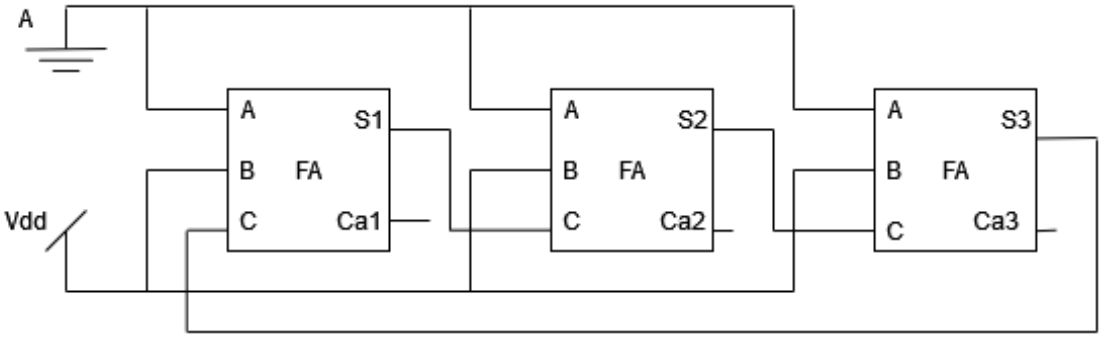


Figure 7: FA ring.

2.1.4 Ripple carry adder:

4-bit ripple carry adder is designed by using four full adders of the same type. The carry-out from each full adder becomes the carry-in for the next one. The type of full adder depends on circuit type for example Static CMOS or Schmitt trigger CMOS. One 4-bit RCA uses four FA with Static CMOS NAND gates, while another goes for four FA with Schmitt trigger CMOS NAND gates. In an alternative setup, a 4-bit RCA employs four FA with Static CMOS XOR gates, while another scenario employs four FA with Schmitt trigger CMOS XOR gates.

Propagation delay = max[Ts, Tc]
Ts=ts+3tc
Tc=4tc

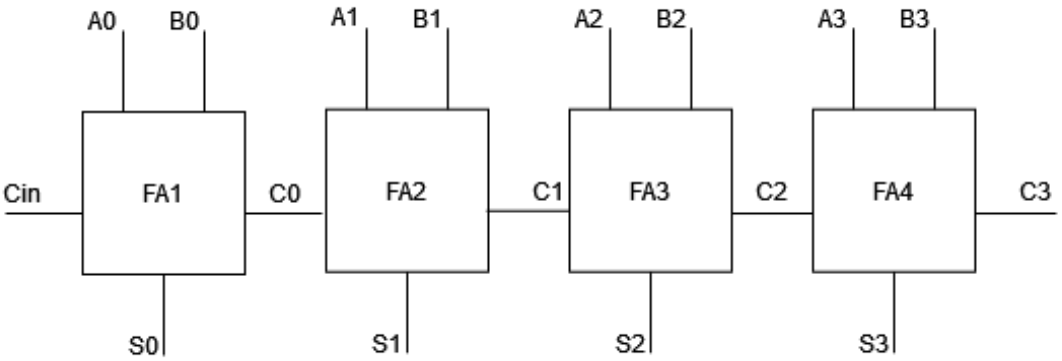


Figure 8: RCA.

2.2 Performance Metrics Exploration:

2.2.1 Noise Margin analysis:

Noise margin is the measure of a CMOS circuit's ability to handle input signal noise without affecting its overall operation. In CMOS circuits, there are two types of noise margins:
High noise margin: The difference between the minimum input voltage considered as a logic high (VIH) and the input voltage level that causes the output to switch from high to low (VOH to VOL)[15]. It can be mathematically represented as Noise margin high (NM_H) = V_{IH}–V_{OH}
V_{IH} represents the input high voltage which corresponds to an output low voltage with a slope of -1.
V_{OH} represents the output voltage when the output level is logic 1.

Low noise margin: The difference between the maximum input voltage that is considered as a logic low (Vil) and the input voltage level that would cause the output to switch from low to high (VOL to VOH). Noise margin low(NM_L) = V_{IL}–V_{OL}
V_{IL} represents the input low voltage which corresponds to an output high voltage with a slope of -1.
$V_{OL}$the output voltage (Vout) at the second 1 slope point (when Vin increases).

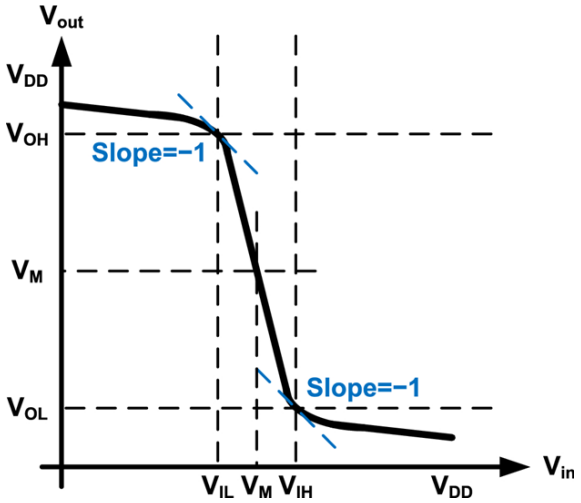


Figure 9: VTC curve

Source: [15].

2.2.2 Propagation delay:

It is the duration it takes for a signal to travel through a circuit from input to output. The propagation delay from low to high and high to low are measured When input and output voltages reach 50% Voltage level during the rising and falling edges.

$$t_{PHL} = t_{PLH} = t_{out} - t_{input}$$

$$t_{pd} = (t_{PHL} + t_{PLH})/2$$

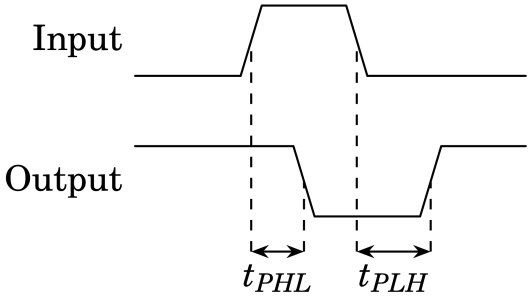


Figure 10: Propagation delay diagram

Source: [15].

2.2.3 Dynamic Characteristics Analysis:

Average current is measured by transient analysis of I(Vdd). Average power is the product of Vdd and measured average I(Vdd). The power delay product is the product of calculated average power and measured delay. and energy-delay Product is the product of calculated power delay product and measured delay.

2.3 Test Bench:

For all circuits, the test bench code is designed using the 90nm GPDK Technology. The code starts by including the 90nm GPDK standard cell library which provides the necessary transistor models for simulation.
The circuit is designed through the integration of various subcircuits, for example, the full adder uses the subcircuit of the NAND gates, Inverters, and XOR gates. While designing the subcircuits, the bulk of the PMOS and NMOS transistors are connected to Vdd and ground respectively.
Defining the power supply voltage (Vdd). And, the input voltage signals (Vin) are configured to oscillate between 0V and 180 mV, with no delay(0ns) and both the rise and fall times are 0.1 nanoseconds. The signal is generated by a pulse with a width of 10 microseconds, and the pulse repeats every 20 microseconds.
Instantiate the circuit: start with the name, inputs, outputs, Vdd, Vss, and name of subcircuit which is needed to instantiate.
Add the plot command with the signal name which needs to analyze then simulate, for simulation put enough time to see the clear signal, for example, the final time for full adders and RCA is 60us and step size is 0.001.

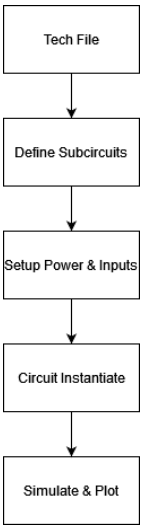


Figure 11: Test Bench flow chart

The spice code of full adder implementation using Static CMOS NAND gates is in the appendix [B.1]. The full adder is designed by using subcircuit XOR gates and the sub-circuit of this XOR gate is designed by using a subcircuit of static CMOS NAND gate and Inverter [1]. The spice code of full adder implementation using Schmitt trigger CMOS NAND gates is in the appendix [B.2]. The full adder is designed by using subcircuit XOR gates and the sub-circuit of this XOR gate is designed by using a subcircuit of Schmitt trigger CMOS NAND gate and Inverter [1]. The static CMOS and Schmitt trigger CMOS NAND gate are similar as in report [1].

The spice code of full adder implementation using Static CMOS XOR gates is in the appendix [B.4]. The spice code of Full adder implementation using Schmitt trigger CMOS XOR gates is in the appendix [B.4].

The Spice code for the Ring oscillator: full adder utilizing static CMOS NAND gates is provided in the appendix [C.1]. The Spice code for the ring oscillator (FA employing Schmitt trigger CMOS NAND gates) is available in the appendix [C.2]. The Spice code for the ring oscillator (FA implemented with static CMOS XOR gates) is detailed in the appendix [C.3]. Lastly, the Spice code for the ring oscillator (FA utilizing Schmitt trigger CMOS XOR gates) is presented in the appendix [C.4].

The Spice code for the 4bit RCA: (FA) utilizing static CMOS NAND gates is provided in the appendix [D.1]. The Spice code for the 4bit RCA: FA employing Schmitt trigger CMOS NAND gates is available in the appendix [D.2]. The Spice code for the 4bit RCA: FA implemented with static CMOS XOR gates is detailed in the appendix [D.3]. Lastly, the Spice code for the 4bit RCA: FA utilizing Schmitt trigger CMOS XOR gates is presented in the appendix [D.4].

2.4 Simulation and analysis:

2.4.1 AIMSPICE simulator:

AIMSPICE simulator used to check the functionality of the different circuits like static CMOS inverter, Schmitt trigger CMOS inverter, CMOS NAND gate, and Schmitt trigger NAND gate, full adders, ring oscillator, RCA etc. The SPICE code for these circuits can be found in the Appendix. **Temperature variation:** Nominal and operating temperatures can change according to requirements as in the figure 12.

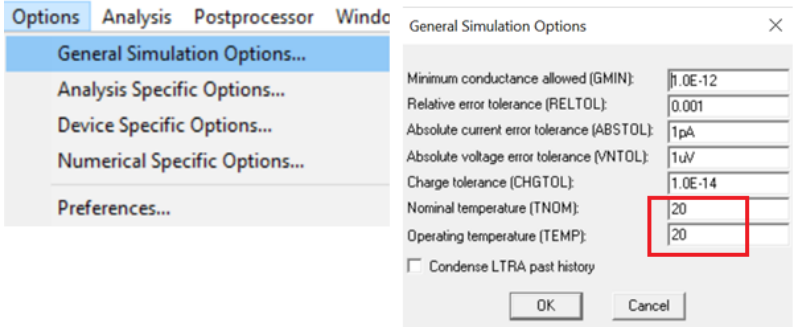


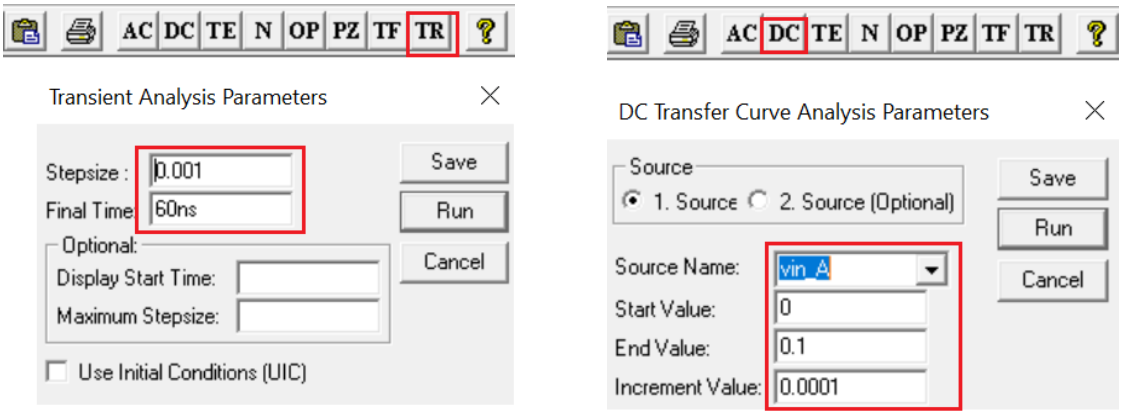
Figure 12: Temprature variation

Source: [**Snap AIMSPICE**].

DC transfer curve analysis is utilized to examine the voltage transfer characteristic(VTC) and calculate the noise margin of a circuit. For the analysis, set the parameters for the analysis: the name of the voltage source (input), the starting and ending values, and the increment for each step (consult the figure 13b which provides a visual instruction for setting these parameters). After setting these parameters, save and run the analysis. This process generates a plot showing the

[1]TFE4590-Specialization project[2023], [Muhammad Naseer ud din], [Ultra low voltage logic- Schmitt trigger based vs Static CMOS].

relationship between the input and output voltages. From the VTC plot, the noise margin can be calculated. Save the generated plots in the .out file format.



(a) (b)

Figure 13: (a)Transient Analysis parameter; (b) DC analysis parameter.

2.4.2 AIM-POSTPROCESSOR:

Once the simulation results are saved in the ".out" file format from AIMSPICE, they can be loaded into AIM-POSTPROCESSOR to generate more detailed and clearer plots. The resulting plots can be saved in a ".txt" file format.

2.4.3 Python Scripts for Data Visualization:

The Python scripts are utilized to process the simulation data and generate graphs. The Python script [A.1] generates graphs between Vin and Vout which show different variables for the noise margin calculation. These scripts are used the ".txt" file, Which is saved from AIM-POSTPROCESSOR. Python scripts calculate the values of VIH, VOH, VIL, and VOL and draw the tangent. The aim of using Python script is to produce clearer and more detailed plots as the original plots from AIMSPICE and AIM-POSTPROCESSOR may not be adequate in terms of clarity. Start of simulation with the different circuits like the full adder, RCA, and ring Oscillator gate at 90 nm.

Description of the Python code [A.1]: The script imports numpy for numerical operations, and matplotlib.pyplot for plotting. It reads data from a text file 'test.txt' that contains pairs of input-output voltages. It computes the derivative of the output voltage with respect to the input voltage and finds certain important indices such as where the derivative is -1, and where the output voltage equals the input voltage. It plots the input-output data and draws tangents to the curve at the critical points. The script identifies key parameters such as the voltage at the midpoint where the output equals the input (VM), and the intersections on the upper and lower tangents. It calculates the high and low noise margins (NMH, NML) which are important measures of the robustness of a digital logic gate to electrical noise. It adjusts the plot's attributes like axes limits, legend, title, grid, etc. to make the plot more readable. Finally, it outputs the plot and prints the high and low noise margins. In the graph Values of $V_{IL}, V_{OL}, V_{IH}, V_{OH}$, and VM will be printed as in the figure 14 and value of Noise margin high and low will be printed in the terminal bar as in the figure 15.

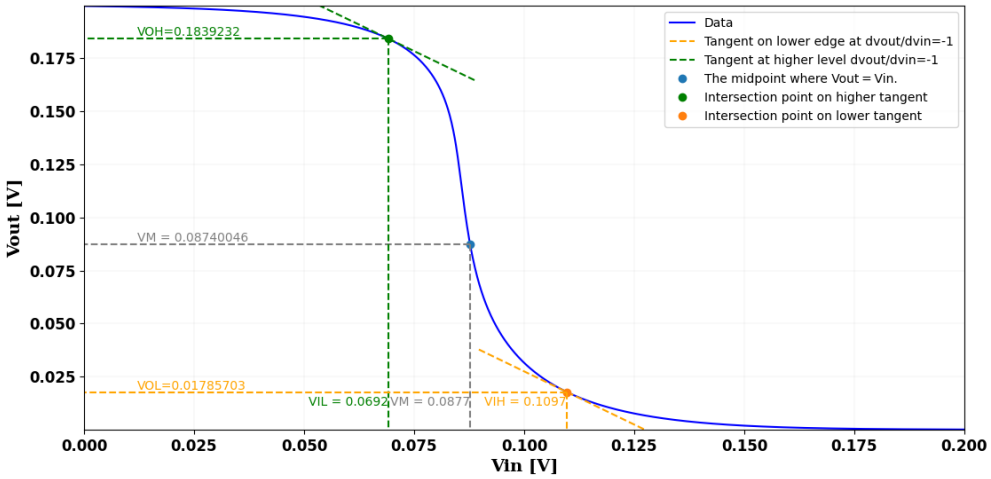


Figure 14: Noise margin output graph

Source: [**subsec: noise margin script**].

```
PROBLEMS  OUTPUT  DEBUG CONSOLE  TERMINAL

[Done] exited with code=0 in 57.685 seconds

[Running] python -u "c:\Users\Naseer\Desktop\chart\graph\28_test.py"
Noise margin high (NMH) = VOH - VIH = 0.08712333 - 0.0419 = 0.04522333 = 45.2233 mV
Noise margin low (NML) = VIL - VOL = 0.0143 - 0.01379263 = 0.00050737 = 0.5074 mV
```

Figure 15: Noise margin values.

Source: [**subsec: noise margin script**].

The Python script [A.2] generates graphs between time and Vin, Vout which shows different times for the propagation delay calculation. These scripts are used the ".txt" file, Which is saved from AIM-POSTPROCESSOR. The aim of using Python script is to produce clearer and more detailed plots as the original plots from AIMSPICE and AIM-POSTPROCESSOR may not be adequate in terms of clarity. Python script needs to be modified and changed according to the graph. There is no significant change only minor changes if needed.

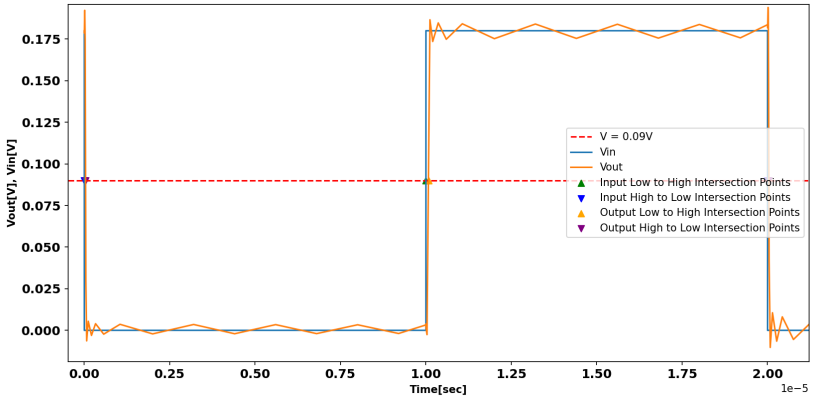


Figure 16: Propagation delay simulation graph

Source: [**Propagation delay script**].

```
t_plh = Output High to Low Intersection Points (time) - Input Low to High Intersection Points (time) = 7.418560667200264e-08 = 74.18560667200263 nS
t_phl = Output Low to High Intersection Points (time) - Input High to Low Intersection Points (time) = 3.816038862713166e-08 = 38.16038862713166 nS
tn= (t_plh_n + t_phl_n ) / 2 =  56.17299764956715
```

Figure 17: delay calcultion.

Source: [**Propagation delay script**].

The Python script [A.3] analyzes current data from 'raw data.txt' for the ring oscillator. It loads the time and current values, calculates the average current using the trapezoidal rule, and then plots the current against time. The Python script [A.4] analyzes current data from 'raw data.txt' for the ripple carry adder. It loads the time and current values, calculates the average current using the mean of the absolute values of the current array, and then plots the current against time. Both scripts provide a quick visual representation of the current profile and highlight the average current level.

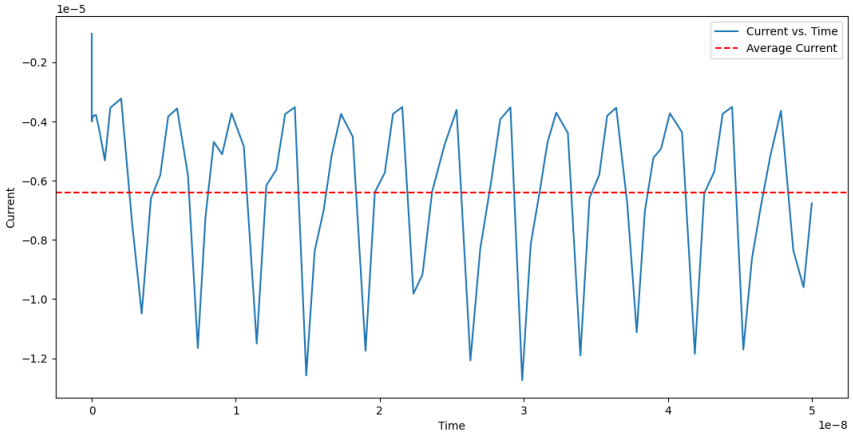


Figure 18: Average current.

Source: [**Average current script1**].

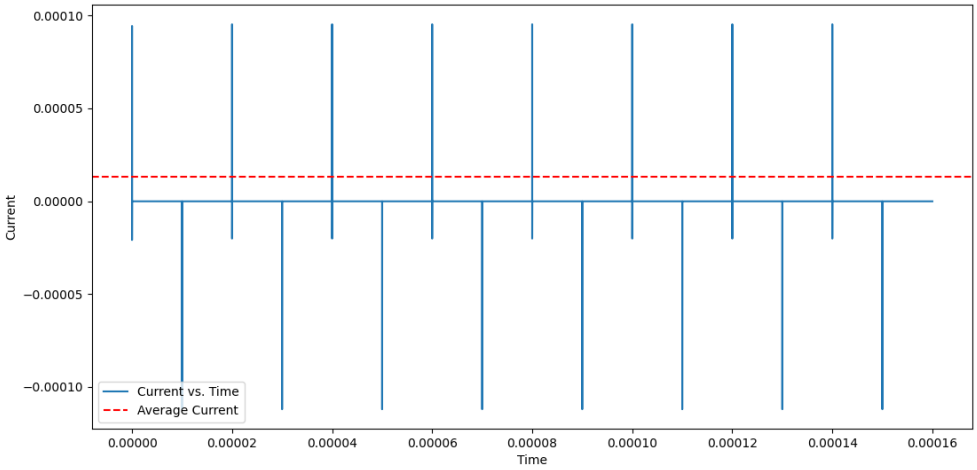


Figure 19: Average Current2.

Source: [**Average current script2**].

3 Results

The result section is categorized into four subsections. The first subsection focuses on topology1, the second subsection on topology2, the third subsection on ring oscillators, and the fourth subsection on RCAs. The results of static CMOS and Schmitt trigger CMOS circuits demonstrate the Noise margin, Propagation delay, average power, Power-delay product, and Energy-delay product at various configurations, dimensions(Width and length), and different process corners such as SS(Slow-Slow), SF(Slow-Fast), TT(Typical-Typical), FS(Fast-Slow), and FF(Fast-Fast).

3.1 Topology1: Full Adder Implementation using Static CMOS vs Schmitt Trigger NAND gates:

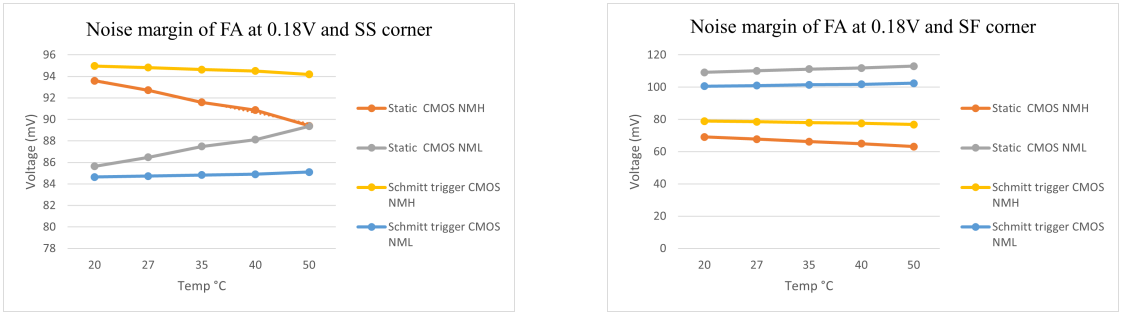
The functionality of full adders implementation using static CMOS, and Schmitt trigger CMOS are shown in the table 2.

Table 2: Full Adder based on static CMOS and Schmitt trigger CMOS.

Inputs			Intermediate				Outputs	
A	B	C	A'	B'	$NANDgateA, B'$	$XORA, B$	SUM	$CARRY$
0	0	0	1	1	1	0	0	0
0	0	1	1	1	1	0	1	0
0	1	0	1	0	1	1	1	0
0	1	1	1	0	1	1	0	1
1	0	0	0	1	0	1	1	0
1	0	1	0	1	0	1	0	1
1	1	0	0	0	1	0	0	1
1	1	1	0	0	1	0	1	1

3.1.1 Noise margins of Topology1: Full Adder Implementation using Static CMOS vs Schmitt Trigger NAND gates:

Figure 20a depicts the noise margin of full adders at 180mV in the SS corner. Static CMOS NM_H and NM_L are changing significantly by raising the temperature. But Schmitt triggers CMOS NM_H and NM_L remain remarkably unaffected by temperature changes, showcasing a robust and stable behavior. Figure 21b shows SF corner at 180mV, Static CMOS NM_H and NM_L are changing by raising the temperature but not significantly as SS corner.

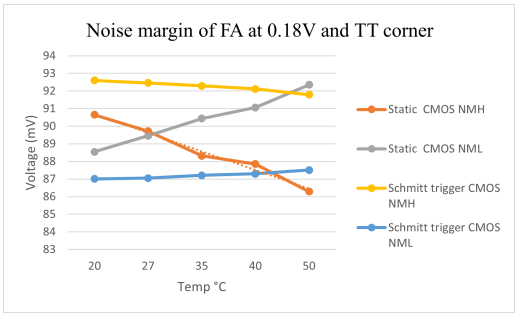


(a) (b)

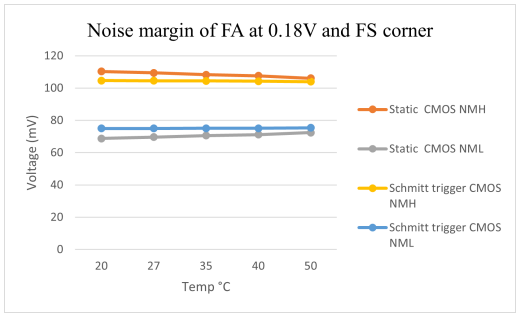
Figure 20: (a) fig: Noise margin of the FA at 0.18v and SS corner; (b) fig: Noise margin of the FA at 0.18v and SF corner.

Figure 21a the TT corner, and figure22 FF corners are at 180mV, the Static CMOS NM_H and NM_L are notably influenced by rising temperatures. On the flip side, Schmitt trigger CMOS

NM_H and NM_L are remain remarkably unaffected by temperature changes. Figure 21b FS corner is showing almost the same trend for both static CMOS and Schmitt trigger CMOS Noise margins.



(a)



(b)

Figure 21: (a) fig: Noise margin of the FA at 0.18v and TT corner; (b) fig: Noise margin of the FA at 0.18v and FS corner.

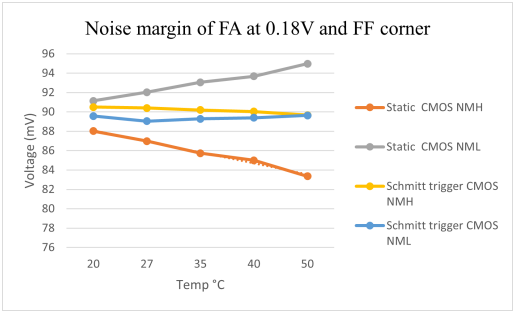


Figure 22: Noise margin of the FA at 0.18v and FF corner.

The first part of table 3 is about when all transistors have the same L and W, showing that all corners have positive noise margins at 27 °C. The 2nd part is when transistors have different dimensions(using dimensions from the report [1]), showing the different values of the noise margins at various temperatures. When the inputs in the test bench are different, the [2] full adder's sum will vary, but the carry will consistently be 0. While both [3] sum and carry changes together when testbench is set all inputs are the same.

Table 3: Noise margin of Full Adder based on Static CMOS Nand gates and Inverters

Supply	temp	corner	[2] Full adder Sum (mV)			[3] FA Sum (mV)		[3] FA Carry (mV)	
$Voltage$	$°C$		VM	NM_H	NM_L	NM_H	NM_L	NM_H	NM_L
When all transistors have w = l = 0.1u									
0.18	27	SS	34.4	128.61	32.27	103.16	24.20	80.33	42.56
0.18	27	SF	45.3	127.15	44.24	107.19	35.61	84.73	56.9
0.18	27	TT	34.3	128.74	32.14	105.04	23.99	78.01	39.99
0.18	27	FS	26.2	101.52	17.52	72.57	11.46	50.82	32.705
0.18	27	FF	33.5	127.34	30.72	101.44	18.46	76.78	44.28
VM=Vdd/2 at 'tt' corner, when NAND gate (Wp/Lp = 0.85u/0.3u, Wn/Ln = 0.1u/0.1u)									
VM=Vdd/2 at 'tt' corner,Inverter Wp/Lp=Wn/Ln=0.1u/0.1u									
0.18	20	SS	86	93.6	85.64	89.63	80.90	71.08	99.41
0.18	27	SS	87	92.72	86.48	88.46	81.29	69.64	100.16
0.18	35	SS	88.1	91.59	87.49	87.06	81.72	67.97	100.97
0.18	40	SS	88.6	90.87	88.12	86.16	81.97	66.91	101.45
0.18	50	SS	90.2	89.41	89.37	84.28	82.42	64.77	102.36
0.18	20	SF	110.7	69.12	109.19	66.64	100.64	49.12	118.36
0.18	27	SF	112	67.79	110.16	65.36	100.45	47.63	118.65
0.18	35	SF	113.5	66.23	111.22	63.39	100.73	45.69	119.19
0.18	40	SF	114.3	65.02	111.84	62.25	100.67	44.52	119.30
0.18	50	SF	116.5	63.17	113.02	59.84	100.41	42.18	119.34
0.18	20	TT	89.1	90.65	88.55	86.77	83.33	68.18	101.96
0.18	27	TT	90	89.72	89.46	85.90	83.68	67.06	102.64
0.18	35	TT	91	88.32	90.44	84.14	84.05	65.08	103.38
0.18	40	TT	91.9	87.85	91.06	83.21	84.27	64.03	103.81
0.18	50	TT	93.4	86.29	92.35	81.27	84.65	61.90	104.61
0.18	20	FS	69.1	110.27	68.80	103.42	64.67	85.38	82.90
0.18	27	FS	69.9	109.41	69.58	102.12	65.10	84.02	83.56
0.18	35	FS	70.9	108.32	70.54	100.55	65.62	82.43	84.31
0.18	40	FS	71.1	107.63	71.12	99.51	65.95	81.43	84.76
0.18	50	FS	72.9	106.09	72.45	97.30	66.63	79.39	85.65
0.18	20	FF	91.8	88.02	91.14	84.17	85.35	65.63	104.04
0.18	27	FF	92.6	86.98	92.03	82.92	85.67	64.20	104.66
0.18	35	FF	93.9	85.74	93.06	81.43	86.00	62.53	105.33
0.18	40	FF	94.3	84.99	93.68	80.46	86.19	61.48	105.71
0.18	50	FF	96.2	83.35	94.97	78.41	86.52	59.35	106.40

[2]When the 2 inputs are same 3rd is different.
[3]When all three inputs are the same '1' or '0'.

[1]Specialization project[2023], [Muhammad Naseer ud din], [Ultra low voltage logic- Schmitt trigger based vs Static CMOS].

The first part of table4 is about when all transistors have the same L and W, showing that all corners have positive noise margins. The 2nd part is when transistors have different dimensions, using dimensions from the report [1]. NM_H is the same for both Sum and carry, while NM_L is the same for both Sum and carry.

Table 4: Noise margins of full Adder implementation using Schmitt trigger Nand gates

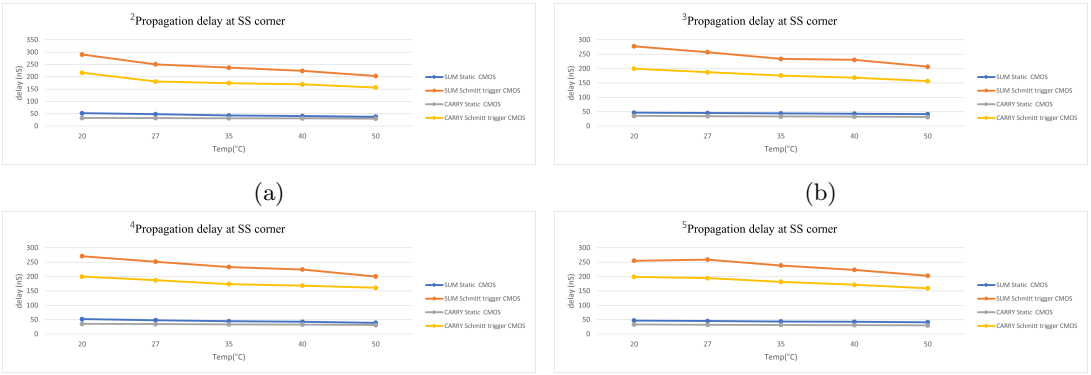
Supply Voltage	temp	corner	VM	NM_H	NM_L
(V)	$°C$		(mV)	(mV)	(mV)
All transistor'S have W=0.1U, and L= 0.1U					
0.18	27	SS	49.1	130.2	47.81
0.18	27	SF	58.1	120.92	57.56
0.18	27	TT	49.5	117.22	48.26
0.18	27	FS	34.2	138.9	39.33
0.18	27	FF	49.1	129.98	47.98
All PMOS'S have W=0.45U, and L= 0.2U. And, all NMOS'S have W=0.1U, and L=0.2U. Inverter's have W=0.1U, and L= 0.2U, for both PMOS and NMOS					
0.18	20	SS	85	94.96	84.64
0.18	27	SS	85.1	94.82	84.73
0.18	35	SS	85.3	94.64	84.83
0.18	40	SS	85.4	94.51	84.91
0.18	50	SS	85.7	94.19	85.10
0.18	20	SF	100.9	78.96	100.64
0.18	27	SF	101.4	78.53	101.01
0.18	35	SF	101.9	77.98	101.49
0.18	40	SF	102.3	77.61	101.79
0.18	50	SF	103.1	76.82	102.47
0.18	20	TT	87.3	92.60	87.01
0.18	27	TT	87.5	92.46	87.05
0.18	35	TT	87.7	92.29	87.21
0.18	40	TT	87.8	92.12	87.30
0.18	50	TT	88.1	91.79	87.51
0.18	20	FS	75.3	104.64	74.97
0.18	27	FS	75.4	104.56	74.99
0.18	35	FS	75.5	104.41	75.06
0.18	40	FS	75.6	104.29	75.13
0.18	50	FS	76	103.96	75.34
0.18	20	FF	89.4	90.57	89.57
0.18	27	FF	89.5	90.41	89.04
0.18	35	FF	89.7	90.19	89.29
0.18	40	FF	89.9	90.03	89.39
0.18	50	FF	90.3	89.67	89.63

[1]Specialization project[2023], [Muhammad Naseer ud din], [Ultra low voltage logic- Schmitt trigger based vs Static CMOS].

3.1.2 Propagation delay of Topology1: Full Adder Implementation using Static CMOS vs Schmitt Trigger CMOS NAND gates:

The graphs in the figures illustrate where all three inputs change from 0 to 1 and from 1 to 0 simultaneously. Additionally, the case where 2 inputs change together from 1 to 0 and from 0 to 1 while the 3rd input remains different. The propagation delay for sum and carry in the static CMOS circuit is almost the same as the temperature rise for all corners. While the delay in Schmitt trigger CMOS is high but decreases with a temperature rise. The propagation delay of a full adder using the static CMOS NAND gate is consistently lower than that of a full adder using the Schmitt trigger CMOS NAND gate across all process corners and temperatures.

Figures 23a, 23b, 23b and 23c at the SS corner demonstrate that the propagation delay for sum and carry in the static CMOS circuit is almost the same as the temperature rise. While the delay in Schmitt trigger CMOS is high but decreases with a temperature rise.

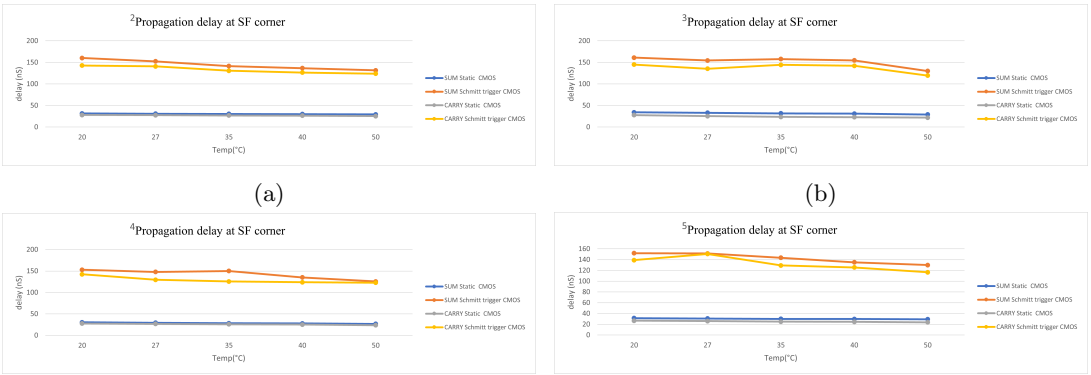


(a) (b)

(c) (d)

Figure 23: Propagation delay of FA1 at SS corner (a) ${}^2SS; (b)^3SS; (c)^4SS; (d)^5SS$.

Figures 24a, 24b, 24b and 24c at the SF corner demonstrate that the propagation delay for sum and carry in the static CMOS circuit is almost the same as the temperature rise. While the delay in Schmitt trigger CMOS is high but decreases with a temperature rise.

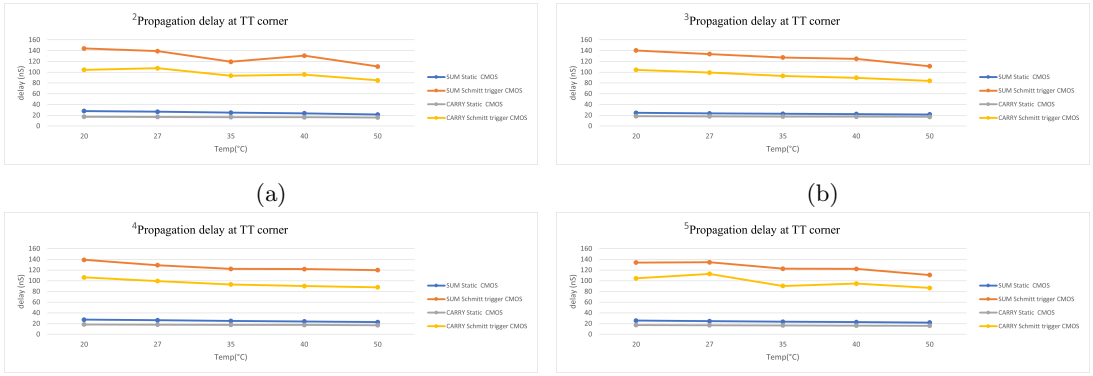


(a) (b)

(c) (d)

Figure 24: Propagation delay of FA1 at SF corner (a) ${}^2SF; (b)^3SF; (c)^4SF; (d)^5SF$.

Figures 25a, 25b, 25b and 25c at the TT corner demonstrate that the propagation delay for sum and carry in the static CMOS circuit is almost the same as the temperature rise. While the delay in Schmitt trigger CMOS is high but decreases with a temperature rise.

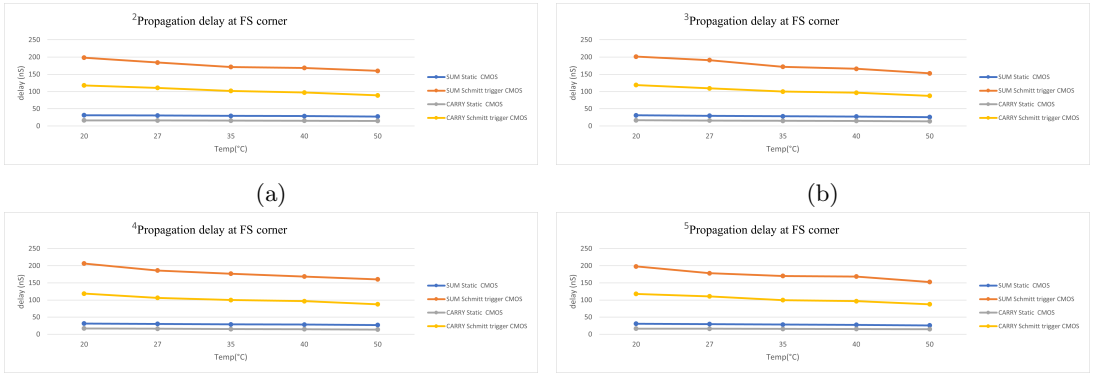


(a) (b)

(c) (d)

Figure 25: Propagation delay of FA1 at TT corner (a) ${}^2TT; (b)^3TT; (c)^4TT; (d)^5TT$.

Figures 26a, 26b, 26b and 26c at the FS corner demonstrate that the propagation delay for sum and carry in the static CMOS circuit is almost the same as the temperature rise. While the delay in Schmitt trigger CMOS is high but decreases with a temperature rise.

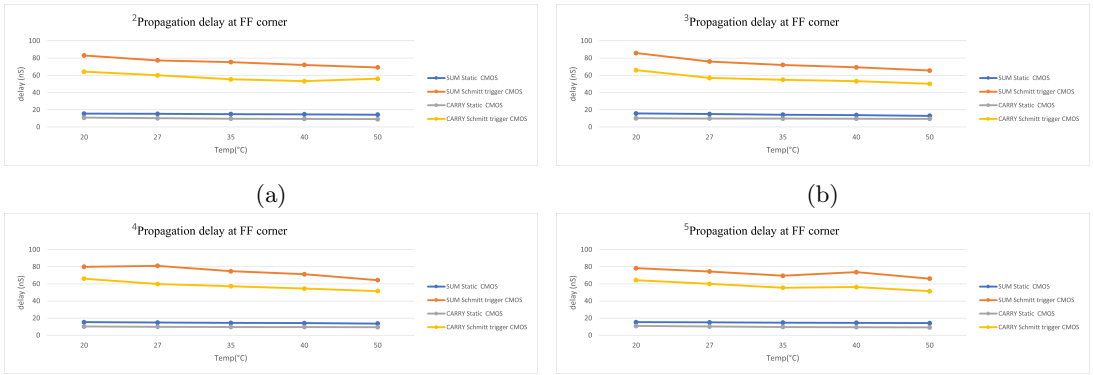


(a) (b)

(c) (d)

Figure 26: Propagation delay of FA1 at FS corner (a) ${}^2FS; (b)^3FS; (c)^4FS; (d)^5FS$.

Figures 27a, 27b, 27b and 27c at the FF corner demonstrate that the propagation delay for sum and carry in the static CMOS circuit is almost the same as the temperature rise. While the delay in Schmitt trigger CMOS is high but decreases with a temperature rise.



(a) (b)

(c) (d)

Figure 27: Propagation delay of FA1 at FF corner (a) ${}^2FF; (b)^3FF; (c)^4FF.(d)^5FF$.

Table 5 details the propagation delay of static CMOS NAND gates and Inverters based FA and demonstrates the delay across various combinations of input. This includes simultaneous transitions of all three inputs[2] from 0 to 1, all three [3] from 1 to 0, [4] two inputs change together(1 to 0) while the third is different(0 to 1), and [5] two inputs change together(0 to 1) while the third is different(1 to 0). These results are measured at various corners and temperatures, indicating the decrease in delay for both sum and carry with the increase in temperature.

Table 5: Propagation delay of full adder implementation using static CMOS Nand gate

Supply	temp	corner	[2]Pro. delay (nS)		[3]Pro. delay (nS)		[4]Pro. delay (nS)		[5]Pro. delay (nS)	
(V)	$°C$		Sum	$Carry$	Sum	$Carry$	Sum	$Carry$	Sum	$Carry$
0.18	20	SS	49.12	33.19	46.79	35.48	51.82	35.54	46.97	33.29
0.18	27	SS	46.66	32.40	45.47	34.53	48.14	34.58	45.30	32.44
0.18	35	SS	43.17	31.56	43.92	33.43	44.66	33.58	43.63	31.60
0.18	40	SS	40.56	31.08	43.06	32.73	42.60	32.97	42.70	31.11
0.18	50	SS	37.84	30.16	41.43	31.27	39.10	31.53	40.95	30.19
0.18	20	SF	31.22	28.07	34.17	27.88	30.42	27.53	31.32	26.61
0.18	27	SF	30.46	27.50	33.13	25.45	29.35	26.72	30.69	25.83
0.18	35	SF	29.67	26.80	31.84	23.58	28.29	25.80	30.05	24.95
0.18	40	SF	29.18	26.35	30.97	22.85	27.72	25.18	29.74	24.48
0.18	50	SF	28.18	25.31	29.04	21.82	26.80	23.57	29.22	23.72
0.18	20	TT	25.74	17.39	24.47	18.36	27.30	18.38	25.66	17.35
0.18	27	TT	24.84	16.90	23.47	18.03	26.20	18.05	24.47	16.91
0.18	35	TT	23.77	16.48	22.66	17.69	24.85	17.68	23.40	16.51
0.18	40	TT	23.08	16.24	22.25	17.48	24.00	17.45	22.81	16.30
0.18	50	TT	21.81	15.72	21.56	17.09	22.68	17.02	21.79	15.94
0.18	20	FS	29.64	16.59	31.10	16.95	31.29	17.00	30.74	16.60
0.18	27	FS	28.62	16.17	29.86	16.11	30.21	16.17	29.68	16.18
0.18	35	FS	27.25	15.74	28.48	15.26	29.06	15.30	28.40	15.75
0.18	40	FS	26.38	15.49	27.62	14.76	28.41	14.79	27.59	15.50
0.18	50	FS	24.9	14.99	25.88	13.77	27.14	13.80	25.96	15.00
0.18	20	FF	14.61	10.88	15.74	10.24	15.32	10.20	15.37	10.89
0.18	27	FF	14.26	10.26	15.12	9.96	14.91	9.94	15.09	10.25
0.18	35	FF	13.91	9.73	14.37	9.76	14.44	9.74	14.77	9.72
0.18	40	FF	13.71	9.53	13.91	9.67	14.17	9.66	14.58	9.51
0.18	50	FF	13.34	9.19	13.05	9.52	13.68	9.51	14.24	9.18

[2]When all 3 inputs change together(0 to 1).[3]When all 3 inputs change together(1 to 0).
[4]When 2 inputs change together(1 to 0) and 3rd is different(0 to 1).
[5]When 2 inputs change together(0 to 1) and 3rd is different(1 to 0).

Table 6 details the propagation delay of Schmitt trigger CMOS NAND gates and Inverters based FA and demonstrates the delay across various combinations of input. This includes simultaneous transitions of all three inputs[2] from 0 to 1, all three inputs [3] from 1 to 0, two inputs[4] change together(1 to 0) while the third is different(0 to 1), and [5] two inputs change together(0 to 1) while the third is different(1 to 0). These results are measured at various corners and temperatures, indicating the decrease in delay for both sum and carry with the increase in temperature.

Table 6: Propagation delay of full adder Implementation using Schmitt trigger CMOS Nand gate

Supply	temp	corner	[2] Pro. delay (nS)		[3] Pro. delay (nS)		[4] Pro. delay (nS)		[5] Pro. delay (nS)	
(V)	$°C$		Sum	$Carry$	Sum	$Carry$	Sum	$Carry$	Sum	$Carry$
0.18	20	SS	245.75	213.94	277.77	199.49	270.99	200.14	255.28	198.99
0.18	27	SS	218.05	187.34	257.14	187.24	251.76	187.50	259.23	194.67
0.18	35	SS	215.65	190.46	233.53	175.98	233.28	173.87	238.74	181.76
0.18	40	SS	202.03	182.19	230.43	168.48	224.70	168.60	223.58	171.50
0.18	50	SS	179.63	164.15	206.54	156.23	200.15	161.09	202.87	159.20
0.18	20	SF	144.71	145.34	160.98	144.99	152.91	142.35	151.99	139.15
0.18	27	SF	138.70	137.54	154.47	135.20	147.83	129.68	151.35	150.54
0.18	35	SF	130.53	127.86	157.83	144.23	150.04	125.71	143.51	129.29
0.18	40	SF	128.17	124.56	154.68	142.12	135.24	124.01	134.95	125.56
0.18	50	SF	117.04	119.65	129.91	119.51	125.70	122.84	129.87	116.58
0.18	20	TT	126.63	111.61	140.29	104.43	139.05	106.24	133.99	104.59
0.18	27	TT	122.86	109.53	133.59	99.21	129.10	99.38	134.56	112.89
0.18	35	TT	105.80	92.88	127.24	93.03	122.11	93.14	122.51	90.25
0.18	40	TT	100.38	100.33	124.75	89.47	121.76	90.04	122.25	94.67
0.18	50	TT	98.50	92.59	110.99	83.97	119.92	87.79	110.66	86.49
0.18	20	FS	154.1	122.06	201.37	118.88	206.56	118.81	198.00	117.94
0.18	27	FS	139.48	108.64	191.28	109.29	186.10	106.26	178.10	110.70
0.18	35	FS	128.91	99.43	171.97	99.96	176.92	99.91	170.30	99.73
0.18	40	FS	124.08	96.68	166.20	96.69	168.63	96.65	168.55	96.61
0.18	50	FS	111.18	88.85	152.88	87.53	160.23	87.51	152.48	87.47
0.18	20	FF	69.45	61.98	85.88	66.04	79.95	66.10	78.32	64.34
0.18	27	FF	65.77	59.39	75.98	56.99	81.05	59.82	74.43	60.07
0.18	35	FF	62.00	56.24	72.02	54.84	74.77	57.34	69.47	55.53
0.18	40	FF	59.80	54.91	69.28	53.16	71.28	54.51	73.67	56.34
0.18	50	FF	55.93	50.81	65.57	50.13	64.33	51.52	66.09	51.48

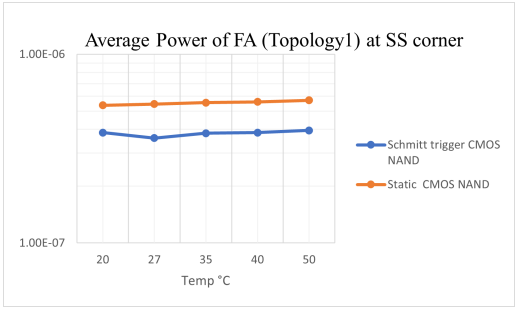
[2]When all 3 inputs change together(0 to 1).[3]When all 3 inputs change together(1 to 0).
[4]When 2 inputs change together(1 to 0) and 3rd is different(0 to 1).
[5]When 2 inputs change together(0 to 1) and 3rd is different(1 to 0).

3.1.3 Average Power of Topology1: Full Adder Implementation using Static CMOS vs Schmitt Trigger CMOS NAND gates:

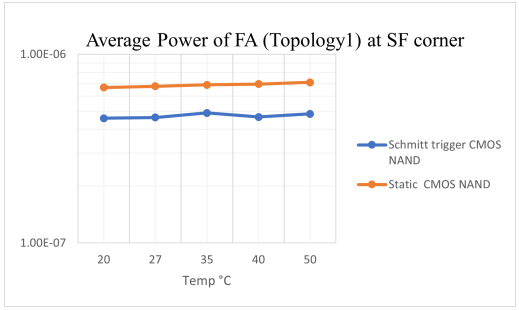
The graphs compare the average power consumption of full adder (Topology1) between static CMOS and Schmitt trigger CMOS. The Average power for static CMOS increases with rising temperature and is consistently higher than that of Schmitt triggers for all process corners.

Figure 28a at SS corner shows an average power for Schmitt trigger CMOS decrease as the temperature rises from 20°C to 27°C, then it begins to increase beyond 27°C.

Figure 28b SF corner demonstrates an average power for Schmitt Trigger CMOS increase with the temperature rise from 20°C to 35°C, dips slightly at 40°C, and then resumes its increase at 50°C.



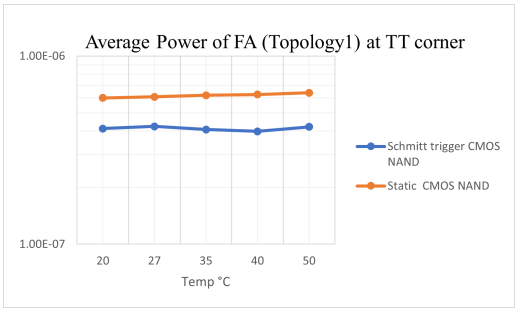
(a)



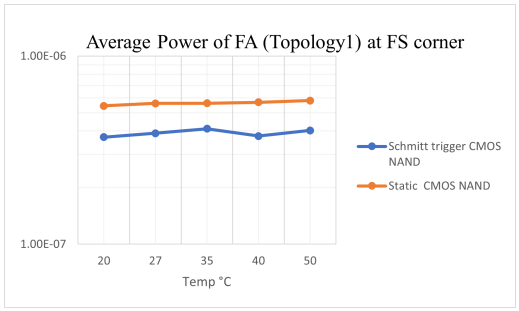
(b)

Figure 28: (a) fig: Average Power of the Full Adder (Typology1) at 0.18v and SS corner; (b) fig: Average Power of the Full Adder (Typology1) at 0.18v and SF corner.

Figure 29a at TT corner indicates an average power for Schmitt Trigger CMOS increase with the temperature rise from 20°C to 27°C, decrease slightly at 35°C and 40°C, and then resumes its increase at 50°C. The graph 29b FS corner shows a similar trend as for SF corner.



(a)



(b)

Figure 29: (a) fig: Average Power of the Full Adder (Typology1) at 0.18v and TT corner; (b) fig: Average Power of the Full Adder (Typology1) at 0.18v and FS corner.

Figure 30 at FF corner indicates an average power for both static CMOS and Schmitt Trigger CMOS increase with the temperature rise.

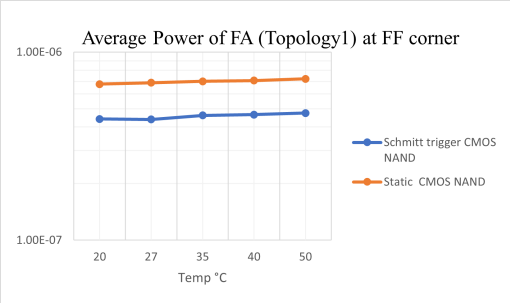


Figure 30: Average Power of the Full Adder (Typology1) at 0.18v and FF corner.

Table 7 provides details about the average current, average power, and power delay product(PDP) of full adder implementation using static CMOS Nand gates across various temperatures and process corners. When comparing the average power at the same temperature across different corners, the SS corner exhibits the lowest average power, followed by FS, TT, SF, and FF has the highest average power among them. The (Power delay product) PDP follows the high to low order, SS, SF, FS, TT, and FF.

Table 7: Average power and energy of full adder using Static CMOS Nand gates

voltage	temp	corner	Average I(Vdd)	Average Power	Pro. delay	PDP
(V)	$°C$		(nA)	(nW)	(nS)	(aJ)
0.18	20	SS	2984	537	49.12	26377
0.18	27	SS	3030	545	46.66	25429
0.18	35	SS	3082	554	43.17	23916
0.18	40	SS	3113	560	40.56	22713
0.18	50	SS	3176	571	37.84	21606
0.18	20	SF	3708	667	31.22	20823
0.18	27	SF	3765	677	30.46	20621
0.18	35	SF	3830	689	29.67	20442
0.18	40	SF	3868	696	29.18	20309
0.18	50	SF	3947	710	28.28	20007
0.18	20	TT	3330	599	25.74	15418
0.18	27	TT	3381	608	24.84	15102
0.18	35	TT	3440	619	23.77	14713
0.18	40	TT	3476	625	23.08	14425
0.18	50	TT	3548	638	21.81	13914
0.18	20	FS	3025	544	29.64	16124
0.18	27	FS	3120	561	28.62	16055
0.18	35	FS	3126	562	27.25	15314
0.18	40	FS	3158	568	26.38	14983
0.18	50	FS	3225	580	24.9	14442
0.18	20	FF	3759	676	14.61	9876
0.18	27	FF	3818	687	14.26	9796
0.18	35	FF	3884	699	13.91	9723
0.18	40	FF	3926	706	13.71	9679
0.18	50	FF	4007	721	13.34	9618

Table 8 presents data on the average current and average power, PDP of full adder implementation using Schmitt trigger CMOS XOR gate over a range of temperatures and process corners. At the same temperature, the average power starts at its lowest in the FS corner, then rises through SS, TT, and FF, reaching its peak in the SF corner. The (Power delay product) PDP follows the high to low order, SS, SF, FS, TT, and FF.

Table 8: Average power and energy of full adder based on Schmitt trigger CMOS Nand gates

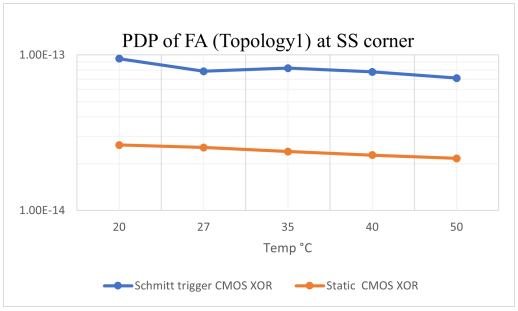
voltage	temp	corner	average Current	average Power	Pro. delay	PDP
(V)	$°C$		(nA)	(nW)	(nS)	(aJ)
0.18	20	SS	2139	385	245.75	94613
0.18	27	SS	2000	360	218.05	78498
0.18	35	SS	2126	382	215.65	82378
0.18	40	SS	2142	385	202.03	77781
0.18	50	SS	2194	395	179.63	70953
0.18	20	SF	2546	458	144.71	66277
0.18	27	SF	2576	463	138.7	64218
0.18	35	SF	2717	489	130.53	63829
0.18	40	SF	2583	465	128.17	59599
0.18	50	SF	2687	483	117.04	56530
0.18	21	TT	2293	412	126.63	52171
0.18	27	TT	2352	423	122.86	51969
0.18	35	TT	2266	407	105.8	43060
0.18	40	TT	2214	398	100.38	39951
0.18	50	TT	2342	421	98.5	41468
0.18	20	FS	2062	371	154.1	57171
0.18	27	FS	2162	389	139.48	54257
0.18	35	FS	2284	411	128.91	52982
0.18	40	FS	2091	376	124.08	46654
0.18	50	FS	2241	403	111.18	44805
0.18	20	FF	2452	441	69.45	30627
0.18	27	FF	2440	439	65.77	28873
0.18	35	FF	2565	461	62	28582
0.18	40	FF	2588	465	59.8	27807
0.18	51	FF	2637	474	55.93	26510

3.1.4 PDP of Topology1: Full Adder Implementation using Static CMOS vs Schmitt Trigger CMOS NAND gates:

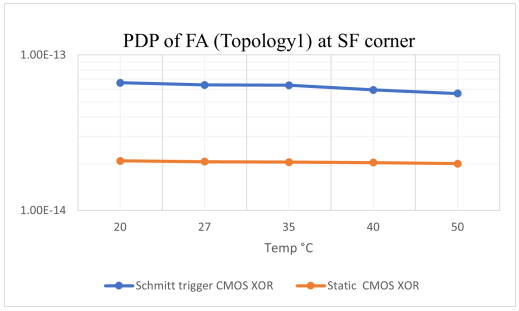
The detailed numbers of PDP for static CMOS are in the table 7 while for Schmitt triggers CMOS are in the table 8. A little bit variations noticed in PDP with a rise in temperature for static CMOS for all process corner.

Figure 31a at the SS corner indicates PDP for Schmitt Trigger CMOS decreases with the temperature rise from 20°C to 27°C, increases slightly at 35°C, and then resumes its little decrease at 40°C.

Figure 31b SF corner demonstrates a small decrease in PDP with the increase in temperature for both cases.



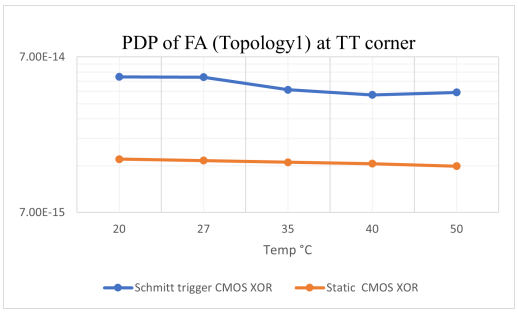
(a)



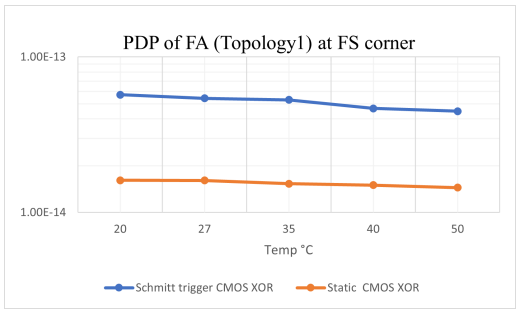
(b)

Figure 31: (a) fig: PDP of the Full Adder (Typology1) at 0.18v and SS corner; (b) fig: PDP of the Full Adder (Typology1) at 0.18v and SF corner.

Figure 32a at the TT corner demonstrates PDP for Schmitt Trigger CMOS slightly decreases with the temperature rise, but at 50°C it slightly increases. The 32b at the FS corner follows the same trend as the SF corner.



(a)



(b)

Figure 32: (a) fig: PDP of the Full Adder (Typology1) at 0.18v and TT corner; (b) fig: PDP of the Full Adder (Typology1) at 0.18v and FS corner.

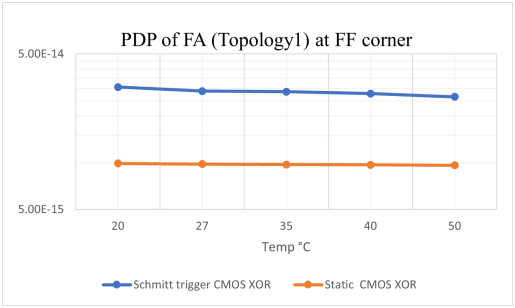


Figure 33: PDP of the Full Adder (Typology1) at 0.18v and FF corner.

Figure 33 at the FF corner shows a slight decrease in PDP with the temperature rise for Schmitt triggers CMOS and for static CMOS looks constant.

3.1.5 ARCHITECTURES of Topology1: Full Adder Implementation using Static CMOS vs Schmitt Trigger CMOS NAND gates and Inverters:

The static CMOS NAND full adder, incorporating 40 transistors, comprises sum and carry. The sum is designed using 2 XOR gates, Each XOR gate is constructed from 3 NAND gates and 2 inverters, with each NAND gate utilizing 4 transistors and each inverter 2 transistors. The carry is designed by using 3 NAND gates, with each NAND gate utilizing 4 transistors. A Schmitt trigger CMOS NAND full adder with 106 transistors, comprises sum and carry. The sum is designed using 2 XOR gates. Each XOR gate is made from 3 NAND gates and 2 inverters, with each NAND gate utilizing 10 transistors and each inverter 4 transistors. The carry is designed by using 3 NAND gates, with each NAND gate utilizing 10 transistors. The number of transistors and number of nodes are given in the table 9.

Table 9: Transistor count and driven nodes for Topology1.

	Number of transistors		Number of driven nodes	
	Static CMOS	**Schmitt trigger CMOS**	**Static CMOS**	**Schmitt trigger CMOS**
NAND2	4	10	2	5
XOR	14	38	8	21
Sum	28	76	16	42
Carry	12	30	6	15
Total(FA)	40	106	22	57

3.2 Topology2: Full Adder Implementation using Static CMOS vs Schmitt Trigger CMOS XOR gates:

The functionality of full adders implementations using static CMOS, and Schmitt trigger CMOS are shown in the table 10.

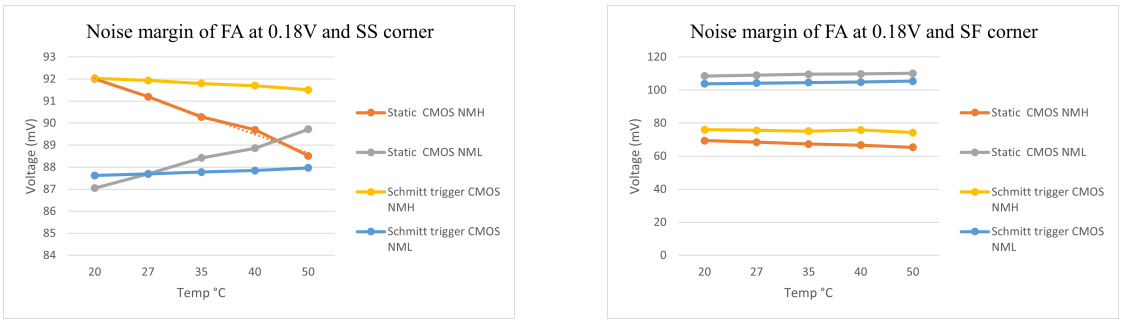
Table 10: Full Adder based on XOR using static CMOS and Schmitt trigger CMOS.

Inputs			Intermediate			Outputs	
A	B	C	A'	B'	$XORA, B$	SUM	$CARRY$
0	0	0	1	1	0	0	0
0	0	1	1	1	0	1	0
0	1	0	1	0	1	1	0
0	1	1	1	0	1	0	1
1	0	0	0	1	1	1	0
1	0	1	0	1	1	0	1
1	1	0	0	0	0	0	1
1	1	1	0	0	0	1	1

3.2.1 Noise margins of Topology2: Full Adder Implementation using Static CMOS vs Schmitt Trigger CMOS XOR gates:

Figure 34a of SS corner, shows that in the static CMOS FA, NMH goes low and NML goes high respectively as temperature increases. For Schmitt trigger CMOS FA, the noise margins remain almost the same with the temperature rise.

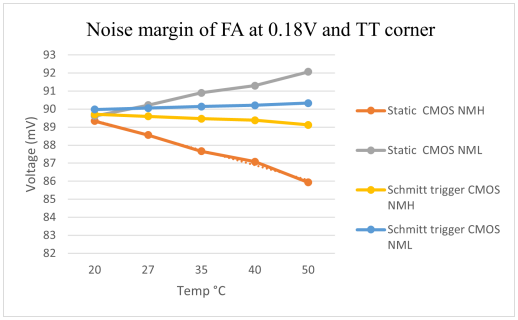
Figure 34b of SF and 35b of FS corner, shows that both static CMOS FA and Schmitt trigger CMOS FA follow almost the similar trend with the temperature rise.



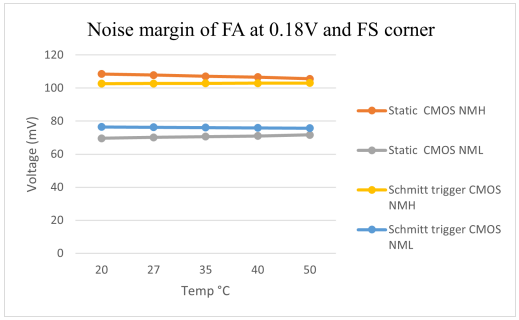
(a) (b)

Figure 34: (a)Noise margin of the FA at 0.18v and SS corner; (b) Noise margin of the FA at 0.18v and SF corner.

Figure 35a of TT and 36 of FF corner, shows that static CMOS FA, NMH and NML go low and high respectively with the rise in temperature. While Schmitt triggers CMOS FA, the noise margins remain almost unchanged with the temperature rise.



(a)



(b)

Figure 35: (a) Noise margin of the FA at 0.18v and TT corner; (b) Noise margin of the FA at 0.18v and FS corner.

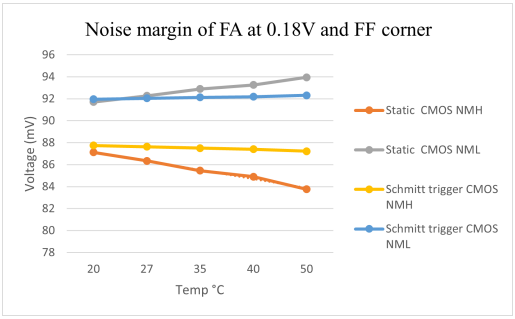


Figure 36: Noise margin of the FA at 0.18v and FF corner.

Table 11 demonstrates the noise margin of the full adder using a simple CMOS XOR gate. Dimensions are set at VM=Vdd/2 at the 'TT' corner. All transistors of the pull-up network have W=1.1U and L=0.3U. While All transistors of the pull-down network have W=0.1U, L=0.3U. The test bench is set when both sum and carry are 1 and 0.

Table 11: Noise margins of full adder implementation using simple XOR gate

Supply Voltage	temp	corner	XOR gate(mV)		Full adder Sum(mV)			Full adder Carry(mV)	
V	$°C$		NM_H	NM_L	VM	NM_H	NM_L	NM_H	NM_L
All PMOS'S have W=1.1U, L= 0.3U While All NMOS'S have W=0.1U, L=0.3U									
0.18	20	SS	87.11	82.75	87.4	92.01	87.05	86.00	86.97
0.18	27	SS	86.07	83.06	88.1	91.20	87.70	84.78	87.59
0.18	35	SS	84.86	83.36	89.0	90.28	88.42	83.34	88.29
0.18	40	SS	84.09	83.52	89.5	89.70	88.86	82.42	88.71
0.18	50	SS	82.53	83.77	90.6	88.51	89.72	80.51	89.50
0.18	20	SF	65.61	100.75	110.3	69.38	108.50	61.72	107.98
0.18	27	SF	64.47	100.57	111.2	68.44	109.01	60.12	108.38
0.18	35	SF	63.15	100.22	112.3	67.34	109.50	58.23	108.72
0.18	40	SF	62.32	99.91	112.9	66.67	109.75	57.02	108.86
0.18	50	SF	60.63	99.09	114.2	65.32	110.08	54.52	108.95
0.18	20	TT	84.51	84.88	90.0	89.34	89.61	83.01	89.50
0.18	27	TT	83.49	85.11	90.7	88.56	90.22	81.78	90.08
0.18	35	TT	82.30	85.32	91.6	87.66	90.90	80.32	90.72
0.18	40	TT	81.54	85.42	92.1	87.08	91.30	79.63	91
0.18	50	TT	80.01	85.53	93.1	85.93	92.07	77.46	91.80
0.18	20	FS	100.86	66.12	69.8	108.54	69.63	101.91	69.66
0.18	27	FS	99.81	66.37	70.3	107.87	70.11	100.88	70.13
0.18	35	FS	98.57	68.65	70.9	107.08	70.64	99.64	70.66
0.18	40	FS	97.79	66.81	71.3	106.58	70.97	98.85	70.99
0.18	50	FS	96.17	67.09	72.0	105.55	71.63	97.22	71.63
0.18	20	FF	82.28	86.52	92.3	87.12	91.70	80.40	91.55
0.18	27	FF	81.27	86.68	93.0	86.35	92.27	79.14	92.08
0.18	35	FF	80.10	86.79	93.8	85.46	92.89	77.66	92.66
0.18	40	FF	79.35	86.83	94.4	84.90	93.26	76.70	92.99
0.18	50	FF	77.83	86.80	95.4	83.76	93.95	74.74	93.60

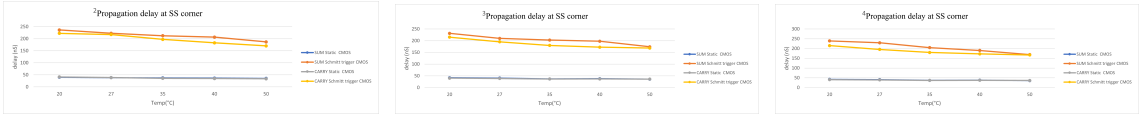
Table 12 demonstrates the noise margin of a Full Adder using the Schmitt trigger CMOS XOR gate. Dimensions are set at VM=Vdd/2 at the 'TT' corner and 27°C. In the XOR gate, all transistors of the pull-up network have W=0.7U and L=0.2U, While all transistors of the pull-down network have W=0.1U and L=0.2U. In the ST CMOS NAND gate, the pull-up network has w=0.45u, l=0.2u, pull-down network has 1=0.1U, L=0.2U. Inverter has w=0.1U, and L=0.2U for all transistors. The noise margin is the same for both sum and carry.

Table 12: Noise margins of full adder implementation using Schmitt trigger XOR gate

Supply Voltage	temp	corner	XNOR gate(mV)		XOR gate(mV)		Full adder(mV)		
(V)	$°C$		NM_H	NM_L	NM_H	NM_L	VM	NM_H	NM_L
0.18	20	SS	84.82	80.14	92.00	87.52	87.6	92.04	87.62
0.18	27	SS	84.43	79.77	91.88	87.57	87.7	91.93	87.69
0.18	35	SS	83.97	79.33	91.73	87.63	87.8	91.80	87.78
0.18	40	SS	83.67	79.03	91.62	87.66	87.9	91.70	87.85
0.18	50	SS	83.02	78.42	91.42	87.72	88	91.51	87.97
0.18	20	SF	67.75	96.82	75.96	103.36	103.9	75.97	103.82
0.18	27	SF	67	96.79	75.58	103.61	104.3	75.59	104.16
0.18	35	SF	66.12	96.72	75.13	103.87	104.7	75.14	104.57
0.18	40	SF	65.53	96.69	74.84	104.04	105	75.85	104.82
0.18	50	SF	64.3	96.60	74.23	104.32	105.6	74.25	105.35
0.18	20	TT	83.36	82.67	89.67	89.86	90	89.71	89.98
0.18	27	TT	81.96	82.31	89.56	89.90	90	89.6	90.05
0.18	35	TT	81.52	81.84	89.42	89.95	90.1	89.47	90.14
0.18	40	TT	81.21	81.56	89.32	89.98	90.2	89.38	90.21
0.18	50	TT	80.54	80.96	89.12	99.03	90.4	89.12	90.33
0.18	20	FS	96.29	68.51	102.43	76.43	76.5	102.62	76.46
0.18	27	FS	96.21	67.82	102.51	76.24	76.3	102.73	76.27
0.18	35	FS	96.12	66.98	102.56	76.02	76.5	102.83	76.06
0.18	40	FS	96.02	66.46	102.60	75.87	75.9	102.9	75.93
0.18	50	FS	95.87	65.32	102.65	75.59	75.7	103.02	75.67
0.18	20	FF	80.29	84.73	87.71	91.81	92	87.74	91.96
0.18	27	FF	79.89	84.38	87.6	91.84	92.1	87.63	92.04
0.18	35	FF	79.41	83.94	87.46	91.89	92.2	87.50	92.12
0.18	40	FF	79.08	83.67	87.36	91.91	92.2	87.41	92.18
0.18	50	FF	78.39	83.08	87.16	91.95	92.4	87.22	92.31

3.2.2 Propagation delay of Topology2: Full Adder Implementation using Static CMOS vs Schmitt Trigger CMOS XOR gates:

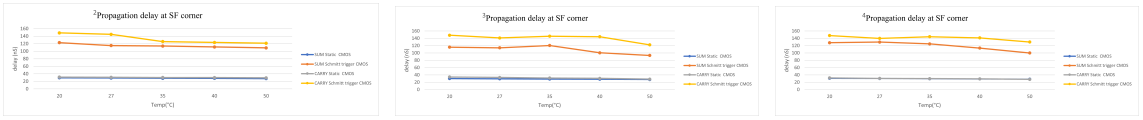
The [2] graphs illustrate where all three inputs change from 0 to 1 simultaneously. The [3] graphs depict when all three inputs change from 1 to 0 simultaneously. And, the graphs [4] illustrate the case where 2 inputs change together and 3rd input remains different. The propagation delay of static CMOS XOR FA is consistently lower than that of Schmitt trigger CMOS XOR FA across all process corners and temperatures. The graphs in the figure 37a, 37b, and 37c at the SS corner demonstrate that the propagation delay for both sum and carry in the Static CMOS circuit are almost the same with the temperature rise. While the delay in Schmitt trigger CMOS is high but decreases with a temperature rise.



(a) (b) (c)

Figure 37: Propagation delay of FA at SS corner (a) $_2SS$; $(b)_3SS$; $(c)_4SS$.

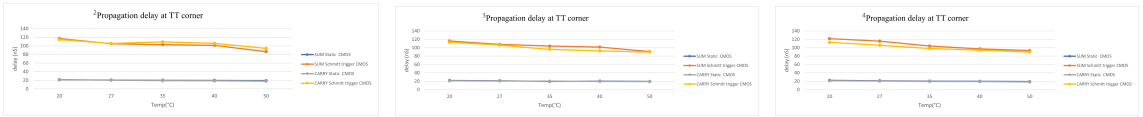
The graphs in the figure 38a at the SF corner demonstrate a decrease in the propagation delay for both sum and carry in the Schmitt trigger CMOS circuit as temperature rises from 20°C to 35°C However, from 35°C to 50°C, the delay remains constant. In contrast, figure 38b and 38c show the reverse trend, with almost consistent delay from 20°C to 35°C, and then decrease with rise in temperature from 35°C to 50°C.



(a) (b) (c)

Figure 38: Propagation delay of FA at SF corner (a) $_2SF$; $(b)_3SF$; $(c)_4SF$.

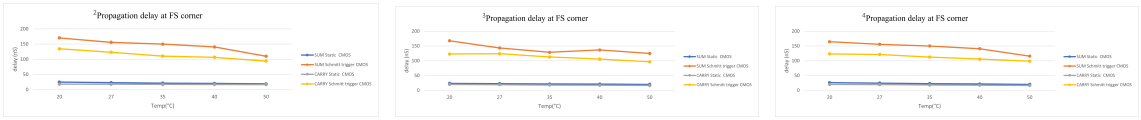
The graphs in the figure 39a at the TT corner illustrate the declining trend in the propagation delay for both sum and carry in the Schmitt trigger CMOS circuit as temperature rises from 20°C to 27°C and 40°C to 50°C, with the delay remains constant between 27°C to 40°C. The graph 39b and 39c show the decrease in delay as the rise in temperature.



(a) (b) (c)

Figure 39: Propagation delay of FA at TT corner (a) $_2TT$; $(b)_3TT$; $(c)_4TT$.

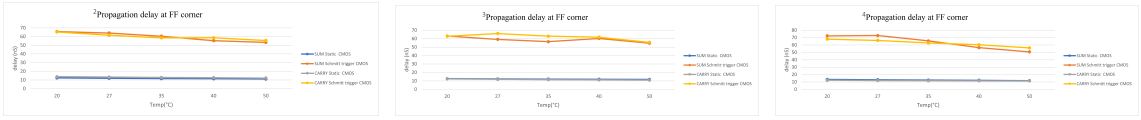
The graphs in the figure 40a, 40b and 40c at the FS corner illustrate significant difference between delay of sum and carry, and also showing the decreasing trend in the propagation delay for both sum and carry in the Schmitt trigger CMOS circuit as temperature increases.



(a) (b) (c)

Figure 40: Propagation delay of FA at FS corner (a) ${}_2FS; (b)_3FS; (c)_4FS$.

The graphs in the figure 41a, 41b and 41c at the FF corner illustrate the decreasing trend in the propagation delay for both sum and carry in the Schmitt trigger CMOS circuit as temperature increases.



(a) (b) (c)

Figure 41: Propagation delay of FA at FF corner (a) ${}_2FF; (b)_3FF; (c)_4FF$.

Table 13 is about the results of static CMOS XOR-based FA which demonstrates the propagation delay across various combinations of input, including simultaneous transitions of all three inputs from 0 to 1, all three from 1 to 0, and two inputs change together while 3rd is different. These results are measured across various corners and temperatures. Propagation delay for both sum and carry decreases with an increase in temperature.

Table 13: Propagation delay of full Adder implementation using static CMOS XOR gate

Supply	temp	corner	[2]Propagation delay		[3]Propagation delay		[4]Propagation delay	
$voltage(V)$	$°C$		$Sum(nS)$	$Carry(nS)$	$Sum(nS)$	$Carry(nS)$	$Sum(nS)$	$Carry(nS)$
0.18	20	SS	39.92	41.01	42.02	40.35	41.99	40.69
0.18	27	SS	38.23	38.60	40.64	38.89	40.60	39.26
0.18	35	SS	37.29	35.47	37.01	36.64	36.97	36.87
0.18	40	SS	36.45	34.83	38.06	37.08	38.01	37.28
0.18	50	SS	35.07	33.74	35.82	36.10	35.77	36.28
0.18	20	SF	29.45	31.28	30.12	34.37	30.94	31.9
0.18	27	SF	28.91	30.77	29.47	33.09	30.25	30.54
0.18	35	SF	28.32	30.24	28.77	31.64	29.61	29.95
0.18	40	SF	28.01	29.92	28.34	30.69	29.19	29.22
0.18	50	SF	27.41	29.28	27.54	28.58	28.43	27.95
0.18	20	TT	21.12	21.74	21.76	21.01	22.06	21.14
0.18	27	TT	20.54	20.27	21.19	20.47	21.14	20.36
0.18	35	TT	19.95	19.28	19.51	20.12	20.26	19.58
0.18	40	TT	19.64	18.80	20.19	19.63	19.81	19.16
0.18	50	TT	19.11	18.01	19.41	19.09	19.09	18.42
0.18	20	FS	24.72	18.19	23.69	20.04	25.99	20.19
0.18	27	FS	23.01	17.64	22.71	19.11	24.51	19.32
0.18	35	FS	21.36	17.18	21.73	17.89	22.71	18.19
0.18	40	FS	20.39	16.95	21.18	17.23	21.62	17.41
0.18	50	FS	18.98	16.57	20.15	16.45	19.98	16.55
0.18	20	FF	12.40	13.72	12.63	12.40	13.39	12.34
0.18	27	FF	11.98	13.28	12.38	11.89	13.00	11.88
0.18	35	FF	11.61	12.80	12.12	11.47	12.54	11.64
0.18	40	FF	11.43	12.55	11.97	11.27	12.26	11.57
0.18	50	FF	11.14	12.11	11.70	10.97	11.72	11.39

[2]When all 3 inputs change together(0 to 1).[3]When all 3 inputs change together(1 to 0).
[4]When 2 inputs change together and 3rd is different.

Table 14 details the propagation delay of Schmitt trigger CMOS XOR based FA, demonstrates the delay across various combinations of input. This includes simultaneous transitions of all three inputs from 0 to 1, all three from 1 to 0, and two inputs change together while the third is different. These results are measured at various corners and temperatures, indicating the decrease in delay for both sum and carry with the increase in temperature.

Table 14: Propagation delay of full adder implementation using Schmitt trigger CMOS XOR gate

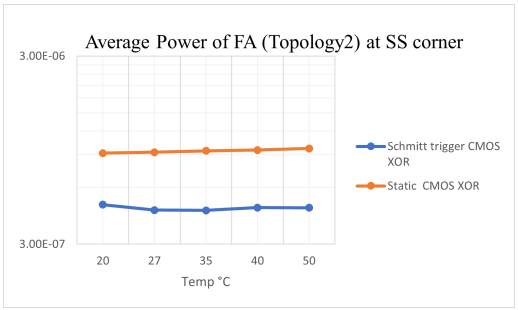
Supply	temp	corner	[2]Propagation delay		[3]Propagation delay		[4]Propagation delay	
$voltage(V)$	$°C$		$Sum(nS)$	$carry(nS)$	$Sum(nS)$	$carry(nS)$	$Sum(nS)$	$carry(nS)$
0.18	20	SS	236.24	222.33	282.51	224.08	239.17	214.99
0.18	27	SS	222.51	217.23	247.64	197.77	229.31	195.49
0.18	35	SS	212.44	197.33	234.71	180.14	204.76	179.96
0.18	40	SS	206.51	182.82	224.81	182.01	190.08	172.61
0.18	50	SS	186.78	170.29	215.97	168.66	169.07	166.92
0.18	20	SF	122.90	148.80	135.8	142.26	127.94	147.64
0.18	27	SF	115.19	144.89	132.16	140.62	129.79	139.79
0.18	35	SF	113.97	125.77	127.14	134.57	124.86	144.46
0.18	40	SF	111.42	123.34	124.06	134.34	113.38	141.16
0.18	50	SF	108.93	121.22	118.06	129.38	100.03	129.97
0.18	20	TT	117.15	114.65	138.71	106.75	121.68	112.95
0.18	27	TT	105.08	105.65	133.23	111.65	115.69	106.03
0.18	35	TT	102.95	109.15	128.21	103.33	104.15	98.07
0.18	40	TT	101.42	105.76	124.99	98.2	97.32	94.12
0.18	50	TT	86.54	94.24	112.15	91.94	93.25	89.89
0.18	20	FS	170.44	134.37	198.02	131.86	164.37	123.23
0.18	27	FS	155.72	123.20	179.95	119.44	155.77	121.46
0.18	35	FS	149.90	110.33	166.56	111.49	149.98	112.55
0.18	40	FS	140.59	106.48	154.68	107.71	140.78	105.69
0.18	50	FS	109.96	94.04	143.77	98.37	115.65	98.64
0.18	20	FF	65.77	65.31	79.71	66.85	72.37	68.00
0.18	27	FF	64.08	61.58	72.36	62.09	72.80	66.19
0.18	35	FF	60.38	58.51	68.57	58.21	65.60	62.75
0.18	40	FF	55.31	58.58	67.02	56.3	56.45	60.37
0.18	50	FF	53.27	55.48	63.67	58.42	50.72	56.17

[2]When all 3 inputs change together(0 to 1).[3]When all 3 inputs change together(1 to 0).
[4]When 2 inputs change together and 3rd is different.

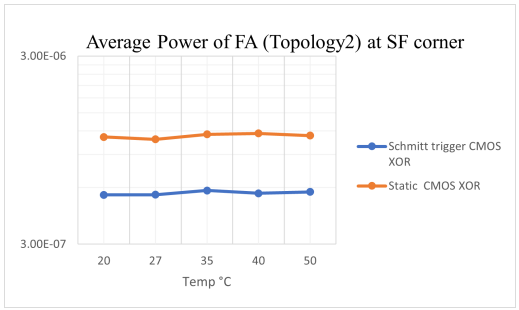
3.2.3 Average Power of Topology2: Full Adder Implementation using Static CMOS vs Schmitt Trigger CMOS XOR gates:

The detailed numbers of average Power for static CMOS are in the table 15 while for Schmitt triggers CMOS is in the table 16. The average power rises with a rise in temperature for both static CMOS and Schmitt trigger CMOS for all process corners only some exceptions.

Figure 42a at the SS corner elaborates for Schmitt Trigger CMOS the average power increases with the temperature rise, decreases slightly at 27°C, and then resumes its little increase at 35°C. Figure 42b at the SF corner indicates for Schmitt Trigger CMOS the average power increases with the temperature rise, decreases slightly at 40°C, and then resumes its increase at 50°C.



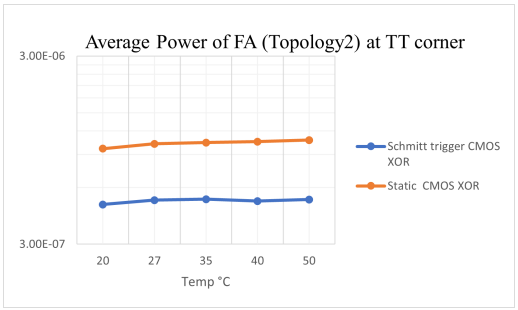
(a)



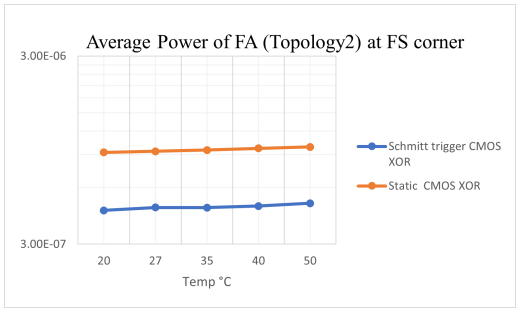
(b)

Figure 42: (a) Average Power of the Full Adder (Typology2) at 0.18v and SS corner; (b) Average Power of the Full Adder (Typology2) at 0.18v and SF corner.

Figure 43a at the TT corner indicates that the average power increases with the temperature rise for Schmitt Trigger CMOS, decreases slightly at 40°C, and then resumes its little increase at 50°C. Figure 43b at the FS corner shows the rise in average power with temperature rise for both cases.



(a)



(b)

Figure 43: (a) fig: Average Power of the Full Adder (Typology2) at 0.18v and TT corner; (b) fig: Average Power of the Full Adder (Typology2) at 0.18v and FS corner.

Figure 44 at the FF corner shows that the Schmitt Trigger CMOS average power increases with the temperature rise from 27°C, and shows the same at 20°C and 27°C.

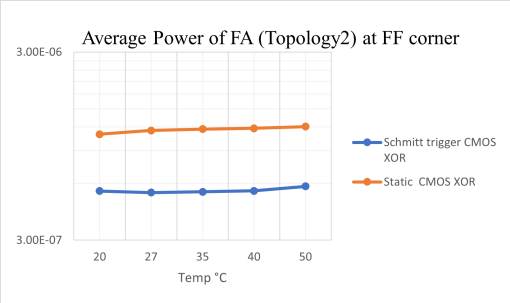


Figure 44: Average Power of the Full Adder (Typology2) at 0.18v and FF corner.

Table 15 provides details about the average current, average power, and PDP of full adder implementation using static CMOS XOR. When looking at the average power for different corners at the same temperature, SS has the lowest average power, followed by FS, TT, FF, and SF has the highest average power among them. The (power delay product) PDP follows the high to low order, SS, SF, FS, TT, and FF.

Table 15: Average power of full adder implementation using static CMOS XOR gate

Voltage (V)	Temp °C	corner	Average Current(nA)	Average Power(nW)	Pro. delay(nS)	PDP(aJ)
0.18	20	SS	5079	914	41.99	38378
0.18	27	SS	5149	926	40.6	37595
0.18	35	SS	5228	941	36.97	34788
0.18	40	SS	5278	950	38.01	36109
0.18	50	SS	5379	968	35.77	34625
0.18	20	SF	6204	1116	30.94	34529
0.18	27	SF	6020	1083	30.25	32760
0.18	35	SF	6403	1152	29.61	34110
0.18	40	SF	6469	1164	29.19	33977
0.18	50	SF	6310	1135	28.43	32268
0.18	20	TT	5370	966	22.06	21309
0.18	27	TT	5700	1026	21.14	21689
0.18	35	TT	5793	1042	20.26	21110
0.18	40	TT	5851	1053	19.81	20859
0.18	50	TT	5967	1074	19.09	20502
0.18	20	FS	5129	923	25.99	23988
0.18	27	FS	5200	936	24.51	22941
0.18	35	FS	5281	950	22.71	21574
0.18	40	FS	5389	970	21.62	20971
0.18	50	FS	5491	988	19.98	19740
0.18	20	FF	6109	1099	13.39	14715
0.18	27	FF	6388	1149	13	14937
0.18	35	FF	6496	1169	12.54	14659
0.18	40	FF	6563	1181	12.26	14479
0.18	50	FF	6697	1205	11.72	14122

Table 16 elaborates the average current, average power, and PDP of full adder implementation using Schmitt trigger CMOS XOR at different corners and different temperatures. As the temperature rises, there is a consistent increase in average current and average power across all corners. Furthermore, comparing the average power for different corners at the same temperature, SS has the lowest average power, followed by FS, TT, FF, and SF has the highest average power among them. The (power delay product) PDP follows the high to low order, SS, FS, SF, TT, and FF.

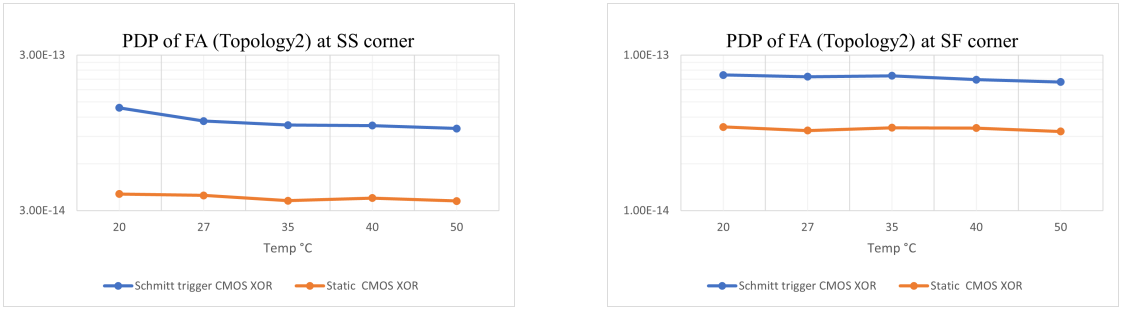
Table 16: Average power of full adder based on Schmitt trigger CMOS XOR gate

Voltage (V)	temp °C	corner	Average Current (nA)	Average Power (nW)	Pro. delay (nS)	PDP(aJ)
0.18	20	SS	2706	487	282.51	137582
0.18	27	SS	2535	456	247.64	112923
0.18	35	SS	2524	454	234.71	106558
0.18	40	SS	2614	470	224.81	105660
0.18	50	SS	2610	469	215.97	101289
0.18	20	SF	3053	549	135.8	74554
0.18	27	SF	3055	550	132.16	72688
0.18	35	SF	3220	579	127.14	73614
0.18	40	SF	3115	560	124.06	69473
0.18	50	SF	3161	569	118.06	67176
0.18	20	TT	2712	488	138.71	67690
0.18	27	TT	2863	515	133.23	68613
0.18	35	TT	2895	521	128.21	66797
0.18	40	TT	2831	509	124.99	63619
0.18	50	TT	2884	519	112.15	58205
0.18	20	FS	2524	454	198.02	89901
0.18	27	FS	2621	471	179.95	84756
0.18	35	FS	2611	470	166.56	78283
0.18	40	FS	2666	479	154.68	74091
0.18	50	FS	2755	495	143.77	71166
0.18	20	FF	3049	548	79.71	43681
0.18	27	FF	2993	538	72.36	38929
0.18	35	FF	3016	543	68.57	37233
0.18	40	FF	3055	549	67.02	36793
0.18	50	FF	3226	580	63.67	36928

3.2.4 PDP of Topology2: Full Adder Implementation using Static CMOS vs Schmitt Trigger CMOS XOR:

The detailed values of PDP for static CMOS are in the table 15 while for Schmitt triggers CMOS is in the table 16.

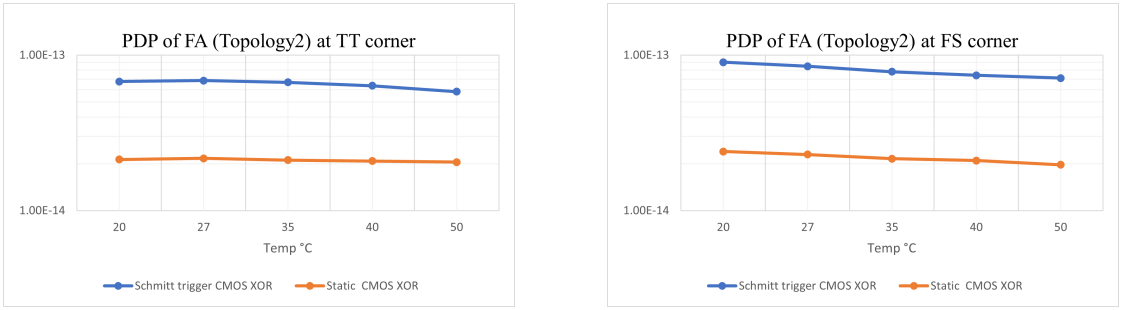
The graphs in the figure 45a at the SS corner indicate PDP for Schmitt Trigger CMOS decreases with the temperature rise from 20°C to 27°C, then it shows almost constant. Static CMOS shows almost the same values except 35°C where a small dip notices. The graph 45b SF corner demonstrates the almost same value from 20°C to 40°C and then a small decrease at 50°C.



(a) (b)

Figure 45: (a) fig: PDP of the Full Adder (Typology2) at 0.18v and SS corner; (b) fig: PDP of the Full Adder (Typology2) at 0.18v and SF corner.

The graphs in the figure 46a at the TT corner indicate PDP for Schmitt Trigger CMOS a small decrease with the temperature rise. The graphs in the figure 46b FS corner demonstrates the PDP decrease with the temperature rise for both cases.



(a) (b)

Figure 46: (a) fig: PDP of the Full Adder (Typology2) at 0.18v and TT corner; (b) fig: PDP of the Full Adder (Typology2) at 0.18v and FS corner.

The graph in the figure 46a at the TT corner indicates PDP decrease with the temperature rise, from 20°C to 40°C and then a small increase at 50°C.

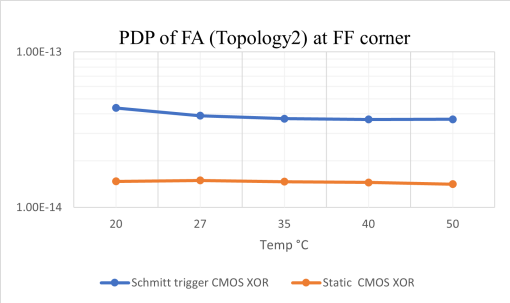


Figure 47: PDP of the Full Adder (Typology2) at 0.18v and FF corner.

3.2.5 ARCHITECTURES of Topology2: Full Adder Implementation using Static CMOS vs Schmitt Trigger CMOS XOR gates::

The static CMOS XOR full adder, incorporating 36 transistors, comprises sum and carry. The sum is designed by using 2 XOR(each XOR consists of 12 transistors) and the carry uses 3 NAND(each NAND consists of 4 transistors). The Schmitt Trigger CMOS XOR full adder, incorporating 90 transistors, comprises sum and carry. The sum is designed by using 2 XOR(each XOR consists of 30 transistors) and the carry uses 3 NAND(each NAND consists of 10 transistors).

Table 17: Transistor count and driven nodes of Topology2.

	Number of transistor		Number of driven nodes	
	Static CMOS	**Schmitt trigger CMOS**	**Static CMOS**	**Schmitt trigger CMOS**
XOR	12	30	5+2	13+2
Sum	24	60	14	30
Carry	12	30	6	15
Total(FA)	36	90	20	45

3.3 Connectivity of Full Adders as Ring oscillator:

In this section, Results for four different ring oscillators are mentioned.

Table 18 in the appendix provides detailed results for the ring oscillator using static CMOS NAND gates for its full adder design. The table includes comprehensive data and analyses relevant to this configuration. A comprehensive set of results for the ring oscillator using full adder Schmitt Trigger CMOS NAND is included in the appendix under Table 20. The results for the Ring oscillator, which uses the static CMOS XOR for its full adders, can be found in Table 21 in the appendix. The detailed results of Ring (FA Schmitt trigger CMOS XOR) are mentioned in the appendix in table 23.

The initial condition is required to simulate the circuit, it is set to greater than Vdd/2. Some time got an error about GMIN, then changed the initial condition. However initial conditions for the ring (FA Schmitt triggers) are highly restrictive. The initial conditions of the ring (FA implementation using Schmitt trigger CMOS NAND gate) for all corners are available in the appendix table 19. The initial conditions of the ring (FA implementation using Schmitt trigger CMOS XOR gate) for all corners are available in the appendix table 22.

3.3.1 Ring oscillator: At the SS corner

The graphs in figure 48 illustrate the propagation delay at the SS corner in the ring oscillator. Delay decreases with the rise in voltage. Schmitt trigger CMOS shows more delay than Static CMOS. Ring oscillator (Schmitt trigger CMOS NAND) experiences the highest delay while Ring oscillator (static CMOS XOR) demonstrates the lowest delay.

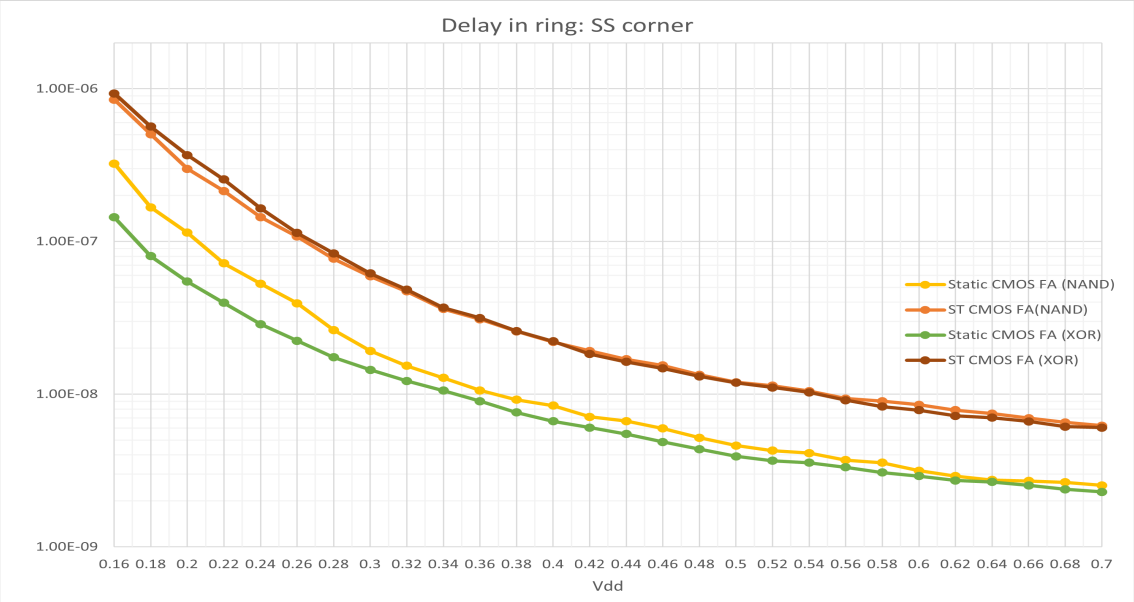


Figure 48: Delay in Ring oscillator: SS corner

The graphs in figure 49 SS corner illustrates the average power in the ring oscillator. Schmitt triggers CMOS full adder for both topologies show less average power consumption.

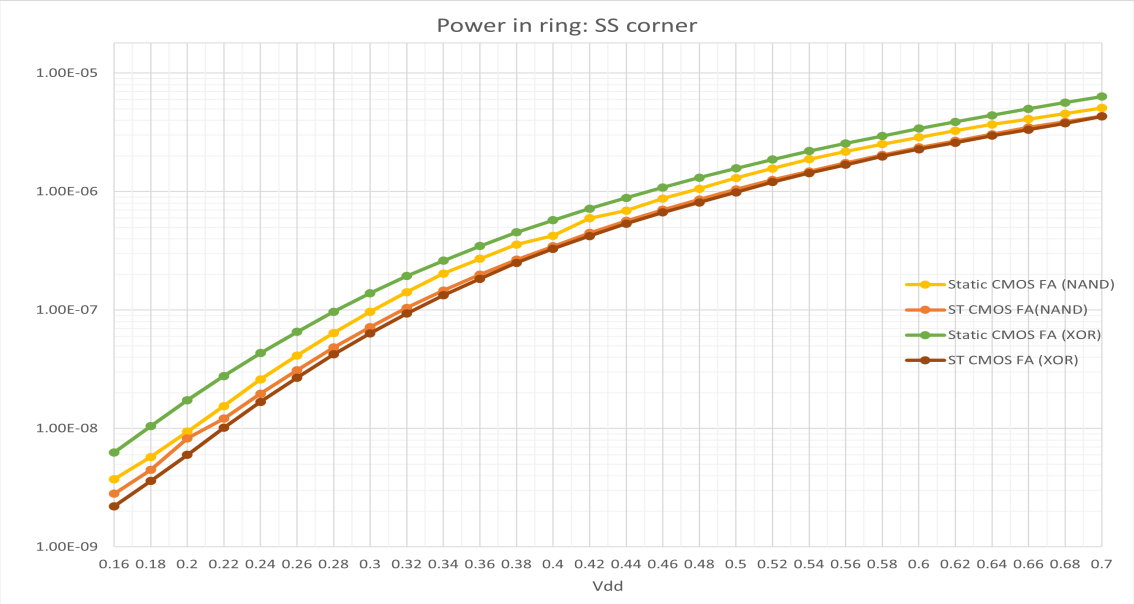


Figure 49: Power in Ring oscillator: SS corner

The graphs in the figure 50 illustrate the PDP in the ring oscillator at the SS corner, static CMOS full adders for both cases show lower PDP than the Schmitt trigger FAs. The static CMOS XOR has the smallest PDP for most Vdd, except at 0.36V, and 0.68V, where it's equal to the static CMOS NAND.

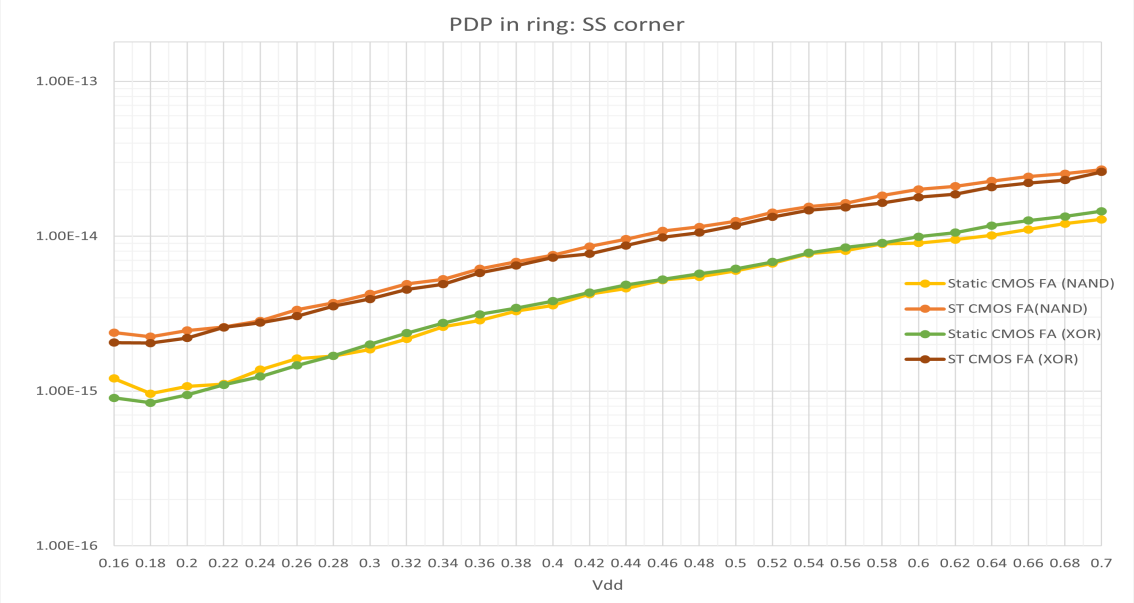


Figure 50: PDP in Ring oscillator: SS corner

Figure 51 demonstrates the EDP in the ring oscillator at the SS corner, FA using Schmitt trigger CMOS XOR gate has higher EDP till 0.4V after it is equal to the static CMOS NAND. While static CMOS XOR has the smallest EDP.

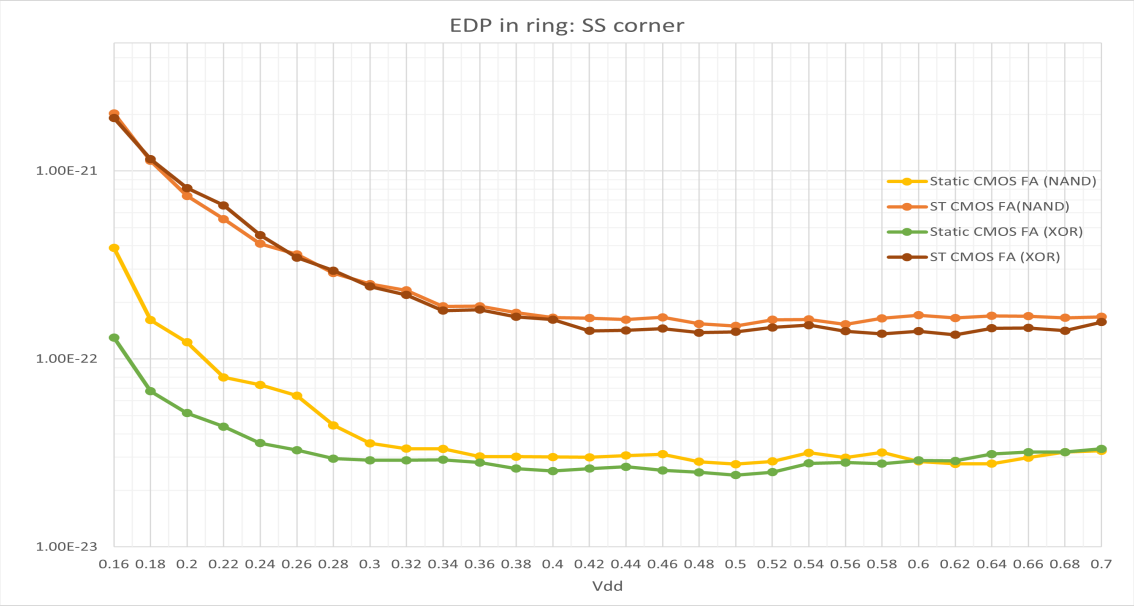


Figure 51: EDP in Ring oscillator: SS corner

3.3.2 Ring oscillator: At the SF corner

Figure 52 illustrates the propagation delay at the SF corner in the ring oscillator. Schmitt trigger CMOS shows more delay than static CMOS. There is a reduction in delay as the voltage increases. Schmitt trigger CMOS shows more delay compared to Static CMOS. Ring oscillator (Schmitt trigger CMOS XOR) shows the longest delay while Ring oscillator (static CMOS XOR) exhibits the shortest delay.

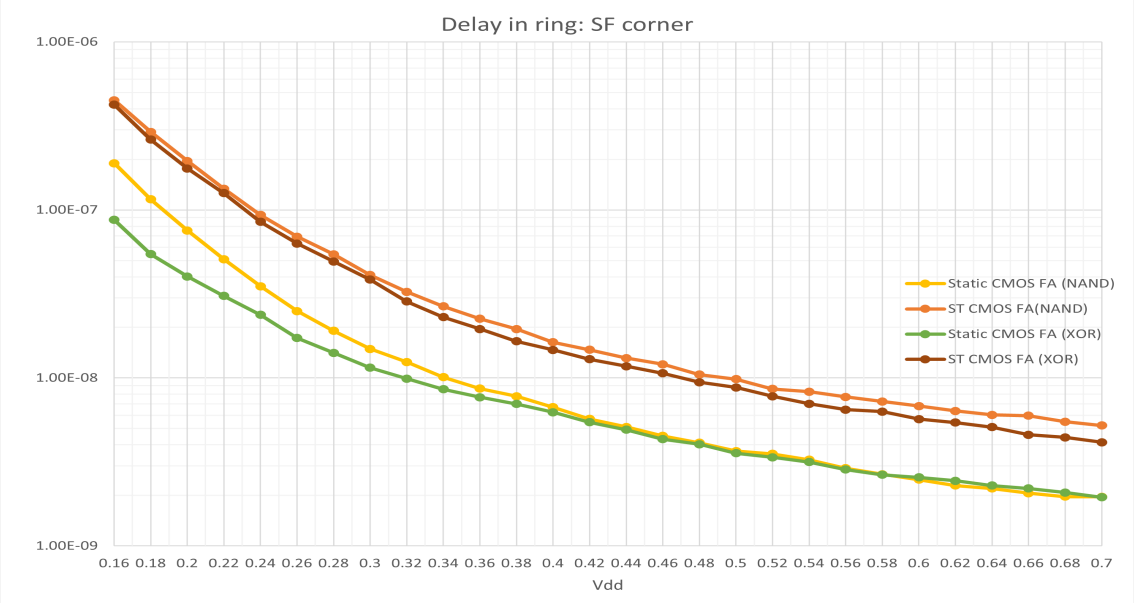


Figure 52: Delay in Ring oscillator: SF corner

Figure 53 illustrates the average power in the ring oscillator at the SF corner. FAs (Schmitt trigger CMOS) show less power than FAs(static CMOS). Schmitt trigger CMOS XOR gate shows less power than the Schmitt trigger CMOS NAND gate at 0.18V, 0.2V, and 0.22V after that both have similar average power.

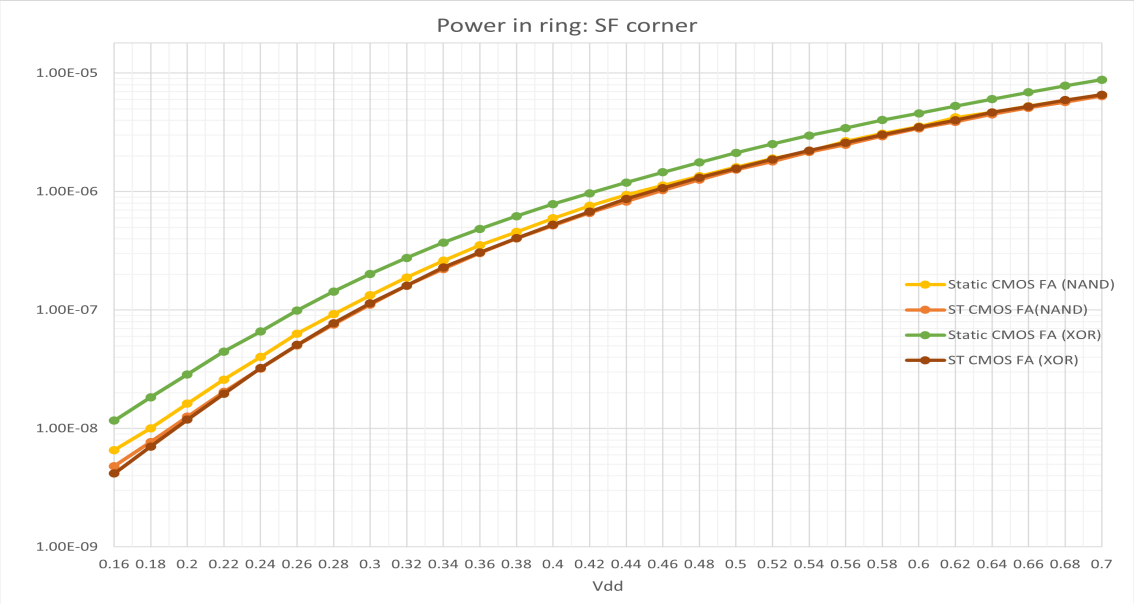


Figure 53: Power in Ring oscillator: SF corner

Figure 54 elaborates the PDP at the SF corner in the ring oscillator, static CMOS full adder for both cases shows less PDP while both Schmitt triggers FA have higher PDP.

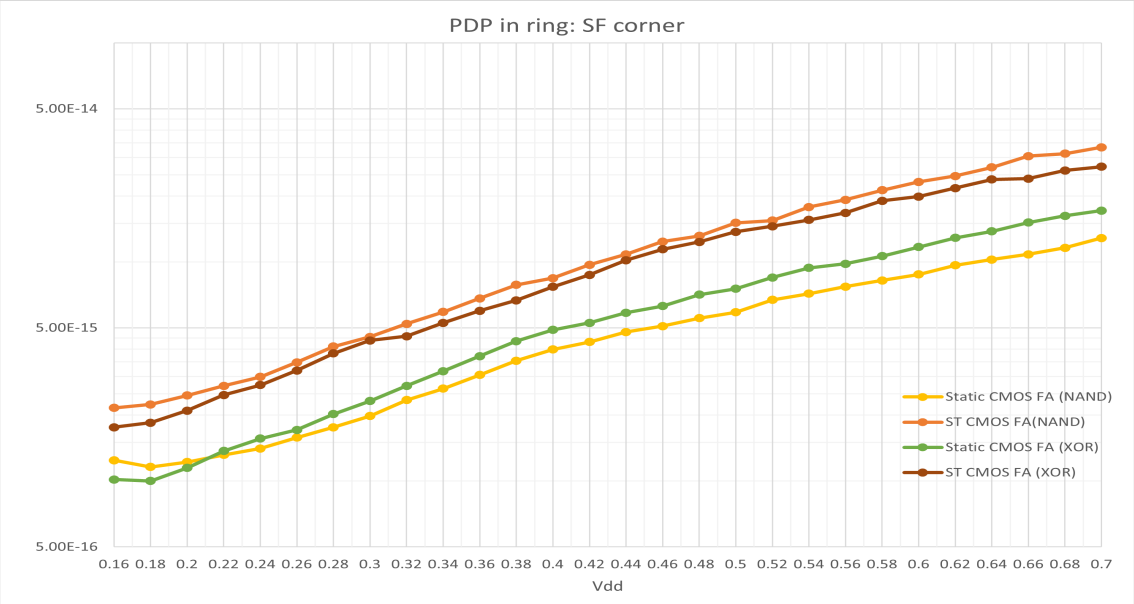


Figure 54: PDP in Ring oscillator: SF corner

Figure 55 demonstrates the EDP at the SF corner in the ring oscillator, Schmitt triggers CMOS XOR had higher EDP than Schmitt triggers CMOS NAND till 0.3V after the trend is reversed.

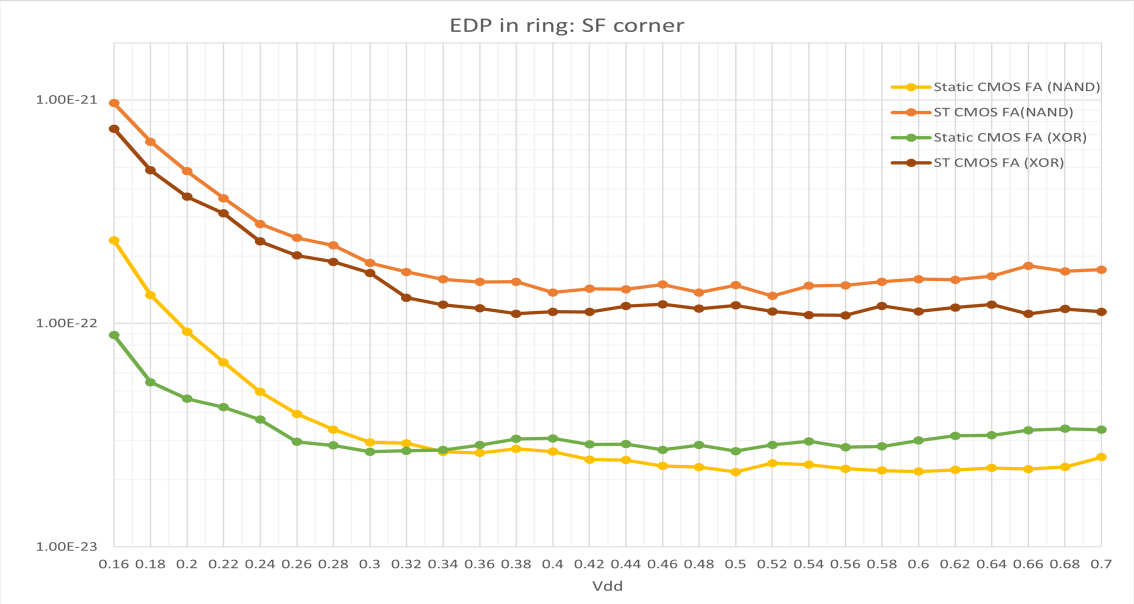


Figure 55: EDP in Ring oscillator: SF corner

3.3.3 Ring oscillator: At the TT corner

Figure 56 displays the propagation delay at the TT corner in the ring oscillator. There is a reduction in delay as the voltage increases. Both cases of Schmitt trigger CMOS show more delay compared to both cases of Static CMOS. Ring (Schmitt trigger CMOS XOR) shows the longest delay while Ring (static CMOS XOR) exhibits the shortest delay.

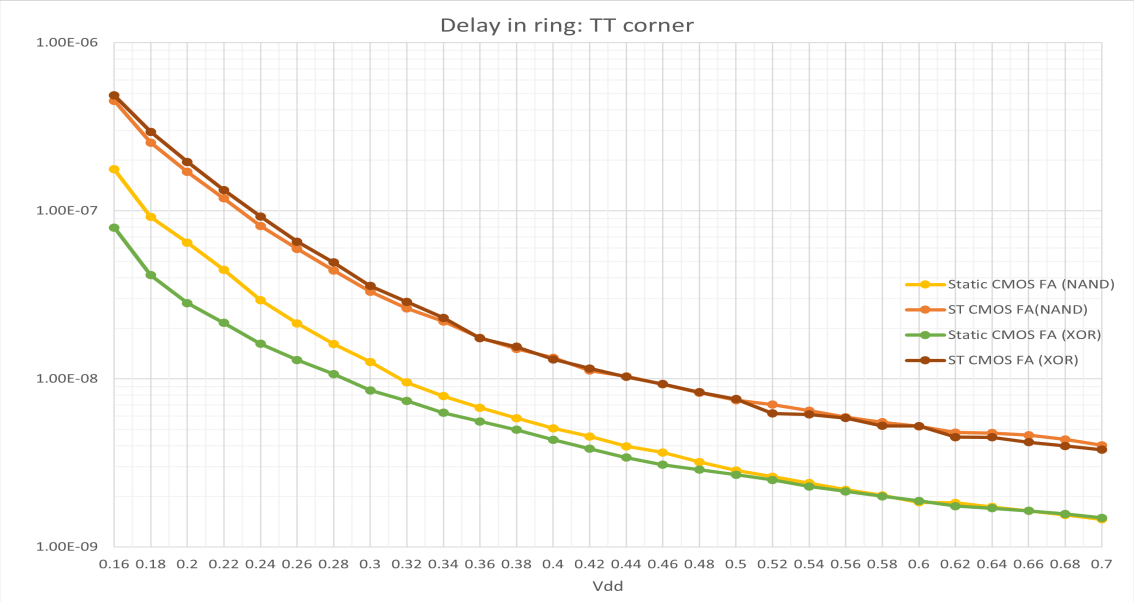


Figure 56: Delay in Ring oscillator: TT corner

The graph 57 illustrates the average power in the ring oscillator at the TT corner. Schmitt trigger CMOS XOR shows less power while static CMOS XOR shows higher average power.

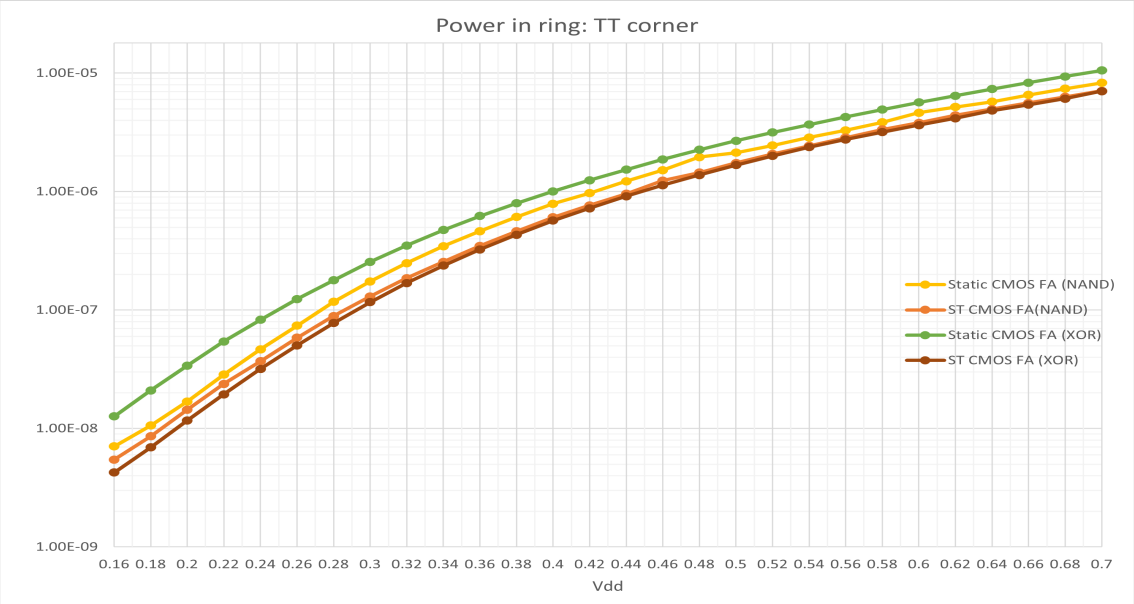


Figure 57: Power in Ring oscillator: TT corner

Figure 58 demonstrates the PDP in the ring oscillator at the TT corner, static CMOS full adder for both cases shows less PDP while both Schmitt triggers FA have higher PDP.

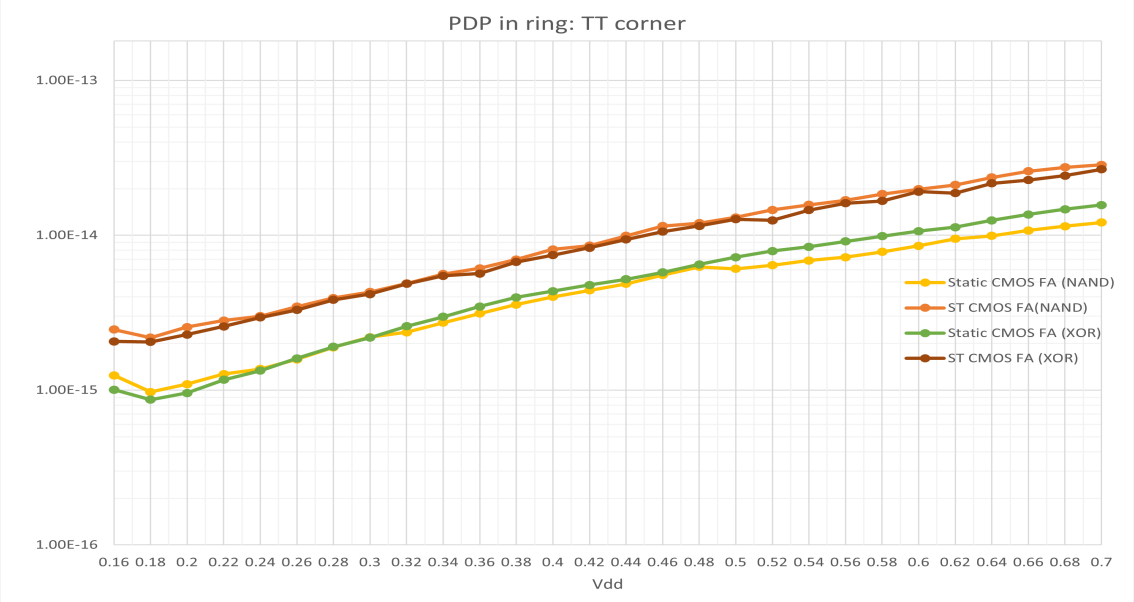


Figure 58: PDP in Ring oscillator: TT corner

Figure 59 demonstrates the EDP in the ring oscillator at the TT corner, Schmitt triggers CMOS XOR has higher EDP. While static CMOS XOR shows less EDP. EDP decreases with the increase in Vdd till 400mV. after it almost these are constant.

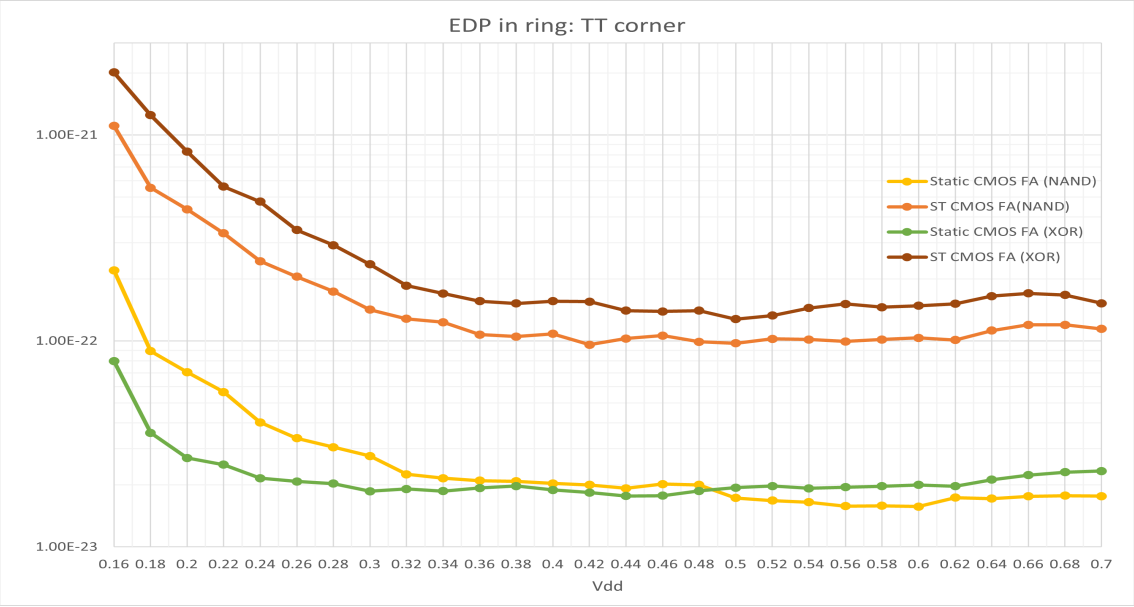


Figure 59: EDP in Ring oscillator: TT corner

3.3.4 Ring oscillator: At the FS corner

Figure 60 depicts the propagation delay at the FS corner in the ring oscillator. There is a decrease in delay as the voltage increases. The ring oscillator (Schmitt trigger CMOS XOR) shows the longest delay. The ring oscillator (static CMOS XOR) shows the lowest delay. From 0.5V to 0.7V, the ring oscillator (static CMOS XOR), and ring oscillator (static CMOS NAND) demonstrate almost equal propagation delay.

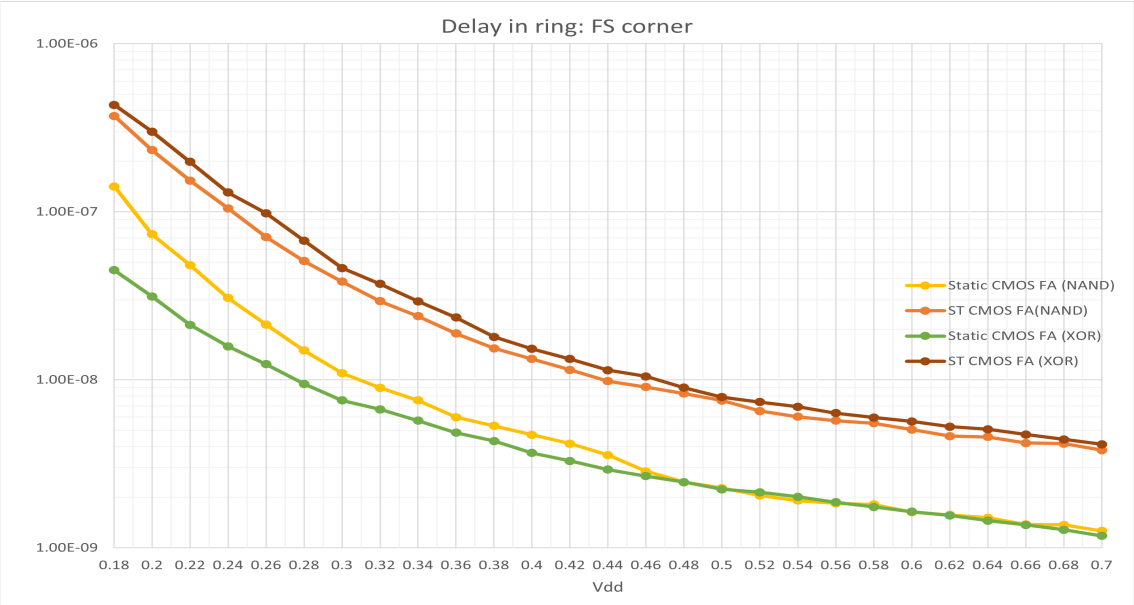


Figure 60: Delay in Ring oscillator: FS corner

Figure 61 represents the average power in the ring at the FS corner. Ring (Schmitt trigger CMOS XOR) shows less power. while Ring (Static CMOS XOR gate) shows higher power.

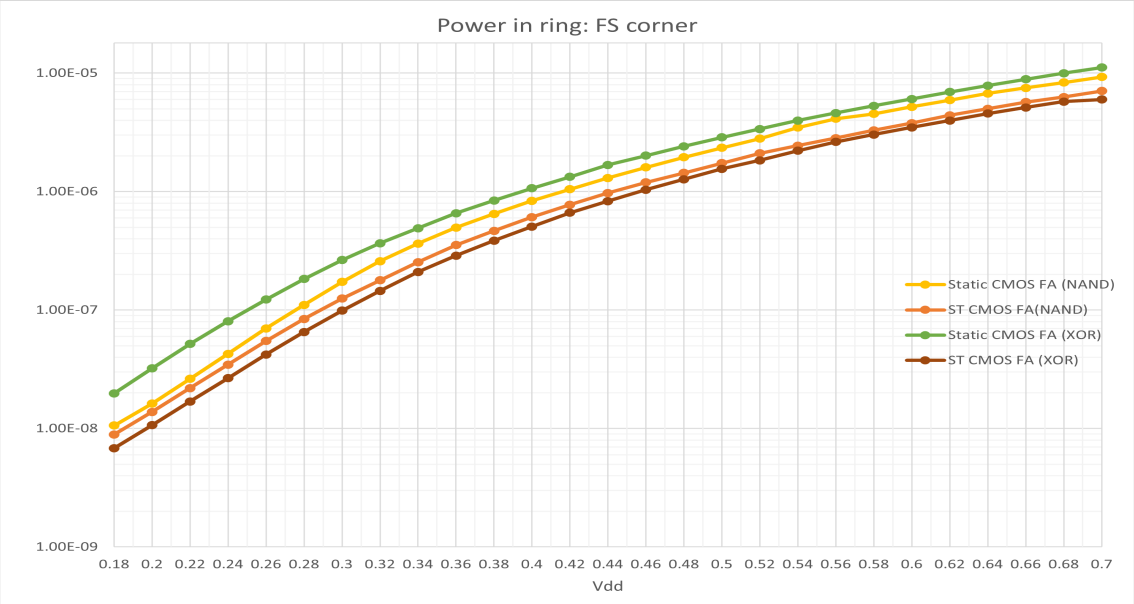


Figure 61: Power in Ring oscillator: FS corner

Figure 62 depicts the PDP in the ring oscillator at the FS corner, static CMOS full adder for both cases shows less PDP while both Schmitt triggers have higher PDP. Ring (Schmitt trigger XOR) shows higher PDP.

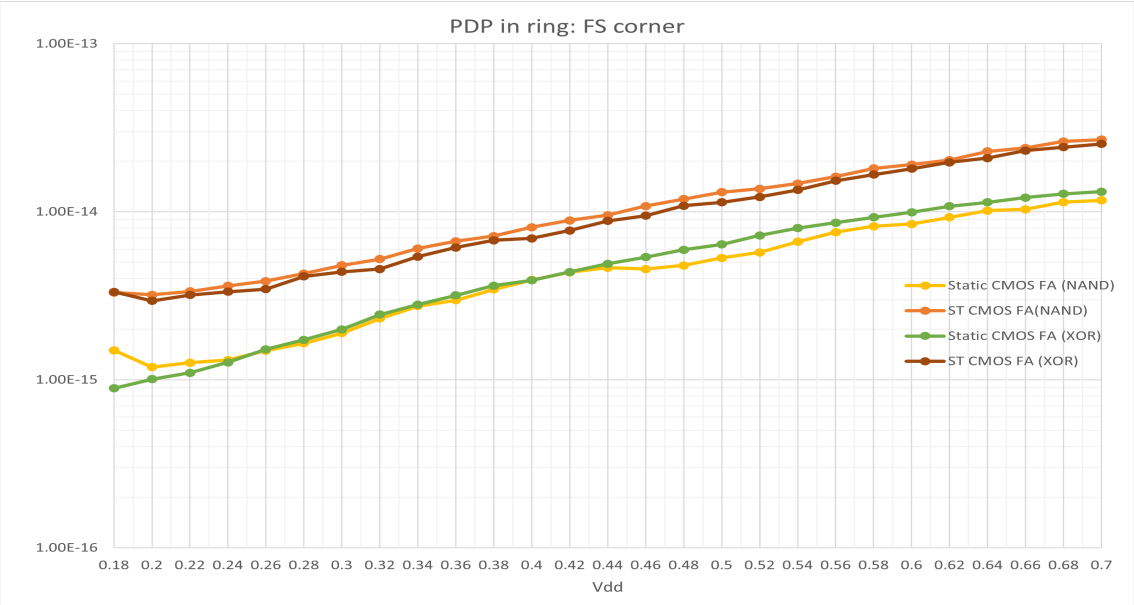


Figure 62: PDP in Ring oscillator: FS corner

Figure 63 highlights the EDP in the ring oscillator at the FS corner, Ring (Schmitt trigger CMOS XOR) has higher EDP. While Ring (static CMOS XOR) shows less EDP.

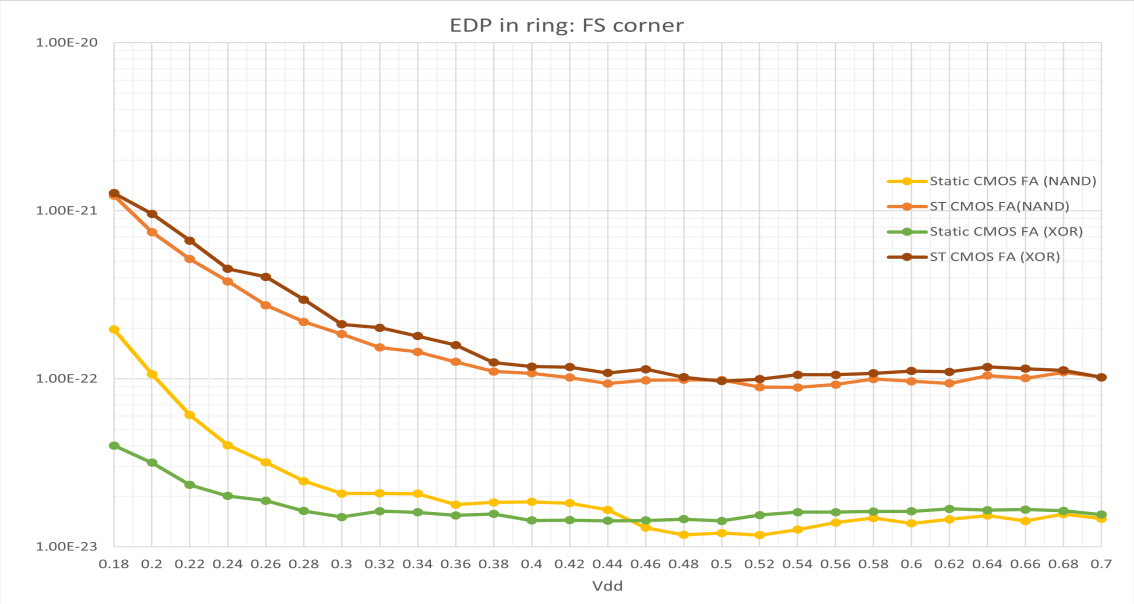


Figure 63: EDP in Ring oscillator: FS corner

3.3.5 Ring oscillator: At the FF corner

Figure 64 illustrates the propagation delay in the ring oscillator at the FF corner. The ring oscillator (Schmitt trigger CMOS XOR) shows the longest delay. Ring oscillator (static CMOS XOR), and ring oscillator (static CMOS NAND) demonstrate almost equal propagation delay From 0.54V to 0.7V.

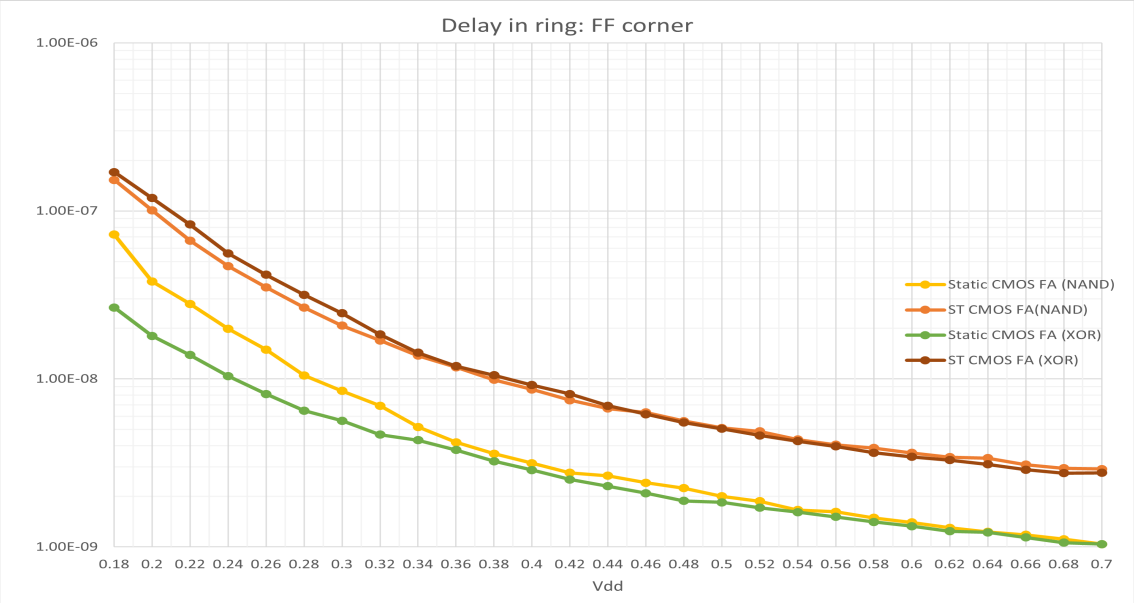


Figure 64: Delay in Ring oscillator: FF corner

Figure 65 reveals the average power in the ring oscillator at the FF corner. The ring oscillator (Schmitt trigger CMOS XOR) shows less power. The ring oscillator (Static CMOS XOR gate) shows less power.

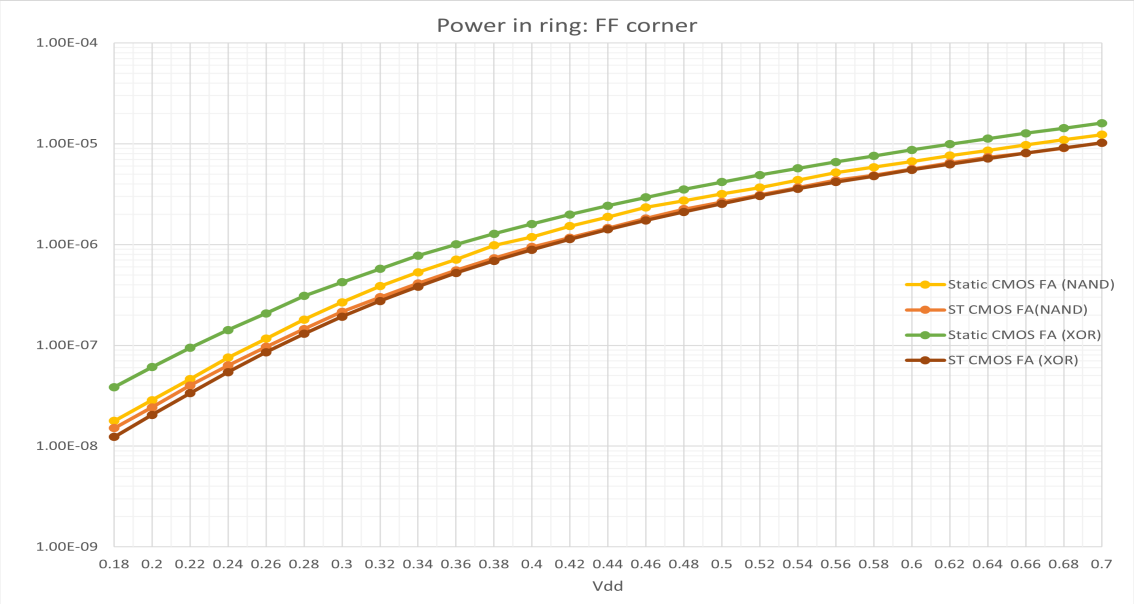


Figure 65: Power in Ring oscillator: FF corner

Figure 66 depicts the PDP in the ring at the FF corner, The ring oscillator (static CMOS) for both cases shows less PDP while both Schmitt triggers have higher PDP.

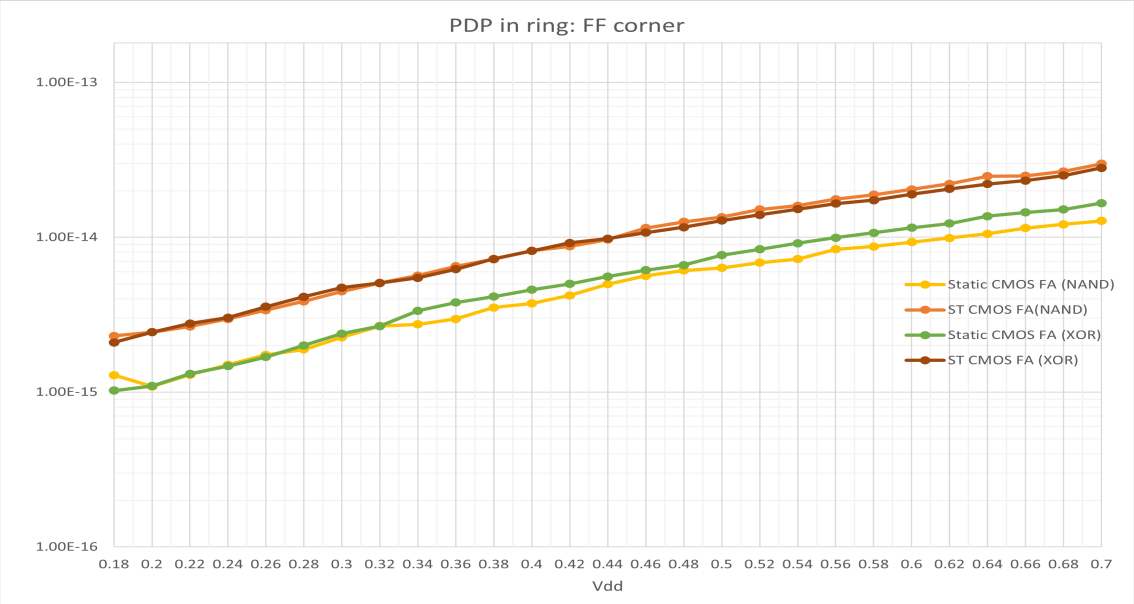


Figure 66: PDP in Ring oscillator: FF corner

Figure 67 demonstrates the EDP in the ring oscillator at the FF corner. Schmitt trigger CMOS XOR has higher EDP. While the static CMOS XOR shows less EDP.

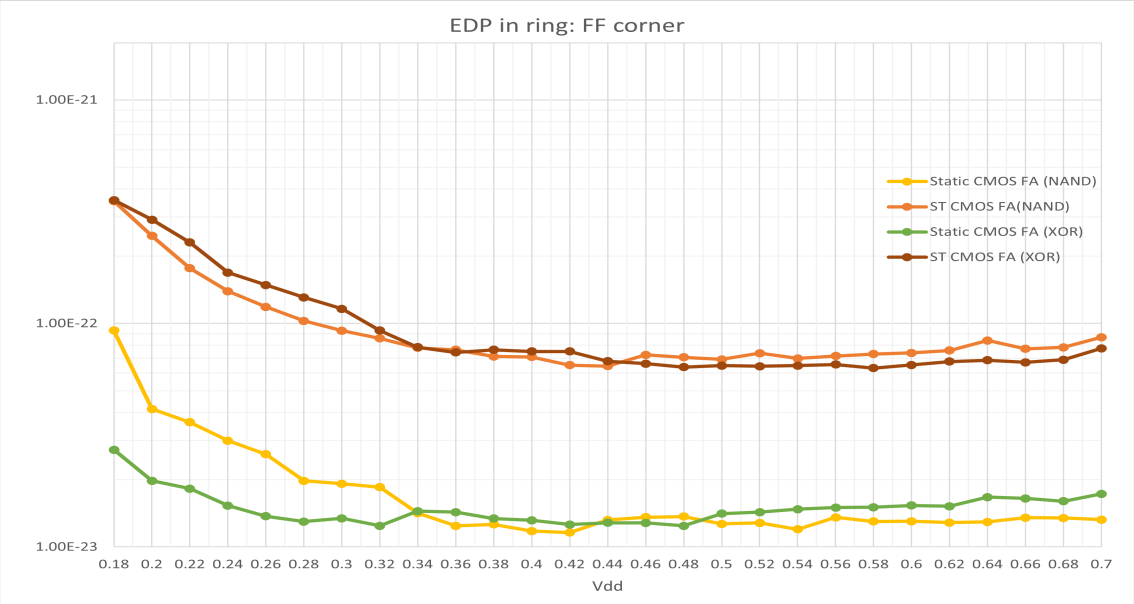


Figure 67: EDP in Ring oscillator: FF corner

3.4 4-bit Ripple Carry Adder:

In this section, results for four different 4-bit Ripple Carry adders are mentioned. Table 24 in the appendix provides detailed results for the 4-bit RCA using full adders(static CMOS NAND gates). The table includes comprehensive data and analyses relevant to this configuration.

A comprehensive set of results for the 4-bit RCA using Full Adder (Schmitt Trigger CMOS NAND) is included in the appendix under Table 25.

The comprehensive results for the 4-bit Ripple Carry Adder, which uses the full adders(static CMOS XOR), can be found in Table 26 in the appendix.

The detailed results of 4-bit RCA (FA Schmitt trigger CMOS XOR) are available in the appendix in table 27.

3.4.1 4-bit Ripple Carry Adder: SS corner

At the SS corner: The RCA using full adder(Schmitt Trigger CMOS NAND gate) encounters operational challenges at specific voltage levels: 0.18V, where the circuit fails to simulate, resulting in the GMIN error. Interestingly, a slight decrease in these voltages to 0.179V, allows the circuit to operate without any issues. While RCA using full adder(Schmitt Trigger CMOS XOR gate) also fails to simulate at specific voltage levels: 0.24V, and 0.50V, leading to a GMIN error. However, with a marginal increase in these voltages to 0.241V, and 0.501V respectively, the circuit functions correctly without any simulation issues.

Figure 68 demonstrates the propagation delay in RCA at the SS corner. The delay for Schmitt trigger CMOS is higher than static CMOS cases. static CMOS NAND has the lowest propagation delay.

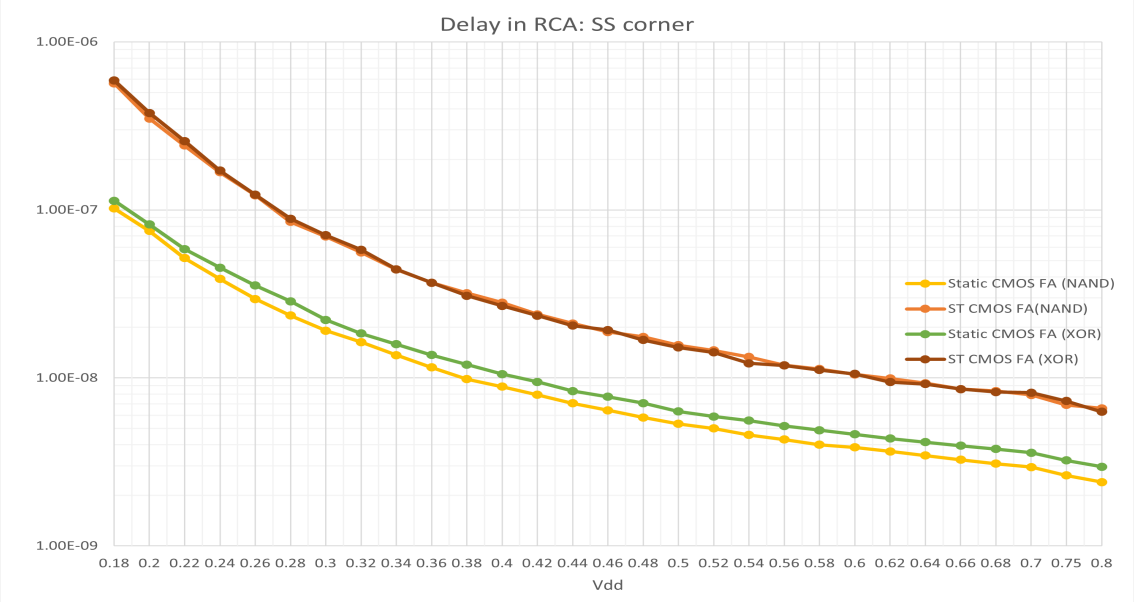


Figure 68: Delay in RCA at SS corner

Figure 69 demonstrates the average power in RCA at the SS corner. RCA (FA using on static CMOS XOR gate) shows more power While Schmitt triggers CMOS XOR has the lowest average power.

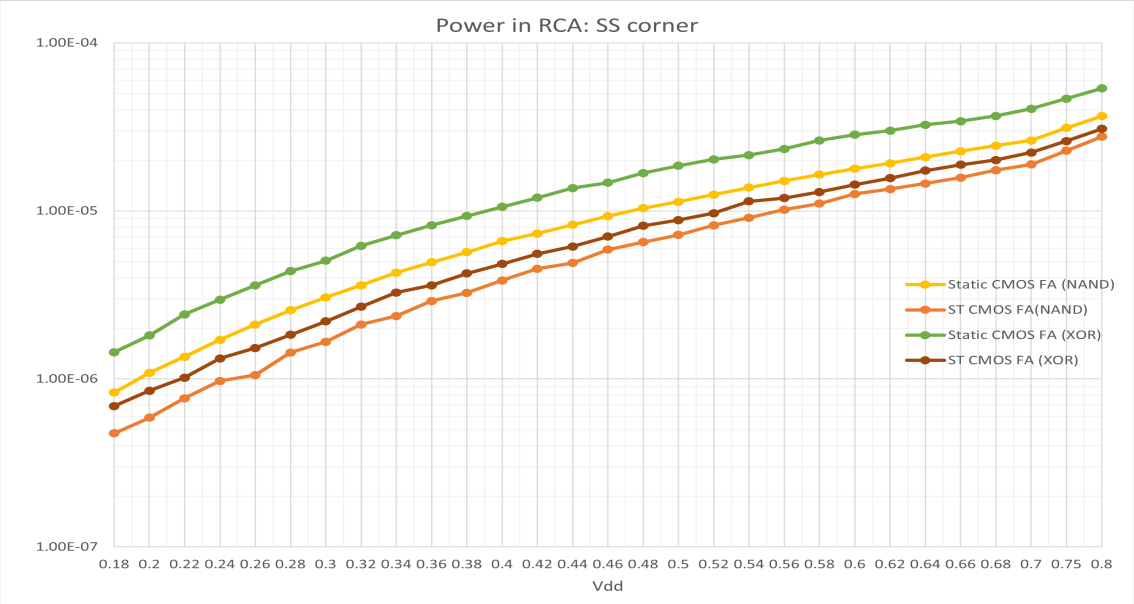


Figure 69: Power in RCA at SS corner

Figure 70 demonstrates the PDP in RCA at the SS corner. Schmitt triggers circuits exhibit higher PDP compared to static CMOS configurations. Static CMOS XOR has more average power consumption than Static CMOS NAND.

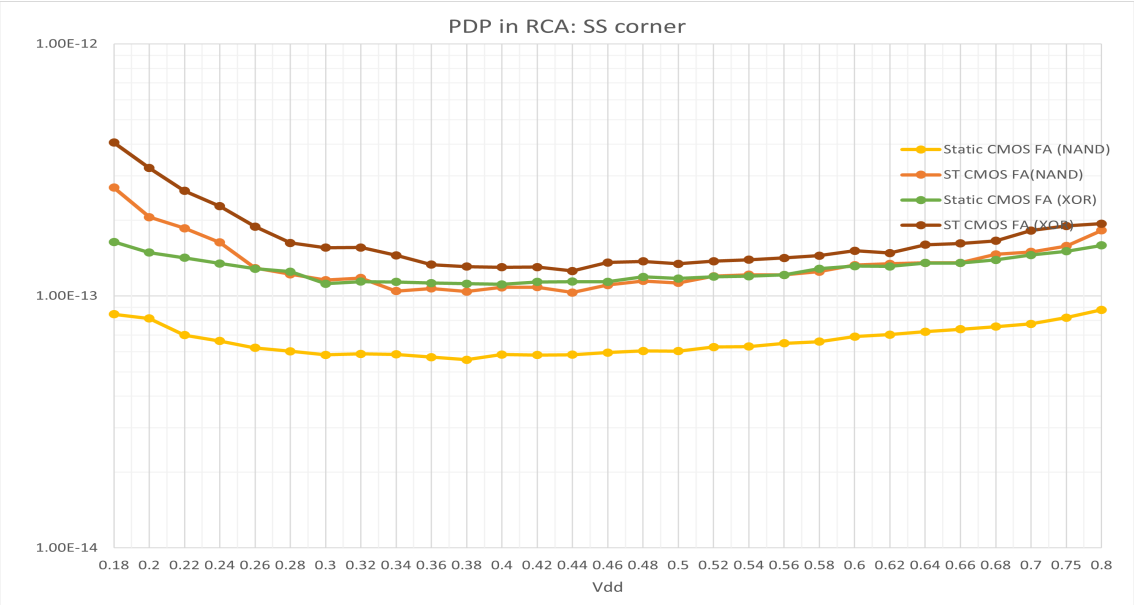


Figure 70: PDP in RCA at SS corner

Figure 71 demonstrates the EDP in RCA at the SS corner. Schmitt triggers circuits exhibit higher EDP compared to static CMOS configurations.

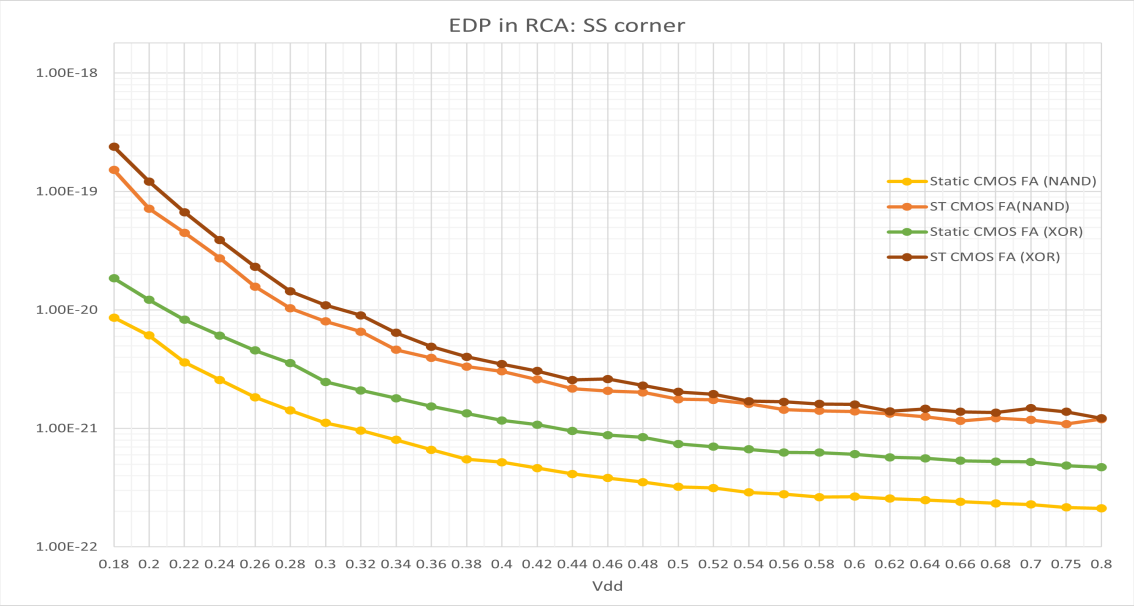


Figure 71: EDP in RCA at SS corner

3.4.2 4-bit Ripple Carry Adder: SF corner

At the SF corner: The RCA using full adder(Schmitt Trigger CMOS NAND gate), exhibits simulation failures (GMIN error) at certain voltage levels: 0.2V, 0.22V, 0.24V, 0.26V, 0.32V, 0.34V, 0.4V and 0.42V. However, a slight change in these voltages to 0.201V, 0.221V, 0.241V, 0.261V, 0.321V, 0.341V, 0.399V, and 0.401V respectively allows the circuit to operate correctly without any simulation problems.

The RCA using full adder(Schmitt Trigger CMOS XOR gate), exhibits simulation failures (GMIN error) at 0.46V, a slight increase to 0.461V allows the circuit to operate correctly without any simulation problems.

Figure 72 shows the propagation delay in RCA at the SF corner. The delay for Schmitt trigger CMOS is higher than static CMOS cases.

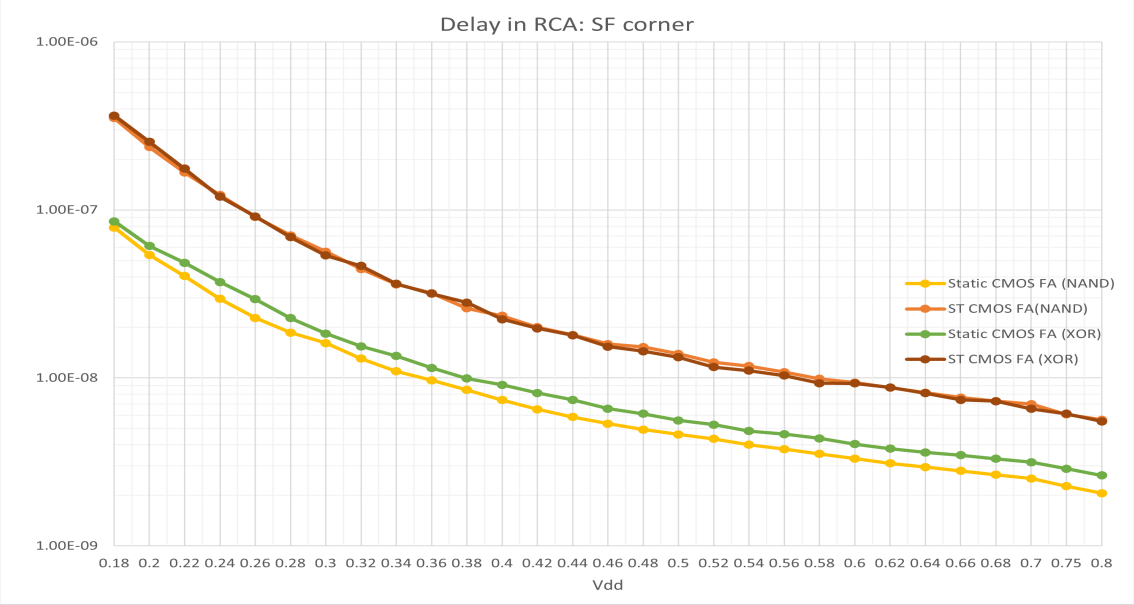


Figure 72: Delay in RCA at SF corner

The graph 73 demonstrates the average power in RCA at the SF corner. RCA (FA using on static CMOS XOR gate) shows the highest average power. Schmitt triggers CMOS NAND shows the lowest average power.

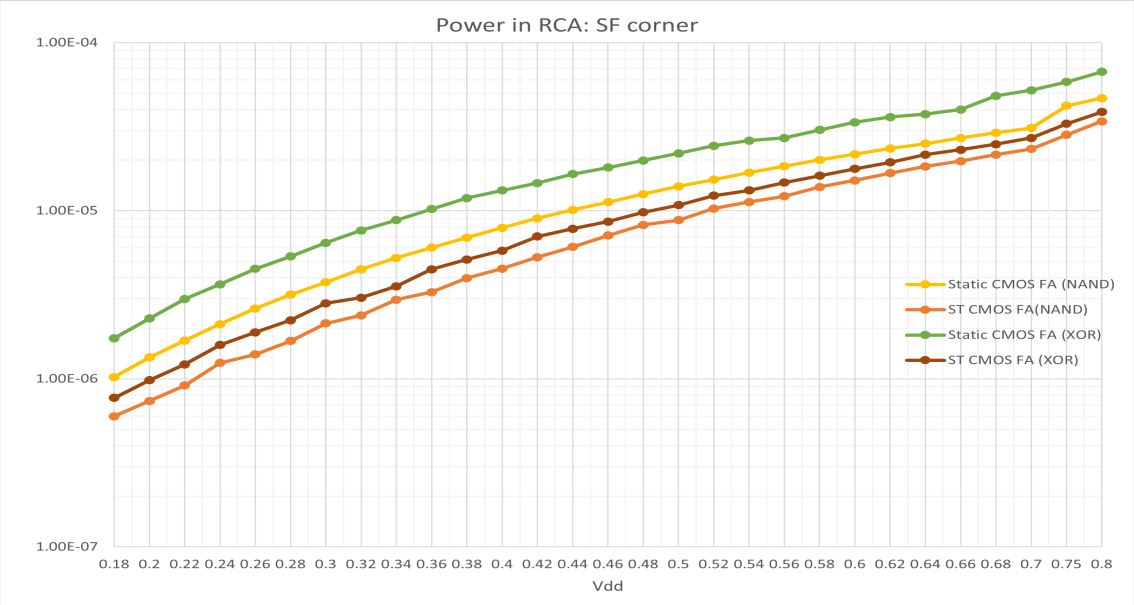


Figure 73: Power in RCA at SF corner

Figure 74 demonstrates the PDP in RCA at the SF corner. Schmitt triggers circuits exhibit higher PDP compared to static CMOS configurations.

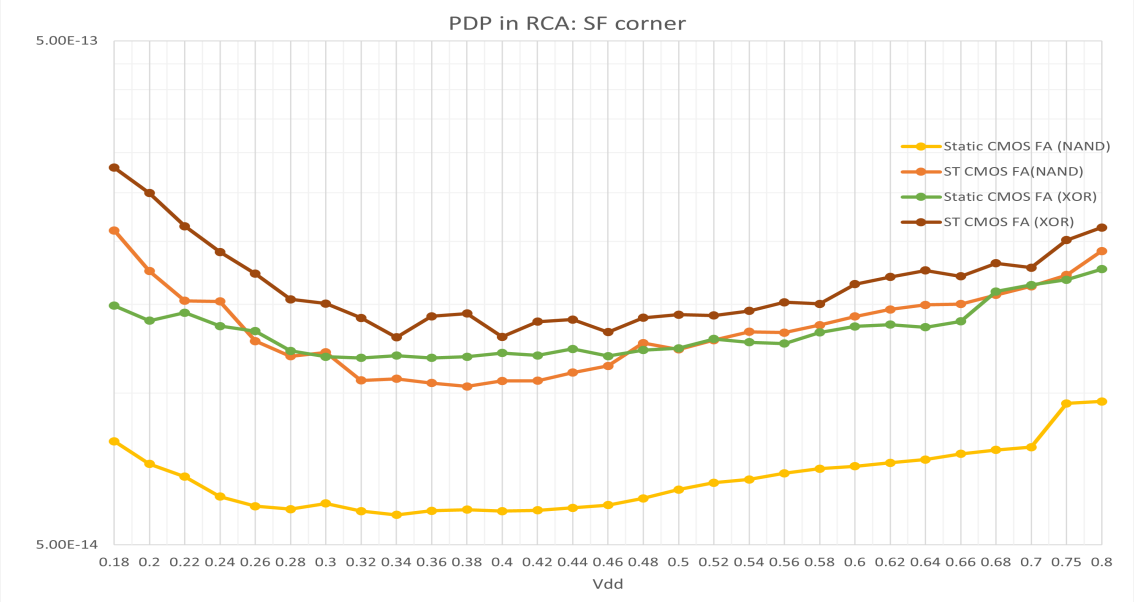


Figure 74: PDP in RCA at SF corner

Figure 75 demonstrates the EDP(Energy-Delay Product) in RCA at the SF corner. Schmitt triggers circuits exhibit higher EDP compared to static CMOS configurations.

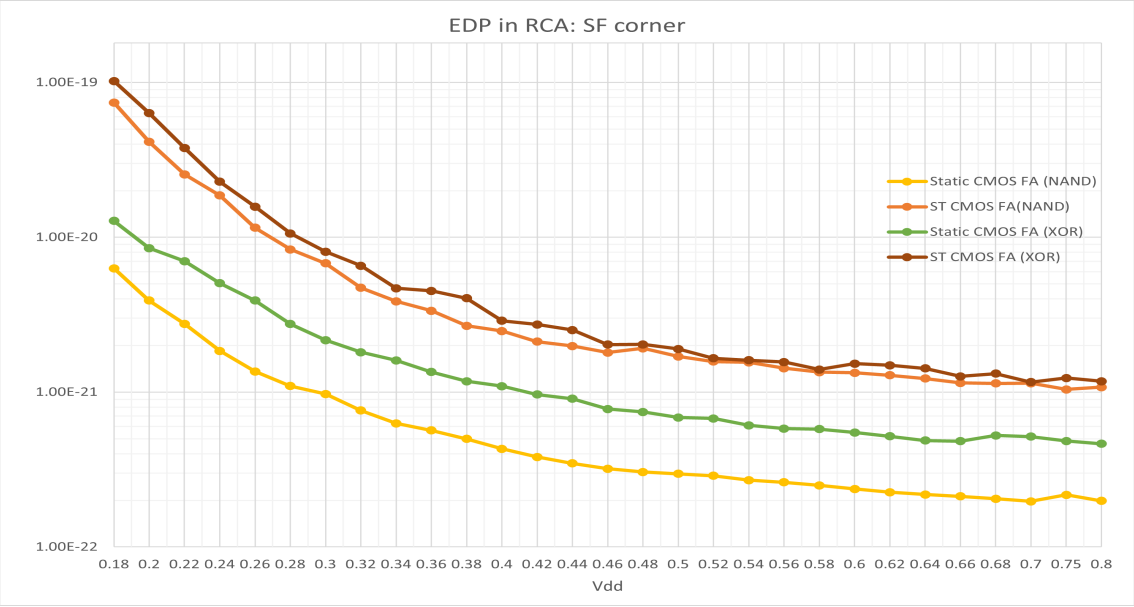


Figure 75: EDP in RCA at SF corner

3.4.3 4-bit Ripple Carry Adder: TT corner

At the TT corner: The RCA using full adder(Schmitt Trigger CMOS NAND gate), exhibits simulation failures (GMIN error) at voltages: 0.22V, 0.24V, 0.26V, and 0.4V. However, a slight increase in these voltages to 0.221V, 0.241V, 0.262V, and 0.401V respectively allows the circuit to operate correctly without any simulation problems.

The RCA using full adder(Schmitt Trigger CMOS XOR gate), exhibits simulation failures (GMIN error) at 0.48V, a slight increase to 0.481V allows the circuit to operate correctly without any simulation problems.

Figure 76 demonstrates the propagation delay in RCA at the TT corner. The delay for Schmitt trigger CMOS is higher than static CMOS cases.

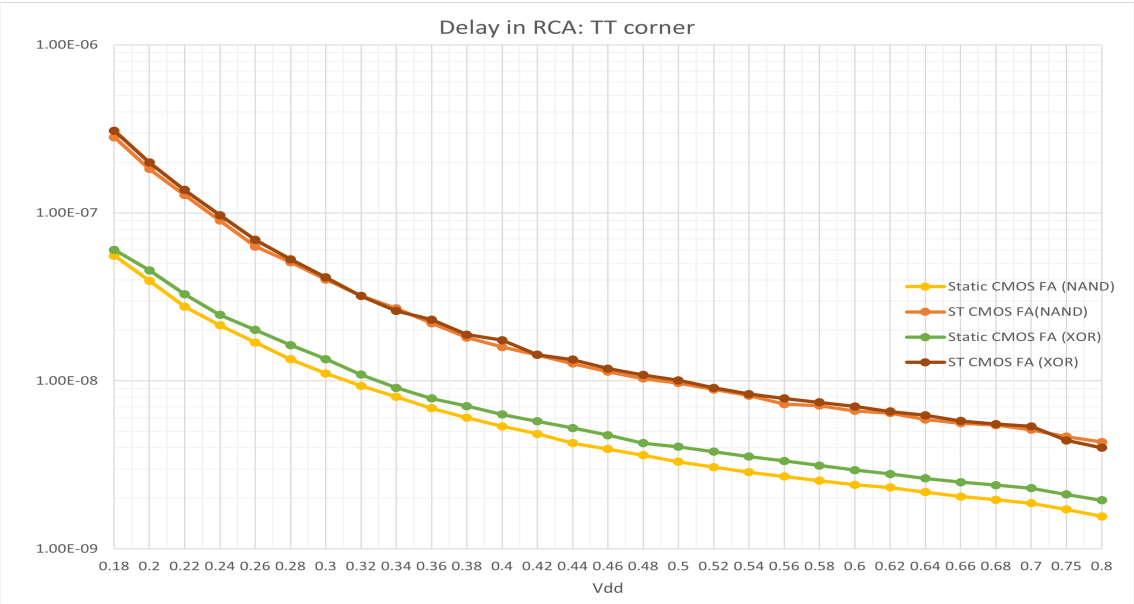


Figure 76: Delay in RCA at TT corner

Figure 77 demonstrates the average power in RCA at the TT corner. RCA (FA using on static CMOS XOR gate) shows more power. Schmitt triggers CMOS NAND shows the lowest average power consumption.

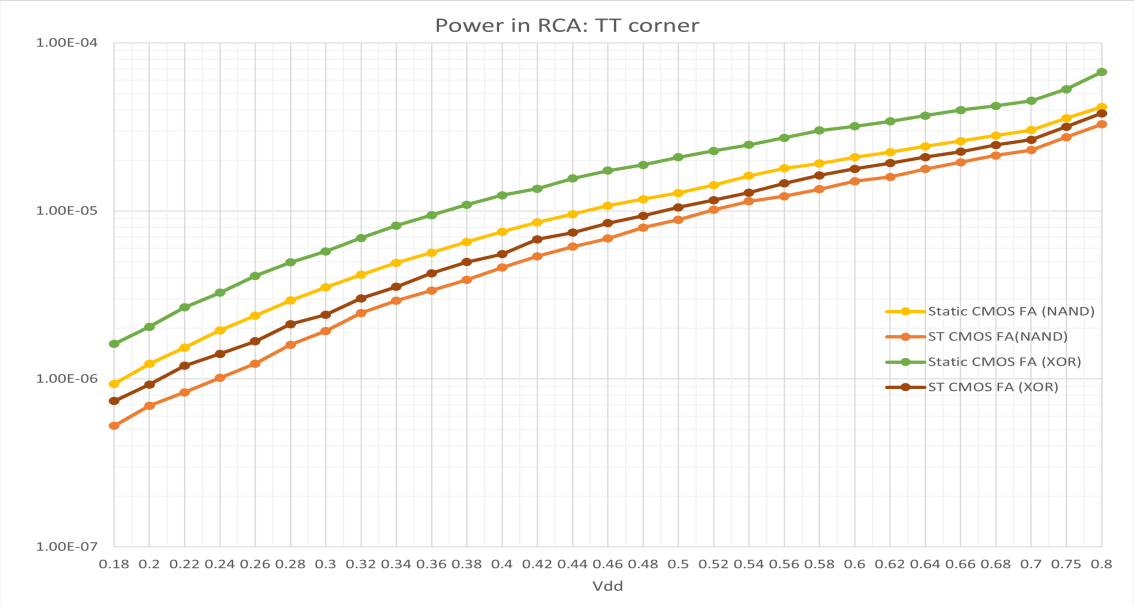


Figure 77: Power in RCA at TT corner

Figure 78 demonstrates the PDP in RCA at the TT corner. Schmitt triggers circuits exhibit higher PDP compared to static CMOS configurations.

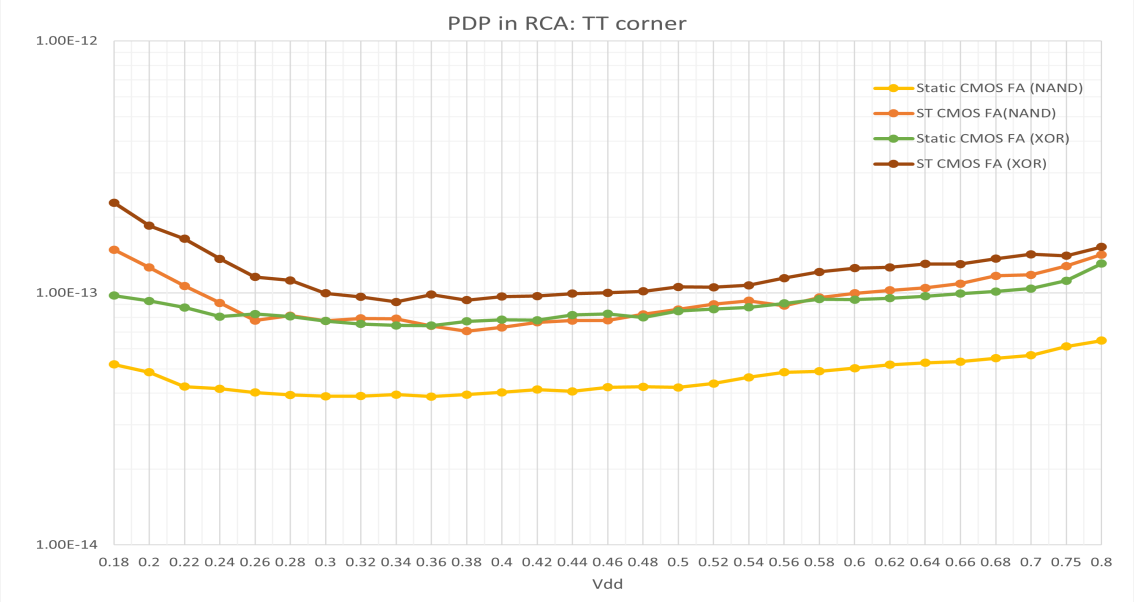


Figure 78: PDP in RCA at TT corner

Figure 79 demonstrates the EDP in RCA at the TT corner. Schmitt triggers circuits exhibit higher EDP compared to static CMOS configurations.

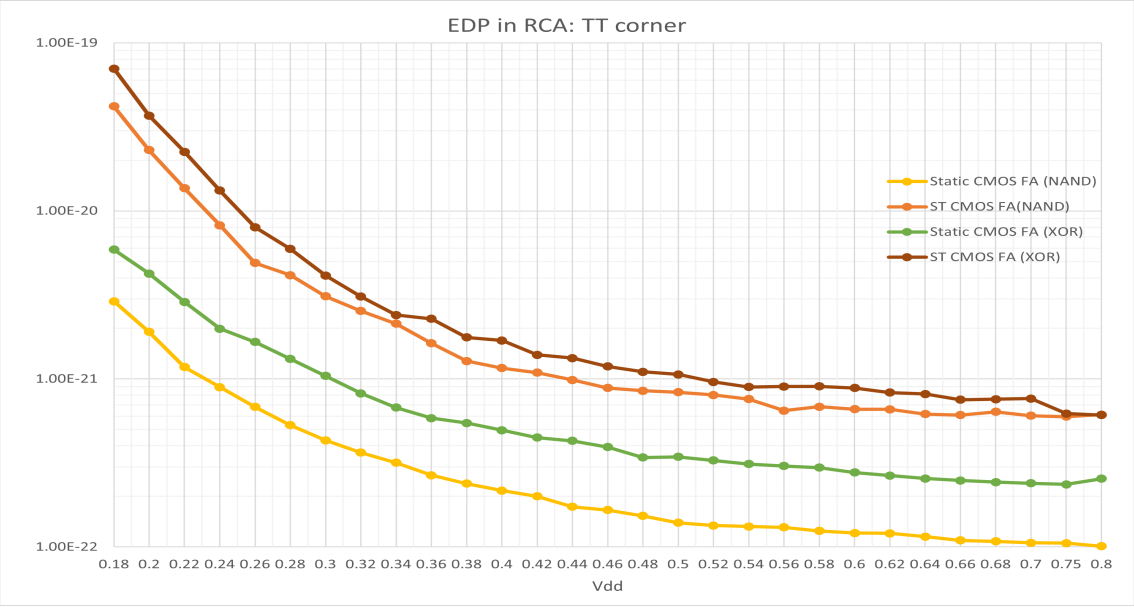


Figure 79: EDP in RCA at TT corner

3.4.4 4-bit Ripple Carry Adder: FS corner

At the FS corner: The RCA using full adder(Schmitt Trigger CMOS NAND gate), encounters simulation problems(GMIN error) at some voltage levels: 0.18V, 0.26V, 0.58V, 0.64V, and 0.66V. However, a slight change in these voltages to 0.181V, 0.261V, 0.579V, 0.641V, and 0.661V respectively allows the circuit to operate correctly without any simulation problems.

Figure 80 demonstrates the propagation delay in RCA at the FS corner. The delay for Schmitt trigger CMOS is higher than static CMOS cases.

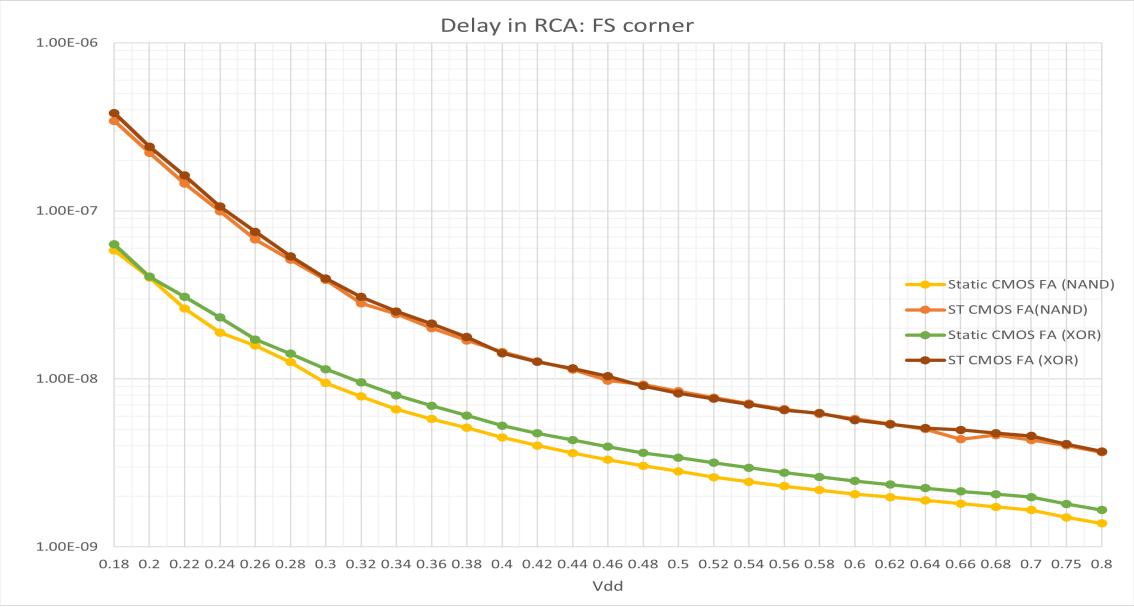


Figure 80: Delay in RCA at FS corner

Figure 81 demonstrates the average power in RCA at the FS corner. RCA (FA using static CMOS XOR gate) shows more power while RCA (FA using Schmitt triggers CMOS NAND gate) shows less power.

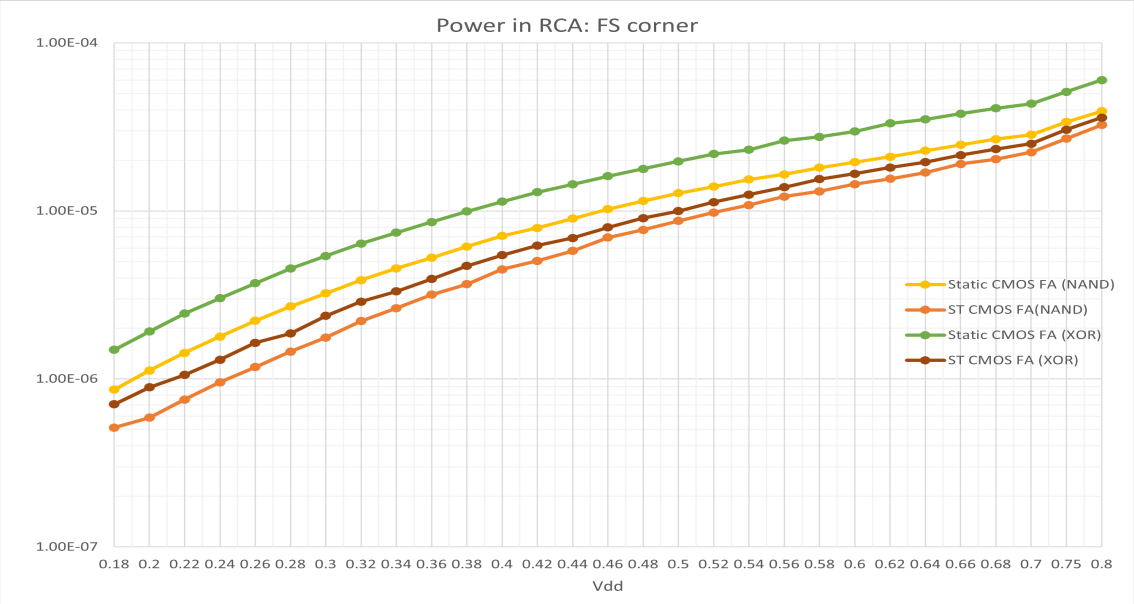


Figure 81: Power in RCA at FS corner

Figure 82 demonstrates the PDP in RCA at the FS corner. Schmitt triggers circuits exhibit higher PDP compared to static CMOS configurations.

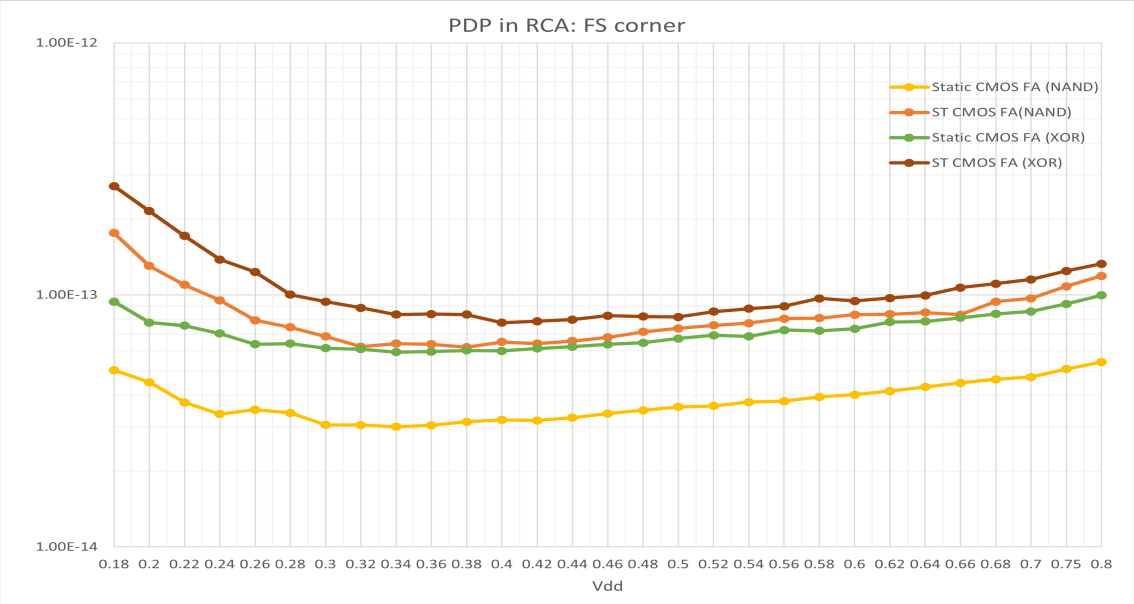


Figure 82: PDP in RCA at FS corner

Figure 83 demonstrates the EDP in RCA. Schmitt triggers circuits exhibit higher EDP compared to static CMOS configurations.

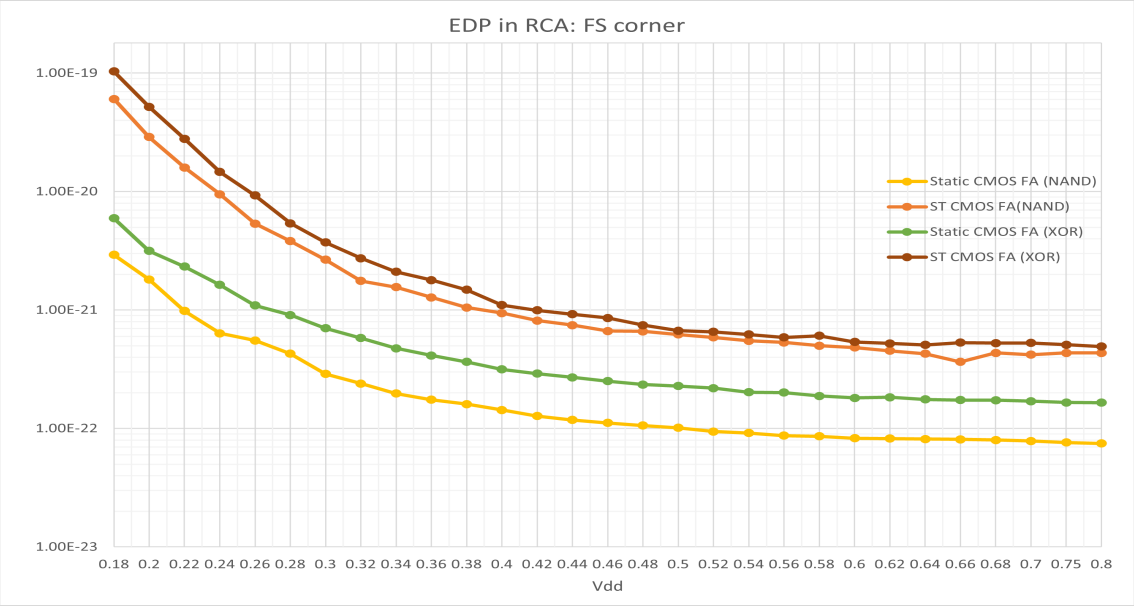


Figure 83: EDP in RCA at FS corner

3.4.5 4-bit Ripple Carry Adder: FF corner

At the FF corner: The RCA using full adder(Schmitt Trigger CMOS NAND gate) exhibits simulation issues(GMIN error) at voltages of 0.2, 0.22V, 0.24V, 0.26V, and 0.34V. Adjusting these voltages to 0.201V, 0.221V, 0.241V, 0.259V, and 0.341V respectively solve the problems.

Figure 84 demonstrates the propagation delay in RCA. The delay for Schmitt trigger CMOS is higher than static CMOS cases.

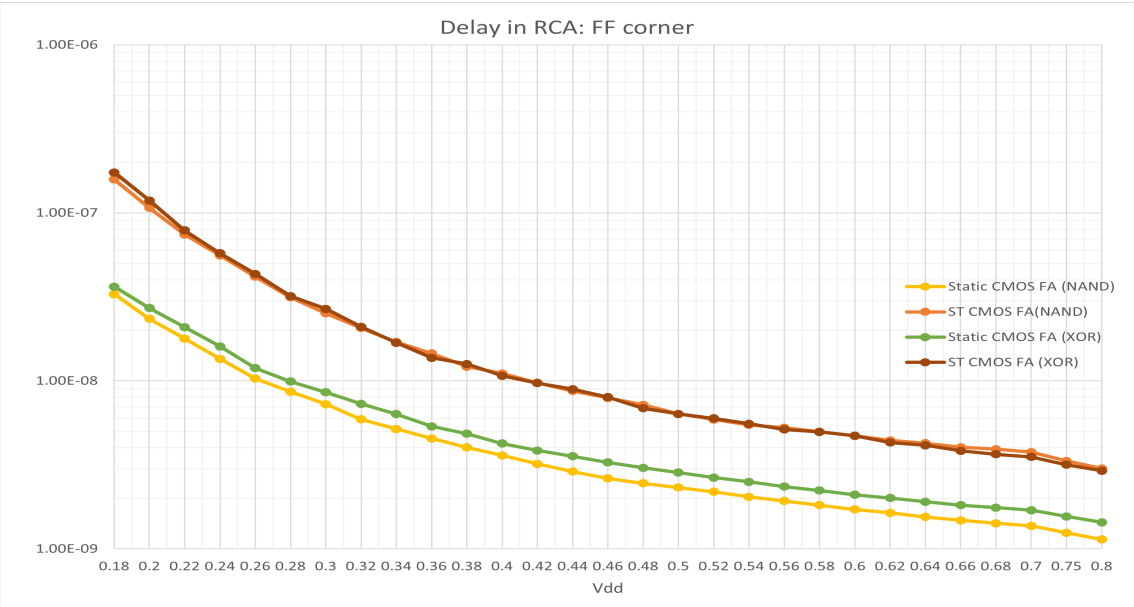


Figure 84: Delay in RCA at FF corner

Figure 85 demonstrates the average power in RCA. RCA (FA using static CMOS XOR gate) shows more power. RCA (FA using Schmitt triggers CMOS NAND), which shows the lowest average power consumption.

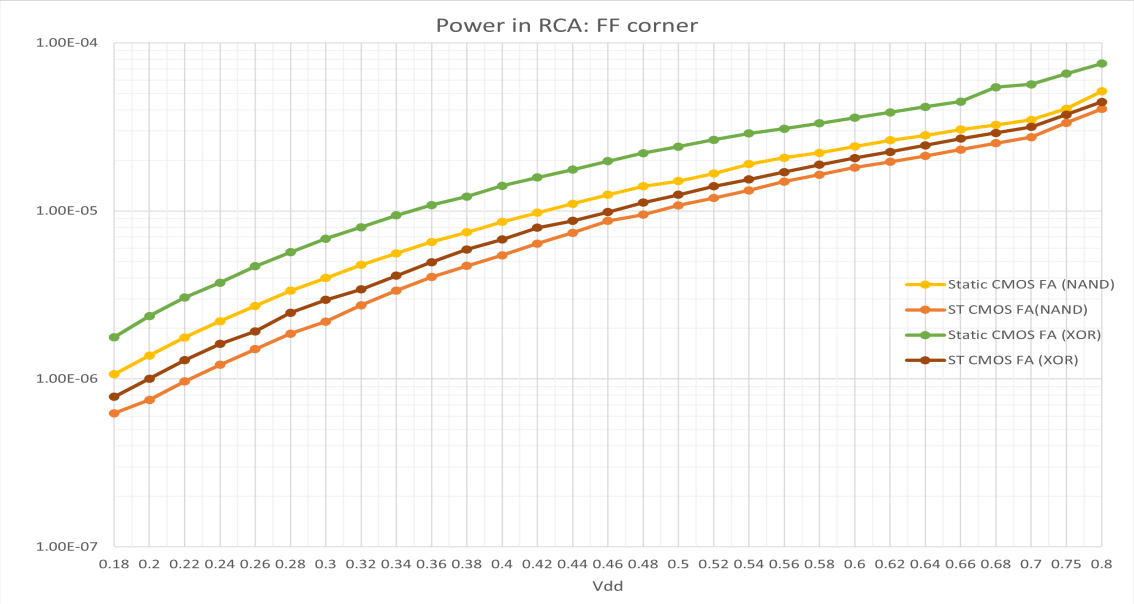


Figure 85: Power in RCA at FF corner

Figure 86 demonstrates the PDP(Power-Delay Product) in RCA. Schmitt triggers circuits exhibit higher PDP compared to static CMOS configurations.

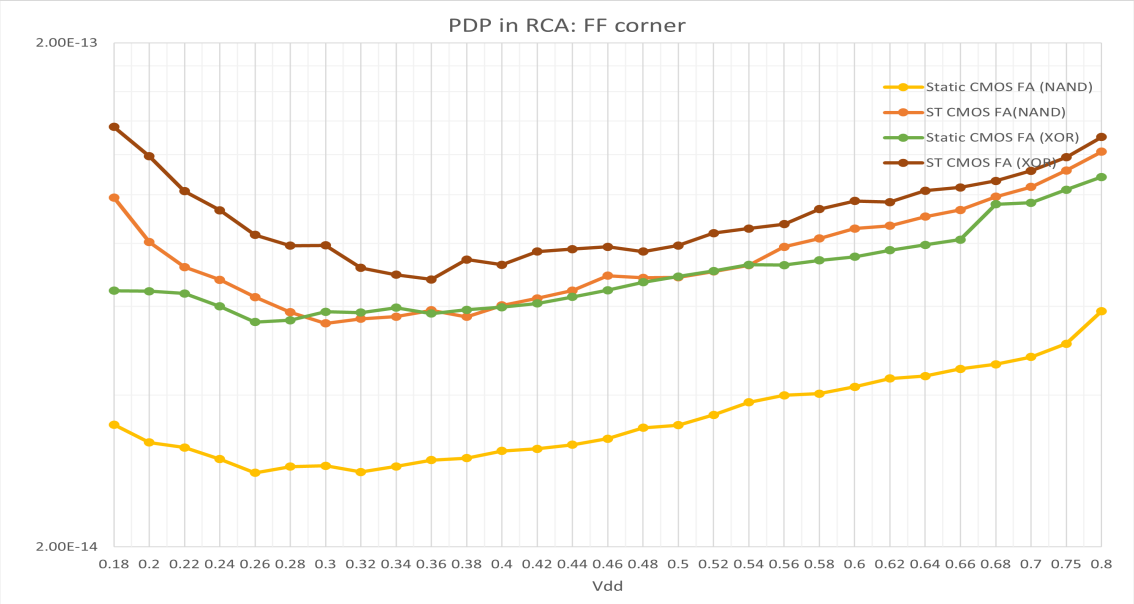


Figure 86: PDP in RCA at FF corner

Figure 87 demonstrates the EDP(Energy-Delay Product) in RCA. Schmitt triggers circuits exhibit higher EDP compared to static CMOS configurations.

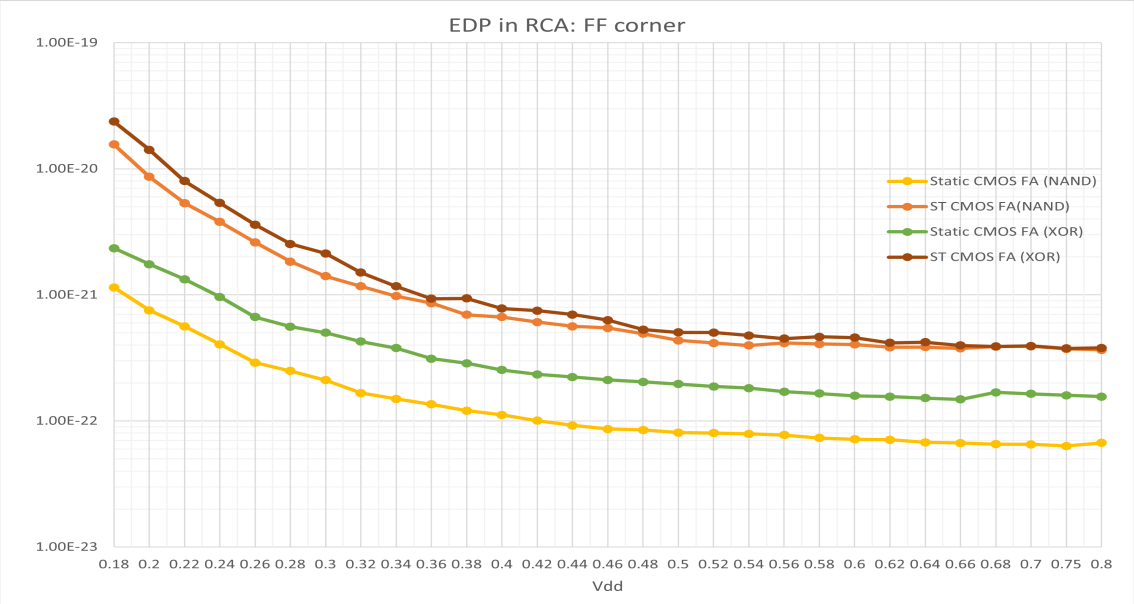


Figure 87: EDP in RCA at FF corner

4 Discussion

This chapter comprises four subsections, The first subsection focuses on full adders, analyzing various parameters such as noise margins, propagation delay, and average power are discussed across four types of full adders. The second subsection delves into four types of ring oscillators in which different parameters for example propagation delay, average power, PDP, and EDP are discussed. The third subsection discusses four types of RCAs, discussing parameters like Propagation delay, average power, PDP, and EDP. The final section outlines future research directions.

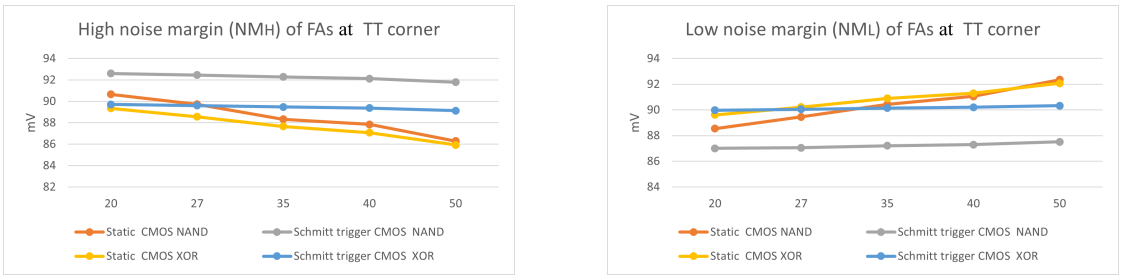
4.1 Full Adders:

In this section, the discussion is about 4 types of full adders, 1) FA implementation using static CMOS NAND and Inverter, 2) FA implementation using ST CMOS NAND and Inverter, 3) FA implementation using static CMOS XOR, and 4) FA implementation using ST CMOS XOR.

4.1.1 Noise margins:

The Schmitt trigger CMOS circuits show the same noise margins for both sum and carry while static CMOS circuits show different noise margins for both sum and carry. High noise margin (NM_H) and Low noise margin (NM_L) have consistent patterns for all four types of the full adder. (NM_H) follows the trend from lowest to highest is SF, FF, TT, SS, and FS. while (NM_L) follows the trend from lowest to highest is FS, SS, TT, FF, and SF.

Both types of Schmitt trigger CMOS (NAND and XOR) full adders, the noise margins (NM_H) and (NM_L) remain almost the same with the rise in temperature for all process corners. In contrast, for static CMOS (NAND and XOR) full adders, the noise margins changed much with the temperature rise, for example, In the figure 88a and 88b (NM_H) decreased and (NM_L) increased with the temperature rises. And same trend is followed by the FF and SS corners. The noise margins of the Schmitt trigger CMOS exhibit better stability against PVT variations in comparison to static CMOS, which aligns with the claims made in Melek's literature[2].



(a) (b)

Figure 88: (a) fig: High Noise margins comparison of FAs at TT. (b) fig: Low Noise margins comparison of FAs at TT.

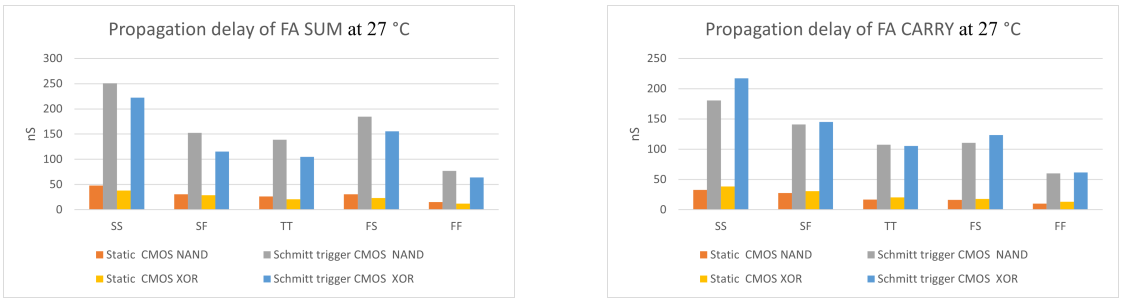
4.1.2 Propagation delay:

From the mentioned results, a common trend is observed that the propagation delay of the full adder decreases as the temperature goes up at 0.18V across all process corners.

In analyzing the sum propagation delay of Full Adders using static CMOS XOR and Schmitt trigger CMOS XOR, the order from lowest to highest is SF, FF, TT, SS, FS. Similarly, carry propagation delay in both full adders with static CMOS XOR and Schmitt trigger CMOS XOR, the order, ranked from the lowest to the highest, is FS followed by SS, TT, FF, and again FS.

In analyzing the sum propagation delay of full adders using static CMOS NAND gates is in the order of SS, SF, FS, TT, and FF. On the other hand, the sum propagation delay of Full Adders using Schmitt Trigger CMOS NAND gates is in order of SS, FS, SF, TT, and FF. Carry propagation delay in Full Adders using Static CMOS NAND gates, the order goes SS, SF, TT, FS, and FF. Switching to Schmitt Trigger CMOS XOR gates for carry propagation delay, SS, SF, FS, TT, and FF.

The propagation delay of the Schmitt trigger CMOS is higher compared to static CMOS, consistent with the findings reported in the literature[14].



(a) (b)

Figure 89: (a) fig: Propagation delay of FA SUM at 27 °C; (b) fig: Propagation delay of FA CARRY at 27 °C.

4.1.3 Average power:

The results presented in the tables offer a comprehensive analysis of the average power consumption of four different configurations of full adders (static CMOS NAND, Schmitt trigger CMOS NAND, static CMOS XOR, and Schmitt trigger CMOS XOR) across various temperatures and process corners at a supply voltage of 0.18V. The process corner analysis reveals that the SS corner offers the most power-efficient solution in all designs. This is followed by the Fs, TT, SF, and finally, the FF corner, which consistently shows the highest Average power. The average power is less in Schmitt triggers CMOS FAs than static CMOS FAs for all process corners.

At the SS corner, 0.18V, and 27°C, FA(static CMOS NAND gates) has an average power consumption of 545nW, while FA(Schmitt trigger CMOS NAND gates) consumes 360nW, achieving an average power saving of 34%. In comparison, FA(static CMOS XOR) consumes 926nW while FA(Schmitt trigger CMOS XOR) consumes 456nW which saves 50% average power. Opting for the Schmitt trigger CMOS NAND over the Schmitt trigger CMOS XOR can save an average power of 21%.

At the SF corner, 0.18V, and 27°C, FA with static CMOS NAND gates uses 677nW, while its Schmitt trigger counterpart uses 463nW, saving 31.6% power. In contrast, FA(static CMOS XOR) uses 1083nW, and the Schmitt trigger version uses 550nW, resulting in a 49% power reduction. Choosing Schmitt trigger CMOS NAND over XOR saves 15.8% more power.

At the TT corner, 0.18V, and 27°C the FA (static CMOS NAND) consumes 608nW, compared to 423nW for the FA(Schmitt trigger CMOS NAND), yielding a 30.4% power saving. Meanwhile, the FA(static CMOS XOR) consumes 1062nW versus 515nW for the FA(Schmitt trigger CMOS XOR), offering a 49.9% power decrease. Selecting Schmitt trigger CMOS NAND over XOR achieves an additional 17.8% power saving.

At the FS corner, 0.18V, and 27°C the FA (static CMOS NAND gates) has a power consumption of 561nW, in contrast to the FA with Schmitt trigger CMOS NAND gates, which consumes 389nW, thus achieving a 30.6% power saving. Meanwhile, FA with static CMOS XOR demands 936nW, whereas the Schmitt trigger CMOS XOR version requires 471nW, leading to a 49.6% decrease in power usage. Selecting Schmitt trigger CMOS NAND over the XOR variant results in an additional power saving of 17.4%.

At the FF corner, 0.18V, and 27°C the FA (static CMOS NAND gates) has a power consumption of 687nW, in contrast to the FA (Schmitt trigger CMOS NAND gates), which consumes 439nW, thus achieving a 36% power saving. Meanwhile, FA with static CMOS XOR demands 1149nW, whereas the Schmitt trigger CMOS XOR version requires 538nW, leading to a 53% decrease in power usage. Selecting Schmitt trigger CMOS NAND over the XOR variant results in an additional power saving of 18.4%.

The power consumption of the Schmitt trigger CMOS is considerably lower than static CMOS, supporting Melek's claim in the literature[2].

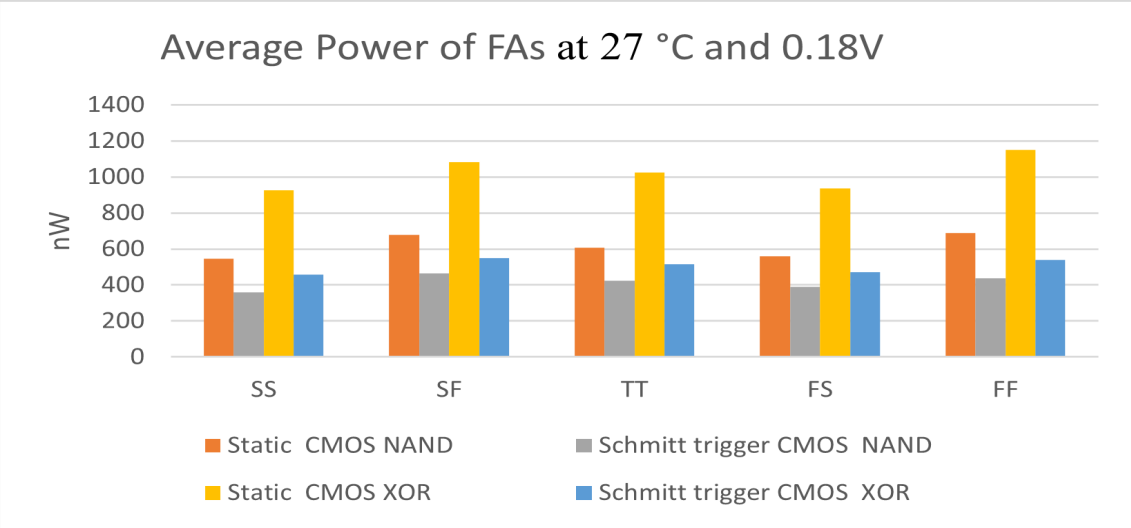


Figure 90: Average Power of the Full Adder at 0.18v and 27°C.

4.1.4 PDP:

Schmitt triggers CMOS full adders consumed for energy than static CMOS full adders. At 0.18V and 27°C, FA(Static CMOS NAND), is 208% (SS), 211% (SF), 316% (TT)), 237% (FS), and 194% (FF) more energy efficient, than the FA(Schmitt trigger CMOS NAND).

At 0.18V and 27°C, FA(Static CMOS XOR), is 208% (SS), 121% (SF), 216% (TT)), 269% (FS), and 160% (FF) more energy efficient, than the FA(Schmitt trigger CMOS XOR).

Opting FA(Schmitt trigger CMOS NAND) is energy efficient over FA(Static CMOS NAND).

4.2 Full adders connectivity as Ring oscillators:

4.2.1 Propagation delay: Full adders connectivity as Ring oscillator:

Propagation delay decreases with an increase in Vdd for all ring oscillators, supporting claim in the literature[10]. Schmitt trigger CMOS FAs show more propagation delay than static CMOS FAs in ring oscillators at all process corners, All process corners follow the same trend as Schmitt Trigger CMOS NAND gates show the longest delays, followed by Schmitt Trigger CMOS XOR, static CMOS NAND, and finally, static CMOS XOR, which has the shortest delays. Static CMOS NAND and static CMOS XOR have almost the same propagation delay at 0.56V for all process corners. The propagation delay of the Schmitt trigger CMOS is higher compared to static CMOS, aligning the literature[14].

4.2.2 Average power: Full adders connectivity as Ring oscillator:

All ring oscillators show the average power increases with the increase in voltage, supporting the claim in the literature[10].

All process corners follow the same trend as Schmitt Trigger CMOS XOR gates show the lowest average power, followed by Schmitt Trigger CMOS NAND, static CMOS NAND, and finally, static CMOS XOR, which has the highest average power.

At the SS corner and 0.18V, static CMOS NAND configuration consumes an average power of 9.96nW while Schmitt trigger CMOS NAND consumes an average power of 4.6nW, achieving an average power saving of 53%. In comparison, static CMOS XOR consumes an average power of 10.5nW while Schmitt trigger CMOS XOR consumes an average power of 3.6nW which saves 65.7% average power. Opting for the Schmitt trigger CMOS XOR over the Schmitt trigger CMOS NAND can save an average power of 21.7%.

At the SF corner and 0.18V, static CMOS NAND configuration consumes an average power of 10.03nW while Schmitt trigger CMOS NAND consumes an average power of 7.8nW, achieving an average power saving of 22%. In comparison, static CMOS XOR consumes an average power of 18.32nW while Schmitt trigger CMOS XOR consumes an average power of 7.03nW which saves 61.6% average power. Opting for the Schmitt trigger CMOS XOR over the Schmitt trigger CMOS NAND can save an average power of 9.8%.

At the TT corner and 0.18V, static CMOS NAND configuration consumes an average power of 10.6nW while Schmitt trigger CMOS NAND consumes an average power of 8.9nW, achieving an average power saving of 16%. In comparison, static CMOS XOR consumes an average power of 20.96nW while Schmitt trigger CMOS XOR consumes an average power of 6.93nW, saving 66.9% average power. Opting for the Schmitt trigger CMOS XOR over the Schmitt trigger CMOS NAND can save an average power of 22%.

At the FS corner and 0.18V, static CMOS NAND configuration consumes an average power of 10.55nW while Schmitt trigger CMOS NAND consumes an average power of 8.9nW, achieving an average power saving of 15.6%. In comparison, static CMOS XOR consumes an average power of 19.79nW while Schmitt trigger CMOS XOR consumes an average power of 6.82nW which saves 65.5% average power. Opting for the Schmitt trigger CMOS XOR over the Schmitt trigger CMOS NAND can save an average power of 23%.

At the FF corner and 0.18V, static CMOS NAND configuration consumes an average power of 17.79nW while Schmitt trigger CMOS NAND consumes an average power of 15.7nW, achieving an average power saving of 12%. In comparison, static CMOS XOR consumes an average power of 38.48nW while Schmitt trigger CMOS XOR consumes an average power of 12.31nW, saving 68% average power. Opting for the Schmitt trigger CMOS XOR over the Schmitt trigger CMOS NAND can save an average power of 21%.

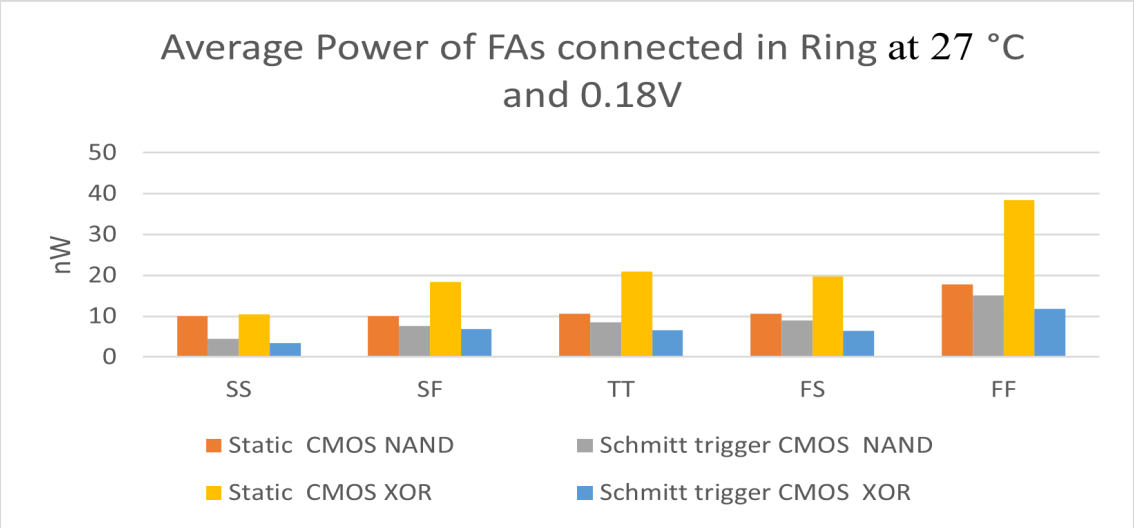


Figure 91: Average Power of the Full Adder connected in ring oscillator at 0.18v and 27°C.

4.2.3 PDP: Full adders connectivity as Ring oscillators:

The power delay product (PDP) increases with the increase in Vdd. PDP is higher for both Schmitt trigger CMOS circuits than static CMOS circuits. Schmitt trigger CMOS NAND gate has the highest PDP for all process corners, followed by the Schmitt trigger CMOS XOR gate, and static CMOS circuits. The PDP values depend on the process corners for static CMOS NAND and static CMOS XOR circuits. At the SS corner, the static CMOS NAND gate has more value of PDP than the static CMOS XOR gate. While the trend is reversed at the SF corner, the static CMOS XOR gate has more value of PDP than the static CMOS NAND gate.
At the TT and FF corner, the value of PDP is higher for static CMOS NAND gate than static CMOS XOR at 0.18V, both are almost equal from 0.2V to 0.3V, static CMOS XOR gate is higher than static CMOS NAND from 0.32 to 0.7V. At the FS corner, the value of PDP is a higher static CMOS NAND gate than static CMOS XOR for 0.18V to 0.22V, both are equal from 0.24V to 0.42V, static CMOS XOR gate is higher than static CMOS NAND from 0.44 to 0.7V.

At the SS corner and 0.18V, static CMOS NAND configuration consumes energy of 1288aJ while Schmitt trigger CMOS NAND consumes energy of 2229aJ, marking a 73% higher energy consumption. In comparison, static CMOS XOR consumes energy of 845aJ while Schmitt trigger CMOS XOR consumes energy of 2040aJ, making a 141% increase.

At the SF corner and 0.18V, static CMOS NAND's energy consumption is 1159aJ, whereas Schmitt triggers CMOS NAND's is 2112aJ, reflecting an 82% energy increase. In comparison, static CMOS XOR consumes energy of 1000aJ while Schmitt triggers CMOS XOR consumes energy of 1846aJ, making an 84% increase.

At the TT corner and 0.18V, static CMOS NAND consumes 1078aJ of energy, whereas Schmitt trigger CMOS NAND requires 2567aJ, reflecting a 138% energy increase. In contrast, static CMOS XOR consumes energy of 866aJ while Schmitt trigger CMOS XOR consumes energy of 2044aJ, making a 136% increase.

At the FS corner and 0.18V, static CMOS NAND and XOR consume 1440aJ and 1009aJ respectively, while their Schmitt trigger counterparts require 3310aJ and 2948aJ, marking energy increases of 129.8% and 192%.

At the FF corner and 0.18V: static CMOS NAND uses 1286aJ, Schmitt trigger NAND 2397aJ (84.9% more); Static CMOS XOR 1023aJ, Schmitt trigger XOR 2094aJ (104% more).

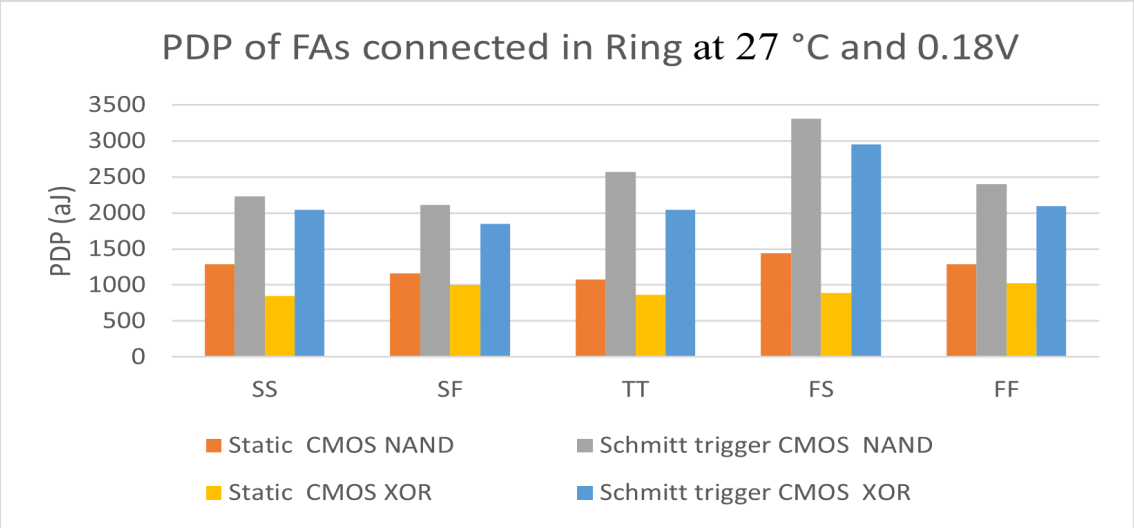


Figure 92: Energy of the Full Adder connected in the ring at 0.18v and 27°C.

In the Ring oscillators, energy consumption increases with a rise in voltage. The PDP patterns in the ring oscillator are aligned with the trend reported in the literature [10].

For the static CMOS NAND and XOR configurations, the point of minimum energy consumption is observed at 0.18V. For the Schmitt trigger CMOS NAND and XOR configurations, the point of minimum energy consumption is observed at 0.18V across SS, SF, and TT corners, while at FS, and FF minimum energy point is at 200mV. Then there is a consistent rise in energy similar to the literature [10].

4.2.4 EDP: Full adders connectivity as Ring oscillators:

The energy-delay product (EDP) decreases with the increase in Vdd for all designed ring oscillators, following the same trend as 32-bit RCA in the literature[10]. EDP is high for both Schmitt trigger CMOS circuits then Static CMOS circuits. Schmitt trigger CMOS XOR has the highest EDP for all process corners, followed by the Schmitt trigger CMOS NAND, and static CMOS circuits. Except for higher voltage for example 0.4V and o.44V at the SS and FF corners respectively where Schmitt trigger CMOS NAND consumes more energy compared to the Schmitt trigger XOR. The EDP values depend on the process corners for static CMOS NAND and static CMOS XOR circuits. But after a specific voltage static CMOS NAND and static CMOS XOR reverse the trend. For example SF at 0.34V, TT at 0.5V, FS at 0.46V, and FF at 0.36V.

4.3 4-bit Ripple Carry Adders:

4.3.1 Propagation delay: 4-bit Ripple Carry Adders:

Propagation delay decreases with an increase in Vdd for all RCAs. Schmitt trigger CMOS FAs show more propagation delay than Static CMOS FAs in ring oscillators at all process corners. All process corners follow the same trend as Schmitt Trigger CMOS XOR gates show the longest delays, followed by Schmitt Trigger CMOS NAND gate, static CMOS XOR gate, and finally, static CMOS NAND gate, which has the shortest delays. Schmitt Trigger CMOS NAND and Schmitt Trigger CMOS XOR have almost the same propagation delay for all process corners.

4.3.2 Average power: 4-bit Ripple Carry Adders:

Average power increases with the increase in Vdd for all four types of RCAs. All process corners(SS, SF, TT, FS, and FF) follow the trend as static CMOS XOR gates show the highest average power, followed by static CMOS NAND, Schmitt Trigger CMOS XOR, and finally, Schmitt Trigger CMOS NAND, which has the lowest average power.

At the SS corner and 0.18V, static CMOS NAND configuration consumes an average power of 830nW while Schmitt trigger CMOS NAND consumes an average power of 474nW, achieving an average power saving of 42.9%. In comparison, static CMOS XOR consumes an average power of 1443nW while Schmitt trigger CMOS XOR consumes an average power of 688nW which saves 52% average power. Opting for the Schmitt trigger CMOS NAND over the Schmitt trigger CMOS XOR can save an average power of 31%.

At the SF corner and 0.18V, static CMOS NAND configuration consumes an average power of 1022nW while Schmitt trigger CMOS NAND consumes an average power of 597nW, achieving an average power saving of 41.5%. In comparison, static CMOS XOR consumes an average power of 5.85nW while Schmitt trigger CMOS XOR consumes an average power of 3.09nW which saves 55.9% average power. Opting for the Schmitt trigger CMOS NAND over the Schmitt trigger CMOS XOR can save an average power of 22%.

At the TT corner and 0.18V, static CMOS NAND configuration consumes an average power of 934nW while Schmitt trigger CMOS NAND consumes an average power of 525nW, achieving an average power saving of 43.7%. In comparison, static CMOS XOR consumes an average power of 1616nW while Schmitt trigger CMOS XOR consumes an average power of 738nW, saving 54.3% average power. Opting for the Schmitt trigger CMOS NAND over the Schmitt trigger CMOS XOR can save an average power of 28.8%.

At the FS corner and 0.18V, static CMOS NAND configuration consumes an average power of 864nW while Schmitt trigger CMOS NAND consumes an average power of 512nW, achieving an average power saving of 40.7%. In comparison, static CMOS XOR consumes an average power of 1489nW while Schmitt trigger CMOS XOR consumes an average power of 706nW, saving 52.5% average power. Opting for the Schmitt trigger CMOS NAND over the Schmitt trigger CMOS XOR can save an average power of 27.4%.

At the FF corner and 0.18V, static CMOS NAND configuration consumes an average power of 1065nW while Schmitt trigger CMOS NAND consumes an average power of 624nW, achieving an average power saving of 41.4%. In comparison, static CMOS XOR consumes an average power of 1772nW while Schmitt trigger CMOS XOR consumes an average power of 783nW, saving 55.8% average power. Opting for the Schmitt trigger CMOS XOR over the Schmitt trigger CMOS NAND can save an average power of 20.3%.

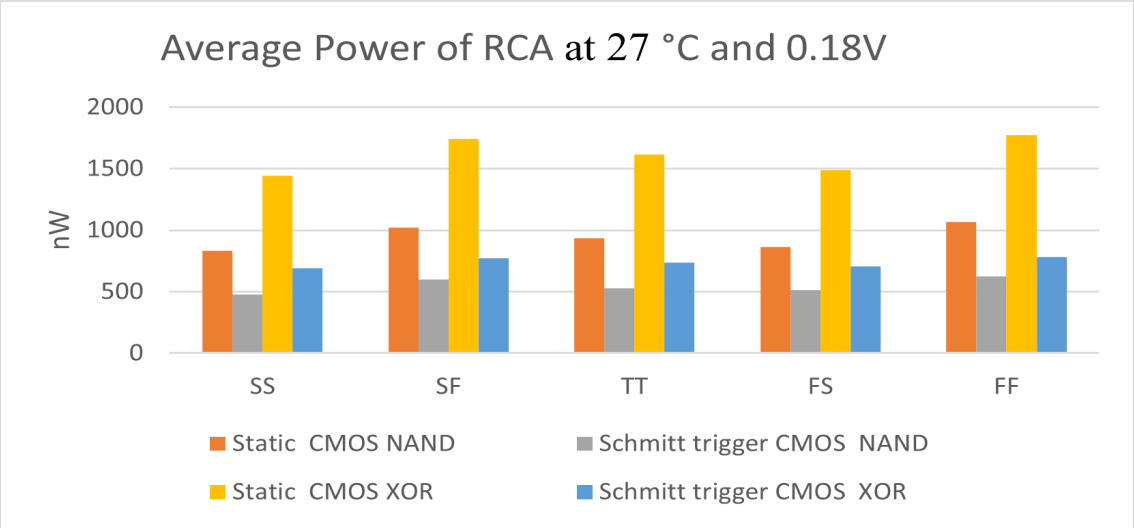


Figure 93: Average Power of the RCA at 0.18v and 27°C.

4.3.3 PDP: 4-bit Ripple Carry Adders:

Power delay product(PDP) is high for both Schmitt trigger CMOS circuits then Static CMOS circuits. All process corners(SS, SF, TT, FS, and FF) follow the trend as Schmitt Trigger CMOS XOR gates show the highest PDP, followed by Schmitt Trigger CMOS NAND, static CMOS XOR, and finally, static CMOS NAND, which has the lowest average power. But at some specific voltages, the PDP of static CMOS XOR goes higher than Schmitt trigger CMOS NAND.

RCA at the SS corner and 0.18V, static CMOS NAND configuration consumes energy of 84613aJ while Schmitt trigger CMOS NAND consumes energy of 268892aJ, marking a 68% higher energy consumption. In comparison, static CMOS XOR consumes energy of 163621aJ while Schmitt trigger CMOS XOR consumes energy of 405554aJ, making a 59% increase.

RCA at the SF corner and 0.18V, static CMOS NAND's energy consumption is 80264aJ, whereas Schmitt triggers CMOS NAND's is 210270aJ, reflecting a 61.8% energy increase. In comparison, static CMOS XOR consumes energy of 149138aJ while Schmitt trigger CMOS XOR consumes energy of 280251aJ, making a 46.7% increase.

RCA at the TT corner and 0.18V, static CMOS NAND consumes 52034aJ of energy, whereas Schmitt trigger CMOS NAND requires 1483666aJ, reflecting a 64.9% energy increase. In contrast, static CMOS XOR consumes energy of 97543aJ while Schmitt trigger CMOS XOR consumes energy of 227787aJ, making a 57% increase.

RCA at the FS corner and 0.18V, static CMOS NAND and XOR consume 50266aJ and 94088aJ respectively, while their Schmitt trigger counterparts require 176122aJ and 270286aJ, marking energy increases of 71% and 65%.

RCA at the FF corner and 0.18V: static CMOS NAND uses 34949aJ, Schmitt trigger NAND 98693aJ (64% more); Static CMOS XOR 64476aJ, Schmitt trigger XOR 136264aJ (52% more)

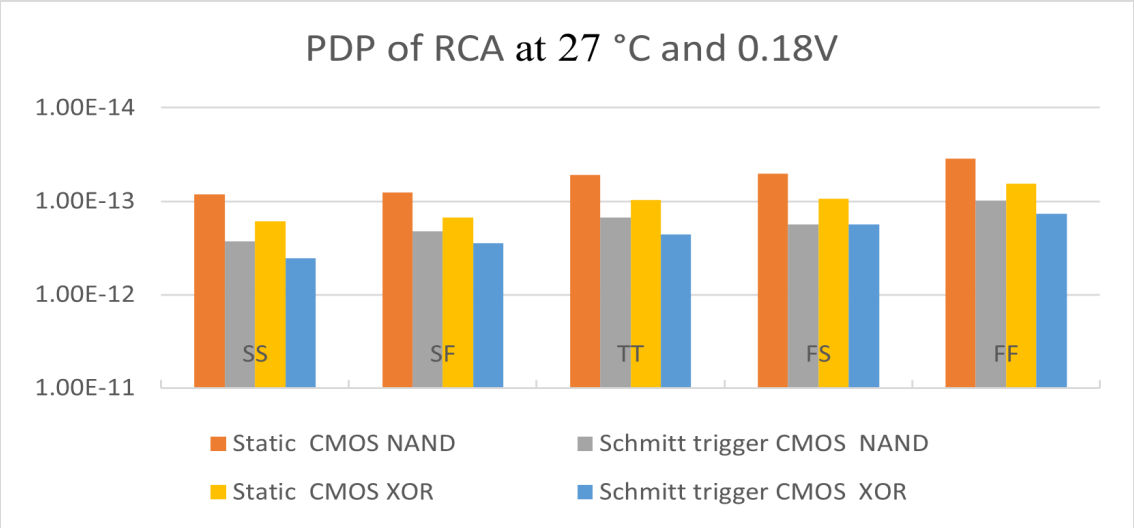


Figure 94: PDP of the RCA at 0.18v and 27°C.

In the RCA, energy consumption decreases with a rise in voltage but after a specific voltage threshold, the trend reverses, and energy starts increasing. The PDP patterns in the RCA are aligned with the trend reported in the literature [10]; however, the RCA exhibits a more gradual increase in energy beyond the threshold voltage, but in the literature [10] more sharp rise is noticed.

For the static CMOS NAND configuration, the point of minimum energy consumption is observed at 0.34V across all process corners, except the SS and FF corners where the lowest energy is at 0.38V and 0.26V respectively.

For the Schmitt trigger CMOS NAND configuration, the point of minimum energy consumption is observed at 0.38V across all process corners, except the FF corner where the lowest energy is reached at 0.3V.

For the static CMOS XOR configuration, the point of minimum energy consumption is observed at 0.34V for TT and FS process corners, at 0.3V for SS and SF process corners, and FF corners where the lowest energy is at 0.26V.

The minimum energy point for the Schmitt trigger CMOS XOR configuration occurs at 0.34V in both the TT and SF process corners, at 0.44V for SS, at 0.4V for FS, and at 0.36V for FF corners.

4.3.4 EDP: 4-bit Ripple Carry Adders:

The energy-delay product (EDP) decreases with the increase in Vdd. The EDP values depend on the process corners for static CMOS NAND and static CMOS XOR circuits. EDP is high for both Schmitt trigger CMOS circuits then static CMOS circuits. Schmitt trigger CMOS XOR configuration has the highest EDP for all process corners, followed by the Schmitt trigger CMOS NAND, static CMOS XOR, and static CMOS CMOS NAND.

4.4 Conclusion and Future work:

4.4.1 Conclusion:

In this thesis, the operation of the static CMOS vs CMOS Schmitt trigger has been analyzed. Both Schmitt triggers CMOS full adders give a stable noise margin with the rise in temperature and low average power consumption as compared to static CMOS full adders. Among both Schmitt trigger CMOS full adders, Schmitt trigger CMOS NAND consumes 15% to 21% less average power than Schmitt trigger CMOS XOR at 0.18V and 27°C. Energy consumption for the Schmitt trigger

is high due to higher propagation delay. However, another drawback is that the area occupied by the Schmitt trigger is much greater than that of static CMOS.

In the ring oscillators, Schmitt triggers consumed less average power and high energy than static CMOS. Schmitt trigger CMOS XOR consumes 9.8% to 23% less average power than Schmitt trigger CMOS NAND at 0.18V and 27°C.

In the RCAs, Schmitt triggers consumed less average power and high energy than static CMOS. Schmitt trigger CMOS NAND consumes 20% to 31% less average power than Schmitt trigger CMOS XOR at 0.18V and 27°C.

4.4.2 Future work:

This thesis dealt with the analysis of the Schmitt trigger CMOS, and static CMOS and showed that it presents a lower dependence on PVT variations. All PMOSs body bias with Vdd and NMOS body bias with Vss. Although some good results have been achieved. For future work, I suggest: applying both forward and reverse body bias techniques to the ST may may reduce even more the dependence on PVT variations, and may operate closer to the minimum supply voltage.

References

[1] Massimo Alioto. 'Ultra-Low Power VLSI Circuit Design Demystified and Explained: A Tutorial'. In: *IEEE Transactions on Circuits and Systems I: Regular Papers* 59.1 (2012), pp. 3–29. DOI: 10.1109/TCSI.2011.2177004.

[2] Luiz Alberto P. Melek. 'Analysis and design of a subthreshold CMOS Schmitt trigger circuit'. In: 2017.

[3] Ying-Khai Teh and Philip K. T. Mok. 'A Stacked Capacitor Multi-Microwatts Source Energy Harvesting Scheme With 86 mV Minimum Input Voltage and ±3 V Bipolar Output Voltage'. In: *IEEE Journal on Emerging and Selected Topics in Circuits and Systems* 4.3 (2014), pp. 313–323. DOI: 10.1109/JETCAS.2014.2337152.

[4] Po-Hung Chen et al. 'Startup Techniques for 95 mV Step-Up Converter by Capacitor Pass-On Scheme and ${V}_{TH}$-Tuned Oscillator With Fixed Charge Programming'. In: *IEEE Journal of Solid-State Circuits* 47 (2012), pp. 1252–1260.

[5] Luiz Alberto Pasini Melek et al. 'Analysis and Design of the Classical CMOS Schmitt Trigger in Subthreshold Operation'. In: *IEEE Transactions on Circuits and Systems I: Regular Papers* 64.4 (2017), pp. 869–878. DOI: 10.1109/TCSI.2016.2631726.

[6] Robert H. Reuss and Michael Fritze. 'Introduction to Special Issue on Circuit Technology for ULP [Scanning the Issue]'. In: *Proceedings of the IEEE* 98.2 (2010), pp. 139–143. DOI: 10.1109/JPROC.2009.2037210.

[7] Hyung-Il Kim and K. Roy. 'Ultra-low power DLMS adaptive filter for hearing aid applications'. In: *ISLPED'01: Proceedings of the 2001 International Symposium on Low Power Electronics and Design (IEEE Cat. No.01TH8581)*. 2001, pp. 352–357. DOI: 10.1109/LPE.2001.945431.

[8] H. Soeleman, K. Roy and B. Paul. 'Sub-Domino logic: ultra-low power dynamic sub-threshold digital logic'. In: *VLSI Design 2001. Fourteenth International Conference on VLSI Design*. 2001, pp. 211–214. DOI: 10.1109/ICVD.2001.902662.

[9] Srinivasa Rao Ijjada et al. 'Design of high efficient & low power basic gates in subthreshold region'. In: *International Journal of Advances in Engineering & Technology* 1.2 (2011), p. 215.

[10] V. Beiu et al. 'On the advantages of serial architectures for low-power reliable computations'. In: *2005 IEEE International Conference on Application-Specific Systems, Architecture Processors (ASAP'05)*. 2005, pp. 276–281. DOI: 10.1109/ASAP.2005.48.

[11] Niklas Lotze and Yiannos Manoli. 'A 62 mV 0.13 μ m CMOS Standard-Cell-Based Design Technique Using Schmitt-Trigger Logic'. In: *IEEE Journal of Solid-State Circuits* 47.1 (2012), pp. 47–60. DOI: 10.1109/JSSC.2011.2167777.

[12] K. Granhaug and S. Aunet. 'Six subthreshold full adder cells characterized in 90 nm CMOS technology'. In: *2006 IEEE Design and Diagnostics of Electronic Circuits and systems*. 2006, pp. 25–30. DOI: 10.1109/DDECS.2006.1649565.

[13] Marco Donato et al. 'A noise-immune sub-threshold circuit design based on selective use of Schmitt-trigger logic'. In: May 2012. DOI: 10.1145/2206781.2206792.

[14] Bhawanand Jha, Kirti Gupta and Rajeshwari Pandey. 'Low Voltage Schmitt Trigger Full Adders Design for High Noise Immunity'. In: *2022 8th International Conference on Signal Processing and Communication (ICSC)*. 2022, pp. 618–623. DOI: 10.1109/ICSC56524.2022.10009098.

[15] J.R. Hauser. 'Noise margin criteria for digital logic circuits'. In: *IEEE Transactions on Education* 36.4 (1993), pp. 363–368. DOI: 10.1109/13.241612.

Appendix

A Python scripts:

A.1 Python script to draw the the graph (DC analysis curve analysis for noise margin) from text file.

```
import numpy as np
import matplotlib.pyplot as plt


data = np.loadtxt('1.txt', skiprows=1)

vout = data[:, 1]
vin = data[:, 0]

dvout_dvin = np.gradient(vout) / np.gradient(vin)
idx = np.argmax(np.abs(dvout_dvin + 1))
idx1 = np.argmin(np.abs(dvout_dvin[idx:] -2)) + idx

idx_upper = np.argmin(np.abs(dvout_dvin[:idx] - 1))


plt.plot(vin, vout, 'b', label='Data')
plt.xlabel('Vin [V]', fontsize=14, fontweight='bold', fontfamily='serif
    ')
plt.ylabel('Vout [V]', fontsize=14, fontweight='bold', fontfamily='
    serif')


x0 = vin[idx]
y0 = vout[idx]
slope = dvout_dvin[idx]
intercept = y0 - slope * x0
x = np.linspace(x0 - 0.02, x0 + 0.02, 100)
y = slope * x + intercept
#plt.plot(x, y, 'r--', label='Tangent at dvout/dvin=-1')


x_upper = vin[idx_upper]
y_upper = vout[idx_upper]
slope_upper = dvout_dvin[idx_upper]
intercept_upper = y_upper - slope_upper * x_upper
x_upper_tangent = np.linspace(x_upper - 0.02, x_upper + 0.02, 100)
y_upper_tangent = slope_upper * x_upper_tangent + intercept_upper
plt.plot(x_upper_tangent, y_upper_tangent, '--', color='orange', label
    ='Tangent on lower edge at dvout/dvin=-1')


x1 = vin[idx1]
y1 = vout[idx1]
slope = dvout_dvin[idx1]
intercept = y1 - slope * x1
x_1 = np.linspace(x1 - 0.02, x1 + 0.02, 100)
y_1 = slope * x_1 + intercept
```

```
plt.plot(x_1, y_1, 'g--', label='Tangent at higher level dvout/dvin
    =-1')

plt.plot(x0, y0, 'o', label='The midpoint where Vout = Vin .')

plt.plot(x1, y1, 'go', label='Intersection point on higher tangent')

plt.plot(x_upper, y_upper, 'o', label='Intersection point on lower
    tangent')

xmin, xmax = plt.xlim()
ymin, ymax = plt.ylim()
if x0 >= xmin and x0 <= xmax:
    plt.axvline(x=x0, ymin=(y0-ymin)/(ymax-ymin), ymax=(0-ymin)/(ymax-
        ymin), linestyle='', color='gray')
    plt.plot([x0, x0], [y0, 0], linestyle='--', color='gray')
    plt.text(x0, ymin+0.1*(ymax-ymin), 'VM = {}'.format(x0), ha='left',
         va='top', color='gray')
if y0 >= ymin and y0 <= ymax:
    plt.axhline(y=y0, xmin=(x0-xmin)/(xmax-xmin), xmax=(0-xmin)/(xmax-
        xmin), linestyle='', color='gray')
    plt.plot([x0, 0], [y0, y0], linestyle='--', color='gray')
    plt.text(xmin+0.1*(xmax-xmin), y0, 'VM = {}'.format(y0), ha='left',
         va='bottom', color='gray')

xmin, xmax = plt.xlim()
ymin, ymax = plt.ylim()
if x1 >= xmin and x1 <= xmax:
    plt.axvline(x=x1, ymin=(y1-ymin)/(ymax-ymin), ymax=(0-ymin)/(ymax-
        ymin), linestyle='', color='green')
    plt.plot([x1, x1], [y1, 0], linestyle='--', color='green')
    plt.text(x1, ymin+0.1*(ymax-ymin), 'VIH = {}'.format(x1), ha='right
        ', va='top', color='green')
if y1 >= ymin and y1 <= ymax:
    plt.axhline(y=y1, xmin=(x0-xmin)/(xmax-xmin), xmax=(0-xmin)/(xmax-
        xmin), linestyle='', color='green')
    plt.plot([x1, 0], [y1, y1], linestyle='--', color='green')
    plt.text(xmin+0.1*(xmax-xmin), y1, 'VOH={}'.format(y1), ha='left',
        va='top', color='green')



xmin, xmax = plt.xlim()
ymin, ymax = plt.ylim()
if x_upper >= xmin and x_upper <= xmax:
    plt.axvline(x=x_upper, ymin=(y0-ymin)/(ymax-ymin), ymax=(0-ymin)/(
        ymax-ymin), linestyle='', color='Orange')
    plt.plot([x_upper, x_upper], [y_upper, 0], linestyle='--', color='
        Orange')
    plt.text(x_upper, ymin+0.1*(ymax-ymin), 'VIL = {}'.format(x_upper),
         ha='center', va='bottom', color='Orange')
if y_upper >= ymin and y_upper <= ymax:
    plt.axhline(y=y_upper, xmin=(x_upper-xmin)/(xmax-xmin), xmax=(0-
        xmin)/(xmax-xmin), linestyle='', color='Orange')
    plt.plot([x_upper, 0], [y_upper, y_upper], linestyle='--', color='
        Orange')
    plt.text(xmin+0.1*(xmax-xmin), y_upper, 'VOL={}'.format(y_upper),
        ha='left', va='bottom', color='Orange')
```

```
plt.xlim(min(vin), max(vin))
plt.ylim(min(vout), max(vout))

plt.xticks(fontsize=12, fontweight='bold')
plt.yticks(fontsize=12, fontweight='bold')
plt.legend(fontsize=10, loc='best')
plt.grid(True, linewidth=0.20, alpha=0.5)
plt.grid(True, which='minor', linewidth=0.5, alpha=0.5, linestyle=':')


VOH = y1
VIH = x1
VOL = y_upper
VIL = x_upper
NMH = VOH - VIH
NML = VIL - VOL
NMH1=NMH * 1000
NML1=NML * 1000

NMH_str = '{:.4f}'.format(NMH1)
NML_str = '{:.4f}'.format(NML1)

print('Noise margin high (NMH) = VOH - VIH =', VOH, '-', VIH, '=', NMH,
    '=', NMH_str, 'mV')
print('Noise margin low (NML) = VIL - VOL =', VIL, '-', VOL, '=', NML,
   '=', NML_str, 'mV')


plt.show()
```

A.2 Python script to draw the graph(Transient analysis for propagation delay) from text file.

```
import matplotlib.pyplot as plt


data = []
with open("2.txt", "r") as file:
    skip_first_row = True
    for line in file:
        # Skip the first row
        if skip_first_row:
            skip_first_row = False
            continue
        # Split the line into two columns
        cols = line.strip().split()
        if len(cols) != 2:
            continue
        x, y = cols
        data.append((float(x), float(y)))


half_point = len(data) // 2 + 1
second_graph_start = None
```

```
for i in range(half_point, len(data)):
    if data[i][0] != data[half_point][0]:
        second_graph_start = i
        break

if second_graph_start is None:
    second_graph_start = len(data)

# Split the data into two graphs
graph1_data = data[:half_point - 1]
graph2_data = data[second_graph_start + 1:]


fig, ax = plt.subplots()


max_input_value = max(y for x, y in graph1_data)


tolerance = 0.01  # You can adjust this value based on your data
    characteristics


half_voltage_input = max_input_value / 2
plt.axhline(y=half_voltage_input, color='r', linestyle='--', label=f'V
    = {half_voltage_input:.2f}V')


input_low_to_high_points = []
input_high_to_low_points = []

for i in range(len(graph1_data) - 1):
    x1, y1 = graph1_data[i]
    x2, y2 = graph1_data[i + 1]


    if y1 < half_voltage_input and y2 >= half_voltage_input:
        intersection_x = x1 + (x2 - x1) * (half_voltage_input - y1) / (
            y2 - y1)
        input_low_to_high_points.append((intersection_x,
            half_voltage_input))


    elif y1 >= half_voltage_input and y2 < half_voltage_input:
        intersection_x = x1 + (x2 - x1) * (half_voltage_input - y1) / (
            y2 - y1)
        input_high_to_low_points.append((intersection_x,
            half_voltage_input))


delay = graph2_data[0][0] - graph1_data[0][0] + (graph2_data[1][0] -
    graph2_data[0][0]) / 2

# Find the corresponding intersection points on the output waveform
output_low_to_high_points = []
output_high_to_low_points = []

for i in range(len(graph2_data) - 1):
```

```
    x1, y1 = graph2_data[i]
    x2, y2 = graph2_data[i + 1]

    # Adjust x values for the delay
    x1 += delay
    x2 += delay


    if y1 < half_voltage_input and y2 >= half_voltage_input:
        intersection_x = x1 + (x2 - x1) * (half_voltage_input - y1) / (
            y2 - y1)
        output_low_to_high_points.append((intersection_x,
            half_voltage_input))


    elif y1 >= half_voltage_input and y2 < half_voltage_input:
        intersection_x = x1 + (x2 - x1) * (half_voltage_input - y1) / (
            y2 - y1)
        output_high_to_low_points.append((intersection_x,
            half_voltage_input))


plt.plot([x for x, y in graph1_data], [y for x, y in graph1_data],
    label="Vin")


plt.plot([x for x, y in graph2_data], [y for x, y in graph2_data],
    label="Vout")


if input_low_to_high_points:
    input_low_to_high_x, input_low_to_high_y = zip(*
        input_low_to_high_points)
    plt.scatter(input_low_to_high_x, input_low_to_high_y, marker='^',
        color='green', label='Input Low to High Intersection Points')


if input_high_to_low_points:
    input_high_to_low_x, input_high_to_low_y = zip(*
        input_high_to_low_points)
    plt.scatter(input_high_to_low_x, input_high_to_low_y, marker='v',
        color='blue', label='Input High to Low Intersection Points')

triangles
if output_low_to_high_points:
    output_low_to_high_x, output_low_to_high_y = zip(*
        output_low_to_high_points)
    plt.scatter(output_low_to_high_x, output_low_to_high_y, marker='^',
         color='orange', label='Output Low to High Intersection Points
        ')


if output_high_to_low_points:
    output_high_to_low_x, output_high_to_low_y = zip(*
        output_high_to_low_points)
    plt.scatter(output_high_to_low_x, output_high_to_low_y, marker='v',
         color='purple', label='Output High to Low Intersection Points
        ')
```

```
plt.xlabel("Time[sec]", fontweight='bold')
plt.ylabel("Vout[V], Vin[V]", fontweight='bold')


plt.legend()

plt.xticks(fontsize=12, fontweight='bold')
plt.yticks(fontsize=12, fontweight='bold')
plt.legend(fontsize=10, loc='best')



time_touch_input_low_to_high = [x for x, _ in input_low_to_high_points]
time_touch_output_low_to_high = [x for x, _ in
    output_low_to_high_points]
time_touch_input_high_to_low = [x for x, _ in input_high_to_low_points]
time_touch_output_high_to_low = [x for x, _ in
    output_high_to_low_points]

print("Input Low to High Intersection Points (time):",
    time_touch_input_low_to_high)
print("Output Low to High Intersection Points (time):",
    time_touch_output_low_to_high)
print("Input High to Low Intersection Points (time):",
    time_touch_input_high_to_low)
print("Output High to Low Intersection Points (time):",
    time_touch_output_high_to_low)

print("New Points")

print("o-high to low: ", output_high_to_low_points[0][0])
print("o-low to high: ", output_low_to_high_points[0][0])
print("i-high to low: ", input_high_to_low_points[0][0])
print("i-low to high: ", input_low_to_high_points[0][0])

t_plh = output_low_to_high_points[0][0] - input_low_to_high_points
    [0][0]
t_phl = output_high_to_low_points[0][0] - input_high_to_low_points
    [0][0]

t_plh_n = t_plh * 10**9
t_phl_n = t_phl * 10**9
tn = (t_plh_n + t_phl_n ) / 2

print('t_plh = output_low_to_high_points[0][0] -
    input_low_to_high_points[0][0] =', output_low_to_high_points[0][0],
     '-', input_low_to_high_points[0][0], '=', t_plh, '=', t_plh_n, 'nS
    ')
print('t_phl = output_high_to_low_points[0][0] -
    input_high_to_low_points[0][0] =', output_high_to_low_points[0][0],
     '-', input_high_to_low_points[0][0], '=', t_phl, '=', t_phl_n, 'nS
    ')
print('tn=', tn)
plt.show()
```

A.3 Python script to draw the graph(Transient analysis for average current) from text file for Ring Oscillator.

```
import numpy as np
import matplotlib.pyplot as plt

time, current = np.loadtxt('raw_data.txt', skiprows=1, unpack=True)
average_current = np.trapz(current, time) / (time[-1] - time[0])
print('Average Current:', average_current)

plt.plot(time, current, label='Current vs. Time')
plt.axhline(average_current, color='r', linestyle='--', label='Average
    Current')


plt.xlabel('Time')
plt.ylabel('Current')
plt.legend()


plt.show()
```

A.4 Python script to draw the graph(Transient analysis for average current) from text file.

```
import numpy as np
import matplotlib.pyplot as plt

time, current = np.loadtxt('raw_data.txt', skiprows=1, unpack=True)


average_absolute_current_amp = np.mean(np.abs(current))


average_absolute_current_nanoamp = average_absolute_current_amp * 1e9

average_absolute_current_nanoamp_rounded = round(
    average_absolute_current_nanoamp, 2)

print('Average Absolute Current:',
    average_absolute_current_nanoamp_rounded, 'nA')

plt.plot(time, current, label='Current vs. Time')
plt.axhline(average_absolute_current_amp, color='r', linestyle='--',
    label='Average Current')


plt.xlabel('Time')
plt.ylabel('Current')
plt.legend()

plt.show()
```

B AIMSPICE code

B.1 Static CMOS Full Adder AIMSPICE code

```
CMOS Full adder
.include 90nm_gpdk90nm_tt.cir

.subckt NAND_gate A B out1 1 0
X1 out1 A 1 1 pmos1v w=0.85u l=0.3u
X2 out1 B 1 1 pmos1v w=0.85u l=0.3u
X3 out1 A 6 0 nmos1v w=0.1u l=0.3u
X4 6 B 0 0 nmos1v w=0.1u l=0.3u
.ends NAND_gate

.subckt INVERTER INPUT OUTPUT 1 0
X1 OUTPUT INPUT 1 1 pmos1v w=100n l=100n
X2 OUTPUT INPUT 0 0 nmos1v w=100n l=100n
.ends INVERTER

.subckt XOR_GATE A B OUT4 1 0
X_INVERTER_1 A A1 1 0 INVERTER
X_INVERTER_2 B B1 1 0 INVERTER

X_NAND_gate_1 A B1 OUT2 1 0 NAND_gate
X_NAND_gate_2 A1 B OUT3 1 0 NAND_gate
X_NAND_gate_3 OUT2 OUT3 OUT4 1 0 NAND_gate

.ends XOR_GATE

.subckt Full_Adder A B C Sum carry 1 0
*SUM
X_XOR_GATE_1 A B OUT4 1 0 XOR_GATE
X_XOR_GATE_2 OUT4 C Sum 1 0 XOR_GATE

*Carry
X_NAND_gate_4 A B OUT5 1 0 NAND_gate
X_NAND_gate_5 C OUT4 OUT6 1 0 NAND_gate
X_NAND_gate_6 OUT5 OUT6 carry 1 0 NAND_gate

.ends Full_Adder

vdd 1 0 dc 180m
vin_A A 0 dc 0 pulse(0 180m 0 0.1ns 0.1ns 10ns 20ns)
vin_B B 0 dc 0 pulse(180m 0 0 0.1ns 0.1ns 10ns 20ns)
vin_C C 0 dc 0 pulse(180m 0 0 0.1ns 0.1ns 10ns 20ns)

X_Full_Adder A B C Sum carry 1 0 Full_Adder

.plot V(Sum)!0.205
.plot V(carry)!0.205
```

B.2 Schmitt trigger CMOS Full Adder AIMSPICE code

```
CMOS Schmitt trigger Full adder
.include 90nm_gpdk90nm_TT.cir

.subckt ST_NAND_gate A B out1 1 0

X1 3 A 1 1 pmos1v w=0.45u l=0.2u
X2 3 B 1 1 pmos1v w=0.45u l=0.2u
X3 out1 A 3 1 pmos1v w=0.45u l=0.2u
```

```
X4 out1 B 3 1 pmos1v w=0.45u l=0.2u
X5 0 out1 3 1 pmos1v w=0.1u l=0.2u

X6 out1 A 6 0 nmos1v w=0.1u l=0.2u
X7 6 B 7 0 nmos1v w=0.1u l=0.2u
X8 7 B 8 0 nmos1v w=0.1u l=0.2u
X9 8 A 0 0 nmos1v w=0.1u l=0.2u
X10 1 out1 7 0 nmos1v w=0.1u l=0.2u

.ends ST_NAND_gate

.subckt INVERTER INPUT OUTPUT 1 0

X1 2 INPUT 1 1 pmos1v w=0.1u l=0.2u
X2 OUTPUT INPUT 2 1 pmos1v w=0.1u l=0.2u

X4 OUTPUT INPUT 5 0 nmos1v w=0.1u l=0.2u
X5 5 INPUT 0 0 nmos1v w=0.1u l=0.2u

.ends INVERTER

.subckt XOR_GATE A B OUT4 1 0
X_INVERTER_1 A A1 1 0 INVERTER
X_INVERTER_2 B B1 1 0 INVERTER

X_ST_NAND_gate_1 A B1 OUT2 1 0 ST_NAND_gate
X_ST_NAND_gate_2 A1 B OUT3 1 0 ST_NAND_gate
X_ST_NAND_gate_3 OUT2 OUT3 OUT4 1 0 ST_NAND_gate

.ends XOR_GATE

.subckt Full_Adder A B C Sum carry 1 0
*SUM
X_XOR_GATE_1 A B OUT4 1 0 XOR_GATE
X_XOR_GATE_2 OUT4 C Sum 1 0 XOR_GATE

*Carry
X_ST_NAND_gate_4 A B OUT5 1 0 ST_NAND_gate
X_ST_NAND_gate_5 C OUT4 OUT6 1 0 ST_NAND_gate
X_ST_NAND_gate_6 OUT5 OUT6 carry 1 0 ST_NAND_gate

.ends Full_Adder

vdd 1 0 dc 180m
vin_A A 0 dc 0 pulse(0 180m 0 0.1ns 0.1ns 10ns 20ns)
vin_B B 0 dc 0 pulse(180m 0 0 0.1ns 0.1ns 10ns 20ns)
vin_C C 0 dc 0 pulse(180m 0 0 0.1ns 0.1ns 10ns 20ns)

X_Full_Adder A B C Sum carry 1 0 Full_Adder
```

B.3 Full Adder using Static CMOS XOR gate : AIMSPICE code

```
CMOS Full adder Based of simple XOR
.include 90nm_gpdk\gpdk90nm_ff.cir


.subckt INVERTER INPUT OUTPUT 1 0
        X1 OUTPUT INPUT 1 1 pmos1v w=1.1u l=0.3u
        X2 OUTPUT INPUT 0 0 nmos1v w=0.1u l=0.3u
.ends INVERTER
```

```
.subckt NAND_gate A B out1 1 0

X1 out1 A 1 1 pmos1v w=1.1u l=0.3u
X2 out1 B 1 1 pmos1v w=1.1u l=0.3u
X3 out1 A 6 0 nmos1v w=0.1u l=0.3u
X4 6 B 0 0 nmos1v w=0.1u l=0.3u

.ends NAND_gate

.subckt XOR_GATE A B out 1 0
        X_INVERTER_1 A A1 1 0 INVERTER
        X_INVERTER_2 B B1 1 0 INVERTER

        X1 3 A1 1 1 pmos1v w=1.1u l=0.3u
        X2 5 A 1 1 pmos1v w=1.1u l=0.3u
        X3 out B 3 1 pmos1v w=1.1u l=0.3u
        X4 out B1 5 1 pmos1v w=1.1u l=0.3u

        X5 out A1 7 0 nmos1v w=100n l=300n
        X6 out A 8 0 nmos1v w=100n l=300n
        X7 7 B1 0 0 nmos1v w=100n l=300n
        X8 8 B 0 0 nmos1v w=100n l=300n

.ends XOR_GATE


.subckt FA_xor A B C Sum carry 1 0

        X_XOR_GATE_1 A B out 1 0 XOR_GATE
        X_XOR_GATE_2 C out Sum 1 0 XOR_GATE

        X_NAND_gate_1 A B OUT2 1 0 NAND_gate
        X_NAND_gate_2 C out OUT3 1 0 NAND_gate
        X_NAND_gate_3 OUT3 OUT2 carry 1 0 NAND_gate

.ends FA_xor


vdd 1 0 dc 180m

vin_A A 0 dc 0 pulse(180m 0 0 0.1ns 0.1ns 10Us 20us)
vin_B B 0 dc 0 pulse(180m 0 0 0.1ns 0.1ns 10us 20us)
vin_C C 0 dc 0 pulse(180m 0 0 0.1ns 0.1ns 10us 20us)

X_FA_xor A B C Sum carry 1 0 FA_xor

.plot I(vdd) !0.205
```

B.4 Full Adder using Static CMOS XOR gate : AIMSPICE code

```
Schmitt trigger Full adder Based of ST XOR type2
.include 90nm_gpdk\gpdk90nm_ff.cir


.subckt INVERTER INPUT OUTPUT 1 0
```

```
        X1 2 INPUT 1 1 pmos1v w=0.1u l=0.2u
        X2 OUTPUT INPUT 2 1 pmos1v w=0.1u l=0.2u

        X4 OUTPUT INPUT 5 0 nmos1v w=0.1u l=0.2u
        X5 5 INPUT 0 0 nmos1v w=0.1u l=0.2u

.ends INVERTER



.subckt ST_NAND_gate A B out1 1 0
        X1 3 A 1 1 pmos1v w=0.45u l=0.2u
        X2 3 B 1 1 pmos1v w=0.45u l=0.2u
        X3 out1 A 3 1 pmos1v w=0.45u l=0.2u
        X4 out1 B 3 1 pmos1v w=0.45u l=0.2u
        X5 0 out1 3 1 pmos1v w=0.45u l=0.2u

        X6 out1 A 6 0 nmos1v w=0.1u l=0.2u
        X7 6 B 7 0 nmos1v w=0.1u l=0.2u
        X8 7 B 8 0 nmos1v w=0.1u l=0.2u
        X9 8 A 0 0 nmos1v w=0.1u l=0.2u
        X10 1 out1 7 0 nmos1v w=0.1u l=0.2u
.ends ST_NAND_gate


.subckt ST_XOR_GATE A B out1 1 0
        X_INVERTER_1 A A1 1 0 INVERTER
        X_INVERTER_2 B B1 1 0 INVERTER

        X1 3 A1 1 1 pmos1v w=0.7u l=0.2u
        X2 3 B 1 1 pmos1v w=0.7u l=0.2u
        X3 4 A 3 1 pmos1v w=0.7u l=0.2u
        X4 4 B1 3 1 pmos1v w=0.7u l=0.2u

*Feedback PMOS
        X9 0 out 4 1 pmos1v w=0.7u l=0.2u

        X5 5 A 4 1 pmos1v w=0.7u l=0.2u
        X6 5 B1 4 1 pmos1v w=0.7u l=0.2u
        X7 out A1 5 1 pmos1v w=0.7u l=0.2u
        X8 out B 5 1 pmos1v w=0.7u l=0.2u


        X10 out A1 6 0 nmos1v w=100n l=200n
        X11 6 B 7 0 nmos1v w=100n l=200n
        X12 7 A1 8 0 nmos1v w=100n l=200n
        X13 8 B 0 0 nmos1v w=100n l=200n

        X14 out A 9 0 nmos1v w=100n l=200n
        X15 9 B1 7 0 nmos1v w=100n l=200n
*Feedback NMOS
        X16 1 out 7 0 nmos1v w=100n l=200n

        X17 7 A 10 0 nmos1v w=100n l=200n
        X18 10 B1 0 0 nmos1v w=100n l=200n

        X_INVERTER_3 out out1 1 0 INVERTER
```

```
.ends ST_XOR_GATE

.subckt ST_FA_xor A B C Sum carry 1 0

        X_ST_XOR_GATE_1 A B out1 1 0 ST_XOR_GATE
        X_ST_XOR_GATE_2 C out1 Sum 1 0 ST_XOR_GATE

        X_ST_NAND_gate_1 A B OUT2 1 0 ST_NAND_gate
        X_ST_NAND_gate_2 C OUT1 OUT3 1 0 ST_NAND_gate
        X_ST_NAND_gate_3 OUT3 OUT2 carry 1 0 ST_NAND_gate

.ends ST_FA_xor

vdd 1 0 dc 180m


vin_A A 0 dc 0 pulse(180m 0 0 0.1ns 0.1ns 10us 20us)
vin_B B 0 dc 0 pulse(180m 0 0 0.1ns 0.1ns 10us 20us)
vin_C C 0 dc 0 pulse(180m 0 0 0.1ns 0.1ns 10us 20us)

X_ST_FA_xor_1 A B C Sum carry 1 0 ST_FA_xor

.plot I(vdd) !0.305
```

C Ring: AIMSPICE code

C.1 Ring: Full Adder using Static CMOS NAND gate AIMSPICE code

```
CMOS Full adder BASED ON NAND
.include 90nm_gpdk\gpdk90nm_FF.cir

.subckt NAND_gate A B out1 1 0
X1 out1 A 1 1 pmos1v w=0.85u l=0.3u
X2 out1 B 1 1 pmos1v w=0.85u l=0.3u
X3 out1 A 6 0 nmos1v w=0.1u l=0.3u
X4 6 B 0 0 nmos1v w=0.1u l=0.3u
.ends NAND_gate


.subckt INVERTER INPUT OUTPUT 1 0
        X1 OUTPUT INPUT 1 1 pmos1v w=0.1u l=0.1u
        X2 OUTPUT INPUT 0 0 nmos1v w=0.1u l=0.1u
.ends INVERTER

.subckt XOR_GATE A B OUT4 1 0
        X_INVERTER_1 A A1 1 0 INVERTER
        X_INVERTER_2 B B1 1 0 INVERTER

        X_NAND_gate_1 A B1 OUT2 1 0 NAND_gate
        X_NAND_gate_2 A1 B OUT3 1 0 NAND_gate
        X_NAND_gate_3 OUT2 OUT3 OUT4 1 0 NAND_gate

.ends XOR_GATE

.subckt Full_Adder A B C Sum carry 1 0
```

```
        *SUM
        X_XOR_GATE_1 A B OUT4 1 0 XOR_GATE
        X_XOR_GATE_2 OUT4 C Sum 1 0 XOR_GATE

        *Carry
        X_NAND_gate_4 A B OUT5 1 0 NAND_gate
        X_NAND_gate_5 C OUT4 OUT6 1 0 NAND_gate
        X_NAND_gate_6 OUT5 OUT6 carry 1 0 NAND_gate

.ends Full_Adder

.subckt Ring_Full_Adder 0 1 Sum3 Sum3 carry3 1 0
X_Full_Adder_1 0 1 Sum3 Sum1 carry1 1 0 Full_Adder
X_Full_Adder_2 0 1 Sum1 Sum2 carry2 1 0 Full_Adder
X_Full_Adder_3 0 1 Sum2 Sum3 carry3 1 0 Full_Adder
.ends Ring_Full_Adder


X_Ring_Full_Adder 0 1 Sum3 Sum3 carry3 1 0 Ring_Full_Adder


*test_bench
vdd 1 0 dc 500m
.ic v(Sum3)= 0.28
.plot I(vdd)!0.205
```

C.2 Ring: Full Adder using Schmitt trigger CMOS NAND gate AIMSPICE code

```
CMOS Schmitt trigger Full adder
.include 90nm_gpdk\gpdk90nm_TT.cir

.subckt ST_NAND_gate A B out1 1 0

        X1 3 A 1 1 pmos1v w=0.45u l=0.2u
        X2 3 B 1 1 pmos1v w=0.45u l=0.2u
        X3 out1 A 3 1 pmos1v w=0.45u l=0.2u
        X4 out1 B 3 1 pmos1v w=0.45u l=0.2u
        X5 0 out1 3 1 pmos1v w=0.45u l=0.2u

        X6 out1 A 6 0 nmos1v w=0.1u l=0.2u
        X7 6 B 7 0 nmos1v w=0.1u l=0.2u
        X8 7 B 8 0 nmos1v w=0.1u l=0.2u
        X9 8 A 0 0 nmos1v w=0.1u l=0.2u
        X10 1 out1 7 0 nmos1v w=0.1u l=0.2u

.ends ST_NAND_gate


.subckt INVERTER INPUT OUTPUT 1 0

        X1 2 INPUT 1 1 pmos1v w=0.1u l=0.2u
        X2 OUTPUT INPUT 2 1 pmos1v w=0.1u l=0.2u

        X4 OUTPUT INPUT 5 0 nmos1v w=0.1u l=0.2u
        X5 5 INPUT 0 0 nmos1v w=0.1u l=0.2u
```

```
.ends INVERTER


.subckt XOR_GATE A B OUT4 1 0
        X_INVERTER_1 A A1 1 0 INVERTER
        X_INVERTER_2 B B1 1 0 INVERTER

        X_ST_NAND_gate_1 A B1 OUT2 1 0 ST_NAND_gate
        X_ST_NAND_gate_2 A1 B OUT3 1 0 ST_NAND_gate
        X_ST_NAND_gate_3 OUT2 OUT3 OUT4 1 0 ST_NAND_gate

.ends XOR_GATE

.subckt Full_Adder A B C Sum carry 1 0
        *SUM
        X_XOR_GATE_1 A B OUT4 1 0 XOR_GATE
        X_XOR_GATE_2 C OUT4 Sum 1 0 XOR_GATE

        *Carry
        X_ST_NAND_gate_4 A B OUT5 1 0 ST_NAND_gate
        X_ST_NAND_gate_5 C OUT4 OUT6 1 0 ST_NAND_gate
        X_ST_NAND_gate_6 OUT5 OUT6 carry 1 0 ST_NAND_gate

.ends Full_Adder

.subckt Ring_Full_Adder 0 1 Sum3 Sum3 carry3 1 0
X_Full_Adder_1 0 1 Sum3 Sum1 carry1 1 0 Full_Adder
X_Full_Adder_2 0 1 Sum1 Sum2 carry2 1 0 Full_Adder
X_Full_Adder_3 0 1 Sum2 Sum3 carry3 1 0 Full_Adder
.ends Ring_Full_Adder


X_Ring_Full_Adder 0 1 Sum3 Sum3 carry3 1 0 Ring_Full_Adder

*test_bench
vdd 1 0 dc 180m
.ic v(Sum3)= 0.16
.plot I(Vdd) !0.205
```

C.3 Ring: Full Adder using static CMOS XOR gate AIMSPICE code

```
.include 90nm_gpdk\gpdk90nm_SF.cir


.subckt INVERTER INPUT OUTPUT 1 0
        X1 OUTPUT INPUT 1 1 pmos1v w=1.1u l=0.3u
        X2 OUTPUT INPUT 0 0 nmos1v w=0.1u l=0.3u
.ends INVERTER

.subckt NAND_gate A B out1 1 0

X1 out1 A 1 1 pmos1v w=1.1u l=0.3u
X2 out1 B 1 1 pmos1v w=1.1u l=0.3u
X3 out1 A 6 0 nmos1v w=0.1u l=0.3u
X4 6 B 0 0 nmos1v w=0.1u l=0.3u
```

```
.ends NAND_gate

.subckt XOR_GATE A B out 1 0
        X_INVERTER_1 A A1 1 0 INVERTER
        X_INVERTER_2 B B1 1 0 INVERTER

        X1 3 A1 1 1 pmos1v w=1.1u l=0.3u
        X2 5 A 1 1 pmos1v w=1.1u l=0.3u
        X3 out B 3 1 pmos1v w=1.1u l=0.3u
        X4 out B1 5 1 pmos1v w=1.1u l=0.3u


        X5 out A1 7 0 nmos1v w=100n l=300n
        X6 out A 8 0 nmos1v w=100n l=300n
        X7 7 B1 0 0 nmos1v w=100n l=300n
        X8 8 B 0 0 nmos1v w=100n l=300n

.ends XOR_GATE


.subckt FA_xor A B C Sum carry 1 0

        X_XOR_GATE_1 A B out 1 0 XOR_GATE
        X_XOR_GATE_2 C out Sum 1 0 XOR_GATE

        X_NAND_gate_1 A B OUT2 1 0 NAND_gate
        X_NAND_gate_2 C out OUT3 1 0 NAND_gate
        X_NAND_gate_3 OUT3 OUT2 carry 1 0 NAND_gate

.ends FA_xor

.subckt Ring_Full_Adder 0 1 Sum3 Sum3 carry3 1 0
X_FA_xor_1 0 1 Sum3 Sum1 carry1 1 0 FA_xor
X_FA_xor_2 0 1 Sum1 Sum2 carry2 1 0 FA_xor
X_FA_xor_3 0 1 Sum2 Sum3 carry3 1 0 FA_xor
.ends Ring_Full_Adder

X_Ring_Full_Adder 0 1 Sum3 Sum3 carry3 1 0 Ring_Full_Adder


vdd 1 0 dc 660m
.ic v(Sum3)= 0.38
.plot I(vdd) !0.205
.plot V(Sum3) !0.205
```

C.4 Ring: Full Adder using Schmitt trigger CMOS XOR gate AIMSPICE code

```
.include 90nm_gpdk\gpdk90nm_ff.cir


.subckt INVERTER INPUT OUTPUT 1 0
        X1 2 INPUT 1 1 pmos1v w=0.1u l=0.2u
        X2 OUTPUT INPUT 2 1 pmos1v w=0.1u l=0.2u

        X4 OUTPUT INPUT 5 0 nmos1v w=0.1u l=0.2u
        X5 5 INPUT 0 0 nmos1v w=0.1u l=0.2u
```

```
.ends INVERTER

.subckt ST_NAND_gate A B out1 1 0

        X1 3 A 1 1 pmos1v w=0.45u l=0.2u
        X2 3 B 1 1 pmos1v w=0.45u l=0.2u
        X3 out1 A 3 1 pmos1v w=0.45u l=0.2u
        X4 out1 B 3 1 pmos1v w=0.45u l=0.2u
        X5 0 out1 3 1 pmos1v w=0.45u l=0.2u

        X6 out1 A 6 0 nmos1v w=0.1u l=0.2u
        X7 6 B 7 0 nmos1v w=0.1u l=0.2u
        X8 7 B 8 0 nmos1v w=0.1u l=0.2u
        X9 8 A 0 0 nmos1v w=0.1u l=0.2u
        X10 1 out1 7 0 nmos1v w=0.1u l=0.2u
.ends ST_NAND_gate


.subckt ST_XOR_GATE A B out1 1 0
        X_INVERTER_1 A A1 1 0 INVERTER
        X_INVERTER_2 B B1 1 0 INVERTER

        X1 3 A1 1 1 pmos1v w=0.7u l=0.2u
        X2 3 B 1 1 pmos1v w=0.7u l=0.2u
        X3 4 A 3 1 pmos1v w=0.7u l=0.2u
        X4 4 B1 3 1 pmos1v w=0.7u l=0.2u

*Feedback PMOS
        X9 0 out 4 1 pmos1v w=0.7u l=0.2u

        X5 5 A 4 1 pmos1v w=0.7u l=0.2u
        X6 5 B1 4 1 pmos1v w=0.7u l=0.2u
        X7 out A1 5 1 pmos1v w=0.7u l=0.2u
        X8 out B 5 1 pmos1v w=0.7u l=0.2u

        X10 out A1 6 0 nmos1v w=100n l=200n
        X11 6 B 7 0 nmos1v w=100n l=200n
        X12 7 A1 8 0 nmos1v w=100n l=200n
        X13 8 B 0 0 nmos1v w=100n l=200n

        X14 out A 9 0 nmos1v w=100n l=200n
        X15 9 B1 7 0 nmos1v w=100n l=200n
*Feedback NMOS
        X16 1 out 7 0 nmos1v w=100n l=200n

        X17 7 A 10 0 nmos1v w=100n l=200n
        X18 10 B1 0 0 nmos1v w=100n l=200n

        X_INVERTER_3 out out1 1 0 INVERTER

.ends ST_XOR_GATE

.subckt ST_FA_xor A B C Sum carry 1 0
        X_ST_XOR_GATE_1 A B out1 1 0 ST_XOR_GATE
        X_ST_XOR_GATE_2 C out1 Sum 1 0 ST_XOR_GATE

        X_ST_NAND_gate_1 A B OUT2 1 0 ST_NAND_gate
        X_ST_NAND_gate_2 C OUT1 OUT3 1 0 ST_NAND_gate
```

```
        X_ST_NAND_gate_3 OUT3 OUT2 carry 1 0 ST_NAND_gate

.ends ST_FA_xor

.subckt Ring_Full_Adder 0 1 Sum3 Sum3 carry3 1 0
X_ST_FA_xor_1 0 1 Sum3 Sum1 carry1 1 0 ST_FA_xor
X_ST_FA_xor_2 0 1 Sum1 Sum2 carry2 1 0 ST_FA_xor
X_ST_FA_xor_3 0 1 Sum2 Sum3 carry3 1 0 ST_FA_xor

.ends Ring_Full_Adder


X_Ring_Full_Adder 0 1 Sum3 Sum3 carry3 1 0 Ring_Full_Adder

vdd 1 0 dc 180m
.ic v(Sum3)= 0.18
.plot V(Sum3) !0.305
.plot I(vdd) !0.305
```

D RCA: AIMSPICE code

D.1 RCA: Full Adder using static CMOS NAND gate AIMSPICE code

```
CMOS Full adder BASED ON NAND
.include 90nm_gpdk\gpdk90nm_TT.cir

.subckt NAND_gate A B out1 1 0
X1 out1 A 1 1 pmos1v w=0.85u l=0.3u
X2 out1 B 1 1 pmos1v w=0.85u l=0.3u
X3 out1 A 6 0 nmos1v w=0.1u l=0.3u
X4 6 B 0 0 nmos1v w=0.1u l=0.3u
.ends NAND_gate


.subckt INVERTER INPUT OUTPUT 1 0
        X1 OUTPUT INPUT 1 1 pmos1v w=0.1u l=0.1u
        X2 OUTPUT INPUT 0 0 nmos1v w=0.1u l=0.1u
.ends INVERTER

.subckt XOR_GATE A B OUT4 1 0
        X_INVERTER_1 A A1 1 0 INVERTER
        X_INVERTER_2 B B1 1 0 INVERTER

        X_NAND_gate_1 A B1 OUT2 1 0 NAND_gate
        X_NAND_gate_2 A1 B OUT3 1 0 NAND_gate
        X_NAND_gate_3 OUT2 OUT3 OUT4 1 0 NAND_gate

.ends XOR_GATE

.subckt Full_Adder A B C Sum carry 1 0
        *SUM
        X_XOR_GATE_1 A B OUT4 1 0 XOR_GATE
        X_XOR_GATE_2 OUT4 C Sum 1 0 XOR_GATE

        *Carry
```

```
        X_NAND_gate_4 A B OUT5 1 0 NAND_gate
        X_NAND_gate_5 C OUT4 OUT6 1 0 NAND_gate
        X_NAND_gate_6 OUT5 OUT6 carry 1 0 NAND_gate

.ends Full_Adder

.subckt RC_adder A0 B0 cin Sum3 carry3 1 0
X_Full_Adder_1 A0 B0 cin Sum0 C0 1 0 Full_Adder
X_Full_Adder_2 A0 B0 C0 Sum1 C1 1 0 Full_Adder
X_Full_Adder_3 A0 B0 C1 Sum2 C2 1 0 Full_Adder
X_Full_Adder_4 A0 B0 C2 Sum3 C3 1 0 Full_Adder
.ends RC_adder

X_RC_adder A0 B0 cin Sum3 carry3 1 0 RC_adder

*test_bench
vdd 1 0 dc 700m
vin_A0 A0 0 dc 0 pulse(0 700m 0 0.2ns 0.2ns 10us 20us)
vin_B0 B0 0 dc 0 pulse(0 700m 0 0.2ns 0.2ns 10us 20us)
vin_cin cin 0 dc 0 pulse(0 700m 0 0.2ns 0.2ns 10us 20us)


*.plot V(A0) V(Sum3) !0.205
.plot I(vdd)!0.205
```

D.2 RCA: Full Adder using Schmitt trigger CMOS NAND gate AIMSPICE code

```
.include 90nm_gpdk\gpdk90nm_TT.cir

.subckt ST_NAND_gate A B out1 1 0

        X1 3 A 1 1 pmos1v w=0.45u l=0.2u
        X2 3 B 1 1 pmos1v w=0.45u l=0.2u
        X3 out1 A 3 1 pmos1v w=0.45u l=0.2u
        X4 out1 B 3 1 pmos1v w=0.45u l=0.2u
        X5 0 out1 3 1 pmos1v w=0.45u l=0.2u

        X6 out1 A 6 0 nmos1v w=0.1u l=0.2u
        X7 6 B 7 0 nmos1v w=0.1u l=0.2u
        X8 7 B 8 0 nmos1v w=0.1u l=0.2u
        X9 8 A 0 0 nmos1v w=0.1u l=0.2u
        X10 1 out1 7 0 nmos1v w=0.1u l=0.2u

.ends ST_NAND_gate


.subckt INVERTER INPUT OUTPUT 1 0

        X1 2 INPUT 1 1 pmos1v w=0.1u l=0.2u
        X2 OUTPUT INPUT 2 1 pmos1v w=0.1u l=0.2u

        X4 OUTPUT INPUT 5 0 nmos1v w=0.1u l=0.2u
        X5 5 INPUT 0 0 nmos1v w=0.1u l=0.2u

.ends INVERTER
```

```
.subckt XOR_GATE A B OUT4 1 0
        X_INVERTER_1 A A1 1 0 INVERTER
        X_INVERTER_2 B B1 1 0 INVERTER

        X_ST_NAND_gate_1 A B1 OUT2 1 0 ST_NAND_gate
        X_ST_NAND_gate_2 A1 B OUT3 1 0 ST_NAND_gate
        X_ST_NAND_gate_3 OUT2 OUT3 OUT4 1 0 ST_NAND_gate

.ends XOR_GATE

.subckt Full_Adder A B C Sum carry 1 0
        *SUM
        X_XOR_GATE_1 A B OUT4 1 0 XOR_GATE
        X_XOR_GATE_2 C OUT4 Sum 1 0 XOR_GATE

        *Carry
        X_ST_NAND_gate_4 A B OUT5 1 0 ST_NAND_gate
        X_ST_NAND_gate_5 C OUT4 OUT6 1 0 ST_NAND_gate
        X_ST_NAND_gate_6 OUT5 OUT6 carry 1 0 ST_NAND_gate

.ends Full_Adder


.subckt RC_adder A0 B0 cin Sum3 carry3 1 0
X_Full_Adder_1 A0 B0 cin Sum0 C0 1 0 Full_Adder
X_Full_Adder_2 A0 B0 C0 Sum1 C1 1 0 Full_Adder
X_Full_Adder_3 A0 B0 C1 Sum2 C2 1 0 Full_Adder
X_Full_Adder_4 A0 B0 C2 Sum3 C3 1 0 Full_Adder
.ends RC_adder

X_RC_adder A0 B0 cin Sum3 carry3 1 0 RC_adder


vdd 1 0 dc 180m

vin_A0 A0 0 dc 0 pulse(0 180m 0 0.2ns 0.2ns 10us 20us)
vin_B0 B0 0 dc 0 pulse(0 18m 0 0.2ns 0.2ns 10us 20us)
vin_cin cin 0 dc 0 pulse(0 180m 0 0.2ns 0.2ns 10us 20us)


.plot I(Vdd) !0.205
```

D.3 RCA: Full Adder using static CMOS XOR gate AIMSPICE code

```
.include 90nm_gpdk\gpdk90nm_TT.cir


.subckt INVERTER INPUT OUTPUT 1 0
        X1 OUTPUT INPUT 1 1 pmos1v w=1.1u l=0.3u
        X2 OUTPUT INPUT 0 0 nmos1v w=0.1u l=0.3u
.ends INVERTER

.subckt NAND_gate A B out1 1 0

X1 out1 A 1 1 pmos1v w=1.1u l=0.3u
X2 out1 B 1 1 pmos1v w=1.1u l=0.3u
```

```
X3 out1 A 6 0 nmos1v w=0.1u l=0.3u
X4 6 B 0 0 nmos1v w=0.1u l=0.3u

.ends NAND_gate

.subckt XOR_GATE A B out 1 0
        X_INVERTER_1 A A1 1 0 INVERTER
        X_INVERTER_2 B B1 1 0 INVERTER

        X1 3 A1 1 1 pmos1v w=1.1u l=0.3u
        X2 5 A 1 1 pmos1v w=1.1u l=0.3u
        X3 out B 3 1 pmos1v w=1.1u l=0.3u
        X4 out B1 5 1 pmos1v w=1.1u l=0.3u


        X5 out A1 7 0 nmos1v w=100n l=300n
        X6 out A 8 0 nmos1v w=100n l=300n
        X7 7 B1 0 0 nmos1v w=100n l=300n
        X8 8 B 0 0 nmos1v w=100n l=300n

.ends XOR_GATE

.subckt FA_xor A B C Sum carry 1 0

        X_XOR_GATE_1 A B out 1 0 XOR_GATE
        X_XOR_GATE_2 C out Sum 1 0 XOR_GATE

        X_NAND_gate_1 A B OUT2 1 0 NAND_gate
        X_NAND_gate_2 C out OUT3 1 0 NAND_gate
        X_NAND_gate_3 OUT3 OUT2 carry 1 0 NAND_gate

.ends FA_xor

.subckt RC_adder A0 B0 cin Sum3 carry3 1 0
X_FA_xor_1 A0 B0 cin Sum0 C0 1 0 FA_xor
X_FA_xor_2 A0 B0 C0 Sum1 C1 1 0 FA_xor
X_FA_xor_3 A0 B0 C1 Sum2 C2 1 0 FA_xor
X_FA_xor_4 A0 B0 C2 Sum3 C3 1 0 FA_xor
.ends RC_adder

X_RC_adder A0 B0 cin Sum3 carry3 1 0 RC_adder


vdd 1 0 dc 340m
vin_A0 A0 0 dc 0 pulse(0 340m 0 0.2ns 0.2ns 10us 20us)
vin_B0 B0 0 dc 0 pulse(0 340m 0 0.2ns 0.2ns 10us 20us)
vin_cin cin 0 dc 0 pulse(0 340m 0 0.2ns 0.2ns 10us 20us)

.plot V(A0) V(Sum3) !0.205
.plot I(vdd)!0.205
```

D.4 RCA: Full Adder using Schmitt trigger CMOS XOR gate AIMSPICE code

```
.include 90nm_gpdk\gpdk90nm_TT.cir
```

```
.subckt INVERTER INPUT OUTPUT 1 0
        X1 2 INPUT 1 1 pmos1v w=0.1u l=0.2u
        X2 OUTPUT INPUT 2 1 pmos1v w=0.1u l=0.2u

        X4 OUTPUT INPUT 5 0 nmos1v w=0.1u l=0.2u
        X5 5 INPUT 0 0 nmos1v w=0.1u l=0.2u

.ends INVERTER

.subckt ST_NAND_gate A B out1 1 0

        X1 3 A 1 1 pmos1v w=0.45u l=0.2u
        X2 3 B 1 1 pmos1v w=0.45u l=0.2u
        X3 out1 A 3 1 pmos1v w=0.45u l=0.2u
        X4 out1 B 3 1 pmos1v w=0.45u l=0.2u
        X5 0 out1 3 1 pmos1v w=0.45u l=0.2u

        X6 out1 A 6 0 nmos1v w=0.1u l=0.2u
        X7 6 B 7 0 nmos1v w=0.1u l=0.2u
        X8 7 B 8 0 nmos1v w=0.1u l=0.2u
        X9 8 A 0 0 nmos1v w=0.1u l=0.2u
        X10 1 out1 7 0 nmos1v w=0.1u l=0.2u
.ends ST_NAND_gate

.subckt ST_XOR_GATE A B out1 1 0
        X_INVERTER_1 A A1 1 0 INVERTER
        X_INVERTER_2 B B1 1 0 INVERTER

        X1 3 A1 1 1 pmos1v w=0.7u l=0.2u
        X2 3 B 1 1 pmos1v w=0.7u l=0.2u
        X3 4 A 3 1 pmos1v w=0.7u l=0.2u
        X4 4 B1 3 1 pmos1v w=0.7u l=0.2u

*Feedback PMOS
        X9 0 out 4 1 pmos1v w=0.7u l=0.2u

        X5 5 A 4 1 pmos1v w=0.7u l=0.2u
        X6 5 B1 4 1 pmos1v w=0.7u l=0.2u
        X7 out A1 5 1 pmos1v w=0.7u l=0.2u
        X8 out B 5 1 pmos1v w=0.7u l=0.2u

        X10 out A1 6 0 nmos1v w=100n l=200n
        X11 6 B 7 0 nmos1v w=100n l=200n
        X12 7 A1 8 0 nmos1v w=100n l=200n
        X13 8 B 0 0 nmos1v w=100n l=200n

        X14 out A 9 0 nmos1v w=100n l=200n
        X15 9 B1 7 0 nmos1v w=100n l=200n
*Feedback NMOS
        X16 1 out 7 0 nmos1v w=100n l=200n

        X17 7 A 10 0 nmos1v w=100n l=200n
        X18 10 B1 0 0 nmos1v w=100n l=200n

        X_INVERTER_3 out out1 1 0 INVERTER

.ends ST_XOR_GATE
```

```
.subckt ST_FA_xor A B C Sum carry 1 0

        X_ST_XOR_GATE_1 A B out1 1 0 ST_XOR_GATE
        X_ST_XOR_GATE_2 C out1 Sum 1 0 ST_XOR_GATE


        X_ST_NAND_gate_1 A B OUT2 1 0 ST_NAND_gate
        X_ST_NAND_gate_2 C OUT1 OUT3 1 0 ST_NAND_gate
        X_ST_NAND_gate_3 OUT3 OUT2 carry 1 0 ST_NAND_gate

.ends ST_FA_xor

.subckt RC_adder A0 B0 cin Sum3 carry3 1 0
X_ST_FA_xor_1 A0 B0 cin Sum0 C0 1 0 ST_FA_xor
X_ST_FA_xor_2 A0 B0 C0 Sum1 C1 1 0 ST_FA_xor
X_ST_FA_xor_3 A0 B0 C1 Sum2 C2 1 0 ST_FA_xor
X_ST_FA_xor_4 A0 B0 C2 Sum3 C3 1 0 ST_FA_xor
.ends RC_adder

X_RC_adder A0 B0 cin Sum3 carry3 1 0 RC_adder

vdd 1 0 dc 680m

vin_A0 A0 0 dc 0 pulse(0 680m 0 0.2ns 0.2ns 10us 20us)
vin_B0 B0 0 dc 0 pulse(0 680m 0 0.2ns 0.2ns 10us 20us)
vin_cin cin 0 dc 0 pulse(0 680m 0 0.2ns 0.2ns 10us 20us)

.plot V(A0) V(Sum3) !0.205
.plot I(Vdd) !0.205
```

E Results of Ring Oscillator in tabular form:

E.1 Ring: static CMOS Nand gate and Inverter

Table 18: Ring: FA using static CMOS Nand gate and Inverter

Voltage(V)	Temp(°C)	Corner	Pro. delay(nS)	I(Vdd)nA	P=VI (nW)	PDP (aJ)	EDP(aJ)*(nS)
0.16	27	SS	323.09	23.35	3.73	1207.06	389990.38
0.18	27	SS	167.29	31.93	5.74	961.48	160846.41
0.20	27	SS	114.23	46.99	9.39	1073.53	122629.73
0.22	27	SS	71.95	70.14	15.43	1110.24	79882.204
0.24	27	SS	52.88	108.38	26.01	1375.47	72734.97
0.26	27	SS	39.34	158.63	41.24	1622.53	63830.37
0.28	27	SS	26.31	228.64	64.01	1684.34	44315.12
0.30	27	SS	19.18	322.59	96.77	1856.18	35601.58
0.32	27	SS	15.35	441.6	141.31	2169.13	33296.28
0.34	27	SS	12.79	597.79	203.24	2599.54	33248.23
0.36	27	SS	10.57	752.66	270.95	2864.02	30272.71
0.38	27	SS	9.2	938.92	356.78	3282.46	30198.67
0.40	27	SS	8.42	1060.9	424.36	3573.11	30085.59
0.42	27	SS	7.1	1416.67	595.00	4224.50	29994.02
0.44	27	SS	6.66	1571.02	691.24	4603.71	30660.75
0.46	27	SS	5.97	1898.16	873.15	5212.72	31119.98
0.48	27	SS	5.19	2198.17	1055.12	5476.08	28420.86

Continued on next page

Table 18: Ring: FA using static CMOS Nand gate and Inverter (continued)

Voltage(V)	Temp(°C)	Corner	Pro. delay(nS)	I(Vdd)nA	P=VI (nW)	PDP (aJ)	EDP(aJ)*(nS)
0.50	27	SS	4.6	2603.18	1301.59	5987.31	27541.64
0.52	27	SS	4.27	3008.24	1564.28	6679.49	28521.44
0.54	27	SS	4.11	3475.9	1876.98	7714.41	31706.23
0.56	27	SS	3.7	3891.45	2179.21	8063.08	29833.41
0.58	27	SS	3.56	4325.55	2508.81	8931.39	31795.76
0.60	27	SS	3.15	4785.83	2871.49	9045.21	28492.43
0.62	27	SS	2.91	5274	3269.88	9515.35	27689.67
0.64	27	SS	2.74	5768.87	3692.07	10116.29	27718.63
0.66	27	SS	2.7	6202.2	4093.45	11052.32	29841.26
0.68	27	SS	2.65	6685.26	4545.97	12046.83	31924.12
0.70	27	SS	2.53	7247.29	5073.10	12834.95	32472.42
0.16	27	SF	189.59	40.98	6.55	1243.10	235680.03
0.18	27	SF	115.51	55.77	10.03	1159.55	133940.62
0.20	27	SF	75.34	80.97	16.20	1220.18	91928.73
0.22	27	SF	61.81	117.43	25.83	1179.09	53813.74
0.24	27	SF	36.22	168.47	40.43	1341.20	44487.86
0.26	27	SF	26.03	243.24	63.24	1646.25	42852.03
0.28	27	SF	19.05	329.60	92.28	1758.09	33491.62
0.30	27	SF	14.86	443.88	133.16	1978.83	29405.50
0.32	27	SF	12.44	587.94	188.14	2340.47	29115.47
0.34	27	SF	10.11	767.56	260.97	2638.44	26674.63
0.36	27	SF	8.64	979.99	352.79	3048.16	26336.14
0.38	27	SF	6.41	1198.14	455.29	3537.64	27487.50
0.40	27	SF	6.70	1487.46	594.98	3986.40	26708.93
0.42	27	SF	6.29	1802.00	756.84	4760.52	29943.71
0.44	27	SF	4.54	2130.27	937.32	4789.71	24475.44
0.46	27	SF	5.77	2448.73	1126.41	5091.40	23013.15
0.48	27	SF	6.41	2807.72	1347.70	5539.08	22765.63
0.50	27	SF	5.51	3211.80	1605.90	6295.14	24676.97
0.52	27	SF	3.95	3656.21	1901.22	6711.33	23691.02
0.54	27	SF	2.95	4068.26	2196.86	6480.74	19118.19
0.56	27	SF	2.87	4747.76	2658.74	7630.61	21899.85
0.58	27	SF	2.83	5315.09	3082.75	8724.19	24689.46
0.60	27	SF	2.48	5890.47	3534.28	8765.02	21737.25
0.62	27	SF	2.17	6804.55	4218.82	9154.85	19866.02
0.64	27	SF	1.81	7286.73	4663.50	8440.94	15278.11
0.66	27	SF	1.54	7960.06	5253.64	8090.60	12459.53
0.68	27	SF	1.53	8667.54	5893.93	9017.71	13797.10
0.70	27	SF	2.48	9379.07	6565.35	12605.47	24202.52
0.16	27	TT	176.72	44.08	7.05	1246.37	330258.65
0.18	27	TT	91.73	58.91	10.60	972.70	89226.05
0.20	27	TT	64.60	84.47	16.89	1091.35	70501.40
0.22	27	TT	44.51	129.56	28.50	1268.70	56470.61
0.24	27	TT	29.40	193.90	46.53	1368.21	40225.51
0.26	27	TT	21.35	284.32	73.92	1578.27	33696.09
0.28	27	TT	16.12	418.71	117.23	1889.90	30465.23
0.30	27	TT	12.59	581.59	174.47	2196.66	27656.06
0.32	27	TT	9.52	776.03	248.32	2364.10	22506.23
0.34	27	TT	8.58	1015.77	345.36	2963.21	25424.39
0.36	27	TT	5.92	1287.65	463.55	2744.25	16245.96

Continued on next page

Table 18: Ring: FA using static CMOS Nand gate and Inverter (continued)

Voltage(V)	Temp(°C)	Corner	Pro. delay(nS)	I(Vdd)nA	P=VI (nW)	PDP (aJ)	EDP(aJ)*(nS)
0.38	27	TT	5.32	1606.04	610.29	3246.77	17272.86
0.40	27	TT	3.95	1969.62	787.85	3112.01	12292.44
0.42	27	TT	3.51	2311.44	970.80	3407.52	11960.41
0.44	27	TT	3.88	2779.17	1222.83	4744.60	18409.06
0.46	27	TT	3.65	3295.62	1515.98	5533.34	20196.72
0.48	27	TT	3.34	4068.69	1952.97	6522.93	21786.61
0.50	27	TT	3.65	4260.91	2130.45	7776.17	28383.03
0.52	27	TT	2.42	4703.67	2445.91	5919.10	14324.23
0.54	27	TT	2.75	5304.71	2864.54	7877.50	21663.13
0.56	27	TT	2.27	5875.81	3290.45	7469.34	16955.40
0.58	27	TT	2.49	6632.64	3846.93	9578.86	23851.37
0.60	27	TT	2.24	7732.88	4639.72	10392.99	23280.29
0.62	27	TT	1.98	8361.06	5183.85	10264.03	20322.79
0.64	27	TT	1.91	8959.94	5734.36	10952.63	20919.53
0.66	27	TT	1.78	9926.57	6551.54	11661.74	20757.90
0.68	27	TT	1.70	10859.45	7384.42	12553.52	21340.99
0.70	27	TT	1.29	11833.85	8283.69	10685.96	13784.90
0.18	27	FS	141.42	58.87	10.59	1498.57	211927.93
0.20	27	FS	80.93	73.49	16.18	1189.50	87417.02
0.22	27	FS	48.14	119.27	26.23	1263.16	60808.74
0.24	27	FS	30.69	177.81	42.67	1309.72	40195.35
0.26	27	FS	21.33	269.15	69.98	1492.69	31839.09
0.28	27	FS	14.94	394.08	110.34	1648.53	24629.13
0.30	27	FS	10.96	576.19	172.85	1894.54	20764.18
0.32	27	FS	8.97	808.03	258.57	2319.39	20804.94
0.34	27	FS	5.74	1069.06	363.48	2086.37	11975.80
0.36	27	FS	5.11	1379.81	496.73	2538.31	12970.78
0.38	27	FS	5.32	1708.43	649.20	3453.77	18374.06
0.40	27	FS	4.71	2085.93	834.37	3929.89	18509.82
0.42	27	FS	4.17	2490.20	1045.88	4361.33	18186.77
0.44	27	FS	3.57	2960.62	1302.67	4650.54	16602.44
0.46	27	FS	2.85	3482.51	1601.95	4565.57	13011.88
0.48	27	FS	2.98	4062.09	1949.80	5810.41	17315.04
0.50	27	FS	2.52	4685.50	2342.75	5903.73	14877.40
0.52	27	FS	2.23	5374.09	2794.52	6231.80	13896.91
0.54	27	FS	1.77	6425.39	3469.71	6141.38	10870.25
0.56	27	FS	2.03	7345.78	4113.63	8350.68	16951.89
0.58	27	FS	2.12	7809.44	4529.47	9602.49	20357.28
0.60	27	FS	1.86	8652.86	5191.72	9656.60	17961.27
0.62	27	FS	1.57	9532.16	5909.94	9278.60	14567.41
0.64	27	FS	1.74	10516.08	6730.29	11710.71	20376.64
0.66	27	FS	1.36	11354.68	7494.09	10191.96	13861.07
0.68	27	FS	1.26	12265.18	8340.32	10508.80	13241.09
0.70	27	FS	2.52	13253.49	9277.44	23379.16	58915.50
0.18	27	FF	72.31	98.83	17.79	1286.40	93019.84
0.20	27	FF	38.07	142.82	28.56	1087.50	41401.12
0.22	27	FF	27.96	210.13	46.22	1292.58	36140.60
0.24	27	FF	19.90	314.21	75.41	1500.70	29863.93
0.26	27	FF	14.94	447.89	116.45	1739.80	25992.69
0.28	27	FF	10.49	641.56	179.63	1884.39	19767.27

Continued on next page

Table 18: Ring: FA using static CMOS Nand gate and Inverter (continued)

Voltage(V)	Temp(°C)	Corner	Pro. delay(nS)	I(Vdd)nA	P=VI (nW)	PDP (aJ)	EDP(aJ)*(nS)
0.30	27	FF	8.48	889.19	266.75	2262.10	19182.64
0.32	27	FF	6.93	1204.85	385.55	2671.89	18516.23
0.34	27	FF	5.17	1559.77	530.32	2741.76	14174.92
0.36	27	FF	4.19	1966.97	708.11	2966.98	12431.66
0.38	27	FF	3.59	2576.02	978.89	3514.21	12616.04
0.40	27	FF	3.15	2967.72	1187.09	3739.33	11778.91
0.42	27	FF	2.76	3626.14	1522.98	4203.42	11601.46
0.44	27	FF	2.65	4269.03	1878.37	4977.69	13190.88
0.46	27	FF	2.41	5083.65	2338.47	5635.73	13582.12
0.48	27	FF	2.24	5677.52	2725.21	6104.47	13674.02
0.50	27	FF	2.00	6339.46	3169.73	6339.46	12678.93
0.52	27	FF	1.87	7048.03	3664.97	6853.51	12816.06
0.54	27	FF	1.66	8058.70	4351.69	7223.82	11991.54
0.56	27	FF	1.62	9221.50	5164.04	8365.75	13552.51
0.58	27	FF	1.49	10094.48	5854.80	8723.65	12998.24
0.60	27	FF	1.40	11078.90	6647.34	9306.28	13028.79
0.62	27	FF	1.30	12270.22	7607.53	9889.80	12856.74
0.64	27	FF	1.23	13359.09	8549.81	10516.27	12935.02
0.66	27	FF	1.18	14705.83	9705.84	11452.90	13514.42
0.68	27	FF	1.11	16073.89	10930.24	12132.57	13467.15
0.70	27	FF	1.04	17504.69	12253.28	12743.41	13253.15

E.2 Ring: Schmitt trigger CMOS Nand gate and Inverter

Table 19: Initial condition FA using Schmitt trigger CMOS NAND gate

Voltage(V)	ic(SS)	ic(SF)	ic(TT)	ic(FS)	ic(FF)
0.16	0.17	0.16	0.16		
0.18	0.20	0.18	0.18	0.16	0.16
0.20	0.17	0.19	*0.2	0.15	0.18
0.22	0.24	0.22	*0.2	0.22	0.18
0.24	0.24	0.28	0.22	0.22	0.16
0.26	0.26	0.19	0.41	0.22	0.16
0.28	0.26	0.22	0.28	0.28	0.17
0.30	0.25	0.28	0.30	0.3	0.19
0.32	0.24	0.28	0.31	0.3	0.19
0.34	0.24	0*.3	0.36	*0.34	0.19
0.36	0.30	0.31	0.36	0.29	0.19
0.38	0.30	0.31	0.36	0.28	0.21
0.40	0.30	0.31	0.36	0.28	0.21
0.42	0.30	0.42	0.36	0.28	0.22
0.44	0.49	0.42	0.36	0.28	0.26
0.46	0.49	0.42	0.36	0.44	0.26
0.48	0.49	0.42	0.36	0.42	0.26
0.50	0.49	0.42	0.50	0.41	0.26
0.52	0.48	0.42	0.50	0.43	0.32
0.54	0.48	0.42	0.51	0.43	0.32
0.56	0.48	0.42	0.51	0.41	0.32
0.58	0.48	0.42	0.51	0.40	0.34
0.60	0.49	0.42	0.51	0.40	0.34
0.62	0.49	0.42	0.51	0.41	0.36
0.64	0.49	0.42	0.51	0.39	0.40
0.66	0.40	0.42	0.51	0.39	0.40
0.68	0.41	0.42	0.51	0.39	0.40
0.70	0.41	0.42	0.51	0.39	0.40

Table 20: Ring: FA using Schmitt trigger CMOS Nand gate

Voltage(V)	Temp(°C)	Corner	Pro. delay(nS)	I(Vdd)nA	P=VI (nW)	PDP (aJ)	EDP(aJ)*(nS)
0.16	27	SS	795.54	17.90	2.86	2278.42	1812579.04
0.18	27	SS	482.8	25.65	4.61	2229.28	1076203.86
0.20	27	SS	305.63	38.40	7.68	2347.23	717386.44
0.22	27	SS	214.09	55.02	12.10	2591.57	554829.71
0.24	27	SS	144.48	81.88	19.65	2839.48	410248.47
0.26	27	SS	107.68	119.57	31.08	3347.60	360470.14
0.28	27	SS	77.03	172.19	48.21	3714.05	286093.80
0.30	27	SS	59.08	239.23	71.76	4240.16	250508.98
0.32	27	SS	47.10	326.11	104.35	4915.13	231502.97
0.34	27	SS	36.10	429.48	146.02	5271.49	190301.10
0.36	27	SS	30.95	552.77	198.99	6158.99	190620.94
0.38	27	SS	25.75	699.39	265.76	6843.53	176221.05
0.40	27	SS	21.95	860.91	344.36	7558.86	165917.17
0.42	27	SS	19.20	1064.99	447.29	8588.10	164891.58
0.44	27	SS	16.92	1285.51	565.62	9570.38	161930.95
0.46	27	SS	15.40	1527.35	702.58	10819.78	166624.76
0.48	27	SS	13.39	1785.94	857.25	11478.59	153698.36

Continued on next page

Table 20: Ring: FA using Schmitt trigger CMOS Nand gate and Inverter (continued)

Voltage(V)	Temp(°C)	Corner	Pro. delay(nS)	I(Vdd)nA	P=VI (nW)	PDP (aJ)	EDP(aJ)*(nS)
0.50	27	SS	11.97	2088.64	1044.32	12500.51	149631.18
0.52	27	SS	11.36	2409.17	1252.77	14231.47	161669.59
0.54	27	SS	10.47	2742.53	1480.97	15505.76	162345.32
0.56	27	SS	9.35	3119.17	1746.73	16331.98	152704.05
0.58	27	SS	8.99	3508.51	2034.93	18294.09	164463.90
0.60	27	SS	8.51	3929.68	2357.80	20064.95	170752.77
0.62	27	SS	7.86	4315.89	2675.85	21032.23	165313.39
0.64	27	SS	7.46	4759.22	3045.90	22722.44	169509.46
0.66	27	SS	6.97	5267.76	3476.72	24232.77	168902.42
0.68	27	SS	6.53	5709.42	3882.40	25352.12	165549.38
0.70	27	SS	6.22	6189.34	4332.54	26948.41	167619.12
0.16	27	SF	435.21	30.12	4.81	2097.36	912793.80
0.18	27	SF	269.36	43.57	7.84	2112.48	569018.34
0.20	27	SF	195.37	63.83	12.76	2493.01	486872.05
0.22	27	SF	133.62	92.45	20.33	2717.69	363138.69
0.24	27	SF	93.21	133.53	32.04	2987.11	278429.40
0.26	27	SF	69.31	193.26	50.24	3482.66	241383.24
0.28	27	SF	50.14	265.93	74.46	3733.44	187194.90
0.30	27	SF	40.97	370.19	111.05	4550.07	186416.73
0.32	27	SF	32.55	501.04	160.33	5218.90	169875.37
0.34	27	SF	26.65	652.41	221.81	5911.49	157541.37
0.36	27	SF	22.49	842.30	303.22	6819.62	153373.29
0.38	27	SF	19.56	1056.93	401.63	7855.96	153662.65
0.40	27	SF	16.30	1293.02	517.21	8430.53	137417.73
0.42	27	SF	14.72	1571.26	659.93	9714.21	142993.22
0.44	27	SF	13.12	1877.07	825.91	10835.97	142168.03
0.46	27	SF	12.05	2234.01	1027.64	12383.13	149216.76
0.48	27	SF	10.46	2617.17	1256.24	13140.32	137447.77
0.50	27	SF	9.84	3063.94	1531.97	15074.60	148334.10
0.52	27	SF	8.60	3451.82	1794.95	15436.57	132754.50
0.54	27	SF	8.27	3988.55	2153.81	17812.06	147305.79
0.56	27	SF	7.71	4445.94	2489.73	19195.82	147999.84
0.58	27	SF	7.24	5057.34	2933.25	21236.78	153754.30
0.60	27	SF	6.80	5686.59	3411.95	23201.30	157768.89
0.62	27	SF	6.36	6254.72	3877.92	24663.61	156860.59
0.64	27	SF	6.02	7018.33	4491.73	27040.25	162782.34
0.66	27	SF	5.96	7727.64	5100.24	30397.45	181168.84
0.68	27	SF	5.48	8379.05	5697.76	31223.72	171106.01
0.70	27	SF	5.21	9156.17	6409.32	33392.58	173975.36
0.16	27	TT	414.21	34.6	5.53	2293.06	949811.09
0.18	27	TT	286.54	49.78	8.9	2567.51	735695.17
0.20	27	TT	179.21	73.54	14.70	2653.78	472365.42
0.22	27	TT	118.04	109.21	24.02	2836.05	334767.65
0.24	27	TT	84.88	161.31	38.71	3286.07	278922.32
0.26	27	TT	59.32	224.38	58.33	3460.71	205289.86
0.28	27	TT	44.17	317.80	88.98	3930.52	173611.16
0.30	27	TT	33.02	433.85	130.15	4297.79	141913.26
0.32	27	TT	26.27	580.29	185.69	4878.16	128149.43
0.34	27	TT	21.98	751.10	255.37	5613.18	123377.70
0.36	27	TT	17.56	967.48	348.29	6116.05	107398.00

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Table 20: Ring: FA using Schmitt trigger CMOS Nand gate and Inverter (continued)

Voltage(V)	Temp(°C)	Corner	Pro. delay(nS)	I(Vdd)nA	P=VI (nW)	PDP (aJ)	EDP(aJ)*(nS)
0.38	27	TT	15.08	1216.12	462.12	6968.88	105090.85
0.40	27	TT	13.37	1513.97	605.59	8096.73	108253.39
0.42	27	TT	11.19	1822.69	765.52	8566.27	95856.65
0.44	27	TT	10.36	2173.84	956.49	9909.27	102660.07
0.46	27	TT	9.27	2688.13	1236.54	11462.73	106259.53
0.48	27	TT	8.28	3013.19	1446.33	11975.62	99158.18
0.50	27	TT	7.47	3492.61	1746.30	13044.90	97445.41
0.52	27	TT	7.02	3992.26	2075.97	14573.36	102305.01
0.54	27	TT	6.46	4506.14	2433.31	15719.23	101546.26
0.56	27	TT	5.91	5085.97	2848.14	16832.54	99480.36
0.58	27	TT	5.52	5756.36	3338.69	18429.58	101731.28
0.60	27	TT	5.22	6334.33	3800.59	19839.13	103560.26
0.62	27	TT	4.79	7108.14	4407.04	21109.76	101115.77
0.64	27	TT	4.76	7754.65	4962.97	23623.78	112449.19
0.66	27	TT	4.62	8501.85	5611.22	25923.85	119768.18
0.68	27	TT	4.36	9262.11	6298.24	27460.32	119727.02
0.70	27	TT	4.02	10116.88	7081.81	28468.90	114445.01
0.18	27	FS	371.61	49.49	8.90	3310.84	1230342.89
0.20	27	FS	232.78	68.88	13.77	3206.77	746473.61
0.22	27	FS	153.35	99.67	21.92	3362.60	515654.79
0.24	27	FS	104.83	144.15	34.59	3626.87	380205.28
0.26	27	FS	70.74	210.47	54.72	3871.14	273844.47
0.28	27	FS	50.97	300.18	84.05	4284.07	218359.42
0.30	27	FS	38.43	416.58	124.97	4802.77	184570.60
0.32	27	FS	29.36	556.42	178.05	5227.74	153486.53
0.34	27	FS	23.89	745.18	253.36	6052.79	144601.36
0.36	27	FS	18.88	982.31	353.63	6676.59	126054.18
0.38	27	FS	15.41	1224.85	465.44	7172.50	110528.22
0.40	27	FS	13.32	1519.26	607.70	8094.65	107820.79
0.42	27	FS	11.47	1842.78	773.97	8877.43	101824.20
0.44	27	FS	9.82	2209.07	971.99	9544.97	93731.66
0.46	27	FS	9.06	2597.88	1195.02	10826.94	98092.16
0.48	27	FS	8.29	2992.31	1436.31	11907.03	98709.32
0.50	27	FS	7.52	3479.98	1739.99	13084.75	98397.32
0.52	27	FS	6.52	4040.07	2100.83	13697.46	89307.48
0.54	27	FS	6.03	4521.56	2441.64	14723.11	88780.35
0.56	27	FS	5.72	5048.68	2827.26	16171.93	92503.44
0.58	27	FS	5.51	5671.08	3289.22	18123.65	99861.33
0.60	27	FS	5.06	6294.84	3776.90	19111.15	96702.43
0.62	27	FS	4.62	7093.91	4398.22	20319.82	93877.57
0.64	27	FS	4.57	7816.44	5002.52	22861.52	104477.16
0.66	27	FS	4.21	8626.302	5693.35	23969.04	100909.66
0.68	27	FS	4.17	9249.419	6289.60	26227.65	109369.31
0.70	27	FS	3.81	10083.58	7058.51	26892.93	102462.07
0.18	27	FF	151.17	87.45	15.47	2379.56	359719.13
0.20	27	FF	103.12	127.75	25.55	2634.716	271691.9139
0.22	27	FF	66.52	181.35	39.89	2654.00	176544.54
0.24	27	FF	46.99	262.91	63.10	2965.07	139328.76
0.26	27	FF	35.06	370.98	96.45	3381.71	118562.90
0.28	27	FF	26.62	517.14	144.80	3854.59	102609.23

Continued on next page

Table 20: Ring: FA using Schmitt trigger CMOS Nand gate and Inverter (continued)

Voltage(V)	Temp(°C)	Corner	Pro. delay(nS)	I(Vdd)nA	P=VI (nW)	PDP (aJ)	EDP(aJ)*(nS)
0.30	27	FF	20.77	717.07	215.12	4468.10	92802.57
0.32	27	FF	16.92	936.11	299.55	5068.51	85759.31
0.34	27	FF	13.75	1209.95	411.38	5656.54	77777.48
0.36	27	FF	11.74	1537.06	553.34	6496.24	76265.94
0.38	27	FF	9.87	1922.33	730.48	7209.89	71161.66
0.40	27	FF	8.65	2364.91	945.96	8182.60	70779.54
0.42	27	FF	7.46	2785.49	1169.90	8727.49	65107.12
0.44	27	FF	6.66	3302.91	1453.28	9678.86	64461.24
0.46	27	FF	6.31	3949.85	1816.93	11464.84	72343.17
0.48	27	FF	5.61	4668.58	2240.92	12571.57	70526.51
0.50	27	FF	5.11	5283.54	2641.77	13499.44	68982.16
0.52	27	FF	4.87	5967.14	3102.91	15111.19	73591.53
0.54	27	FF	4.36	6797.19	3670.48	16003.32	69774.49
0.56	27	FF	4.06	7749.51	4339.72	17619.28	71534.30
0.58	27	FF	3.88	8353.40	4844.97	18798.50	72938.20
0.60	27	FF	3.63	9345.28	5607.17	20354.03	73885.16
0.62	27	FF	3.42	10439.88	6472.72	22136.72	75707.58
0.64	27	FF	3.38	11467.31	7339.07	24806.08	83844.56
0.66	27	FF	3.09	12209.92	8058.54	24900.91	76943.81
0.68	27	FF	2.94	13303.02	9046.05	26595.39	78190.46
0.70	27	FF	2.91	14628.28	10239.79	29797.80	86711.61

E.3 Ring: static CMOS XOR gate and Inverter

Table 21: Ring: FA using static CMOS XOR gate

Voltage(V)	Temp(°C)	Corner	Pro. delay(nS)	I(Vdd)nA	P=VI (nW)	PDP (aJ)	EDP(aJ)*(nS)
0.16	27	SS	143.89	39.25	6.28	903.62	130023.20
0.18	27	SS	80.24	58.12	10.46	839.43	67356.56
0.20	27	SS	54.57	86.49	17.29	943.95	51511.45
0.22	27	SS	39.69	125.79	27.67	1098.37	43594.42
0.24	27	SS	28.7	180.38	43.29	1242.45	35658.52
0.26	27	SS	22.34	252	65.52	1463.71	32699.43
0.28	27	SS	17.45	345.75	96.81	1689.33	29478.88
0.30	27	SS	14.44	461.93	138.57	2001.08	28895.60
0.32	27	SS	12.21	605.41	193.73	2365.45	28882.24
0.34	27	SS	10.56	766.48	260.60	2751.96	29060.80
0.36	27	SS	9.00	965	347.4	3126.6	28139.40
0.38	27	SS	7.59	1193.56	453.55	3442.46	26128.31
0.40	27	SS	6.65	1433.44	573.37	3812.95	25356.12
0.42	27	SS	6.03	1710.13	718.25	4331.07	26116.38
0.44	27	SS	5.49	2012.27	885.39	4860.83	26686.00
0.46	27	SS	4.86	2352.23	1082.02	5258.64	25557.01
0.48	27	SS	4.36	2734.01	1312.32	5721.73	24946.76
0.50	27	SS	3.92	3139.38	1569.69	6153.18	24120.48
0.52	27	SS	3.66	3584.84	1864.11	6822.6	24970.96
0.54	27	SS	3.56	4066.75	2196.04	7817.92	27831.79
0.56	27	SS	3.32	4556.36	2551.56	8471.18	28124.33
0.58	27	SS	3.07	5075.89	2944.01	9038.12	27747.05
0.60	27	SS	2.91	5683.86	3410.31	9924.01	28878.89
0.62	27	SS	2.72	6256.68	3879.14	10551.26	28699.44

Continued on next page

Table 21: Ring: FA using static CMOS XOR gate (continued)

Voltage(V)	Temp(°C)	Corner	Pro. delay(nS)	I(Vdd)nA	P=VI (nW)	PDP (aJ)	EDP(aJ)*(nS)
0.64	27	SS	2.66	6896.87	4413.99	11741.23	31231.67
0.66	27	SS	2.53	7564.21	4992.37	12630.71	31955.71
0.68	27	SS	2.38	8287.78	5635.69	13412.94	31922.80
0.70	27	SS	2.29	9052.65	6336.85	14511.39	33231.10
0.16	27	SF	87.30	72.74	11.6384	1016.03	88699.62
0.18	27	SF	54.57	101.82	18.3276	1000.13	54577.48
0.20	27	SF	40.12	143.08	28.616	1148.07	46060.72
0.22	27	SF	35.14	202.51	44.5522	1565.56	55013.92
0.24	27	SF	23.74	274.39	65.8536	1563.36	37114.27
0.26	27	SF	17.26	381.55	99.203	1712.24	29553.32
0.28	27	SF	15.41	511.56	143.236	2207.27	34014.17
0.30	27	SF	12.28	672.57	201.771	2477.74	30426.74
0.32	27	SF	8.94	859.69	275.100	2459.40	21987.04
0.34	27	SF	8.75	1089.28	370.355	3240.60	28355.32
0.36	27	SF	7.66	1344.22	483.919	3706.82	28394.24
0.38	27	SF	6.95	1634.39	621.068	4316.42	29999.14
0.40	27	SF	6.22	1962.62	785.048	4882.99	30372.25
0.42	27	SF	5.44	2303.46	967.453	5262.94	28630.42
0.44	27	SF	4.58	2707.71	1191.39	5456.57	24991.12
0.46	27	SF	4.38	3166.31	1456.50	6379.48	27942.12
0.48	27	SF	4.06	3665.86	1759.61	7144.02	29004.75
0.50	27	SF	3.56	4238.75	2119.37	7544.97	26860.11
0.52	27	SF	3.37	4843.44	2518.58	8487.64	28603.36
0.54	27	SF	3.16	5502.18	2971.17	9388.91	29668.98
0.56	27	SF	2.84	6145.6	3441.53	9773.96	27758.05
0.58	27	SF	2.65	6913.98	4010.10	10626.78	28160.98
0.60	27	SF	2.56	7613.05	4567.83	11693.64	29935.73
0.62	27	SF	2.44	8515.25	5279.45	12881.87	31431.76
0.64	27	SF	2.29	9417.77	6027.37	13802.68	31608.14
0.66	27	SF	2.20	10422.37	6878.76	15133.28	33293.21
0.68	27	SF	2.08	11489.24	7812.68	16250.38	33800.79
0.70	27	SF	1.95	12568.04	8797.62	17155.37	33452.98
0.16	27	TT	79.42	79.17	12.66	1006.02	79898.82
0.18	27	TT	41.34	116.49	20.96	866.82	35834.56
0.20	27	TT	28.23	169.52	33.90	957.10	27019.21
0.22	27	TT	21.52	246.38	54.20	1166.46	25102.25
0.24	27	TT	16.15	344.3	82.63	1334.50	21552.28
0.26	27	TT	12.96	475.89	123.73	1603.55	20782.12
0.28	27	TT	10.67	637.21	178.41	1903.72	20312.78
0.30	27	TT	8.54	851.76	255.52	2182.20	18636.06
0.32	27	TT	7.39	1093.6	349.95	2586.14	19111.61
0.34	27	TT	6.28	1392.09	473.31	2972.39	18666.61
0.36	27	TT	5.58	1725.71	621.25	3466.60	19343.66
0.38	27	TT	4.98	2097.89	797.19	3970.04	19770.83
0.40	27	TT	4.34	2508.98	1003.59	4355.58	18903.25
0.42	27	TT	3.84	2963.41	1244.63	4779.38	18352.84
0.44	27	TT	3.4	3475.75	1529.33	5199.72	17679.05
0.46	27	TT	3.08	4062.91	1868.93	5756.33	17729.49
0.48	27	TT	2.88	4693.38	2252.82	6488.12	18685.81
0.50	27	TT	2.69	5363.43	2681.71	7213.81	19405.15

Continued on next page

Table 21: Ring: FA using static CMOS XOR gate (continued)

Voltage(V)	Temp(°C)	Corner	Pro. delay(nS)	I(Vdd)nA	P=VI (nW)	PDP (aJ)	EDP(aJ)*(nS)
0.52	27	TT	2.5	6077.13	3160.10	7900.26	19750.67
0.54	27	TT	2.29	6804.46	3674.40	8414.39	19268.96
0.56	27	TT	2.14	7609.45	4261.29	9119.16	19515.01
0.58	27	TT	2	8495.04	4927.12	9854.24	19708.49
0.60	27	TT	1.88	9429.83	5657.89	10636.84	19997.27
0.62	27	TT	1.75	10391.77	6442.89	11275.07	19731.37
0.64	27	TT	1.7	11468.61	7339.91	12477.84	21212.34
0.66	27	TT	1.64	12574.48	8299.15	13610.61	22321.41
0.68	27	TT	1.57	13770.88	9364.19	14701.79	23081.81
0.70	27	TT	1.49	15042.52	10529.76	15689.34	23377.12
0.18	27	FS	44.97	109.98	19.79	890.24	40034.27
0.20	27	FS	31.37	160.93	32.18	1009.67	31673.49
0.22	27	FS	15.83	235.48	51.80	820.08	12981.90
0.24	27	FS	11.86	334.81	80.35	953.00	11302.61
0.26	27	FS	12.38	471.87	122.68	1518.85	18803.42
0.28	27	FS	9.45	653.32	182.92	1728.68	16336.07
0.30	27	FS	7.54	881.4	264.42	1993.72	15032.70
0.32	27	FS	6.67	1145.88	366.68	2445.76	16313.26
0.34	27	FS	5.72	1441.72	490.18	2803.85	16038.06
0.36	27	FS	4.84	1825.94	657.33	3181.51	15398.54
0.38	27	FS	4.32	2215.31	841.81	3636.65	15710.34
0.40	27	FS	3.67	2663.39	1065.35	3909.85	14349.17
0.42	27	FS	3.29	3172.84	1332.59	4384.23	14424.11
0.44	27	FS	2.92	3811.38	1677.00	4896.86	14298.83
0.46	27	FS	2.67	4377.81	2013.79	5376.82	14356.12
0.48	27	FS	2.46	5028.66	2413.75	5937.84	14607.09
0.50	27	FS	2.23	5733.76	2866.88	6393.14	14256.70
0.52	27	FS	2.14	6494.41	3377.09	7226.97	15465.73
0.54	27	FS	2.01	7371.3	3980.50	8000.80	16081.62
0.56	27	FS	1.87	8215.77	4600.83	8603.55	16088.64
0.58	27	FS	1.75	9137.77	5299.90	9274.83	16230.96
0.60	27	FS	1.64	10086.65	6051.99	9925.26	16277.43
0.62	27	FS	1.56	11160.27	6919.36	10794.21	16838.97
0.64	27	FS	1.45	12269.62	7852.55	11386.20	16510.00
0.66	27	FS	1.37	13444.87	8873.61	12156.85	16654.88
0.68	27	FS	1.28	14683.55	9984.81	12780.56	16359.11
0.70	27	FS	1.18	15945.39	11161.77	13170.89	15541.65
0.18	27	FF	26.59	213.8	38.48	1023.28	27209.26
0.20	27	FF	18.04	303.58	60.71	1095.31	19759.51
0.22	27	FF	13.89	429.73	94.54	1313.16	18239.91
0.24	27	FF	10.40	589.62	141.50	1471.69	15305.59
0.26	27	FF	8.13	798.4	207.58	1687.65	13720.65
0.28	27	FF	6.48	1104.37	309.22	2003.76	12984.42
0.30	27	FF	5.64	1407.83	422.34	2382.04	13434.75
0.32	27	FF	4.66	1789.74	572.71	2668.86	12436.88
0.34	27	FF	4.32	2279.21	774.93	3347.70	14462.07
0.36	27	FF	3.78	2783.6	1002.09	3787.92	14318.34
0.38	27	FF	3.24	3359.73	1276.69	4136.49	13402.25
0.40	27	FF	2.87	3993.48	1597.39	4584.51	13157.55
0.42	27	FF	2.52	4720.83	1982.74	4996.52	12591.24

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Table 21: Ring: FA using static CMOS XOR gate (continued)

Voltage(V)	Temp(°C)	Corner	Pro. delay(nS)	I(Vdd)nA	P=VI (nW)	PDP (aJ)	EDP(aJ)*(nS)
0.44	27	FF	2.30	5513.43	2425.90	5579.59	12833.05
0.46	27	FF	2.09	6379.99	2934.79	6133.72	12819.47
0.48	27	FF	1.88	7325.69	3516.33	6610.70	12428.12
0.50	27	FF	1.84	8323.63	4161.81	7657.73	14090.24
0.52	27	FF	1.71	9406.72	4891.49	8364.45	14303.21
0.54	27	FF	1.61	10533.93	5688.32	9158.19	14744.69
0.56	27	FF	1.51	11750.41	6580.22	9936.14	15003.58
0.58	27	FF	1.41	13051.75	7570.01	10673.7	15049.94
0.60	27	FF	1.33	14444.57	8666.74	11526.76	15330.59
0.62	27	FF	1.24	15948.41	9888.01	12261.13	15203.81
0.64	27	FF	1.22	17526.82	11217.16	13684.94	16695.62
0.66	27	FF	1.14	19223.24	12687.33	14463.56	16488.46
0.68	27	FF	1.06	20970.92	14260.22	15115.83	16022.78
0.70	27	FF	1.04	22809.05	15966.33	16604.98	17269.18

E.4 Ring: Schmitt trigger CMOS XOR gate and Inverter

Table 22: Initial condition for FA using Schmitt trigger CMOS XOR gate

Voltage(V)	ic(SS)	ic(SF)	ic(TT)	ic(FS)	ic(FF)
0.16	0.17	0.17	0.17		
0.18	0.17	0.17	0.17	0.18	0.18
0.20	0.17	0.17	0.17	0.18	0.20
0.22	0.17	0.17	0.17	0.18	0.20
0.24	0.21	0.17	0.17	0.24	0.20
0.26	0.21	0.25	0.26	0.25	0.20
0.28	0.21	0.25	0.26	0.25	0.28
0.30	0.21	0.25	0.26	0.25	0.29
0.32	0.21	0.25	0.26	0.25	0.30
0.34	0.32	0.30	0.26	*0.34	0.31
0.36	0.32	0.30	0.26	0.34	0.32
0.38	0.32	0.30	0.26	0.34	0.32
0.40	0.32	0.30	0.36	0.34	0.32
0.42	0.32	0.30	0.36	0.34	0.42
0.44	0.32	0.30	0.35	0.34	0.32
0.46	0.32	0.30	0.35	0.34	0.32
0.48	0.32	0.30	0.35	0.34	0.32
0.50	0.32	0.30	0.35	0.34	0.32
0.52	0.42	0.30	0.35	0.40	0.32
0.54	0.42	0.30	0.36	0.41	0.32
0.56	0.42	0.40	0.36	0.41	0.32
0.58	0.42	0.40	0.36	0.41	0.32
0.60	0.42	0.40	0.36	0.41	0.32
0.62	0.42	0.40	0.36	0.41	0.42
0.64	0.42	0.40	0.36	0.41	0.42
0.66	0.42	0.40	0.37	0.41	0.42
0.68	0.42	0.40	0.37	0.41	0.42
0.70	0.42	0.40	0.37	0.41	0.42

Table 23: Ring: FA using Schmitt trigger CMOS XOR gate

Voltage (V)	Temp (°C)	Corner	Pro. delay(nS)	I(Vdd)nA	P=VI(nW)	PDP (aJ)	EDP(aJ)*(nS)
0.16	27	SS	931.47	13.8	2.20	2056.68	1915741.08
0.18	27	SS	565.92	20.03	3.60	2040.36	1154685.04
0.20	27	SS	367.74	29.95	5.99	2202.76	810043.91
0.22	27	SS	254.55	46.01	10.12	2576.60	655875.05
0.24	27	SS	164.66	70.01	16.80	2766.68	455562.05
0.26	27	SS	113.58	103.23	26.83	3048.46	346244.59
0.28	27	SS	83.53	150.9	42.25	3529.30	294803.22
0.30	27	SS	61.79	212.04	63.61	3930.58	242870.87
0.32	27	SS	48.41	291.98	93.43	4523.12	218964.26
0.34	27	SS	36.84	391.72	133.18	4906.52	180756.49
0.36	27	SS	31.54	510.28	183.70	5793.92	182740.33
0.38	27	SS	25.88	658.01	250.04	6471.13	167472.93
0.40	27	SS	22.19	821.33	328.53	7290.12	161767.87
0.42	27	SS	18.31	1002.04	420.85	7705.88	141094.80
0.44	27	SS	16.28	1217.41	535.66	8720.55	141970.57
0.46	27	SS	14.74	1452.13	667.97	9846.02	145130.36
0.48	27	SS	13.06	1685.69	809.13	10567.25	138008.33
0.50	27	SS	11.89	1971.98	985.99	11723.42	139391.47
0.52	27	SS	11.05	2316.59	1204.62	13311.12	147087.94
0.54	27	SS	10.28	2648.99	1430.45	14705.07	151168.15
0.56	27	SS	9.13	3008.18	1684.58	15380.22	140421.43
0.58	27	SS	8.3	3407.89	1976.57	16405.58	136166.33
0.60	27	SS	7.85	3796.43	2277.85	17881.18	140367.30
0.62	27	SS	7.21	4173.94	2587.84	18658.34	134526.67
0.64	27	SS	7.01	4629.3	2962.75	20768.89	145589.92
0.66	27	SS	6.63	5043.69	3328.83	22070.17	146325.28
0.68	27	SS	6.13	5536.28	3764.67	23077.42	141464.64
0.70	27	SS	6.04	6152.01	4306.40	26010.69	157104.61
0.18	27	SF	422.44	26.04	4.16	1760.05	743517.21
0.18	27	SF	262.25	39.11	7.03	1846.18	484162.68
0.20	27	SF	176.24	59.41	11.88	2094.08	369061.30
0.22	27	SF	125.81	89.17	19.61	2468.06	310507.26
0.24	27	SF	84.82	134.7	32.32	2742.06	232581.61
0.26	27	SF	63.02	195.01	50.70	3195.27	201366.41
0.28	27	SF	49.34	276.68	77.47	3822.38	188596.69
0.30	27	SF	38.46	379.41	113.82	4377.63	168363.74
0.32	27	SF	28.49	502.12	160.67	4577.72	130419.45
0.34	27	SF	22.99	674.21	229.23	5270.02	121157.98
0.36	27	SF	19.52	851	306.36	5980.14	116732.47
0.38	27	SF	16.53	1063.69	404.20	6681.46	110444.57
0.40	27	SF	14.66	1312.62	525.04	7697.20	112841.00
0.42	27	SF	12.91	1609.05	675.80	8724.59	112634.46
0.44	27	SF	11.74	1970.85	867.17	10180.62	119520.51
0.46	27	SF	10.66	2329.14	1071.40	11421.17	121749.68
0.48	27	SF	9.43	2727.22	1309.06	12344.48	116408.52
0.50	27	SF	8.77	3129.5	1564.75	13722.85	120349.46
0.52	27	SF	7.77	3601.89	1872.98	14553.07	113077.40
0.54	27	SF	7.01	4106.8	2217.67	15545.88	108976.62
0.56	27	SF	6.48	4618.38	2586.29	16759.17	108599.46
0.58	27	SF	6.3	5203.44	3017.99	19013.36	119784.22
0.60	27	SF	5.69	5827.66	3496.59	19895.63	113206.14

Continued on next page

Table 23: Ring: FA using Schmitt trigger CMOS XOR gate (continued)

Voltage(V)	Temp(°C)	Corner	Pro. delay(nS)	I(Vdd)nA	P=VI (nW)	PDP (aJ)	EDP(aJ)*(nS)
0.62	27	SF	5.42	6465.9	4008.85	21728.01	117765.81
0.64	27	SF	5.1	7291.79	4666.74	23800.40	121382.05
0.66	27	SF	4.59	7928.46	5232.78	24018.47	110244.80
0.68	27	SF	4.43	8689.19	5908.64	26175.31	115956.64
0.70	27	SF	4.14	9392.41	6574.68	27219.20	112687.50
0.16	27	TT	485.28	26.59	4.25	2064.57	1001897.06
0.18	27	TT	294.84	38.53	6.93	2044.83	602898.66
0.20	27	TT	195.18	58.47	11.69	2282.43	445485.64
0.22	27	TT	132.77	88.17	19.39	2575.39	341934.90
0.24	27	TT	92.42	132.67	31.84	2942.72	271966.80
0.26	27	TT	65.5	193.45	50.29	3294.45	215786.70
0.28	27	TT	49.26	277.62	77.73	3829.15	188624.28
0.30	27	TT	35.72	388.41	116.52	4162.20	148673.83
0.32	27	TT	28.73	527.98	168.95	4854.03	139456.48
0.34	27	TT	23.05	697	236.98	5462.38	125908.06
0.36	27	TT	17.45	900.98	324.35	5659.95	98766.23
0.38	27	TT	15.53	1138.07	432.46	6716.20	104302.68
0.40	27	TT	13.07	1423.36	569.34	7441.32	97258.13
0.42	27	TT	11.51	1719.37	722.13	8311.77	95668.57
0.44	27	TT	10.28	2075.69	913.30	9388.76	96516.46
0.46	27	TT	9.31	2462.46	1132.73	10545.73	98180.75
0.48	27	TT	8.33	2876.37	1380.65	11500.87	95802.31
0.50	27	TT	7.58	3347.07	1673.53	12685.39	96155.29
0.52	27	TT	6.23	3848.19	2001.05	12466.59	77666.89
0.54	27	TT	6.14	4390.38	2370.80	14556.74	89378.40
0.56	27	TT	5.85	4918.75	2754.5	16113.82	94265.87
0.58	27	TT	5.25	5475.82	3175.97	16673.87	87537.82
0.60	27	TT	5.24	6075.93	3645.55	19102.72	100098.27
0.62	27	TT	4.5	6701.11	4154.68	18696.09	84132.43
0.64	27	TT	4.49	7534.97	4822.38	21652.48	97219.67
0.66	27	TT	4.2	8196.54	5409.71	22720.80	95427.39
0.68	27	TT	3.99	8952.41	6087.63	24289.67	96915.818
0.70	27	TT	3.79	10043.92	7030.74	26646.51	100990.30
0.16	27	FS	723.97	28.84	4.61	3340.68	2418557.28
0.18	27	FS	432.38	37.89	6.82	2948.91	1275053.19
0.20	27	FS	299.7	53.38	10.67	3199.59	958919.28
0.22	27	FS	198.33	76.7	16.87	3346.62	663735.22
0.24	27	FS	130.33	110.76	26.58	3464.48	451526.22
0.26	27	FS	98.05	161.79	42.06	4124.51	404408.44
0.28	27	FS	67.32	232.95	65.22	4391.01	295603.08
0.30	27	FS	46.22	329.19	98.75	4564.54	210973.43
0.32	27	FS	37.22	453.83	145.22	5405.29	201185.14
0.34	27	FS	29.31	615.46	209.25	6133.30	179767.17
0.36	27	FS	23.49	799.76	287.91	6763.09	158864.99
0.38	27	FS	18	1015.77	385.99	6947.86	125061.60
0.40	27	FS	15.28	1265.28	506.11	7733.39	118166.2
0.42	27	FS	13.31	1579.53	663.40	8829.88	117525.81
0.44	27	FS	11.42	1887.39	830.45	9483.75	108304.50
0.46	27	FS	10.48	2256.59	1038.03	10878.56	114007.40
0.48	27	FS	8.98	2642.92	1268.60	11392.04	102300.54

Continued on next page

Table 23: Ring: FA using Schmitt trigger CMOS XOR gate (continued)

Voltage(V)	Temp(°C)	Corner	Pro. delay(nS)	I(Vdd)nA	P=VI (nW)	PDP (aJ)	EDP(aJ)*(nS)
0.50	27	FS	7.89	3109.85	1554.92	12268.35	96797.346
0.52	27	FS	7.37	3525.23	1833.11	13510.09	99569.37
0.54	27	FS	6.92	4093.08	2210.26	15295.02	105841.54
0.56	27	FS	6.34	4693.85	2628.55	16665.04	105656.38
0.58	27	FS	5.97	5214.04	3024.14	18054.13	107783.18
0.60	27	FS	5.65	5807.98	3484.78	19689.05	111243.14
0.62	27	FS	5.26	6408.72	3973.40	20900.11	109934.61
0.64	27	FS	5.08	7118.76	4556.00	23144.51	117574.12
0.66	27	FS	4.73	7774.99	5131.49	24271.96	114806.38
0.68	27	FS	4.42	8445.39	5742.86	25383.46	112194.91
0.70	27	FS	4.13	8551.99	5986.39	24723.80	102109.30
0.18	27	FF	283.58	47.71	7.63	2164.73	613875.91
0.18	27	FF	170.05	68.44	12.31	2094.87	356234.33
0.20	27	FF	119.34	102.16	20.43	2438.35	290993.27
0.22	27	FF	82.95	152.08	33.45	2775.30	230211.79
0.24	27	FF	55.84	225.49	54.11	3021.92	168744.39
0.26	27	FF	41.73	328.01	85.28	3558.84	148510.51
0.28	27	FF	31.69	464.99	130.19	4125.94	130751.33
0.30	27	FF	24.59	640.68	192.20	4726.29	116219.62
0.32	27	FF	18.38	859.73	275.11	5056.58	92940.08
0.34	27	FF	14.32	1122.88	381.77	5467.07	78288.55
0.36	27	FF	11.93	1448.9	521.60	6222.73	74237.23
0.38	27	FF	10.52	1811.15	688.23	7240.25	76167.46
0.40	27	FF	9.19	2219.13	887.65	8157.52	74967.62
0.42	27	FF	8.14	2691.72	1130.52	9202.45	74907.96
0.44	27	FF	6.92	3215.02	1414.60	9789.09	67740.52
0.46	27	FF	6.17	3772.7	1735.44	10707.67	66066.36
0.48	27	FF	5.5	4390.51	2107.44	11590.94	63750.20
0.50	27	FF	5.05	5081.59	2540.79	12831.01	64796.62
0.52	27	FF	4.61	5821.93	3027.40	13956.33	64338.68
0.54	27	FF	4.26	6607.73	3568.17	15200.42	64753.79
0.56	27	FF	3.97	7423.2	4156.99	16503.25	65517.93
0.58	27	FF	3.64	8218.69	4766.84	17351.29	63158.72
0.60	27	FF	3.44	9181.17	5508.70	18949.93	65187.77
0.62	27	FF	3.29	10061.59	6238.18	20523.63	67522.74
0.64	27	FF	3.1	11128.53	7122.25	22079.00	68444.91
0.66	27	FF	2.88	12233.18	8073.89	23252.82	66968.14
0.68	27	FF	2.75	13383.54	9100.80	25027.21	68824.85
0.70	27	FF	2.76	14523.21	10166.24	28058.84	77442.40

F Results of RCA in Tabular form:

F.1 RCA: static CMOS NAND

Table 24 demonstrates the Propagation delay average current, average power, power delay product, and energy-delay product of 4bit ripple carry adder using Full adder(static CMOS NAND gate).

Table 24: RCA using FA static CMOS NAND

Voltage (V)	Temp (°C)	Corner	Pro. delay(nS)	I(Vdd)nA	P=VI(nW)	PDP (aJ)	EDP(aJ)*(nS)
0.18	27	SS	101.9	4613.1	830.35	84613.48	8622113.6
0.20	27	SS	74.94	5431.92	1086.38	81413.61	6101136.4
0.22	27	SS	51.69	6147.11	1352.36	69903.70	3613322.5
0.24	27	SS	38.8	7113.22	1707.17	66238.30	2570046.2
0.26	27	SS	29.49	8117.46	2110.53	62239.81	1835452.0
0.28	27	SS	23.53	9149.26	2561.79	60278.98	1418364.5
0.30	27	SS	19.12	10178.54	3053.56	58384.10	1116304.0
0.32	27	SS	16.33	11260.64	3603.40	58843.60	960915.99
0.34	27	SS	13.66	12623.48	4291.98	58628.49	800865.18
0.36	27	SS	11.55	13733.6	4944.09	57104.30	659554.76
0.38	27	SS	9.84	14931.7	5674.04	55832.61	549392.90
0.40	27	SS	8.87	16508.49	6603.39	58572.12	519534.72
0.42	27	SS	7.94	17475.77	7339.82	58278.19	462728.89
0.44	27	SS	7.07	18780.97	8263.62	58423.84	413056.55
0.46	27	SS	6.41	20211.15	9297.12	59594.59	382001.36
0.48	27	SS	5.82	21644.05	10389.1	60464.81	351905.24
0.50	27	SS	5.33	22665.17	11332.5	60402.67	321946.27
0.52	27	SS	5.01	24060.95	12511.6	62683.58	314044.77
0.54	27	SS	4.58	25470.78	13754.2	62994.33	288514.04
0.56	27	SS	4.3	26921.12	15075.8	64826.05	278752.04
0.58	27	SS	4	28397.47	16470.5	65882.13	263528.52
0.60	27	SS	3.86	29755.57	17853.3	68913.90	266007.65
0.62	27	SS	3.65	30999.99	19219.9	70152.97	256058.36
0.64	27	SS	3.45	32653.57	20898.2	72099.08	248741.83
0.66	27	SS	3.26	34293.14	22633.4	73785.12	240539.49
0.68	27	SS	3.09	35951.39	24446.9	75541.06	233421.87
0.70	27	SS	2.95	37484.09	26238.8	77404.64	228343.70
0.75	27	SS	2.63	41554.8	31166.	81966.8	215572.79
0.80	27	SS	2.4	45848.28	36678.6	88028.69	211268.87
0.18	27	SF	78.51	5679.74	1022.35	80264.94	6301601.2
0.20	27	SF	53.97	6704.81	1340.96	72371.71	3905901.6
0.22	27	SF	40.42	7677.18	1688.97	68268.55	2759415.0
0.24	27	SF	29.54	8794.75	2110.74	62351.25	1841856.2
0.26	27	SF	22.76	10082.22	2621.37	59662.54	1357919.5
0.28	27	SF	18.61	11299.15	3163.76	58877.61	1095712.3
0.30	27	SF	16.1	12507.3	3752.19	60410.2	972605.16
0.32	27	SF	13.03	13993.44	4477.90	58347.04	760262.02
0.34	27	SF	10.95	15410.39	5239.53	57372.88	628233.05
0.36	27	SF	9.68	16768.91	6036.80	58436.29	565663.36
0.38	27	SF	8.49	18206.98	6918.65	58739.35	498697.15
0.40	27	SF	7.38	19766.8	7906.72	58351.59	430634.76
0.42	27	SF	6.5	21443.63	9006.32	58541.10	380517.21
0.44	27	SF	5.85	23007.41	10123.2	59221.07	346443.2
0.46	27	SF	5.34	24407.32	11227.3	59954.14	320155.11
0.48	27	SF	4.93	26135.8	12545.1	61847.75	304909.44
0.50	27	SF	4.61	27938.46	13969.2	64398.15	296875.47
0.52	27	SF	4.34	29429.9	15303.5	66417.39	288251.50
0.54	27	SF	4	31218.73	16858.1	67432.45	269729.82
0.56	27	SF	3.77	32838.05	18389.3	69327.69	261365.39
0.58	27	SF	3.53	34602.98	20069.7	70846.14	250086.87
0.60	27	SF	3.31	36062.83	21637.6	71620.78	237064.78

Continued on next page

Table 24: RCA using FA static CMOS NAND (continued)

Voltage(V)	Temp(°C)	Corner	Pro. delay(nS)	I(Vdd)nA	P=VI (nW)	PDP (aJ)	EDP(aJ)*(nS)
0.62	27	SF	3.1	37861.49	23474.1	72769.78	225586.32
0.64	27	SF	2.95	39104.74	25027.0	73829.74	217797.75
0.66	27	SF	2.8	41004.31	27062.8	75775.96	212172.70
0.68	27	SF	2.65	42813.36	29113.0	77149.67	204446.6
0.70	27	SF	2.52	44286.2	31000.3	78120.85	196864.55
0.75	27	SF	2.27	56066.58	42049.9	95453.35	216679.11
0.80	27	SF	2.06	58433.76	46747.0	96298.83	198375.60
0.18	27	TT	55.66	5193.65	934.85	52034.14	2896220.2
0.20	27	TT	39.4	6144.77	1228.95	48420.78	1907779.0
0.22	27	TT	27.67	6982.29	1536.10	42503.99	1176085.4
0.24	27	TT	21.41	8112.43	1946.98	41684.91	892473.92
0.26	27	TT	16.92	9156.63	2380.72	40281.84	681568.84
0.28	27	TT	13.46	10449.15	2925.76	39380.75	530064.98
0.30	27	TT	11.08	11707.64	3512.29	38916.19	431191.44
0.32	27	TT	9.35	13027.35	4168.75	38977.83	364442.72
0.34	27	TT	8.04	14446.14	4911.68	39489.96	317499.34
0.36	27	TT	6.88	15654.15	5635.49	38772.19	266752.72
0.38	27	TT	6.04	17196.65	6534.72	39469.75	238397.29
0.40	27	TT	5.37	18779.84	7511.93	40339.09	216620.94
0.42	27	TT	4.84	20332.55	8539.67	41332.00	200046.9
0.44	27	TT	4.26	21711.52	9553.06	40696.07	173365.27
0.46	27	TT	3.93	23341.86	10737.2	42197.41	165835.8
0.48	27	TT	3.61	24475.33	11748.1	42410.85	153103.17
0.50	27	TT	3.3	25565.68	12782.8	42183.37	139205.12
0.52	27	TT	3.07	27369.23	14231.9	43692.23	134135.1
0.54	27	TT	2.86	29927.6	16160.9	46220.18	132189.73
0.56	27	TT	2.7	32020.27	17931.3	48414.64	130719.55
0.58	27	TT	2.55	33054.69	19171.7	48887.88	124664.11
0.60	27	TT	2.41	34760.06	20856.0	50263.04	121133.94
0.62	27	TT	2.32	36071.64	22364.4	51885.44	120374.2
0.64	27	TT	2.18	37868.47	24235.8	52834.08	115178.31
0.66	27	TT	2.05	39432.13	26025.2	53351.67	109370.92
0.68	27	TT	1.96	41333.91	28107.0	55089.83	107976.07
0.70	27	TT	1.87	43202.77	30241.9	56552.42	105753.03
0.75	27	TT	1.72	47496.5	35622.3	61270.48	105385.23
0.80	27	TT	1.56	51862.57	41490.0	64724.48	100970.20
0.18	27	FS	58.13	4804.07	864.73	50266.90	2922015.24
0.20	27	FS	40.15	5609.1	1121.82	45041.07	1808399.08
0.22	27	FS	26.23	6487.11	1427.16	37434.51	981907.38
0.24	27	FS	18.87	7436.05	1784.65	33676.38	635473.35
0.26	27	FS	15.79	8534.32	2218.92	35036.79	553231.02
0.28	27	FS	12.58	9655.91	2703.65	34011.97	427870.67
0.30	27	FS	9.45	10767.11	3230.13	30524.75	288458.95
0.32	27	FS	7.87	12088.82	3868.42	30444.48	239598.09
0.34	27	FS	6.59	13379.76	4549.11	29978.69	197559.56
0.36	27	FS	5.77	14611.7	5260.21	30351.42	175127.71
0.38	27	FS	5.12	16141.6	6133.80	31405.09	160794.09
0.40	27	FS	4.49	17764.11	7105.64	31904.34	143250.49
0.42	27	FS	4.01	18860.15	7921.26	31764.26	127374.70
0.44	27	FS	3.62	20448.01	8997.124	32569.59	117901.91

Continued on next page

Table 24: RCA using FA static CMOS NAND (continued)

Voltage(V)	Temp(°C)	Corner	Pro. delay(nS)	I(Vdd)nA	P=VI (nW)	PDP (aJ)	EDP(aJ)*(nS)
0.46	27	FS	3.3	22271.98	10245.11	33808.86	111569.25
0.48	27	FS	3.04	23875.19	11460.09	34838.67	105909.57
0.50	27	FS	2.82	25499.93	12749.96	35954.90	101392.82
0.52	27	FS	2.6	26832.54	13952.92	36277.59	94321.74
0.54	27	FS	2.44	28492.43	15385.91	37541.62	91601.56
0.56	27	FS	2.3	29422.53	16476.61	37896.21	87161.30
0.58	27	FS	2.18	31140.45	18061.46	39373.98	85835.28
0.60	27	FS	2.06	32520.78	19512.46	40195.68	82803.10
0.62	27	FS	1.98	33856.75	20991.18	41562.54	82293.84
0.64	27	FS	1.89	35661.63	22823.44	43136.30	81527.62
0.66	27	FS	1.81	37481.83	24738.00	44775.79	81044.18
0.68	27	FS	1.73	39314.98	26734.18	46250.14	80012.74
0.70	27	FS	1.66	40604.32	28423.02	47182.21	78322.48
0.75	27	FS	1.5	45126.97	33845.22	50767.84	76151.76
0.80	27	FS	1.38	49041.33	39233.06	54141.62	74715.44
0.18	27	FF	32.8	5919.59	1065.52	34949.25	1146335.70
0.20	27	FF	23.4	6888.61	1377.72	32238.69	754385.45
0.22	27	FF	17.86	8014.4	1763.16	31490.18	562414.62
0.24	27	FF	13.54	9192.86	2206.28	29873.11	404482.01
0.26	27	FF	10.32	10457.15	2718.85	28058.62	289565.00
0.28	27	FF	8.62	11957.19	3348.01	28859.87	248772.11
0.30	27	FF	7.27	13289.5	3986.85	28984.39	210716.58
0.32	27	FF	5.91	14887.28	4763.92	28154.82	166395.00
0.34	27	FF	5.17	16429.52	5586.03	28879.81	149308.61
0.36	27	FF	4.55	18153.23	6535.16	29734.99	135294.20
0.38	27	FF	4.02	19641.2	7463.65	30003.89	120615.66
0.40	27	FF	3.6	21526.72	8610.68	30998.47	111594.51
0.42	27	FF	3.21	23228.21	9755.84	31316.27	100525.23
0.44	27	FF	2.89	25091.88	11040.42	31906.83	92210.75
0.46	27	FF	2.63	27100	12466	32785.58	86226.07
0.48	27	FF	2.46	29197.18	14014.64	34476.03	84811.03
0.50	27	FF	2.32	30075.37	15037.68	34887.42	80938.83
0.52	27	FF	2.19	32105.17	16694.68	36561.36	80069.39
0.54	27	FF	2.04	35138.08	18974.56	38708.10	78964.54
0.56	27	FF	1.93	37002.41	20721.34	39992.20	77184.95
0.58	27	FF	1.82	38158.4	22131.87	40280.00	73309.61
0.60	27	FF	1.72	40272.03	24163.21	41560.73	71484.46
0.62	27	FF	1.64	42441.85	26313.94	43154.87	70773.99
0.64	27	FF	1.55	43999.24	28159.51	43647.24	67653.23
0.66	27	FF	1.48	46173.47	30474.49	45102.24	66751.32
0.68	27	FF	1.42	47720.62	32450.02	46079.03	65432.22
0.70	27	FF	1.37	49678.39	34774.87	47641.57	65268.95
0.75	27	FF	1.25	53981.76	40486.32	50607.9	63259.87
0.80	27	FF	1.14	64402.67	51522.13	58735.23	66958.16

F.2 RCA: Schmitt trigger CMOS NAND

Table 25 demonstrates the Propagation delay average current, average power, power delay product, and energy-delay product of 4bit ripple carry adder using Full adder(Schmitt trigger CMOS NAND gate).

Table 25: RCA using FA Schmitt trigger CMOS NAND

Voltage (V)	Temp (°C)	Corner	Pro. delay(nS)	I(Vdd)nA	P=VI(nW)	PDP (aJ)	EDP(aJ)*(nS)
0.179	27	SS	566.32	2637.81	474.80	268892.02	152278929.
0.20	27	SS	349.4	2940.46	588.09	205479.34	71794483.0
0.22	27	SS	241.75	3485.91	766.90	185398.12	44819996.3
0.24	27	SS	167.54	4054.59	973.10	163033.44	27314622.8
0.26	27	SS	122.34	4054.59	1054.19	128970.02	15778192.3
0.28	27	SS	84.89	5125.71	1435.19	121834.02	10342490.4
0.30	27	SS	69.45	5545.43	1663.62	115539.03	8024185.91
0.32	27	SS	55.84	6586.29	2107.61	117689.09	6571759.27
0.34	27	SS	44.15	6961.72	2366.98	104502.37	4613780.02
0.36	27	SS	36.84	8070.51	2905.38	107034.33	3943144.78
0.38	27	SS	31.98	8561.15	3253.23	104038.51	3327151.84
0.40	27	SS	28.06	9632.05	3852.82	108110.12	3033570.22
0.42	27	SS	23.92	10776.05	4525.94	108260.50	2589591.36
0.44	27	SS	21.07	11123.24	4894.22	103121.33	2172766.49
0.46	27	SS	18.78	12782.03	5879.73	110421.40	2073713.90
0.48	27	SS	17.57	13591.87	6524.09	114628.39	2014020.89
0.50	27	SS	15.66	14389.63	7194.81	112670.80	1764424.77
0.52	27	SS	14.57	15800.75	8216.39	119712.80	1744215.5
0.54	27	SS	13.32	16858.47	9103.573	121259.6	1615177.91
0.56	27	SS	11.9	18177.8	10179.56	121136.85	1441528.62
0.58	27	SS	11.3	19050.43	11049.24	124856.51	1410878.65
0.60	27	SS	10.5	21023.31	12613.98	132446.8	1390691.95
0.62	27	SS	9.93	21775.54	13500.83	134063.28	1331248.46
0.64	27	SS	9.29	22751.2	14560.76	135269.53	1256653.97
0.66	27	SS	8.57	23917.07	15785.26	135279.73	1159347.29
0.68	27	SS	8.36	25696.12	17473.36	146077.3	1221206.25
0.70	27	SS	7.91	26977.52	18884.26	149374.52	1181552.51
0.75	27	SS	6.91	30442.14	22831.60	157766.39	1090165.75
0.80	27	SS	6.59	34528.71	27622.96	182035.35	1199613.01
0.18	27	SF	351.95	3319.14	597.44	210270.83	74004821.4
0.201	27	SF	236.61	3690.67	738.13	174649.88	41323909.4
0.221	27	SF	167.15	4146.87	912.31	152492.85	25489179.9
0.241	27	SF	122.44	5173.84	1241.72	152036.39	18615335.9
0.261	27	SF	90.85	5368.02	1395.68	126798.00	11519598.3
0.28	27	SF	70.52	5993.7	1678.23	118349.20	8345985.77
0.30	27	SF	56.35	7126.8	2138.04	120478.5	6788966.51
[1]0.32	27	SF	44.45	7453.03	2384.96	106011.89	4712228.89
0.341	27	SF	36.09	8699.95	2957.98	106753.60	3852737.65
0.36	27	SF	31.95	9104.16	3277.49	104716.04	3345677.74
0.38	27	SF	25.96	10452.03	3971.77	103107.18	2676662.53
0.399	27	SF	23.42	11290.99	4516.39	105773.99	2477226.94
0.421	27	SF	20.02	12589.02	5287.38	105853.51	2119187.38
0.44	27	SF	18.04	13836.32	6087.98	109827.17	1981282.21
0.46	27	SF	15.9	15486.58	7123.82	113268.84	1800974.65
0.48	27	SF	15.26	17162.54	8238.01	125712.1	1918367.7
0.50	27	SF	13.9	17565.22	8782.61	122078.2	1696888.07
0.52	27	SF	12.37	19801.51	10296.7	127371.23	1575582.15
0.54	27	SF	11.75	20857.2	11262.8	132338.9	1554982.47
0.56	27	SF	10.82	21767.16	12189.6	131891.57	1427066.85
0.58	27	SF	9.87	23828.95	13820.7	136411.20	1346378.61
0.60	27	SF	9.38	25229.46	15137.6	141991.40	1331879.3

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Table 25: RCA using FA Schmitt trigger CMOS NAND (continued)

Voltage(V)	Temp(°C)	Corner	Pro. delay(nS)	I(Vdd)nA	P=VI (nW)	PDP (aJ)	EDP(aJ)*(nS)
0.62	27	SF	8.76	26980.68	16728.0	146537.46	1283668.2
0.64	27	SF	8.17	28635.55	18326.7	149729.56	1223290.53
0.66	27	SF	7.63	29828.12	19686.5	150208.44	1146090.44
0.68	27	SF	7.27	31683.31	21544.6	156629.61	1138697.27
0.70	27	SF	6.99	33308.21	23315.7	162977.07	1139209.7
0.75	27	SF	6.07	37681.67	28261.2	171545.80	1041283.02
0.80	27	SF	5.63	42494.28	33995.4	191394.23	1077549.55
0.18	27	TT	282.29	2919.9	525.58	148366.5	41882391.3
0.20	27	TT	182.33	3457.95	691.59	126097.6	22991376.2
0.221	27	TT	127.94	3783.93	832.464	106505.5	13626316.3
[1]0.24	27	TT	89.97	4227.84	1014.68	91290.90	8213442.59
[1]0.262	27	TT	63.04	4740.08	1232.42	77691.80	4897691.52
0.28	27	TT	50.92	5702.41	1596.67	81302.68	4139932.50
0.30	27	TT	40.13	6428.8	1928.64	77396.32	3105914.4
0.32	27	TT	32.07	7713.09	2468.18	79154.81	2538494.91
0.34	27	TT	27.02	8590.7	2920.83	78921.04	2132446.57
0.36	27	TT	22.03	9324.22	3356.71	73948.52	1629085.98
0.38	27	TT	18.11	10243.34	3892.46	70492.61	1276621.29
0.401	27	TT	15.89	11489.66	4595.86	73028.27	1160419.35
0.42	27	TT	14.25	12772.96	5364.64	76446.16	1089357.8
0.44	27	TT	12.68	13916.98	6123.47	77645.61	984546.39
0.46	27	TT	11.35	14905.33	6856.45	77820.72	883265.26
0.48	27	TT	10.33	16593.58	7964.91	82277.60	849927.68
0.50	27	TT	9.7	17714.55	8857.27	85915.56	833381.00
0.52	27	TT	8.89	19512.97	10146.7	90204.55	801918.51
0.54	27	TT	8.16	21110.4	11399.6	93020.86	759050.27
0.56	27	TT	7.28	21825.27	12222.1	88977.26	647754.45
0.58	27	TT	7.13	23188.49	13449.3	95893.68	683721.94
0.60	27	TT	6.63	25034.08	15020.4	99585.57	660252.33
0.62	27	TT	6.43	25678.71	15920.8	102370.7	658243.89
0.64	27	TT	5.9	27719.69	17740.6	104669.5	617550.34
0.66	27	TT	5.6	29462.65	19445.3	108893.9	609806.14
0.68	27	TT	5.46	31465.94	21396.8	116826.7	637874.01
0.70	27	TT	5.12	32898.27	23028.7	117907.3	603685.88
0.75	27	TT	4.66	36579.27	27434.4	127844.5	595755.59
0.80	27	TT	4.33	40952.51	32762.0	141859.4	614251.61
[1]0.181	27	FS	343.36	2849.65	512.93	176122.04	176122.04
0.20	27	FS	221.43	2941.73	588.34	130277.45	130277.45
0.22	27	FS	145.51	3425.03	753.50	109642.74	109642.74
0.24	27	FS	99.54	3983.66	956.07	95168.04	95168.04
0.261	27	FS	67.53	4518.69	1174.85	79338.25	79338.25
0.28	27	FS	51.23	5188.18	1452.69	74421.32	74421.32
0.30	27	FS	38.84	5873.48	1762.04	68437.78	68437.78
0.32	27	FS	28.21	6904.7	2209.50	62330.10	62330.10
0.34	27	FS	24.32	7749.04	2634.67	64075.26	64075.26
0.36	27	FS	20.07	8821.6	3175.77	63737.82	63737.82
0.38	27	FS	16.95	9628.95	3659.00	62020.06	62020.06
0.40	27	FS	14.49	11221.96	4488.78	65042.48	65042.48
0.42	27	FS	12.71	11999.79	5039.91	64057.27	64057.27
0.44	27	FS	11.36	13135.96	5779.82	65658.78	65658.78

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Table 25: RCA using FA Schmitt trigger CMOS NAND (continued)

Voltage(V)	Temp(°C)	Corner	Pro. delay(nS)	I(Vdd)nA	P=VI (nW)	PDP (aJ)	EDP(aJ)*(nS)
0.46	27	FS	9.78	15087.28	6940.14	67874.65	67874.65
0.48	27	FS	9.25	16082.01	7719.36	71404.12	71404.12
0.50	27	FS	8.44	17455.87	8727.93	73663.77	73663.77
0.52	27	FS	7.75	18794.42	9773.09	75741.51	75741.51
0.54	27	FS	7.12	20078.44	10842.35	77197.58	77197.58
0.56	27	FS	6.61	21734.99	12171.59	80454.23	80454.23
0.579	27	FS	6.19	22512.47	13057.23	80824.26	80824.26
0.60	27	FS	5.79	24019.04	14411.42	83442.14	83442.14
0.62	27	FS	5.4	25034.86	15521.61	83816.71	83816.71
0.641	27	FS	5.03	26425.77	16912.49	85069.83	85069.83
0.661	27	FS	4.38	28860.79	19048.12	83430.77	83430.77
0.68	27	FS	4.63	29841.81	20292.43	93953.95	93953.95
0.70	27	FS	4.33	31962.13	22373.49	96877.21	96877.21
0.75	27	FS	4.02	35889.82	26917.36	108207.80	108207.80
0.80	27	FS	3.66	40614.26	32491.40	118918.55	118918.55
0.18	27	FF	158	3470.25	624.64	98693.91	15593637.78
0.201	27	FF	107.2	3754.78	750.95	80502.48	8629866.19
0.221	27	FF	74.42	4387.12	965.16	71827.68	5345416.20
0.241	27	FF	55.87	5053.22	1212.77	67757.61	3785618.02
[1]0.259	27	FF	41.66	5782.01	1503.32	62628.41	2609099.95
0.28	27	FF	31.44	6636.03	1858.08	58418.29	1836671.33
0.30	27	FF	25.29	7323	2196.9	55559.60	1405102.30
0.32	27	FF	20.64	8586.84	2747.78	56714.36	1170584.40
0.341	27	FF	17.06	9872.85	3356.76	57266.47	976966.13
0.36	27	FF	14.59	11220.14	4039.25	58932.66	859827.55
0.38	27	FF	12.16	12381.34	4704.90	57211.69	695694.22
0.40	27	FF	11.07	13617.14	5446.85	60296.69	667484.42
0.42	27	FF	9.75	15204.69	6385.96	62263.20	607066.25
0.44	27	FF	8.72	16815.66	7398.89	64518.32	562599.78
0.46	27	FF	7.92	18954.81	8719.21	69056.16	546924.81
0.48	27	FF	7.2	19784.79	9496.69	68376.23	492308.88
0.50	27	FF	6.36	21545.63	10772.81	68515.10	435756.05
0.52	27	FF	5.9	22941	11929.32	70382.98	415259.62
0.54	27	FF	5.47	24524.02	13242.97	72439.05	396241.60
0.56	27	FF	5.27	26688.76	14945.70	78763.86	415085.58
0.58	27	FF	4.98	28339.91	16437.14	81856.99	407647.84
0.60	27	FF	4.72	30231.38	18138.82	85615.26	404104.06
0.62	27	FF	4.43	31574.56	19576.22	86722.68	384181.50
0.64	27	FF	4.26	33172.5	21230.4	90441.50	385280.80
0.66	27	FF	4.03	35065.81	23143.43	93268.04	375870.20
0.68	27	FF	3.92	37161.75	25269.99	99058.36	388308.77
0.70	27	FF	3.77	39246.79	27472.75	103572.27	390467.49
0.75	27	FF	3.34	44584.58	33438.43	111684.37	373025.80
0.80	27	FF	3.01	50539.63	40431.70	121699.42	366315.28

[1]Got error: reduce GMIN=10^{-11}.

F.3 RCA: static CMOS XOR

Table 26 demonstrates the Propagation delay average current, average power, power delay product, and energy-delay product of 4bit ripple carry adder using Full adder(CMOS XOR gate).

Table 26: RCA using FA static CMOS XOR

Voltage (V)	Temp (°C)	Corner	Pro. delay(nS)	I(Vdd)nA	P=VI(nW)	PDP (aJ)	EDP(aJ)*(nS)
0.18	27	SS	113.38	8017.35	1443.12	163621.28	18551381.38
0.20	27	SS	81.95	9070.07	1814.01	148658.44	12182559.76
0.22	27	SS	58.47	11010.1	2422.22	141627.32	8280949.42
0.24	27	SS	45.34	12347.12	2963.30	134356.42	6091720.1
0.26	27	SS	35.53	13874.29	3607.31	128167.91	4553806.0
0.28	27	SS	28.54	15626.7	4375.47	124876.08	3563963.4
0.30	27	SS	22.14	16830.53	5049.15	111788.38	2474994.7
0.32	27	SS	18.41	19337.83	6188.10	113923.02	2097322.8
0.34	27	SS	15.86	21065.96	7162.42	113596.08	1801633.8
0.36	27	SS	13.68	22826.38	8217.49	112415.35	1537842.0
0.38	27	SS	11.99	24530.09	9321.43	111763.99	1340050.3
0.40	27	SS	10.53	26398.35	10559.3	111189.85	1170829.1
0.42	27	SS	9.47	28546.52	11989.5	113540.92	1075232.5
0.44	27	SS	8.35	31030.26	13653.3	114005.17	951943.21
0.46	27	SS	7.73	32004	14721.8	113799.82	879672.63
0.48	27	SS	7.08	35020.82	16809.9	119014.75	842624.46
0.50	27	SS	6.31	37142.04	18571.0	117183.13	739425.58
0.52	27	SS	5.89	38923.15	20240.0	119213.82	702169.42
0.54	27	SS	5.57	39770.14	21475.8	119620.62	666286.89
0.56	27	SS	5.18	41752.84	23381.5	121116.63	627384.18
0.58	27	SS	4.88	45310.07	26279.8	128245.62	625838.63
0.60	27	SS	4.62	47328.14	28396.8	131193.60	606114.45
0.62	27	SS	4.36	48459.02	30044.5	130994.42	571135.68
0.64	27	SS	4.15	50868.47	32555.8	135106.65	560692.62
0.66	27	SS	3.95	51836.31	34211.9	135137.26	533792.17
0.68	27	SS	3.78	54072.02	36768.9	138986.72	525369.80
0.70	27	SS	3.59	57864.74	40505.3	145414.09	522036.58
0.75	27	SS	3.23	62099.03	46574.2	150434.90	485904.72
0.80	27	SS	2.96	67030.01	53624.0	158727.06	469832.10
0.18	27	SF	85.5	9690.59	1744.30	149138.18	12751314.4
0.20	27	SF	61.01	11413.79	2282.75	139271.06	8496927.7
0.22	27	SF	48.45	13548.4	2980.64	144412.39	6996780.5
0.24	27	SF	37.21	15207.91	3649.89	135812.71	5053591.2
0.26	27	SF	29.42	17349.99	4510.99	132713.54	3904432.4
0.28	27	SF	22.68	19099.3	5347.80	121288.19	2750816.2
0.30	27	SF	18.35	21448.99	6434.69	118076.69	2166707.2
0.32	27	SF	15.41	23827.17	7624.69	117496.54	1810621.6
0.34	27	SF	13.51	25843.3	8786.72	118708.61	1603753.3
0.36	27	SF	11.48	28428.51	10234.2	117489.34	1348777.6
0.38	27	SF	9.93	31304.32	11895.6	118123.72	1172968.5
0.40	27	SF	9.1	32993.61	13197.4	120096.74	1092880.3
0.42	27	SF	8.13	34790.8	14612.1	118796.66	965816.89
0.44	27	SF	7.41	37534.12	16515.0	122376.24	906807.97
0.46	27	SF	6.56	39254.19	18056.9	118453.44	777054.59
0.48	27	SF	6.12	41435.9	19889.2	121722.09	744939.25
0.50	27	SF	5.59	43919.29	21959.6	122754.41	686197.18
0.52	27	SF	5.27	46730	24299.	128058.89	674870.36
0.54	27	SF	4.83	48395.18	26133.3	126224.30	609663.40
0.56	27	SF	4.63	48391.93	27099.4	125470.59	580928.86
0.58	27	SF	4.37	52079.3	30205.9	132000.19	576840.84
0.60	27	SF	4.04	55942.64	33565.5	135604.95	547844.03

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Table 26: RCA using FA static CMOS XOR

Voltage(V)	Temp(°C)	Corner	Pro. delay(nS)	I(Vdd)nA	P=VI (nW)	PDP (aJ)	EDP(aJ)*(nS)
0.62	27	SF	3.79	58198.39	36083.0	136754.57	518299.84
0.64	27	SF	3.6	58666.17	37546.3	135166.85	486600.68
0.66	27	SF	3.47	60609.26	40002.1	138807.32	481661.42
0.68	27	SF	3.3	70914.08	48221.5	159131.19	525132.94
0.70	27	SF	3.15	74319.2	52023.4	163873.83	516202.58
0.75	27	SF	2.88	77706.77	58280.0	167846.62	483398.27
0.80	27	SF	2.63	83779.65	67023.7	176272.38	463596.36
0.18	27	TT	60.33	8982.4	1616.8	97543.47	5884797.8
0.20	27	TT	45.54	10205.79	2041.1	92954.33	4233140.4
0.22	27	TT	32.82	12119.33	2666.25	87506.41	2871960.3
0.24	27	TT	24.7	13592.9	3262.2	80578.71	1990294.1
0.26	27	TT	20.12	15773.7	4101.1	82515.37	1660209.4
0.28	27	TT	16.32	17639.78	4939.13	80606.73	1315501.9
0.30	27	TT	13.47	19137.39	5741.2	77334.19	1041691.5
0.32	27	TT	10.91	21554.95	6897.5	75252.64	821006.31
0.34	27	TT	9.09	24046.21	8175.71	74317.21	675543.49
0.36	27	TT	7.87	26177.2	9423.7	74165.24	583680.46
0.38	27	TT	7.08	28655.66	10889.1	77095.18	545833.92
0.40	27	TT	6.32	30972.47	12388.9	78298.40	494845.91
0.42	27	TT	5.75	32241.16	13541.2	77862.40	447708.80
0.44	27	TT	5.24	35456.77	15600.9	81749.12	428365.43
0.46	27	TT	4.76	37715.9	17349.3	82582.73	393093.81
0.48	27	TT	4.26	39094.36	18765.2	79940.14	340545.02
0.50	27	TT	4.06	41715.59	20857.7	84682.64	343811.54
0.52	27	TT	3.79	43784.68	22768.0	86290.84	327042.31
0.54	27	TT	3.55	45748.52	24704.2	87699.91	311334.69
0.56	27	TT	3.34	48593.22	27212.2	90888.75	303568.45
0.58	27	TT	3.14	51888.1	30095.0	94498.60	296725.62
0.60	27	TT	2.95	53145.02	31887.0	94066.68	277496.72
0.62	27	TT	2.79	55065.33	34140.5	95252.00	265753.10
0.64	27	TT	2.63	57637.28	36887.8	97015.06	255149.63
0.66	27	TT	2.5	60249.75	39764.8	99412.08	248530.21
0.68	27	TT	2.4	62064.79	42204.0	101289.7	243095.36
0.70	27	TT	2.3	64632.17	45242.5	104057.7	239332.92
0.75	27	TT	2.11	70615.15	52961.3	111748.4	235789.28
0.80	27	TT	1.95	83737.29	66989.8	130630.1	254728.83
0.18	27	FS	63.18	8273.38	1489.20	94088.18	5944491.63
0.20	27	FS	40.63	9567.99	1913.59	77749.48	3158961.64
0.22	27	FS	30.8	11138.78	2450.53	75476.37	2324672.29
0.24	27	FS	23.23	12602.38	3024.57	70260.78	1632158.12
0.26	27	FS	17.18	14270.68	3710.37	63744.27	1095126.61
0.28	27	FS	14.14	16198.98	4535.71	64135.00	906868.92
0.30	27	FS	11.41	17967.47	5390.24	61502.64	701745.23
0.32	27	FS	9.53	19982.48	6394.39	60938.57	580744.58
0.34	27	FS	7.99	21848.47	7428.47	59353.55	474234.89
0.36	27	FS	6.93	23866.51	8591.94	59542.16	412627.23
0.38	27	FS	6.06	26151.84	9937.69	60222.45	364948.09
0.40	27	FS	5.27	28412.36	11364.94	59893.25	315637.45
0.42	27	FS	4.74	30768.46	12922.75	61253.85	290343.24
0.44	27	FS	4.33	32713.27	14393.83	62325.32	269868.64

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Table 26: RCA using FA static CMOS XOR

Voltage(V)	Temp(°C)	Corner	Pro. delay(nS)	I(Vdd)nA	P=VI (nW)	PDP (aJ)	EDP(aJ)*(nS)
0.46	27	FS	3.95	35010.93	16105.02	63614.85	251278.69
0.48	27	FS	3.63	37087.67	17802.08	64621.55	234576.24
0.50	27	FS	3.4	39465.17	19732.58	67090.78	228108.68
0.52	27	FS	3.17	41977.22	21828.15	69195.24	219348.94
0.54	27	FS	2.96	42805.8	23115.13	68420.79	202525.54
0.56	27	FS	2.77	46755.81	26183.25	72527.61	200901.48
0.58	27	FS	2.61	47558.17	27583.73	71993.55	187903.18
0.60	27	FS	2.47	49532.74	29719.64	73407.52	181316.57
0.62	27	FS	2.35	53549.02	33200.39	78020.92	183349.16
0.64	27	FS	2.24	54776.79	35057.14	78528.00	175902.73
0.66	27	FS	2.14	57426.98	37901.80	81109.86	173575.11
0.68	27	FS	2.06	60046.31	40831.49	84112.87	173272.51
0.70	27	FS	1.98	61997.04	43397.92	85927.89	170137.23
0.75	27	FS	1.8	68196.44	51147.33	92065.19	165717.34
0.80	27	FS	1.66	75038.63	60030.90	99651.30	165421.15
0.18	27	FF	36.38	9846.13	1772.30	64476.39	2345651.34
0.20	27	FF	27.16	11843.11	2368.62	64331.77	1747250.96
0.22	27	FF	20.9	13845.23	3045.95	63660.36	1330501.68
0.24	27	FF	16.05	15582.86	3739.88	60025.17	963404.08
0.26	27	FF	11.93	18010.99	4682.85	55866.48	666487.21
0.28	27	FF	9.93	20264.24	5673.98	56342.69	559482.94
0.30	27	FF	8.56	22804.21	6841.26	58561.21	501283.96
0.32	27	FF	7.3	24971.73	7990.95	58333.96	425837.91
0.34	27	FF	6.34	27674.71	9409.40	59655.60	378216.53
0.36	27	FF	5.36	30098.31	10835.39	58077.69	311296.46
0.38	27	FF	4.85	32051.97	12179.74	59071.78	286498.13
0.40	27	FF	4.24	35240.17	14096.06	59767.32	253413.47
0.42	27	FF	3.85	37621.53	15801.04	60834.01	234210.95
0.44	27	FF	3.56	39995.43	17597.98	62648.84	223029.87
0.46	27	FF	3.27	42939.51	19752.17	64589.61	211208.02
0.48	27	FF	3.04	45937.02	22049.76	67031.29	203775.15
0.50	27	FF	2.85	48288.84	24144.42	68811.59	196113.05
0.52	27	FF	2.66	51002.09	26521.08	70546.09	187652.60
0.54	27	FF	2.51	53534.46	28908.60	72560.60	182127.12
0.56	27	FF	2.35	55088.65	30849.64	72496.66	170367.15
0.58	27	FF	2.23	57235.66	33196.68	74028.60	165083.78
0.60	27	FF	2.1	59733.78	35840.26	75264.56	158055.58
0.62	27	FF	2.01	62225.71	38579.94	77545.67	155866.81
0.64	27	FF	1.91	65009.65	41606.17	79467.79	151783.49
0.66	27	FF	1.82	67765.82	44725.44	81400.30	148148.55
0.68	27	FF	1.76	79973.6	54382.04	95712.40	168453.83
0.70	27	FF	1.7	80982.52	56687.76	96369.198	163827.63
0.75	27	FF	1.56	87383.88	65537.91	102239.13	159493.05
0.80	27	FF	1.44	94085.42	75268.33	108386.40	156076.42

F.4 RCA: Schmitt trigger CMOS XOR

Table 27 demonstrates the Propagation delay average current, average power, power delay product, and energy-delay product of 4bit ripple carry adder using Full adder(Schmitt trigger CMOS XOR gate).

Table 27: RCA using FA Schmitt trigger CMOS XOR

Voltage (V)	Temp (°C)	Corner	Pro. delay(nS)	I(Vdd)nA	P=VI(nW)	PDP (aJ)	EDP(aJ)*(nS)
0.18	27	SS	588.69	3827.28	688.91	405554.66	238745974.8
0.20	27	SS	377.54	4256.64	851.32	321410.37	121345272.3
0.22	27	SS	256.83	4618.25	1016.01	260943.13	67018024.71
0.241	27	SS	171.39	5519.94	1324.78	227055.00	38914957.13
0.26	27	SS	123.17	5881.07	1529.07	188336.56	23197414.33
0.28	27	SS	88.61	6542.54	1831.91	162325.65	14383675.97
0.30	27	SS	70.73	7324.53	2197.35	155419.20	10992800.16
0.32	27	SS	57.92	8401.73	2688.55	155721.02	9019361.74
0.34	27	SS	44.29	9615.56	3269.29	144796.87	6413053.45
0.36	27	SS	36.87	10023.81	3608.57	133048.03	4905481.04
0.38	27	SS	30.82	11165.8	4243.00	130769.38	4030312.39
0.40	27	SS	26.86	12086.68	4834.67	129859.28	3488020.52
0.42	27	SS	23.46	13213.12	5549.51	130191.51	3054292.91
0.44	27	SS	20.46	13951.41	6138.62	125596.17	2569697.70
0.46	27	SS	19.27	15296.01	7036.16	135586.89	2612759.40
0.48	27	SS	16.82	16985.81	8153.18	137136.63	2306638.21
0.501	27	SS	15.18	17655.77	8827.88	134007.29	2034230.72
0.52	27	SS	14.19	18607.39	9675.84	137300.20	1948289.97
0.54	27	SS	12.21	21102.88	11395.55	139139.72	1698896.09
0.56	27	SS	11.86	21284.24	11919.17	141361.40	1676546.30
0.58	27	SS	11.14	22347.96	12961.81	144394.63	1608556.28
0.60	27	SS	10.56	23855.3	14313.18	151147.18	1596114.22
0.62	27	SS	9.44	25289.32	15679.37	148013.33	1397245.85
0.64	27	SS	9.19	27121.33	17357.65	159516.81	1465959.52
0.66	27	SS	8.57	28539.31	18835.94	161424.04	1383404.06
0.68	27	SS	8.24	29528.74	20079.54	165455.43	1363352.79
0.70	27	SS	8.16	31796.79	22257.75	181623.26	1482045.83
0.75	27	SS	7.29	34667.82	26000.86	189546.30	1381792.57
0.80	27	SS	6.29	38465.87	30772.69	193560.25	1217494.02
0.18	27	SF	364.2	4274.99	769.48	280251.24	102067503.2
0.20	27	SF	254.14	4906.26	981.25	249375.38	63376259.91
0.22	27	SF	176.11	5533.2	1217.30	214379.40	37754357.44
0.24	27	SF	119.91	6621.28	1589.10	190549.84	22848831.84
0.26	27	SF	91.33	7269.83	1890.15	172627.92	15766108.78
0.28	27	SF	68.82	7969.62	2231.49	153571.38	10568783.03
0.30	27	SF	53.56	9370.4	2811.12	150563.58	8064185.73
0.32	27	SF	46.4	9494.18	3038.13	140969.58	6540988.727
0.34	27	SF	36.32	10450.76	3553.25	129054.34	4687253.81
0.36	27	SF	31.71	12442.13	4479.16	142034.37	4503910.16
0.38	27	SF	28.08	13483.64	5123.78	143875.83	4040033.37
0.40	27	SF	22.35	14468.85	5787.54	129351.5	2891006.45
0.42	27	SF	19.72	16738.86	7030.32	138637.93	2733940.06
0.44	27	SF	17.96	17712.24	7793.38	139969.20	2513846.92
0.461	27	SF	15.34	18731.4	8616.44	132176.2	2027583.69
0.48	27	SF	14.42	20380.83	9782.79	141067.95	2034199.88
0.50	27	SF	13.27	21567.15	10783.5	143098.04	1898910.99
0.52	27	SF	11.61	23615.52	12280.0	142571.61	1655256.47
0.54	27	SF	11.04	24428.22	13191.2	145631.27	1607769.29
0.56	27	SF	10.32	26218.34	14682.2	151521.03	1563697.03
0.58	27	SF	9.3	27861.72	16159.7	150286.11	1397660.89
0.60	27	SF	9.27	29586.93	17752.1	164562.50	1525494.41

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Table 27: RCA: Schmitt trigger CMOS XOR (continued)

Voltage(V)	Temp(°C)	Corner	Pro. delay(nS)	I(Vdd)nA	P=VI (nW)	PDP (aJ)	EDP(aJ)*(nS)
0.62	27	SF	8.77	31267.6	19385.9	170014.44	1491026.71
0.64	27	SF	8.12	33707.83	21573.0	175172.85	1422403.55
0.66	27	SF	7.4	34926.39	23051.4	170580.48	1262295.61
0.68	27	SF	7.28	36557.32	24858.9	180973.35	1317486.03
0.70	27	SF	6.55	38683.25	27078.2	177362.70	1161725.69
0.75	27	SF	6.12	43848.19	32886.1	201263.19	1231730.73
0.80	27	SF	5.51	48328.76	38663.0	213033.17	1173812.78
0.18	27	TT	308.56	4101.26	738.22	227787.2	70286037.3
0.20	27	TT	199.53	4631.67	926.33	184831.4	36879413.8
0.22	27	TT	137.04	5440.62	1196.93	164028.1	22478419.6
0.24	27	TT	96.84	5870.31	1408.87	136435.3	13212403.8
0.26	27	TT	69.08	6443.19	1675.22	115724.8	7994272.42
0.28	27	TT	52.93	7560.79	2117.02	112053.9	5931014.62
0.30	27	TT	41.33	8037.3	2411.19	99654.48	4118719.77
0.32	27	TT	32.02	9415.23	3012.87	96472.21	3089040.25
0.34	27	TT	26.06	10386.62	3531.45	92029.60	2398291.58
0.36	27	TT	23.16	11815.75	4253.67	98514.99	2281607.33
0.38	27	TT	18.87	13054.45	4960.69	93608.23	1766387.47
0.40	27	TT	17.49	13823.11	5529.24	96706.47	1691396.29
0.42	27	TT	14.32	16145.05	6780.92	97102.78	1390511.93
0.44	27	TT	13.39	16870.27	7422.91	99392.88	1330870.7
0.46	27	TT	11.85	18354.85	8443.23	100052.2	1185619.60
0.481	27	TT	10.86	19459.41	9340.51	101438.0	1101616.81
0.50	27	TT	10.07	20974.77	10487.3	105607.9	1063472.22
0.52	27	TT	9.1	22255.89	11573.0	105314.8	958365.33
0.54	27	TT	8.35	23769.22	12835.3	107175.4	894914.69
0.56	27	TT	7.86	26024.74	14573.8	114550.4	900366.89
0.58	27	TT	7.45	28035.29	16260.4	121140.4	902496.63
0.60	27	TT	7.04	29685.98	17811.5	125393.5	882770.79
0.62	27	TT	6.57	31025.96	19236.0	126381.1	830324.12
0.64	27	TT	6.24	32630.1	20883.2	130311.5	813144.18
0.66	27	TT	5.78	34117.84	22517.7	130152.7	752282.81
0.68	27	TT	5.54	36267.48	24661.8	136626.8	756912.75
0.70	27	TT	5.37	37869.91	26508.9	142352.9	764435.56
0.75	27	TT	4.43	42246.85	31685.1	140365.1	621817.65
0.80	27	TT	4	47586.92	38069.5	152278.	609112.57
0.18	27	FS	382.34	3927.37	706.92	270286.31	103341270.2
0.20	27	FS	241.21	4458.94	891.78	215108.18	51886244.94
0.22	27	FS	162.37	4802.91	1056.64	171566.66	27857280.09
0.24	27	FS	106.19	5415.33	1299.67	138012.93	14655593.49
0.26	27	FS	75.14	6317.6	1642.57	123423.16	9274016.29
0.28	27	FS	53.74	6662.63	1865.53	100253.92	5387645.99
0.30	27	FS	39.6	7909.04	2372.71	93959.39	3720792.05
0.32	27	FS	30.79	9010.23	2883.27	88775.99	2733412.86
0.33	27	FS	25.19	9757.96	3317.70	83573.02	2105204.48
0.36	27	FS	21.32	10937.22	3937.39	83945.35	1789714.88
0.38	27	FS	17.74	12390.23	4708.28	83525.01	1481733.82
0.40	27	FS	14.21	13639.6	5455.84	77527.48	1101665.58
0.42	27	FS	12.64	14802.49	6217.04	78583.45	993294.92
0.44	27	FS	11.55	15690.33	6903.74	79738.25	920976.86

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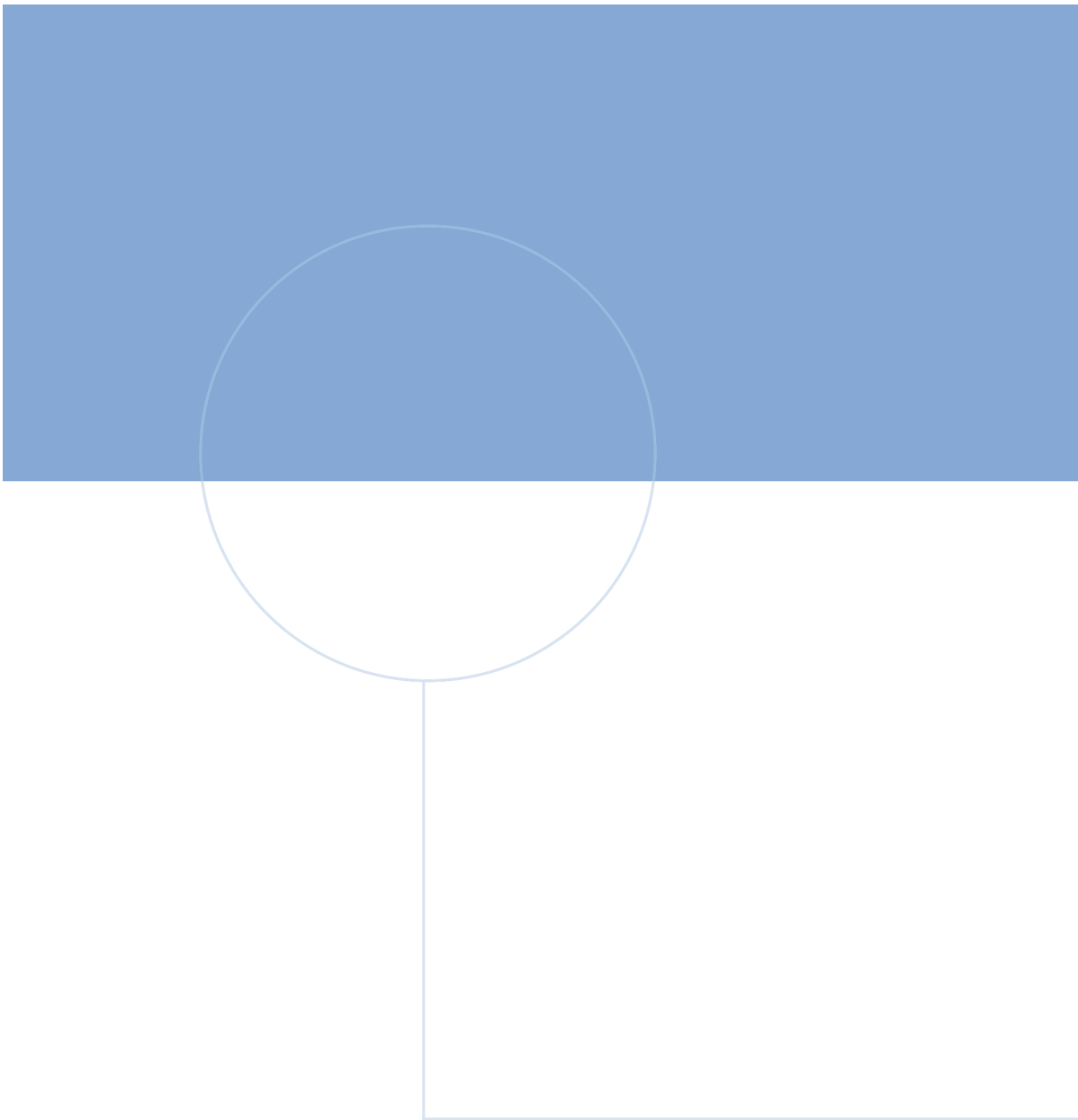
Table 27: RCA: Schmitt trigger CMOS XOR (continued)

Voltage(V)	Temp(°C)	Corner	Pro. delay(nS)	I(Vdd)nA	P=VI (nW)	PDP (aJ)	EDP(aJ)*(nS)
0.46	27	FS	10.37	17325.1	7969.54	82644.19	857020.27
0.48	27	FS	9.07	18853.74	9049.79	82081.64	744480.49
0.50	27	FS	8.2	19931.1	9965.55	81717.51	670083.58
0.52	27	FS	7.62	21677.56	11272.33	85895.16	654521.14
0.54	27	FS	7.05	23164.95	12509.07	88188.96	621732.20
0.56	27	FS	6.52	24705.08	13834.84	90203.18	588124.78
0.58	27	FS	6.26	26675.76	15471.94	96854.34	606308.22
0.60	27	FS	5.68	27738.7	16643.22	94533.48	536950.22
0.62	27	FS	5.37	29195.26	18101.06	97202.69	521978.49
0.64	27	FS	5.1	30468.32	19499.72	99448.59	507187.84
0.66	27	FS	4.97	32560.6	21489.99	106805.28	530822.24
0.68	27	FS	4.75	34302.56	23325.74	110797.26	526287.02
0.70	27	FS	4.58	35916.7	25141.69	115148.94	527382.14
0.75	27	FS	4.09	40553.3	30414.97	124397.24	508784.74
0.80	27	FS	3.7	44878.24	35902.59	132839.59	491506.48
0.18	27	FF	173.92	4352.71	783.48	136264.1	23699069.35
0.20	27	FF	118.59	5021.57	1004.31	119101.5	14124258.42
0.22	27	FF	78.7	5867.36	1290.81	101587.4	7994933.97
0.24	27	FF	57.55	6738.01	1617.12	93065.39	5355913.43
0.26	27	FF	43.35	7380.13	1918.83	83181.44	3605915.65
0.28	27	FF	31.95	8852.41	2478.67	79193.65	2530237.43
0.30	27	FF	26.83	9852.36	2955.70	79301.64	2127663.15
0.32	27	FF	20.97	10662.34	3411.94	71548.56	1500373.43
0.34	27	FF	16.87	12093.06	4111.64	69363.37	1170160.11
0.36	27	FF	13.71	13752.9	4951.04	67878.81	930618.52
0.38	27	FF	12.6	15529.6	5901.24	74355.72	936882.13
0.40	27	FF	10.74	16895.7	6758.28	72583.92	779551.37
0.42	27	FF	9.71	18905.22	7940.19	77099.26	748633.89
0.44	27	FF	8.94	19812.18	8717.35	77933.19	696722.72
0.46	27	FF	8.01	21378.55	9834.133	78771.40	630958.95
0.48	27	FF	6.88	23348.09	11207.08	77104.73	530480.55
0.50	27	FF	6.36	24923.67	12461.83	79257.27	504076.24
0.52	27	FF	5.99	26935.8	14006.61	83899.62	502558.78
0.54	27	FF	5.56	28517.63	15399.52	85621.33	476054.60
0.56	27	FF	5.14	30362.36	17002.92	87395.01	449210.38
0.58	27	FF	4.97	32454.43	18823.56	93553.13	464959.10
0.60	27	FF	4.71	34371.77	20623.06	97134.62	457504.06
0.62	27	FF	4.3	36255.02	22478.11	96655.88	415620.29
0.64	27	FF	4.14	38411.77	24583.53	101775.8	421351.91
0.66	27	FF	3.84	40784.99	26918.09	103365.4	396923.43
0.68	27	FF	3.66	42772.45	29085.26	106452.0	389614.58
0.70	27	FF	3.53	45124.87	31587.40	111503.5	393607.54
0.75	27	FF	3.17	49896	37422	118627.7	376049.93
0.80	27	FF	2.92	55678.22	44542.57	130064.3	379787.82



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