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Doctoral thesis

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Thesis for the Degree of Philosophiae Doctor
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Chapter 1

Introduction

Increase in greenhouse gases (GhG) – and in particular carbon dioxide CO_2 and methane CH_4 levels – of the Earth's atmosphere have become a major concern in the recent years due to its role in climate change. The 2015 Paris Agreement goal of limiting the global warming below 2°C – aiming for 1.5°C – necessitates significant decarbonization of key industries [1]. The United Nations (UN) sets targets of $\sim 45\%$ reduction in GhG by 2030 and net-zero – meaning cutting GhG emission close to zero with remaining emission reabsorbed by the atmosphere – by 2050 to reach the Paris Agreement. Even though GhG emissions are country dependent, the following industry sectors are key drivers of global and local GhG emissions [2, 3]

- *energy generation* – electricity and heat generation from fossil fuels such as coal, oil and natural gas.
- *Manufacturing* – such as cement, metal and chemical production and refinement, and the use of fossil fuels as energy source and raw materials.
- *Agriculture and deforestation* – production of food, feed and timber, release of stored CO_2 by deforestation and CH_4 through agricultural practices.
- *Transportation* – comprising use and manufacturing within automotive, maritime, aerospace and railway sectors.
- *Commercial and residential buildings* – in particular the use of fossil fuels in heating of buildings and water.

Electricity generation is the largest driver of CO_2 emissions world-wide, accounting for $\sim 40\%$ [2, 3, 4]. Introduction of renewable electricity sources (RES) is thus integral to reach net-zero. Increase in investment and deployment of wind and solar photovoltaic (PV) electricity generation is projected to be a significant contributor to the decarbonization of the grid-connected electricity production by 2050 [4, 5]. Electricity generation from PV solar and wind is expected to double in the next five years and provide $\sim 20\%$ of global power generation by 2027, with wind and PV solar account for $\sim 80\%$ of global renewable generation increase, while investments in hydropower, bioenergy, geothermal and concentrated solar are expected to remain limited [6]. For the net-zero scenario, an estimated 38% share of generated electricity being PV solar and 31% from wind, while the share of fossil fuels is projected to be reduced to 12% [5] by 2050. Furthermore, a $\sim 7\%$ increase in energy efficiency is required for a $\sim 40\%$ larger world economy [4] if net-zero is to be reached. Increase of energy efficiency is a major factor towards reaching net-zero.

The electrification of the transportation sector by replacing internal combustion engines (ICE) with battery-supported electric motors, will reduce GhG emission. Significant electrification of the world's passengers vehicle fleet is projected to be electrified, with estimates of 35% of new car sale being electric vehicles (EV) by 2030 [7] and 50% of the world's passengers vehicle fleet being electric by 2043 [5]. A total of 14% all new cars sold were electric in 2022, up from less than 5% in 2020 [7]. In fact, the global EV sales are exponential. It took five years from 2012 to 2017 for the EV sales to grow from 100 thousand to 1 million, while the next five years from 2017 to 2022, the EV sales grew from 1 million to 10 million [7]. If the trend continues, global EV sales would reach 100 million by 2027, an optimistic projection, and the growth will more likely stabilize with estimates ranging from 15 to 20 million new EV sales by 2027.

Most of modern power loads require a direct current (DC)-voltage as input source [8]. Electric cars rely on efficient and safe conversion of battery DC-voltage to rotating magnetic fields to provide motor torque, comprising a sophisticated system with power electronics as the enabling technology. Modern railways require similar sophisticated drive trains, although the source energy is typically tapped from the electricity grid through pantographs or generated by diesel generator for heavy rail-electric locomotives, or tapped from low-voltage $(750 - 1500V)$ DC-rails in case of light rail vehicles [9]. The same is true for maritime [10] and aerospace [11]. The alternating current (AC)-source is rectified, and DC converted to AC again through inverters to provide power to the motors. RES and storage technologies require sophisticated electric energy conversion interface in order to efficiently interact and deliver power to the AC-grid. PV solar generates DC-power.

Fast charging of EV requires DC-power. Batteries and fuel cells store DC-power, and wind turbines require in principle similar conversion trains as EVs. AC generated by the turbines are rectified to DC before converted to AC at proper frequency and voltage levels for transmission and distribution. Aluminium smelting – which mainly utilize the Hall-Héroult processes – requires DC-voltage, and generates 1.5 ton CO_2 for each ton of aluminium. The Norwegian aluminium production demanded $\sim 13\%$ of its hydro power electricity production and contributed to $\sim 4\%$ of Norway's total CO_2 emissions in 2020 [12]. The required AC rectification generates substantial energy losses.

Common for all integration of RES and electric transportation is the use of power electronics as a key enabling technology. Power electronic converters (PEC) using semiconductor devices facilitates the required manipulation of source voltage to meet the needs of the load. PEC enable the realization of DC-voltage grids, which simplifies RES integration and bidirectional vehicle-to-grid (V2G-G2V) charging, increasing efficiency and reliability while reducing cost and complexity as the number of AC/DC conversions are reduced or completely eliminated compared to interfacing AC-grids [13]. Furthermore, AC-currents will occupy a lower cross-section area of the conductor than DC-currents due to the skin effect, effectively increasing the resistance and consequently power losses. Vast resources are used to monitor and control the frequency of the AC-grid in order to reduce imbalances between generation and load. The ease of transforming one voltage level to another have historically favored the use of AC over DC in transmission, distribution and domestic power supplies, however, with the invention of the transistor and rapid development of the semiconductor technology, the conversion and handling of DC-power with multiple voltage levels not only became possible, but in most cases more energy and capital efficient.

Silicon-based metal-oxide-semiconductor field-effect transistors (MOSFETs) and insulated-gate bipolar transistors (IGBTs) have been the work horse of the power electronic industry. Silicon (Si) semiconductors have been optimized for several decades and are rapidly reaching their limits in terms of electrical characteristics. Lowering the on-state resistance have been a primary manufacturing goal as it will reduce die and consequently device size for the same power handling, increasing producer yield. However, Si is close to its technological limit, and designing more power, gravimetric, volumetric and efficient power electronic systems is becoming increasingly difficult with Si based transistors. A solution to designing optimal and high-performance power electronics in the future is semiconductors based on wide-bandgap (WBG) materials. Silicon Carbide (SiC) is such a semiconductor material, which to date is the closest competitor to Si IGBTs. SiC has superior semiconductor material properties compared to Si, as illustrated in Figure 1.1.

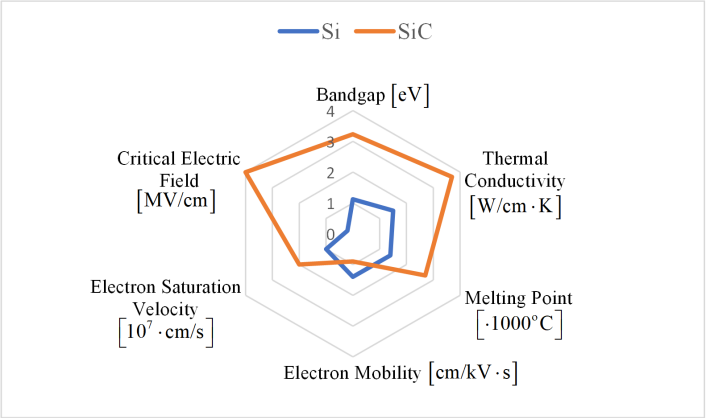

Figure 1.1: Radar chart of Si vs. SiC semiconductor material data.

With higher bandgap, critical electric field strength and thermal conductivity, SiC devices can be manufactured with smaller dies for same power handling capability. Reduction in switching losses in excess of 80% compared to similarly rated Si IGBT devices are obtainable, and paired with an order of magnitude lower specific on-resistance, increased thermal conductivity and melting point, power electronic systems employing SiC devices can achieve massive improvements in power efficiency and power density [14, 15, 16, 17]. The higher obtainable switching frequency permits reduced volume and weight of the passive energy storage components of the converter, increasing power density.

However, engineering challenges are still present in using SiC devices for power electronic applications. For example, both the increase in switching frequency and the increase in device dv/dt and di/dt, shifts the spectral content of the device current and voltage to higher frequencies. This demands improved filtering and shielding to avoid corresponding increases in electromagnetic emission levels due to increased high-frequency energy present in the device switching waveforms. While it is clear that increased switching frequency reduce volume and weight of passive components, the relationship between the required attenuation of an electromagnetic interference (EMI) filter as a function of frequency, its volume and its mass is less clear [16]. Higher di/dt demands stricter design of commutation loops to reduce potential voltage overshoots due to parasitic inductances in the circuit layout. Higher dv/dt increases stresses on insulation system and bearings/shafts of motors [18, 19].

Even though the semiconductor potential of SiC has been known for many years – as Lloyde Wallace at Westinghouse patented a silicon carbide unipolar tran-

sistor device in 1962 [20] – it was not until 2011 that Cree introduced the first commercially available SiC power MOSFET, namely the CMF20120, a n-channel device with a blocking voltage of $1200V$. The field-effect transistor (FET) was patented by Julius Edgar Lilienfeld [21] in 1925. The MOSFET device is considered invented by M. M. (John) Atalla and Dawon Kahng at Bells Labs in 1959 [22, 23], realizing the long anticipated device by Lilienfeld, Heil and Schokley [24, 25, 26, 27, 28]. The Si-based power MOSFET became commercially available in the late 1970 , with the vertical diffused MOSFET (VDMOS) being the first to fulfill the need for a power switch [29]. Thus, the Si power MOSFET has more than 30 years of development over its SiC-based counterparts in terms of yield, cost and reliability. For instance, SiC bulk crystals cannot be grown via traditionally melt-based Czochralski method used for silicon [30]. SiC crystal growth process (e.g. Physical Vapor Transport (PVT)) require significantly higher temperatures ($> 2200°C$) than Si crystal growth ($> 1425°C$) and takes longer time. SiC wafers cost more and have a higher defect density and lower purity, presenting challenges such as near-interface-traps in the gate dielectric, causing degraded reliability [31, 32].

Furthermore, as the SiC power MOSFETs are newer market participants compared to its Si-based counterparts, they face some challenges. The mathematical modelling used in simulation and design stages is less developed. Proper mathematical modelling of key device states, such as drain-source voltage, drain-source current and gate-source voltage, accelerate the design process of power electronic systems by modelling key metrics such as semiconductor power loss, over-voltages and electromagnetic radiated and conducted noise. Different device geometries result in different device characteristics and driving requirements, demanding different gate driving technologies than existing drivers for Si-based MOSFETs and IGBTs. The faster switching speed capabilities of SiC MOSFETs pose challenges with respect to device over-voltages under variable operating conditions, electromagnetic interference and device protection features.

High-performance gate driver circuits capable of controlling device dv/dt, di/dt, device power losses and over-voltages in real-time are limited in their commercial availability. Some adaptive gate drivers – albeit limited in their capabilities – are commercially available, such as UCC5880-Q1, DRV8718-Q1 and DRV8714-Q1, RAA227063. Adaptive gate drivers are thus a research topic with significant potential, and their use can result in significant performance enhancement and flexibility in power electronic systems.

Development of high-voltage SiC MOSFET technology has matured to a degree allowing them to be used and replace its Si-based counterpart in critical infrastructure such as medium-voltage DC (MVDC) grid, data centers, EV charging

stations and drive trains, RES grid integration, solid state transformer and fully electric remotely operated vehicles. Thus, research on high-voltage SiC MOSFETs is crucial for implementing SiC MOSFET efficiently and reliably within the power electronic systems of the future.

Based on the aforementioned challenges imposed in fully exploiting the benefits of SiC MOSFETs, the following research questions have been posed:

- Can high-voltage, high-current SiC MOSFETs be accurately modelled and simulated in real-time without suffering from long simulation times?
- Can high-voltage, high-current SiC MOSFETs be driven such that they can operate optimally under different load, source or environmental conditions?

1.1 Contributions

The aim of this PhD thesis is to develop real-time simulation models of high-voltage and high-current SiC MOSFET half-bridge power modules and their applications, and adaptive gate driver circuits for these devices to tackle the posed challenges. The main contributions of this thesis are summarized as follows

- Dynamic modelling and real-time simulation of SiC MOSFET half-bridge modules switching transients.
- Equivalent device capacitance modelling and their impact on the switching transients of SiC MOSFET half-bridge modules.
- Development and experimental verification of adaptive current source gate drivers for high-voltage, high-current SiC MOSFET devices.
- Development and experimental verification of adaptive voltage source gate drivers for high-voltage, high-current SiC MOSFET devices.

The research of this thesis have been published in the following journal [J#] and conference [C#] papers. Paper [O#] are co-authored papers and paper [R#] is under review.

1.1.1 List of Publications

J1 G. L. Rødal and D. Peftitsis, "An Adaptive Current-Source Gate Driver for High-Voltage SiC mosfets," IEEE Transactions on Power Electronics, vol. 38, no. 2, pp. 1732–1746, Feb. 2023 [33].

J2 G. L. Rødal and D. Peftitsis, "Real-Time FPGA Simulation of High-Voltage Silicon Carbide MOSFETs," IEEE Transactions on Power Electronics, vol. 38, no. 3, pp. 3213–3234, Mar. 2023 [34].

J3 G. L. Rødal, Y. V. Pushpalatha, D. A. Philipps, and D. Peftitsis, "Capacitance Variations and Gate Voltage Hysteresis Effects on the Turn-ON Switching Transients Modeling of High-Voltage SiC MOSFETs," IEEE Transactions on Power Electronics, vol. 38, no. 5, pp. 6128–6142, May 2023 [35].

C1 G. Rødal and D. Peftitsis, "Design Challenges of a SiC-based MVDC Power Supply for Deep-Sea applications," in 2019 10th International Conference on Power Electronics and ECCE Asia (ICPE 2019 - ECCE Asia), May 2019, pp. 2368–2375, iSSN: 2150-6086 [36].

C2 G. L. Rodal and D. Peftitsis, "An Adaptive Current Source Gate Driver for SiC MOSFETs with Double Gate Current Injection," in PCIM Europe digital days 2021; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management, May 2021, pp. 1–7 [37].

C3 G. L. Rødal, Y. V. Pushpalatha, and D. Peftitsis, "Design Evaluation of Medium-Voltage and High-Power Modularized DC/DC Converters with SiC MOSFETs," in 2021 23rd European Conference on Power Electronics and Applications (EPE'21 ECCE Europe), Sep. 2021, pp. P.1–P.11 [38].

C4 G. L. Rødal and D. Peftitsis, "Real-time FPGA Simulation of Dual Active Bridge Converter with SiC MOSFET Device Model," in 2022 International Power Electronics Conference (IPEC-Himeji 2022- ECCE Asia), May 2022, pp. 2613–2620 [39].

O1 T. N. Ubostad, A. Giannakis, G. L. Rodal, D. A. Phillips, and D. Peftitsis, "Reduction of Parasitic Inductance and Thermal Management in a Multichip SiC Half-Bridge Module," in PCIM Europe digital days 2021; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management, May 2021, pp. 1–7 [40].

O2 H. B. Ekren, D. A. Philipps, G. Lyng Rødal, and D. Peftitsis, "Four Level Voltage Active Gate Driver for Loss and Slope Control in SiC MOSFETs,"

in 2022 IEEE 13th International Symposium on Power Electronics for Distributed Generation Systems (PEDG), Jun. 2022, pp. 1–6, iSSN: 2329-5767 [41].

R1 G. L. Rødal and D. Peftitsis, "Gate-Drive Circuits for Adaptive Operation of High-voltage SiC MOSFETs".

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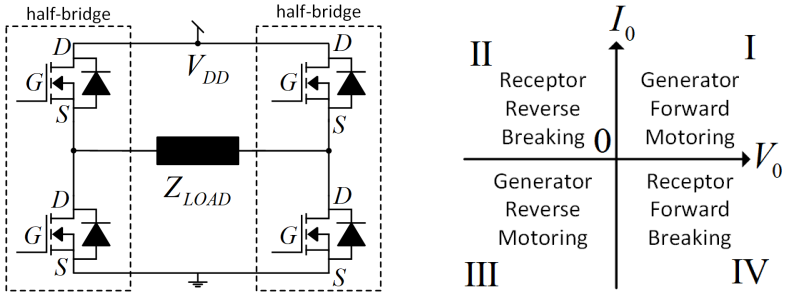
Chapter 2

Background

Power electronics are electric circuits whose main task is to process electric energy to meet specified requirements. Power electronics is a combination of low-power signal-level information-processing circuitry with high-power energy-processing circuitry which employs semiconductor devices [1]. The power electronic circuit typically have two or more ports, where the energy form at one port is manipulated to meet the requirements at another port. Typically, the electric source energy is processed in a way to optimally suit a given load. The transistor is the governing entity of the power electronic system. With the seemingly simple act of turning it on and off, it is able to synthesise complex system voltages and currents waveforms with high precision through pulse-width modulation (PWM). The two most commonly used transistor technologies in modern power electronic systems are the metal–oxide–semiconductor field-effect transistor (MOSFET) and insulated-gate bipolar transistor (IGBT). Although the two transistor types both behave as three-terminal electrical switches, the MOSFET is an unipolar (current flow through single-polarity p or n charge carrier) device while the IGBT is a bipolar device (current flow through both p and n polarity charge carriers). They differ in their physical structure (i.e. semiconductor layering, doping, geometry etc.), resulting in different electrical characteristics. IGBTs typically have a higher power handling capability than MOSFETs, while MOSFETs can operate at higher switching frequencies.

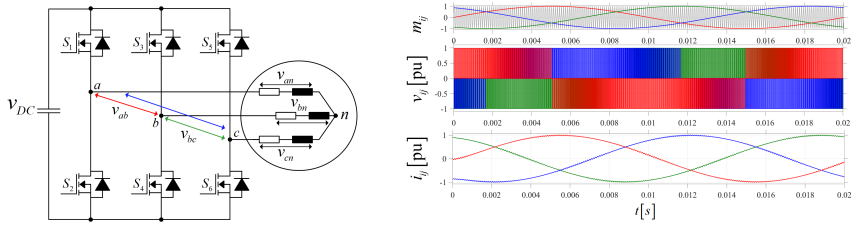
Examples of typical power electronic systems employing MOSFETs and IGBTs are electrical drives, telecommunication and data center power supplies, renewable energy grid interfaces, electrical vehicle drive trains or electrified marine vessels. The most utilized power electronic switch configuration for high power, high efficiency power electronic system is the half-bridge circuit, that is, a combination



(a) Full-bridge topology.

(b) Current (torque) / voltage (speed) quadrant.

Figure 2.1: Full-bridge.



(a) Three-phase inverter topology utilizing three half-bridge circuits.

(b) Generated waveforms by manipulation of the semiconductor switches $S_1 - S_6$.

Figure 2.2: Three-phase inverter.

of two power transistors connected drain-to-source, as illustrated in Figure 2.1(a). The full-bridge (H-bridge) – comprised of two half-bridges connected drain-to-drain and source-to-source – can deliver positive and negative voltage/current to a load. In the case of a DC-motor, the full-bridge motor controller can provide forward speed and positive torque (quadrant I), reverse speed and positive torque (quadrant II), reverse speed and negative torque (quadrant III) and positive speed and negative torque (quadrant IV). Most modern power electronic system utilize some combination of the half-bridge, from the high-power topologies such as the dual-active bridge (DAB) [2], phase-shifted full-bridge and three-phase inverter (Figure 2.2(a)), to the lower power synchronous buck/boost, half-bridge LLC and totem-pole voltage source gate drivers where the half-bridge is used. For example, considering an electrical drive with a DC-voltage battery energy source. The use of an AC-motor require a rotating magnetic field to produce torque, which again requires alternating currents. Thus, the DC-currents supplied by the source must be manipulated in order to produce AC-currents, a process enabled by power electronics. A set of three 120° phase-shifted currents are required to run through the

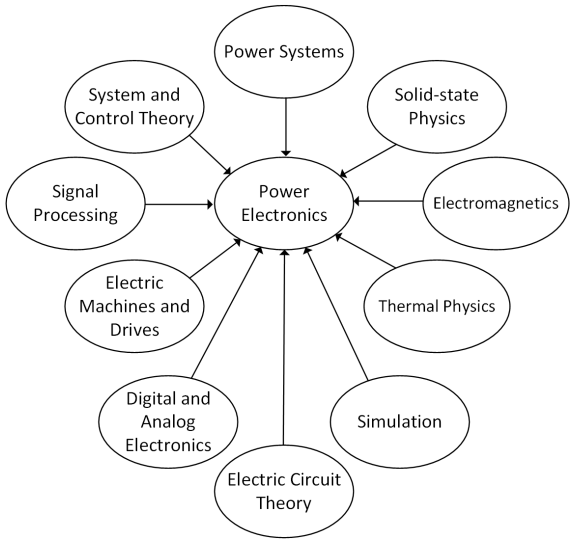


Figure 2.3: The interdisciplinary nature of power electronics.

stator in order to rotate the rotor of a synchronous motor. A common way of manipulating the DC-current provided by the source into three-phase AC-currents is by the use of three-phase inverter topologies and pulse-width modulation control strategies of the switches, as illustrated in Figure 2.2

Power electronics are highly interdisciplinary in nature and involve many fields of engineering, as visualized in Figure 2.3. Power electronics are increasingly integrated into the electricity grid through e.g. interfacing electric vehicle charging [3] or energy generation [4] such as solar and wind, hence power system and control theory is integral to a functioning power electronic system. Optimal design of passive components, such as DC-link capacitors and filter inductors, require understanding of electromagnetics and their design are enabled by finite element method (FEM) simulations. The generation of proper electromagnetic fields generating torque in electric machines enabled by power electronics require understanding of the construction and working principles of electrical machines. Thermal physics and control theory are integral in proper functioning electrical drives. Optimal control of power electronics require measuring of voltages and current – as well as environmental data acquisition such as ambient temperatures – facilitated by signal processing, digital and analog electronic circuitry. Electric simulation and circuit theory are disciplines necessary for arriving at the best performing power electronics topology for a given application. The next generation and future of power electronics are enabled by the study and the discernment of solid-state, quantum and thermal physics.

Power electronics are increasingly used in industrial, defense, aerospace, automotive and commercial applications, driven by the development and introduction of wide-bandgap (WBG) semiconductor materials. WBG semiconductors, i.e. devices comprising semiconductors materials with higher bandgap energy E_g than conventional silicon, allows the WBG semiconductor devices to withstand higher critical electric field strength E_{cr} than silicon. Semiconductors are solid materials of which their conductivity can be controlled over a wide temperature range by introducing impurities into the intrinsic semiconductor material by the process of doping [5]. By interfacing to semiconductor materials – one doped with an electron donor material (n-type), and the other doped with an electron acceptor element (p-type) – allows for the creation of the pn-junction. This junction is rectifying, conducting current in only one direction when it becomes forward bias, while blocking current in the other direction (reverse bias), and is the governing building block in all semiconductor power devices. The E_g is the minimum electron energy required to break an electron out of the semiconductor material's valence band into its conduction band required for current to flow. The electric field which a semiconductor can withstand is limited by impact ionization which leads to avalanche breakdown, and determines the breakdown voltage of the device. Impact ionization occurs if the electric field is high enough such that a significant amount of charge carriers (electron/holes) gain sufficient kinetic energy so that they can be lifted from the valance band to conduction band. These charge carriers have sufficient kinetic energy to knock bound carriers into conduction from their bound valence state, generating electron-hole pairs in the process through impact ionization. This effect multiplies like an avalanche, and if this occurs in a region of the semiconductor with high enough electric field, an avalanche breakdown may occur. Hence, using a semiconductor material with higher bandgap energy requires a higher electric field strength to reach breakdown. The breakdown voltage is related to the width of the reverse-biased space-charge (depletion) region, spreading out from the pn-junction increasing in width with applied electric field, leaving only ionized donors and acceptors impurities. The breakdown voltage V_{BB} is

$$V_{BB} = \int_0^w E \, dx = \frac{1}{2} E_{cr} w \tag{2.1}$$

Assuming a constant critical electric field E_{cr}, the V_{BB} is related to the width w of the space-charge region according to Equation 2.1. A high bandgap is advantageous because the critical field strength increases with the bandgap energy, hence reducing the required space-charge width – and consequently material use – to handle a given V_{BB}. For example, to isolate $10kV$, $\sim 1000\mu m$ of Si material is needed, $\sim 100\mu m$ needed for 4H-SiC and only $\sim 20\mu m$ needed with diamond.

However, unnecessary large energy gaps can prove disadvantageous because the ionization energy of the impurities becomes larger with increasing bandgap and hence they release an unfavorably low number of carriers at room temperature, increasing semiconductor resistance. Furthermore, the built-in threshold voltage increase with increasing band-gap [5].

Other material properties are advantageous in high power electronics – such as thermal conductivity – allowing the WBG materials to transport more energy over a temperature gradient – allowing higher semiconductor power dissipation, consequently enabling higher switching frequencies than Si devices. Higher saturation drift velocity reduce the semiconductor on-state resistance, reducing conduction loss. This allows for manufacturing devices with lower cross-section area for same current rating, effectively reducing the equivalent device capacitances, hence enabling higher device dv/dt and di/dt and consequently increased switching frequency. These traits attracts WBG power electronics particularly to high temperature operation and applications with high volumetric and/or gravimetric power density restrictions. With the size of passive components of the power electronic system being inversely proportional to switching frequency, a higher switching frequency increase system power density. The higher blocking voltage per rated ampere enabled by WBG devices generally increase system efficiency, as the same power can be handled with increased system voltages, reducing ohmic I^2R-losses. For example, solid state transformers (SST) are being increasingly used as an alternative to classical grid-frequency transformers due to their increased power density, inherent controllability, active and reactive power flow control, bi-directional power flow, voltage sag and fault current handling capabilities and harmonic control [6, 7]. The transformer area product is inversely proportional to the operating frequency of the transformer voltage, and the transformer core volume and consequently final volume V_f is proportional to the area product A_p as $V_f \propto A_p^{3/4}$ [8], where A_p is the product of the transformer core and window cross section area. On the other hand, higher switching frequencies increase average semiconductor power losses in hard-switched applications, increase conductor resistance through skin effect, increase magnetic core hysteresis and eddy current power loss, consequently posing system thermal management challenges.

The two most commonly used WBG materials in modern power electronics is Silicon Carbide (SiC) and Gallium Nitride (GaN), and are typically used in transistor based switches. Commercially, SiC is mostly used in MOSFET devices and to some degree JFET (Junction Field Effect Transistor) in the $1.2 - 1.7kV$ range. GaN-based transistors are typically termed GaN FETs or GaN HEMT (high electron mobility transistor), and are commercially available as lateral GaN-on-substrate (substrate commonly being Si or SiC) devices. The lower intrinsic

carrier concentration of SiC and GaN resulting in reduced intrinsic leakage current compared to Si [9], and paired with better thermal conductivity makes them suitable for high temperature operation.

In terms of the semiconductor device material composition, Baliga's figure of merit (BFOM) [10] –

$$R_{on(sp)} = \frac{4V_{BB}^2}{\epsilon_s \mu_n E_{cr}^3} \tag{2.2}$$

– where $R_{on(sp)}$ is the specific drift region resistance, V_{BB} is the breakdown voltage, ϵ_s is the semiconductor permittivity, μ_n is the drift region electron mobility and E_{cr} is the critical field at breakdown – can act as an indication of the performance of the semiconductor material used. The specific on-resistance of the device is typically compared with the *unipolar limit* given by BFOM for the material of interest to gauge the technology's maturity. Table 2.1 shows important material physical properties of Si, SiC and GaN governing their electrical and thermal characteristics. The 4H polytype of SiC is the most widely used due to its high electron mobility, high electric field strength, as well as the availability of single crystal wafer of high quality [11]. Furthermore, only n-type SiC MOSFET are considered as p-type SiC MOSFET have higher on-resistance due to lower hole mobility and incomplete ionization of acceptors at room temperature. With the higher bandgap and critical electrical field of SiC compared to Si, the specific on-resistance $R_{sp(on)}$ of Si-based device ranges 1000-times higher than for SiC-based devices [10]. There is significant reduction of the specific resistance of the drift regions between Si and 4H-SiC devices. The $R_{sp(on)}$-ratio of Si to 4H-SiC devices increase from $\sim$ 500 at $V_{BB} = 100V$ to $\sim$ 1300 at $V_{BB} = 44kV$, signalling SiC benefits for increasing blocking voltages [12]. Reducing die size increase the number of MOSFET structures which can be produced per wafer, increasing production yield. The lower $R_{sp(on)}$ allows for a smaller chip size for a given rated current, reducing equivalent device capacitances which enables faster switching speeds and lower switching losses. The lower intrinsic carrier concentration of SiC compared to Si results in lower leakage current, and paired with the superior thermal conductivity of SiC compared to Si, SiC enables more robust high temperature operation [13, 14, 15]. Both E_{cr} and μ_n are heavily dependent on the donor doping density N_D. Other effects, such as incomplete ionization of dopants at room temperature impacts $R_{on(sp)}$ [11]. Si MOSFETs have been optimized for $\sim$ 60 years and are close to their unipolar limit, while SiC MOSFET still have ways to go [16]. This is illustrated in Figure 2.4, where the $R_{on(sp)}$ is plotted against their rated blocking voltage V_{BB}. Blue (second generation) and red (third generation) shows $R_{on(sp)}$ for commercial planar SiC MOSFETs, while green shows

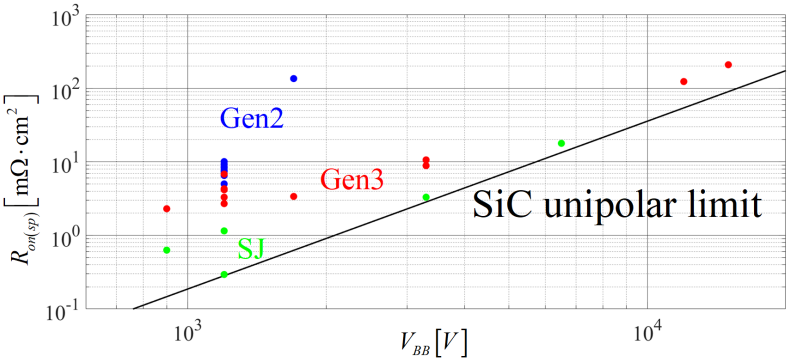


Figure 2.4: Specific on resistance $R_{on(sp)}$ of SiC MOSFETs.

Table 2.1: Semiconductor Material Properties

Property	Si	4H-SiC[1]	GaN
Bandgap [eV]	1.12	3.26	3.44
Relative Permittivity	11.7	9.7	8.9
Critical Electric Field [MV/cm]	0.2	2.5	3.3
Electron Mobility $[\mathrm{cm^2/\,kV\cdot s}]$	1.4	0.9	1
Thermal Conductivity $[\mathrm{W/\,cm\cdot K}]$	1.5	3.7	1.3
Electron Saturation Velocity $[10^7\cdot \mathrm{cm/s}]$	1	2	2.4

[1] $N_D \sim 10^{16}$ cm^{-3}, room temperature

$R_{on(sp)}$ for superjunction (SJ) SiC MOSFETs from literature [17, 18, 19, 20, 21]. The SJ MOSFET structure achieves a better trade-off between $R_{on(sp)}$ and V_{BB} by introducing a transverse electric field into the drift layer by p-pillars, allowing for a smaller device [22]. Significant challenges still exist in wafer fabrication of SiC SJ MOSFETs. The latest generation SiC MOSFET – 4th generation SiC MOSFET –is currently only offered by ROHM.

Normally-off GaN devices are commercially available either as cascode (normally-on depletion mode GaN HEMT cascoded with LV Si MOSFET) devices up to $V_{BB} = 900V$ blocking voltage, enhancement mode (e-mode) GaN HEMTs up to $V_{BB} = 650V$ or more complex combinations of these two up to $V_{BB} = 900V$. They are currently limited in their V_{BB} due to their lateral device structure. The

lateral structure means current flow through drain and source laterally in a 2D electron gas on the AlGaN/GaN interface. High current density in the channel is sensitive to surface traps, leading to issues like current collapse and increased dynamic $r_{DS(on)}$, being more severe with increasing V_{BB} [23]. Charge trapping can cause unstable threshold voltage, increase in gate leakage current, gate- and drain-lag, current collapse and kink effects [24]. Furthermore, the lateral structure leads to inhomogeneous electric field distribution, which may cause premature breakdown or enhanced electron trapping. Increasing the V_{BB} rating means increasing the distance between drain and source laterally. To reduce $r_{DS(on)}$, the surface area must increase, increasing device capacitances as well as cost. Vertical GaN devices grown on native GaN substrate would mitigate the lateral issues. However, there are big challenges for vertical GaN such as the quality of native GaN substrates, GaN doping challenges and ability to form high quality interface with gate dielectrics [23]. Thus, most of GaN power devices are realized with hybrid substrate materials, either GaN-on-Si or GaN-on-SiC (GaN-on-substrate). This leads to challenges such as differences in thermal expansion coefficients and lattice mismatch. Furthermore, the inherent absence of pn-junction of GaN-on-substrate – which allows for avalanche breakdown and short-term protects Si and SiC against overvoltages – subjects the device to overvoltage destruction [25]. However, vertical GaN structures – fully utilizing high electron mobility and critical electric field strength – are heavily researched. NexGen Power System is shipping engineering samples of $V_{BB} = 1200V$ Gan-on-Gan vertical Fin-JFETs (fin-channel junction field-effect transistors), achieving $R_{sp,on} = 0.82\text{m}\Omega \cdot \text{cm}^2$ and robust avalanche capability [26].

The vast majority of SiC MOSFETs are vertically structured as illustrated in Figure 2.5, with their blocking voltages dependent on the thickness of the drift layer. A vertical transistor structure utilize 3 dimensions, rather than the 2 dimensional expansion available for a lateral devices, increasing material yield while avoiding the aforementioned challenges. By increasing the thickness of the drift layer vertically, their V_{BB} can be increased without increasing surface area. The current handling can be increased by increasing the surface area without increasing chip thickness. Hence, SiC MOSFETs are becoming the most attractive WBG semiconductor technology to replace Si based IGBTs commonly deployed in high-voltage high-current power electronics systems. 4H-SiC holds material properties which are highly suitable for power electronic applications, with some key properties summarized in Table 2.1.

The unipolar conduction of SiC MOSFET removes the tail current seen in IGBTs due to bipolar conduction and minority carrier recombination, further reducing turn-off switching losses. High-current, high-voltage SiC MOSFETs (i.e. SiC

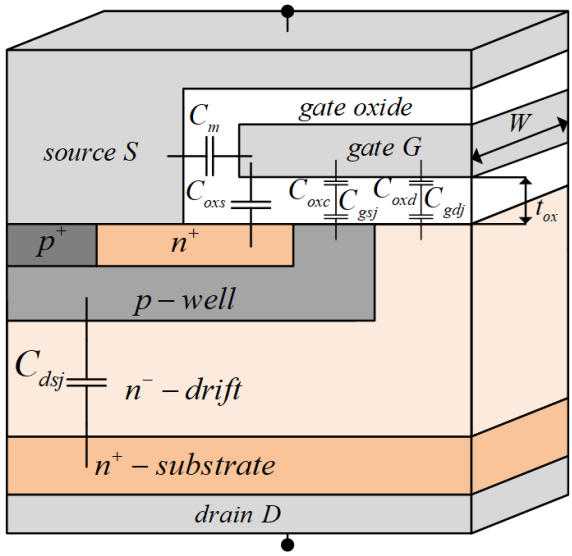


Figure 2.5: Vertical SiC MOSFET cross section.

power MOSFETs) are commercially available for blocking voltages up to $3.3kV$, and are becoming a big competitor to the well established Si IGBT in applications such as medium-voltage (MV) drives [27, 28, 29] and medium- and high-voltage (HV) direct-current (DC) grids [30, 31, 32, 33, 34, 35]. The replacement of Si IGBTs with SiC MOSFETs have resulted in significant inverter weight reduction in the electric vehicle industry. With the release of Model 3 in 2018, Tesla became the first EV company to employ SiC MOSFETs in an in-house inverter design [36]. This led to an inverter weight (4.8kg) of under half of what was achieved by the 2019 Nissan Leaf (11.15kg) and below 60% of the inverter weight of Jaguar I-Pace (8.23kg), both using Si IGBT inverters. Other companies have followed suit, with McLaren's and BorgWarner's $800V$ SiC inverters [37, 38], and Porche doubling their system voltage from $400V$ to $800V$ using SiC based power modules, reducing the weight of Porche's Teycan with 30kg [39, 40]. The transformation of EV charging infrastructure from $400V$ to $800V$, enabling faster charging and reduced weight, is largely driven by the use of SiC power MOSFETs. As of 2022, large-volume EVs including BYD's Han and and Hyundai's Ioniq 5 are employing SiC, and key SiC device players – including STMicroelectronics, Infineon, Wolfspeed, onsemi and ROHM, delivered record revenue in 2021 and is projected to move towards 1 billion USD revenue by 2025 [41]. Infineon projects that SiC will be the

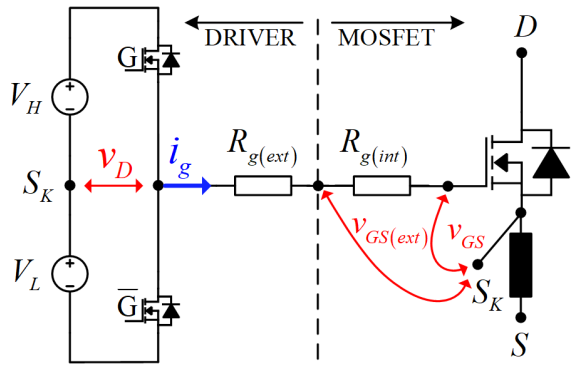


Figure 2.6: The conventional totem-pole voltage source gate driver.

dominating semiconductor technology in x[1]EV's drivetrain with 55% dominance over Si and GaN, covering a 6 billion € market with an estimated 70 million xEV produced by 2030 [42].

As stated in chapter 1, by turning the SiC MOSFET on and off, the system's voltages and currents can be controlled with precision. MOSFETs – and especially power SiC MOSFETs – require specific circuitry to turn them on and off. Circuits whose purpose are to turn transistors on and off are termed gate drivers. As the name suggests, for MOSFETs, their task is to drive charge into and from the device's gate. This act controls the electric field on the gate, which allows current to flow – or stop current from flowing – between the MOSFET's drain and source terminals which connect the device to the larger power electronic circuit. Consequently, the gate driver is a crucial component of the power electronics system, responsible for safe and optimal system operation and switching of the MOSFET.

The totem-pole voltage source gate driver – illustrated in its basic form in Figure 2.6 – is the predominantly used gate driver for SiC MOSFETs. The driver circuit is connected to the MOSFET's gate G and source connection S_K (in this case S_K, where the K refers to *Kelvin*-source, a source connection separate from the device power source S dedicated to gate control and implemented in specific devices to reduce parasitic gate drive loop inductance) of the device. The driver controls the conductivity of the MOSFET's channel between the device drain D and source S by adjusting the voltage v_{GS} between G and S. It benefits from robust and effective operation with proven functionality over many decades. However, with fixed on-state (V_H) and off-state (V_L) driving voltages, the only design parameter of the driver to control the switching transients of the MOSFET is

[1]Battery electric vehicle (BEV), plug-in hybrid electric vehicle (PHEV), full hybrid electric vehicle (FHEV), fuel cell electric vehicle (FCEV), mild hybrid electric vehicle (MHEV).

$R_g = R_{g(ext)} + R_{g(int)}$, with $R_{g(ext)}$ being the only adjustable part as $R_{g(int)}$ is typically integrated into the device package. This limits power electronic system designers with respect to switching losses, turn-on/off delay and total switching time, device dv/dt and di/dt, and locks the design at a specific device behaviour which is only optimal for certain load, source and environmental operation conditions.

The potential for lower conduction losses and faster switching speed makes SiC power MOSFETs obvious candidates in future high-performance power electronic systems. This PhD thesis addresses some of the current challenges imposed by SiC MOSFETs with respect to mathematical modelling, real-time simulation and adaptive gate driving. The modelling is a benefit in designing the power electronic system were SiC MOSFET is employed. Accurate modelling allows for system simulation, enabling critical system parameters such as switching and conduction loss, di/dt, dv/dt and EMI, heat flow and thermal challenges to be assessed even before the prototyping phase. Adaptive gate driving allows for fully exploiting SiC MOSFETs capabilities. By tailoring device switching loss, conduction loss, dv/dt, di/dt turn-on/off delay and total switching times, the power electronic system can be made capable of adapting its operation depending on source, load or environmental conditions for optimal performance.

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Chapter 3

Real-time SiC MOSFET Modelling

This chapter gives an overview of modelling aspects of a SiC MOSFET half-bridge module drain-source voltage v_{DS}, source current i_S and gate-source voltage v_{GS}. In particular, the MOSFET's intrinsic voltage dependent capacitances and the concept of real-time simulation are presented. Dynamic modelling and real-time simulation of a $3.3kV$ half-bridge SiC MOSFET power module with extension to the dynamics of the dual-active bridge converter are presented [J2], [C4]. In [J3], a more in-depth analysis of the device capacitances and v_{GS}-hysteresis effects on the turn-on transient are investigated, and experimental validation of the real-time capable simulation model is extended to a $1.2kV$ half-bridge SiC MOSFET power module. The dynamic model allows for accurate estimation of SiC MOSFET switching losses and electrical characteristics such as device dv/dt, di/dt, turn-on and -off times and delay times.

3.1 Introduction

An accurate mathematical model of the evolution of the SiC MOSFET key device states, such as the gate-source voltage v_{GS}, drain-source voltage v_{DS} and source-current i_S[1], is beneficial for power electronics converter design. A mathematical device model allows for estimation of turn-on and -off delay times, total turn-on and -off times, and switching energies, as well as device dv/dt and di/dt. Such models are critical for assessing their switching behaviour in designing ef-

[1] In [J2], [J3] the term drain-current i_D is used, while its actually the source current which is measured and derived in the dynamic equations. The term drain-current i_D is used some places, however, the term source-current i_S is the correct term.

ficient and reliable modern power electronic system, rapid converter prototyping and evaluation of converter designs.

Real-time capable simulation models of the energy-processing components of a power electronic system are beneficial in development processes. Controllers can be tested on the system independently from the hardware development by using a real-time model of the targeted hardware. This enables controller development and verification even before the hardware is finalized. This can minimize risk of potentially costly failures by discovering and mitigating them earlier in the project process. Testing of control systems have traditionally been carried out directly on the hardware to be controlled (the plant), e.g. on a prototype in the lab or on deployed hardware in the field. Even though this obviously is the most accurate method of testing the controller, it can be expensive and potentially unsafe, as the behaviour of the controller on the plant is unknown. Bringing the physics of the plant into a real-time digital environment with proper controller input/output interfaces – i.e. putting the hardware-in-the-loop (HIL) – allows an alternative testing platform of the plant dynamics integrated with the controller. Thus, a HIL simulation can reproduce plant dynamics in real-time allowing for closed-loop controller testing and verification. As presented in [J2], a real-time capable simulation model of a DAB with SiC MOSFET dynamics is implemented on a platform which is capable of hosting the final system's controller, sensing and signal processing, allowing for a smooth flow from controller prototyping to real usage. The modelled states are outputted through an on-board digital-to-analog converter (DAC). As the model is running in real-time – meaning 1 simulation second corresponds to 1 wall clock second – the total simulation time is drastically reduced compared to non-real-time simulation tools (i.e. LTSPICE or PLECS). This is particularly useful for large, complex systems with large time constant dynamics, e.g. thermal dynamics, and numerous states, e.g. multi-phase converters or modular multi-level converters (MMC).

3.2 SiC MOSFET Modelling

The key device states v_{GS}, v_{DS} and i_S evolution in time is mathematically modelled in [J2], [J3], [C4]. The work in [J2], [C4] models both turn-on and turn-off switching transitions and shows the real-time capable models applied in the dual-active bridge power electronic converter application. The work in [J3] focuses on the the turn-on switching transient and how different physical semiconductor effects impacts the switching transient. Common for all models is the use of the Shichman and Hodges equations with voltage-dependent non-linear device capacitances and electrical module parameters to obtain electrical state time evolution.

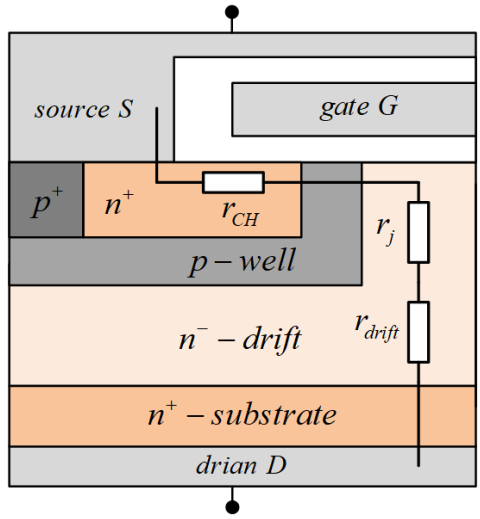


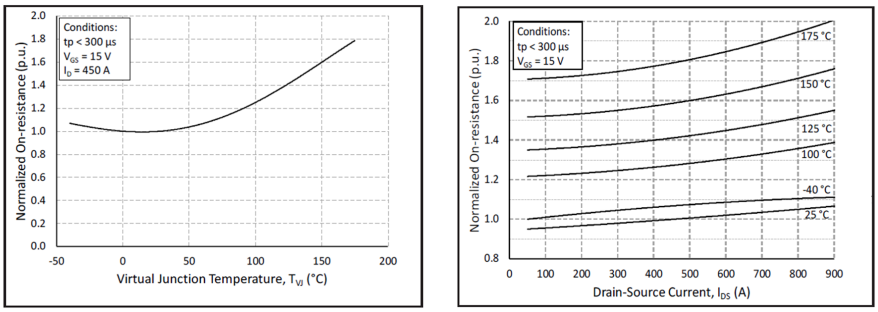
Figure 3.1: MOSFET cross section with $r_{DS(on)}$ components.

3.2.1 Power Losses

Despite the advances in WBG power transistors, the device's conduction and switching losses are still a major contributor to total system power losses. The instantaneous conduction loss is governed by the device drain-source on-state resistance $r_{DS(on)}$ and the source-current (which in on-state is equal to the device channel current i_{CH}) as

$$p_{cond} = r_{DS(on)} \cdot i_S^2 \tag{3.1}$$

As the SiC MOSFET has a layered device structure, the total resistance between its drain and source terminals $r_{DS(on)}$ can be modelled by the series connection of several discrete resistors. As illustrated in Figure 3.1, $r_{DS(on)}$ is typically comprised of the drain and source contact resistances (negligible), channel r_{CH}, JFET r_J, drift r_{drift} and substrate (negligible) resistances [1, 2, 3]. The r_{CH} is dominant at room temperature. For low enough temperatures – well below 0°C – some of the free carriers in the SiC bulk (i.e. $r_{bulk} = r_J + r_{drift}$) can "freeze out". This can cause a reduction in the doping concentration and an increase in r_{bulk}, making r_{bulk} dominating over r_{CH} for temperatures below -140°C [1]. The r_{CH} is dominant and typically reducing for temperatures up to 100°C . Above this temperature, the channel resistance r_{CH} is dominant. For even increasing temperatures, the mobility in the drift region decrease, and mechanisms such as Coulomb and phonon scattering becomes dominant over thermal emissions of electrons from interface



(a) Normalized $r_{DS(on)}$ as a function of virtual junction temperature.

(b) Normalized $r_{DS(on)}$ as a function of drain current.

Figure 3.2: Datasheet values of normalized $r_{DS(on)}$ for different operating conditions CAB450M12XM3 SiC MOSFET half-bridge module [4].

traps [1, 3], causing the increasing r_{bulk} to become the dominant part of $r_{DS(on)}$.

The $r_{DS(on)}$ is dependent on the temperature T_j in the conducting channel (usually termed junction temperature), the value of v_{GS} and the the value of i_S. The $r_{DS(on)}$ as a function of these parameters are usually accurately and extensively described in the device manufacturer datasheet for several operating conditions, as seen in Figure 3.2. These values can be used for developing a model for the on-state drain-source voltage drop $v_{DS(on)}$. Hence, for a given i_S determined by the system operating condition, the system's semiconductor conduction loss can be accurately determined. The $r_{DS(on)}$ values can be stored in lookup tables (LUT), and by inputting i_S, T_j and v_{GS}, p_{cond} can be estimated in real-time. Its average value can also be accurately estimated for a given operating condition, e.g. at a worst-case T_j as

$$P_{cond} = r_{DS(on)}\left(v_{GS}, T_j, I_S^{RMS}\right) \cdot \left(I_S^{RMS}\right)^2 \tag{3.2}$$

Switching losses are more complex to estimate than conduction losses. Estimation of switching losses require a mathematical description of the evolution of v_{GS}, v_{DS} and i_S. The main loss mechanisms of the SiC power MOSFET during the switching transient is the v_{DS}-i_{CH} overlap and the power losses of the internal gate resistance $R_{G(int)}$, with the v_{DS}-i_{CH} loss generally being the largest loss contributor for high-voltage, high-current SiC MOSFETs (i.e. SiC power MOSFETs) operating at nominal conditions. Power losses will also occur in other parts of the power circuit, i.e. the gate-driver circuit and its external gate resistance $R_{G(ext)}$ as well as in ohmic contacts of the power device. The v_{DS}-i_{CH} loss is dependent on the system operating point, as input/output, source/load voltage/current typic-

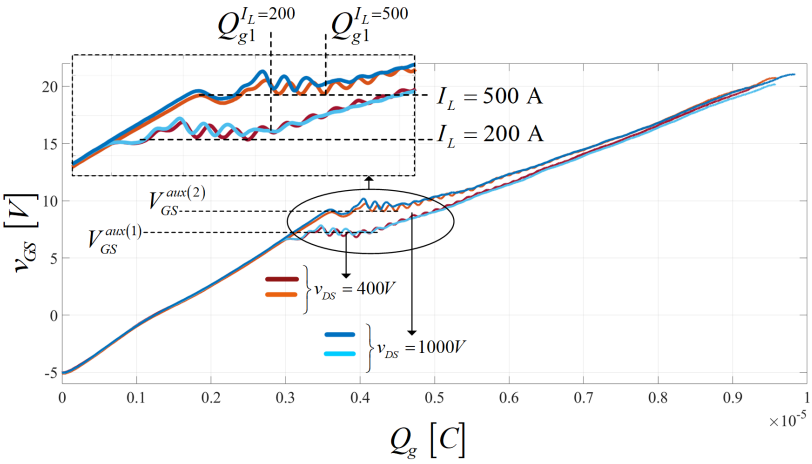
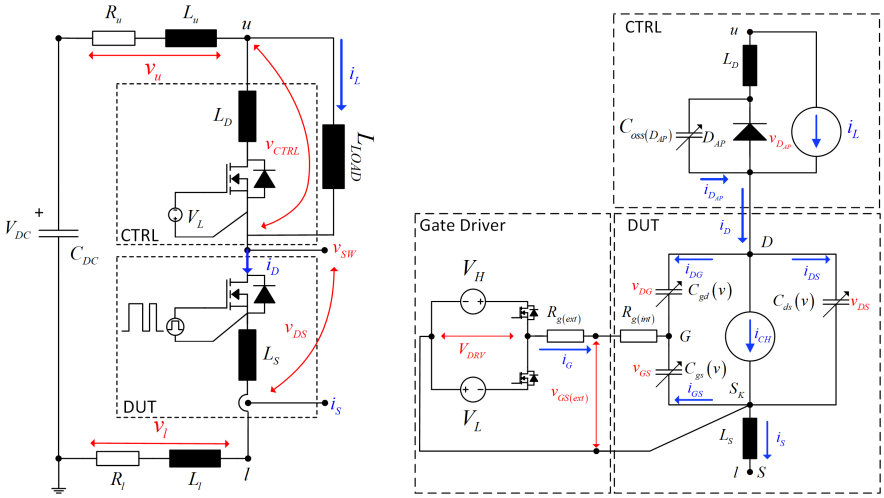


Figure 3.3: Gate-source voltage v_{GS} vs. gate charge Q_g obtained from experimental double-pulse testing of the FMF750DC-66A SiC MOSFET half-bridge module.

ally dictates the level of v_{DS} and i_{CH} during switching, with significant variations depending on the topology used.

The gate driver [2] operation also depends on the system operating point where the driven device is employed. The total device's gate charge Q_g – that is the amount of charge moving between the gate-source high V_H and low V_L potential levels during switching transients – required, depends on both the blocking voltage level V_{DS} prior to turn-on and after turn-off, and the fully-on source current I_S after turn-on and prior to turn-off. This is depicted in Figure 3.3, where v_{GS} is plotted against gate charge Q_g for different switching load currents I_L and blocking voltages V_{DS}. Considering the turn-on process, the device is considered turned on when the output capacitance $C_{oss} = C_{gd} + C_{ds}$ is discharged. That is, when Q_{g_1} has been moved from the driver to the gate at the given device operating point. As seen in Figure 3.3, the charge value Q_{g_1} depends on the load-current I_L, which in this instance is the value of the device switching current after turn-on and prior to turn-off. This flattening of the v_{GS}-Q_g characteristics is termed the Miller region, which flattens as the displacement current caused by $C_{gd}(dv_{DG}/dt)$ causes v_{GS} to stall. Obtaining information – e.g. at which v_{GS} level or time duration after the driver voltage V_{DRV} switch state – of the Miller region for a particular device is useful when employing adaptive gate drivers. As discussed in [J1], sinking or sourcing current during the Miller plateau allows for controlling device v_{DS} slew rate.

[2] Conventional voltage source totem-pole based gate drivers. See chapter 4.



(a) Double pulse test (DPT) schematic.

(b) Detailed schematic of gate driver, DUT and CTRL switch.

Figure 3.4: Equivalent circuit schematics used with the dynamic switching model.

The gate driver, as illustrated in Figure 3.4(b), will mainly loose power to the surroundings through Joule heating in the total gate-drive resistance. The gate driver instantaneous losses (neglecting driving and quiescent losses of driver IC's and accompanying power supplies) are given by

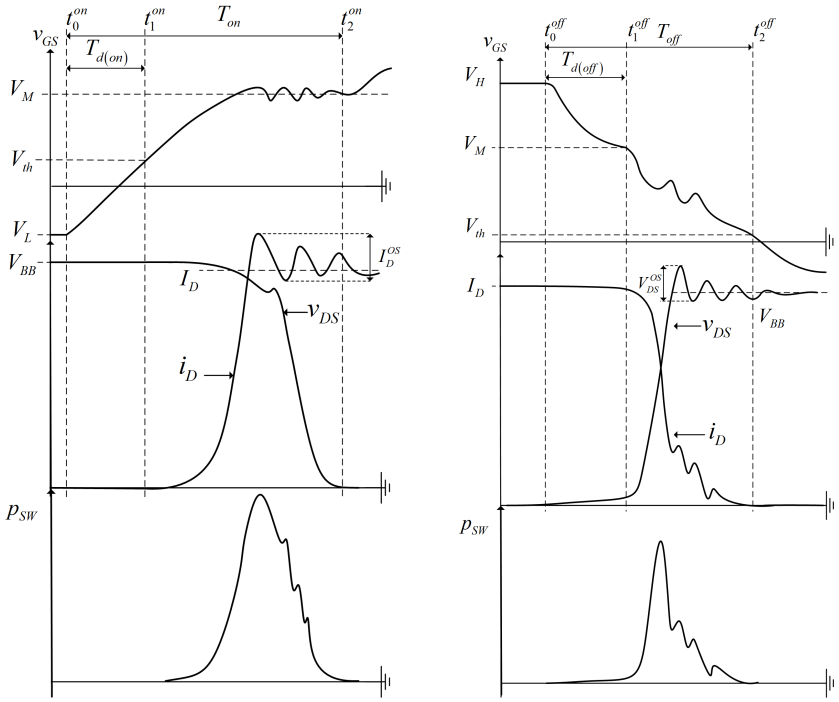
$$p_D = R_g i_g^2 \tag{3.3}$$

where R_g is the total gate resistance and i_g the gate current. Per switching instant, the gate driver's voltages push charge onto the gate to charge the device input capacitance C_{iss}, from V_L to V_H during turn-on and from V_H to V_L during turn-off. For a conventional voltage source gate driver (CVSGD), the gate current i_g is given by

$$i_g = \frac{(V_{HL} - v_{GS})}{R_g} = \frac{V_{HL}}{R_g} e^{-t/\tau_{iss}} \tag{3.4}$$

where $R_g = R_{g(ext)} + R_{g(int)}$, $V_{HL} = V_H + V_L$, $C_{iss} = C_{gs} + C_{gd}$ and $\tau_{iss} = C_{iss} R_g$. This demands the energy

$$E_D = \int_0^{T_{g(f)(on/off)}} p_D \, dt = \frac{C_{iss} V_{HL}^2}{2} = \frac{Q_g V_{HL}}{2} \tag{3.5}$$



(a) Turn-on. **(b)** Turn-off.

Figure 3.5: Theoretical switching waveforms

per switching instant, where $T_{g(f)(on/off)}$ is the time duration for C_{iss} to be fully charged (i.e. when the charge $Q_{g(f)}$ (Figure 3.3) has been moved) This would yield the average power loss

$$P_D = 2f_{sw}E_D = f_{sw}Q_gV_{HL} \tag{3.6}$$

during continuous switching operation, i.e. the driver loss incurred at both turn-on and turn-off. The $v \cdot i$-overlap switching energy is caused by the product of the device drain-source voltage v_{DS} and the device channel current i_{CH} during the finite switching time $T_{on/off}$

$$E_{vi} = \int_0^{T_{on/off}} i_{CH} \cdot v_{DS}\, dt \tag{3.7}$$

as illustrated in Figure 3.5.

Consider the a hard-switched double-pulse test (DPT), that is illustrated in Figure 3.4(a). At turn-on of the switched device (DUT), the load current commutates from the upper switch (CTRL) (continuously in off-state, i.e. $V_{DRV}^{CTRL} = V_L$) to DUT while the switch-node is clamped at the voltage $v_{SW} = V_{DC} - v_u - v_{CTRL} - v_l$, where v_u and v_l are the voltage drops between the connections of the dc-link source and module. When the channel current of DUT reaches the load current I_L, the voltage commutation between the switches takes place. The channel of DUT is now fully conducting and its output capacitance $C_{oss(DUT)}$ is discharging through its own channel, adding a component to the channel current. As this happens, the output capacitance $C_{oss(CTRL)}$ of CTRL gets charged by V_{DC}, adding a third current component to the channel current of DUT. The channel of DUT acts as a v_{GS}-dependent resistance in series with V_{DC}. Thus, at the end of the voltage commutation, two additional loss components exists in DUT related to the half-bridge output capacitances [5]. The first $i_{C_{oss(DUT)}}$ is related to the output energy of the DUT stored in $C_{oss(DUT)}$ during off-state, discharging through the DUT channel and R_l. The second is the output energy of CTRL due to charging of $C_{oss(CTRL)}$ by V_{DC}, yielding a current $i_{C_{oss(CTRL)}}$ flowing from the dc-link, charging $C_{oss(CTRL)}$ while flowing through the channel of DUT, via R_u and R_l, as illustrated in Figure 3.6(a). The measured source current during turn-on $i_{S(on)}$ is then equal to the total channel current

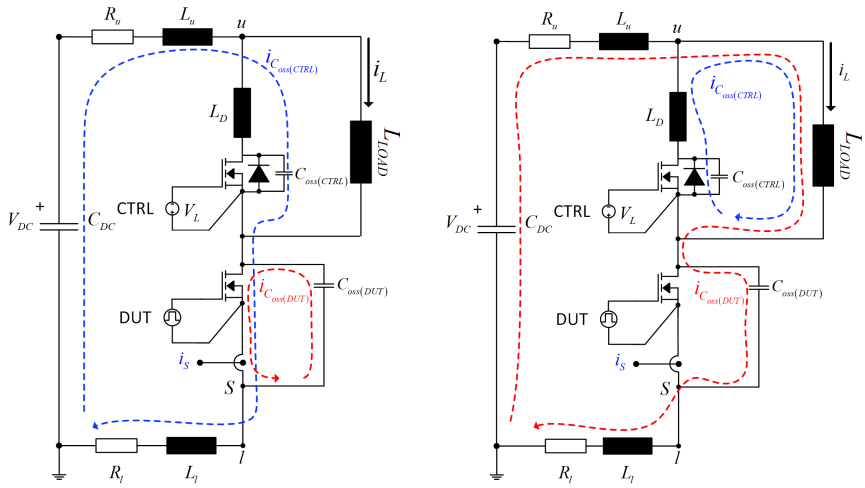
$$i_{S(on)} = i_{CH} = i_{g_o} + i_{C_{oss(DUT)}} + i_{C_{oss(CTRL)}} \tag{3.8}$$

where i_{CH} is the total channel current and i_{g_o} is the channel current component generated by v_{GS}-control of the inversion layer.

During DUT turn-off, the inductive load current source I_L is charging $C_{oss(DUT)}$ while discharging $C_{oss(CTRL)}$. The total channel current i_{CH} of DUT during the v_{DS} commutation is $(i_{C_{oss(DUT)}} + i_{C_{oss(CTRL)}})$ less than i_D prior to turn-off, and equal to $i_{CH} = i_{g_o}$. The discharge current of $C_{oss(CTRL)}$ is dissipated in the CTRL-L_{LOAD} loop, i.e. in the diode and ohmic contacts of CTRL. The current charging $C_{oss(DUT)}$ is flowing from the dc-link via $C_{oss(DUT)}$, R_u and $R_l$as illustrated in Figure 3.6(b). During turn-off, the measured DUT current $i_{S(off)}$ is then

$$i_{S(off)} = i_{CH} + i_{C_{oss(DUT)}} \tag{3.9}$$

The energy required for switching the device on and off is then the sum of the gate driver and $v \cdot i$-overlap energy



(a) Turn-on. **(b)** Turn-off.

Figure 3.6: Current path of $i_{C_{oss(DUT)}}$ (red) and $i_{C_{oss(CTRL)}}$ (blue) during switching transients.

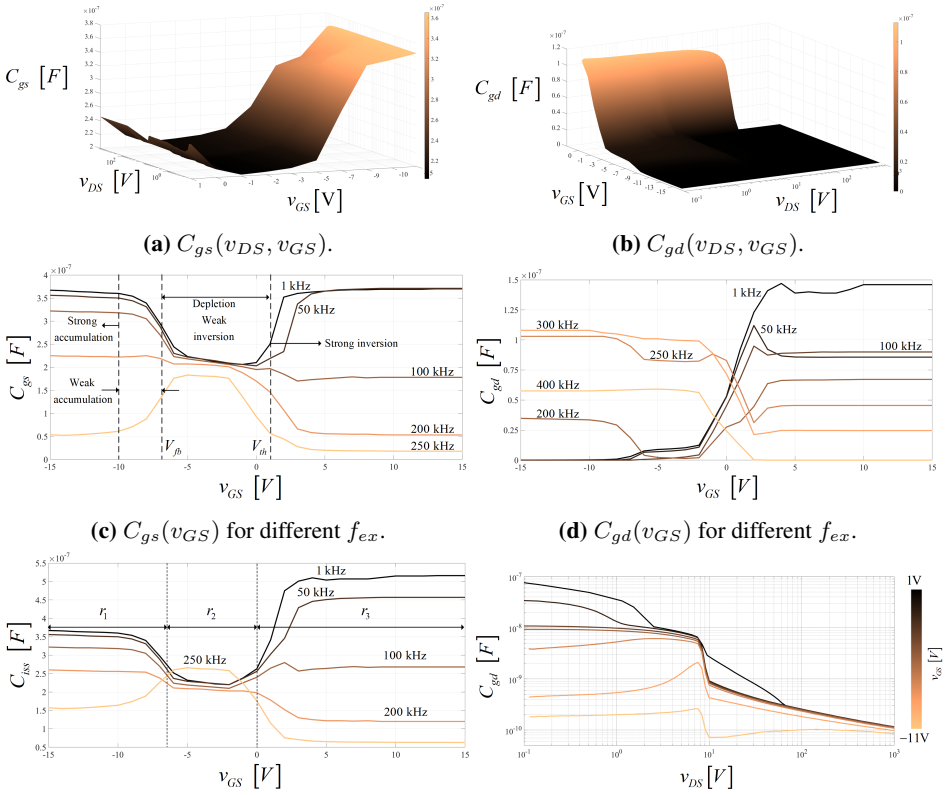
$$E_{sw} = \left(E_{D(on)} + E_{D(off)} + E_{vi(on)} + E_{vi(off)} \right) \tag{3.10}$$

3.2.2 Equivalent Device Capacitances

The equivalent device capacitances are charged and discharged during turn-on and turn-off transients, and their values are thus highly influential on the evolution of the dynamic states. The equivalent device capacitances – denoted C_{eq} and represented by the input capacitance C_{iss}, the output capacitance C_{oss} and reverse transfer capacitance C_{rss} – are integral to the evolution of the state variables and defined as follows:

$$C_{eq} \begin{cases} C_{iss} = C_{gs} + C_{gd} \\ C_{oss} = C_{ds} + C_{gd} \\ C_{rss} = C_{gd} \end{cases} \tag{3.11}$$

The equivalent device terminal capacitances are typically given in the device manufacturer datasheet only as a function of v_{DS} for a single value of the small signal measurement frequency f_{ex} and the gate-source bias V_{GS}. Although they are most likely accurate at these operating points, such simple measurements are far from



(a) $C_{gs}(v_{DS}, v_{GS})$.

(b) $C_{gd}(v_{DS}, v_{GS})$.

(c) $C_{gs}(v_{GS})$ for different f_{ex}.

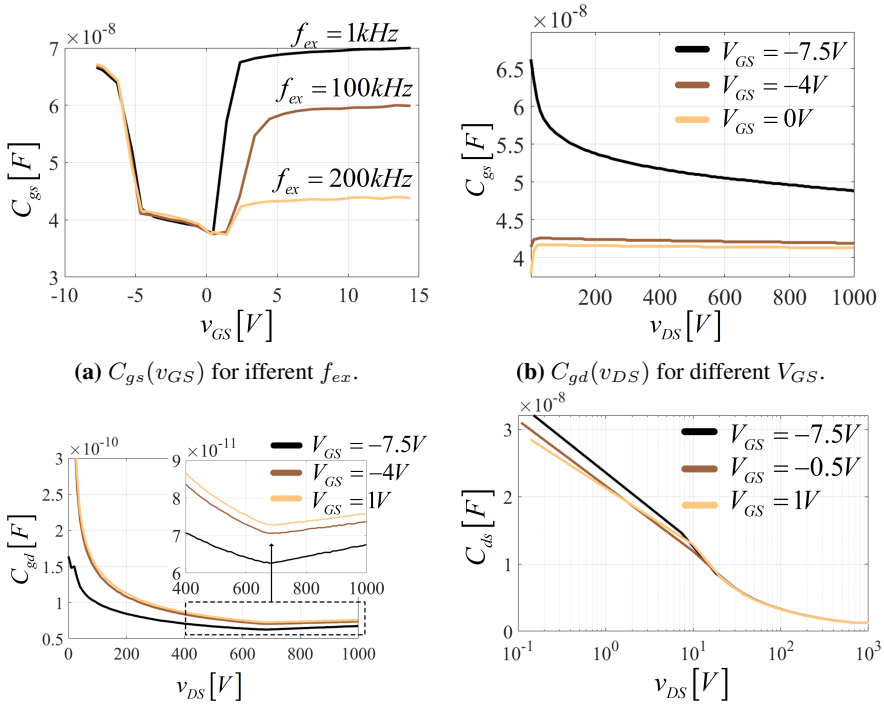
(d) $C_{gd}(v_{GS})$ for different f_{ex}.

(e) $C_{iss}(v_{GS})$ for different f_{ex}.

(f) $C_{gd}(v_{DS})$ for different V_{GS}.

Figure 3.7: Device capacitance measurements of a $3.3kV/750A$ SiC MOSFET half-bridge module using the Power Device Analyzer/Curve Tracer (Keysight B1505A).

extensive enough to cover the whole operating range of the MOSFET switching transition. Since parts of the device capacitances are bias-dependent, they vary both with respect to v_{DS} and v_{GS}. Furthermore, the value of f_{ex} has significant impact on the measured value of the capacitances. This is visualized in Figure 3.7 for a $3.3kV/750A$ SiC MOSFET half-bridge module and in Figure 3.8 for a $1.2kV/450A$ SiC MOSFET half-bridge module, which clearly illustrates the impact of v_{GS}, v_{DS} and f_{ex} on C_{eq}. The work in [J2], [J3] emphasizes the correct modelling of the half-bridge module equivalent capacitances.



(a) $C_{gs}(v_{GS})$ for ifferent f_{ex}.

(b) $C_{gd}(v_{DS})$ for different V_{GS}.

(c) $C_{gd}(v_{DS})$ for different V_{GS}.

(d) $C_{ds}(v_{DS})$ for different V_{GS}.

Figure 3.8: Device capacitance measurements of a $1.2V/450A$ SiC MOSFET half-bridge module using the Power Device Analyzer/Curve Tracer (Keysight B1505A).

3.3 Real-Time Simulation

The dynamic SiC MOSFET switching model described in [J2], [J3], [C4] is presented as real-time capable discrete-time model. The forward Euler discrete integration method allows for the model's dynamic differential equations to be transformed to HDL[3] and run on real-time capable systems such as FPGAs. This makes the dynamic switching model suitable for real-time engineering techniques such as HIL[4].

The real-time modelling and model-based engineering approach is described in [J2] and illustrated in Figure 3.9. Employing a real-time model of critical converter system components allows for a faster *design* to *realization* time. A detailed and accurate simulation model accelerates the progress in both the *Project Definition* phase – where accurate modelling of non-idealities such as semiconductor

[3] Hardware description language.

[4] Hardware-in-the-loop.

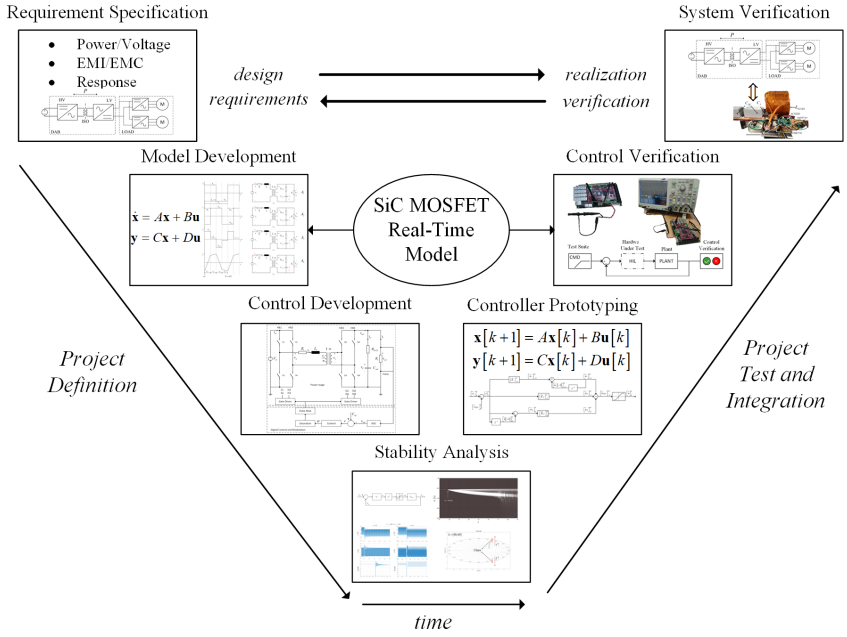


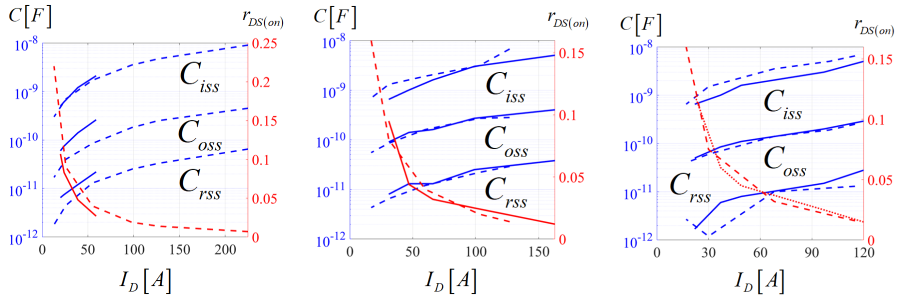
Figure 3.9: Typical model-based design V-model flowchart for converter prototyping.

voltage and currents rise and fall times – have serious impact on system performance, control and stability analysis. Similarly, in the *Project Test and Integration* phase, an accurate real-time simulation model enables more robust and optimized controller realization and accelerated testing environment through HIL verification. Thus a real-time capable plant model allows for accurate and reliable control verification through HIL simulation [J2].

The continuous-time differential equations governing the switching transition detailed in [J2], [J3] are discretized into discrete-time difference equations using the forward Euler discrete integration method

$$\left(\frac{dy}{dt}\right) \approx \frac{y\left[k+1\right]-y\left[k\right]}{T_s} = f\left(y\left[k\right]\right) \tag{3.12}$$

with $y[k]$ being the state, k the sample number and T_s the sampling period. The function $f(y[k])$ is the integrator input. Taking the differential equation governing the evolution of v_{GS} during turn-on transient (see Figure 3.4(b)), given by [J2]



(a) Manufacturer 1. **(b)** Manufacturer 2. **(c)** Manufacturer 3.

Figure 3.10: Device capacitances (blue) and $r_{DS(on)}$ (red) vs. rated continuous drain current I_D. Dotted lines is $V_{BB} = 1200V$ rated devices, full lines is $V_{BB} = 600V$ rated devices.

$$\frac{(V_H - V_L) - v_{GS}}{R_g} = (C_{gs} + C_{gd}) \frac{dv_{GS}}{dt} - C_{gd} \frac{dv_{DS}}{dt} \tag{3.13}$$

and solved as

$$\begin{gathered} \frac{dv_{GS}}{dt} = \frac{V_{HL} - v_{GS}}{(C_{gs} + C_{gd})\, R_g} + \frac{C_{gd}}{C_{gs} + C_{gd}} \frac{dv_{DS}}{dt} \\ v_{GS}(0) = V_L - \frac{C_{gd}}{C_{gd} + C_{gs}} v_{DS(on)} \end{gathered} \tag{3.14}$$

is thus discretized as

$$\begin{gathered} \frac{v_{GS}[k+1] - v_{GS}[k]}{T_s} = \frac{V_{HL} - v_{GS}[k]}{(C_{gs} + C_{gd})\, R_g} + \dots \\ \frac{C_{gd}}{C_{gs} + C_{gd}} \left(\frac{v_{DS}[k+1] - v_{DS}[k]}{T_s} \right) \end{gathered} \tag{3.15}$$

The capacitances C_{gd} and C_{gs} are dependent on both v_{DS} and v_{GS} and provided to C_{gs} and C_{gd} in "(3.15)" through LUTs with one sample delay $[k-1]$ as

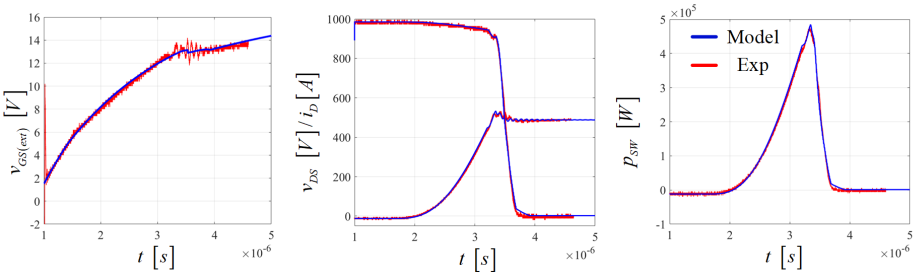
$$(3.15) \leftarrow \text{LUT} \begin{cases} C_{gs} = C_{gs}\left(v_{GS}[k-1], v_{DS}[k-1]\right) \\ C_{gd} = C_{gd}\left(v_{GS}[k-1], v_{DS}[k-1]\right) \end{cases} \tag{3.16}$$

The discretization is performed on the dynamic equations which includes derivations or integrations. The discrete-time model is built using Xilinx System Generator (XSG) toolbox in Simulink® and simulated in Simulink. XSG is used to generate a real-time capable HDL-based ip-core of the model and run on real-time capable hardware such as FPGAs for real-time simulation. Thus, as long as the ip-core clock rate and signal word lengths are high enough – as discussed in [J2] – accurate real-time dynamic models of SiC MOSFET devices can be developed. In fact, as switching transient times are inversely related to the intrinsic device capacitances, the ip-core update rate required for sufficient model accuracy increases with reduction in device capacitance. As the semiconductor $r_{DS(on)}$ increases – and hence current handling capability of the device reduces – the intrinsic device capacitances reduce since a reduction in capacitance implies a reduction in device surface area or increase in length between capacitance electrodes. This is illustrated in Figure 3.10, where intrinsic device capacitances are plotted as a function of the device $r_{DS(on)}$ for leading SiC MOSFET device manufacturers.

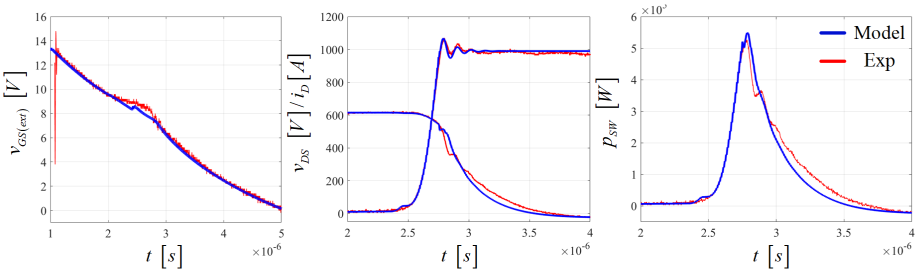
A sample set of experimental and simulated model waveforms discussed in [J2] is shown in Figure 3.11 for $3.3kV/750A$ rated SiC MOSFET half-bridge module and for a $1.2kV/450A$ rated SiC MOSFET half-bridge module shown in Figure 3.12 discussed in [J3]. The real-time models shows good accuracy with the experimental waveforms, with a deeper analysis contained in [J2], [J3].

3.3.1 Application Integration

The dynamic switching model is applicable in all power electronics topologies where the half-bridge circuit is used in a similar way as described in [J2], [J3], [C4]. For example, the dynamic switch model is integrated with the governing dynamic equations of the dual-active bridge (DAB) converter topology [6] – as illustrated in Figure 3.13(a) – in [J2], [C4]. The DAB dynamics are synthesized and implemented on the PicoZed system-on-module (SOM) shown in Figure 3.13(c). The DAB waveforms of the output load voltage v_o and output bridge current i_{B_o} using the SiC MOSFET dynamic switching model are outputted through the digital-to-analog converter (DAC) and observed in real-time on an oscilloscope. The measured DAC waveforms are shown in Figure 3.13(b). By using the dynamic switch models in dynamic models of converters, the converter real-time operation and performance can be analyzed on an early design phase. System simulation including switching dynamics can be performed in real-time. The model is suitable for HIL-testing, as well as providing a device simulation model with reduced simulation time compared to higher level tools such as LTSPICE or PLECS. With regards to the fact that users are not longer dependent on dedicated LTSPICE or PLECS models, usually provided by manufacturers, the model can act as a initial analysis tool or possibly replace existing simulation models. Power electronic system



(a) Turn-on switching waveforms for $V_{BB} = 1kV$ and $I_D = 500A$.

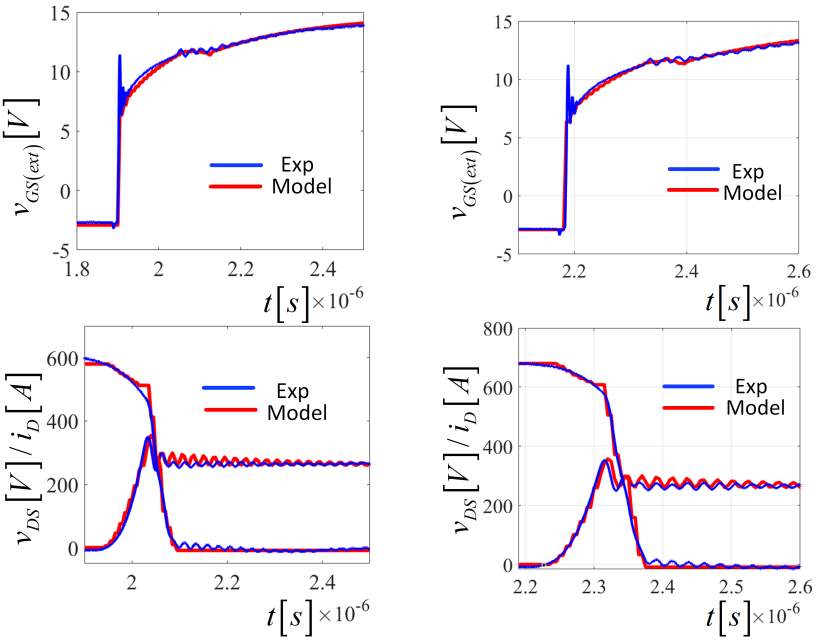


(b) Turn-off switching waveforms for $V_{BB} = 1kV$ and $I_D = 600A$.

Figure 3.11: Real-time model (blue) vs. experimental (red) switching waveforms of a $3.3kV/750A$ rated SiC MOSFET half-bridge model.

designers can use the real-time model and perform rapid converter designs and real-time closed loop control verification using HIL, without the risk for hardware failures. The same benefits can apply to device manufacturers that will be able to validate their devices' performance in power electronic systems quickly without convergence issues, which is often encountered using high-level simulation tools.

The DAB exhibits zero-voltage switching (ZVS) capabilities at specific operating points. As illustrated in Figure 3.14(a), for a voltage gain $G = nv_o/(v_i)$ and phase shift between the bridges D, ZVS in either primary or secondary bridge is possible. Considering the case where the modelled device is used in a DAB operating within the constraints of ZVS, the switching dynamics of the device is governed by the hard-switched turn-off transition of the complementary switch in the half bridge. Assume the case where the upper switch S_H is turned off in one of the bridges as illustrated in Figure 3.14(b). The drain-source voltage v_{DS}^H and drain current i_D^H behave as illustrated in Figure 3.14(c). The switch S_H is turned off under hard-switching (HS) conditions. Its v_{DS}^H rises, and since the bridge is clamped to the DC-link voltage, V_{DC}, the drain-source voltage v_{DS}^L of the lower switch S_L falls with $v_{DS}^L = V_{DC} - v_{DS}^H - v_D^L$, where v_D^L is the voltage drop of the anti-parallel diode D_L of S_L. Due to the charging/discharging of the output

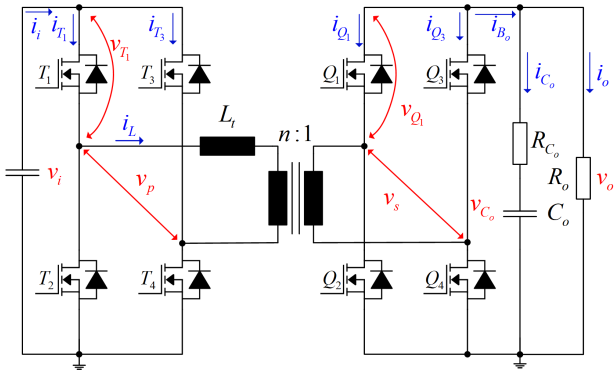


(a) Turn-on switching waveforms for $V_{BB} = 600V$ and $I_D = 300A$.

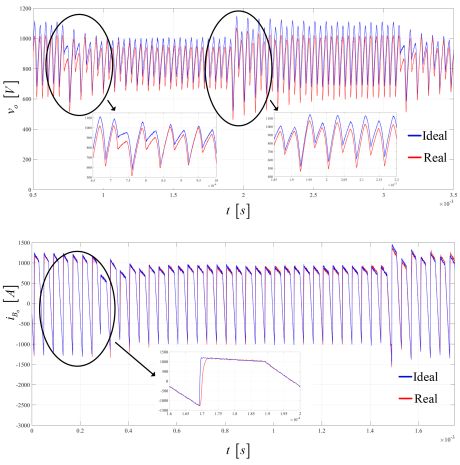
(b) Turn-off switching waveforms for $V_{BB} = 700V$ and $I_D = 300A$.

Figure 3.12: Real-time model (red) vs. experimental (blue) switching waveforms of a $1.2kV/450A$ rated SiC MOSFET half-bridge model.

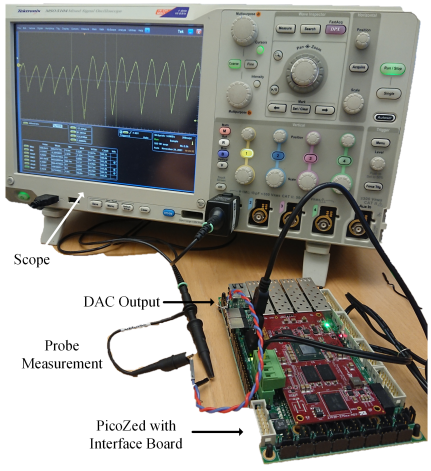
capacitances C_{oss} of the devices, the drain current of the upper switch i_D^H slightly drops as discussed in [J2], [C4]. The current i_D^H commutates to the anti-parallel diode D_L of S_L as $i_D^L = i_D^H - i_L$ where i_L is assumed constant current during the switching transient. When v_{DS}^H reaches its blocking voltage value, D_L becomes forward biased and i_D^H continues to commutate to D_L. When i_D^H reaches zero, i_L has fully commutated to D_L, causing a forward voltage drop v_D^L over S_L. At the time that i_D^H has reached zero, the lower switch S_L can turn on, thus commutating i_D^L flowing through D_L to the channel of S_L. This turn-on happens at zero voltage (only with the diode voltage drop D_L). The ZVS causes only a small power loss p_{SW}^L compared to the hard-switching power loss p_{SW}^H in the upper switch, due to the initial i_D^L increase in D_L as v_{DS}^H increases. Thus, the ZVS event of S_L can be completely captured by the description of the hard-switched turn-off event of S_H by adding the forward voltage drop v_D^L. Therefore, the presented model can be used for assessing the performance of SiC MOSFETs operating either under hard- or soft-switching conditions in power converters.



(a) Dual-active bridge (DAB) schematic.

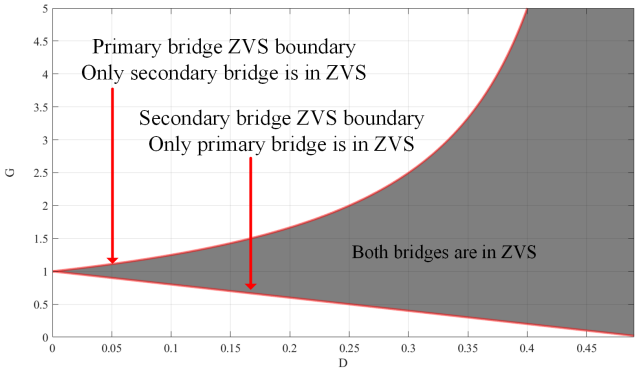


(b) RT DAC waveforms of DAB output voltage v_o (upper) and output bridge current i_{B_o} (lower).

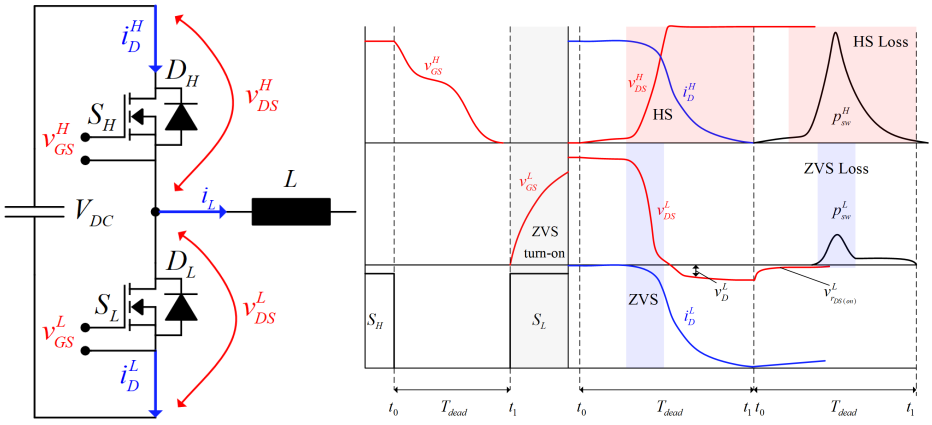


(c) RT DAB model running on the PicoZed module. The real-time waveforms of the output voltage are outputted via the DAC on the interface board and monitored with the scope.

Figure 3.13: Real-time (RT) simulation and scope supervision of ip-core outputted waveforms via the interface-board DAC.



(a) ZVS boundary for the DAB converter using single phase shift SPS) modulation.



(b) Modelled half-bridge used in the DAB.

(c) Half-bridge voltages and current waveforms during ZVS turn-on.

Figure 3.14: Dual-active bridge zero-voltage switching turn-on.

3.4 Conclusion

This chapter have focused on the mathematical modelling and real-time simulation of high-voltage, high-current SiC MOSFETs. A procedure for an accurate real-time dynamic switching model and how key device characteristics, such as the equivalent device capacitances and threshold voltage hysteresis, impacts the trajectory of drain-source voltage, gate-source voltage and source current of the device is presented. It is shown that in-depth device characteristic measurements – such as voltage dependent capacitances obtained from power device analyser – are integral to achieve high modelling accuracy of the turn-on and -off switching transient of high-voltage, high-current SiC MOSFET half bridge modules with different ratings. A discrete-time version of the dynamic model is presented and it has shown that the dynamic switching model can be implemented on the FPGA of SOM devices and run in real-time. The switching waveforms obtained using this model show a very good accuracy when compared to real experimental waveforms measured on a DPT setup. The proposed model was utilized to assess the design and operation of a high-power DAB converter, as well as to identify critical design and operating parameters of this converter, such as the turn-on and turn-off switching energies. Such models are important in assessing converter design aspect such as deadtime, switching frequency, system power density and thermal management, and hence important for an optimal converter design.

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Chapter 4

Gate Drivers

This chapter presents a number of adaptive gate drivers. These are an adaptive current source gate driver capable of double current injection/sinking during turn-on/off that was first introduced in [C2]. A deeper analysis and comprehensive experimental work of the driver was presented in [J1]. In [R1], two multi-level voltage source gate drivers are presented. One driver enables over-driving operation and is capable of independently controlling turn-on and turn-off delay times, switching times and switching energy, as well as device dv/dt and di/dt. The other is a variable-voltage-source multi-level gate driver with integrated synchronous buck converter capable of adaptively manipulating turn-off delay times, turn-off times and energy, device voltage and current overshoots, voltage and current harmonic spectrum during switching transients, as well as conduction losses. Furthermore, the voltage-source over-drive concept is compared to the conventional adaptive current source over-drive concept, which is capable of adaptively control turn-on and turn-off delay times. This chapter gives an overview of the developed adaptive gate drivers, while extensive analysis of each one can be found in [C2], [J1] and [R1].

4.1 Introduction

To efficiently conduct current, SiC power MOSFETs should have as high a voltage potential on the gate referenced to the source terminal, v_{GS} illustrated in Figure 4.1, as safely allowed by the gate dielectric material and structure. For SiC power MOSFETs, the gate-source voltage v_{GS} on-state value V_H is typically in the range of $15V$ to $20V$. The MOSFET threshold voltage V_{th} is the minimum v_{GS} required to create a conducting channel between drain and source. To stop the MOSFET from conducting current, v_{GS} must obtain a voltage level V_L which is

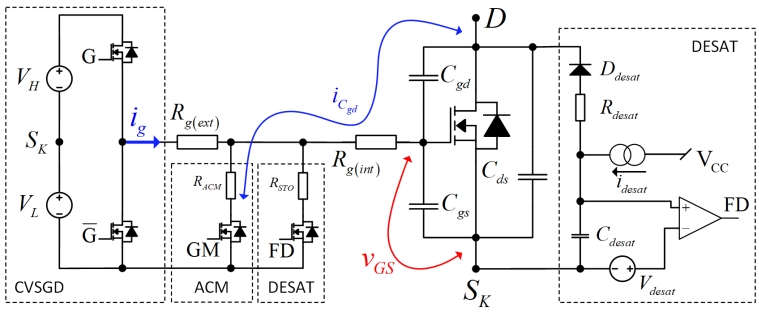


Figure 4.1: Conventional totem-pole voltage source gate driver with DESAT and ACM protection.

below V_{th} and stay there during its intended off-time. V_L is typically in the range of $-3V$ to $-10V$. Depending on several factors, most notably the values of V_H and V_L, whether the MOSFET is going from on-state to off-state or vice versa (i.e. v_{GS} traverse from V_H to V_L or from V_L to V_H), and semiconductor junction temperature, the value of V_{th} can vary, typically ranging from $1V$ to $3V$. A conventional totem-pole voltage source gate driver topology using the half-bridge circuit with the mentioned driving voltage parameters is illustrated in Figure 4.1.

To enable optimal operation of the SiC MOSFET based power electronic converter systems, it is integral to drive the SiC MOSFET devices comprising the switching blocks of the system in an optimal way. Thus, the gate driver circuits are one of the most critical building blocks in modern power electronic systems. The driver circuits are vital in ensuring the correct and optimal turn-on and turn-off transition of the semiconductor device. In this PhD thesis, the gate drive is defined as the electric circuit responsible for manipulating the charge provided to the MOSFET gate in order to facilitate the desired switching and conduction performance of the MOSFET. The gate driver tasks usually include

- *Safe operation* of the SiC MOSFET semiconductor device. This includes avoiding device failures due to short circuit in bridge-based circuit by providing the correct dead-time as well as turning the device off if a short circuit occurs. Avoid gate-oxide destruction and premature turn-on of the device due to gate voltage oscillations/spikes caused by dv/dt-induced Miller current injected into the gate path caused by turn-on of complementary bridge-switch. Avoid device voltage above rated breakdown voltage V_{BB} due to power loop parasitics and high di/dt values.

- Minimization or manipulation of device *switching loss*. A low device switching loss P_{sw}

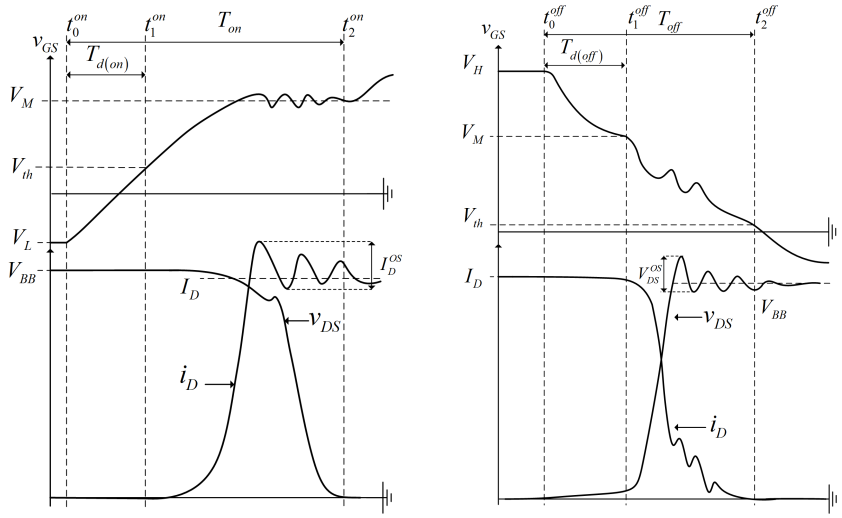
$$P_{sw} = f_{sw} \underbrace{\left(E_{on} + E_{off}\right)}_{E_{SW}\ (3.10)} \tag{4.1}$$

  yields a higher system efficiency, reducing thermal requirements while increasing system reliability and system components' lifetime. The power loss generated by current-voltage overlap of the device induces Joule heating. Due to the thermal impedances between device channel and ambient temperature, the junction temperature increase. The stress induced on the semiconductor depends on the maximum temperature, average temperature and the magnitude of the temperature fluctuations [1]. In fact, Young's modulus of SiC is around 3 times that of Si, resulting in higher temperature-dependent mechanical stress in SiC-based devices compared to Si-based devices [2]. The temperature-induced mechanical stress might cause failures such as bond wire lift-off and solder fatigue, as well as module aging due to direct bonded copper (DCB) substrate strain and silicone gel aging [1]. Power cycling and the consequential temperature swings leading to mechanical stress is a major factor of power module failure [3, 4].

The *safe operation* challenges have been present since the introduction of the transistors and are met with robust solutions. When MOSFETs are operated in bridge circuits (e.g. in synchronous converters), cross-conduction of the upper and lower switch may occur if there is not sufficient time between upper and lower switch switching events (i.e. dead-time). Implementing the optimal dead-time is a challenge and have a major impact on converter's operation. Converters suitable for high-power transmission, such as the dual-active bridge (DAB) converter, experience dead-time effects such as voltage reversal, voltage sag, phase drift, and increased reflow power [5]. The DAB is also not able to transfer its rated power with too high dead-time, while – aside from potential bridge short circuiting – a too low dead-time may lead to loss of zero-voltage switching (ZVS) capabilities, especially at light loads [6]. Deciding on the optimal dead-time T_{dt} requires detailed knowledge of the device switching transients. The dead-time should be larger than (ideally equal)

$$T_{dt} \geq T_{off} - T_{d(on)} \tag{4.2}$$

where T_{off} is the turn-off time and $T_{d(on)}$ is the turn-on delay time of the complementary switches of a half-bridge, as defined in Figure 4.2. The total switch-



(a) Turn-on. **(b)** Turn-off.

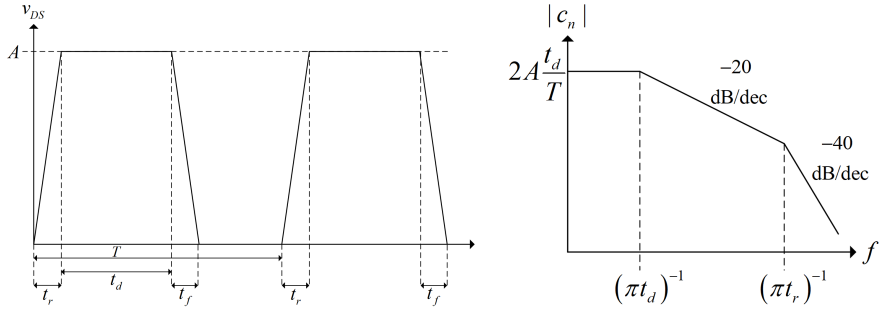
Figure 4.2: Theoretical switching waveforms

ing time is T_{on}/T_{off}, while the partial switching time is defined as $T_{p(on)} = T_{on} - T_{d(on)}$ and $T_{p(off)} = T_{off} - T_{d(off)}$. An accurate model to determine these parameters is thus beneficial in converter design phases. The gate-drain dv/dt-induced Miller current $i_{C_{gd}}$

$$i_{C_{gd}} = C_{gd}\frac{dv_{DS}}{dt} \tag{4.3}$$

may cause gate oscillations, premature turn-on or gate oxide destruction. Such effects are commonly dealt with by including an active Miller clamp (ACM) circuit to the gate driver, shunting $i_{C_{gd}}$ into a low-impedance path through R_{ACM} to mitigate the effects. Figure 4.1 shows the conventional totem-pole voltage source gate driver with the ACM and DESAT logic. The GM signal is high when the dv/dt of opposing bridge switch is expected. Shorts circuits in SiC MOSFET are commonly dealt with by a desaturation (DESAT) detection circuit or a direct device current sensing scheme, such as shunt resistor or device parasitic inductance sensing. The DESAT logic monitors whether v_{DS} voltage reaches the pre-defined DESAT threshold voltage V_{desat} during a short-circuit event. The FD signal latch high, enabling a soft turn-off through R_{STO}.

The manipulation of *switching loss* is limited for the conventional totem-pole voltage source gate drivers (CVSGDs), as they have limited design parameters



(a) Trapezoidal approximation of PWM-switched device's v_{DS} with its rise-time t_r equal to its fall-time t_f.

(b) Magnitude spectral envelope.

Figure 4.3: Theoretical spectral envelope of a trapezoidal approximation of a PWM switched device's v_{DS}.

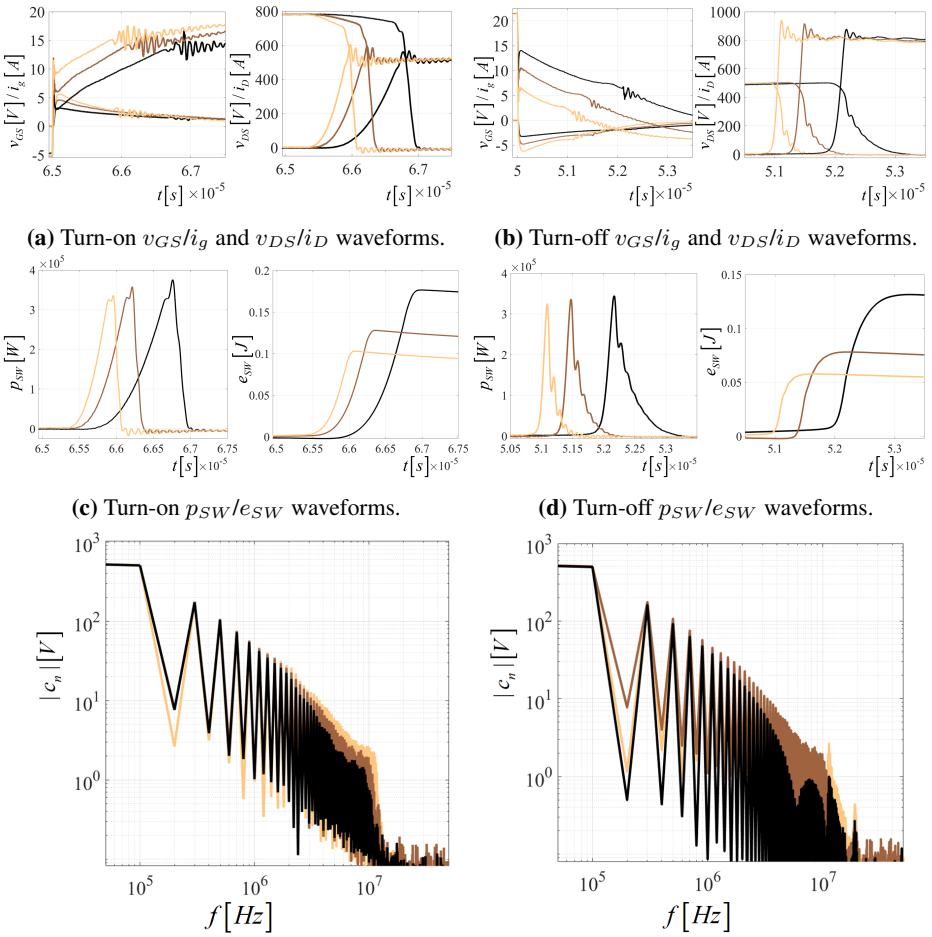
available for shaping the switching transients. The on-state voltage level V_H and off-state voltage level V_L are fixed and limited by the voltage rating of the gate $[V_{GS}^{max}, V_{GS}^{min}]$, usually in the range of $[20\,V, -10\,V]$ for SiC MOSFETs. The lower limit of R_g is generally limited by the device's internal resistance $R_{g(int)}$. For a CVSGD, the gate current i_g is given by

$$i_g = \frac{(V_{HL} - v_{GS})}{R_g} = \frac{V_{HL}}{R_g} e^{-t/\tau_{iss}} \tag{4.4}$$

where $R_g = R_{g(ext)} + R_{g(int)}$, $V_{HL} = V_H - V_L$, $C_{iss} = C_{gs} + C_{gd}$, $\tau_{iss} = C_{iss} R_g$ and neglecting the gate-source loop inductance. This governs how fast charge can be moved into and from the gate, and hence how fast the device can be turned on and off. The CVSGD drive strength, defined by the peak gate current the circuit can provide, is thus limited to

$$I_g = \frac{V_{HL}}{R_g} \tag{4.5}$$

The device is considered turned on when the output capacitance $C_{oss} = C_{gd} + C_{ds}$ is discharged while $v_{GS} \geq V_{th}$. Thus, the only configurable design parameters available for the CVSGD for a given device are the V_H/V_L values and R_g. For given values of V_H/V_L, lowering the R_g results in lower switching times hence a lower switching loss. However, this reduce the gate loop damping, increasing device voltages and current slew rates. This increases the bandwidth and shifts



(a) Turn-on v_{GS}/i_g and v_{DS}/i_D waveforms.

(b) Turn-off v_{GS}/i_g and v_{DS}/i_D waveforms.

(c) Turn-on p_{SW}/e_{SW} waveforms.

(d) Turn-off p_{SW}/e_{SW} waveforms.

(e) Spectral content of v_{DS} during turn-on.

(f) Spectral content of v_{DS} during turn-off.

Figure 4.4: Turn-on and -off switching transients using the CVSGD for $R_{G(ext)} = 1.25\Omega$ (yellow), $R_{G(ext)} = 2.5\Omega$ (brown) and $R_{G(ext)} = 5\Omega$ (black).

the spectral content of the electromagnetic energy generated by the switch during switching transients to higher frequencies. Assuming an equal rise and fall time $t_f = t_r$ of a PWM-switched device's v_{DS}, it can be approximated as an trapezoidal waveform as illustrated in Figure 4.3(a). The trapezoidal waveform has the frequency content described by the summation of the harmonic amplitudes

$$x(t) = c_0 + \sum_{n=1}^{\infty} 2c_n \cos(n\omega_0 t + \angle c_n), \quad \omega_0 = \frac{2\pi}{T} \tag{4.6}$$

$$c_0 = \frac{At_d}{T} \qquad c_n = \frac{2At_d}{T}\left|\frac{\sin\left(n\pi t_d/T\right)}{\left(n\pi t_d/T\right)}\right|\left|\frac{\sin\left(n\pi t_r/T\right)}{\left(n\pi t_r/T\right)}\right| \tag{4.7}$$

giving an amplitude envelope as seen in Figure 4.3(b). Reducing t_r/t_f increases the higher frequency content of the electric E and magnetic B fields, increasing the higher-frequency electromagnetic field energy density given by

$$u = \frac{(\mathbf{E}\cdot\mathbf{D} + \mathbf{B}\cdot\mathbf{H})}{2} \tag{4.8}$$

where $\mathbf{E}$ is the electric field, $\mathbf{D} = \epsilon\mathbf{E}$ is the electric displacement field, $\mathbf{B}$ is the magnetic flux density and $\mathbf{H} = \mu\mathbf{B}$ is the magnetizing field, with μ being the permeability of the material and ϵ being the permittivity of the material[1]. Furthermore, the oscillations caused by device and power loop inductances and capacitance adds to the high-frequency spectral content.

This is visualized in Figure 4.4, where a SiC MOSFET half-bridge module is switched in a double-pulse test using the totem-pole CVSGD of Figure 4.1 with different vales of $R_{g(ext)}$. The lower total R_g allows for faster charge transfer to/from the gate, hence lower switching times and higher voltage/current slew rates. This reduces the instantaneous power loss due to $v_{DS}\cdot i_D$ product, resulting in a lower total switching energy E_{SW} and lower average switching loss (4.1) over a switching cycle. The higher slew rates of the voltage and current shifts the frequency content of the waveforms to higher frequencies, as seen in Figure 4.4(e) and Figure 4.4(f). The turn-on spectral content is extracted from a trapezoid as seen in Figure 4.3(a) using the turn-on waveform for both the turn-on and -off transients, with $1/T = 100kHz$. The same is done for the turn-off spectral content, only using the turn-off transition for both the turn-on and -off transient. Of the shown waveforms, the yellow colored waveforms have the lowest gate resistance, hence highest v_{DS} and i_S slew rates, hence more frequency content located at higher frequencies than the higher gate resistance waveforms (brown/black). As pointed out in chapter 1, while it is clear that increased switching frequency reduce volume and weight of passive components, the relationship between the required attenuation of an electromagnetic interference (EMI) filter as a function of frequency, its volume and its mass is less clear [7]. The benefits of reduced switching losses can reappear as challenges with respect to filtering. Increasing high-frequency content may cause challenges in EMI filtering strategies, as parasitic inductance and capacitances of passive and active filter elements, printed circuit board (PCB) tracks

[1] Poynting's theorem in this form is limited to fields in vacuum and nondispersive linear materials.

and cables may cause unwanted frequency interactions and resonances with the filtered waveforms.

Voltage and current ratings of SiC MOSFETs influence its device parameters. The device continuous drain-current I_D rating is limited by the device thermal capabilities, with limiting factor typically being maximum allowed junction temperature $T_{j(max)}$ for a fully turned on device. The current rating is thus limited by the power dissipation of the device. As the conduction loss is proportional to $r_{DS(on)}$, a higher current rating typically demands a lower $r_{DS(on)}$ for a given conduction loss performance. A lower $r_{DS(on)}$ requires a larger surface area for a given voltage rating (i.e. drift region length). Thus, the resulting larger surface area of the device electrodes required for larger current handing increase the device capacitances given by

$$C = \epsilon_0 \epsilon_r \frac{A}{d} \tag{4.9}$$

where ϵ_0 is vacuum permittivity, ϵ_r is the relative permittivity of the material in between the electrodes, A is the area overlap of and d is the distance between the two electrodes. Increasing the voltage rating demands a thicker drift region, increasing the distance between drain-source and drain-gate. Thus, C_{oss} and C_{rss} might actually decrease for higher rated blocking voltages. To create the inversion layer in the MOSFET channel, sufficient charge must be moved from the driver power supply to the gate electrode to lift the gate-source potential above the threshold voltage. As the rate of change of the voltage across a capacitor is related to the rate of change of the charge

$$\frac{dQ}{dt} = i = C\frac{dv}{dt} \tag{4.10}$$

a higher capacitance results in a slower voltage change for the same current. Thus, the CVSGD is limited in its driving capability, i.e. its charge moving ability, due to its power supply on- and off-state driving voltages and the total gate driving circuit gate resistance.

Designing a power electronic system using a CVSGD forces the user to compromise between switching loss, EMI and device voltage/current overshoots. The switching loss directly impacts overall system efficiency, affecting thermal requirements, system robustness and reliability as well as gravimetric and volumetric system traits. EMI caused by fast device voltage/current slew rates and oscillations pose challenges with respect to EMC standards and interaction with nearby electronic equipment. Voltage and current overshoots increase the electrical device

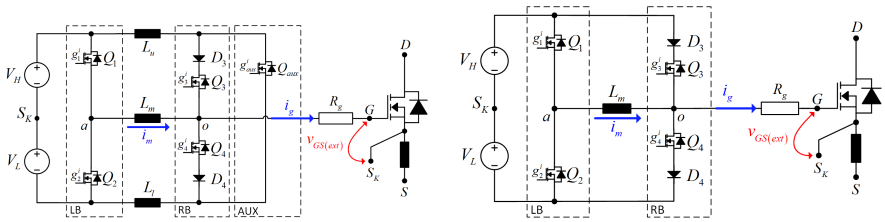
stress. Adding to the complexity is that these parameters change with source and load variations.

However, by employing adaptive gate drivers, a more flexible power electronic system can be designed, and the limitations of CVSGD can be overcome. CVSGD are often limited to a maximum gate drive peak current. The relatively high input capacitance of high-power SiC MOSFET devices resulting in a slower evolution of v_{GS}, allows for a larger time span for manipulation of the gate current. Thus, their high input capacitance, which limits the switching speed of the device using CVSGD, becomes an opportunity to shape the voltage and current transients of the device to the designer's needs by utilizing adaptive gate driving circuits.

4.2 Adaptive Gate Drivers

Adaptive gate drivers allows for precision manipulation of gate current i_G and gate-source voltage v_{GS}, enabling control of the switching energy, conduction power losses, dv/dt and di/dt without modifying the power or gate drive circuit hardware. Non-idealities (or parasitics) exist in the power circuit, such as stray inductance in power module leads, DC-link bus-bars and gate-driver loop and stray capacitance between transformer sides and windings, within power module packages and within the semiconductor die. Such non-idealities may cause unwanted effects during switching transients, such as v_{DS} overshoots and high frequency oscillations in power and gate loops. Considering the turn-off transition using a CVSGD, increasing the device di/dt reduce the turn-off switching loss, but increase the voltage overshoot seen between device source and drain. Thus, switching the transistor using a CVSGD is a compromise between efficiency and safety margin. A higher efficiency is beneficial as a higher percentage of the source energy is transferred to the load to perform the intended work, and less is dissipated as heat. However, due to the unavoidable stray inductance in the power loop, the device di/dt induces oscillatory voltage overshoots in the device v_{DS} above the device steady-state blocking voltage, and the device must hence be rated at higher voltage. The effects caused by unavoidable parasitics can be manipulated and – to a certain extent – mitigated by adaptive gate driver circuits. For example, by sensing system voltages or load conditions, the presented adaptive gate drivers can adjust the device di/dt to accommodate the device's blocking voltage safety margin – and consequently adjust the device switching loss – as will be discussed in the following sections.

Three novel gate driver topologies capable of adaptive gate-driving functionalities are introduced in this work. The driver topologies are categorized as follows.



(a) Current source gate driver capable of over-drive and extended adaptive operation.

(b) Conventional current source full-bridge gate driver capable of over-drive operation.

Figure 4.5: Schematic diagrams of current source adaptive gate drivers.

4.2.1 Adaptive Over-Drivers

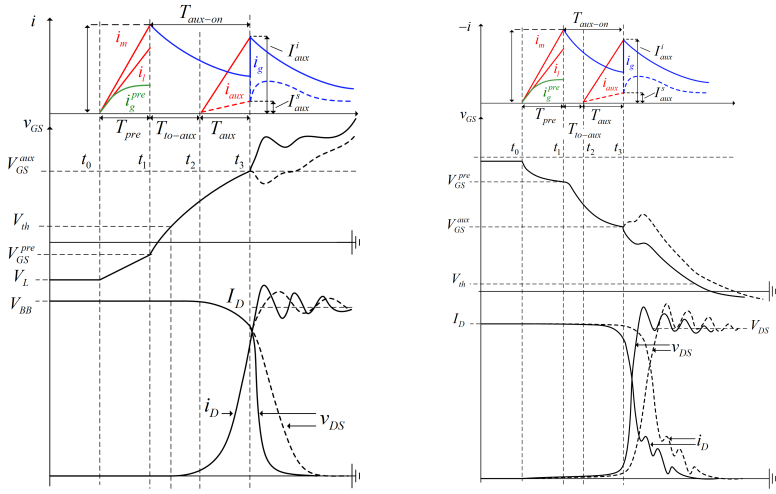
Adaptive over-drivers are defined as adaptive gate drivers capable of supplying a higher peak current I_g than the corresponding peak gate current using the CVSGD defined by "(4.5)". Within this category, the drivers can further be classified into two categories

- Adaptive Current Source Over-Driver (ACSOD),
- Adaptive Voltage Source Over-Driver (AVSOD).

4.2.1.1 Adaptive Current Source Over-Driver

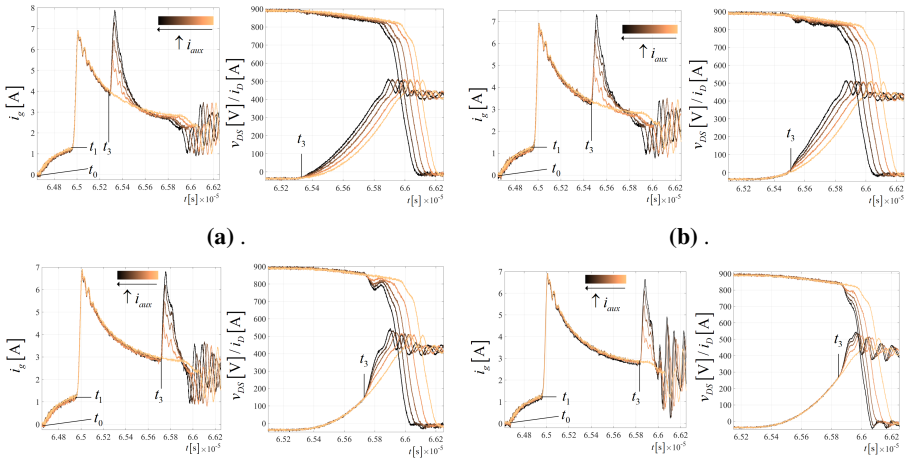
The adaptive current source over-drivers (ACSOD) are magnetic energy based drivers. They generate over-drive and adaptive driving capabilities by charging inductors to predefined current levels. The ACSOD can operate as a full-bridge based driver with an auxiliary switch, making the driver capable of both over-driving and multiple gate current injections/sinkings (Extended Adaptive Current Source Over-Driver (EACSOD)) during switching transients. This driver – illustrated in Figure 4.5(a) – was first introduced in [C2] and further explored in [J1]. By operating the driver without the auxiliary switch, the driver retains its over-driving capabilities, but loose its extended adaptability. This is the conventional full-bridge current source gate driver (CCSGD), as illustrated in Figure 4.5(b).

The adaptive turn-on and -off operation are illustrated in Figure 4.6 with a set of experimental results showing ACSOD adaptive turn-on is shown in Figure 4.7. Further discussions and experimental results are given in [C2], [J1] and [R1].



(a) Turn-on. **(b)** Turn-off.

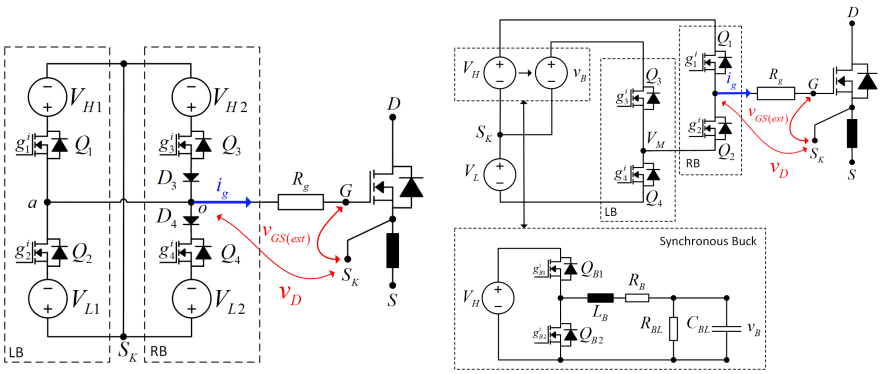
Figure 4.6: Adaptive current source over-drive with extended operation.



(a) . **(b)** .

(c) . **(d)** .

Figure 4.7: Experimental results showing EACSOD with different values of I^i_{aux} and t_3 .



(a) Voltage source gate driver capable of over-drive and extended adaptive operation.

(b) Variable voltage source multi-level gate driver.

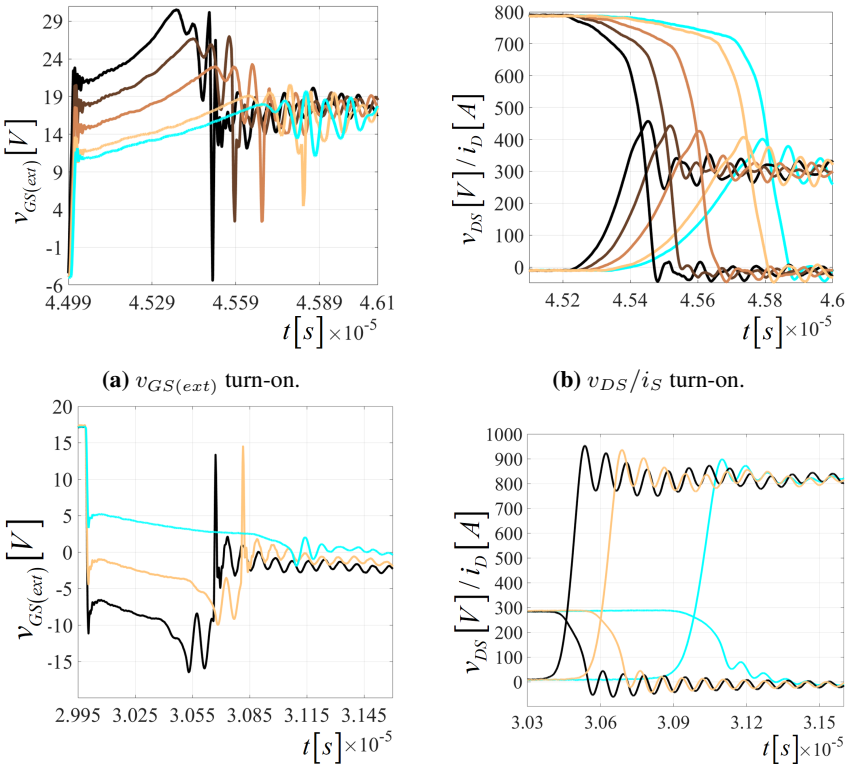
Figure 4.8: Schematic diagrams of voltage source adaptive gate drivers.

4.2.1.2 Adaptive Voltage Source Over-Driver

The adaptive voltage source over-drivers (AVSOD) are full-bridge based driver which utilize voltage sources with different potential levels to generate its over-driving capability as well as its extended adaptability. The driver schematic is illustrated in Figure 4.8(a). The AVSOD driver is introduced in [R1].

The voltage sources V_{H1} and V_{H2} are used for turn-on, while the voltage sources V_{L1} and V_{L2} are used for the turn-off process. For the configuration presented in [R1], the voltages V_{H1} and V_{L1} are used as over-drive voltages, i.e. $V_{H1} > V_{H2}$ and $V_{L1} > V_{L2}$, while V_{H2} and V_{L2} are kept at a fixed level corresponding to conventional V_H and V_L driving levels. By controlling the switches Q_1 and Q_3, the applied gate driving voltage v_D, takes either the value of V_{H1} or V_{H2} at turn-on, while it either takes the voltage V_{L1} or V_{L2} at turn-off. Depending on when the voltage source is applied to the gate during the switching transients, different switching properties can be achieved, including turn-on and -off full over-drive mode, delay control mode, independent di/dt and dv/dt control mode and combined di/dt and dv/dt control mode as is explored in [R1].

Figure 4.9 shows experimental results using the AVSOD gate driver in full over-drive mode, as given in [R1]. Turn-on full over-drive mode with V_{H1} ranging from $25V$ to $40V$ is shown in Figure 4.9(a) and Figure 4.9(b), while turn-off full over-drive mode with V_{L1} ranging from $-15V$ to $-24V$ is shown in Figure 4.9(c) and Figure 4.9(d). Note that in these figures showing AVSOD experimental waveforms, the $v_{GS(ext)} = v_D - (i_g R_g)$ is measured, hence showing a different voltage than the applied v_D. Figure 4.10 shows the percentage change in turn-on/off delay



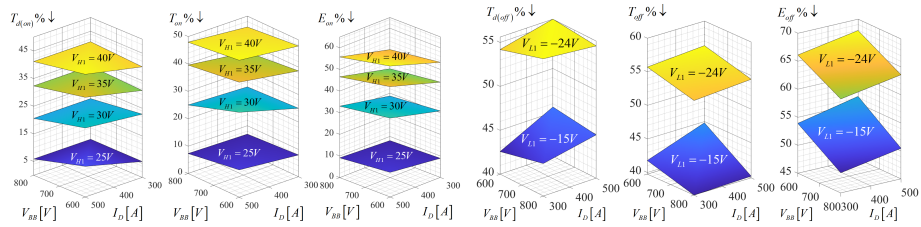
(a) $v_{GS(ext)}$ turn-on.

(b) v_{DS}/i_S turn-on.

(c) $v_{GS(ext)}$ turn-off.

(d) v_{DS}/i_S turn-off.

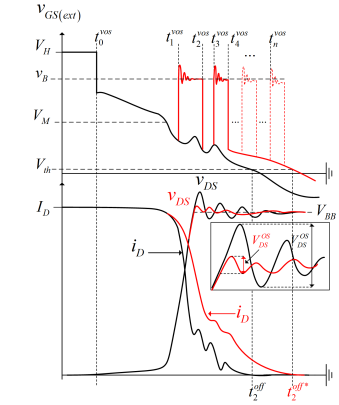
Figure 4.9: Experimental results showing AVSOD turn-on and -off switching transients using full over-drive mode.



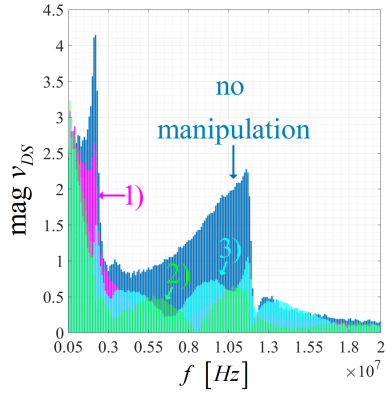
(a) Turn-on change in turn-on delay time $T_{d(on)}$, turn-on time T_{on} and turn-on energy E_{on}.

(b) Turn-off change in turn-off delay time $T_{d(off)}$, turn-off time T_{off} and turn-off energy E_{off}.

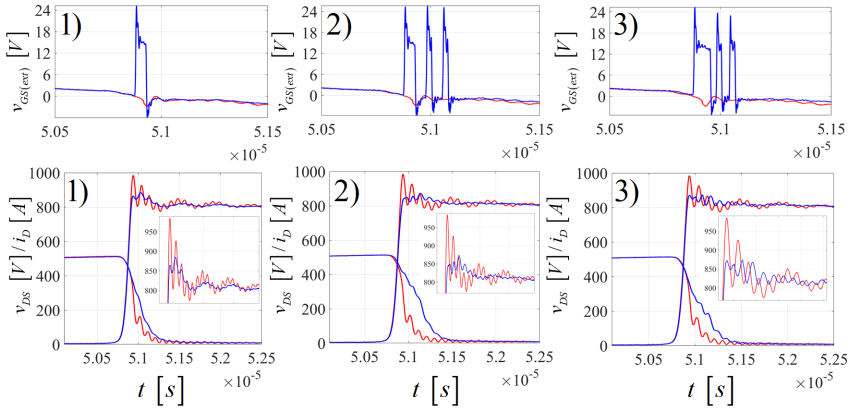
Figure 4.10: AVSOD turn-on and -off full over-drive mode parameter change from experimental results.



(a) Theoretical switching waveforms.



(b) Frequency spectrum of v_{DS} oscillations during turn-off.



(c) $v_{GS(ext)}$ with $v_B = 15V$ upper figures and i_D/v_{DS} lower figures.

Figure 4.11: Multi-pulse VVSMGD turn-off v_{DS} oscillation manipulation.

time, turn-on/off time and turn-on/off switching energy of the AVSOD in overdrive mode compared to the CVSGD. Further discussions and experimental results are given in [R1].

4.2.2 Variable Voltage Source Multi-level Gate Driver

Variable Voltage Source Multi-level Gate Driver (VVSMGD) are defined as adaptive gate drivers which are capable of providing a variable voltage to the driven gate. The driver introduced in [R1] is illustrated in Figure 4.8(b). The driver uses combinations of the four switches $(Q_1 - Q_4)$ to provide the static voltage V_H/V_L or the variable voltage v_B to the driven gate.

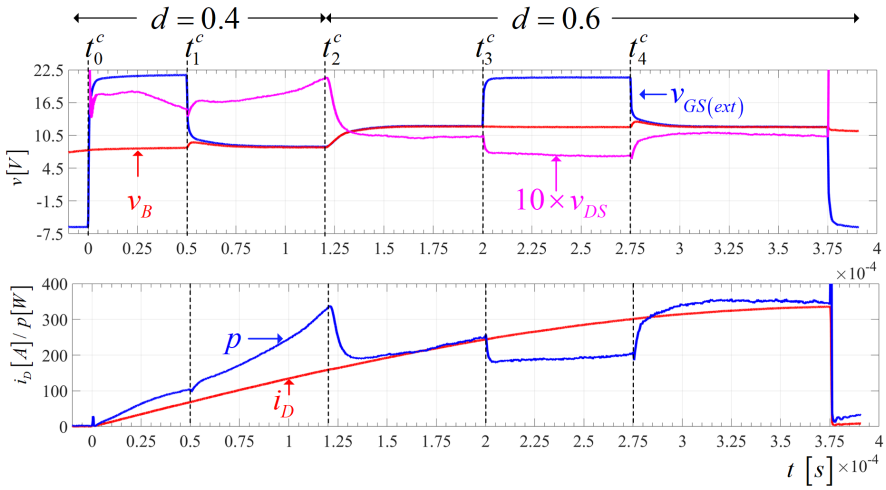
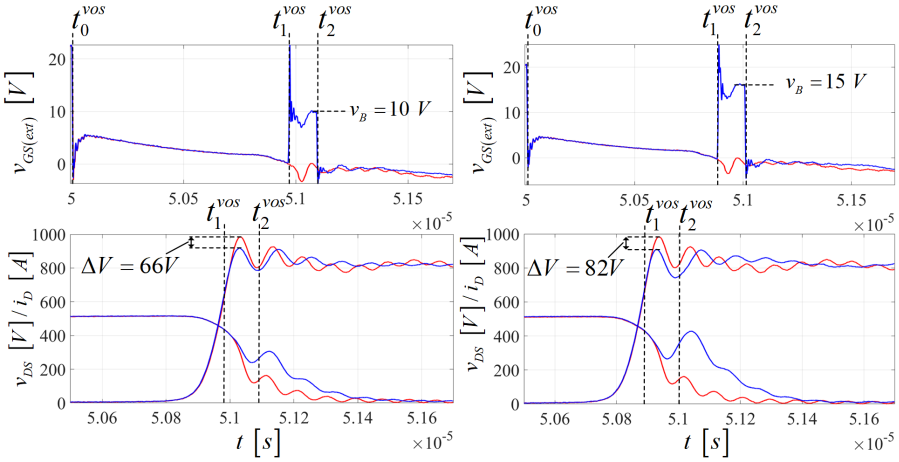


Figure 4.12: Experimental single pulse test waveforms showing VVSMGD conduction loss manipulation operation. Upper figure shows v_{GS} (blue waveform), v_B (red waveform) and $10 \cdot v_{DS}$ (magenta waveform) with the buck converter duty-cycle d changes. The lower figure shows the drain current i_D (red waveform) and the instantaneous power loss of the device $p = i_D \cdot v_{DS}$.

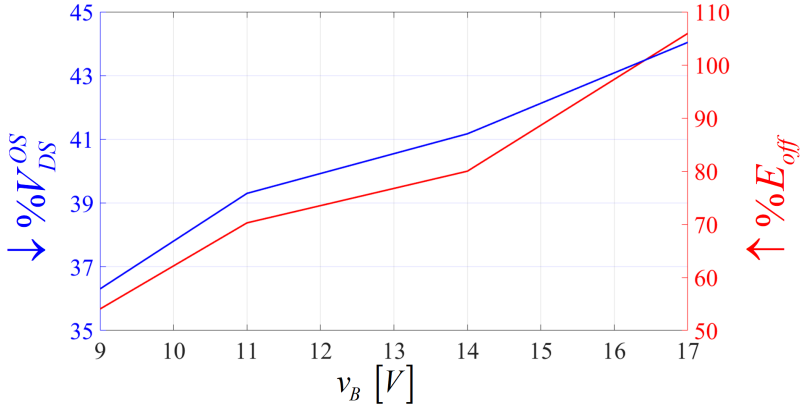
With the synchronous buck converter, the driver can regulate the voltage $v_B = d \cdot V_H$, where $d = [0, 1]$ is the duty-cycle of buck's high-side switch Q_{B1}. The v_B can be regulated at any given time instant, i.e. either during device on or off state, regulate to a constant v_B value or some arbitrary waveform, e.g. a sine wave (see Figure 5.3(a)).

The VVSMGD has several operating modes which can be used separately or together summarized below and further discussed in [R1].

- *Switching Delay Manipulation* - The device turn-off delay time $T_{d(off)}$ can be manipulated by providing the variable voltage source v_B to the gate prior to the actual turn-off instant. By adjusting the duty-cycle d of the buck converter, v_B can be set to a pre-defined voltage level. Similarly, by adjusting v_B to a value below device threshold voltage V_{th} and applying v_B to the gate prior to turn-on allows reduction of turn-on delay time $T_{d(on)}$.
- *Turn-off Voltage Overshoot Manipulation* - By controlling v_{GS} during v_{DS} overshooting oscillatory behaviour, the magnitude of the overshoot V_{DS}^{OS} and frequency spectrum of the oscillations can be manipulated. By manipulating v_{GS} while the MOSFET is in the saturation region, the slope of i_D can be adjusted, and the overshoot and oscillatory behaviour of v_{DS} controlled.



(a) Experimental switching showing $v_B = 10V$ (left) and $v_B = 15V$ (right) in blue waveforms compared to no overshoot manipulation shown in red waveform color.



(b) V_{DS}^{OS} reduction and E_{off} increase.

Figure 4.13: VVSMGD in single pulse mode.

- *Turn-on Current Overshoot Manipulation* - Similarly to the turn-off voltage overshoot manipulation, by controlling v_{GS} during i_D peak time (i.e. when v_{GS} reaching the Miller plateau and v_{DS} is falling) the i_D peak value can be manipulated.

- *Conduction Loss Manipulation* - By manipulating v_{GS} during DUT conduction, the value of the drain-source on-state resistance $r_{DS(on)}$ can be adjusted. Thus, the drain-source voltage $v_{DS(on)} = r_{DS(on)} \cdot i_D$ is controllable and consequently the instantaneous conduction loss.

Considering for example the turn-off transient, a high di/dt causes oscillatory overshoots in device v_{DS}. The magnitude and frequency spectrum of the v_{DS} oscillations can be manipulated by applying v_B – with potentially different amplitudes – to the gate during the turn-off instant. The cost is increasing turn-off switching losses since i_D slew rate increases. This VVSMGD's operating mode is shown in Figure 4.11. The theoretical v_B injection pattern is illustrated in Figure 4.11(a), where Figure 4.11(c) shows experimental switching waveforms with different injection patterns of the buck voltage v_B at $15V$. The impact on the frequency spectrum of the v_{DS} oscillations (that is v_{DS} minus steady-state V_{BB}) is shown in Figure 4.11(b), where it can be seen that the frequency spectrum can be significantly manipulated using the operation mode. Manipulation of the waveform's frequency spectrum can be beneficial when certain operation modes benefits from reduced EMI compared to switching losses or vice versa. An example can be that the power electronic system employing the adaptive gate driver temporary operate around EMI sensitve equipment, where higher system losses can be tolerated for the needed reduction in EMI.

Experimental results showing the conduction loss manipulation mode are shown in Figure 4.12. At $t = t_0^c$, the device under test (DUT) is turned on with $v_{DRV} = V_H = 20V$ applied to the gate. At $t = t_1^c$, Q_2 and Q_3 are turned on while Q_1 is turned off, applying $v_B = 9V$ to the gate. Thus, as $v_{GS} \rightarrow v_B$, $r_{DS(on)}$ increases, affecting v_{DS}. At $t = t_2^c$, v_B is still applied to the gate, but a change in the duty-cycle of the buck converter from $d = 0.4 \rightarrow d = 0.6$ is performed, resulting in $v_B \rightarrow 11V$, reducing $r_{DS(on)}$ and v_{DS}. At $t = t_3^c$, V_H is applied to the gate, further reducing $r_{DS(on)}$ and v_{DS}. Again, at $t = t_4^c$, $v_B = 11V$ is applied to the gate and $r_{DS(on)}$ and v_{DS} increase. The drain current i_D (red waveform) and instantaneous power loss $p = i_D \cdot v_{DS}$ (blue waveform) are shown in the lower plot in Figure 4.12, and it is clear how manipulating v_{GS} results in fine-grained control of the conduction power loss, p. Figure 4.13 shows experimental results of v_{DS} overshoot, V_{DS}^{OS}, manipulation operation of the VVSMGD, where its seen that by applying different values of v_B in a single pulse, V_{DS}^{OS} can be controlled. Applying higher values of v_B reduce the V_{DS}^{OS} at the cost of increasing the turn-off switching energy E_{off}, as seen in Figure 4.13(b). The experimental results are performed on an inductive load pulse-test setup shown in Figure 4.14.

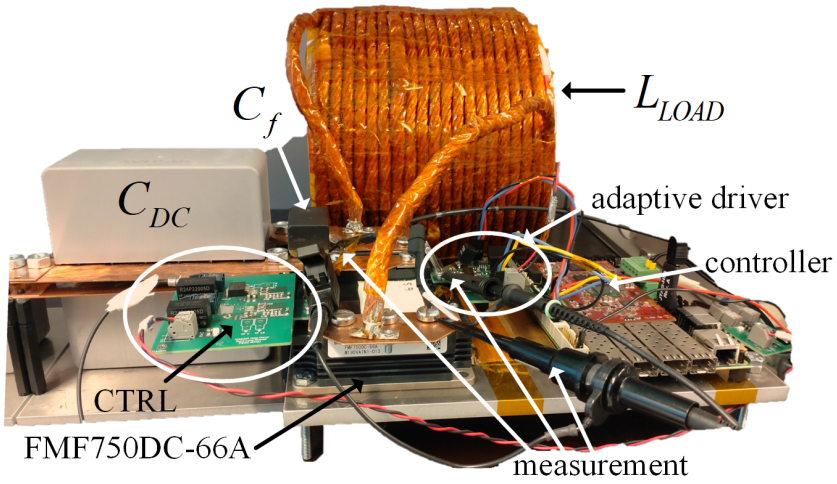


Figure 4.14: Photograph of the experimental setup.

4.3 Discussion

A summary of the capabilities of the discussed gate driver topologies is given in Table 4.1. The presented capabilities include gate over-driving (OD), controlling turn-on/off delay time $T_{d(on)}$/$T_{d(off)}$, controlling turn-on/off partial switching time $T_{p(on)}$/$T_{p(off)}$, controlling dv/dt and di/dt at turn-on and turn-off and conduction loss (CL). The symbol $\times$ indicates that the driver lacks the ability to control this parameter. The symbol Y^i indicates that the driver can independently control the parameter without significantly affecting the other parameters. The symbol Y^c indicate that the driver can control the parameter, but it will affect some of the other parameters. The symbol $Y_{\downarrow}$ means the driver has the ability only to reduce the parameter, as is the case with the VVSMGD. As this driver incorporates a buck converter from the on-state voltage V_H, the driver may only reduce dv/dt and di/dt parameters during the partial switching transient. The symbol P indicates that the driver can passively control the parameter, e.g. through hardware interference changing the gate resistance R_g.

Table 4.2 shows the maximum achieved parameters changes during experimental testing of the adaptive gate driver capable of over-driving, i.e. AVSOD and ACSOD, compared to the CVSGD. Both AVSOD and ACSOD achieve significant reduction in turn-on and turn-off delay times $T_{d(on/off)}$, turn-on and turn-off times $T_{on/off}$, as well as turn-on and turn-off switching energies $E_{on/off}$ compared to CVSGD with the used maximum over-drive parameters indicated by $V_{H/L}$ and I_M.

Table 4.1: Gate Driver Summary.
* Varying dv/dt during the turn-off causes a varying discharge current of the blocking diode, hence affecting DUT's di/dt. The MOSFET is in saturation region and v_{GS} goes below the Miller plateau, hence any change in applied gate driving voltage affects i_S [J1].
** Varying di/dt during the turn-on affects DUT dv/dt due to power loop stray inductance.

	CVSGD	CCSGD	ACSOD	AVSOD	VVSMGD
OD	$\times$	Y	Y	Y	$\times$
$T_{d(on)}$	P	Y^c	Y^c	Y^i	Y^i
$T_{d(off)}$	P	Y^c	Y^c	Y^i	Y^i
dv/dt_{on}	P	Y^c	Y^i	Y^i	$Y^i_{\downarrow}$
dv/dt_{off}	P	Y^c	Y^{c^*}	Y^{c^*}	$Y^{c^*}_{\downarrow}$
di/dt_{on}	P	Y^c	$Y^{c^{**}}$	$Y^{c^{**}}$	$Y^{c^{**}}_{\downarrow}$
di/dt_{off}	P	Y^c	Y^i	Y^i	$Y^i_{\downarrow}$
CL	$\times$	$\times$	$\times$	$\times$	Y

While they both achieve 55% reduction in E_{on}, ACSOD achieve higher reduction in $T_{d(on)}$ and T_{on} which can be attributed to the pre-charge current injected into the gate prior to turn-on, as explained in [J1], [R1]. While the ACSOD achieves higher $T_{d(off)}$ reduction, the difference is less than for turn-on, and the T_{off} reduction is higher using the AVSOD. Furthermore, AVSOD achieves higher E_{off} reduction than the ACSOD. This can be attributed to the following. Firstly, the pre-charge interval is less pronounced during turn-off. The gate-source pre-charged potential difference between $V_{GS}^{pre(off)}$ and V_H is a lower percentage of the potential difference between V_H and V_{th} at turn-off than the potential difference between the achieved $V_{GS}^{pre(on)}$ and V_L, and V_L and V_{th} at turn-on. Furthermore, the maximum over-drive value of the AVSOD voltage is a higher percentage increase for turn-off – from $V_L = -5V$ to $V_L = -24V$ ($\uparrow 380\%$) – than for turn-on – $V_H = 20V$ to $V_H = 40V$ ($\uparrow 100\%$) – further explaining the greater percentage reduction of E_{off} obtained with the AVSOD driver. While the increase in v_{DS} slew rate contributes significantly to the i_S overshoot at turn-on, the effect on increasing i_S slew rate on the v_{DS} overshoot at turn-off is less pronounced. However, significant overshoot in v_{DS} is observed in *turn-off* di/dt and *turn-off* di/dt *and* dv/dt mode of up to 40% [R1].

Table 4.2: Adaptive Over-driver Maximum Achieved Values.

	$\downarrow T_{d(on)}$	$\downarrow T_{on}$	$\downarrow E_{on}$	$\uparrow I_S^{OS}$
AVSOD$_{V_H=40V}$	40%	48%	55%	150%
ACSOD$_{I_M=16A}$	75%	65%	55%	150%
	$\downarrow T_{d(off)}$	$\downarrow T_{off}$	$\downarrow E_{off}$	$\uparrow V_{DS}^{OS}$
AVSOD$_{V_L=-24V}$	57%	55%	68%	10%
ACSOD$_{I_M=-16A}$	65%	50%	50%	15%

The ACSOD and AVSOD gate drivers are capable of significant reduction in switching parameters such as turn-on and turn-off delay times, turn-on and turn-off times and turn-on and turn-off energies through their over-drive capability. The ACSOD over-drive capability is available with CCSGD, hence the over-drive capability is available with a four-switch bridge topology. While the ACSOD uses an energy storing inductor with two voltage sources for controllability, the AVSOD use four voltage sources. Two driving voltage sources (V_H and V_L) are commonly available (e.g. R24P22005D dual output $+20/-5V$) as isolated power supplies. Adding two more voltages sources either requires circuitry to derive the voltages from V_H and V_L or an additional two-output power supply. This adds circuit complexity compared to the single inductor required for the ACSOD driver. However, the flexibility and capabilities of the AVSOD are superior to the ACSOD, as it allows for controlling the time instant and duration of the applied voltages, allowing for more complex control of the switching parameters and additional independent di/dt and dv/dt controllability. The current source gate driver can achieve additional di/dt and dv/dt control by employing the auxiliary circuit described in [J1], termed ACSOD driver with extended controllability (EACSOD). The EACSOD adds two additional inductors and an additional driver switch. It further requires an additional control signal, isolation and driver circuitry for the auxiliary switch, adding circuit complexity and control requirements.

The VVSMGD employs a four-switch bridge topology with an integrated synchronous buck converter [R1], where the circuit and control complexity of the additional buck adds to the four-switch topology. Even though only one extra driver signal is required for the buck – as the driver signal of the lower buck switch can be derived simply by inverting the upper switch signal – additional duty-cycle control requirements are demanded depending on how the buck voltage v_B is in-

tended to be used. The synchronous buck further requires its own LCR filtering. The VVSMGD have capabilities that the (E)ACSOD and AVSOD do not, that is, fine grained turn-off delay control and conduction loss manipulation ability. Even though not explored in [R1], the VVSMGD could include turn-on over-drive capability by having a high V_H voltage which can be applied similarly as with the AVSOD, and step this voltage down to the on-state operating voltage of the DUT using the buck converter. The on-state voltage of the DUT would then be v_B derived from V_H, which would then be within the voltage safety limits of the DUT gate.

Another version of a multi-level voltage source gate driver is co-authored in [O2]. Schematic detailing signal paths and isolation, discrete voltages supplies and the driver's discrete switches gate driving are given in Appendix B, together with a photograph of the respective adaptive gate driver PCB.

4.4 Conclusion

This chapter introduces three novel adaptive gate drivers. The extended adaptive current source over-driver (EACSOD) is capable of accurately controlling the gate current of high-voltage SiC MOSFETs. The gate current manipulation achieved enables independent control of turn-on and turn-off total switching and delay times, di/dt and dv/dt. The driver can provide reduced switching loss, shorter turn-on and turn-off delay times and shorter total turn-on and turn-off times compared to conventional voltage and current source gate drivers. Furthermore, the driver's ability to independently control di/dt and dv/dt is advantageous with respect to electromagnetic compatibility, the adaptive switching loss capability is advantageous for active thermal control and the adaptive turn-on and turn-off delay times is advantageous for dead-time critical power electronic systems, amongst others. From experiments on a 3.3kV/750A SiC MOSFET half-bridge power module, the driver have been tested in different operating modes. In adaptive turn-on operation, it has been shown that di/dt can be controlled in a range between $1.24A/ns$ to $4.5A/ns$, allowing turn-on switching energy reduction from $0.1183J$ to $0.0818J$ (30% decrease), respectively. Device dv/dt has been shown to be controllable independent from di/dt between $5.5V/ns$ to $9.5V/ns$ with $r_{g(ext)} = 1.5\Omega$ and $4.5V/ns$ to $7.5V/ns$ with $r_{g(ext)} = 4\Omega$. Furthermore, the ACSOD driver in over-drive mode achieved a maximum reduction of $50 - 55\%$ in E_{on}, a $60 - 65\%$ reduction in T_{on} and a $60 - 75\%$ reduction in $T_{d(on)}$, while a maximum $40 - 50\%$ reduction in E_{off}, a $45 - 50\%$ reduction in T_{off} and a $60 - 65\%$ reduction in $T_{d(off)}$ is achieved at turn-off for switching conditions $V_{BB} \in [600, 800]V$ and $I_L \in [300, 500]A$, compared to the CVSGD.

This chapter further presents two novel adaptive voltage source gate drivers, namely the adaptive voltage source over-driver (AVSOD) and the variable voltage source multi-level gate driver (VVSMGD). Their operating modes are verified experimentally on the FMF750DC-66A SiC MOSFET half-bridge power module using a double pulse test setup. The AVSOD is seen to be able to independently control the DUT's switching losses, turn-on/off time and turn-on/off delay times, as well as di/dt and dv/dt. The over-driving capability of the AVSOD achieved a $50-55\%$ reduction in E_{on}, a 48% reduction in T_{on} and a 40% reduction in $T_{d(on)}$ for turn-on using the over-drive mode with $V_{H1}=40V$, while a maximum $60-68\%$ reduction in E_{off}, a 55% reduction in T_{off} and a $53-57\%$ reduction in $T_{d(off)}$ is achieved at turn-off using the over-drive mode with $V_{L1}=-24V$ for switching conditions $V_{BB}\in[600,800]V$ and $I_L\in[300,500]A$, compared to the CVSGD. A total of 5 different adaptive gate driver modes – *full over-drive*, *delay control*, di/dt *control*, dv/dt *control* and di/dt *and* dv/dt *control* – are presented and experimentally verified for the AVSOD driver. The VVSMGD is shown to control turn-off delay times and consequently total turn-off switching times, turn-off v_{DS} and turn-on i_S overshoots (or equivalently turn-on dv/dt) of the switched DUT. It has been shown that the voltage overshoot on v_{DS} can be reduced by 44% and i_S overshoot by 73%, at the cost of increased switching energy. Furthermore, the frequency spectrum of the DUT waveforms is shown to be controllable, and by manipulating the duty-cycle of the integrated buck converter, the driver can accurately adjust the DUT conduction loss through the dynamic adjustment of $r_{DS(on)}$.

These results prove the applicability of the proposed adaptive gate drivers to power semiconductor devices requiring adaptive functionalities for improving electrical and thermal performance.

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Chapter 5

Applications of Real-time Models and Adaptive Gate Drivers

This chapter discusses combination possibilities of real-time models with adaptive gate drivers and possible applications for the proposed real-time simulation models and adaptive gate drivers.

5.1 Real-time Simulation with Adaptive Gate Drivers

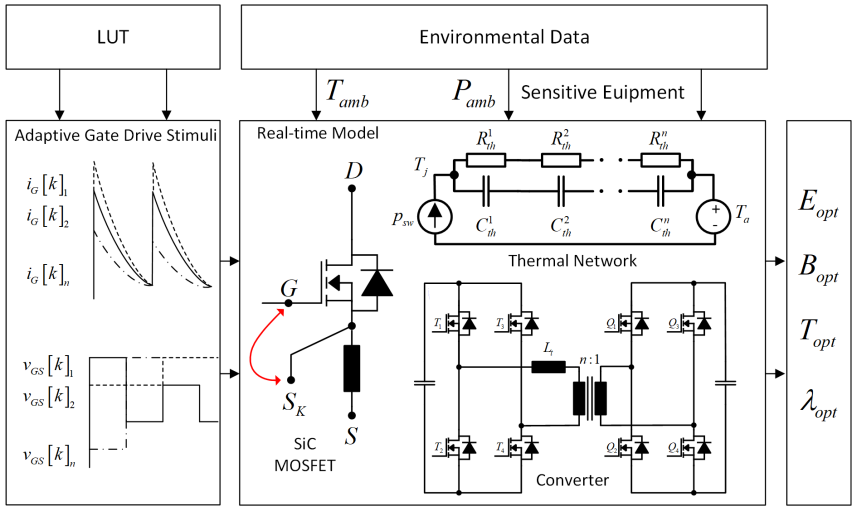
Different gate current or gate-source voltage waveforms can be programmed, either hard-coded waveforms in LUTs or by discretizing governing dynamic equations. For example, a set of i_G or v_{GS} – as defined by the adaptive gate driver (see chapter 4) – is provided as input to the discrete-time dynamic SiC MOSFET model in the given application (e.g. DAB [1]). Based on environmental inputs, e.g. ambient temperature T_{amb} and pressure P_{amb}, or sensitive equipment in close proximity, different adaptive gate drive stimuli can be inputted to the real-time model. Then, different device parameters – as discussed in chapter 4 – such as switching and conduction loss, electric E and magnetic B fields can be analysed, and an optimal operating point for e.g. the device or complete system lifetime can be assessed. Critical device parameters – from the temperature-dependent $r_{DS(on)}$ and aging effects to package stressors due to electric field concentration – can be included in the model, alongside the device model discussed in [J2], [J3], [C4]. This is illustrated in Figure 5.1. For example, a deep-sea remotely operated vehicle is tasked to change its course. Environmental data – such as water temperature and pressure or EMI sensitive equipment– can be sensed or received for the specific location or path the vehicle is planned to take. The real-time model can take the environmental data inputs, run a complete system real-time simulation with a set of

adaptive gate driver inputs, and arrive at an optimal gate drive operation for different parts of the mission path. Optimal system parameters – such as optimal electric E_{opt} and magnetic B_{opt} fields for sensitive surrounding equipment, optimal semiconductor parameters, passive components, controller and other ICs, temperature T_{opt} and lifetime λ_{opt} – can be evaluated based on different adaptive gate drive and environmental inputs.

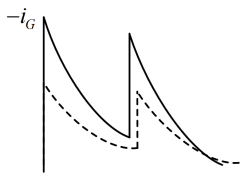
The power electronic real-time system can be utilized with RES integration in power grids, e.g. with day-ahead power forecasting models typically used with wind and PV energy generation. Considering for example PV energy generation, both physical deterministic plant models with expected weather conditions, or stochastic machine learning based methods based on historical power generation data, can be used as a source model for the system. Similar modelling can be applied to the load, for example EV charging or residential energy use. The real-time model can run different adaptive gate driver stimuli with source and load models adapted to the application intended, and arrive at optimal operating points for different times of the day.

5.2 Adaptive Gate Driver Applications

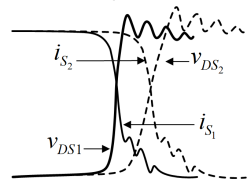
As discussed in subsection 3.3.1, the adaptive gate drivers can be used to achieve optimal performance of a power electronic system in real-time. An active slew rate control utilizing the presented adaptive gate drivers can, for example, be integrated with EV battery management systems (BMS), as Texas Instruments discuss in [2] using their *variable gate resistance* UCC5880-Q1 gate driver. Typical charge -and discharge-curves of lithium-ion battery cells depends on several operating condition. For example, both discharge rate and battery temperature severely affects the battery cell voltage with respect to remaining discharge capacity, as illustrated in Figure 5.2. A full cell voltage yields the maximum rated DC-link voltage powering the EV drive train, hence, if a CVSGD is used, the gate drive strength must be designed in a way to meet safety margins for device v_{DS} overshoots during switching action for full cell voltage. The drive resistance to the device gate must be chosen high enough to meet safety margins at full cell voltage, being higher than necessary at lower battery state of charge (SOC) where margins are higher. Thus, the resulting switching loss is higher than needed considering v_{DS} overshoots when battery SOC is 100%. Adaptive gate drivers can thus improve drive train efficiency – hence EV range, system operating condition range, reliability and longevity – by increasing di/dt and reducing p_{sw} at turn-off when v_{DS} margins allows for it, i.e. increasing di/dt when SOC reduce, improving efficiency. An adaptive switching and conduction loss optimization can be utilized considering environmental conditions. For example, a planned EV route speed limits, elev-



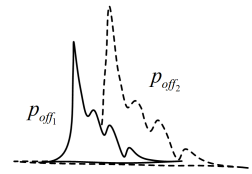
(a) Real-time model with with a set of adaptive gate drive stimuli stored in look-up tables (LUT). Sensed environmental parameters such as ambient temperature or pressure or information about EMI sensitive equipment can be inputted to the model and resulting optimal operating parameters based on some goal can be assessed.



(b) Different i_G stimuli (dotted vs. full) from the ACSOD (see 4.2.1.1).



(c) Different gate drive stimuli effect on turn-off v_{DS} and i_S.



(d) Different gate drive stimuli effect on turn-off switching losses p_{off}.

Figure 5.1: Real-time model of a complete power electronic system with different adaptive gate-driver stimuli.

ation and weather conditions can be analysed to estimate required motor torque and, hence the battery discharge rate and temperature during different parts of the route. Adaptive gate driving can then be used to provide optimal device driving considering some goal, e.g. battery lifetime. An example of voltage overshoot V_{DS}^{OS} - turn-off switching energy E_{off} control using the VVSMGD single pulse, variable v_B control mode is shown in Figure 4.13 [R1].

Other application examples includes combined power and data transfer using adaptive gate drivers. Superimposing high-frequency data transfer and power transfer are used in power electronic systems [3, 4, 5], and can reduce overhead cost, system reliability and flexibility. Utilizing adaptive gate driving in this process

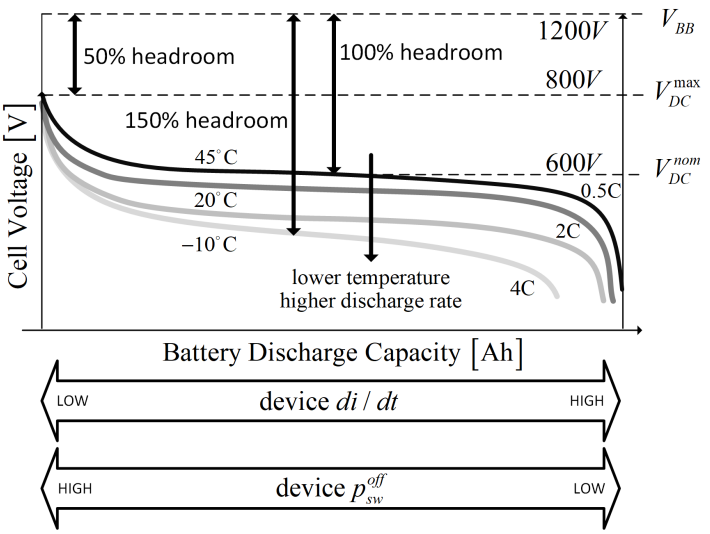
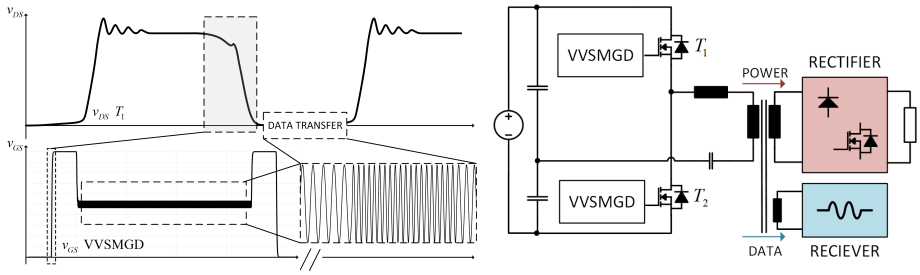


Figure 5.2: Battery cell voltage vs. discharge curves for different temperatures and discharge rates (C-rates).

can simplify the data transfer process and combine several features alongside data transfer – such as active device power loss and voltage overshoot control – as discussed earlier. The VVSMGD ability to manipulate v_{GS} through use of a the high-bandwidth synchronous buck converter allows it to generate a high frequency voltage v_B. This can for example be used in to generate radio frequency communication waveforms in the device's v_{GS}. Through the v_{GS} dependent $r_{DS(on)}$, data can be coded into the $v_{DS} = r_{DS(on)}(v_{GS}) \cdot i_S$ and transferred through some media to a receiver, as conceptually illustrated in Figure 5.3.

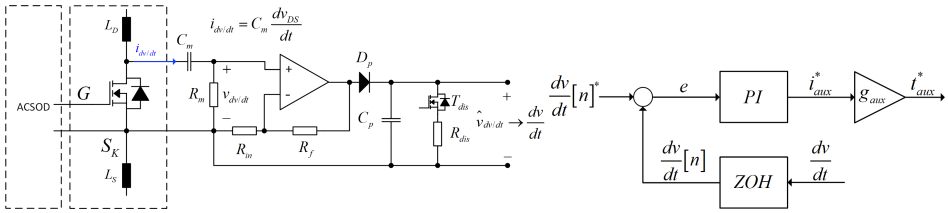
Closed loop control of switching loss, dv/dt or di/dt is possible by employing measurements of driven device dv/dt and/or di/dt. The closed loop control allows for real-time control of mentioned parameters and can adapt the DUT parameters to a specific application. An example of a closed-loop dv/dt control scheme is illustrated in Figure 5.4, with a dv/dt measurement circuit illustrated in Figure 5.4(a) and the dv/dt closed loop block diagram illustrated in Figure 5.4(b). A simulation of the closed loop dv/dt control operation in MATLAB Simulink® is depicted in Figure 5.5. A step command in desired device dv/dt during turn-off is provided to a PI-controller, as seen in Figure 5.5(a). Here, the step command $dv/dt[n]^*$ is colored in blue, while the sampled measured $dv/dt[n]$ is colored in red. The error (Figure 5.5(b)) via the PI-controller provides the command i^*_{aux} for ACSOD second current sinking, and through the gain g_{aux}, a charging time and sinking time are generated. The auxiliary current is sinked as seen in Fig-



(a) Radio frequency data transfer using the VVSMGD during device on-time.

(b) DC-DC power converter using the VVSMGD with separate data and power transfer.

Figure 5.3: Combined power and data transfer concept.

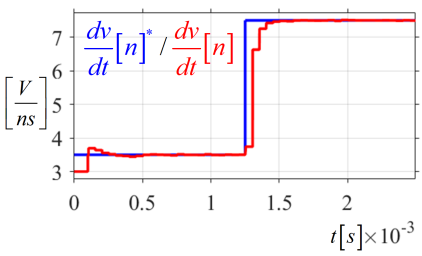


(a) dv/dt measurement circuit schematic.

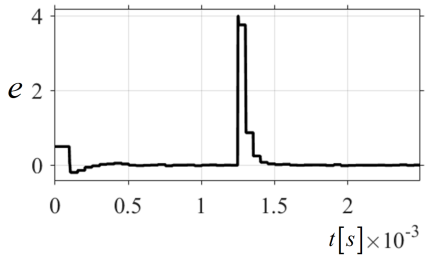
(b) Block diagram.

Figure 5.4: Closed loop dv/dt control.

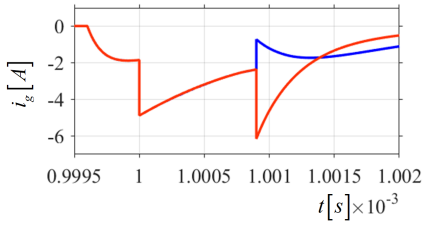
ure 5.5(c) which manipulates the device dv/dt as seen in Figure 5.5(d), with resulting changes in device switching loss p_{sw} and average switching energy E_{sw} as seen in Figure 5.5(e) and Figure 5.5(f).



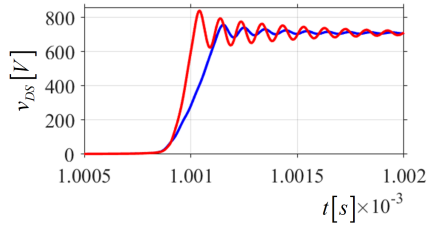
(a) dv/dt command (blue), measured dv/dt (red).



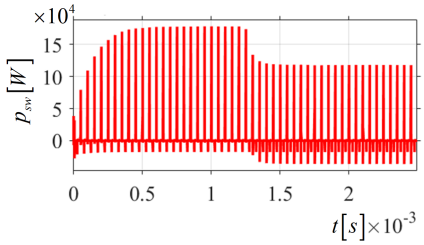
(b) dv/dt control error.



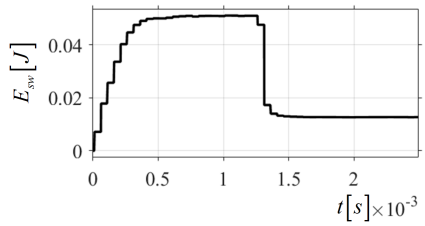
(c) ACSOD gate current i_g. Low dv/dt (blue) and high dv/dt (red).



(d) Device v_{DS}. Low dv/dt (blue) and high dv/dt (red).



(e) Device switching loss p_{sw}.



(f) Average device switching energy E_{sw}.

Figure 5.5: Simulation waveforms of ACSOD closed loop operation for controlling dv/dt during SiC MOSFET turn-off.

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Chapter 6

Conclusions

This PhD thesis have proposed a real-time modelling approach and adaptive gate drivers for high-power SiC MOSFETs. A procedure for an accurate real-time dynamic switching model and how key device characteristics, such as the equivalent device capacitances and threshold voltage hysteresis, impact the trajectory of drain-source voltage, gate-source voltage and source current of the device have been investigated in depth. It is shown that in-depth device characteristic measurements – such as voltage dependent capacitances obtain from power device analyser – are integral to achieve high modelling accuracy of the turn-on and -off switching transient of high-voltage, high-current SiC MOSFET half bridge modules with different ratings. A discrete-time version of the dynamic model is presented and it has shown that the dynamic switching model can be implemented on the FPGA of SOM devices and run in real-time. The switching waveforms obtained using this model show very good accuracy when compared to real experimental waveforms measured on a DPT setup. The proposed model was utilized to assess the design and operation of a high-power DAB converter, as well as to identify critical design and operating parameters of this converter, such as the turn-on and turn-off switching energies and maximum switching frequency. Such models are important in assessing converter design aspect such as deadtime, switching frequency, system power density and thermal management, and hence important for an optimal converter design.

This PhD thesis also proposed three novel adaptive gate driver topologies which are able to manipulate device performance in real-time. A novel adaptive current source gate driver capable of adaptively control the gate current – and hence the switching transients – of high-voltage SiC MOSFETs is proposed. Two configurations – the conventional current source over-driver (CCSGD) and the cur-

rent source over-driver capable of extended adaptive operation (EACSOD) – are presented. The gate current manipulation of the novel EACSOD enables independent control of turn-on and turn-off delay times, di/dt and dv/dt. The driver can provide reduced switching loss, shorter turn-on and turn-off delay times and shorter total turn-on and turn-off times compared to conventional voltage and current source gate drivers. Furthermore, the EACSOD ability to independently control di/dt and dv/dt is advantageous with respect to controlling electromagnetic compatibility, the adaptive switching loss capability is advantageous for active thermal control and the adaptive turn-on and turn-off delay times is advantageous for dead-time critical power electronic systems, amongst others. Furthermore, two adaptive voltage source gate drivers, namely the adaptive voltage source over-driver (AVSOD) and the variable voltage source multi-level gate driver (VVSMGD) have been developed. The concept of gate over-driving is introduced and the over-driving capabilities of the AVSOD are compared with an adaptive current source over-driver based on a full-bridge driver topology. The presented AVSOD is able to independently control the DUT's switching losses, turn-on/off time and turn-on/off delay times, as well as di/dt and dv/dt. The presented VVSMGD has shown to control turn-off delay times and consequently turn-off times, turn-off v_{DS} overshoots and turn-on i_S overshoots of the switched DUT. Its conduction loss manipulation feature opens possibilities with respect to active thermal control and gate driver data transfer. The conduction loss manipulation concept can be integrated into the other presented gate driver concepts, hence allowing for adaptive gate driver concept capable of accurate switching loss, switching times and conduction loss manipulation. By combining the adaptive gate drivers with real-time models, one can arrive at optimal system operation with respect to for example device temperature or EMI.

6.1 Suggestions for Future Work

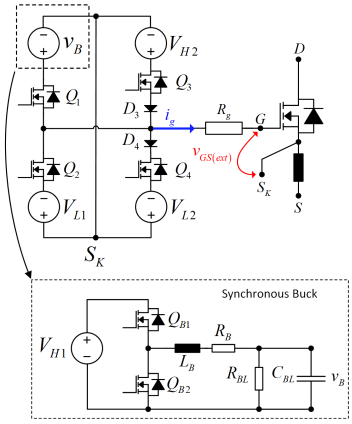
Several aspects of the presented work are subject to further research. The presented real-time simulation models should be verified on more devices. This could verify the model's applicability across different manufacturers, device ratings and device types. This could also build a library of device characteristics, such as voltage and frequency dependent capacitances, available for power electronic system designers. Similar research should be performed with different topologies and in different environments – e.g. different temperature and pressure conditions – to investigate model accuracy and applicability across applications.

Such research should also be performed with the presented adaptive gate drivers. They should be tested on more devices to gauge their applicability and performance in different applications. Important aspects such as cost, complexity and ro-

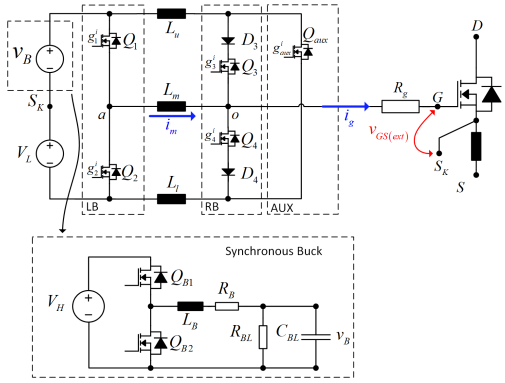
bustness are valuable topics for further investigations. Aspects such as switching loss, switching times and conduction loss should be investigated in greater detail to indicate their relevance for different applications. The presented application areas – such as adaptive gate drivers integration in battery management systems and gate driver data transfer – are interesting application areas to investigate further.

The adaptive gate driver's current and voltage patterns can be implemented as driving sources of the SiC MOSFET real-time model, as discussed in section 5.1. The power electronic system can run on different adaptive gate driver stimuli and optimal system operation can assessed based on environmental data, load and source profiles.

The ACSOD and AVSOD can be modified to include the variable voltage source v_B of the VVSMGD, as illustrated in Figure 6.1. Including the synchronous buck variable voltage source v_B in one of the bridge legs in the AVSOD – as illustrated in Figure 6.1(a) – yields an additional, controllable voltage to be applied to the gate during switching transients. The voltage v_B further allows the AVSOD and ACSOD to manipulate the conduction loss during switch on-state. Other modifications to the adaptive gate drivers can be investigated, such as the use of GaN devices instead of Si MOSFETs as the gate driver switches to potentially reduce gate driver losses.



(a) AVSOD with extended adaptability.



(b) ACSOD with extended adaptability.

Figure 6.1: Schematic diagrams of AVSOD and ACSOD with variable voltage source v_B.

Appendices

Appendix A

Collection of Articles

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Rødal, Gard Lyng; Peftitsis, Dimosthenis. An Adaptive Current-Source Gate Driver for High-Voltage SiC mosfets. IEEE transactions on power electronics 2023 ;Volum 38.(2) s. 1732-1746 https://doi.org/10.1109/TPEL.2022.3208827

Rødal, Gard Lyng; Peftitsis, Dimosthenis. Real-Time FPGA Simulation of High-Voltage Silicon Carbide MOSFETs. IEEE transactions on power electronics 2023 ;Volum 38.(3) s. 3213-3234 https://doi.org/10.1109/TPEL.2022.3223951

Rødal, Gard Lyng; Vivekanandham Pushpalatha, Yoganandam; Philipps, Daniel Alexander; Peftitsis, Dimosthenis. Capacitance Variations and Gate Voltage Hysteresis Effects on the Turn-On Switching Transients Modelling of High-Voltage SiC MOSFETs. IEEE transactions on power electronics 2023 ;Volum 38.(5) s. 6128-6142 https://doi.org/10.1109/TPEL.2023.3243951

Rødal, Gard Lyng; Peftitsis, Dimosthenis. Real-Time FPGA Simulation of Silicon Carbide MOSFETs. IEEE 8th Workshop on Wide Bandgap Power Devices and Applications (WiPDA)

This article is accepted and published
Gate-Drive Circuits for Adaptive Operation of SiC MOSFETs. IEEE transactions on power electronics 2024, Volume: 39, Issue: 7
https://doi.org/10.1109/TPEL.2024.3382335

Gate-Drive Circuits for Adaptive Operation of High-voltage SiC MOSFETs

Gard Lyng Rødal, *Student Member, IEEE,* and Dimosthenis Peftitsis, *Senior Member, IEEE*

***Abstract*—This paper proposes and compares three adaptive gate-drive circuits for Silicon Carbide (SiC) metal oxide semiconductor field-effect transistors (MOSFETs). The concept of adaptive over-driving is presented. A novel adaptive voltage source gate driver that enables over-driving operation and capable of independently controlling turn-on and turn-off delay times, switching times and switching energy, as well as device dv/dt and di/dt is presented. The voltage source over-driver is compared to a second driver, that is, the conventional adaptive current source over-drive concept. This driver is capable of adaptively control turn-on and turn-off delay times, switching times and switching energy. Furthermore, a novel variable-voltage source multi-level gate driver with integrated synchronous buck converter is presented. This driver is capable of adaptively manipulating turn-off delay times, turn-off times and switching energy, device voltage and current overshoots, voltage and current harmonic spectrum during switching transients. Furthermore, this driver is capable of adjusting the conduction loss of the MOSFET by manipulating the on-state resistance through the gate-source voltage. The presented gate drivers are experimentally validated on a 3.3 kV/750 A high-power SiC MOSFET power module.**

***Index Terms*—Adaptive gate driver, SiC MOSFET, Switching transient**

I. Introduction

Silicon carbide (SiC) metal-oxide semiconductor field-effect transistors (MOSFETs) are becoming the most attractive wide-bandgap (WBG) semiconductor technology to replace silicon (Si) based insulated-gate bipolar transistors (IGBTs) commonly deployed in high-voltage high-current power electronics systems. Even though high-voltage $(> 3.3kV)$ SiC MOSFETs are yet to reach the market, the available devices $(\leq 3.3kV)$ are considered as potential replacements of the well established Si IGBTs in applications such as medium-voltage (MV) drives and medium- and high-voltage (HV) direct-current (DC) grids [1]–[9].

Gate drivers are the key components to exploit the fast-switching capabilities of SiC MOSFETs and ensure safe operation when employed in power electronic converters. Adapting the conventional totem-pole voltage source gate driver (CVSGD) technology used for Si IGBTs, poses limitation in exploiting the fast-switching characteristics of SiC MOSFETs. Even though fast switching unlocks the utilization of higher switching frequencies, it causes overvoltages (i.e., due to high di/dt) that might be severe for the safe operation of SiC MOSFETs. Besides, reducing deadtimes in half-bridge circuits necessitates the minimization of turn-on and turn-off delay times. Therefore, the drive circuits for SiC MOSFETs should not only perform optimal turn-on and turn-off transients, but also ensure safe operation of the devices. These challenges become more prominent under varying load current and blocking voltage conditions, where optimal tuning of the gate-drive circuits for various operating points is not possible. A solution to this, is the utilisation of adaptive gate drivers which are able to continuously optimise their operation based on the loading conditions.

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Adaptive gate drivers are able to manipulate the movement of gate charge in a more flexible way than the CVSGDs, both during the switching transients and during conduction phase. Adaptability during the switching transient allows for both manipulation of the switching loss and switching time parameters. The switching loss can either be minimized to optimize efficiency or adapted in a way to minimize device junction temperature variations and thus improving reliability. The turn-on and turn-off delay times can be manipulated to accommodate optimal system deadtime conditions, as well as device di/dt and dv/dt control for complying with electromagnetic interference requirements. Furthermore, by adjusting the on-state gate driver voltage supply values, $v_{GS} = V_H$, the device on-state drain-source resistance, $r_{DS(on)}(v_{GS})$, can be manipulated.

Adaptive current-source gate drivers (ACSGD) are implemented either as inductor-less or inductor-based topologies. The *inductor-less* ACSGDs are typically current-mirror based circuit topologies [10]–[14]. On the other hand, inductor-based ACSGDs utilize a single or multiple inductors as an energy storing element in the gate driving circuitry. The inductor-based ACSGDs can be categorized into continuous (CCS) and discontinuous (DCS) current source drivers [15], depending on whether the current through the driver inductor is continuous or discontinuous. The CCS typically needs a larger inductor value and higher driver losses than the DCS for the same gate drive current [15], [16]. On the other hand, DCS typically have a circuit topology with higher component count, with more drive switches and higher control complexity. For CCS-based ACSGDs, the drive circuit is typically implemented as a full-bridge type [17]–[23] used in synchronous converter applications for driving both converter switches. Amongst the ACSGDs with DCS, the driver circuit is typically implemented as a full-bridge type [24]–[31], a half-bridge type [32]–[34] or a half-bridge type hybrid circuit with additional blocking switches and resonance circuitry [35]–[38]. An ACSGD capable of multi-functional switching transient adaptability has been proposed by the authors in [39], [40]. This driver

is capable of independently control the device's turn-on/off delays, as well as di/dt and dv/dt. In all these ACSGD concepts, the peak value of the gate current is always kept lower than the critical value which excites oscillations in the gate loop [40]. However, allowing the gate current to exceed the oscillation-excited current and by well-controlling this value, speeding-up the switching transients becomes possible. The first contribution of this paper is the design and operation of a traditional ACSGD in over-driving mode for improving switching speed of SiC MOSFETs. The term over-driving refers to the supply of a gate current that is significantly higher than the corresponding gate current using a CVSGD.

The second family of adaptive gate drivers, namely adaptive voltage source gate drivers, can control the gate current either by adjusting the voltage source supply level or the impedance seen by the gate path. Variable impedance drivers are most commonly implemented as variable gate resistance or variable input capacitance circuits [41]. Variable resistance drivers [42]–[46] simply vary the applied gate resistance seen by the device, thus enabling control of the gate current and consequently the device switching transient. Variable capacitance drivers regulate the switching transients by controlling the input capacitance C_{iss}, for example by controlling the Miller capacitance C_{gd} [47] or the gate-source capacitance C_{gs} [48].

Variable voltage source drivers are commonly implemented as multi-level voltage source circuits [49]–[56] or two-level circuits with voltage level controllability, e.g. using a buck converter [57]. By adjusting the gate-source voltage, v_{GS}, level prior to the switching transient, the turn-on and turn-off delays can be controlled. Besides, by adjusting the value of v_{GS} during the switching transients, switching parameters such as di/dt, dv/dt, total switching time, as well as v_{DS} and i_D overshoot values can be controlled. However, none of these gate driver concepts has explored the possibility for slightly over-driving the gate in order to achieve faster switching performance. Besides, the combination of over-driving features with adaptive functionalities for manipulating switching parameters has not been studied either. Finally, none of the presented gate drivers are capable of adjusting switching and conduction power losses simultaneously.

The second contribution of this paper is the development of a voltage source gate driver with over-driving functionality, for improving the switching performance of SiC MOSFETs. Finally, the third contribution of the paper is a novel variable voltage source multi-level gate driver that incorporates a synchronous DC/DC buck converter for online adjustment of switching and conducting characteristics of SiC MOSFETs. An extensive theoretical and experimental performance evaluation of the three gate driver concepts is shown in the paper.

The paper is organized as follows. Section II presents the switching characteristics of SiC MOSFETs and the limitations using CVSGDs. Section III shows the design and operation of adaptive over-drivers, while in Section IV the proposed variable-source, multilevel gate driver is presented. A thorough experimental validation of the gate drivers is shown in Section V. Discussion of the findings is included in Section VI and the conclusions are drawn in Section VII.

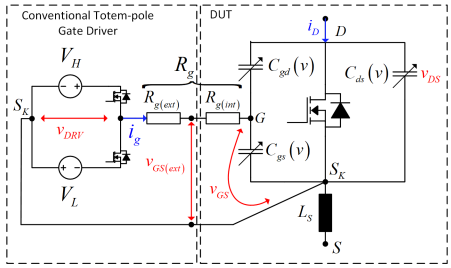


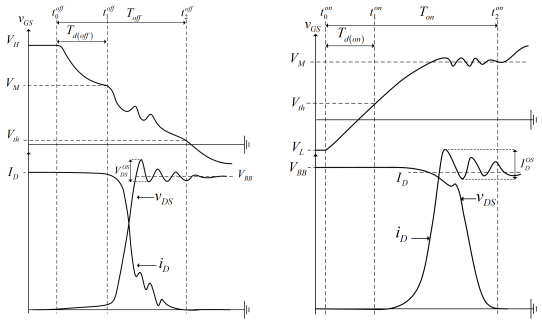
Fig. 1. Circuit schematic of the totem-pole based CVSGD connected to the equivalent SiC MOSFET circuit.

II. Switching Characteristics of SiC MOSFETs and Performance Limitations using the CVSGD

The schematic diagram of a CVSGD is shown in Fig. 1. The CVSGD supplies the driving voltage, v_{DRV} that can switch between a positive, V_H, and a negative value, V_L. The gate current is governed by the values of V_H and V_L, as well as by the value of the resistance, R_g in the gate path.

Theoretical switching waveforms are shown in Fig. 2 and the parameters depicted are determined as follows. The turn-on time $T_{on} = t_2^{on} - t_0^{on}$ is defined as the time duration from the time instant that the gate drive voltage v_{DRV} changes from the off-state voltage level V_L until the device has reached linear region, i.e. $v_{DS} \leq (v_{GS} - V_{th})$. The turn-on delay time $T_{d(on)} = t_1^{on} - t_0^{on}$ is defined as the time duration from the time point when v_{DRV} changes from V_L until the device starts conducting (i.e. $v_{GS} > V_{th}$ and $i_D > 0$). The turn-on switching energy E_{on} is the switching energy incurred by the device from the time instant that i_D starts rising until $v_{DS} \leq (v_{GS} - V_{th})$:

$$E_{on} = \int_{t_1^{on}}^{t_2^{on}} i_D \cdot v_{DS}\, dt \tag{1}$$



(a) Theoretical turn-off waveforms. (b) Theoretical turn-on waveforms. .

Fig. 2. Theoretical switching waveforms of SiC MOSFETs.

Similarly, for turn-off, the turn-off time $T_{off} = t_2^{off} - t_0^{off}$ is the time duration from when v_{DRV} changes from the positive driver supply level V_H until $v_{GS} \leq V_{th}$. Finally, the turn-off delay time $T_{d(off)} = t_2^{off} - t_0^{off}$ is defined as the time duration from the time instant that v_{DRV} changes from V_H until the device reaches the saturation region (i.e., $v_{DS} \geq (v_{GS} - V_{th})$. The turn-off switching energy is thus defined as

$$E_{off} = \int_{t_1^{off}}^{t_2^{off}} i_D \cdot v_{DS}\, dt \tag{2}$$

The drain current i_D can be approximated in the saturation region (i.e. for $v_{DS} \geq (v_{GS} - V_{th})/P_{vf}$ while $v_{GS} \geq V_{th}$, where P_{vf} is a parameter defining the sharpness of transition between ohmic and saturation region) considering its transfer characteristics as [58], [59]

$$i_D \approx g_s(v_{GS} - V_{th})^x(1 + \lambda v_{DS}) \tag{3}$$

where g_s is the MOSFET's transconductance, x is a fitting parameter to be adjusted to the specific device used and λ is the channel modulation index, with the value of v_{DS} being the device's blocking voltage.

The manipulation of *switching loss* is limited when using CVSGDs, as they have limited design parameters available for shaping the switching transients. The values for the positive and negative driver supplies, V_H and V_L, are limited by the voltage rating of the gate $[V_{GS}^{max}, V_{GS}^{min}]$, which are usually in the range of $[20\,V, -20\,V]$ for SiC MOSFETs. The lower value of R_g is generally limited by the device's internal resistance $R_{g(int)}$. For a CVSGD, the gate current i_g is given by

$$i_g = \frac{(V_{HL} - v_{GS})}{R_g} = \frac{V_{HL}}{R_g} e^{-t/\tau_{iss}} \tag{4}$$

where $R_g = R_{g(ext)} + R_{g(int)}$, $V_{HL} = V_H - V_L$, $C_{iss} = C_{gs} + C_{gd}$ and $\tau_{iss} = C_{iss}R_g$. The time duration of which the CVSGD can move the amount of charge Q_{g_1} is given by

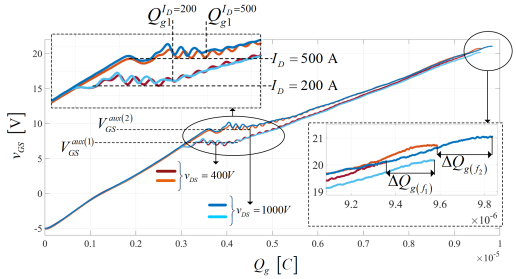
$$T_{g_1} = -\tau_{iss} \cdot \ln\left(\frac{Q_{g_1}}{C_{iss}V_{HL}}\right) \tag{5}$$

Considering the turn-on process, the device is considered turned on when the output capacitance $C_{oss} = C_{gd} + C_{ds}$ is discharged. That is, when Q_{g_1} has been moved from the driver to the gate at the given device operating point, as seen in Fig. 3a. Thus, the only configurable design parameters available for the CVSGD is the V_H/V_L values and R_g.

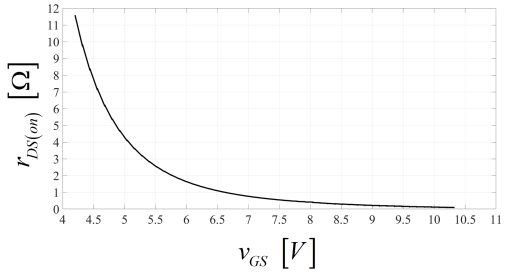
As seen in Fig. 3b, the on-state resistance of SiC MOSFETs, $r_{DS(on)}$, is dependent on the value of v_{GS}. Adjusting the value of v_{GS} allows for conduction loss

$$p_{cond} = r_{DS(on)}(v_{GS}) \cdot i_D^2 \tag{6}$$

manipulation during operation in power converters in order to, for example, achieve active thermal control.



(a) The FMF750DC-66A $Q_g(v_{GS})$ characteristics.



(b) $r_{DS(on)}$ vs. v_{GS}. Measured $r_{DS(on)}$ on-state v_{GS} dependency of the FMF750DC-66A.

Fig. 3. (a) Gate charge (b) and on-state drain-source resistance on-state gate-source voltage dependency of the Mitsubishi FMF750DC-66A SiC MOSFET half-bridge power module used as device under test (DUT) using the B1505A Power Device Analyser.

III. Adaptive Over-Drivers

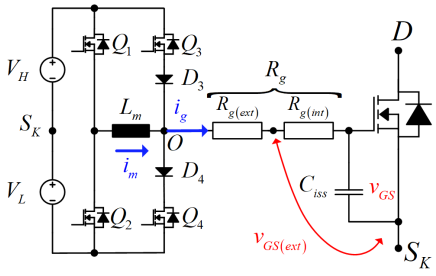
This section introduces a class of adaptive gate drivers termed *over-drivers*. They are defined as adaptive gate drivers capable of supplying a higher peak current I_g than the corresponding gate current using the CVSGD, i.e.

$$I_g = \frac{V_{HL}}{R_g} \tag{7}$$

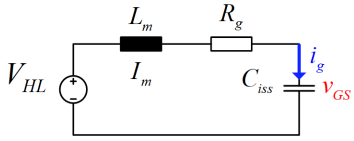
Two ways of achieving over-drive capabilities are discussed in the following. One over-driving principle is based on a current source topology and presented in subsection III-A, while a novel over-driver based on a voltage source topology is presented in subsection III-B.

A. Adaptive Current Source Over-Driver

The circuit schematic of the adaptive current-source over-driver (ACSOD) is shown in Fig. 4a with its equivalent RLC-circuit illustrated in Fig. 4b. The driver topology utilizes 4 discrete switches $(Q_1 - Q_4)$ configured in a full-bridge with an energy storing inductor, L_m. This type of full-bridge inductor-based current source gate driver is utilized in [17]–[22], [24]–[26], [29], [30] for high switching frequency operation of synchronous converter topologies, and in [27], [28], [31], [60] for individual-switch driving. The operating principle of the ACSOD is based on charging L_m to a peak current I_m via

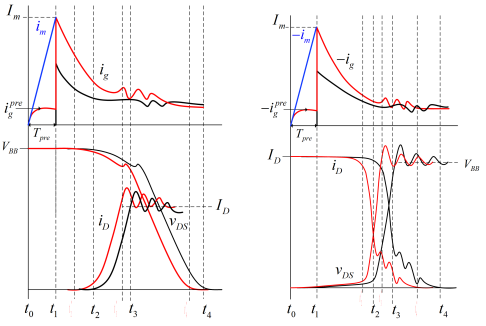


(a) ACSOD circuit schematic.



(b) ACSOD equivalent RLC-circuit schematic.

Fig. 4. The adaptive current source over-driver (ACSOD).



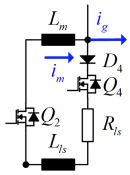
(a) ACSOD turn-on transition. (b) ACSOD turn-off transition.

Fig. 5. ACSOD theoretical switching waveforms (red) and CVSGD theoretical switching waveforms (black).

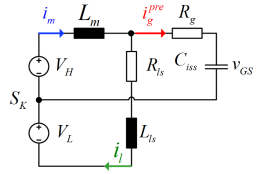
the voltage sources V_H and V_L. The charged current i_m is then injected into the gate at turn-on and sunk from the gate at turn-off process. By adjusting the magnitude I_m, the switching energies E_{on}/E_{off} and switching times can be controlled.

The procedure for the turn-on transition is illustrated with the red waveforms in Fig. 5a and for the turn-off in Fig. 5b.

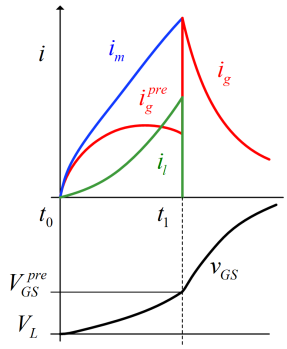
1) Pre-charge Interval: The ACSOD operation is initiated by the pre-charge interval. At turn-on, the current i_m is charged to an amplitude of I_m by V_{HL} through L_m, by turning Q_1 and Q_4 on for the time duration $T_{pre} = t_1 - t_0$, as seen in Fig. 5a. Due to on-state resistance of the discrete switches $(Q_1 - Q_4)$ and blocking diodes (D_3/D_4), R_{ls} comprising the driver and a stray inductance L_{ls} in the lower path between Q_2 and Q_4, a current divider is formed between the path through $R_g \rightarrow C_{iss} \rightarrow V_L$ and the path through $Q_4 \rightarrow V_L$, as illustrated in Fig. 6a-6b. Thus, a current, i_g^{pre} flows into the gate between t_0 and t_1, as illustrated theoretically in Fig.



(a) Lower part of the ACSOD circuit during pre-charge interval.



(b) Equivalent circuit during pre-charge interval.



(c) Current waveforms during pre-charge interval

Fig. 6. Pre-charge interval.

6c and measured as seen in Fig. 7. This current charges the gate-source voltage, v_{GS}, to a pre-charge value V_{GS}^{pre}. An in-depth explanation and mathematical derivation of the pre-charge interval is given in [40].

2) Turn-on: The inductor current i_m having an amplitude I_m is then injected into the gate at the time instant t_1 by turning Q_4 off while keeping Q_1 on, realising the equivalent circuit illustrated in Fig. 4b.

3) Turn-off: For the turn-off process, the current i_m is similarly charged to an amplitude of I_m by turning Q_2 and Q_3 on at the time point t_0 and keeping them on for a time interval T_{pre}. The inductor current i_m with the amplitude I_m is then sunk from the gate at t_1 by turning Q_3 off while keeping Q_2 on. Similarly as for the turn-on, a pre-charge current $-i_g^{pre}$ is sunk from the gate during the T_{pre} interval at turn-off, causing v_{GS} to slightly decrease below V_H prior to the turn-off instant t_1.

4) ACSOD Design: The energy storing element, L_m, yields significant benefits in terms of switching speed flexibility. Considering the equivalent RLC circuit of the ACSOD given in Fig. 4b and using Kirchhoff's laws, the evolution of v_{GS} can be described by the following differential equation

$$\frac{d^2 v_{GS}}{dt^2} + \frac{R_g}{L_m}\frac{dv_{GS}}{dt} + \frac{v_{GS}}{C_{iss}L_m} = \frac{V_{HL}}{C_{iss}L_m} \tag{8}$$

Equation "(8)" is written in the Laplace domain as

$$v_{GS}(s)\left(s^2+2\alpha_s s+\omega_{0_s}^2\right)= \left(\frac{V_H\omega_{0_s}^2}{s}+sV_L+\frac{I_m}{C_{iss}}+\frac{R_g}{L_m}V_L\right) \qquad (9)$$
$$\alpha_s=\frac{R_g}{2L_m},\ \omega_{0_s}^2=\frac{1}{C_{iss}L_m}$$

A critically damped response yields the fastest response in v_{GS} to stimuli from i_g. Thus, the damping of the RLC equivalent circuit must be $\zeta_s=\alpha_s/\omega_{0_s}=1$, and L_m then be chosen as

$$L_m=C_{iss}\left(\frac{R_g}{2}\right)^2 \qquad (10)$$

for a given C_{iss} and R_g to preserve a damping of 1. With the response of v_{GS} being critically damped, $v_{GS}(s)$ have a single pole $s_s=-\alpha_s$, and the time response of $v_{GS}(t)$ is described as

$$v_{GS}=V_H+\underbrace{e^{-\alpha_s t}}_{e(t)}\cdot\underbrace{(k_{s_1}^v t+k_{s_2}^v)}_{l(t)} \qquad (11)$$
$$k_{s_1}^v=\frac{I_m}{C_{iss}}+\alpha_s k_{s_2}^v,\ k_{s_2}^v=-V_{HL}$$

and the gate current i_g given by

$$i_g=C_{iss}\frac{dv_{GS}}{dt}=C_{iss}e^{-\alpha_s t}\cdot(k_{s_1}^i t+k_{s_2}^i) \qquad (12)$$
$$k_{s_1}^i=-\alpha_s k_{s_1}^v,\ k_{s_2}^i=k_{s_1}^v-\alpha_s k_{s_2}^v$$

Even though the response of v_{GS} is critically damped, the evolution of $v_{GS}(t)$ may still overshoot the voltage source value of V_H if the energy stored in L_m at the turn-on instant is greater than the energy capacity of C_{iss}. Thus, overshoot in v_{GS}, i.e. $v_{GS}(t)>V_H,\ t\geq t_1$, occurs if the magnetic field energy E_L of L_m is greater than the electric field energy capacity E_C of the C_{iss}, according to the following criterion:

$$E_L=\frac{L_m I_m^2}{2}>E_C=\frac{C_{iss}V_{HL}^2}{2} \qquad (13)$$

For a value of I_m greater than the overshoot value I_m^{OS}, v_{GS} overshoots, hence the peak pre-charge value I_m of i_m should not exceed I_m^{OS}

$$I_m^{OS}=V_{HL}\sqrt{\frac{C_{iss}}{L_m}} \qquad (14)$$

The overshoot is visualized in Fig. 7, where the ACSOD is tested on a capacitive passive load C_L in the same range as the input capacitance of the 3.3 kV/750 A SiC MOSFET power module (Mitsubishi FMF750DC-66A) that is used for the experimental validation in this paper. The parameters of the driver for the passive test are summarized in Table I. As seen in Fig. 7, for values of $I_m>I_m^{OS}$, an overshoot occurs in v_{GS}.

The energy dissipation of the gate driver is given by

TABLE I
ACSOD PASSIVE LOAD TEST PARAMETERS

$V_H[V]$	$V_L[V]$	$C_L[nF]$	R_g	$L_m[\mu H]$	$I_m^{OS}[A]$
20	-5	300	3.7	~ 1	13.5

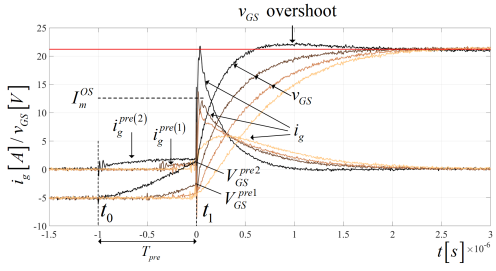


Fig. 7. Gate current i_g and gate-source voltage v_{GS} waveforms showing effect of $I_m>I_m^{OS}$.

$$E_D=\int_0^\infty R_g i_g^2 dt \qquad (15)$$

The energy dissipation of the gate driver's total gate resistance R_g is the major contributor of the driver's overall energy use, as compared to the efficiency of driver's on-board DC/DC converters and other ICs such as signal isolators and discrete switch drivers, both in active and quiescent state. The ideal energy dissipation of the CVSGD is constant and given by

$$E_D^V=0.5C_{iss}V_{HL}^2 \qquad (16)$$

with "(4)" used in "(15)". The energy dissipation of the ACSOD depends on the value of I_m as given in "(12)". Similarly, by using "(12)" in "(15)" with the condition $I_m=I_m^{OS}$ yielding $k_{s_1}^1=0$ and $\alpha_s=2/(R_gC_{iss})$ for $\zeta_s=1$, the energy dissipation of the ACSOD is given by

$$E_D^{C(max)}=\frac{\alpha_s R_g(V_{HL}C_{iss})^2}{2}=C_{iss}V_{HL}^2=2E_D^V \qquad (17)$$

Therefore, using the maximum I_m given by "(14)" with the ACSOD results in twice the energy dissipation compared to the CVSGD. This is illustrated in Fig. 8, where the energy use of the ACSOD driver is compared to that of the CVSGD for different values of R_g and I_m. The red line marks the I_m^{OS} boundary for a critically damped driver, where I_m values larger than I_m^{OS} yields v_{GS} overshoot for the given R_g.

A comparison of estimated v_{GS} rise times during the turn-on between the CVSGD and the ACSOD, that is v_{GS} traversing from the off-state voltage level $v_{GS}=-5V$ to an approximation of the Miller plateau voltage (i.e. an estimation of the turn-on time) is provided in [40], for different values of I_m and R_g. A higher I_m results in faster v_{GS} rise times at the cost of higher gate driver energy use.

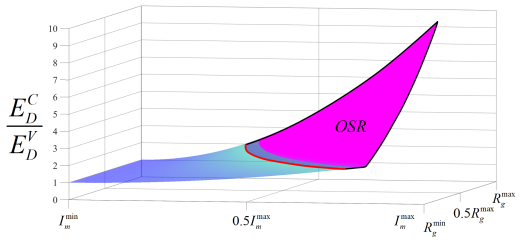
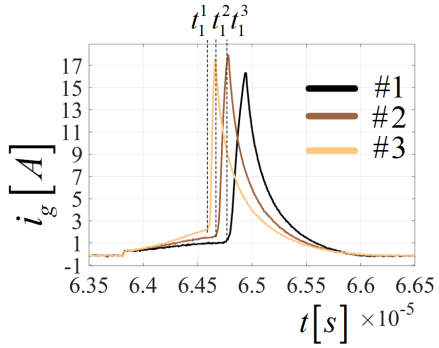
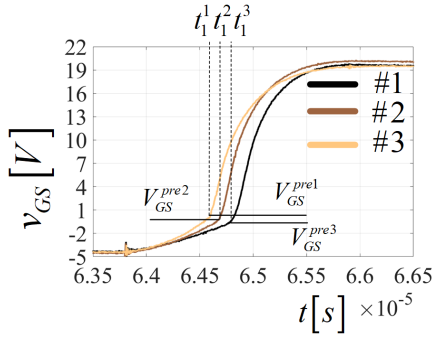


Fig. 8. Gate driver energy comparison of the ACSOD E_D^C and CVSGD E_D^V. The boundary of I_m^{OS} is marked with the red line.



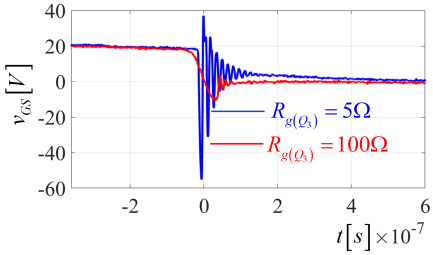
(a) i_g.



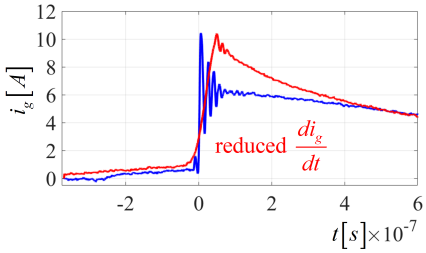
(b) v_{GS}.

Fig. 9. Comparing i_g and v_{GS} waveforms of the ACSOD driver using the 3 discrete gate driver MOSFET switches of Table II. Test performed on a passive load C_L similar to the C_{iss} of the FMF750DC-66A DUT.

5) Practical ACSOD Design Considerations: The effect of R_{ls} on the pre-charge current i_g^{pre} can be adjusted by the proper choice of the discrete switches $(Q_1 - Q_4)$ that is of low-voltage Silicon MOSFET type. Choosing components for a gate driver (and general power electronic systems) is generally a compromise between price, size, thermal requirements and device characteristics. A comparison between 3 discrete low-voltage Silicon MOSFET switches with different electrical



(a) v_{GS} comparing $R_{g(Q_3)} = 5\Omega$ to $R_{g(Q_3)} = 100\Omega$.



(b) i_g comparing $R_{g(Q_3)} = 5\Omega$ to $R_{g(Q_3)} = 100\Omega$.

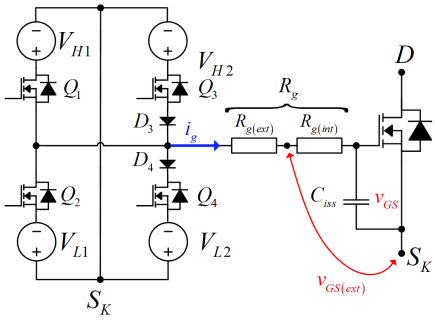
Fig. 10. Effect of increased v_{GS} comparing $R_{g(Q_3)}$ on di_g/dt and gate oscillations.

TABLE II
GATE DRIVER DISCRETE SWITCH RATED PARAMETERS

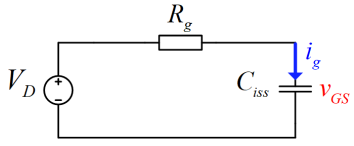
#	Device	V_{BB}	$r_{DS(on)}$	C_{oss}	Package
1	DMN4060SVT	60 V	46 $m\Omega$	57 pF	TSOT-26-6
2	DMN10H170SVT	100 V	115 $m\Omega$	36 pF	TSOT-26-6
3	DMN10H220LVT	100 V	250 $m\Omega$	22 pF	TSOT-26-6

characteristics is given in Table II. The i_g and v_{gs} responses by employing these 3 MOSFET types in the ACSOD gate driver are shown in Fig. 9. It can be seen that the choice of discrete driver switches impacts the response of the driver, and consequently the response of the driven device i_g and v_{GS}. Their varying values of the device equivalent capacitances impact the di/dt and dv/dt values of the discrete switches – and consequently the slew rate of i_g and v_{GS} – while their $r_{DS(on)}$ impacts the pre-charge current flowing into the gate prior to turn-on and the obtained maximum value I_m, as described in [40].

The gate resistors of $Q_1 - Q_4$, $R_{g(Q_{1-4})}$ also impact the di/dt and dv/dt of the discrete driver switches. A low $R_{g(Q_{1-4})}$ results in a high di/dt and dv/dt, which impact the response of v_{GS} and i_g to the applied i_m. Considering the turn-off instant at t_1 when i_g is sunk from the gate, the discrete driver switch Q_3 is turned off while Q_2 is on, forcing i_g to be sunk from the driver as L_m resists its change in current. Due to unavoidable stray inductances L_{GS} in the PCB tracks between the node O and S_K, the value of di/dt of the current though



(a) AVSOD circuit schematic.



(b) AVSOD equivalent RLC-circuit schematic.

Fig. 11. The adaptive voltage source over-driver (AVSOD).

switch Q_3 directly determines the di/dt of the sunk i_g. The interaction between the rapidly changing i_g and L_{gs} causes voltage transients and oscillations in v_{GS}. This is seen in Fig. 10 where a simple turn-off instant is performed with different $R_{g(Q_3)}$ values. Increased $R_{g(Q_3)}$ reduces switch di/dt, hence reducing oscillations and voltage overshoots in v_{GS}.

B. Adaptive Voltage Source Over-Driver

This section presents a novel adaptive voltage source over-driving circuit concept (AVSOD). The circuit schematic of the AVSOD is shown in Fig. 11a with its equivalent RLC-circuit illustrated in Fig. 11b. The voltage sources V_{H1} and V_{H2} are used for turn-on, while the voltage sources V_{L1} and V_{L2} are used for the turn-off process. For the configuration presented in this paper, the voltages V_{H1} and V_{L1} are used as over-drive voltages, i.e. $V_{H1} > V_{H2}$ and $V_{L1} > V_{L2}$, while V_{H2} and V_{L2} are kept at a fixed level corresponding to conventional V_H and V_L driving levels. By controlling the switches Q_1 and Q_3, the voltage V_D in Fig. 11b, takes either the value of V_{H1} or V_{H2} at turn-on, while it either takes the voltage V_{L1} or V_{L2} at turn-off. Depending on when the voltage source is applied to the gate during the switching transients, different switching properties can be achieved, as is explained below.

1) Turn-on Modes: The driver's operation for the different main modes during turn-on switching transients is presented in the following subsections. It should be specified that the driver can operate in different ways and versions of the 5 presented modes, e.g. i_D overshoot reduction or frequency spectrum control (as it will be shown for the VVSMGD in Section IV).

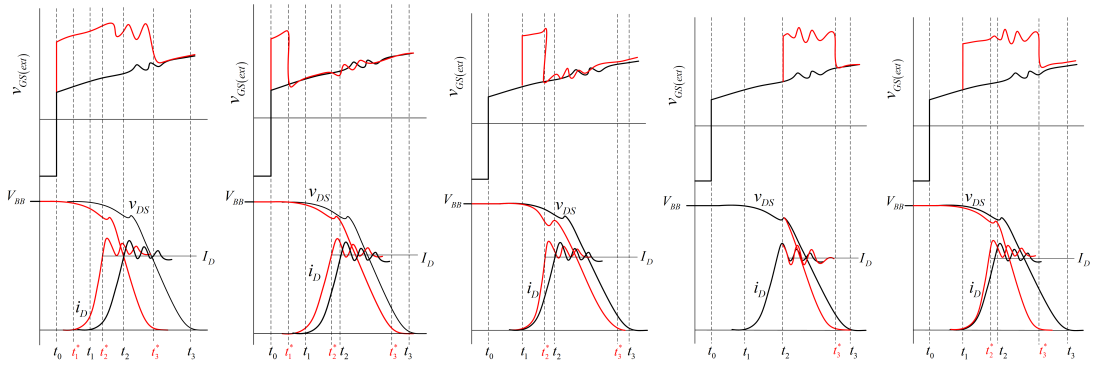
a) Turn-on Full Over-Drive Mode: The overall turn-on time T_{on} and turn-on switching energy E_{on} can be controlled by applying the turn-on full over-drive mode. As illustrated in Fig. 12a, by applying V_{H1} with a higher voltage level than V_H, T_{on} can be reduced. The full over-drive mode is initiated by applying the voltage source V_{H1} to the gate at the time instant t_0 by turning Q_1 on, while turning Q_4 off. At the time instant t_3^*, the voltage level V_{H2} is applied to the gate by turning Q_3 on while turning Q_1 off, removing V_{H1} from the gate. This results in the reduced turn-on time $T_{on}^* = t_3^* - t_0$, as well as reduced turn-on delay time $T_{d(on)}$ and switching energy, E_{on}.

b) Turn-on Delay Control Mode: The turn-on delay time $T_{d(on)}$ can be manipulated by applying the voltage source V_{H1} in the time-range $[t_0^{on}, t_1^{on}]$ (see Fig. 2b). As illustrated in Fig. 12b, by applying V_{H1} with a higher voltage level than V_H, $T_{d(on)}$ can be reduced. Assuming the device is in the off-state, the turn-on delay control mode is initiated by applying the voltage source V_{H1} to the gate at time instant t_0 by turning Q_1 on, while turning Q_4 off. At time instant t_1^*, the voltage level V_{H2} is applied to the gate by turning Q_3 on while turning Q_1 off, removing V_{H1} from the gate. This results in the reduced turn-on delay time $T_{d(on)}^* = t_1^* - t_0$, as well as reduced T_{on} and E_{on}.

c) Turn-on di/dt Control Mode: The device di/dt can be controlled with the turn-on di/dt control mode. By applying V_{H1} with a higher voltage level than V_H during i_D rise time, di/dt can increase, without significantly affecting the device dv/dt, as illustrated in Fig. 12c. The turn-on is initiated by turning Q_3 on while turning Q_4 off, applying V_{H2} to the gate. The mode is initiated by applying the voltage source V_{H1} to the gate at time instant t_1 by turning Q_1 on, while turning Q_3 off. At time instant t_2^*, the voltage level V_{H2} is again applied to the gate by turning Q_3 on while turning Q_1 off, removing V_{H1} from the gate. Thus, the device's di/dt increases, while dv/dt is the same. This operating mode will also reduce T_{on} and E_{on}.

d) Turn-on dv/dt Control Mode Mode: The device dv/dt can be controlled with the turn-on dv/dt control mode. By applying V_{H1} with a higher voltage level than V_H during v_{DS} fall time after i_D has reached the load current value I_D, the $|dv/dt|$ can increase, as illustrated in Fig. 12d. The turn-on is initiated by turning Q_3 on while turning Q_4 off, applying V_{H2} to the gate. This mode is initiated by applying the voltage source V_{H1} to the gate at t_2 by turning Q_1 on, while turning Q_3 off. At t_3^*, the voltage level V_{H2} is applied to the gate by turning Q_3 on again while turning Q_1 off, removing V_{H1} from the gate. Therefore, $|dv/dt|$ can increase, while keeping di/dt the same. This mode will reduce T_{on} and E_{on}.

e) Turn-on di/dt and dv/dt Control Mode: The device di/dt and dv/dt can be controlled with the turn-on di/dt and dv/dt control mode. If V_{H1} with a higher voltage level than V_H is applied during i_D rise time and v_{DS} fall time, di/dt and $|dv/dt|$ can increase, as depicted in Fig. 12e. The turn-on is initiated by turning Q_3 on while turning Q_4 off, applying V_{H2} to the gate. The mode is initiated by applying the voltage source V_{H1} to the gate at t_1 by turning Q_1 on, while turning Q_3 off. At t_3^*, the voltage level V_{H2} is applied to the gate by turning Q_3 on while turning Q_1 off, removing V_{H1} from the



(a) Turn-on full over-drive mode theoretical waveforms. (b) Turn-on delay control mode theoretical waveforms. (c) Turn-on di/dt control mode theoretical waveforms (d) Turn-on dv/dt control mode theoretical waveforms. (e) Turn-on di/dt and dv/dt control mode theoretical waveforms.

Fig. 12. The adaptive voltage source over-driver (AVSOD) 5 key operation modes theoretical waveforms during turn-on transition.

gate. This results in increased device di/dt and $|dv/dt|$ while maintaining $T_{d(on)}$. This mode will also reduce T_{on} and E_{on}.

2) Turn-off Modes: The driver operation for the different operating modes during turn-off switching transients is presented in the following subsections.

a) Turn-off Full Over-drive Mode: The overall turn-off time T_{off} and turn-off switching energy E_{off} can be controlled by applying the turn-off full over-drive mode. As illustrated in Fig. 13a, by applying V_{L1} with a lower voltage level than V_L, T_{off} can be reduced. The full over-drive mode is initiated by applying the voltage source V_{L1} to the gate at t_0 by turning Q_2 on, while turning Q_3 off. At t_3^*, the voltage level V_{L2} is applied to the gate by turning Q_4 on while turning Q_2 off, removing V_{HL1} from the gate. This results in the reduced turn-on time $T_{off}^* = t_3^* - t_0$, as well as reduced $T_{d(off)}$ and E_{off}.

b) Turn-off Delay Mode: The turn-off delay time $T_{d(off)}$ can be manipulated by applying the voltage source V_{L1} in the time-range $[t_0^{off}, t_1^{off}]$ (see Fig. 2a). As illustrated in Fig. 13b, by applying V_{L1} with a lower voltage level than V_L, $T_{d(off)}$ can decrease. Assuming the device is in the on-state, the turn-off delay control mode is initiated by applying V_{L1} to the gate at t_0 by turning Q_2 on, while turning Q_3 off. At t_1^*, V_{L2} is applied to the gate by turning Q_4 on and Q_2 off, removing V_{L1} from the gate. This results in the reduced turn-off delay time $T_{d(off)}^* = t_1^* - t_0$, as well as reduced T_{off} and E_{off}.

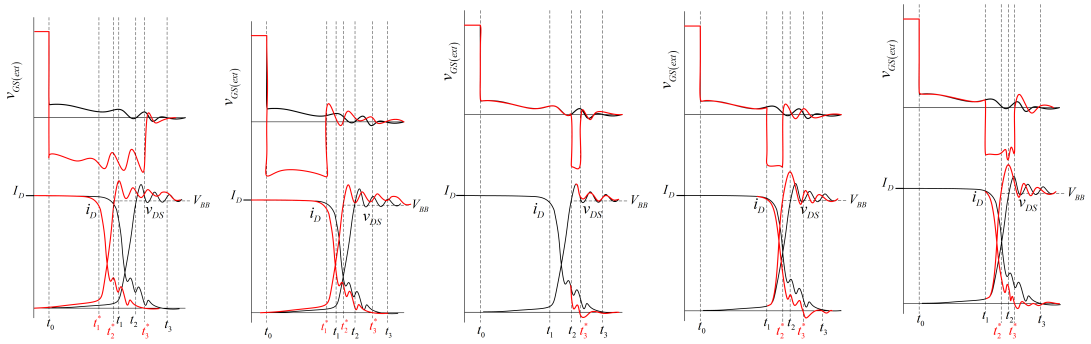
c) Turn-off di/dt Control Mode: The device di/dt can be controlled during turn-off with the turn-off di/d control mode. If $V_{L1} < V_L$ is applied during i_D fall time, $|di/dt|$ can increase, without affecting the device dv/dt, as illustrated in Fig. 13c. At t_0, V_{L2} is applied to the gate by turning Q_4 on while turning Q_3 off, initiating the turn-off transient. The mode is initiated by applying V_{L1} to the gate at t_2 by turning Q_2 on and Q_4 off. At t_3^*, V_{L2} is again applied to the gate by turning Q_4 on while turning Q_2 off, removing V_{L1} from the gate. Thus, $|di/dt|$ can increase while dv/dt is kept the same. This mode will also reduce T_{off} and E_{off}.

d) Turn-off dv/dt Control Mode Mode: The device's dv/dt can be controlled with the turn-off dv/dt control mode. By applying V_{L1} during v_{DS} rise time, dv/dt can increase, as illustrated in Fig. 13d. The turn-off transient is initiated at t_0 by turning Q_4 on and Q_3 off, applying V_{L2} to the gate. At t_1, V_{L1} is supplied to the gate by turning Q_2 on and Q_4 off, removing V_{L2} from the gate. V_{L2} is again applied to the gate at t_3^*, removing V_{L1} from the gate, by turning Q_4 on and Q_2 off. This results in increased device $|dv/dt|$, and as a result, increased di/dt. This mode will reduce T_{off} and E_{off}.

e) Turn-off di/dt and dv/dt Control Mode: The device's di/dt and dv/dt can be controlled with the turn-off di/dt and dv/dt control mode. By applying V_{L1} during v_{DS} rise time and i_D fall time, $|di/dt|$ and dv/dt can increase, as illustrated in Fig. 13e. The turn-off is initiated by turning Q_4 on while turning Q_3 off, applying V_{L2} to the gate. The mode is initiated by applying V_{L1} to the gate at t_1 by turning Q_2 on and Q_4 off. At t_3^*, V_{L2} is applied to the gate by turning Q_4 on while turning Q_2 off, removing V_{L1} from the gate. This results in increased device dv/dt and $|di/dt|$ while keeping $T_{d(off)}$ the same. This mode will reduce T_{off} and E_{off}.

IV. Variable Voltage Source Multi-Level Gate Driver

This section presents a novel voltage source gate driver topology with variable voltage source and multi-level voltage level driving capabilities. The variable voltage source multi-level gate driver (VVSMGD) circuit schematic is shown in Fig. 14 and it is based on the circuit topology introduced by Zhao et al. [55], [56], [61]. The driver utilises three voltage sources $V_H > v_B > V_L$ where the fixed voltage V_H is the highest voltage level, v_B is the variable middle voltage and derived from V_H and the fixed V_L is the lowest off-state voltage level. The voltage sources provide the gate



(a) Turn-off full over-drive mode theoretical waveforms. (b) Turn-off delay control mode theoretical waveforms. (c) Turn-off di/dt control mode theoretical waveforms (d) Turn-off dv/dt control mode theoretical waveforms. (e) Turn-off di/dt and dv/dt control mode theoretical waveforms.

Fig. 13. The adaptive voltage source over-driver (AVSOD) 5 key operation modes theoretical waveforms during turn-off transition.

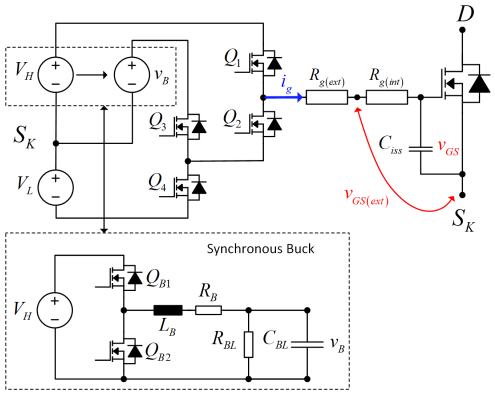


Fig. 14. The variable voltage source multi-level gate driver (VVSMGD) circuit schematic showing the 4-switched $Q_1 - Q_4$ driver circuit with the integrated synchronous buck converter with the switches Q_{B1} and Q_{B1}.

current i_g to the MOSFET gate through the gate resistors $R_g = R_{g(ext)} + R_{g(int)}$. The multi-level driving capability is achieved by the two half-bridge circuits comprising Q_1/Q_2 and Q_3/Q_4 and by introducing a buck converter in the circuit, the variable mid-level voltage is achieved. The voltage v_B is controlled by adjusting the duty-cycle d of the buck converter, as seen in Fig. 15.

The VVSMGD has several operating modes which can be used separately or together and they are described in the following subsections.

A. Turn-off Delay Manipulation

The device turn-off delay time $T_{d(off)}$ can be manipulated by providing the variable voltage source v_B to the gate prior to the actual turn-off instant, as illustrated in Fig. 16a. By adjusting the duty-cycle d of the buck converter, v_B can be set to a pre-defined voltage level $v_B = V_{GS}^{pre}$. Turning Q_2 and Q_3 on at t_B^{off}, applies v_B to the gate to adjust the turn-off delay time and turn-off time of the DUT. The turn-off transition is then initiated by turning Q_3 off at $t_0^{off^*}$, while turning Q_4 on, applying V_L to the gate. Thus, $T_{d(off)}$ and T_{off} can be adjusted depending on the value V_{GS}^{pre}.

B. Turn-off Voltage Overshoot Manipulation

By controlling v_{GS} during v_{DS} overshooting oscillatory behaviour, the magnitude of the overshoot V_{DS}^{OS} and frequency spectrum of the oscillations can be manipulated. Due to the falling i_D and the unavoidable parasitic inductance L_{eq} of the power module layout and power circuit loop, the anticipated voltage overshoot approximately equals to

$$V_{DS}^{OS} = L_{eq}\frac{di_D}{dt} \tag{18}$$

By manipulating v_{GS} while the MOSFET is in the saturation region, the slope of i_D can be adjusted (as seen from "(3)"). Thus, the overshoot and oscillatory behaviour of v_{DS} can be controlled, as illustrated in Fig. 16b.

C. Turn-on Current Overshoot Manipulation

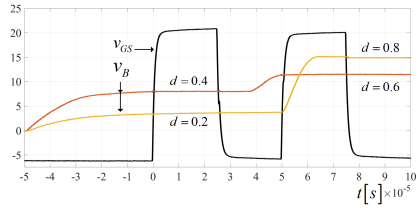
Similarly to the turn-off voltage overshoot manipulation, by controlling v_{GS} during i_D peak time (i.e. when v_{GS} reaching the Miller plateau and v_{DS} is falling) the i_D peak value can be manipulated as illustrated in Fig. 16c.

D. Conduction Loss Manipulation

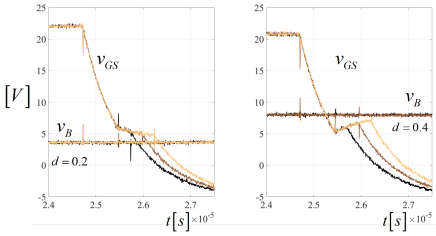
By manipulating v_{GS} during DUT conduction, the value of the drain-source on-state resistance $r_{DS(on)}$ can be adjusted, based on the $r_{DS(on)} - (v_{GS})$ plot shown in Fig. 3b. Thus, the drain-source voltage $v_{DS(on)} = r_{DS(on)} \cdot i_D$ is controllable and consequently the instantaneous conduction loss

$$p_{cond} = v_{DS(on)} \cdot i_D \tag{19}$$

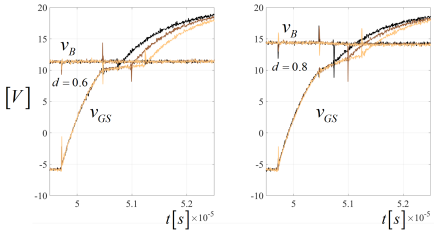
can also be adjusted.



(a) Double pulse testing of the VVSMGD on a passive load with duty cycle d changes.



(b) Turn-off test with $d = 0.2$ and $d = 0.4$ with different t_n^{vos} timing values.



(c) Turn-on test with $d = 0.6$ and $d = 0.8$ with different t_n^{ios} timing values.

Fig. 15. VVSMGD test on passive RC-load.

TABLE III
DOUBLE PULSE TEST CIRCUIT PARAMETERS

L_D	L_S	L_{up}	L_{low}	L_{LOAD}	C_f	C_{DS}
$7nH$	$7nH$	$20nH$	$20nH$	$80\mu H$	$10\mu F$	$800\mu F$

By applying v_B to the gate during conduction phase and adjusting v_B, p_{cond} can be controlled. The driver switches Q_2 and Q_3 are turned on while Q_1 and Q_4 are turned off, and by adjusting the buck converter duty-cycle d, $p_{cond}(d)$ can be controlled to a desired value.

V. EXPERIMENTAL RESULTS

The performance of the proposed adaptive gate drivers was experimentally validated on a double-pulse test (DPT) circuit as illustrated in Fig. 17a with a photo of the experimental setup shown in Fig. 17b. The setup employs a high-voltage 3.3 kV, 750 A SiC MOSFET half-bridge power module (Mitsubishi FMF750DC-66A) connected to an inductive load.

TABLE IV
MEASUREMENT EQUIPMENT

Scope	Tektronix MSO 5104	$f_{bw} = 1GHz, 10GS/s.$
Voltage Probe v_{DS}	Tektronix P5100A	$f_{bw} = 500MHz$
Voltage Probe $v_{GS(ext)}$	Tektronix TPP0500B	$f_{bw} = 500MHz$
Current Probe i_D	PEM CWTUM	$f_{bw} = 30MHz$

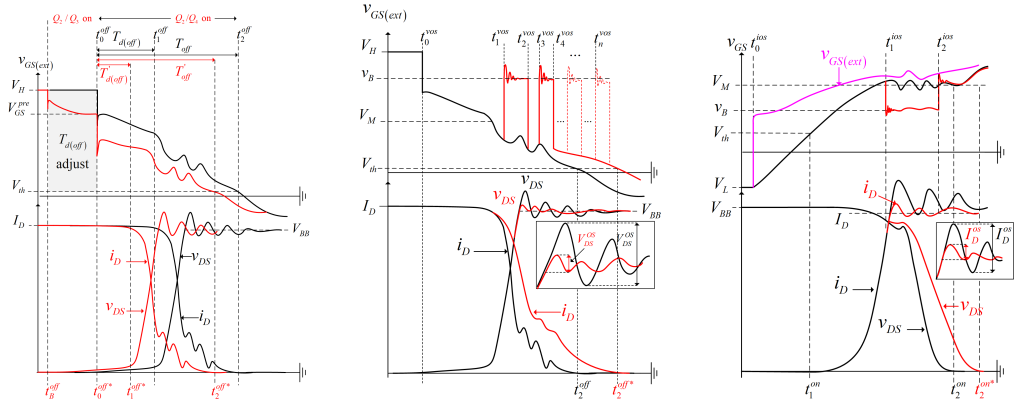
TABLE V
TURN-ON AND TURN-OFF EXPERIMENTAL DATA USING THE ACSOD FOR $I_D = 300A$ AND $V_{BB} = 800V$.

	I_m	5	7.5	10	12.5	16
$T_{d(on)}$	val $[ns]$	330	280	230	190	130
	% ↓	2.94	17.64	32.59	44.11	61.76
T_{on}	val $[ns]$	850	750	670	560	360
	% ↓	2.29	12.64	22.98	35.63	58.62
E_{on}	val $[mJ]$	47.9	45.7	42.5	37.3	24.1
	% ↓	1.23	5.77	12.37	23.09	50.31
$E_{D(on)}$	val $[\mu J]$	76.1	83.8	93.1	105.9	136.6
	% ↑	−1	9.0	21.1	37.7	77.6
$T_{d(off)}$	val $[ns]$	870	795	705	595	345
	% ↓	3.33	11.67	21.7	33.89	61.67
T_{off}	val $[ns]$	1403	1313	1211	1097	812
	% ↓	11.2	16.89	23.35	30.56	48.60
E_{off}	val $[mJ]$	25.62	22.42	21.91	20.9	15.63
	% ↓	4.22	16.19	18.13	21.86	41.57
$E_{D(off)}$	val $[\mu J]$	111.2	117.6	125.8	136.2	165.0
	% ↑	0.7	6.5	13.9	23.4	49.5

The electrical parameters of the DPT are listed in Table III, while Table IV summarizes the measurement equipment used during testing. The PicoZed 7030 (xc7z30sbg485-1) SOM's FPGA is used for the controller and adaptive driver signals generation. The FPGA has a maximum clock frequency of $f_{clk} = 250MHz$ yielding a minimum signal pulse-width of $4\ ns$.

A. Adaptive Current Source Over-Driver

A photograph of the printed circuit board (PCB) shown in Fig. 18. Experimental results of the ACSOD (section III-A) for varying pre-charged peak current ($I_m = 6 - 16A$) are shown in Fig. 19 for the turn-on transient and in Fig. 20 for the turn-off transient. For both cases, the maximum value of the pre-charged current i_m amplitude $I_{m(max)}$ is estimated by "(14)". The lowest testing I_m current corresponds to the gate current that would be supplied in case of a CVSGD. From these measurements, it is observed that by varying I_m, the turn-on and turn-off delay times, as well as turn-on and turn-off switching energies can be manipulated. Table V presents the numerical results of these three parameters for the experimental results shown in these two figures. From this table, it is observed that a reduction of 61.76% in $T_{d(on)}$



(a) Turn-off delay manipulation theoretical waveforms.

(b) Turn-off voltage overshoot manipulation and frequency spectrum control theoretical waveforms.

(c) Turn-on current overshoot and frequency spectrum manipulation theoretical waveforms.

Fig. 16. Theoretical waveforms of the variable voltage source multi-level gate driver (VVSMGD) shown in red color and compared to theoretical waveforms using the CVSGD (black lines).

is achieved for a peak I_m of 16 A. Similarly, the turn-on time, T_{on} is reduced by 58.62% and the switching energy by 50.31%. The corresponding decrease for turn-off transients are 61.67%, 48.6% and 41.57%. It should be noted that the percentage reduction values are compared to CVSGD with $R_{g(ext)} = 1.2\Omega$.

B. Adaptive Voltage Source Over-Driver

The PCB of the AVSOD is shown in Fig. 21. Experimental results of the turn-on and turn-off switching transients are presented in the following subsections.

1) Turn-on Full Over-Drive Mode: Experimental results of the AVSOD showing the turn-on full over-drive mode (section III-B1a) under various values of V_{H1} are shown in Fig. 22. Key performance data of the AVSOD for this mode of operation have been extracted from the experimental measurements and are presented in Table VI. It is observed that by increasing V_{H1} to 40 V, the turn-on delay time, $T_{d(on)}$ can be reduced by 41%, the turn-on time, T_{on} by 46% and turn-on energy, E_{on} by 50%.

2) Turn-on Delay Control Mode: Experimental results of the AVSOD showing the turn-on delay control mode (section III-B1b) for different values of V_{H1} are illustrated in Figs. 23a-23b, while Table VII summarizes key data extracted from the measurements. It can be seen that for $V_{H1} = 40V$, $T_{d(on)}$ can be reduced by 41%, whereas the reduction of T_{on} is lower compared to mode 1 of the AVSOD.

3) Turn-on di/dt Control Mode: Experimental results of the AVSOD showing the turn-on di/dt control mode (section III-B1c) for various values of V_{H1} are shown in Figs. 23c-23d. Table VIII summarizes key experimental data of di/dt and E_{on} control as V_{H1} varies. From these plots, it is seen that dv/dt is approximately constant and equals $dv/dt \approx 5.5\ V/ns$ across all V_{H1} levels, while di/dt can be adjusted in a range between 23% to 93% and E_{on} up to 33%.

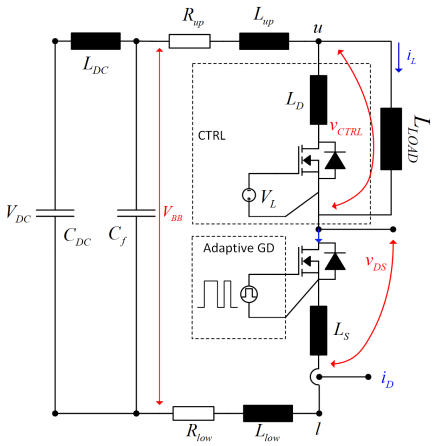
4) Turn-on dv/dt Control Mode: Figs. 23e-23f illustrate experimental results of the turn-on dv/dt control mode (section III-B1d) using the AVSOD, where as shown in Table IX dv/dt can vary up to 57% when $V_{H1} = 40V$. Using this mode

TABLE VI
TURN-ON EXPERIMENTAL DATA USING THE AVSOD IN FULL OVER-DRIVE MODE FOR $I_D = 300A$ AND $V_{BB} = 800V$.

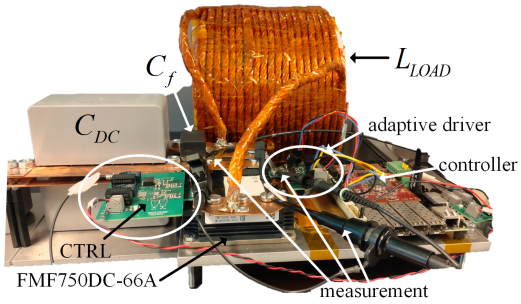
	$V_{H1}[V]$	20	25	30	35	40
$T_{d(on)}$	val $[ns]$	340	320	270	230	200
	% ↓		5.88	20.58	32.35	41.17
T_{on}	val $[ns]$	870	810	660	550	470
	% ↓		6.89	24.13	36.78	45.97
E_{on}	val $[mJ]$	48.5	44.6	34.6	28.5	24.2
	% ↓		8.04	28.65	41.23	50.10
$E_{D(on)}$	val $[\mu J]$	76.9	87.3	107.1	124.8	143.0
	% ↑		13.5	37.3	62.3	86.0

TABLE VII
TURN-ON DELAY CONTROL EXPERIMENTAL DATA USING THE AVSOD FOR $I_D = 300A$ AND $V_{BB} = 800V$.

	$V_{H1}[V]$	20	25	30	35	40
$T_{d(on)}$	val $[ns]$	340	320	270	230	200
	% ↓		5.88	20.58	32.35	41.17
T_{on}	val $[ns]$	870	850	780	740	710
	% ↓		2.29	10.34	14.94	18.39
E_{on} $[mJ]$		48.5	48.3	47.9	48.0	48.8



(a) Double pulse test (DPT) equivalent circuit schematic.

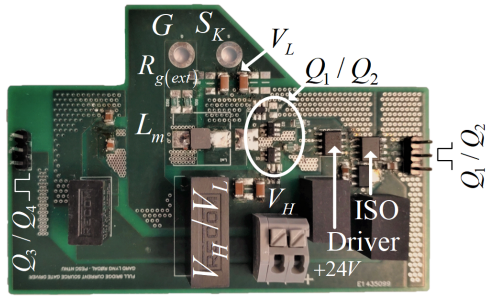


(b) Photo of the experimental setup.

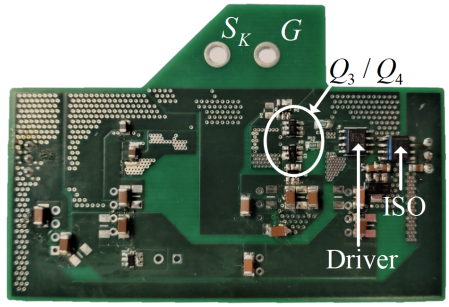
Fig. 17. Double pulse test (DPT) setup.

TABLE VIII
TURN-ON di/dt CONTROL MODE EXPERIMENTAL DATA USING THE AVSOD FOR $I_D = 300A$ AND $V_{BB} = 800V$.

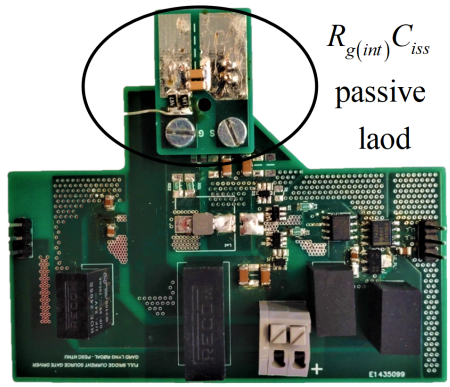
	$V_{H1}[V]$	20	27.5	30	35	40
di/dt	val $[A/ns]$	0.85	1.04	1.16	1.40	1.63
	% ↑		23.4	37.24	65.91	92.69
E_{on}	val $[mJ]$	48.5	42.0	39.2	34.4	32.6
	% ↓		13.40	19.17	29.07	32.78



(a) Top-side view.



(b) Bottom-side view.



(c) Top-side view with passive RC-load.

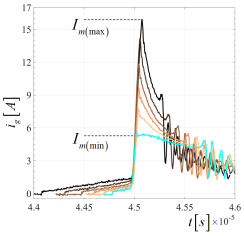
Fig. 18. Photograph of the ACSOD printed circuit board (PCB).

of operation, di/dt is kept constant at $di/dt \approx 0.85\ A/ns$ across all V_{H1} levels.

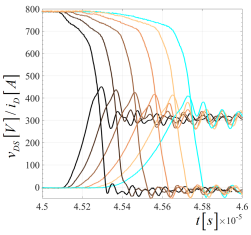
5) Turn-on di/dt and dv/dt Control Mode: Controlling dv/dt and di/dt simultaneously also becomes possible with the proposed AVSOD, as shown in the turn-on experimental results of Figs. 23g-23h. For a value of $V_{H1} = 40V$, dv/dt can increase by 57%, while di/dt increases by 178% (Table X). it is worth mentioning that with this control mode of the4 AVSOD, the peak value of the drain current $\hat{I}_D$ can also be controlled.

6) Turn-off Full Over-Drive Mode: Experimental results of the AVSOD showing the turn-off full over-drive mode (section III-B2a) are shown in Fig. 24. From the analysis of the experimental results, it is revealed that the turn-off delayed time, $T_{d(off)}$, can be reduced by 54%, the turn-off time, T_{off}, by 55% and the turn-off energy, E_{off} by 63%, when $V_{L1} = -24V$ (Table XI).

7) Turn-off Delay Control Mode: The turn-off delay control mode of the AVSOD (section III-B2b) is experimentally shown

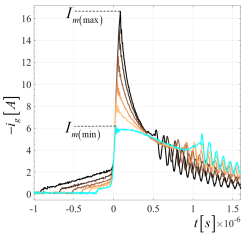


(a) Gate current i_g.

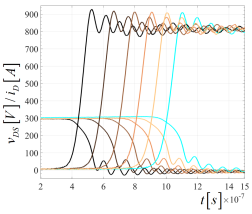


(b) Drain-source voltage v_{DS} and drain current i_D.

Fig. 19. ACSOD turn-on waveforms for varying values of I_m.



(a) Gate current i_g.



(b) Drain-source voltage v_{DS} and drain current i_D.

Fig. 20. ACSOD turn-off waveforms for varying values of I_m.

in Figs. 25a-25b, while from Table XII it is observed that by applying $V_{L1} = -24V$ to the external gate circuit, $T_{d(off)}$ can be reduced by 54% and T_{off} by 42%.

8) Turn-off di/dt Control Mode: Experimental results of the AVSOD showing the turn-off di/dt control mode (section III-B2c) are presented in Figs. 25c-25d. Based on these results, it is clear that di/dt is able to increase by approximately 81% for $V_{L1} = -24V$ resulting in a 18% reduction of E_{off} value (Table XIII). For this mode of AVSOD's operation, dv/dt is approximately constant at $dv/dt \approx 4\ V/ns$.

9) Turn-off dv/dt Control Mode: The turn-off dv/dt control mode of the AVSOD (section III-B2d) is experimentally shown in Figs. 25e-25f, while the numerical results of dv/dt, di/dt and E_{off} manipulation are given in Table XIV. In particular, for $V_{L1} = -24V$, dv/dt increases by 72%, di/dt increases by 210%, leading to a 58% decrease of E_{off}.

TABLE IX
TURN-ON dv/dt CONTROL MODE EXPERIMENTAL DATA USING THE AVSOD FOR $I_D = 300A$ AND $V_{BB} = 800V$.

	$V_{H1}[V]$	20	30	35	40
$\lvert dv/dt\rvert$	val $[V/ns]$	5.45	6.67	7.50	8.57
	% ↑		22.22	37.50	57.14
E_{on}	val $[mJ]$	48.50	47.85	47.04	45.05
	% ↓		1.32	2.99	7.11

TABLE X
TURN-ON di/dt AND dv/dt CONTROL MODE EXPERIMENTAL DATA USING THE AVSOD FOR $I_D = 300A$ AND $V_{BB} = 800V$.

	$V_{H1}[V]$	20	27.5	30	35	40
di/dt	val $[A/ns]$	0.85	1.28	1.42	1.92	2.35
	% ↑		51.01	67.82	127.0	178.1
I_D^{OS}	$\hat{I}_D[A]$	400	417	428	441	456
	% ↑		17	28	41	56
$\lvert dv/dt\rvert$	val $[V/ns]$	5.45	5.71	6.0	6.67	8.57
	% ↑		4.76	10.0	22.22	57.14
E_{on}	val $[mJ]$	48.5	38.79	34.35	28.23	24.14
	% ↓		20.02	29.17	1.79	50.22

TABLE XI
TURN-OFF FULL OVER-DRIVE MODE EXPERIMENTAL DATA USING THE AVSOD FOR $I_D = 300A$ AND $V_{BB} = 800V$.

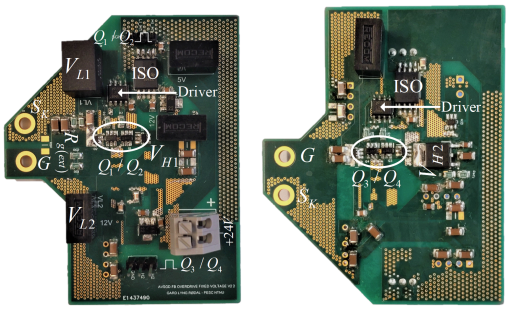
	$V_{L1}[V]$	-5	-15	-24
$T_{d(off)}$	val $[ns]$	880	530	400
	% ↓		39.77	54.54
T_{off}	val $[ns]$	1580	870	710
	% ↓		44.93	55.06
E_{off}	val $[mJ]$	26.75	13.25	9.74
	% ↓		50.46	63.58
$E_{D(off)}$	val $[\mu J]$	110.4	155.8	204.5
	% ↑		41.2	85.2

TABLE XII
TURN-OFF DELAY CONTROL MODE EXPERIMENTAL DATA USING THE AVSOD FOR $I_D = 300A$ AND $V_{BB} = 800V$.

	$V_{L1}[V]$	-5	-15	-24
$T_{d(off)}$	val $[ns]$	880	530	400
	% ↓		39.77	54.54
T_{off}	val $[ns]$	1580	1150	910
	% ↓		27.21	42.40
E_{off} $[mJ]$		26.75	26.60	24.91

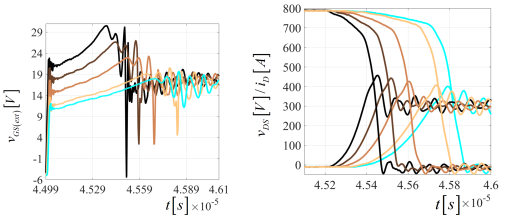
TABLE XIII
TURN-OFF di/dt CONTROL MODE EXPERIMENTAL DATA USING THE AVSOD FOR $I_D = 300A$ AND $V_{BB} = 800V$.

	$V_{L1}[V]$	-5	-15	-24
$\lvert di/dt\rvert$	val $[A/ns]$	0.461	0.795	0.838
	% ↑		72.22	81.53
E_{off}	val $[mJ]$	26.75	22.30	21.90
	% ↓		16.48	17.98



(a) Top-side view. (b) Bottom-side view.

Fig. 21. Photograph of the AVSOD printed circuit board (PCB).



(a) $v_{GS(ext)}$ mode 1) turn-on. (b) v_{DS}/i_D mode 1) turn-on.

Fig. 22. The adaptive voltage source over-driver (AVSOD) turn-on operation mode 1) as described in section III-B for $I_D = 300A$ and $V_{BB} = 800V$.

10) Turn-off di/dt and dv/dt Control Mode: Finally, experimental results of the AVSOD showing the turn-off di/dt and dv/dt control mode (section III-B2e) are shown in Figs. 25g-25h. As summarized in Table XV, dv/dt can increase by approximately 73% and di/dt by 219% when $V_{L1} = -24V$. Moreover, the controllability of V_{DS}^{OS} is also shown in this table.

C. Adaptive Current Source and Voltage Source Over-Drive Comparison

To assess the ACSOD and AVSOD performance in terms of turn-on/off delay time, turn-on/off time and turn-on/off

TABLE XIV
TURN-OFF dv/dt CONTROL MODE EXPERIMENTAL DATA USING THE AVSOD FOR $I_D = 300A$ AND $V_{BB} = 800V$.

	$V_{L1}[V]$	-5	-15	-24
dv/dt	val $[V/ns]$	4.05	5.5	7.0
	$\% \uparrow$		35.71	72.72
$\lvert di/dt \rvert$	val $[A/ns]$	0.46	0.96	1.42
	$\% \uparrow$		109.6	209.5
E_{off}	val $[mJ]$	26.75	15.77	11.10
	$\% \downarrow$		41.04	58.50

TABLE XV
TURN-OFF di/dt AND dv/dt CONTROL MODE EXPERIMENTAL DATA USING THE AVSOD FOR $I_D = 300A$ AND $V_{BB} = 800V$.

	$V_{L1}[V]$	-5	-15	-24
dv/dt	val $[V/ns]$	4.05	5.5	7.0
	$\% \uparrow$		35.71	72.72
V_{DS}^{OS}	$\hat{V}_{DS}[V]$	898	936	956
	$\% \uparrow$		38.77	59.18
$\lvert di/dt \rvert$	val $[A/ns]$	0.46	1.07	1.47
	$\% \uparrow$		133.3	219.3
E_{off}	val $[mJ]$	26.75	13.72	9.99
	$\% \downarrow$		48.72	62.66

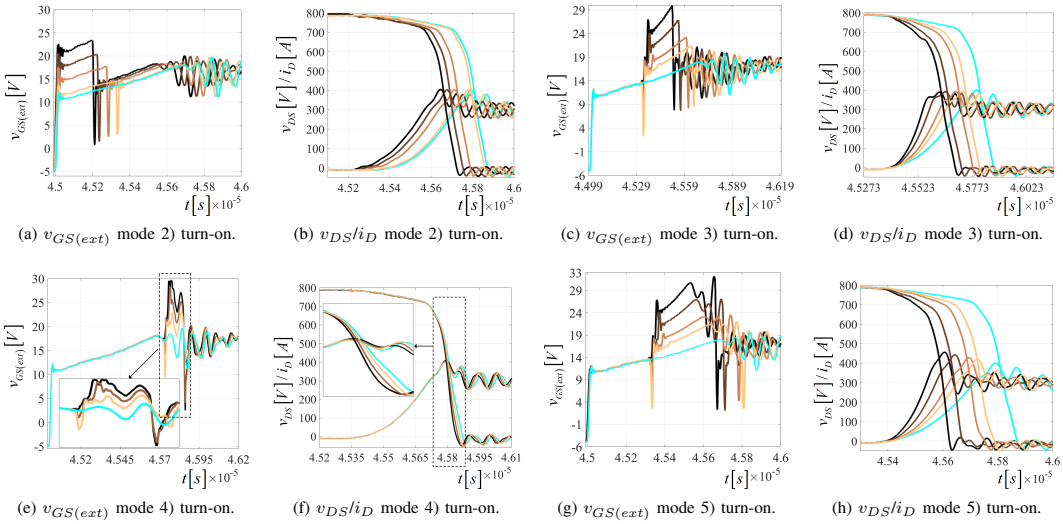
switching energy, the drivers in over-drive mode have been tested across a set of load currents and blocking voltages. The over-drive performance of the ACSOD with varying values of the current i_m amplitude I_m is shown in Fig. 27a while the over-drive performance of the AVSOD with varying values of the V_{H1} is shown in Fig. 27b. The same performance metrics are evaluated at turn-off in Fig. 28a for the ACSOD and Fig. 28b for the AVSOD, all compared to the CVSGD.

From Fig. 27, it can be seen that the controllability window becomes wider when utilising the ACSOD, where the values of $T_{d(on)}$ can be manipulated from 0% to approximately 80%, the value of T_{on} between 0% to approximately 70% and finally E_{on} can vary from 0% to approximately 60%, compared to 5-45%, 10-50% and 10-55% when using the AVSOD. Similarly, for the turn-off process, the controllability window for the turn-off delay time, $T_{d(off)}$, is wider for ACSOD compared to that one of the AVSOD as shown in Fig. 28, even though the manipulation range for T_{off} and E_{off} are approximately the same for ACSOD and AVSOD. However, as it is illustrated in Fig. 26, the cost for the larger manipulation window is the higher gate drive energy use from the ACSOD compared to AVSOD.

A way to decide which over-driver concept should be utilised in a power converter that exhibits adaptive operation through the adjustment of switching energies can be seen in Fig. 29. This figure shows a comparison between the turn-on energy by using the ACSOD with $I_{m(max)}$, i.e. $E_{on(I_{m(max)})}^{ACSOD}$, and when using the AVSOD with $V_{H1} = 40V$, i.e. $E_{on(V_{H1}=40V)}^{AVSOD}$, and $V_{H1} = 30V$, i.e. $E_{on(V_{H1}=30V)}^{AVSOD}$ (Fig. 29a). The same comparison of the turn-off energy between the ACSOD with $I_{m(max)}$, i.e. $E_{off(I_{m(max)})}^{ACSOD}$, and AVSOD with $V_{L1} = -24V$, i.e. $E_{off(V_{L1}=-24V)}^{AVSOD}$, and $V_{L1} = -15V$, i.e. $E_{off(V_{H1}=-15V)}^{AVSOD}$, is shown in Fig. 29b.

D. Variable Voltage Source Multi-level Gate Driver

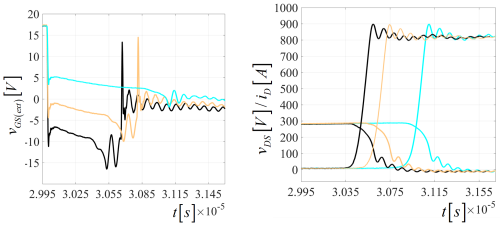
Experimental results of the different operating modes of the VVSMGD are given in the following subsections, with a photograph of the printed circuit board (PCB) shown in Fig. 30.



(a) $v_{GS(ext)}$ mode 2) turn-on. (b) v_{DS}/i_D mode 2) turn-on. (c) $v_{GS(ext)}$ mode 3) turn-on. (d) v_{DS}/i_D mode 3) turn-on.

(e) $v_{GS(ext)}$ mode 4) turn-on. (f) v_{DS}/i_D mode 4) turn-on. (g) $v_{GS(ext)}$ mode 5) turn-on. (h) v_{DS}/i_D mode 5) turn-on.

Fig. 23. The adaptive voltage source over-driver (AVSOD) turn-on operation modes 2)-5) as described in section III-B for $I_D = 300A$ and $V_{BB} = 800V$.



(a) $v_{GS(ext)}$ mode 6) turn-off. (b) v_{DS}/i_D mode 6) turn-off.

Fig. 24. The adaptive voltage source over-driver (AVSOD) turn-off operation mode 6) as described in section III-B for $I_D = 300A$ and $V_{BB} = 800V$.

TABLE XVI
VVSM GATE DRIVER PARAMETERS

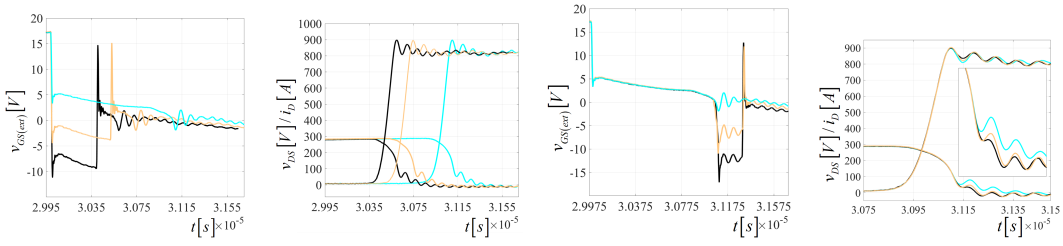
L_B	R_B	R_{BL}	C_{BL}	f_{sw_B}	$R_{g(ext)}$
$3.3\mu H$	1.4Ω	$5k\Omega$	$6.8\mu F$	$2MHz$	1.2Ω

1) Turn-off Delay Manipulation: Experimental results verifying the effect of the turn-off delay manipulation are shown in Fig. 31. The effect of applying a variable voltage v_B to the gate prior to turn-off is clear, with a maximum reduction of 88.9% in $T_{d(off)}$, 51.7% in T_{off} and 6.7% in E_{off} comparing the maximum delay manipulation with $v_B = V_{GS}^{pre} = 9V$ to no delay manipulation (marked in light blue color Fig. 31).

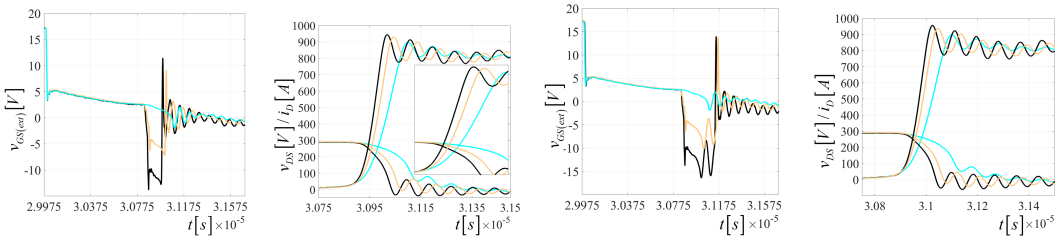
2) Turn-off Voltage Overshoot Manipulation: Experimental results demonstrating the voltage overshoot manipulation are shown in Figs. 32 and 33. In Fig. 32a, a single-pulse operation mode with two different buck voltage v_B levels is shown, resulting in different reduction in V_{DS}^{OS}. Fig. 32b presents the percentage reduction in V_{DS}^{OS} and the resulting percentage increase in the turn-off energy E_{off} over a set of v_B values compared to no overshoot manipulation (red waveforms in Fig. 32a) while operating as in Fig. 32a. Using no overshoot manipulation yields an overshoot value of $V_{DS}^{OS} = 185V$, while using a single-pulse operation mode with $v_B = 9V$ yields $V_{DS}^{OS} = 103V$, i.e. a $\sim 44\%$ reduction. Using no overshoot manipulation yields a turn-off energy of $E_{off} = 0.0517J$, while using a single-pulse operation mode with $v_B = 9V$ results in $E_{off} = 0.1056J$, i.e. a $\sim 104\%$ increase. Fig. 33a shows the multi–pulse operation mode of the VVSMGD with a buck voltage value of $v_B = 13V$. From these measurements, it is revealed that using a multi–pulse operation allows for both reduction in V_{DS}^{OP} as well as manipulation of the frequency spectrum imposed by v_{DS}, as seen in Fig. 33b.

3) Turn-on Current Overshoot Manipulation: The experimental results validating the manipulation of the drain current overshoot are shown in Fig. 34. The i_D overshoot is clearly adjustable by applying v_B to the gate during the time interval where i_D reaches the peak value. As seen in Fig. 34b, using no i_D overshoot manipulation yields an overshoot of approximately $I_D^{OS} \approx 75A$ at a load current level $I_D \approx 300A$ and this overshoot is reduced to $I_D^{OS} \approx 20A$ overshoot with $v_B = 9V$. The turn-on energy with no i_D overshoot manipulation is $E_{on} \approx 0.103J$ and is increased to $E_{on} \approx 0.187J$ using $v_B = 9V$. The controllability window for various values of v_B is shown in Fig. 34b, where it is observed that I_D^{OS} can be reduced up to 73% when $v_B = 9V$ at a cost of 45% higher E_{on}.

4) Conduction Loss Manipulation: Exemplary experimental results showing the conduction loss manipulation mode

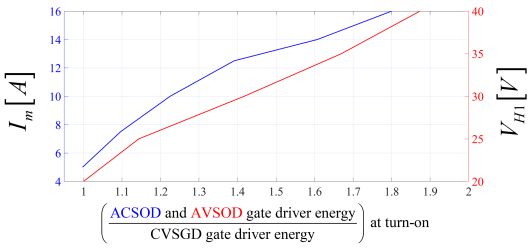


(a) $v_{GS(ext)}$ mode 7) turn-off. (b) v_{DS}/i_D mode 7) turn-off. (c) $v_{GS(ext)}$ mode 8) turn-off. (d) v_{DS}/i_D mode 8) turn-off.

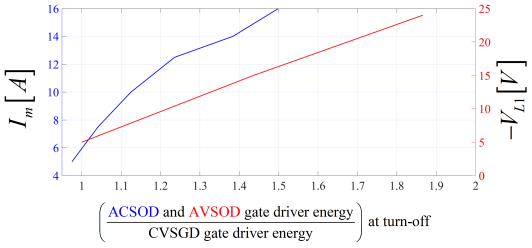


(e) $v_{GS(ext)}$ mode 9) turn-off. (f) v_{DS}/i_D mode 9) turn-off. (g) $v_{GS(ext)}$ mode 10) turn-off. (h) v_{DS}/i_D mode 10) turn-off.

Fig. 25. The adaptive voltage source over-driver (AVSOD) turn-off operation modes 7)-10) as described in section III-B for $I_D = 300A$ and $V_{BB} = 800V$.

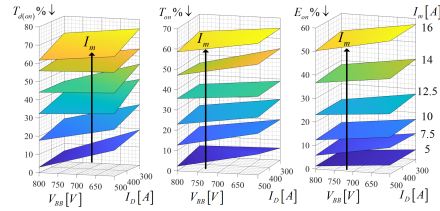


(a) Turn-on ACSOD (blue) and AVSOD (red) gate drive energy ratio to CVSGD gate driver energy for different values of I_m and V_{H1}.

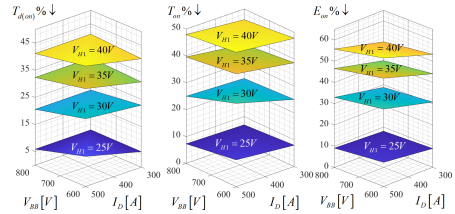


(b) Turn-off ACSOD (blue) and AVSOD (red) gate drive energy ratio to CVSGD gate driver energy for different values of I_m and V_{L1}.

Fig. 26. ACSOD and AVSOD over-drive mode gate drive energy ratio to CVSGD gate driver energy for $R_{g(ext)} = 1.2\Omega$.



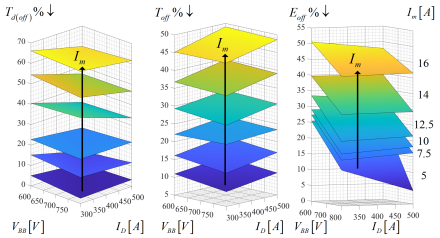
(a) Turn-on over-drive ACSOD values for different I_m.



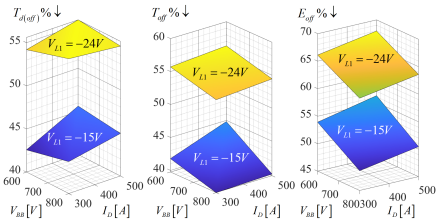
(b) Turn-on over-drive AVSOD values for different V_{H1}.

Fig. 27. Comparison of turn-on over-drive performance in terms of $T_{d(on)}$, T_{on} and E_{on} between ACSOD and AVSOD.

are shown in Fig. 35. At $t = t_0^c$, the DUT is turned on with $v_{DRV} = V_H = 20V$ applied to the gate. At $t = t_1^c$, Q_2 and Q_3 are turned on while Q_1 is turned off, applying $v_B = 9V$ to the gate. Thus, as $v_{GS} \to v_B$, $r_{DS(on)}$ increases as observed in Fig. 3b, affecting v_{DS}. At $t = t_2^c$, v_B is still applied to the gate, but a change in the duty cycle of the buck converter from $d = 0.4 \to d = 0.6$ is performed, resulting in $v_B \to 11V$, reducing $r_{DS(on)}$ and v_{DS}. At $t = t_3^c$, V_H is applied to the gate, further reducing $r_{DS(on)}$ and v_{DS}. Again, at $t = t_4^c$, $v_B = 11V$ is applied to the

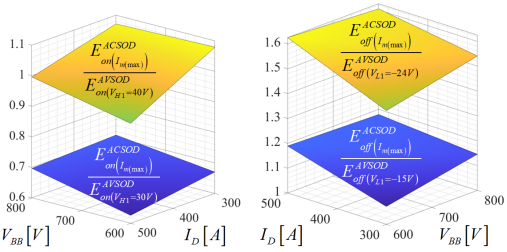


(a) Turn-off over-drive ACSOD values for different I_m.



(b) Turn-off over-drive AVSOD values for different V_{L1}.

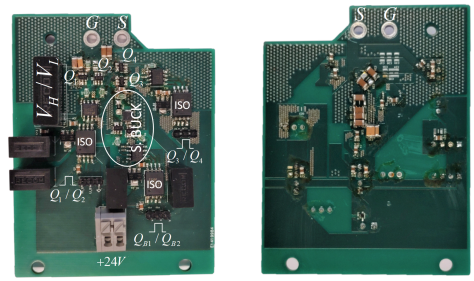
Fig. 28. Comparison of turn-off over-drive performance in terms of $T_{d(off)}$, T_{off} and E_{off} between ACSOD and AVSOD.



(a) E_{on} comparison between ACSOD and AVSOD for maximum levels of I_m vs. $V_{H1} = 40V$ and $V_{H1} = 30V$.

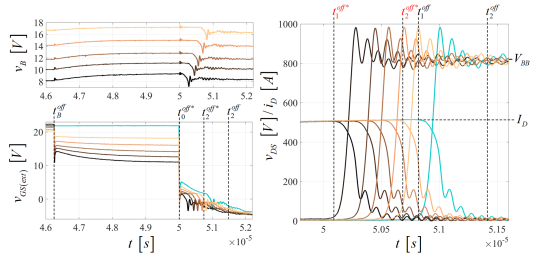
(b) E_{off} comparison between ACSOD and AVSOD for maximum levels of I_m vs. $V_{L1} = -24V$ and $V_{L1} = -15V$.

Fig. 29. Ratio > 1 means ACSOD is resulting in a higher $E_{on/off}$ value than AVSOD.

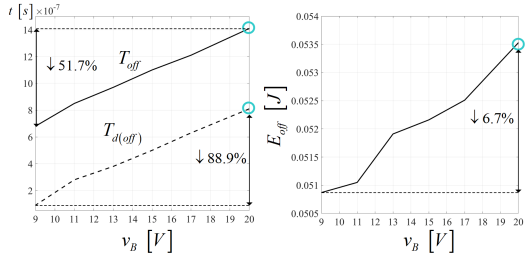


(a) Top-side view. (b) Bottom-side view.

Fig. 30. Photograph of the variable voltage source multi-level gate driver (VVSMGD) printed circuit board (PCB).



(a) V_B, $v_{GS(ext)}$ and i_D/v_{DS} waveforms.



(b) $T_{d(off)}$, T_{off} and E_{off} reduction.

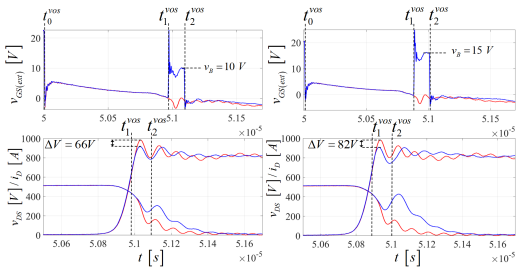
Fig. 31. VVSMGD turn-off delay manipulation

gate and $r_{DS(on)}$ and v_{DS} increase. The drain current i_D (red waveform) and instantaneous power loss $p = i_D \cdot v_{DS}$ (blue waveform) are shown in the lower plot in Fig. 35, and it is clear how manipulating v_{GS} results in fine-grained control of the conduction power loss, p.

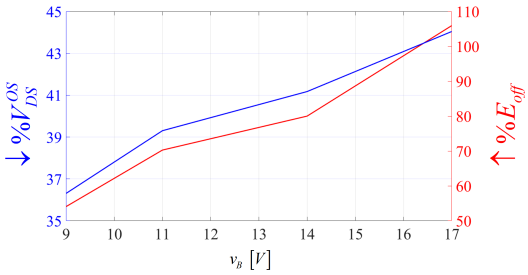
VI. Discussion

The ACSOD is seen to be able to control the overall $T_{d(on/off)}$, $T_{(on/off)}$ and $E_{on/off}$ by adjusting the pre-charge current amplitude I_m. For $V_{BB} \in [600, 800]V$ and $I_D \in [300, 500]A$ of the SiC MOSFET power module, the ACSOD achieves a maximum reduction of $50-55\%$ in E_{on}, a $60-65\%$ reduction in T_{on} and a $60-75\%$ reduction in $T_{d(on)}$ for turn-on, while a maximum $40-50\%$ reduction in E_{off}, a $45-50\%$ reduction in T_{off} and a $60-65\%$ reduction in $T_{d(off)}$ is achieved at turn-off given the I_m^{OS} constraint.

The presented AVSOD has been shown to be able to independently control $T_{d(on/off)}$, $T_{(on/off)}$ and $E_{on/off}$, as well as device dv/dt and di/dt. For $V_{BB} \in [600, 800]V$ and $I_D \in [300, 500]A$, the AVSOD achieves a maximum $50-55\%$ reduction in E_{on}, a 48% reduction in T_{on} and a 40% reduction in $T_{d(on)}$ for turn-on using the over-drive mode with $V_{H1} = 40V$, while a maximum $60-68\%$ reduction in E_{off}, a 55% reduction in T_{off} and a $53-57\%$ reduction in $T_{d(off)}$ is achieved at turn-off using the over-drive mode with $V_{L1} = -24V$. As can be seen in Fig. 29, using the AVSOD in over-drive mode with $V_{H1} = 40V$ yields a similar E_{on} values as using the ACSOD with $I_{m(max)} \approx I_m^{OS} \approx 16A$. For turn-



(a) $v_B = 10V$ (left) and $v_B = 15V$ (right) in blue waveforms compared to no overshoot manipulation shown in red waveform color.



(b) V_{DS}^{OS} reduction and E_{off} increase.

Fig. 32. Single-pulse VVSMGD turn-off voltage overshoot V_{DS}^{OS} manipulation.

off, using the AVSOD in over-drive mode with $V_{L1} = -15V$ yields marginally lower E_{off} as using the ACSOD with $I_{m(max)} \approx I_m^{OS} \approx 16A$, while using $V_{L1} = -24V$ yields a lower E_{off} than using the ACSOD with $I_{m(max)} \approx I_m^{OS}$ with a factor of $1 : 1.6$.

The AVSOD shows a higher degree of control capabilities compared to the ACSOD with the same number of discrete driver switches. While the AVSOD is capable of independently increasing or decreasing the DUT switching parameters E_{on}/E_{off}, T_{on}/T_{off}, $T_{d(on)}/T_{d(off)}$, di/dt and dv/dt by controlling the length, timings and magnitude of the applied voltages, the ACSOD may only adjust the amplitude of I_m, hence dependently reducing or increasing the DUT switching parameters compared to the previous switching instant. A caveat to this – an operating point of the ACSOD which is not shown in this paper, but addressed in [40] – is the ACSOD ability to reduce dv/dt and di/dt by commutating i_g away from the gate at a specified time instant during the switching interval. For instance, during turn-on, the increase of dv/dt is accomplished by turning Q_4 on for a given time period after injecting i_m into the gate, hence commutating i_g into V_L (i.e. V_L is effectively applied to the gate), reducing dv/dt and increasing E_{on}. The same can be accomplished for turn-off by turning Q_3 on for a certain time period after the turn-off is initiated by turning Q_2 on. Turning Q_3 on after v_{DS} rise will effectively reduce di/dt, which will increase E_{off}. Furthermore, while the ACSOD is limited in L_m driving energy by the internal gate resistance $R_{g(int)}$ and the critical damping criterion (which one may move away from, however, proper driver design considering the effective RLC circuit must be done to ensure safe operation and avoid excessive v_{GS} voltages), there is no restriction on the AVSOD over-drive levels V_{H1}/V_{L1}. However, strict safety consideration must be adhered to (e.g. hard-coded maximum on-time of the AVSOD Q_1/Q_2 for a given DUT and V_{H1}/V_{L1}) when using high over-drive voltages to ensure that v_{GS} does not exceed its safe operating limits.

Both the ACSOD and AVSOD can be further modified to include the proven adaptive capabilities of the VVSMGD. By including the synchronous buck into the ACSOD and AVSOD high-side voltage source, the conduction loss and $T_{on}/T_{d(on)}$ manipulation capabilities of the VVSMGD can be included in the over-drivers, yielding an even higher degree of adaptability. Inclusion of these capabilities in the ACSOD and AVSOD drivers is shown in Fig. 36.

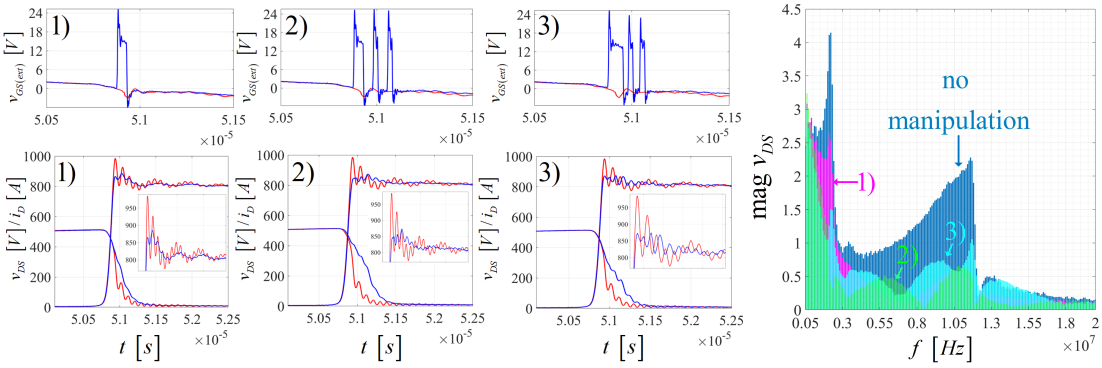
Using the turn-off delay manipulation as descried in section IV-A includes reducing v_{GS} prior to actual turn-off. Evidently, this leads to an increase in device $r_{DS(on)}$, as seen from Fig. 3b. Thus, the instantaneous conduction loss p_{cond} will slightly increase during during $T_{d(off)}$ adjust (Fig. 16a). However, as seen from Fig. 3b, significant increase in $r_{DS(on)}$ occur for decreasing v_{GS} below $10V$, hence keeping V_{GS}^{pre} below such level keeps the increase in p_{cond} low during this time interval. Furthermore, $T_{d(off)}$ adjust should be significantly lower than the pwn on-time, hence the increase in instantaneous p_{cond} is low on the average conduction loss.

VII. Conclusion

This paper presented two novel adaptive voltage source gate drivers, namely the adaptive voltage source over-driver (AVSOD) and the variable voltage source multi-level gate driver (VVSMGD). The paper introduced the concept of gate over-driving and compares the over-driving capabilities of the AVSOD with an adaptive current source over-driver (ACSOD) based on a full-bridge driver topology. The working principles of the presented drivers are accurately described, and their operating modes verified experimentally on the FMF750DC-66A SiC MOSFET half-bridge power module using a double pulse test setup.

The presented AVSOD is seen to be able to independently control the DUT's switching losses, turn-on/off time and turn-on/off delay times, as well as di/dt and dv/dt. The over-driving capability of the AVSOD is able to reduce E_{on} up to 55% and E_{off} by 68% in over-drive mode with the utilised driver voltage levels, while the over-driving capability of the ACSOD is able to reduce E_{on} up to 58% and E_{off} by 50% in over-drive mode with the given $I_{m(max)}$ values.

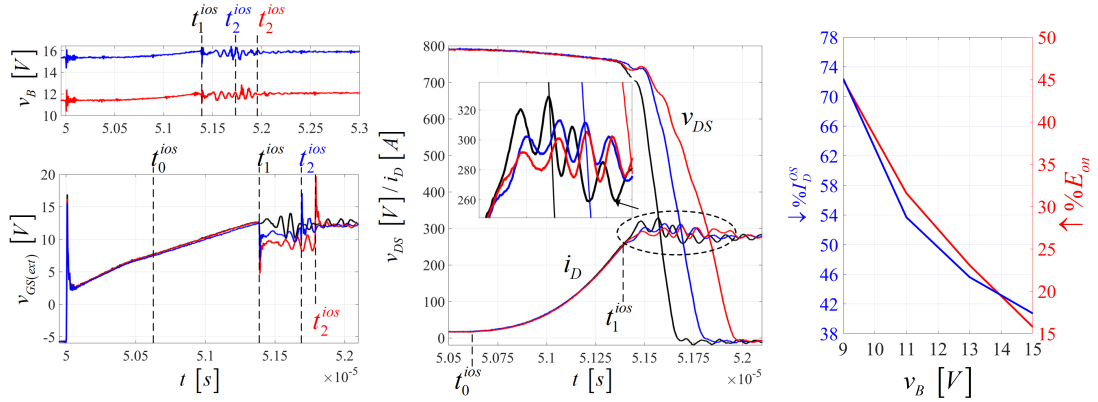
The presented VVSMGD has shown to control turn-off delay times and consequently turn-off times, turn-off v_{DS} overshoots and turn-on i_D overshoots of the switched DUT. From experiments, it has been shown that by using the VVSMGD, the voltage overshoot on v_{DS} can be reduced by 44%. Furthermore, by manipulating the duty-cycle of the



(a) $v_{GS(ext)}$ with $v_B = 15V$ upper figures and i_D/v_{DS} lower figures.

(b) Frequency spectrum of the v_{DS} oscillations.

Fig. 33. Multi-pulse VVSMGD turn-off voltage overshoot V_{DS}^{OS} manipulation.



(a) Drain current i_D overshoot manipulation with $v_B = 15V$ (blue waveform color), $v_B = 11V$ (red waveform color) compared to no manipulation (black waveform color).

(b) I_D^{OS} reduction and E_{on} increase.

Fig. 34. Turn-on current overshoot I_D^{OS} manipulation.

integrated buck converter, the driver can accurately adjust the DUT conduction loss through the dynamic adjustment of $r_{DS(on)}$.

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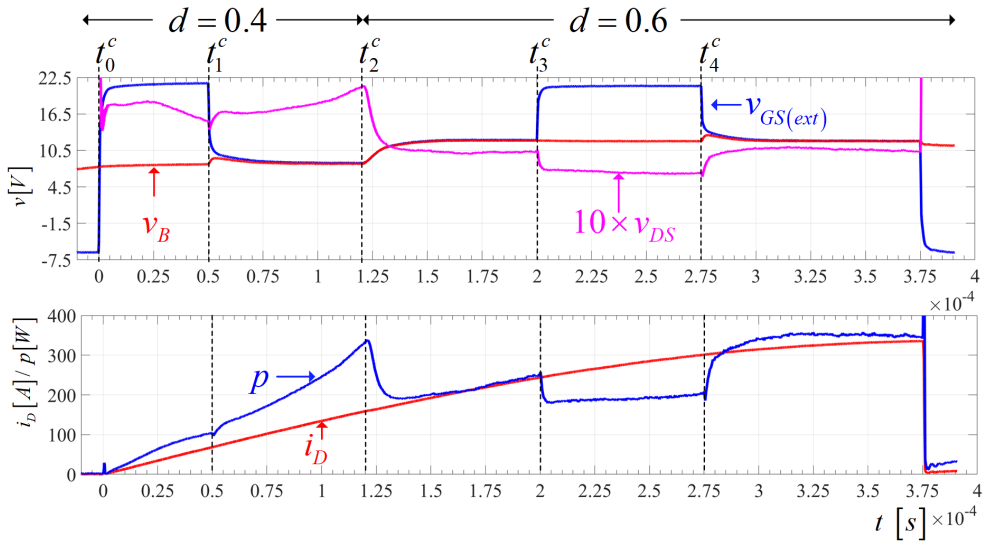

Fig. 35. Single pulse test showing the conduction loss manipulation operation. Upper figure shows v_{GS} (blue waveform), v_B (red waveform) and $10 \cdot v_{DS}$ (magenta waveform) with the buck converter duty-cycle d changes. The lower figure shows the drain current $_D$ (red waveform) and the instantaneous power loss of the device $p = i_D \cdot v_{DS}$.

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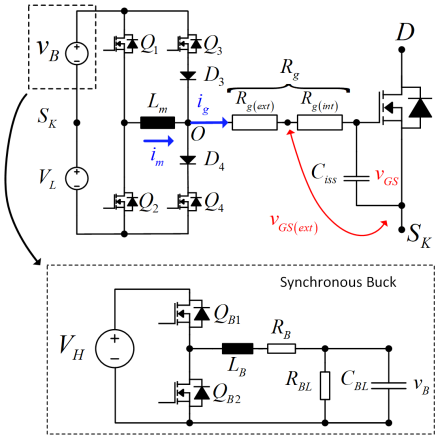
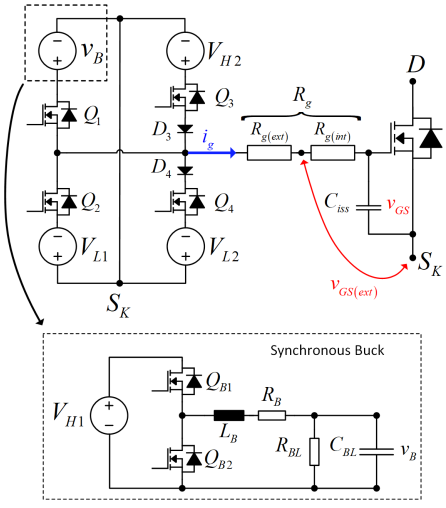


(a) Modified ACSOD.



(b) Modified AVSOD.

Fig. 36. ACSOD and AVSOD with the capabilities of VVSMGD.

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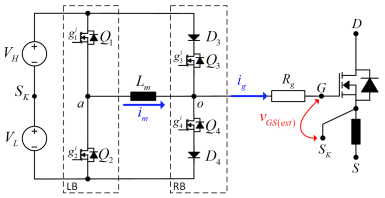
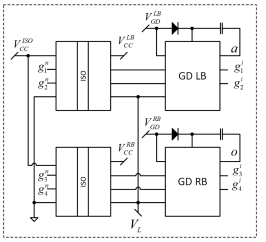
Appendix B

Adaptive Gate Drivers

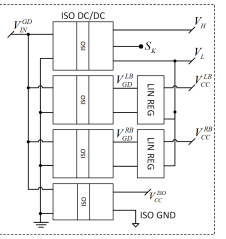
Adaptive gate driver schematic and PCB details.



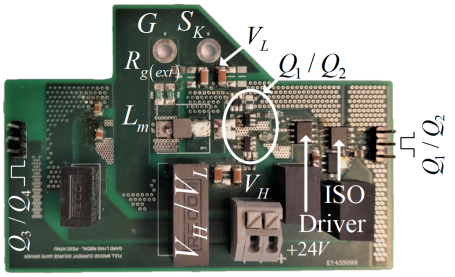
(a) CCSGD circuit schematic.



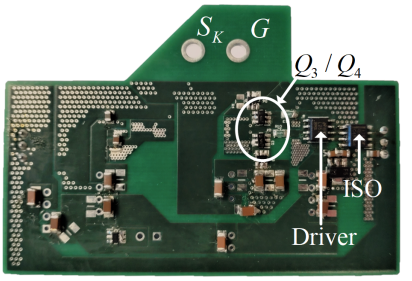
(b) CCSGD signal and drive schematic.



(c) CCSGD power supply schematic.

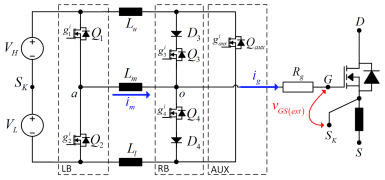


(d) PCB top side.

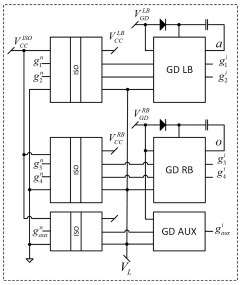


(e) PCB bottom side.

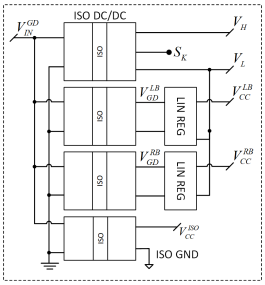
Figure B.1: The conventional current source full-bridge gate driver (CCSGD).



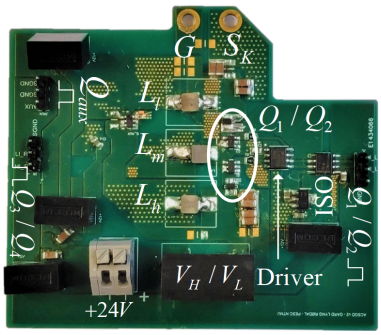
(a) EACSOD circuit schematic.



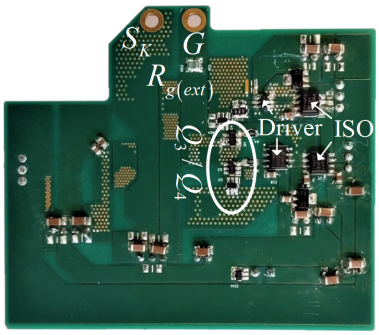
(b) EACSOD signal and drive schematic.



(c) EACSOD power supply schematic.

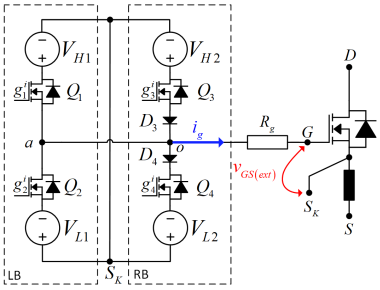


(d) PCB top side.

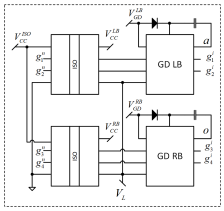


(e) PCB bottom side.

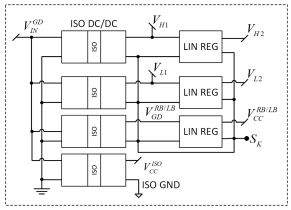
Figure B.2: The extended adaptive current source over-driver (ACSOD).



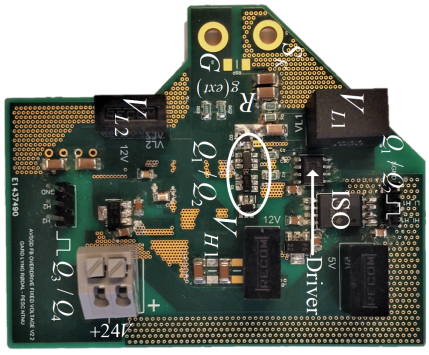
(a) AVSOD circuit schematic.



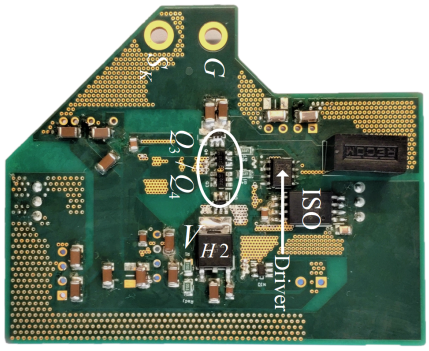
(b) AVSOD signal and drive schematic.



(c) AVSOD power supply schematic.

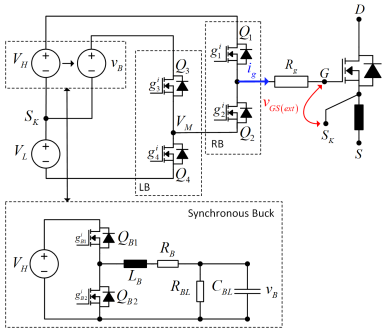


(d) PCB top side.

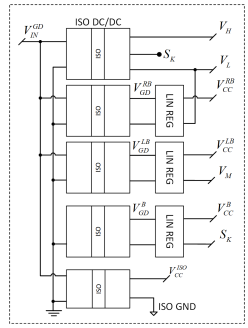


(e) PCB bottom side.

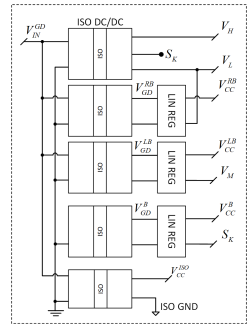
Figure B.3: The adaptive voltage source over-driver (AVSOD).



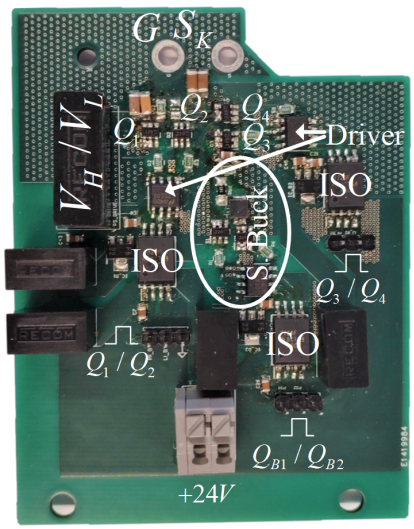
(a) VVSMGD circuit schematic.



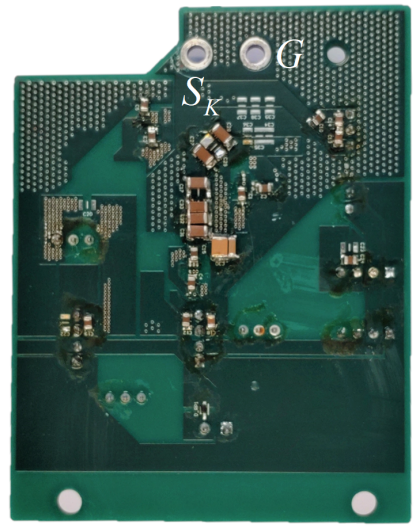
(b) VVSMGD signal and drive schematic.



(c) VVSMGD power supply schematic.



(d) PCB top side.



(e) PCB bottom side.

Figure B.4: The variable voltage source multi-level gate driver (VVSMGD).

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