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TFE4930_1 - MASTER THESIS

Passive Ramp Generator for CMOS Image Sensors

By :
Mudasir Ali Tariq

Supervisors: Trond Ytterdal, Nguyen Thanh Trung

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Abstract

CMOS Image Sensors are a key building block in all systems requiring imaging capability such as mobile phones, digital cameras, space imaging equipment and is used in many more imaging devices. In most of these sensors one of the most common ADC utilized to convert the analog information into digital form is the 'SSADC'(Single Slope ADC)[1], which includes a ramp generator for it's operation. Most of these ramp generators are mixed signal circuits, and not many are found in literature which are purely analog in nature, this thesis thus aims to build a "Continuous Time Passive Ramp Generator" under given specifications of **slope range**, **voltage swing**, **linearity** and **noise**. The designed ramp generator operates at a supply voltage of 1.8V with an operating temperature range of $40°C - 125°C$ and is tested over ss,sf,fs and ff corners.It consumes a maximum average power of 3.5mW , covering a slope range of 125mV/µs to 2000mV/µs, the maximum output noise is $18\mu V_{rms}$ and the maximum INL is 0.7%.

Preface

This Master Thesis concludes the 2 year's Master Program in "Electronic System Design(ELSYS)' at the Norwegian University of Science and Technology(NTNU). The topic for the thesis was given by my external supervisor from the company "SONY", Nguyen Thanh Trung. The university supervior was Professor Trond Ytterdal. The topic for this thesis focuses on building a continuous time passive ramp generator for SSADCs used widely in image sensors, the goal was to build and simulate the circuit schematic until it meets the given specifications that were given by the external supervisor, and finally then reporting the key results, so that a comparison can be made in the future with the existing ramp generator topologies. The thesis includes hand analysis and schematic simulation results.

I am thankful to both Nguyen Thanh Trung and Trond Ytterdal for the guidance they provided me during our regular meeetings.

Glossary

apmom1v8 1.8V alternate polarity Metal ON Metal Capacitor. 9

CMOS Complementary Metal Oxide Semiconductor. 1, 2, 36

egslvtnfet EG Super-low Vt nfet. 9

egslvtpfet EG Super-low Vt pfet. 9

fs fast slow corner. 31

FVF Flipped Voltage Follower. 19, 20

pnoise Periodic Noise Analysis. 36

pss Periodic Steady-State Analysis. 36

PVT Process Voltage Temperature. iv, v, 3, 8, 17–19, 23, 28–31

SAR-ADC Successive Approximation Register ADC. 1

sf slow fast corner. 31

ss slow slow corner. 17, 23, 25, 31

SS-ADC Single Slope ADC. 1, 36

tt typical typical corner. 31

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Chapter 1

Introduction

Most of the modern visual systems require a CMOS Image Sensor[2] to capture the raw analog information and convert it to digital information for further processing, that is they require an ADC for the data conversion, this is accomplished by using various architectures which include pixel-level ADCs[3], column-level ADCs[4] and chip level ADCs[5], out of all of these architectures the column-level method is widely adopted since it provides a good trade-off between speed and area[6]. In this column-level architecture various architectures of ADCs are used which include "SS-ADC"[1], "SAR-ADC"[7] and "cyclic ADC"[8]. Out of all of these architectures the SS-ADC architecture is widely adopted due to its simplicity since it only contains a single ramp generator, some comparators and digital circuits. The operation is very simple, the input voltage which carries the light intensity information is compared(through a comparator) with the ramping voltage from the ramp generator, the amount of time it takes for the ramping voltage to reach the level of the input voltage carries the information about the pixel intensity, the subsequent digital circuits in the pipeline can convert this time information to a digital value by means of a counter[6].This thesis focuses on a single but pivotal block of the SS-ADC, which is the "RAMP Generator". While most of the the ramp generators use counter based or shift register based techniques[6],[9],[10] to ramp up or down the voltage, this thesis works on the possibilty of using a "Passive Ramp Generator" instead of "Counter/Shift Register-based" topologies. After the final implementation of the design a comparison can be made in context of how does it rival with the existing popular topologies.

1.1 Process Technology

The the technology used in this thesis is the 22nm-FDSOI technology where FDSOI is the abbreviation for "**Fully depleted Silicon on Insulator**", the transistor implemented in this technology has the benefit of lower leakage power dissipation[11] when compared to its bulk CMOS counterpart.Figures of both a transistor implemented in bulk CMOS and a transistor implemented in FDSOI are shown below.

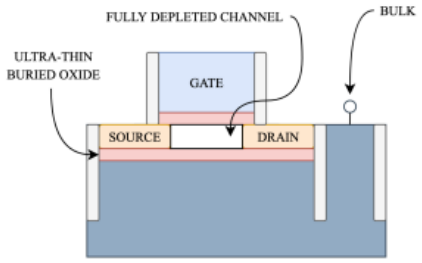

Figure 1.1: FDSOI MOSFET[12].

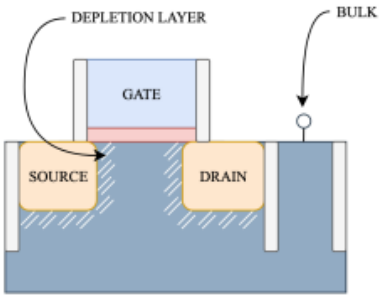

Figure 1.2: Traditional MOSFET[12].

The "ULTRA-THIN BURIED OXIDE" layer ensures a very low leakage current from the channel towards the substrate and hence ensuring very low leakage power dissipation, this fact is important as it would reduce the the amount of leakage in the logic gates that are used to program our ramp generator. The FDSOI tranistor is especially known for it's back-gate effect in which applying a bias voltage at the body can drastically alter the threshold voltage, this effect however is not used in this thesis as it would require extra biasing circuitry to generate the bias voltages which would consume a little extra power, and so the author was reluctant to do that.

1.2 Thesis Outline

The thesis is organized as follows:

Chapter 2 - Background Theory This chapter dwells upon the existing ramp-generators used in the context of CMOS image sensors, it describes how they function and how they differ from the continuous ramp generator. This chapter also mentions the key specifications of the ramp generator that we will be looking at in this thesis.

Chapter 3 - Design Procedure This chapter takes the reader to a step by step procedure towards designing a passive ramp generator such that it fulfills all the specifications.The chapter starts off by discussing the design of the first stage, then it moves onto choosing a reliable architecture for the buffer, finally it ends on the final design with the first stage and the buffer cascaded.

Chapter 4 - Final Results This chapter shows the schematic simulation results of the ramp generator designed in chapter 3. It shows the final results of all the relevant specifications.

Chapter 5 - Discussion This chapter discusses the simulation results of Chapter 4, and also discusses potential improvements that can be made to the final design, it also looks upon areas which were not accounted in great detail in this thesis

Chapter 6 - Conclusion and Future Work This chapter concludes the thesis with some final remarks from the author.

Chapter 2

Background Theory

2.1 Basic Topology

Conceptually implementing a a "Continuous Time Passive Ramp Generator" is pretty simple, if we consider a ramping down operation then it could be simply realized by a constant current source discharging a capacitor as shown in figure 2.1, however building a constant current source over PVT variations is the real challenge and another notable thing to mention here is that we need to feed this ramp to a load of about 200pF[13] and this is a rough value since it is not fixed by the designer, hence if one directly attaches a current source to this large capacitive load then there would be uncertainty in the rate of change of the ramp. Also it may be required that the starting point of the ramp is not the supply voltage in the case of a ramping down slope, in that case we have flexibility to set the starting bias point to a particular value at the output of the buffer. In light of the problems highlighted above the actual implementation would be that as shown in figure 2.2, where we have included a buffer to drive the large output capacitor with an uncertain value, this way the biasing current which realizes the current source is also minimized.

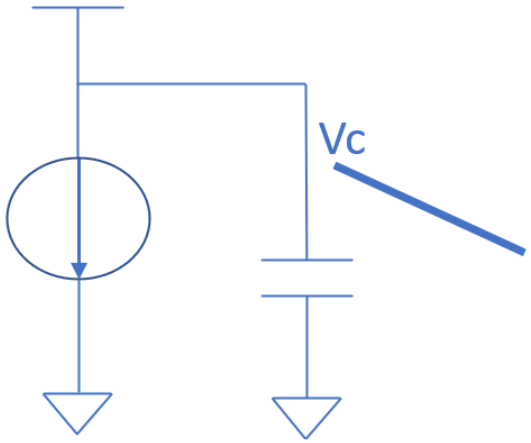

Figure 2.1: Simple Ramp Generator

2.2 Specifications of a RAMP Generator

In this thesis the critical specifications for the "RAMP GENERATOR" that are focused upon are as follows:

- Voltage Swing

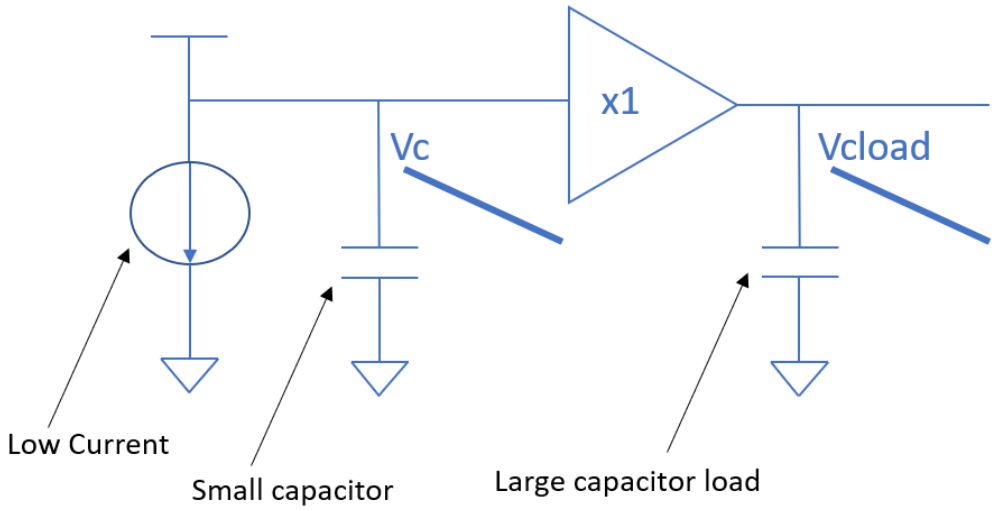

Figure 2.2: Simple Ramp Generator with Buffer

- Integral Non-Linearity(INL)
- Noise
- Slope-Range
- Power Consumption

We will go through each of these to specifications so that it is clear what they are and how do we compute them in our simulations.

2.2.1 Voltage Swing

It is simply the voltage range the Ramp should cover, this is shown in figure 2.3

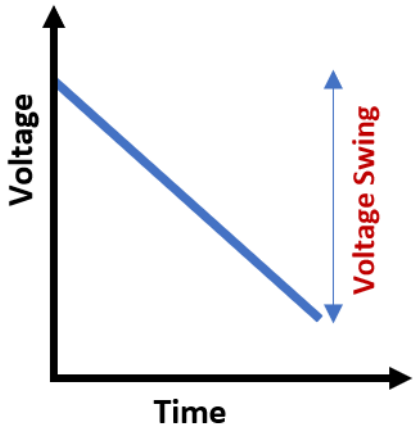

Figure 2.3: Voltage Swing Illustration

2.2.2 Integral Non-Linearity(INL)

This would be simply a measure of how straight the ramp is, and the way it is measured in this thesis is shown in figure 2.4, it is measured as a percentage in this thesis where we simply represent INL_{max} as a fraction of the voltage swing.

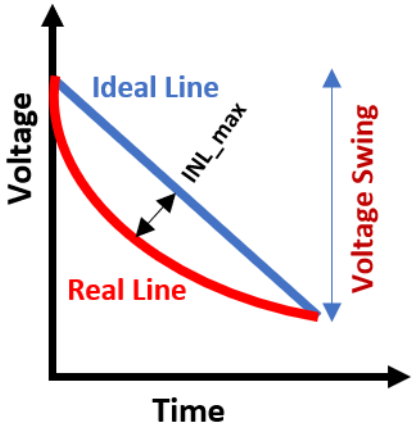

Figure 2.4: INL Measurement Illustration

2.2.3 Noise

For this thesis the noise measurement at the output is the total integrated noise in Volts(V) covering the frequency range 200kHz to 1GHz. Since the time period from one ramp to another ramp is on average 5µs which translates to a frequency of $\frac{1}{5\mu s} = 200kHz$ and noise power below this frequency is almost cancelled out by the CDS(Correlated Double Sampling) method[14] often used in image sensors.

2.2.4 Slope-Range

It is the range of values for the slope magnitude of the ramp, for this thesis it goes from 125mV/µs to 2000mV/µs

2.2.5 Power Consumption

It is simply the average power consumed by the ramp generator circuit, which includes both dynamic and static power.

2.3 Previous Work

In this section we would discuss some of the architectures usually used as Ramp Generators that are mentioned in the literature, however a general review of most of the architectures reveal that the majority of the RAMP Generators are mixed-signal circuits in nature[9],[10] instead of being purely analog. One of the architecture is summarized in figure 2.5 where a digital counter may count up or down depending on weather we want to ramp or down, the counter value is then converted to an analog value by the use of a DAC, normally a Current Steering DAC[6], by this a ramp at the output is generated which is discrete in nature and resembles a staircase. Another popular implementation found in literature was to use a shift register to tap different points of a resistor ladder to generate the ramp[9], the resistor ladder is supplied current by a programmable current source, the illustration of this architecture is shown in figure 2.6, a capacitor variant of this topology is also mentioned in[15]. A general overview of various ramp generator topologies is presented in [16], where it is mentioned that the topology in figure 2.6 and it's capacitive variant suffer from issues of high area consumption and reduced linearity due to matching constraints. In comparison, a continuous time ramp generator that is also mentioned in [16] by the name of 'Continuous CTIA' where a passive integrator is used to generate the ramp, occupies a lower area with high linearity and also the area stays the same with an increase in resolution, however the implementation is not just that of the passive integrator instead extra hardware is added to auto-calibrate the input current to the integrator continuously. This calibration is done by comparing the ramp against a clock-frequency, the reader can refer to [17] for an in-depth explanation.

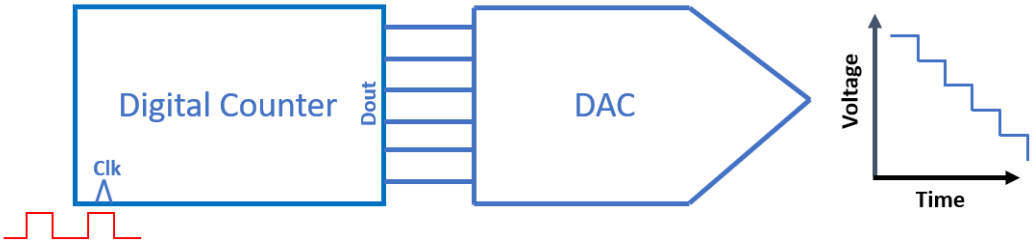

Figure 2.5: Popular Architecture for Ramp Generators in CMOS Image Sesnors

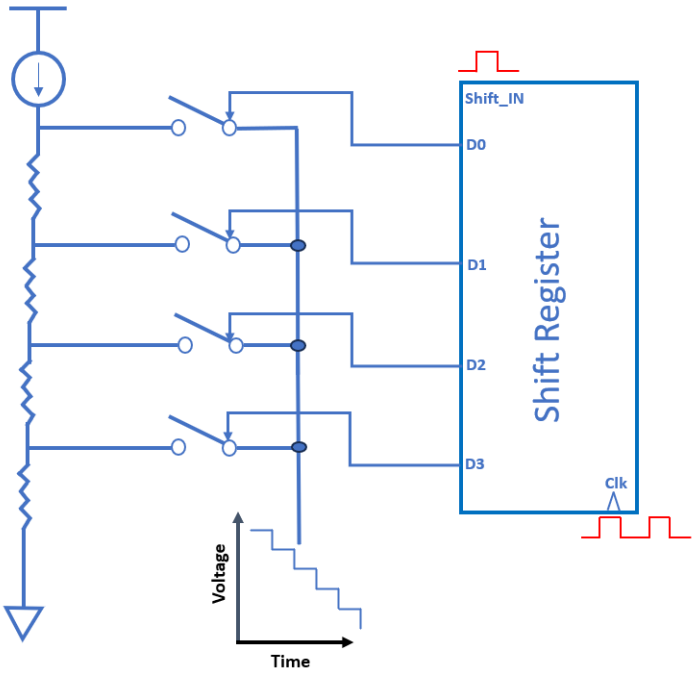

Figure 2.6: Shift Register Based Topology for Ramp Generators

Chapter 3

Design Procedure

The approach to the design was such that it was taken in two stages, the first being the implementation of the first stage of the passive ramp generator and testing out it's performance according to the given specifications over PVT before connecting it to the buffer and subsequently the output load. And so the design was done so that it fulfills the specification with a reasonable margin so that when the buffer and the output load are connected they do not deteriorate the performance too much and we still remain within the given specifications. The overall architecture of the first-stage is shown in figure 3.1. So in principle we wish to implement the current source shown in figure 2.1 with capability of it being programmed so that it can fulfill the requirement of the slope range from 125mV/µs to 2000mV/µs, this is done by using a cascoded current mirror[18] configuration which can provide high output impedance, an essential factor for the linearity requirement, and also it can provide good matching between the bias current and the mirrored current which is essential for maintaining the accuracy of the slope value over PVT. Signals $\overline{B0} - \overline{B4}$ are digital bits which are supplied to switches SW_0-SW_4 which are chosen as PMOS switches since we will start ramping down from the supply, this enables the current source to be programmed over the entire slope range, for example a digital value of 1 would correspond to the switch SW_0 to be closed, this would connect the the top plate of capacitor 'C' to the cascode configuration of M1 and M2 and this would generate the ramp slope of 125mV/µs, accordingly in this way the transistors from M2-M10 are scaled in a binary fashion so that we can cover the entire slope range in steps of 125mV/µs. The switch SW_{reset} is the reset switch to set the capacitor to the supply voltage before ramping.

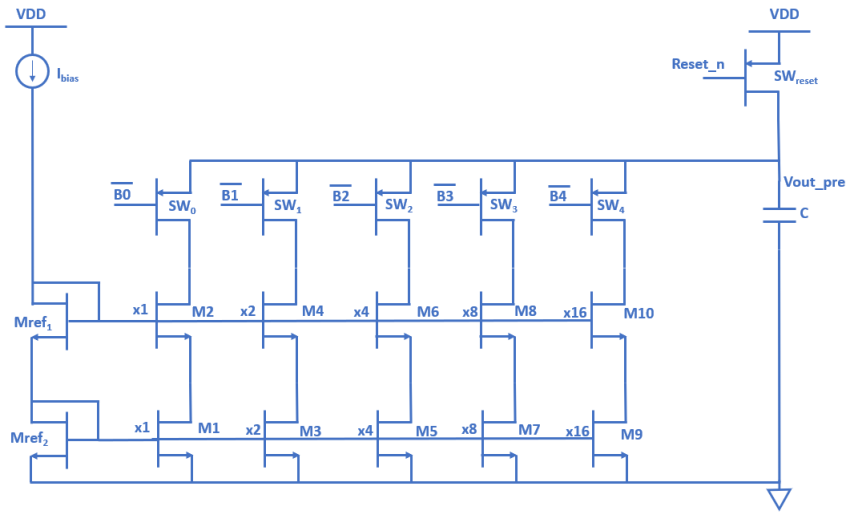

Figure 3.1: First Stage of Ramp Generator.

3.1 Device Sizing

The transistors used for the design are "egslvtnfet" and "egslvtpfet" which are the I/O transistors in the technology, and the capacitor used is the "apmom1v8" metal-on-metal capacitor. To reduce the area and power consumption the device sizes should be minimized which includes the capacitor size and the transistor sizes.However the noise specifications limits us to choosing a capacitor value with a reasonable size and then accordingly select the bias current to attain the slope value.Flicker noise and thermal noise are the two major sources of noises in this circuit,however at the beginning of our analysis we can ignore the effect of flicker noise since it is almost cancelled out by the technique of CDS in CMOS Image Sensors, but the design procedure is such that if in the future we see flicker noise contributing a significant portion of noise power in the frequency range of 200kHz-1GHz, then we will have the liberty to come back and upscale our device sizes. In the context of flicker noise we are mainly referring to the device sizes of $Mref_1$,$Mref_2$ and M1-M10, which will be selected with their minimum widths and lengths of 160nm and 150nm for the beginning of the design phase.That leaves us to only deal with thermal noise from the current mirror combination and the reset switch SW_{reset}.

3.1.1 Noise Analysis

Before running the simulations to size the capacitor, hand analysis was done to see the impact of various noise sources on the output, after doing such an analysis it was predicted that the current mirror combination only contributes minimal noise when compared to the noise of the reset switch SW_{reset}. This analysis is presented in more detail below:

Noise Model for the current mirror configuration

If we ignore the noise contribution of the cascode device then the thermal noise model for the current mirror configuration is shown in figure 3.2, this is taken from[18]

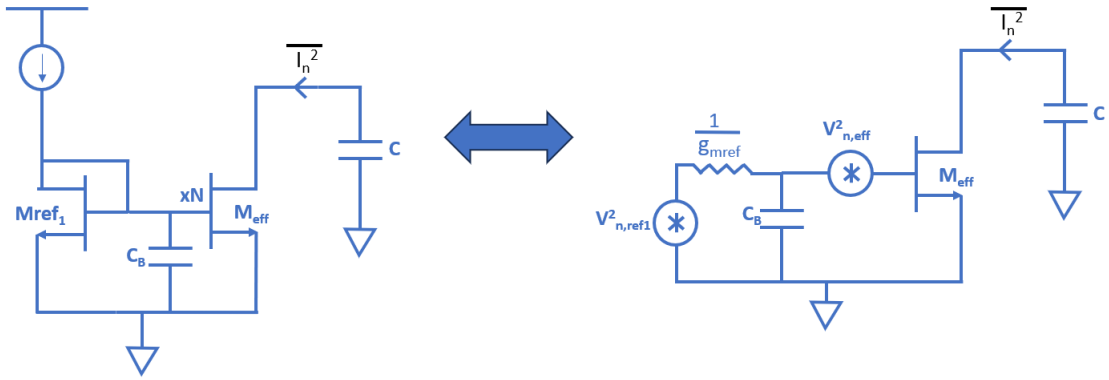

Figure 3.2: Noise Model for Current mirror configuration

It is shown in [18] that the noise current at the output(without the capacitor load 'C') is given by:

$$I_n^2 = (\frac{g_{mref1}^2}{C_B^2\omega^2 + g_{mref1}^2} V_{n,ref1}^2 + V_{n,eff}^2) g_{meff}^2 \tag{3.1}$$

When dealing with thermal noise only, the gate-reffered noises $V_{n,ref1}^2$ and $V_{n,eff}^2$ will take the form of $\frac{4kT\gamma}{g_{mref1}}$ and $\frac{4kT\gamma}{g_{meff}}$ respectively, we also have to consider that in our case with the capacitor connected at

the output our noise at the output is $V^2_{n,out,CM} = I^2_n \frac{1}{(\omega C)^2}$. Substituting for $\omega = 2\pi f$ and carrying out the aforementioned operations yields the expression for the thermal noise power at the output as:

$$V^2_{n,out,CM} = \frac{kT\gamma}{\pi^2 f^2 C^2}\left(\frac{g_{mref1}}{C_B^2 4\pi^2 f^2 + g^2_{mref1}} + \frac{1}{g_{meff}}\right)g^2_{meff} \tag{3.2}$$

It is also worthy to note that in the context of ramp generation we are not dealing with a continuous time noise system, in the sense that the ramp does not continue forever, we generate a ramp and then reset the system by the charging the output to the supply, this is an example of a cyclo-stationary system described in [19] and [20], so then for the purpose of exactness we must multiply out equation 3.2 by the duty-cycle of the system "m"(0.5 in our case) and thus the final equation for the output thermal noise is:

$$V^2_{n,out,CM} = \frac{mkT\gamma}{\pi^2 f^2 C^2}\left(\frac{g_{mref1}}{C_B^2 4\pi^2 f^2 + g^2_{mref1}} + \frac{1}{g_{meff}}\right)g^2_{meff} \tag{3.3}$$

We integrate equation 3.3 to get the total Noise Power from the current mirror, since it is a quite complex integral to solve we use the software from [21] to solve the equation, the result is as follows:

$$\begin{aligned}&\int_{f_1}^{f_2} \frac{mkT\gamma}{\pi^2 f^2 C^2}\left(\frac{g_{mref1}}{C_B^2 4\pi^2 f^2 + g^2_{mref1}} + \frac{1}{g_{meff}}\right)g^2_{meff}\, df \\ &= \frac{-2mkT\gamma}{\pi^2 C^2}\left(\frac{1}{f}\Big|_{f_1}^{f_2} + g_{mref1}g^2_{meff}\left(\frac{C_B 2\pi tan^{-1}\left(\frac{C_B 2\pi f}{g_{mref1}}\right)}{g^{\frac{3}{2}}_{mref1}} - \frac{1}{g_{mref1}}\Big|_{f_1}^{f_2}\right)\right)\end{aligned} \tag{3.4}$$

We also recognize the following relationships:

$$g_{meff} = N g_{mref1} \tag{3.5}$$

$$C_B \approx C_{ox} W_{mref1} L_{mref1} (N+1) \tag{3.6}$$

Substituting the above relationships in equation 3.4 and evaluating the integral at f_1 and f_2 gives us the following:

$$V^2_{n,out,CM} = \frac{-2mkT\gamma}{\pi^2 C^2}\beta \tag{3.7}$$

where β is given by

$$\begin{aligned}\beta = &\left(\frac{1}{f_2} - \frac{1}{f_1}\right)(1 + N g^2_{mref1}) + N g^{\frac{3}{2}}_{mref1} C_{ox} W_{mref1} L_{mref1} (N+1) 2\pi \left(tan^{-1}\left(\frac{C_{ox} W_{mref1} L_{mref1} (N+1) 2\pi f_2}{g_{mref1}}\right)\right. \\ &\left. - tan^{-1}\left(\frac{C_{ox} W_{mref1} L_{mref1} (N+1) 2\pi f_1}{g_{mref1}}\right)\right)\end{aligned} \tag{3.8}$$

Noise Model for the reset switch SW_{reset}

This is a simple sampling switch model depicted in the figure 3.3, this is simpler to analyze than the current mirror noise model, since the noise power is just $\frac{kT}{C}$[18], for exactness we can include the effect of the cyclo-stationary nature of the system where the duty cycle is taken into account but for now we ignore it and we take it into account later:

$$V_{n,out,sw}^2 \approx \frac{kT}{C} \tag{3.9}$$

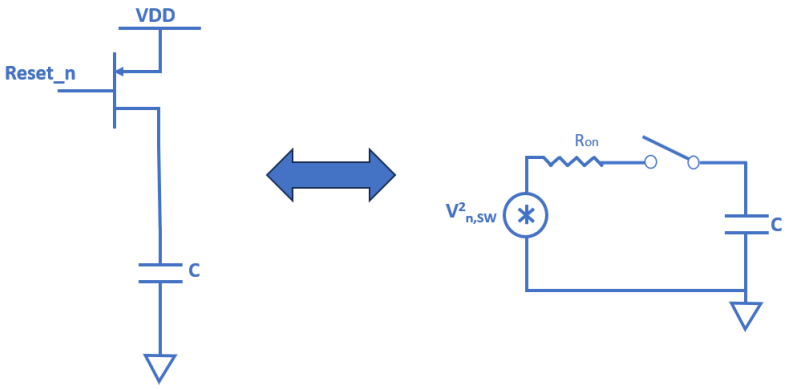

Figure 3.3: Noise Model for the reset switch.

After obtaining the noise expressions from the reset switch and the current mirror combination, we can superimpose them to get the expression for the total output noise power which is:

$$\begin{aligned} V_{n,out,total}^2 &\approx V_{n,out,CM}^2 + V_{n,out,sw}^2 \\ &\approx \frac{-2mkT\gamma}{\pi^2 C^2}\beta + \frac{kT}{C} \end{aligned} \tag{3.10}$$

Now the capacitor 'C' could be sized appropriately for the given noise specification, and in doing so the numbers would reveal that the noise from the current mirror is very negligible when compared to the noise from the switch as mentioned before.

According to the noise specification:

$$\begin{aligned} V_{n,out,total,rms} &\leq 20\mu V \\ V_{n,out,total}^2 &\leq 400\mu V^2 \end{aligned} \tag{3.11}$$

So the minimum size for the capacitor can be determined by the equation 3.10:

$$\begin{aligned} \frac{kT\pi^2 C_{min} - 2mkT\gamma\beta}{\pi^2 C_{min}^2} &= 400\mu V^2 \\ kT\pi^2 C_{min} - 2mkY\gamma\beta &= (400\mu V^2)\pi^2 C_{min}^2 \\ C_{min}^2(400\mu V^2\pi^2) + C_{min}(-kT\pi^2) + 2mkT\gamma\beta &= 0 \end{aligned} \tag{3.12}$$

We see that equation 3.12 results in a quadratic equation of the form $aC_{min}^2 + bC_{min} + c = 0$, where:

$$a = (400\mu V^2)\pi^2$$
$$b = -kT\pi^2 \tag{3.13}$$
$$c = 2mkT\gamma\beta$$

Then we can determine the value of C_{min} by the quadratic formula:

$$C_{min} = \frac{-b \pm \sqrt{b^2 - 4ac}}{2a}$$

Before plugging in terms into the quadtratic formula we must find the value of β in equation 3.8, and to find β we must know $C_B = C_{ox}W_{ref}L_{ref}(N+1)$,$f_1$(start frequency),$f_2$(end frequency),$g_{mref1}$ and N. For simplicity we select the bias current I_{bias} to be $1\mu A$ which is yet to be determined, and although we initially stated that we are going to use minimum dimensions for the current mirror configuration at the beginning phase of the design, again for simple calculation we use dimensions of $1\mu m \times 1\mu m$. The value of N is chosen to be 16 since that is the configuration with the most number of transistors in it and it is more likely to get the maximum noise in that configuration. The value of f_1 and f_2 in 3.8 are the starting and ending frequency boundaries which in our case are 200kHz and 1GHz, so now we have the values below which we need to plug in equation 3.8.

$$\begin{aligned}
&N = 16\\
&W_{ref} = 1\mu m\\
&L_{ref} = 1\mu m\\
&C_{ox} = 5.57 \times 10^{-3}(determined\ from\ simulation)\\
&C_B = C_{ox}W_{ref}L_{ref}(N+1)\\
&C_B = (5.57 \times 10^{-3})(160 \times 10^{-}9)(150 \times 10^{-}9)(17)\\
&C_B = 2.27 \times 10^{-}15F\\
&g_{mref1} = 20 \times 10^{-6}S(determined\ from\ simulation)\\
&f_1 = 200kHz\\
&f_2 = 1GHz
\end{aligned} \tag{3.14}$$

Plugging in the above values in 3.8 yields a value of $\beta = -5 \times 10^{-6}$.

Substituting for 'a' , 'b' and 'c' in 3.12 yields:

$$C_{min} = \frac{kT\pi^2 \pm \sqrt{k^2T^2\pi^4 - 4(400\mu V^2\pi^2)(2mkT\gamma\beta)}}{2\pi^2(400\mu V^2)} \tag{3.15}$$

m is 0.5, γ is $\frac{2}{3}$(approximately) and we will evaluate at a temperature of 125°C(398K).First Evaluating the term inside the square-root gives us:

$$\begin{aligned}
&kT^2\pi^2 - 4(400\mu V^2\pi^2)(2mkT\gamma\beta)\\
&(1.38 \times 10^{-23})(398)^2\pi^2 - 4(400 \times 10^{-12}\pi^2)(2(0.5)(1.38 \times 10^{-23})(398)(\frac{2}{3})(-5 \times 10^{-6}))\\
&= (2.16 \times 10^{-17}) + 1.45 \times 10^{-29}
\end{aligned} \tag{3.16}$$

The second term of the value 1.45×10^{-29} is insignificant and is a consequence of the second term under the square root, this means that we can simplify 3.15 to:

$$C_{min} = \frac{kT\pi^2 \pm \sqrt{k^2T^2\pi^4}}{2\pi^2(400\mu V^2)}$$

$$C_{min} = \frac{2kT\pi^2}{2\pi^2(400\mu V^2)} \tag{3.17}$$

$$C_{min} = \frac{kT}{400\mu V^2}$$

This implies that :

$$V^2_{n,out,total} = \frac{kT}{C} \tag{3.18}$$

The above result is an important result since it tells us that the current-mirror configuration contributes negligible amount of noise at the output when compared to the reset switch SW_{reset}, and thus we only need to consider the noise from the reset switch when sizing our capacitor, below now we also take into account the duty cycle which we ignored in the beginning for the reset switch:

$$C_{min} = m\frac{kT}{V^2_{n,out,total}}$$

$$C_{min} = (0.5)\frac{(1.38 \times 10^{-23})(398)}{400 \times 10^{-12}} \tag{3.19}$$

$$C_{min} = 6.86pF$$

We size the capacitor to be then 7pF, of course we give us the liberty to scale this value up when we simulate over corners or when we include the buffer in our final design.Now that we have our capacitor sized, we can select the biasing current I_{bias} according the slope requirement:

$$\begin{aligned} Slope &= \frac{I_{bias}}{C} \\ I_{bias} &= Slope \times C \\ I_{bias} &= (125mV/\mu s)(7pF) \\ I_{bias} &= 875nA \end{aligned} \tag{3.20}$$

Now that we have our noise and slope requirement satisfied at least in our hand analysis, we need to look at our INL requirement, the output impedance of the cascode is the major factor in determining the INL, the higher the the output impedance the more better the INL performance, we would now proceed to do a more rigorous analysis to derive an expression for INL.

3.1.2 INL Analysis

We wish to derive the profile of how a real ramp looks like when subject to a finite output impedance 'r_o' as shown in figure 3.4, this would help in determining the INL expression from which we can determine the minimum 'r_0' for the given specification.

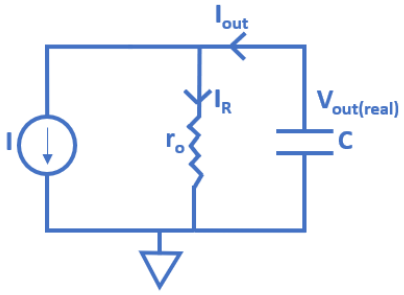

Figure 3.4: Real Model of Ramp Generator

KCL at the output node:

$$I_{out} = I + I_R \tag{3.21}$$

Output voltage:

$$V_{out(real)} = I_R r_o \tag{3.22}$$

Output current can also be expressed as:

$$I_{out} = -C\frac{dV_{out(real)}}{dt} \tag{3.23}$$

Substituting for I_R in 3.21 from 3.22 and then plugging in that expression in place of I_{out} yields:

$$C\frac{dV_{out(real)}}{dt} + \frac{V_{out(real)}}{r_o} + I = 0 \tag{3.24}$$

Solution to the differential equation in 3.24 is:

$$V_{out(real)} = Ae^{-\frac{t}{Cr_o}} - Ir_o \tag{3.25}$$

The constant 'A' can be determine by the initial condition, since we are ramping down from the power supply, then we can say that at t=0 $V_{out(real)} = V_{DD}$, plugging this in 3.25, gives the value of 'A' as:

$$A = V_{DD} + Ir_o \tag{3.26}$$

Thus our final solution is:

$$V_{out(real)} = (V_{DD} + Ir_o)e^{\frac{-t}{Cr_o}} - Ir_o \tag{3.27}$$

To calculate the INL_{max} shown in figure 2.4 we need to determine the difference between the real ramp shown in 3.27 and the straight ramp connecting the two end points of the real ramp which is shown in figure 2.4, although the starting point need not be V_{DD} for simplicity of analysis we assume that our region of interest is from V_{DD} to $V_{DD} - 1$ giving us a voltage swing of 1V, the straight line equation is then:

$$V_{straight} = -\frac{t}{t_2} + V_{DD} \tag{3.28}$$

Where t_2 is the end time point of the ramp, the starting time point is from 0.

t_2 can be determined from equation 3.27 by setting $V_{out(real)}(t = t_2) = V_{DD} - 1$, this evaluates to:

$$t_2 = Cr_o ln(1 - \frac{1}{V_{DD} + Ir_o}) \tag{3.29}$$

The difference between the straight line and real ramp is:

$$V_{straight} - V_{out(real)} = [-\frac{t}{t_2} + V_{DD}] - [(V_{DD} + Ir_o)e^{\frac{-t}{Cr_o}} - Ir_o] \tag{3.30}$$

To obtain the INL_{max} we set the derivative of 3.30 to zero and evaluate the expression for t_{cr} which is the critical time where we hit INL_{max}:

$$\frac{d(V_{straight} - V_{out_{real}})}{dt} = 0$$

$$[-\frac{1}{t_2}] - [-\frac{1}{Cr_o}(V_{DD} + Ir_o)e^{-\frac{t_{cr}}{Cr_o}}] = 0$$

$$\frac{1}{Cr_o}(V_{DD} + Ir_o)e^{-\frac{t_{cr}}{Cr_o}} = \frac{1}{t_2}$$

Substituting in for t_2:

$$(V_{DD} + Ir_o)e^{\frac{t_{cr}}{Cr_o}} = -\frac{Cr_o}{Cr_o ln(1 - \frac{1}{V_{DD}+Ir_o})} \tag{3.31}$$

$$e^{-\frac{t_{cr}}{Cr_o}} = -\frac{1}{(V_{DD} + Ir_o)ln(1 - \frac{1}{V_{DD}+Ir_o})}$$

$$-\frac{t_{cr}}{Cr_o} = ln[\frac{1}{(V_{DD} + Ir_o)ln(1 - \frac{1}{V_{DD}+Ir_o})}]$$

$$t_{cr} = -Cr_o ln[\frac{-1}{(V_{DD} + Ir_o)ln(1 - \frac{1}{V_{DD}+Ir_o})}]$$

We plug t_{cr} back into equation 3.30 to get the maximum between the real and the straight line:

$$(V_{straight} - V_{out(real)})_{max} = [-\frac{t_{cr}}{t_2} + V_{DD}] - [(V_{DD} + Ir_o)e^{\frac{-t_{cr}}{Cr_o}} - Ir_o]$$

$-\frac{t_{cr}}{t_2}$ above is given by:

$$-\frac{t_{cr}}{t_2} = -\frac{ln[\frac{-1}{(V_{DD}+Ir_o)ln(1-\frac{1}{V_{DD}+Ir_o})}]}{ln(1-\frac{1}{V_{DD}+Ir_o})}$$

$e^{-\frac{t_{cr}}{Cr_o}}$ is given by:

$$e^{-\frac{t_{cr}}{Cr_o}} = e^{ln[\frac{-1}{(V_{DD}+Ir_o)ln(1-\frac{1}{V_{DD}+Ir_o})}]} = \frac{-1}{(V_{DD}+Ir_o)ln(1-\frac{1}{V_{DD}+Ir_o})}$$

Plugging back $-\frac{t_{cr}}{t_2}$ and $e^{-\frac{t_{cr}}{Cr_o}}$ gives us:

$$(V_{straight} - V_{out(real)})_{max} = -\frac{ln[\frac{-1}{(V_{DD}+Ir_o)ln(1-\frac{1}{V_{DD}+Ir_o})}]}{ln(1-\frac{1}{V_{DD}+Ir_o})} + V_{DD} + \frac{1}{ln(1-\frac{1}{V_{DD}+Ir_o})} + Ir_o$$

$$(V_{straight} - V_{out(real)})_{max} = \frac{1 - ln[\frac{-1}{(V_{DD}+Ir_o)ln(1-\frac{1}{V_{DD}+Ir_o})}]}{ln(1-\frac{1}{V_{DD}+Ir_o})} + V_{DD} + Ir_o \tag{3.32}$$

$INL_{max}(\%)$ is $(V_{straight} - V_{out(real)})_{max}$ normalized by the voltage swing which is just 1V, hence $INL_{max}(\%) = (V_{straight} - V_{out(real)})_{max}$, so our expression for $INL_{max}(\%)$ is:

$$INL_{max}(\%) = \frac{1 - ln[\frac{-1}{(V_{DD}+Ir_o)ln(1-\frac{1}{V_{DD}+Ir_o})}]}{ln(1-\frac{1}{V_{DD}+Ir_o})} + V_{DD} + Ir_o \tag{3.33}$$

Our INL specification is $INL_{max}(\%) \leq 0.01$,so we can calculate minimum output resistance r_{omin} required to for $INL_{max}(\%) = 0.01$ as:

$$0.01 = \frac{1 - ln[\frac{-1}{(V_{DD}+Ir_{omin})ln(1-\frac{1}{V_{DD}+Ir_{omin}})}]}{ln(1-\frac{1}{V_{DD}+Ir_{omin}})} + V_{DD} + Ir_{omin} \tag{3.34}$$

Unfortunately the equation in 3.34 is a non-linear equation and so can not be solved using analytical methods, one can use numerical methods such as the Newton-Raphson method. However in our case we used a much more simpler approach, since we already knew that a high output impedance on the order of $\sim M\blacksquare$ would give a good INL performance we started plugging in for r_{omin} in equation 3.34 starting from the value of $1M\blacksquare$ and then gradually increasing or decreasing the value according to weather we are under or overestimating, after a few iterations it was observed that choosing a value for $romin = 800k\blacksquare$ gave us a value for $INL_{max}(\%) = 0.0097$ which is just under our requirement of 0.01.The value of 'I' used is 14µA since it is the maximum current drawn from the capacitor at the steepest ramp, we have taken this value because we know that the output impedance of the cascode is inversely proportional to the biasing current

$(r_o \sim \frac{1}{I})$ and so the r_{omin} obtained would be of the worst case scenario, V_{DD} is 1.8V. We then check from simulations that choosing the minimum lengths for the transistors in the cascode configuration has a greater output impedance than the computed value of r_{omin} when the branch is carrying the highest current. The result of the simulated output impedance with minimum channel length is shown in figure 3.5, it can be seen that the the worst case output impedance is about $76M\Omega$ at a temperature of $125°$C at the ff corner, so we conclude that the minimum channel length is sufficient enough to fulfill our INL requirement.

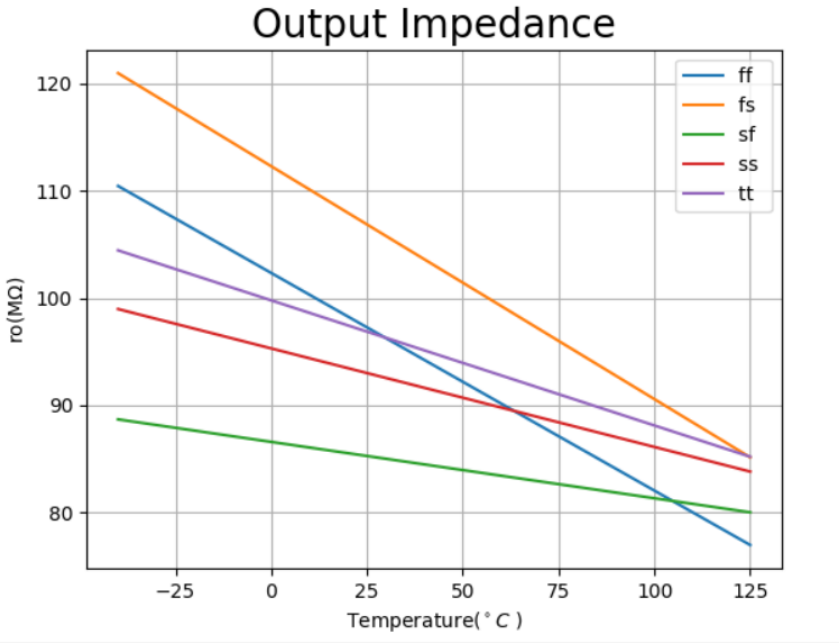

Figure 3.5: Output Impedance over PVT

Voltage Swing

We also need to ensure that the cascode transistors in the circuit in figure 3.1 remain in saturation as we discharge node Vout_pre from 1.8V to 800mV, the minimum voltage that is required to keep the cascode transistors in saturation is approximately $V_{OD(Mref1)} + V_{OD(Mref2)} + V_{thn}$, this value is checked in simulations over temperature and corners and is shown in figure 3.6, it can be seen that the highest voltage is around 730mV at the ss corner at a temperature $-40°$C, since this is less than 800mV so we do not need to increase the unit width of the transistors further to reduce the the overdrive voltages neither we need to switch to a different architecture such as the high-voltage swing cascode mirror[18] which would require more transistors and current to generate the necessary bias voltage.

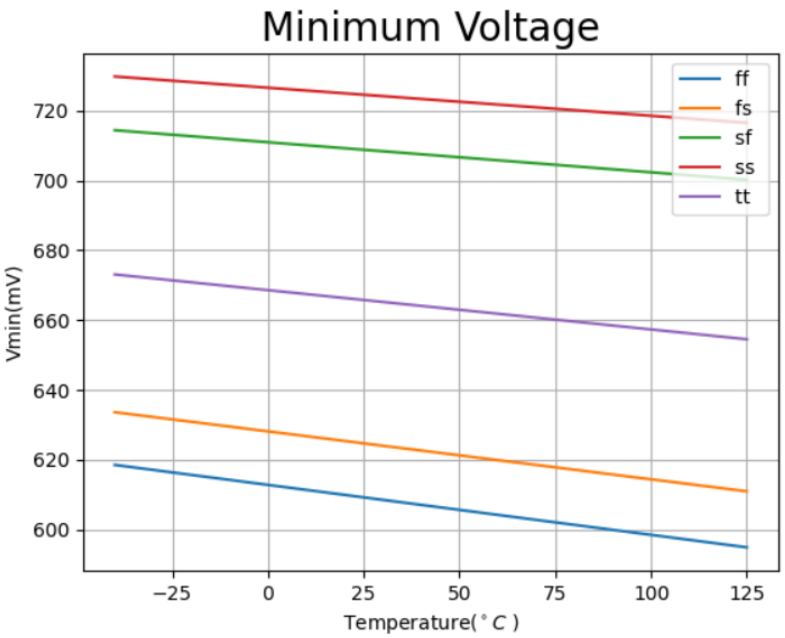

Figure 3.6: Minimum Voltage over PVT

3.2 First Stage Simulation results

Before designing the buffer we check the performance of our first stage ramp generator, this would aid us in verifying our initial hand analysis and also aid us in designing the buffer, the final results after the inclusion of the buffer are presented in chapter 4.

3.2.1 Slope Accuracy

Although the error in the slope is not bounded by any specification in this thesis it is still important to report the findings.We mention the results obtained for the slowest and fastest ramp that is $125mV/\mu s$ and $2000mV/\mu s$ over all corners and in the temperature range of $-40°$C-$125°$C, the results are shown in table 3.1, it can be seen that the mean value is close to the required ideal value however the the min and max values deviate quite a bit with the maximum deviation being around 12% in the case of the steepest slope.

Slope Magnitude(Required)(mV/µs)	**Min(mV/µs)**	**Max(mV/µs)**	**Mean(mV/µs)**
125	108	147	125.4
2000	1763	2243	2000

Table 3.1: Slope accuracy from first stage

3.2.2 Noise Result

The maximum noise value obtained after simulation was $14\mu V_{rms}$ at $125°$C, of which about 94% of the noise was thermal noise coming from the reset switch SW_{reset}.

3.2.3 INL Result

The results for $INL_{max}(\%)$ were obtained over all corners and a temperature range of $-40°$C-$125°$C. The results are shown in table 3.2

INL_{max}**(Required)(%)**	**Min(%)**	**Max(%)**	**Mean(%)**
0.01	0.00028	0.0007	0.00053

Table 3.2: INL Results from first stage

3.3 Final Device Sizes

After the obtaining the simulation results we can finalize the device sizes in figure 3.1, the unit transistor widths and lengths of M_{ref1} and M_{ref2} are kept to their minimum dimensions of 160nm and 150nm respectively, the switches from $SW_0 - SW_4$ were sized such that they provide a low on resistance, so a high $\frac{W}{L}$ was needed, the lower limit to this value was set by the branch carrying the highest current, which is the branch of SW_4, because SW_4 will have the highest voltage drop across it and it will cause the cascode transistor to be more nearer to the triode region,thereby decreasing its output impedance which eventually would degrade our INL performance, so the switch SW_4 was sized such that it has a high enough $\frac{W}{L}$ so that we can stay within the INL specification, this value was determined during the process of simulating for INL, and the lower limit was identified as 2µm/150nm, the rest of the switches from $SW_0 - SW_3$ were also given the same dimensions. The reset switch SW_{reset} dimensions were constrained by the minimum time that was required to reset the capacitor 'C' before the next ramp cycle, a $\frac{W}{L}$ ratio of 1µm/150nm was found to be adequate.The capacitor 'C' is sized at $50\mu m \times 46\mu m$ for a 7pF capacitance.

3.4 Buffer Design

The whole purpose of the buffer is to drive the huge capacitor load at the output without degrading the linearity, this can be achieved by providing a very low output impedance at the output, but the question is how low. To find this answer the author had two options, one option was to perform a full exact mathematical analysis to derive an expression for the INL_{max} at the buffer's output, this is what we did for the first stage, or the second option was to rely on the simulator and find the optimum value through it. The author went with the second option as an exact mathematical analysis was extremely complicated. In the simulation method, we have our buffer model as shown in figure 3.7 consisting of a dependent voltage source with gain "A", an AC coupling capacitor and a output resistance of R_{out}, our input is the ramp output of the first stage. The ac coupling capacitor is simply included in the model to seperate the DC points of V_{out} and V_{out_pre}, which would be the case in the real buffer, the input ramp from the first stage is selected at the corner and temperature where we were getting the worst INL performance. To find the required value of R_{out} we inject out first stage ramp signal at the input, we sweep R_{out} at low values from $30 - 100\Omega$ and plot INL_{max} against it, the gain "A" is chosen to be 0.9(a reasonable value for a non-ideal buffer), the result is shown in figure 3.8, from the figure it can be seen that we require an output resistance of about 35Ω to meet or maintain our INL specification from the first stage.Three buffer topologies were considered all of which have the capability to provide the required output impedance but with each having certain merits and demerits. The three buffer topologies included a flipped voltage follower(FVF)[22], a unity gain buffer using an opamp and a simple source follower.The FVF and the unity gain buffer have the advantage of providing a low output impedance(through the use of feedback) at a lower power consumption than the source-follower, hence they were more attractive ot the author and the first to be tried and tested. The FVF was rejected after an initial hand analysis, the opamp unity gain buffer was tried and tested in simulations but was ultimately rejected due to it's excessive noise contribution at the output, finally the source follower was chosen which was able to meet all the specification simultaneously across PVT. We will now focus on each of the three architectures and emphasize on the merits and de-merits of each of them.

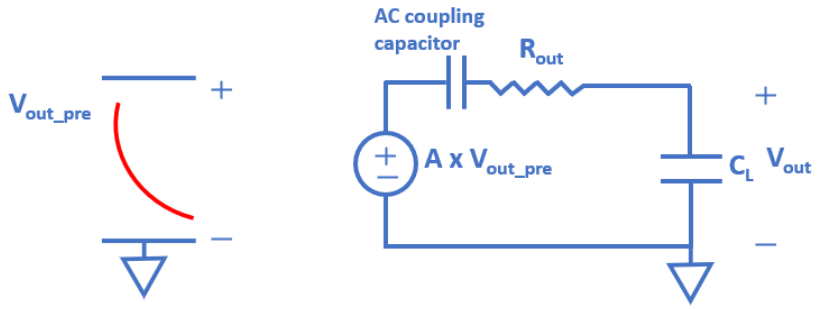

Figure 3.7: Simulation to calculate R_{out}

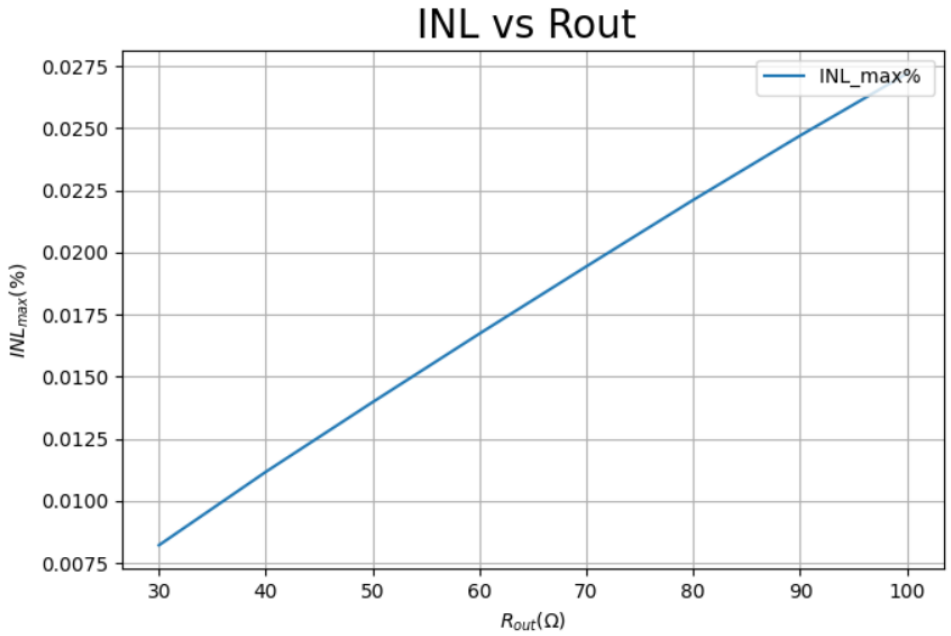

Figure 3.8: $INL_{max}(\%)$ vs R_{out}

3.4.1 Flipped Voltage Follower

A good buffer must have a very low output impedance(ideally zero), a source follower can accomplish this task but at the expense of burning a lot of power, hence our first choice was for a architecture which is simple in construction than an opamp but can still can provide a very low output impedance at a relatively low current consumption through the use of feedback, the FVF shown in figure 3.9 fulfills that requirement,where the output impedance is given by $\frac{1}{g_{m2}(gm1ro1+1)}$, here we can see that the output impedance of the traditional source follower($\frac{1}{g_m}$) is scaled further down approximately by the intrinsic gain of the device, this intrinsic gain could achieve a reasonable value simply by just increasing the channel length of the device, that way we can get sufficient gain at low biasing current, hence saving power. With all it's advantages the FVF suffers from one major disadvantage which is critical to our application and that is the voltage swing. It will be demonstrated that the voltage swing necessary for our application is not achievable with this architecture. The nfet version of the FVF is chosen instead of the pfet version because we would start ramping from V_{DD}.

The maximum voltage that V_{in} in figure 3.9 can go to is given by:

$$V_{in(max)} = V_{gs2} + V_{th1} \tag{3.35}$$

The minimum voltage is given by:

$$V_{in(min)} = V_{gs1} + V_{OD2} \tag{3.36}$$

Then the voltage swing range is given by:

$$\begin{aligned} V_{in(max)} - V_{in(min)} &= V_{gs2} + V_{th1} - V_{gs1} - V_{OD2} \\ &= V_{gs2} - V_{OD1} - V_{OD2} \\ &= V_{OD2} + V_{th2} - V_{OD1} - V_{OD2} \\ &= V_{th2} - V_{OD1} \end{aligned} \tag{3.37}$$

The above result is disappointing for us since it shows that the voltage swing we can get at the input is a threshold voltage minus an overdrive voltage, the threshold voltage for an nfet device in our case is approximately 400mV, that means that the maximum attainable voltage swing with this architecture would always be less than 400mV. This is considerably insufficient for us as we need a voltage swing of 1V, hence we reject this topology as our choice for buffer.

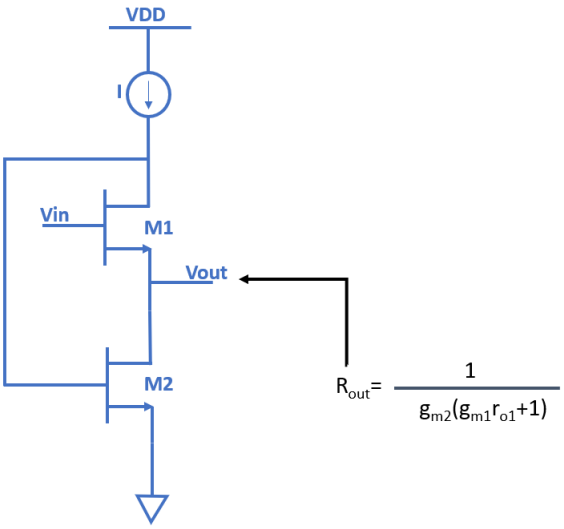

Figure 3.9: FVF

3.4.2 Unity Gain Buffer

The unity gain buffer configuration as shown in figure 3.10 was tried and tested in simulations but was not considered due to it's noise performance, the current mirror opamp[23] was chosen as the opamp architecture, with a pfet source follower as our output stage, a pfet source follower is suitable as an output stage because we need to discharge the load capacitor for the downward ramp and hence sink current. The opamp architecture is shown in figure 3.11,since we need an output resistance of $\leq 35\Omega$ to maintain linearity , we wish to choose an open loop output resistance($\frac{1}{g_{m10}}$) of $1K\Omega$ and an open loop gain(A_v) to be around 30-35dB which will give us a closed loop output resistance of $R_{out} \approx \frac{1}{g_{m10}A_v} \approx 18 - 32\Omega$ which is below 35Ω and we expect the buffer to maintain the linearity.

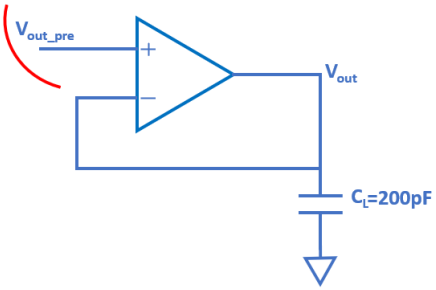

Figure 3.10: Unity Gain Configuration

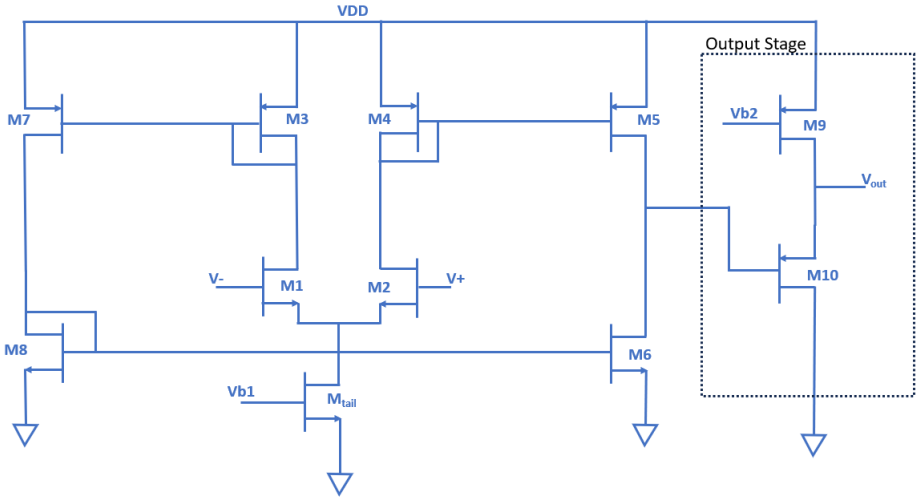

Figure 3.11: Current mirror opamp with output buffer

The device dimensions in figure 3.11 are shown in table 3.3

Device Name	**Width**	**Length**
M1/M2	75µm	150nm
M3/M4	70µm	150nm
M7/M5	70µm	150nm
M8/M6	150µm	150nm
M_{tail}	96µm	150nm
M9	480µm	8µm
M10	120µm	150nm

Table 3.3: Device Dimensions for Opamp

Our goal with the opamp in the unity gain feedback configuration is to stay equal to or below the output

resistance required over the entire temperature range, over all corners and also over voltage swing. For our setup we have chosen the starting bias point at V_{out} as 1.7V and the endppoint as 700mV, so we must ensure that the output resistance is low enough for this entire voltage range.

It is essential to note that the bias current in the output branch is not very well defined over temperature(as observed in simulation), also it varies quite a bit as the output voltage swings from a high voltage near the supply to a lower voltage. However M9 was sized such that lowest current at a particular corner is still sufficient enough to provide a sufficiently low open-loop output resistance, which was $\approx 1.2K\Omega$ with the the output dc voltage at 1.7V, the temperature at $125°C$ and the corner being ss.The variation in the output resistance over PVT and over the voltage swing is shown in figure 3.12,since the closed loop output resistance is given by $R_{out(CL)} \approx \frac{R_{out(OL)}}{A_v}$ where $R_{out(CL)}$ is the closed loop output resistance $R_{out(OL)}$ is the open loop output resistance and A_v is the open loop voltage gain, we must then ensure that in our worst case open loop output resistance of $1.2k\Omega$ the gain is equal to or greater than $A_v = \frac{1.2k\Omega}{R_{out(required)}} = \frac{1.2k\Omega}{35\Omega} \approx 34.3$ which in dB translates to approximately 32 , the open loop gain plot in figure 3.13 shows that if the output voltage is at a high voltage of 1.7V than the gain drops significantly with the temperature and furthermore our requirement for 32dB is not satisfied in fact the gain drops to 27dB, this is the case with every other corner at this temperature and voltage level, this issue is primarily due to fact mentioned above that the bias current in the output stage branch is not well defined by the current source M9 across temperature, and this is illustrated in figure 3.14, this would mean that the source to gate voltage drop across M10 would be quite low at low temperatures and if the output voltage is high then M5 would have a lower source-drain voltage which degrades it's output resistance, this is even the case when we have ensured by sizing M5 appropriately that it stays in saturation at this temperature and output voltage. The variation in this biasing current was mysterious to the author, however dealing with this issue means to increase "$\frac{W}{L}$" of M5 further so that it is in deep saturation and it maintains its high output resistance and we do not degrade our DC gain, but as we will see in the following discussion that this measure was not required. The question is that even if the open-loop gain is not high enough and consequently the closed loop output impedance is not low enough at this output voltage and high temperature can we still get away with this as this will be a momentary condition as we ramp down, to verify this we connected our unity gain buffer to the output of out first stage "V_{out_pre}" in figure 3.1 and simulated for INL performance over PVT at our final output node V_{out}, the results achieved are summarized in table 3.4, it is seen that we are still under the specification and hence we can tolerate the gain degradation at high temperatures at high output voltage levels.

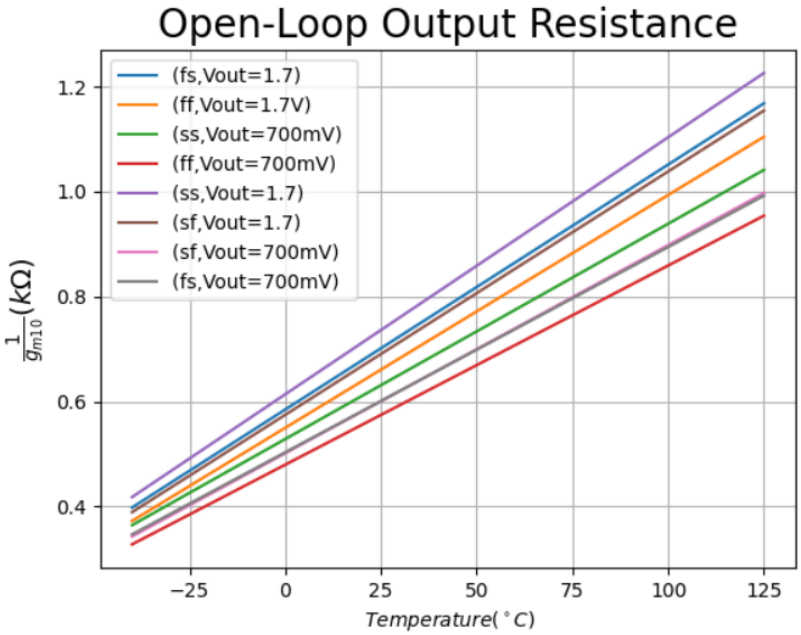

Figure 3.12: Open loop output resistance of the opamp

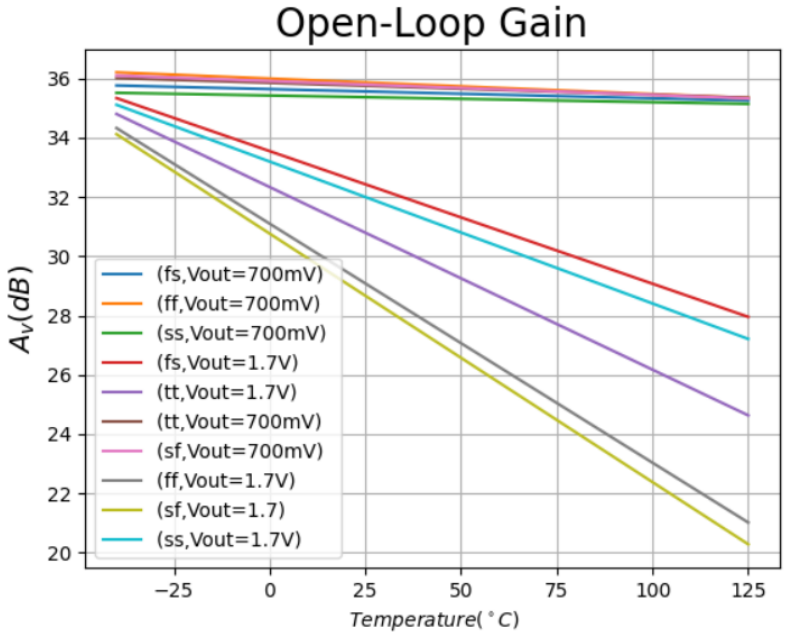

Figure 3.13: Open loop gain of the opamp

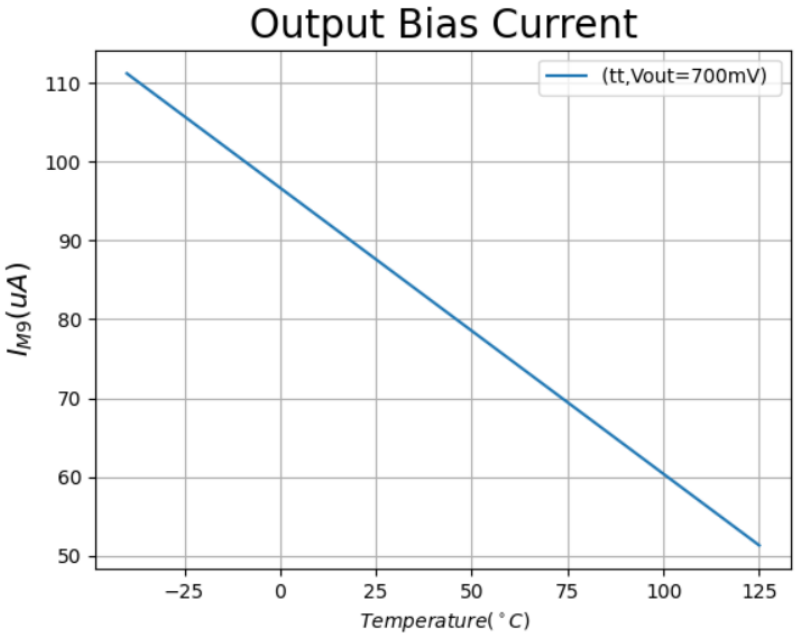

Figure 3.14: Output Bias Current in the output stage

INL_{max}**(Required)(%)**	**Min(%)**	**Max(%)**	**Mean(%)**
0.01	0.001	0.006	0.0019

Table 3.4: INL Measurement with the unity gain buffer.

It is also interesting to see the mechanism by which the buffer ensures that V_{out} follows V_{out_pre} and this is shown in figure 3.15, where we at first see that the slewing action of the opamp brings the output voltage down which was initially at the supply voltage and then the linear feedback action takes over and makes the buffer output track the input from the first stage.The maximum total static current consumption of the opamp is 1.4mA at the ss corner at a temperature of $-40°C$, with M_{tail} carrying a bias current of $600\mu A$, M6 and M8 carrying a current of about $350\mu A$ and the output branch carrying a current of $107\mu A$, and the rest of the current is to generate the biases of Vb1 and Vb2.

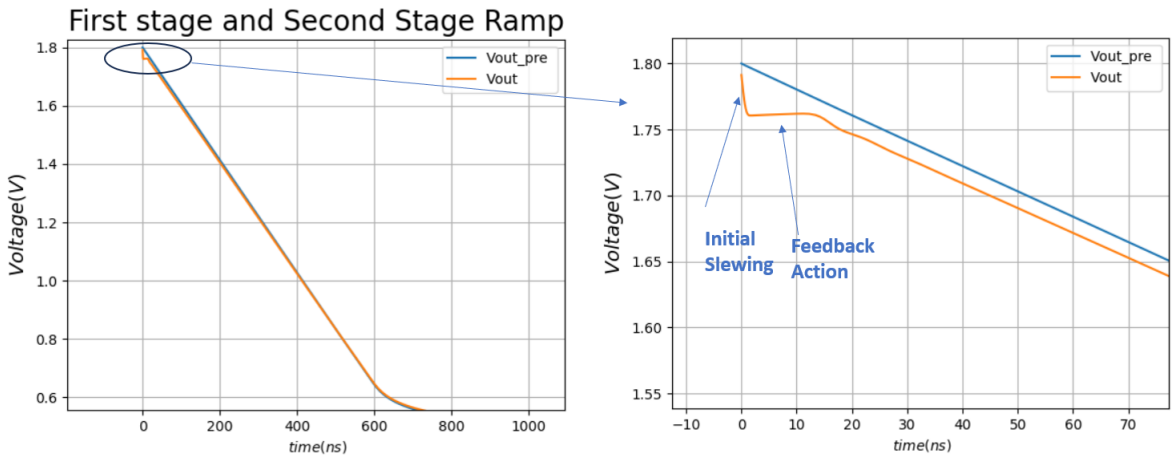

Figure 3.15: Ramp outputs pre and post buffer

Stability

Our initial choice of using the unity gain buffer was to get a low overall output resistance without burning too much static current, however due to stability concerns the biasing current had too still be fairly large. This is due to the high frequency poles formed at the gates of M10, M3 and M4, we are forced to increase the current in the branches containing M3,M4,M5 and M7 to lower the impedances at these nodes and move them further away into the high frequency range, hence the opamp is designed such that much of the gain is extracted from g_{m1} and g_{m2} rather than the output impedances of M5 and M6 hence the channel length is kept minimum for these devices, this ensures stability.As a comparison for stability performance with regards to power consumption we perform an experiment where we decrease the bias tail current in M_{tail} from $600\mu A$ to $100\mu A$ while we increase the channel lengths of M3,M4,M5,M6,M7,M8 from 150nm to 500nm keeping our open loop gain roughly constant and run a transient simulation under nominal conditions to observe the ramp characteristics and then we run a transient simulation under the same conditions but with the original channel lengths and biasing current, the comparison is shown in figure 3.16 where the plot on the left is with low bias current and long channel lengths and the right one is our original design.

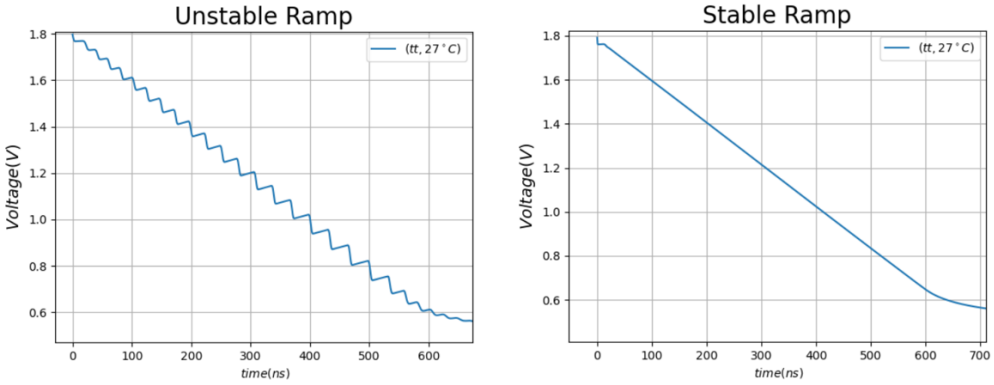

Figure 3.16: Stability Comparison

Noise Issue

The main issue with the unity gain configuration acting as the buffer is it's noise contribution at the output, of which the majority comes from the biasing circuitry, the biasing scheme used to generate Vb1 and Vb2 in figure 3.11 for the opamp is shown in figure 3.17, where we can see that the gate-referred noises of M_{ref2} and N0 travel through a cascade of common source amplifiers until they reache the output, the first stage consists of N0 and P0 and the second one is the output branch of the amplifier in figure 3.11 consisting of M9 and M10, here N0 contributes the major part of the noise(about 70%) since the gate noise of M_{ref2} is filtered by the low pass filter formed by the resistance of the diode connected device M_{ref2} and the capacitance at the node generating Vb2. Flicker noise is the major contributor from N0 since N0 is sized at it's minimum dimensions. One could lower this noise by increasing the dimensions of N0, but there are other sources of noise within the amplifier that also prove problematic, this includes the thermal noise generated from the output transistors M9 and M10 and the flicker noise from M6 which also travels through a common source stage consisting of M5 and M6 and then ultimately through the follower M10 to the output. It is also important to note here that the flicker noise of M6 has a significant contribution even though M6 is a fairly large transistor. In conclusion what we get out as our maximum noise value is $25\mu V(rms)$ which is above our specification.

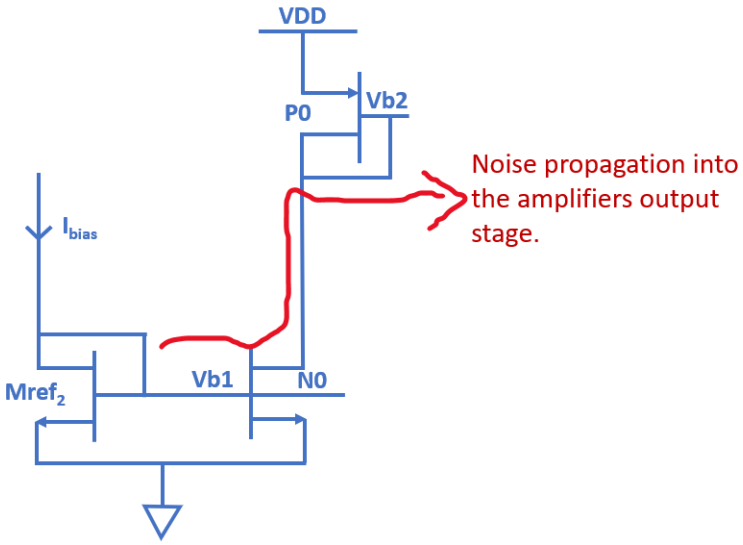

Figure 3.17: Noise Propagation into the opamp

3.4.3 Source Follower

The final choice ultimately made was that of a source follower owing to it's simplicity and noise performance but this was at the cost of more power consumption, the structure is shown in figure 3.18, as shown the follower branch consumes 2mA of current to ensure our INL performance, the device dimensions are shown in table 3.5, for maximum voltage swing at the output we must ensure the node at the gates of M1,M3 and M5 is biased at a voltage that approximately equals $V_{gs3} + V_{OD4}$, however this value would vary over corners so for this we use transistors M2 and M1 to generate the bias voltage[18] where it could be thought of as V_{gs1} generating V_{gs3} and V_{ds2} generating V_{OD4}, and so this configuration would ensure that the bias voltage dynamically adjusts itself over PVT variations if variations in M3 are similar to M1 and variations in M4 are similar to M2.The channel lengths for M4 and M6 are chosen higher than the minimum channel length because it would simultaneously help in increasing the output impedance of the cascode configuration of M6 and M5, and also reduce the flicker noise contribution at the output. It is also important to note that we have chosen two different ideal current sources for biasing(which in reality can be tapped from a Bandgap reference)[23], we have chosen this option over biasing everything from a single current source, as we did with our unity gain buffer where the single current source in figure 3.1 carrying I_{bias} biases everything, the disadvantage of that strategy is that it forms multiple cascades of common source stages seen by the gate-referred noise of M_{ref2}, this was already illustrated in the previous section.The biasing currents must also be of a low value since otherwise they can generate excessive shot and thermal noise at the output, in this case they are chosen to be $1\mu A$.M_{sf} has it's bulk connected to it's source since the body effect would degrade the gain of the source follower.

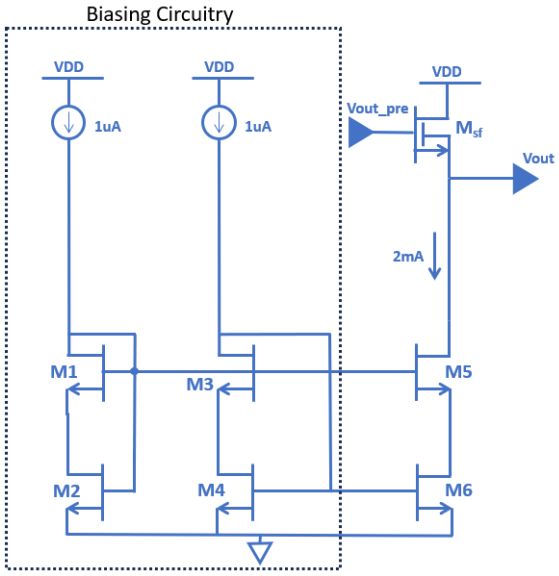

Figure 3.18: Source Follower Implementaion

Device Name	Width	Length
M1	1µm	150nm
M2	1µm	2µm
M3	1µm	150nm
M4	2µm	2µm
M5	200µm x 20	150nm
M6	200µm x 20	2µm
M_{sf}	250µm	150nm

Table 3.5: Device Dimensions for Source Follower

We would now provide justification on the amount of biasing current chosen for the source follower, if we have the dimension of M_{sf} as shown in table 3.5 and we bias the source follower at 2mA under nominal conditions then we have a plot of the output resistance over PVT as shown in figure 3.19, it seen that the variation in the output resistance ranges from about 24Ω to 40Ω.The value 40Ω is slightly larger than 35Ω which was our initial target for getting the INL under specification, however we know that $\frac{1}{g_{Msf}}$ is not the exact output resistance instead it is the parallel combination of this resistance with the resistance of the cascode consisting of M11 and M12 that forms the exact output resistance, and so this parallel combination would further lower the resistance $\frac{1}{g_{Msf}}$ such that it is enough to compensate for the 5Ω above specification . So to conclude, this biasing current gives us the required output resistance.

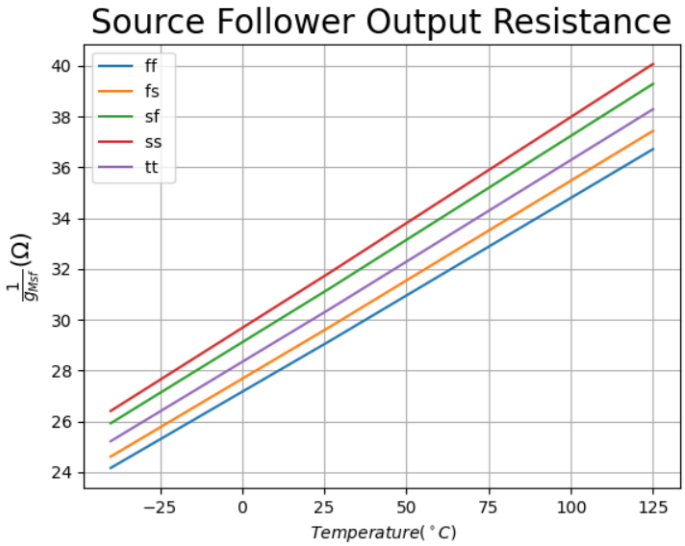

Figure 3.19: Output Resistance of source follower over PVT

Since now we have chosen our buffer topology we can now arrive at the final design shown in figure 3.20, the only change made in the first stage was to decrease the capacitance of C by 0.2pF(the new dimensions are then $50\mu m \times 44.5\mu m$) to accommodate for the parasitic capacitance C_p seen at the gate of M_{sf}.

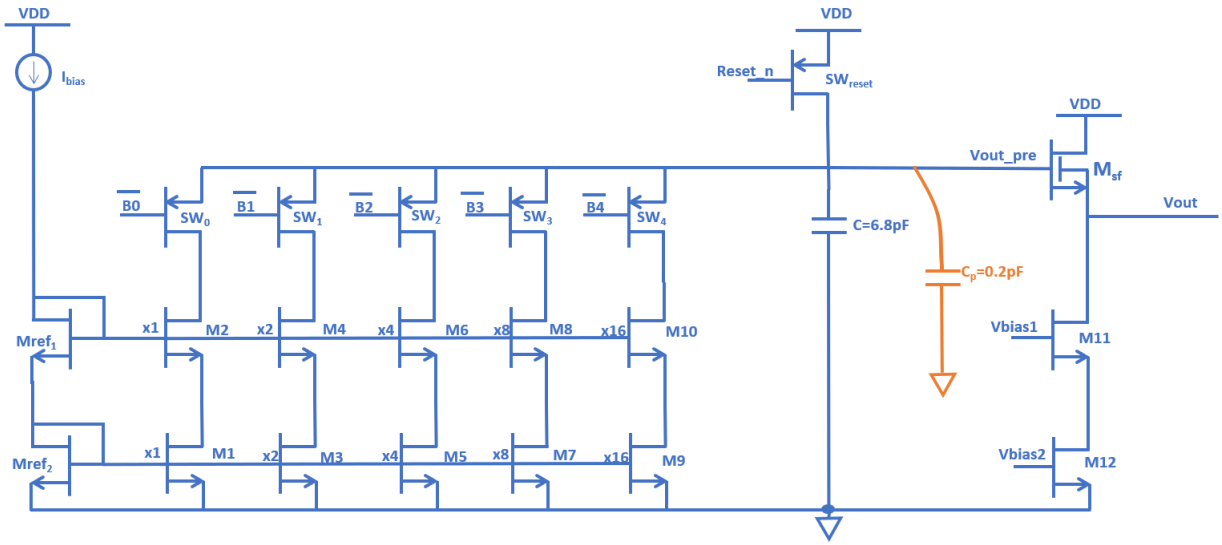

Figure 3.20: Final Design

Choosing starting bias point

Since now the output is isolated from the first stage, we can make our starting bias point selection, we want to make a selection such that that bias point exists over all corners and temperatures, and second to that it should satisfy our INL specification. The ramps obtained at $2000mV/\mu s$ are shown in figure 3.21, it can be seen that the bias point 1.3V exists over all PVT variations and it also ensures our INL specification(checked through simulations), so the final ramp range chosen for the final design is from 1.3V to 0.3V.

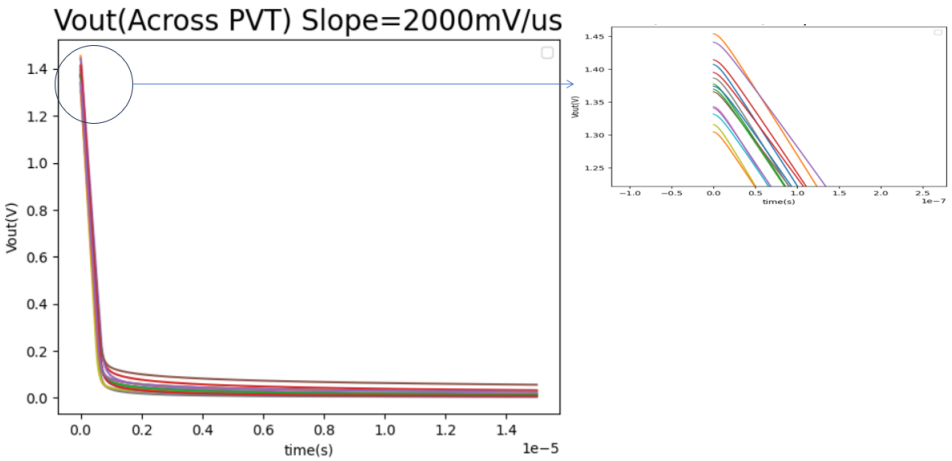

Figure 3.21: Starting bias point selection

Chapter 4

Final Results

The final results are simulated at a supply voltage of 1.8V, over a temperature range of $-40°C$-$-125°C$ and at corners ss,sf,fs and tt.

4.1 Slope Range

4.1.1 Over Corners

We wish to see the slope range coverage from 125mV/µs to 2000mV/µs, and quantify the error over PVT.

Target Slope(mV/µS)	**Mean(mV/µs)**	**Max.error(%)**
125	128	20
250	256	13
375	384	15
500	511.5	11.5
625	639	11.8
750	766	11.1
875	892	12
1000	1019	12.7
1125	1143	11
1250	1266	10.8
1375	1388	9.4
1500	1508	10.2
1625	1626	8.8
1750	1742	9.2
1875	1855	9
2000	1970	11.7

Table 4.1: Slope Measurement across PVT

4.1.2 Mismatch

Montecarlo mismatch simulation was performed on 200 points at a temperature of $27°C$ and at the tt-corner to see how the mismatch effects the slope accuracy, the results are tabulated in table 4.2

Target Slope(mV/µS)	**Mean(mV/µs)**	**Max.error(%)**
125	126.6	56
250	255.8	48
375	381.8	48
500	511	39
625	636	39
750	764	40
875	888	40
1000	1016	47
1125	1138	43.5
1250	1262	44.7
1375	1381	41.5
1500	1503	38.7
1625	1619	36
1750	1735	36.2
1875	1846	33.5
2000	1960	31.4

Table 4.2: Slope Measurement during Mismatch

4.2 Power Consumption

Although no limitation was imposed on the power consumption in the specification, it is still important to report the result. The power consumption was computed as follows, the ramp generator ran for each slope value sequentially and then the average current drawn was computed and ultimately the power.The total maximum average current consumption was 1.955mA of which 1.954mA was consumed by the output buffer and only 1µA was consumed by the first stage. So virtually all the power is consumed by the buffer, which amounted to 3.5mW.

4.3 Noise

The maximum total integrated noise generated at the output was $18\mu V_{(rms)}$ at a temperature of $125°$C.

4.4 INL

The final results for the INL measurement are shown in table 4.3, the voltage swing of 1V is chosen from 1.3V to 0.3V.

INL_{max}**(Required)(%)**	**Min(%)**	**Max(%)**	**Mean(%)**
0.01	0.0023	0.007	0.003

Table 4.3: INL Final Result

Chapter 5

Discussion

This chapter would attempt to compare the performance of the continuous time passive ramp generator built in this thesis with the ones that are already the popular ones.The performance specs for a standalone ramp generator are not found in literature, a general overview is presented in [16], where a continuous time ramp has the advantages of having high resolution, linearity and low power consumption, however as aforementioned there are no real numbers to compare with.The "Passive Continuous Time Ramp Generator" implemented in this thesis however can serve as a vital source of information and results to compare with if established numeric data is available for the current state of the art ramp generators.

5.1 Source Follower vs Unity Gain

When we compare the performance of the Source Follower vs the Unity Gain Buffer then it can be seen from chapter 3 that the Source Follower requires twice as much of bias current for the same level of performance when compared the unity gain topology, the downside however of the unity gain topology was it's noise contribution to the output, however on second glance we notice that the noise was not way ahead of our specification, it was $25\mu V_{rms}$, this value can be brought down by further optimization of the device sizes and biasing currents. If this is done then the unity gain topology is a better topology in terms of power consumption.Although no layout was done in this thesis but we can still have rough estimate of the areas of the two topologies from the device size information in tables 3.3 and 3.5, this is done by adding up all the transistor areas(computed from widths and lengths) in the given tables, for the source follower it amounts to $8643.8\mu m^2$ and for the unity gain configuration it amounts to $3959.4\mu m^2$, so we see that in terms of area performance the unity gain configuration is also superior. So for future implementation of this kind of architecture, the author recommends the unity gain configuration with some alterations to improve the noise performance.

5.2 Supply Noise

Apart from the intrinsic noise from the devices the supply may also add noise to the output but the assumption in this thesis was that the supply was well regulated, it is also important to have an accurate spectrum for the supply noise to accurately determine it's effect on the output noise, thus simulations for supply noise were not performed in this thesis. There are three potential paths of supply noise in our final design in 3.20,1)through I_{bias}, 2)through the reset switch SW_{reset}, 3)through M_{sf},case 1 can be neglected since we can easily assume that I_{bias} is a very good current source.Now we would look at case 2 and 3, 2)In the reset phase SW_{reset} in figure 3.20 forms a common-gate path from the supply to the input of the buffer, for part of the charging operation of the capacitor 'C' the reset switch SW_{reset} is in saturation, this is approximately from the duration when the capacitor charges from 0V to approximately a threshold voltage of the reset switch, during this time the SW_{reset} switch has the capability to act as a good amplifier and so would amplify the noise on the supply rail and dump it onto the capacitor but this would have no real consequence

on the sampled noise on the capacitor because we are still some time away from sampling the final voltage, so the correct model for SW_{reset} to employ in this regard is the model that is closest in time when we have actually sampled the supply voltage, and that model is the transistor SW_{reset} being in deep triode, or in much simpler terms it is just considered a simple switch having a finite R_{on}, if we consider this then the noise added by the supply can simply modelled as being in series with the thermal noise of the switch, so we just to make a small addition in the figure of 3.3, which gives us a complete model as shown in figure 5.1. The amount of noise power deposited on the capacitor by the supply is dependent on the spectrum of the supply, so at the very extreme it can be the case that the size of the capacitor instead of being determined by the $\frac{kT}{C}$ noise, is actually determined by the noise spectrum of the supply, or alternatively we can also increase the channel length of SW_{reset} to increase R_{on}(creates an RC-filter with a lower cut-off frequency), however then we also would have to increase its width by the same proportion to keep the resetting time the same.3)Another path that the supply noise could take is through the source follower transistor in figure M_{sf}, but the advantage we have here is that M_{sf} is in saturation and presents itself as a current source to the supply noise, which means that if the output impedance of M_{sf} is high enough then we can easily say that the noise through this path is negligible when compared to noise in case 2.

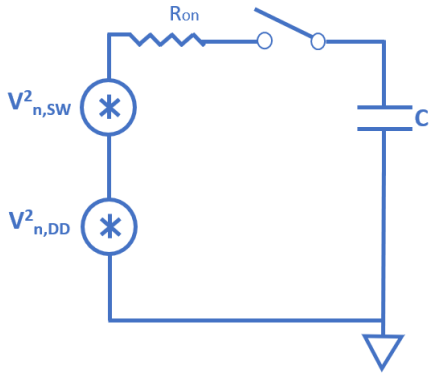

Figure 5.1: Noise Model with addition of supply noise.

5.3 Slope Accuracy over Corners and Mismatch

The results obtained in chapter 4 for slope accuracy tell us that the mean value for the slope is almost precisely close to the target value, but there are some outliers which give rise to our maximum error. Another thing to note here is that the mean value for the slopes stays the same for both corner and mismatch simulations and this can be seen in tables 4.1 and 4.2 respectively. However the relative percentage error for the case of outliers is much greater due to mismatch than PVT variations, the maximum value in this case is an error of 56%, this value is quite high but since the author was not given any strict specifications in regards to the slope accuracy, the value was just reported as it is, however in this section it is important to highlight why this is the case and how it can be tackled with. In the beginning of the design phase in chapter 3 we selected minimum dimensions for our cascode current mirror configurations in figure 3.1 and we stayed with that decision till our final design in figure 3.20, unfortunately the minimum dimensions happen to be the reason for high mismatch and ultimately high relative error in slope. Another factor is the magnitude of the current I_{bias} in figure 3.1, this bias current was chosen after the capacitor value was chosen that met the noise specification, this value can be considered a bit low if we want to accomplish good matching in the current mirror configuration, we can scale up this value but it would then require scaling up our capacitor with the same proportion which would increase both area and power consumption. On the other hand if we wish to reduce mismatch by increasing device dimension of our unit transistor in the current mirror configuration then there is a potential problem which the author foresees and that is that the capacitances of the devices in the cascode structure would increase, the immediate solution that one could think of is to size the capacitor 'C' accordingly so the net capacitance remains the same, the same procedure that we applied in section 3.4.3 where we took the input capacitance of the source follower into account, however there is a slight subtlety in the case of the cascode structures and that is that our ramp generator is programmable so if the unit dimension of the transistor is increased then the parasitic capacitance at node $Vout\_pre$

would vary quite a bit from when we program the slope for $125mV/\mu s$ to when we program the slope for $2000mV/\mu s$, this can potentially cause large slope errors for the configurations that deviate quite a lot from the configuration that the capacitor is sized for, for example if we size capacitor 'C' appropriately for the configuration of $125mV/\mu s$ then we would have quite an accurate value in this configuration however by the time we reach the $2000mV/\mu s$ we would have varied our parasitic capacitance by a lot and this would result in slope errors in this configuration. So to find an optimal size for high accuracy is something to be considered for a more improved design, apart from that auto-calibration techniques as mentioned in [17] can be employed. Further improvement of the slope accuracy for a given slope range in the presence of mismatch is an area where more innovative ideas can be put into.

5.4 Back-Gate biasing

An important feature of the 22nm FDSOI technology is the the back-gate voltage bias whereby you could control the threshold voltage of the device with a body bias, this effect was not utilized in this thesis, however after finishing the design we can identify a potential area where it can be utilized, and these are the switches in our final design in figure 3.20 which include the transistors from $SW_0 - SW_4$ and the reset switch SW_{reset}, the dimensions of these switches can be reduced considerably if we utilize the back-gate effect to lower the threshold voltage.

Chapter 6

Conclusion and Future works

The performance of a continuous time passive ramp generator was presented in this thesis, however due to lack of numeric data on the popular ramp generators existing in literature a conclusive decision on the performance of our design is pre-mature. The design however can further be improved by using auto-calibration techniques as in [17]. Post-layout simulations are also required for better authentication of the design performance, so in the future if this thesis is to be taken forward then a layout of the current design would be necessary. Since the ramp generator implemented here is a stand-alone component while in reality it is to be used within a SS-ADC which in turn would be used in a complete CMOS Image Sensor, it would be an interesting project to create behaviour models around this design and see how it impacts the overall performance of the system.Lastly for the noise simulations pss and pnoise analysis tools in cadence were used in this thesis, this was chosen because it had a faster simulation run time when compared to a transient simulation, however for future work the author recommends also using the transient simulation to determine the noise power, and then verifying with the results obtained in this thesis.

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Appendix

A Passive Ramp

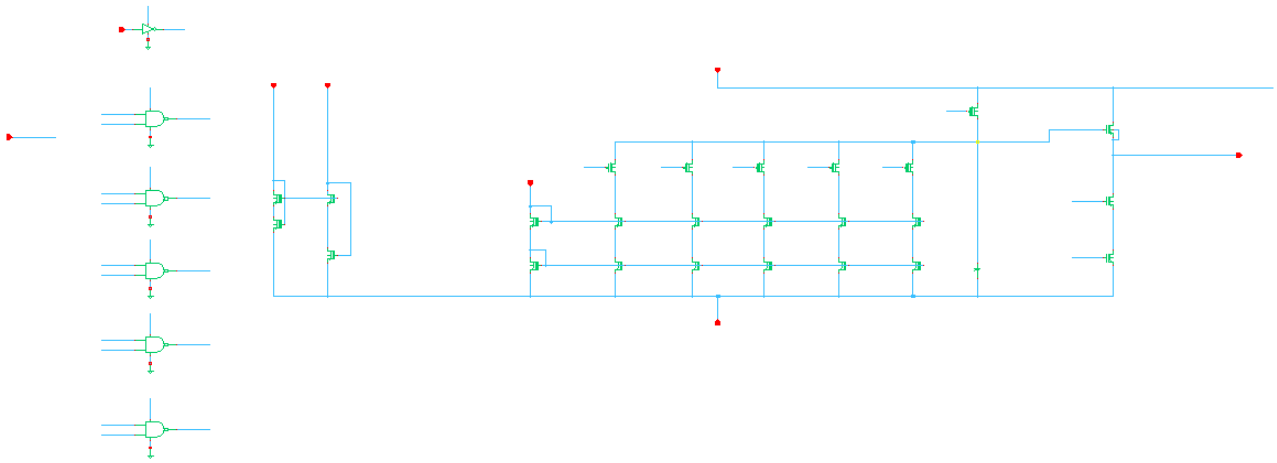

Figure 1: Schematic of Passive ramp

B Opamp Schematic

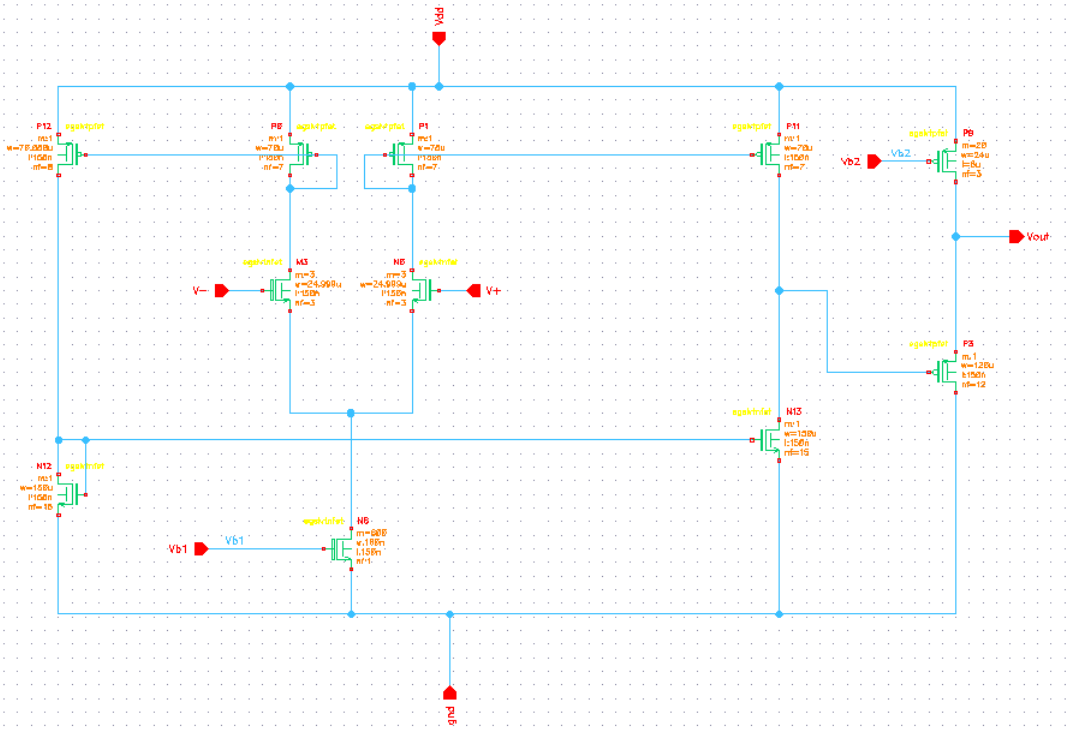

Figure 2: Schematic of Opamp

C Slope Measurement Testbench

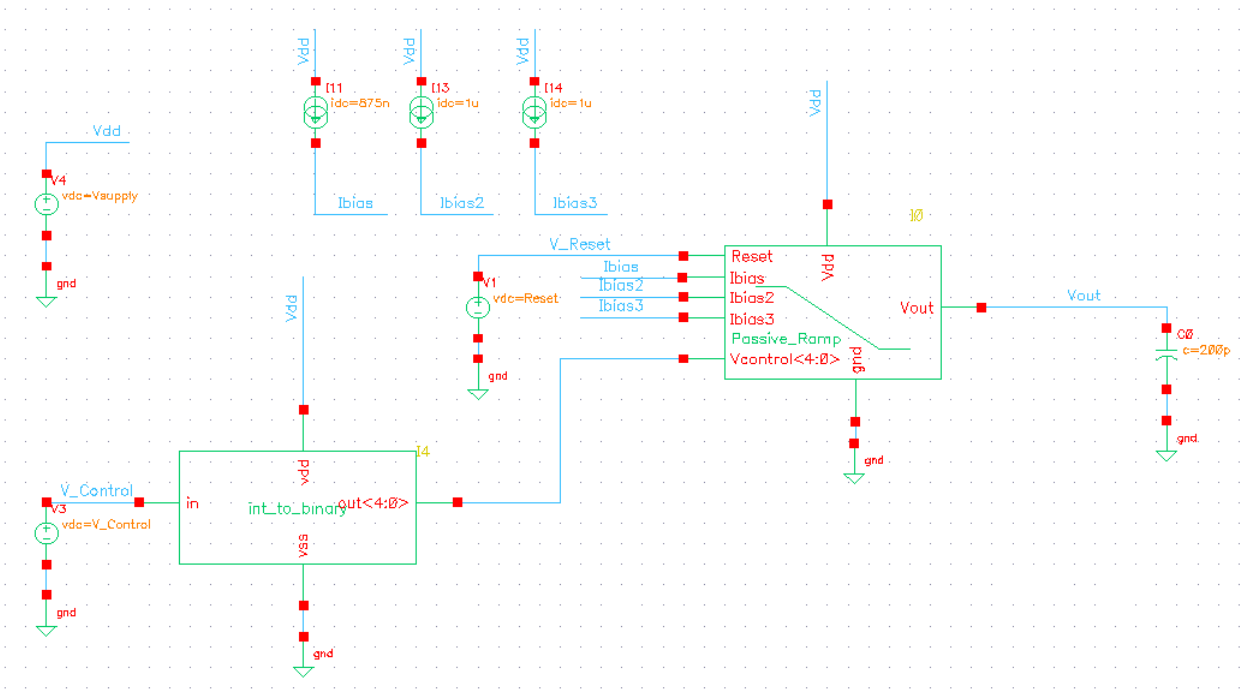

Figure 3: Testbench to test the slope accuracy

D Noise Measurement Testbench

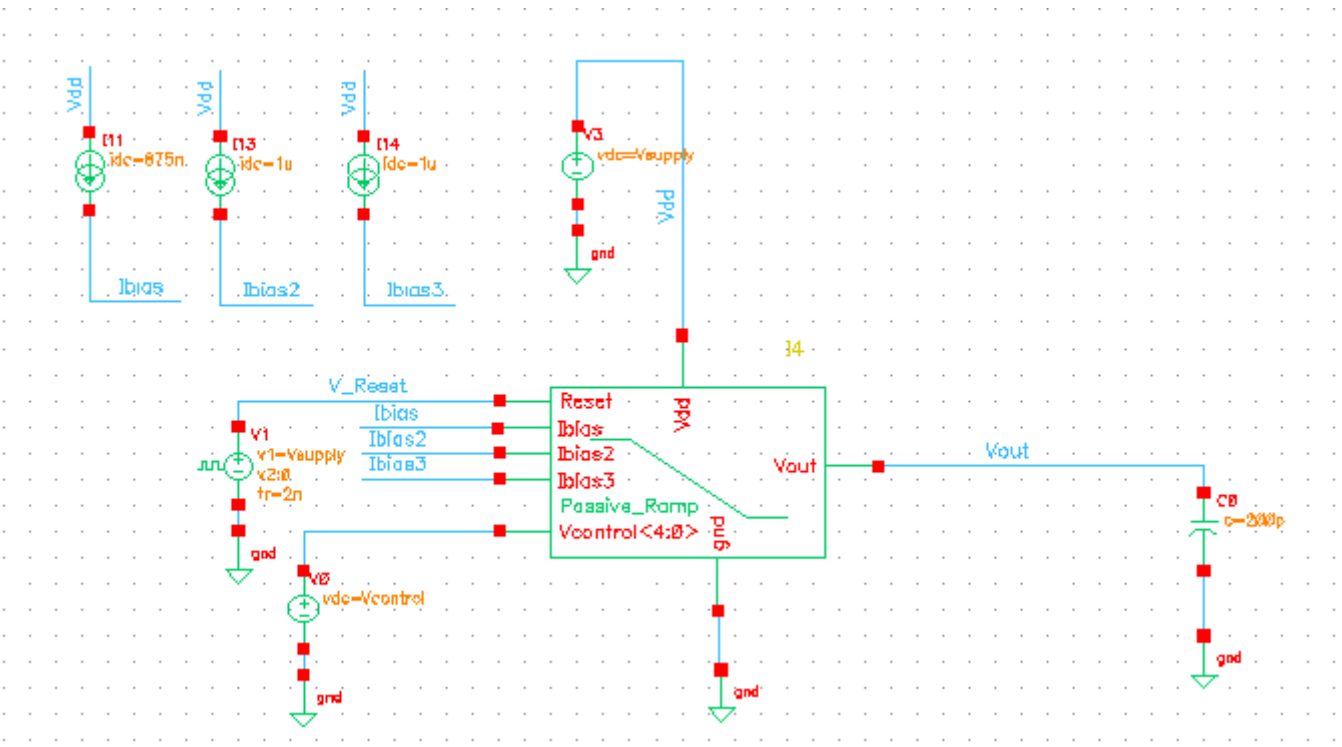

Figure 4: Testbench to test the noise at the output

E INL Measurement Testbench

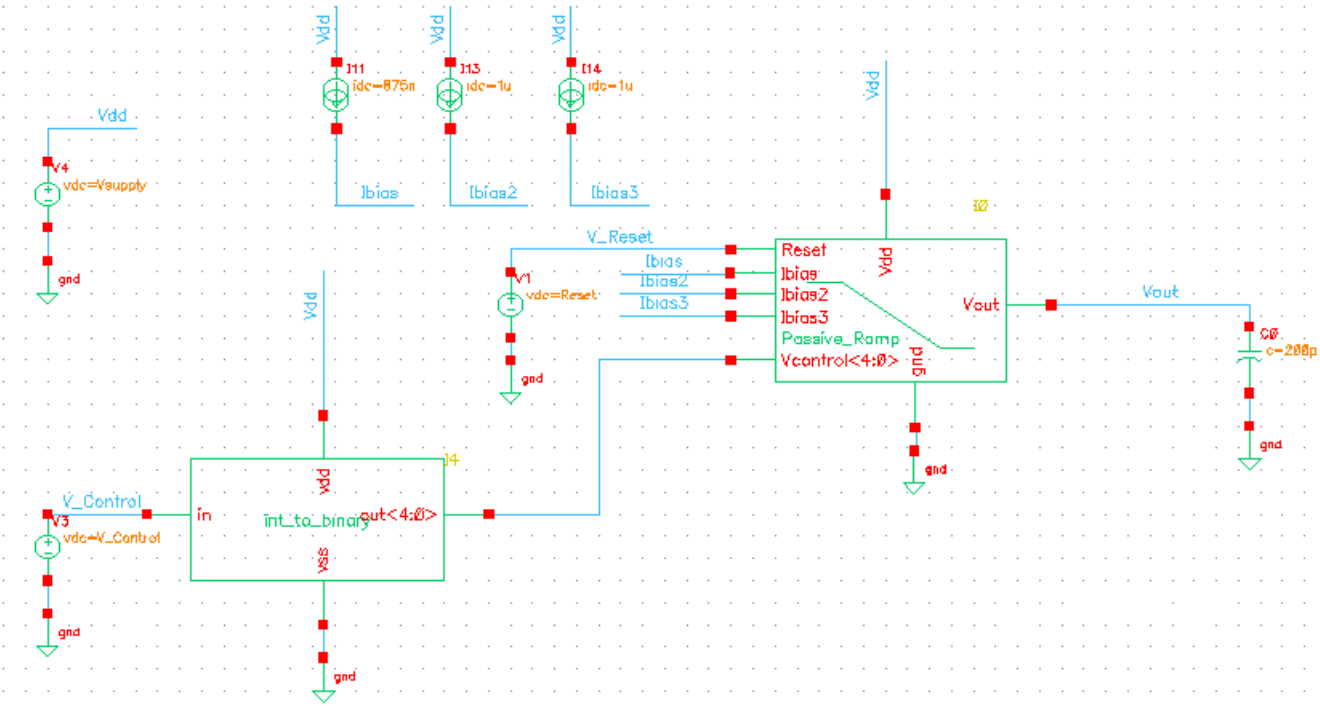

Figure 5: Testbench to test the INL at the output

F Opamp operating point measurement and output resistance measurement Testbench

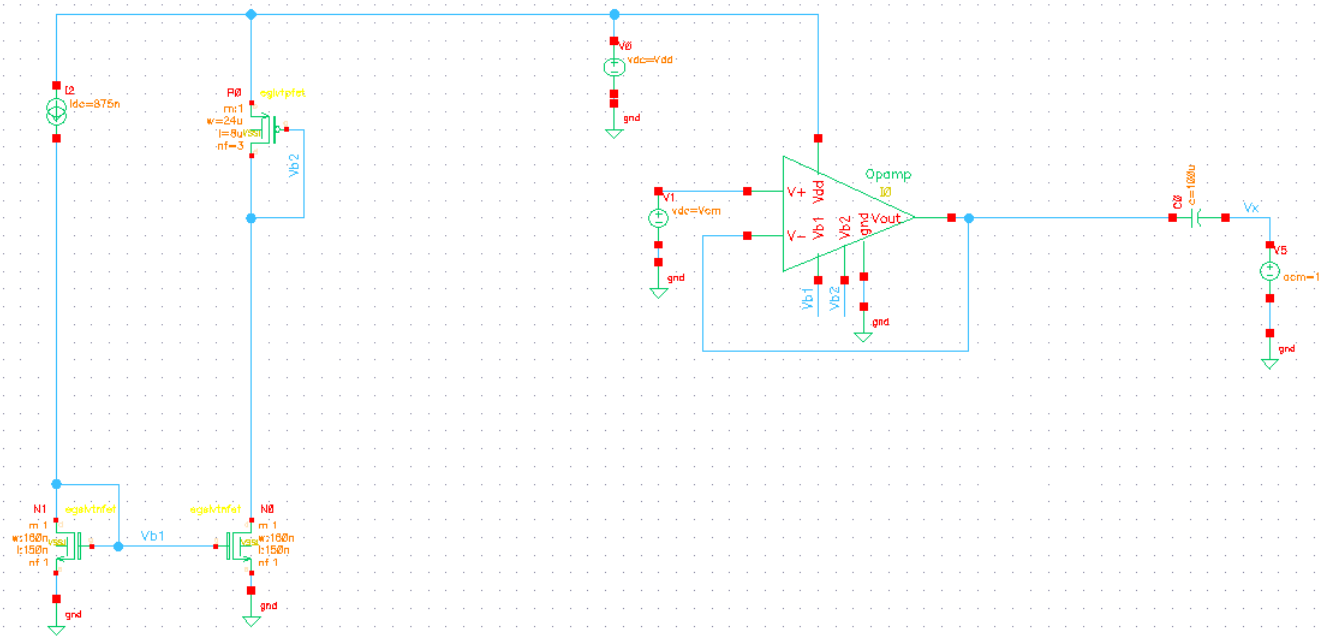

Figure 6: Testbench to check the operating points and close loop output resistance of the opamp.

G Opamp DC Gain and Stability TestBench

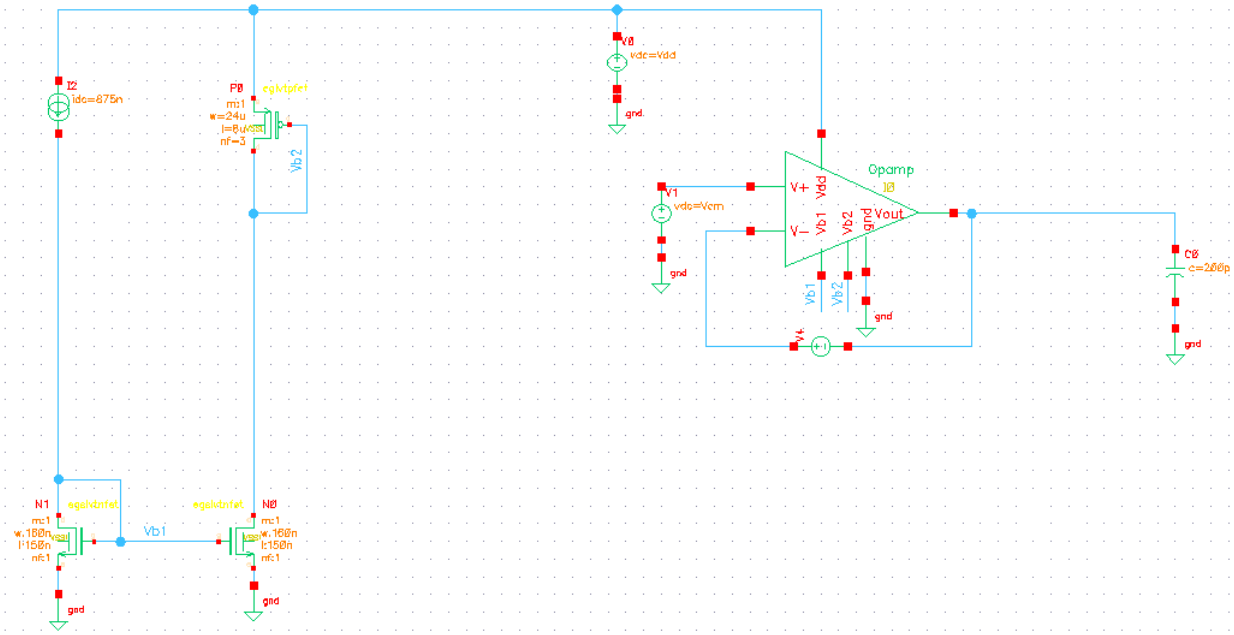

Figure 7: Testbench to check the open loop DC Gain and Stability of the opamp

H Source Follower Ramp Testbench

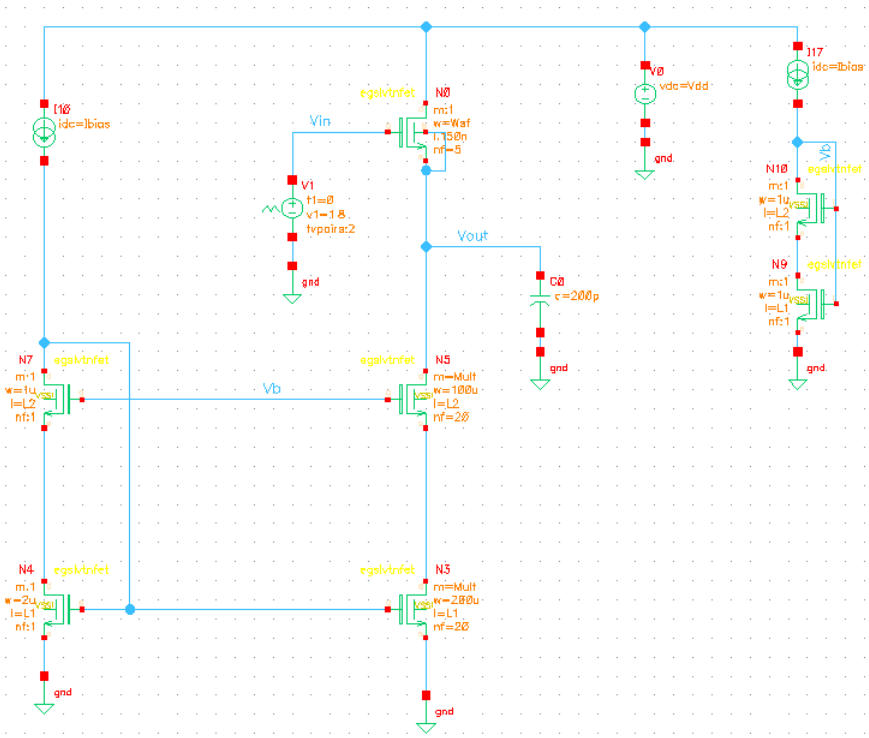

Figure 8: Testbench to check the DC points and the ramp response of the source follower.

I VerilogA for int to binary convertor

```
// VerilogA for Master_Thesis, int_to_binary, veriloga

`include "constants.vams"
`include "disciplines.vams"

module int_to_binary(in, out, vss, vdd);

input in;
input vdd;
input vss;
output[4:0] out;

electrical vdd;
electrical vss;
electrical in;
electrical[4:0] out;



integer rem;

genvar i;

analog begin

rem = floor(V(in,vss));

for(i=4; i>=0; i=i-1) begin

if(rem >= pow(2,i)) begin

 V(out[i],vss) <+ V(vdd,vss)*1;
 rem = rem - pow(2,i);

end

else begin

 V(out[i],vss) <+ 0;


end


end
```

Figure 9: VerilogA code for the "int_to_binary" block used in "C".