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Origin of Leakage Currents and Nanowire-to-Nanowire Inhomogeneity in Radial p−i−n Junction GaAs Nanowire Array Solar Cells on Si

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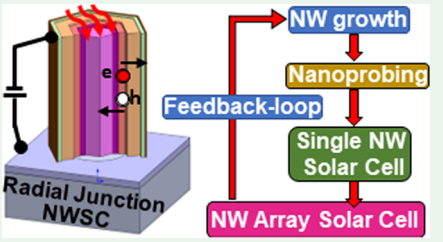
ABSTRACT: To realize the promising potential of radial junction nanowire (NW) array-based solar cells, it is crucial to get physical insight into how the overall photoconversion efficiency (PCE) is impacted by the hole mask properties, NW growth, and post-growth device processing. In this work, we have fabricated and analyzed a radial p−i−n junction GaAs NW array solar cell grown by molecular beam epitaxy (MBE) on a Si substrate. Multiple electrical measurements are correlated through a range of characterization techniques such as nanoprobing of as-grown individual NWs, multicontact single-NW studies, and structural characterization of the fabricated NW array solar cell. A relatively high leakage current density (~120 mA/cm^2 at −1 V) was measured from the solar cell, resulting in a PCE of only ~2.1%. The origin of this high leakage current was further investigated by measuring the electrical transport properties of individual as-grown NWs in the array through nanoprobing, revealing a high variation in electrical properties from NW to NW. In contrast to this, planar single-NW solar cells have shown rectifying characteristics with high on/off ratios and an average PCE of ~5.2%, indicating a leakage path in the vertical configuration of the NWs. Furthermore, structural analysis of the NW array reveals a regular occurrence of NWs with off-centered nucleation for the p-GaAs NW core in the holes in the hole mask, leading to a partial or full electrical shortening of the n-GaAs NW shell to the p-Si substrate. This is shown to be predominantly responsible for the high leakage current density and poor PCE from the NW array solar cell. These findings will help to improve the structural design of radial junction NW array solar cells in order to further improve the PCE.



KEYWORDS: *nanowire, solar cell, GaAs on Si, radial junction, molecular beam epitaxy, nanoprobing*

1. INTRODUCTION

The arrangement of vertically standing III−V semiconductor nanowires (NWs) selectively grown in an array pattern is one of the most promising designs to outperform and replace conventional thin-film-based solar cells[1,2] and has shown a lot of interest recently.[3−6] This unique geometry of the NW and their arrangement benefit from enhanced light absorption, due to an intrinsic light trapping and antireflection phenomenon,[7,8] together with a low material consumption[6] give this design an important advantage in achieving future high-efficiency and low-cost solar cells.[3,4] Additionally, superior-quality hetero-epitaxial interfaces[9] together with the possibility for monolithic integration of III−V semiconductor NWs on the industry-favorable Si-platform[10,11] make this design very promising for high-performance III−V NW/Si tandem solar cells.[12−14] However, according to simulations, an optimization in NW length, diameter, pitch, and array symmetry is crucial to achieve a high photoconversion efficiency (PCE) from such solar cells.[15,16]

A promising, but also challenging, aspect of NW devices is the several degrees of freedom in designing different NW geometries while retaining a high crystal phase purity. Through epitaxial growth engineering[17,18] and compositional modulations,[19,20] the NW geometry can be configured with axial and/or radial heterostructures.[21] The axial junction NW array solar cell (NWASC) geometry provides flexibility in designing multijunction tandem solar cells to enhance the PCE by utilizing the solar spectrum in a more efficient way. Using such axial junction NW arrays, PCEs of ~13.8[1] and ~15.3%[5] and a power-per-weight ratio of ~560 W/g[6] have been achieved using In*P*- and GaAs-based NW structures. In a vertically standing axial junction NW structure, the light absorption and carrier extraction take place along the length of the NW, and the generated photocarriers are transported vertically along the NW in order to be extracted by the top and bottom electrodes. This limits the length of the NWs to a certain point: while longer NWs increase the light absorption due to a larger

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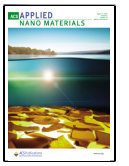

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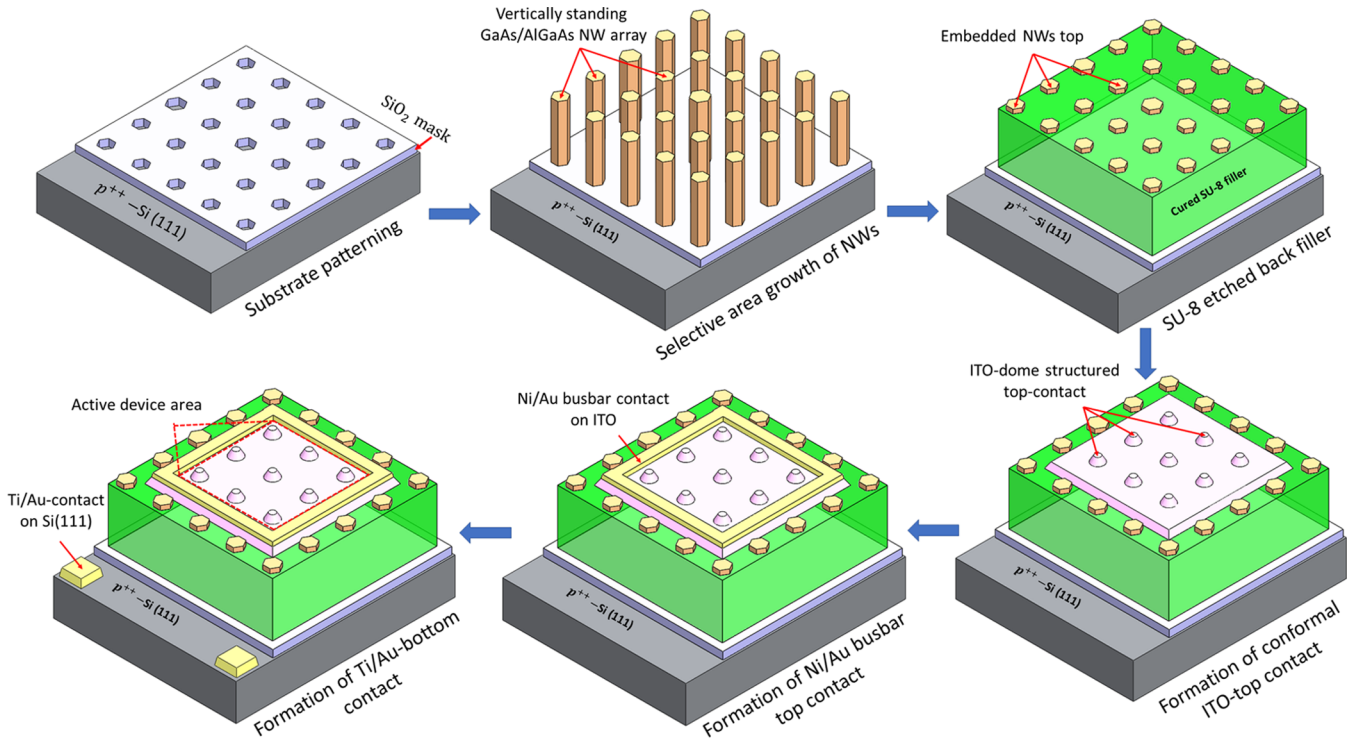
Scheme 1. Step-by-Step Fabrication Process of a Radial Junction GaAs NW Array Solar Cell



absorbing volume, they conversely reduce the carrier extraction efficiency. This limits the achievable PCE of the axial NWASC to a large degree.[15,16] On the other hand, by using a radial junction (core−shell) NW geometry, the light absorption and the generated carrier extraction can be controlled independently and the photocarriers can be extracted and collected radially through a much shorter distance.[22,23] Thus, the light absorption in the radial NW configuration can be enhanced by increasing the NW length without reducing the carrier extraction efficiency.[24,25] Moreover, the carrier extraction through the very short radial distance may make it possible to collect the carriers before their thermalization,[26,27] providing a new way to fabricate hot carrier solar cells with a potential to achieve a PCE even beyond the Shockley−Queisser theoretical limit.[28] In this regard, Krogstrup et al. demonstrated a PCE of ∼40% using a vertically standing single radial junction GaAs NW solar cell, in which it was shown that the vertical GaAs NWs have a larger absorption cross section compared to their actual physical dimension due to a nanoantenna effect.[29] Although the radial junction NW array geometry is theoretically capable of surpassing the Shockley−Queisser theoretical limit for a single junction solar cell, the highest achieved PCE so far is only 6.63%.[30] This is partly related to the structural design and device processing complexities of radial junction NWs.[30]

Another major challenge in NWASCs, especially with radial junction NW geometries, is the lack of reliable characterization techniques which can correlate the final photovoltaic performance to the mask hole patterning, epitaxial growth, and post-growth device processing all together. These are all essential aspects to monitor the NWASC in order to improve the overall PCE performance and need to be optimized through new design ideas and characterization in a feedback loop. Only a few characterization techniques have been demonstrated to overcome this challenge, including electron beam-induced current (EBIC) scanning,[31,32] individual probing of the as-grown NWs in an array,[33] and conductive-probe atomic force microscopy (C-AFM) mapping.[34] However, while these characterization techniques, either independently or combined with other techniques, can be utilized to understand and monitor axial junction NWASCs, radial junction NWASCs have so far not been studied in this way.

In this work, we have fabricated and characterized a GaAs NWASC using a radial p−i−n junction NW geometry with an AlGaAs passivation shell, in which a relatively high leakage current density and a low PCE of ∼2.11% were measured. The origin of this low PCE and high leakage current density has then been further analyzed through a combination of different characterization techniques including electrical nanoprobing of individual as-grown NWs in the array, planar single-NW solar cell (SNWSC) measurements, and structural characterizations of the fabricated NWASC through transmission electron microscopy (TEM). From nanoprobing measurements, a high degree of inhomogeneity in the electrical properties of NW to NW in the array was determined. In contrast to the NWASC, consistent and better performance is achieved with the SNWSCs with high on/off ratios and an average PCE of ∼5.2%. TEM analysis on the fabricated NWASC reveals an off-centered growth of the NWs in the holes of the hole mask for a large percentage of the NWs in the array, leading to partial and/or full electrical shortening of the n-GaAs NW shell to the p-Si substrate. The impact of this shortening and its variation from NW to NW in the array on the PCE, alongside with some other key issues with radial junction GaAs NWASCs, are also addressed in this work.

2. EXPERIMENTAL DETAILS

2.1. Growth Details for Radial p−i−n Junction NWs. The radial junction GaAs NWs were grown in a solid-source Veeco GEN930 molecular beam epitaxy (MBE) system on heavily p-type

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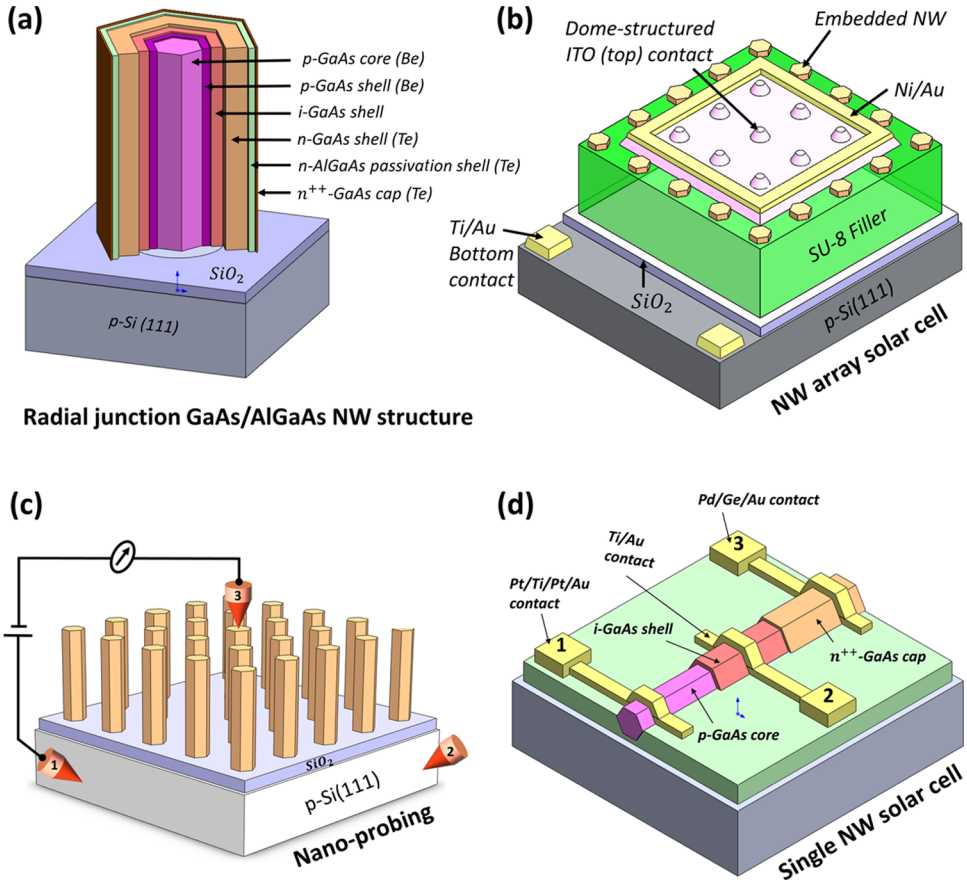

Figure 1. (a) Cross-sectional schematic representation of intended radial p−i−n junction GaAs NWs grown on a p-Si(111) substrate with a hole-patterned SiO_2 mask. The NWs are composed of a Be-doped p-GaAs core, a Be-doped p-GaAs shell, an i-GaAs shell, a Te-doped n-GaAs shell, a Te-doped n-AlGaAs passivation shell, and a Te-doped n^{++}-GaAs cap. (b) Schematic representation of an NWASC array solar cell with the NWs embedded in an SU-8 filler. The device includes a dome-structured ITO (top) contact, a Ni/Au metal-square contact on top of the ITO, and Ti/Au bottom contacts on the p-Si(111) substrate located outside the NW array region (c) Schematic representation of the nanoprobing technique with W-nanoprobes probing the Si substrate with probe 1 and probe 2 and the n^{++}-GaAs cap from the NW top with probe 3. (d) Schematic representation of selective-area shell-etched planar single GaAs NW solar cell. The outermost n^{++}-GaAs cap, i-GaAs shell, and inner p-GaAs core are shown with light-orange, dark-orange, and pink colors, respectively. The positions of the metal contacts to p-, i-, and n^{++}-GaAs are shown with yellow color. The light-green-colored layer represents the cured photoresist in which the NW is partly embedded.

doped Si(111) substrates with a 40 nm thermally grown silicon oxide patterned by electron beam lithography (EBL) and etched using a 30:1 buffered oxide etchant (BOE) (see Scheme 1). The self-catalyzed GaAs NW growth method was used to grow a Be-doped p-type GaAs NW core at 625 °C. Ga predeposition and a Be-doped GaAsSb stem (~90 nm) growth step were adopted for 45 s and 1 min, respectively, to enhance the vertical yield of the NWs in the array.[35] Ga, As_2, and Sb_2 fluxes were 0.7 ML/s, 3×10^{-6}, and 1×10^{-7} Torr, respectively. Ga and Al fluxes are stated as equivalent to thin-film growth rates at 585 °C on a GaAs(001) substrate. A Be flux equivalent to a thin-film doping level of 2.4×10^{18} cm^{-3} at a GaAs(001) growth rate of 1 ML/s at 585 °C was used for the p-GaAsSb stem and the p-GaAs NW core. The p-GaAs core was grown for 14 min with the same Ga and As_2 fluxes as used for the GaAsSb stem growth step. The Ga catalyst droplets on top of the grown NWs were then solidified under an As_2 flux of 1×10^{-5} Torr for 15 min, and the As_2 flux was kept the same for further radial shell growth. After the Ga catalyst solidification process, the substrate temperature was ramped down to 370 °C and the Ga flux was changed to 0.2 ML/s for the radial shell growth. A p-type-doped GaAs shell followed by an intrinsic GaAs shell were then successively grown for 44 and 53 min, respectively. After this, an n-GaAs emitter shell was grown followed by an n-AlGaAs passivation shell, using a Te dopant flux equivalent to a thin-film doping level of 1×10^{18} cm^{-3} at a GaAs(001) growth rate of 1 ML/s at 550 °C. The radial n-GaAs emitter shell and the n-AlGaAs (Al flux of 0.1 ML/s) passivation shell were grown for 140 and 19 min, respectively. In order to achieve an ohmic electrical contact to the outermost shell of the NW, an n^{++}-GaAs cap was finally grown with a Te flux equivalent to a thin-film doping level of 1×10^{19} cm^{-3} at a GaAs(001) growth rate of 1 ML/s for 9 min. The intended radial p−i−n junction GaAs NW array and individual NW structure on a Si substrate with hole-patterned SiO_2 mask is schematically shown in Scheme 1 and in Figure 1a, respectively. The intended dimensions of the core and the radial shells of the as-grown GaAs NWs and expected doping levels are summarized in Table 1.

2.2. Fabrication of the NW Array Solar Cell. For the NWASC, three 500 μm × 500 μm sized NW arrays were grown on the same Si substrate with an intended 1 μm NW-to-NW pitch. The arrays were then separated by scribing and breaking of the substrate into three pieces. One of those arrays (array #1) was used to fabricate the NWASC. The purpose of the other two arrays (array #2 and array #3) will be introduced in Sections 2.3 and 2.4. In order to fabricate the NWASC, an ~15 nm thick Al_xO_y dielectric shell was first deposited by atomic layer deposition (ALD). A transparent and dielectric SU-8 layer was then applied to the NW array to fill the interspace between the NWs. The SU-8 was diluted prior to its use, enabling it to fill the tiny interspace in between the NWs in the array. The filler layer was then etched back until the neck of the NWs was uncovered and then cured at 185 °C for 2 min. To avoid any stress in the SU-8 produced through a rapid increase in temperature, the curing temperature was

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ACS Appl. Nano Mater. 2023, 6, 14103−14113

Table 1. Summary of the Intended Core and Radial Shell Dimensions and Nominal Doping Levels of the Radial p−i−n Junction GaAs NWs[a]

NW segment	nominal dimensions (nm)	nominal doping level (cm^{-3})[b]
p-GaAsSb(Be) core stem	90 (height)	3.4×10^{18}
p-GaAs(Be) core	90 (diameter)	3.4×10^{18}
p-GaAs(Be) shell	25 (layer thickness)	1.2×10^{18}
i-GaAs shell	30 (layer thickness)	X
n-GaAs(Te) emitter shell	80 (layer thickness)	5×10^{18}
n-AlGaAs(Te) passivation shell	16 (layer thickness)	3.3×10^{18}
n^{++}-GaAs(Te) cap	5 (layer thickness)	5×10^{19}

[a]The NWs were designed to be around 400 nm in diameter. [b]The doping levels are estimated from the levels achieved for thin films with a growth rate of 1 ML/s on a GaAs(001) substrate adjusting for changes in dopant/group III flux ratio.

increased in 60 °C steps. This slow increase in curing temperature is crucial for the structural quality of the NWs, NW/substrate interface, and vertical alignment of the NWs during processing, as an improper curing can bend or even break the NWs. The Al_xO_y dielectric shell at the NW top was then removed using CHF_3/Ar dry etching such that an electrical contact to the n^{++}-GaAs cap at the top of the NWs can be formed. Bi-layered indium tin oxide (ITO) was then deposited through sputtering to form a conformal transparent conducting electrode (TCE) at the top of the NW array. Process details for the ITO deposition can be found in our previous work.[6] By utilizing this method, the NWs were embedded in an SU-8 filler in such a way that an ITO dome-structured array could be fabricated as a top contact.[36] A Ni (20 nm)/Au (200 nm) metal stack was then deposited on the ITO outside of the active device area and a Ti (20 nm)/Au (200 nm) bottom contact was then formed to the p^{++}-Si substrate (after etching out the SiO_2 mask, outside the NW array region). The fabricated NWASC structure is schematically presented in Figure 1b. The ITO (top) contact around the active area of the device is made in such a way that the last rows of the NWs at the four edges of the NW array are not electrically connected (see Figure 1b).

2.3. Nanoprobing to Single As-Grown Vertically Standing NWs. NW array #2 was used to measure the dark current−voltage ($I-V$) characteristics of single as-grown NWs through an in situ nanoprobing technique.[37] The principle of the $I-V$ measurements of single as-grown radial p−i−n junction GaAs NWs using this nanoprobing technique is schematically shown in Figure 1c. Two-point in situ probing was carried out inside a Thermo Fisher Scientific Helios Dual Beam 4 UX focused ion beam (FIB) system, using Imina

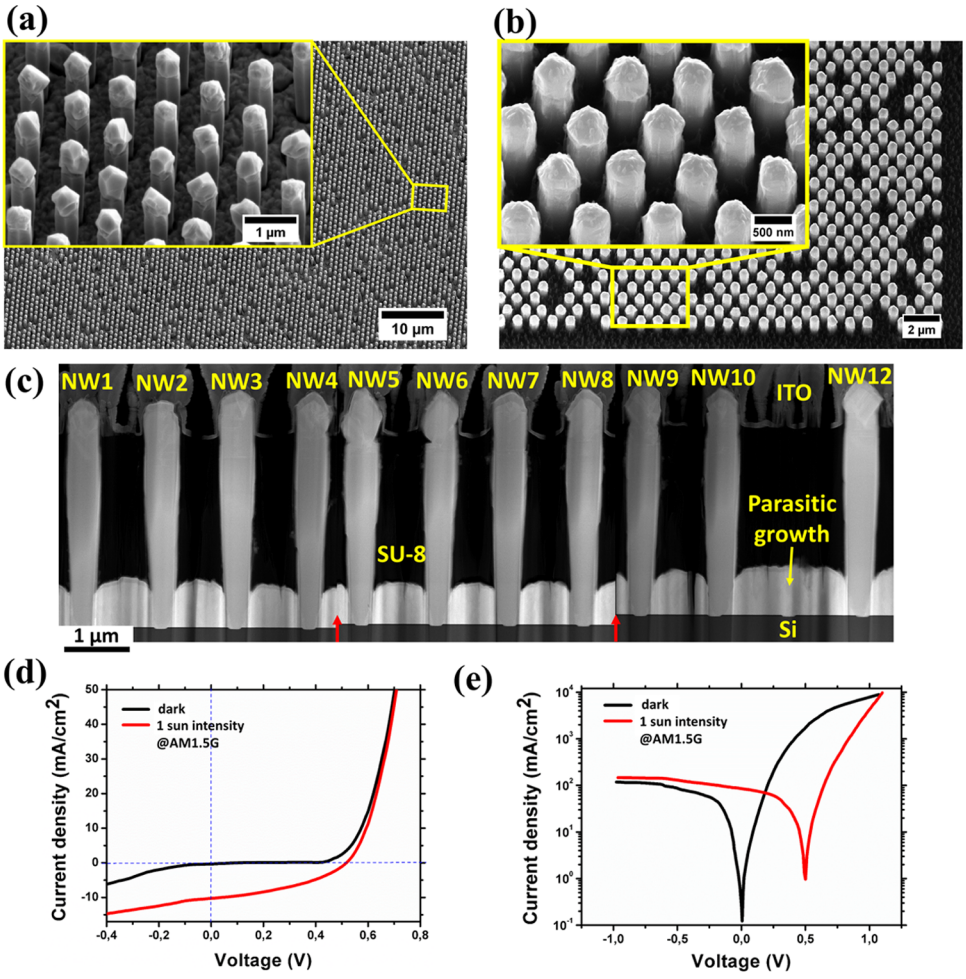

Figure 2. 30° tilted view SEM image of (a) as-grown radial p−i−n junction GaAs NW array and (b) NW array after ALD deposition of a 15 nm conformal Al_2O_3 dielectric cap and an SU-8 filler. (c) Cross-sectional HAADF STEM image of the fully fabricated NWASC including a dome-shaped ITO (top) contact, an SU-8 filler, and the Si substrate with hole-patterned SiO_2 mask. One missing NW (NW11) in the array is highlighted. The shorter than the normal 1 μm NW pitch distances between NW 4 and 5, and NW 8 and 9 are due to STEM image stitching errors (the stitching positions are marked with vertical red arrows in the image). Current density−voltage ($J-V$) characteristics of the NWASC measured in dark mode and at 1 sun intensity (air mass 1.5G) are shown in (d) linear and (e) logarithmic scales.

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miBots as a portable probing platform and an Agilent B2910 source meter unit (SMU) to generate and record $I-V$ sweeps. In this process, the Si substrate with the as-grown NWs was first mounted on a 45° pre-tilted stub. Two miBot W-probes (probe 1 and probe 2) were then used to contact the p-Si substrate on two different sides and $I-V$ sweeps were recorded between probes 1 and 2. Individual NWs were then probed one by one by bringing a 100 nm radius W-nanoprobe further sharpened by FIB (probe 3) into contact with the outermost n^{++}-GaAs radial cap at the NW top, with either probe 1 or 2 in contact with the Si substrate. $I-V$ sweeps were captured using the SMU, consistently sweeping larger voltage ranges until a current limit of 1 μA was reached. In order to measure only the dark currents from the as-grown individual NWs in their vertical configuration, the electron beam was turned off during this measurement process.

2.4. Fabrication of Planar Single-NW Solar Cell. To understand the influence of the bottom Si substrate contact on the overall NWASC performance and to inspect the rectification properties from individual radial p−i−n junction GaAs NWs, planar (SNWSC) devices were fabricated using NW array #3. The fabricated structure of a two-step cascaded planar single-NW device is schematically shown in Figure 1d. In order to fabricate such devices, a two-step cascaded etching profile was created for each single NW in a planar geometry using our previously optimized radial NW shell etching recipe, $H_3PO_4/H_2O_2/H_2O$ (1:1:200).[6,38] A first-step selective-area etching was carried out using EBL at the bottom half of the NW for 4.5 min to remove the radial NW n^{++}-GaAs cap shell, n-AlGaAs passivation shell, and n-GaAs emitter shell, exposing the i-GaAs shell. After the first etching step, a second selective-area etching was further employed at the bottom part of the NW for 4 min to remove the radial i-GaAs and p-GaAs shells, exposing the inner p-GaAs NW core. Once this two-step cascaded etching profile is made (inspected with scanning electron microscopy after each step), single NWs were embedded in a curable photoresist layer through a resist etch-back method. This structure helps to form better electrical contacts in the planar single-NW configuration.[39] Three different metal electrodes were then deposited successively to form separate electrical contacts to the outermost radial n^{++}-GaAs cap, i-GaAs shell, and inner p-GaAs core separately at the top, middle, and bottom parts of the NW, respectively. In this process, Pd (20 nm)/Ge (40 nm)/Au (250 nm), Ti (10 nm)/Au (250 nm), and Pt (5 nm)/Ti (10 nm)/Pt (10 nm)/Au (200 nm) metal electrodes were deposited to form ohmic electrical contacts to the n^{++}-GaAs cap, i-GaAs shell, and p-GaAs NW core separately.[40,41] All of the metal contacts were then annealed at 280 °C for 30 s to form ohmic electrical contacts between the NW and the metal electrodes.[6] This single-NW device allows us to measure the electrical properties of the p−i (between contacts 1-2), n−i (between contacts 3−2), and p−i−n (between contacts 1−3) junctions of the radial GaAs NW separately.

2.5. Characterization of the Single-NW Solar Cells and NW Array Solar Cell. The fabricated planar SNWSC devices with their three electrical contacts were first characterized through dark-mode $I-V$ measurements using a Keithley 2636A SMU at room temperature. The p−i, n−i, and p−i−n counterparts of each SNWSC were measured separately before and after the contact annealing process. For the NWASC, the dark-mode $I-V$ characteristic of the overall as-grown array device was measured between the top Ni/Au and bottom Ti/Au contact. The light-mode $I-V$ characteristics for both the planar SNWSCs (the p−i−n junction part) and NWASC were then measured in a solar simulator at 1 sun intensity @ AM1.5G using a tungsten−halogen lamp as an illumination source.

2.6. Structural Characterization of the Fabricated NW Array Solar Cell. In order to understand the detailed growth mechanisms and crystal quality of the NWs and the NWASC, cross-sectional TEM of processed devices was carried out. The TEM lamella was prepared by FIB as described in our previous work.[6] The TEM was performed with a double spherical aberration corrected cold FEG JEOL ARM 200FC, operated at 200 kV. This instrument is equipped with a large Centurio detector, covering a solid angle of 0.98 sr, for energy-dispersive X-ray spectroscopy (EDS), and a GIF Quantum ER for electron energy loss spectroscopy (EELS). High-angle (HA) and low-angle (LA) annular dark-field (ADF) scanning TEM (STEM) images were acquired with a semiconvergence beam angle of 27.4 mrad and with semi-collection angles of 51−203 and 29−51 mrad, respectively. The limited angular collection range of the LAADF STEM images, just outside the range of the 000-diffraction disk, makes these images sensitive to strain and diffraction contrast. EDS and EELS mapping were performed simultaneously in STEM mode.

3. RESULTS AND DISCUSSION

A tilted view SEM image of an as-grown radial p−i−n junction GaAs NW array is shown in Figure 2a. From the SEM image, the NWs are estimated to be ∼3.5 μm long with a diameter of ∼400 nm and as intended with an NW-to-NW pitch of ∼1 μm, i.e., ∼14.4% areal coverage of the NWs in the array (a detailed calculation of areal coverage of the NWs in the array is shown in our previous work[6]). Using a Be-doped p-GaAsSb NW stem as a nucleation layer resulted in a high NW yield (∼90%) in the array.[19] The total diameter of the GaAs NW was designed to be around 400 nm such that it lies close to the second modal absorption peak according to simulations, which leads to very efficient light absorption in the NW array due to an optical antenna effect.[15,16] The GaAs NW array after ALD deposition of a 15 nm conformal Al_2O_3 dielectric cap on the NWs and an SU-8 filler between the NWs until the neck of the NWs is shown in Figure 2b. A cross-sectional TEM image of a fabricated GaAs NWASC with the deposited dome-structured ITO top contact and the cured SU-8 filler is shown in Figure 2c. Unwanted parasitic growth on the SiO_2 hole mask in between the NWs is also observed in Figure 2c. The dark and light-mode $J-V$ characteristics measured from the fabricated NWASC in linear and log scale are shown in Figure 2d,e, respectively. At 1 sun intensity @ AM 1.5G, a V_{oc} of ∼0.52 V, a J_{sc} of ∼10.3 mA/cm^2, and a fill factor (FF) of ∼39% are measured, resulting in a PCE of ∼2.11%, where the areal NWs coverage is ∼14.4%.

As shown by Li et al., for a radial p−i−n junction GaAs NWASC, a high doping density (>10^{18}/cm^3) for both the NW emitter shell and collector core, an optimized emitter shell thickness, a high carrier lifetime as well as an optimized passivation shell are essential for efficient photovoltaic performance.[42] Furthermore, the right thickness for the n-GaAs NW emitter shell is crucial as thin emitters will suffer from severe shell depletion and thicker emitters will lead to a high carrier recombination rate and low carrier collection efficiency. Here an n-GaAs NW emitter shell thickness of ∼80 nm and a p-GaAs collector core to n-GaAs emitter shell thickness ratio of ∼7:2 were chosen so that shorter-wavelength solar radiation photons are mostly absorbed in the emitter region and longer-wavelength solar radiation photons in the core.[42] In addition, in this work, an ∼16 nm thin radial AlGaAs NW passivation shell is utilized. This is critical as GaAs surfaces possess a very high density of surface states which can lead to a high surface recombination rate and degrade the photovoltaic performance.[2,3,5] Despite these design components in the NW structure, the measured PCE value from the NWASC device is still quite low compared to predicted values.[15,16] One of the main reasons for the low photovoltaic performance of this NWASC is attributed to its dark $J-V$ characteristics, which shows a high leakage current density (∼120 mA/cm^2 at −1 V) and thus a low rectification ratio (RR) (∼75 at ± 1 V). The physical cause of this high leakage current in the NWASC and its possible leakage path is thoroughly investigated further through a combination of an

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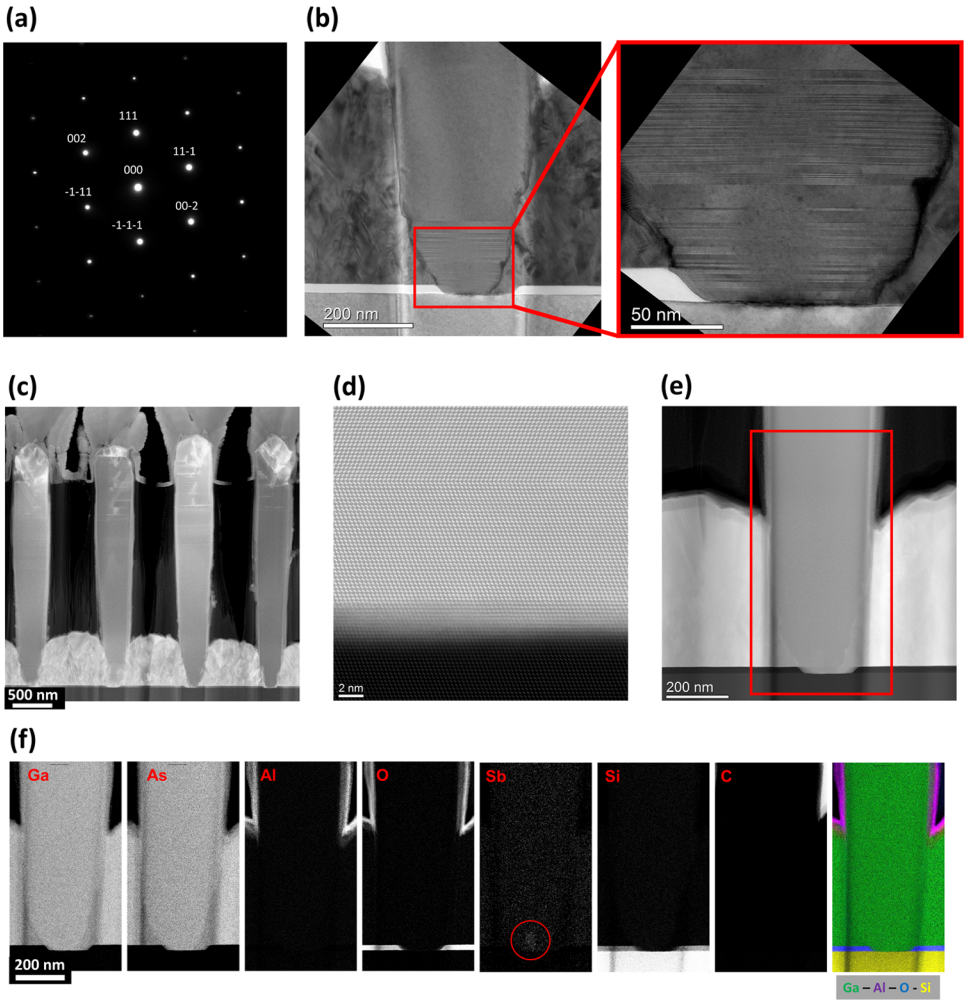

Figure 3. (a) Si [1−10] zone axis diffraction pattern. (b) BF TEM image from the bottom of a GaAs NW. A high density of (111) twinning planes is observed along the cubic [111] direction at the bottom of the NW; a magnified image for the red rectangle frame marked region is shown to the right. (c) LAADF STEM image of four NWs in the array (NWs 1−4 in Figure 2c). Regions with a high structural defect density are visible with bright contrast at the upper part of the NWs. (d) High-resolution HAADF STEM image from the bottom part of NW (NW 12) showing epitaxial relationship between the Si substrate and the NW. (e) HAADF STEM image from the bottom part of NW (NW 12 in Figure 2c) with a red rectangle frame indicating where element mapping shown in (f) was carried out. (f) Element mapping using combined EDS and EELS from inside the red rectangle frame on the HAADF STEM image in (e). Elevated Sb signal at the bottom of the NW is shown in the Sb mapping with a red circular frame.

analysis of TEM data, dark-mode $I-V$ characteristics of as-grown individual NWs in the array as measured by nano-probing, and $I-V$ measurements of planar SNWSCs.

TEM analysis showed that all of the NWs were grown epitaxially on the Si(111) substrate. For all of the TEM images as shown in Figure 3, the Si substrate was oriented along the [1−10] direction as demonstrated by the observed [1−10] zone axis diffraction pattern in Figure 3a. All NWs were found to have cubic zinc blende crystal structure. For many of the NWs in the array, a high density of (111) twinning planes are observed in the bottom 100−200 nm of the NW, as shown in the bright field (BF) TEM image in Figure 3b. Further, strain-sensitive LAADF STEM imaging of the NW array reveals a high density of strained regions at the Si/NW interfaces as well as regions with dislocations in the upper part of the NWs, as shown in Figure 3c. The LAADF imaging conditions were optimized so that the strained interfaces/regions and defects are clearly visible in bright contrast. The high density of defects observed at the NW top, present mostly right below the Ga catalyst droplet may increase the recombination of photo-generated carriers in those specific regions and also increase the vertical channel resistance of the NWs and especially the contact resistance at the n^{++}-GaAs NW cap/ITO interface, which reduces the collection efficiency of electrons. At the other end of the NW, the high density of (111) twinning planes at the NW bottom may increase the (p-type) NW core channel resistance and negatively affect the hole transport through the NW core and reduce the collection efficiency of holes at the p-Si substrate. A high-resolution HAADF STEM image from the bottom part of an NW is shown in Figure 3d, which shows a high crystalline quality at the p-Si/p-GaAsSb NW interface with a few nm thin intermixed region. However, the HAADF STEM image from the bottom part of this NW shows that it has not grown symmetrically from the center of the SiO_2 mask hole, as shown in Figure 3e. The TEM studies show that this was the case for a high percentage of the NWs in the array. In order to understand this in more detail, an elemental mapping was carried out (see Figure 3f) through combined EDS and EELS scans carried out in the region enclosed by the red frame in the HAADF STEM image in

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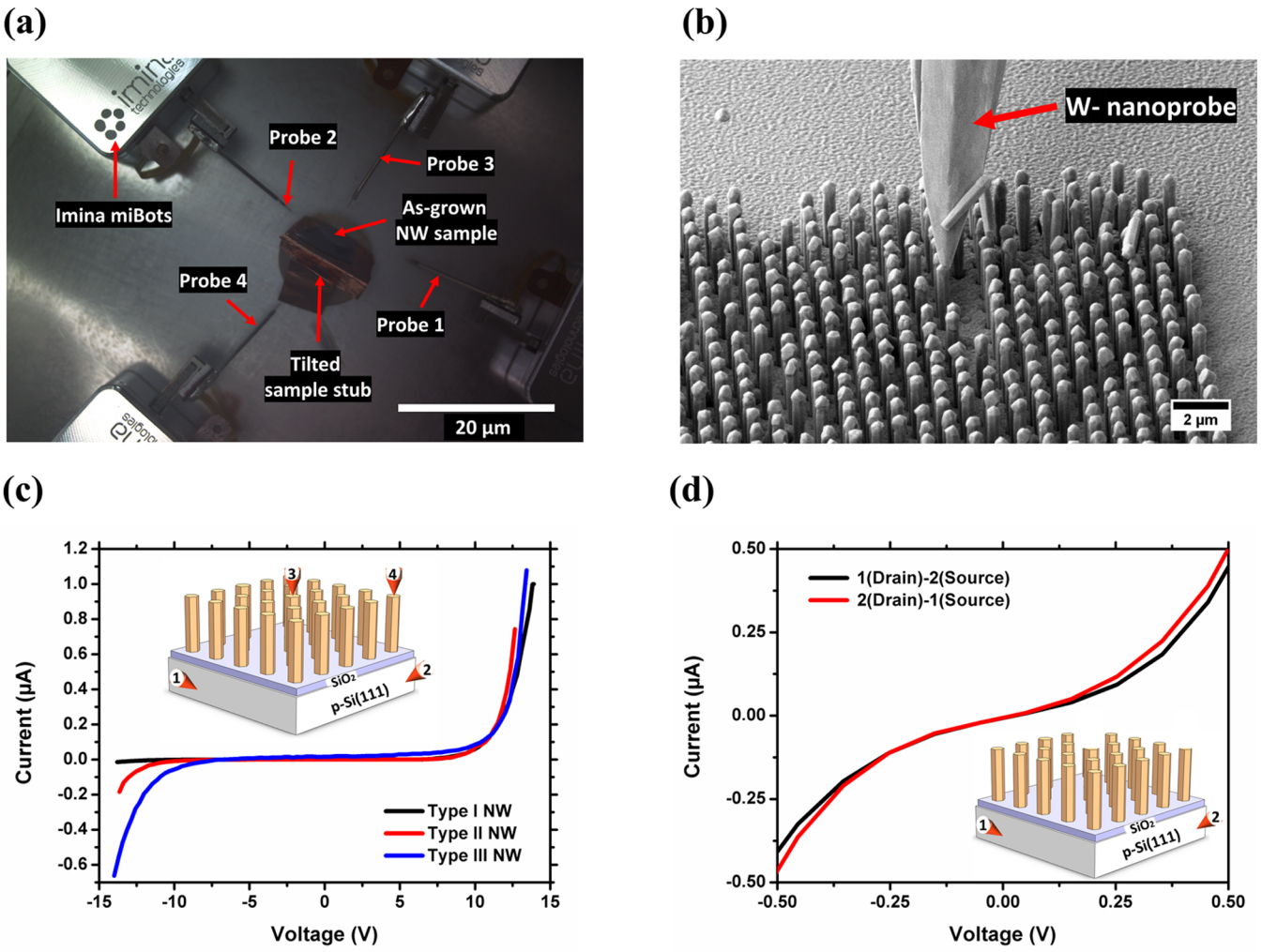

Figure 4. (a) Nanoprobing set up inside the FIB with four miBots carrying W-nanoprobes, a pre-tilted sample stub, and the mounted NW array sample. (b) Tilted view SEM image of the NW array with a FIB-sharpened W-nanoprobe in electrical contact to a single as-grown NW at the top (n^{++}-GaAs cap). (c) Dark-mode *I*−*V* characteristics of three typical types of as-grown NWs measured between the NW top and bottom p-Si substrate with probe 1 or 2 and probe 3, respectively. Probe 4 was used as a backup. (d) Dark-mode *I*−*V* characteristics of W-probe/p-Si/W-probe contacts measured between probes 1 and 2.

Figure 3e. A region with an elevated Sb signal was found at the bottom of the NW, marked with a red circle in the Sb signal image of Figure 3f. As Sb was used to achieve a high nucleation yield in the NW array, a region of elevated Sb content is likely a trace of the initial Ga catalyst particle location. It is notable that the region with elevated Sb was found exactly at the center of the NW, but the region is off-centered with respect to the hole in the SiO_2 hole mask. This indicates that the GaAsSb nucleation layer and/or the p-GaAsSb NW core stem for a number of NWs in the array are nucleating slightly off-centered or at the edge of the hole as previously reported by Plissard et al.[43] This means that the radial i-GaAs NW shell, which (together with the NW core) is intended to fill the entire hole according to the NW growth design, may not do so for such off-centered NWs in the array. This leads to the possibility of partial contact between the n-GaAs NW shell and the p-Si substrate, forming a hetero p−n junction, depending on how much the grown p-GaAs NW core is off-centered in the hole. A simulated band alignment of the n-GaAs/p-Si interface at equilibrium is shown in Figure S1 in the Supporting Information. If the n-GaAs shell is in contact with the p-Si substrate due to NWs not being centered in the SiO_2 nanohole, then there will be three p-n junctions near the p-Si substrate: (1) the p-Si substrate/p-GaAs core junction, (2) the p-Si substrate/n-GaAs shell junction and (3) the GaAs p−i−n solar cell junction. To illustrate the effect when the p-GaAs NW core is off-centered in the hole, we consider first the band diagram for the p-Si/n-GaAs junction at equilibrium in dark mode (see Figure S1, Supporting Information). During illumination (e−h pair generation in NWs) the electrostatic potential difference between n-GaAs and p-GaAs will be reduced, and thus also the electrostatic potential difference between p-Si and n-GaAs. This will increase the diffusion of electrons and holes across the p-Si/n-GaAs junction (i.e., increase leakage current) and reduce the overall PCE of the NW array solar cell. Apart from this, the dielectric Al_2O_3 layer was found to completely cap the NWs, as seen both in Figure 3e,f.[44,45] Overall, the possible shortening of some NWs between the n-GaAs shell and the p-Si substrate as well as the parasitic growth between the NWs are most likely the major reasons for the high leakage current measured from the NWASC.

In order to confirm whether these structural, growth, and/or processing-related deformations arise from the off-centered p-

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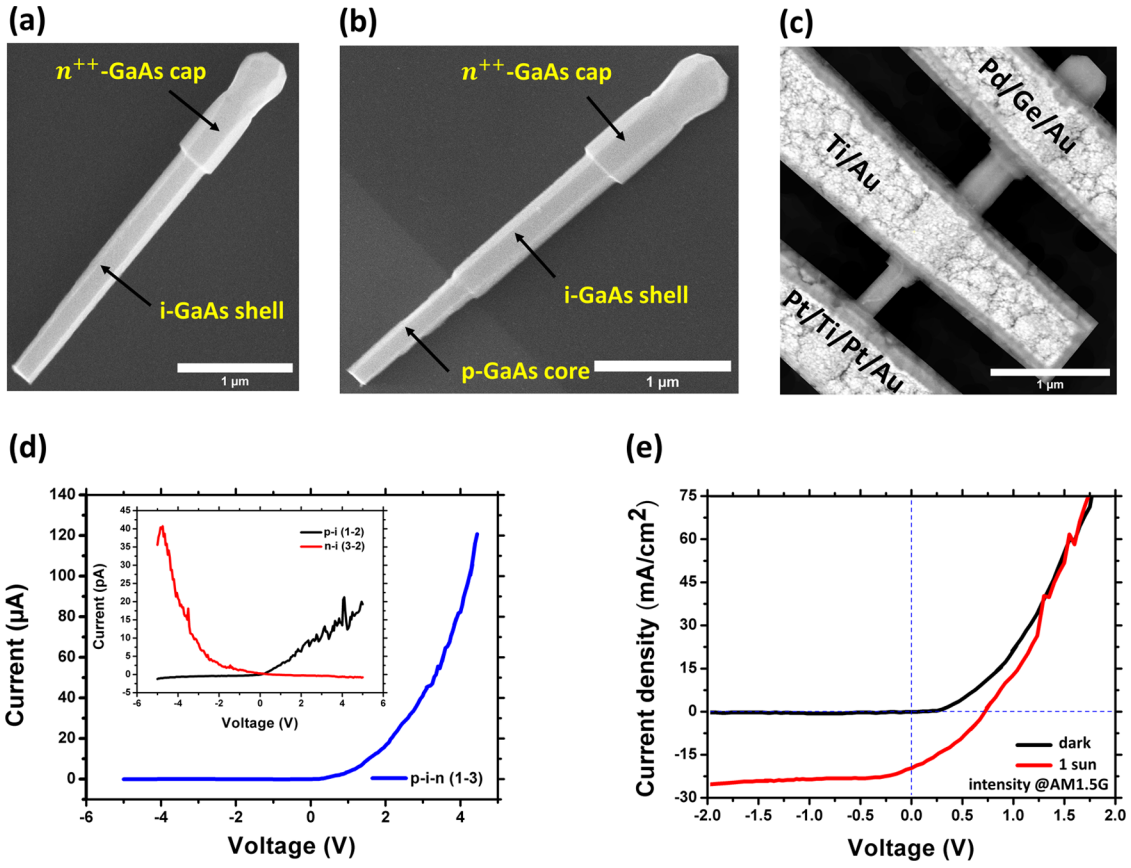

Figure 5. Top-view SEM image of a planar single radial p−i−n junction GaAs NWSC: (a) after a first selective-area shell etching, showing the outermost unetched n^{++}-GaAs cap at the top and i-GaAs shell at the etched region, and (b) after a second shell etching, showing a cascaded selective-area shell-etched single NW with n^{++}-GaAs cap (top), i-GaAs shell (middle), and p-GaAs core (bottom). (c) Single NWSC device with a Pd/Ge/Au n-GaAs contact (top), a Ti/Au i-GaAs contact (middle), and a Pt/Ti/Pt/Au p-GaAs contact (bottom). (d) Dark-mode current−voltage (I−V) characteristics of a single NWSC in for the p−i (contact 1−2), i−n (contact 2−3), and p−n (contact 1−3) counterparts, respectively. (e) Dark- and light-mode J−V curves of the single NWSC device measured for the p−n (contact 1−3) counterpart of the device at 1 sun intensity @ AM 1.5G.

GaAs NW core growth, unwanted parasitic growth, and/or asymmetric hole mask profile, and to investigate their effect on the electrical performance of the overall NWASC device, a nanoprobing scheme (see Figure 1c) was utilized to probe the electrical characteristics of single as-grown vertical NWs. This scheme allows us to measure I−V characteristics from individual as-grown NWs in an array prior to the post-growth processing steps such as the Al_2O_3 dielectric encapsulation through ALD deposition, SU-8 filling, ITO (top) contact deposition, top and bottom metal contact formations, that are part of the final NWASC. An in-chamber photo of the Imina miBot nanoprobing setup with four W-nanoprobes, a pre-tilted sample stub, and a mounted sample piece inside the FIB chamber is shown in Figure 4a. A tilted view SEM image taken during the probing of an individual as-grown NW from array #2 with a FIB-sharpened W-nanoprobe is shown in Figure 4b. A total of 20 NWs were chosen arbitrarily in array #2 to measure the dark-mode I−V characteristics by probing on top of the NW (at the n^{++}-GaAs NW shell) and at the bottom of the Si substrate. Three typical types of I−V characteristics observed from these as-grown single-NW measurements are shown in Figure 4c. Type I NWs (12 of 20 NWs measured) show highly rectifying I−V characteristics with an on/off ratio >100 at ±10 V. Type II NWs (5 of 20 NWs measured) also show rectifying I−V characteristics but with a high leakage current (>50 nA at −10 V) and a low on/off ratio ∼5−10 at ±10 V. In contrast, type III NWs (3 of 20 NWs measured) show completely nonrectifying I−V characteristics. To eliminate the possibility that these variations in the I−V measurements are not related to the contacting process, all NWs were contacted repeatedly a few times and similar results were observed. These sampling results indicate a high NW-to-NW inhomogeneity in the electrical characteristics, where a rather high fraction of type II and type III NWs in the array are responsible for the high leakage current and poor PCE performance as the NWs are connected in parallel to each other in the NWASC device. It is worth mentioning here that the turn-on voltage in all three types of NWs measured through nanoprobing is significantly higher compared to the overall NWASC device. This is attributed to the highly resistive and small area of the W-probe/n^{++}-GaAs NW cap electrical contact. The I−V characteristics of the W-probe/p-Si/W-probe contacts, as measured using probe 1 and 2, are shown in Figure 4d. As they have slightly Schottky-like behavior, this can also contribute to the high turn-on voltage in the individual NW I−V measurements.

From the TEM data and nanoprobing results shown so far, it is demonstrated that the SiO_2 hole mask and the p-Si substrate contact have a critical role in the electrical characteristics and PCE performance of the radial junction GaAs NWASC.

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However, ensuring that the individual NWs have an optimized radial p−i−n geometry is equally important to achieve a high PCE from the NWASC. Thus, to understand the optoelectronic characteristics of the individual NWs, five substrate-contact-free planar SNWSC devices were fabricated. A cascaded etching profile in the NW was created in such a way that separate electrical contacts can be formed onto the outermost n^{++}-GaAs NW cap, the i-GaAs NW shell, and the inner p-GaAs NW core, respectively. A top-view SEM image of the single NW after the first shell etching, with an unetched part at the top and a shell-etched region for the rest of the NW, is shown in Figure 5a. Here, the n^{++}-GaAs cap, n-AlGaAs passivation shell, and n-GaAs emitter shell were removed to have access to the i-GaAs shell in the NW. A similar SEM image after the second shell etching from the same NW, with a cascaded etching profile in the NW showing an unetched part at the top, i-GaAs shell at the middle and p-GaAs core at the NW bottom, is shown in Figure 5b. A final SEM image of a fabricated planar SNWSC device with Pd/Ge/Au n^{++}-GaAs cap contact (top), Ti/Au i-GaAs contact (middle) and Pt/Ti/Pt/Au p-GaAs core contact (bottom) is shown in Figure 5c. Dark-mode $I-V$ characteristics for the p−i, i−n, and p−i−n counterparts of the device after contact annealing are shown in Figure 5d. The low forward current in the p−i and i−n measurements compared to the p−i−n part of the device and the rectifying characteristics clearly signify the existence of an intrinsic GaAs shell in the NW between the p-GaAs core and n-GaAs shell. This is encouraging as the i-GaAs NW shell acts as the active solar emission absorber region in each NW. Interestingly, all of the measured planar SNWSC devices show highly rectifying $I-V$ characteristics of the radial p−i−n junction with an on/off ratio $>10^3$ at ±5 V (see Figure 5d), contrary to the NWASC and nanoprobing measurements. The highly rectifying dark-mode $I-V$ characteristics translate to better photovoltaic performance for single NWSC devices. A planar SNWSC device with V_{oc} ∼0.72 V, J_{sc} ∼20.1 mA/cm^2, FF ∼39%, and PCE ∼5.6% is shown in Figure 5e.

The key performance parameters from the NWASC and single planar NWSC devices are summarized in Table 2. When the NWASC and nanoprobing measurement of the single as-grown NWs are compared to the single planar NWSCs, one must pay attention to that there is no possibility for carrier leakage through a substrate contact in the planar single NWSC configuration. This indicates a severe leakage path through the substrate contact in the vertical configuration of the NWASC device. The higher on/off ratio and PCE in the planar SNWSCs thus indicates how a reduction in leakage current through proper insulation between the collector NW core and emitter shell, an absence of parasitic growth between the NWs as well as a higher degree of control in the hole mask patterning are important issues in order to minimize NW-to-NW inhomogeneity and to achieve a higher PCE from the NWASC device. Another difference between planar NW devices compared to vertical NW devices is that the small additional resistance that is added to the vertical NWs due to Si substrate will be eliminated due to a substrate-free device configuration. The higher V_{oc} and J_{sc} in the single planar NW devices compared to the NW array device can be ascribed to a few factors; (i) larger absorption cross section in the single-NW device, (ii) in the vertical NWs of the array device the carriers are primarily photogenerated near the defective NW-top region due to the Ga catalyst droplet crystallization process, (iii) better metal/NW electrical contacts in the planar NW devices compared to the ITO/NW vertical contact in the array device. Semi-log characteristics for single planar and type I, type II, and type III single vertical NWs are shown in Supporting Information, Figure S2. The calculated ideality factor (η) and reverse saturation current density, J_0 (dark), are listed in Table S1 in the Supporting Information.

We also believe that the Ti/Au contact on the active absorber region (i-GaAs NW shell), fabricated to investigate the existence of the i-GaAs shell in the planar NWSC devices, induces a shadowing effect which reduces the effective absorption in the NW and limits the PCE of the planar SNWSC. Thus, an even higher PCE from the planar SNWSC is expected if this Ti/Au i-GaAs NW contact is omitted. However, this is not the purpose of this work, instead we have focused on a few fundamental structural and electrical issues which limit the PCE of radial p−i−n junction NWASCs.

Table 2. Summary of Key Performance Parameters from the Planar SNWSC and the NWASCs Studied in This Work

parameter	single NWSC device	NWASC device
device area[a]	0.17 μm^2	500 μm × 500 μm
V_{oc} (V)	0.72	0.52
I_{sc} (A)	35 pA	25.8 μA
J_{sc} (mA/cm^2)	20.1	10.3
V_{max} (V)	0.42	0.31
J_{max} (mA/cm^2)	13.2	6.8
FF (%)	38.6	39.4
PCE (%)	5.58	2.11

[a]Note that the NWs cover ∼14.4% of the NWASC device area.

4. CONCLUSIONS

In this work, we have demonstrated three different electrical measurement schemes alongside structural analysis of a radial p−i−n junction GaAs nanowire (NW) array solar cell, which allows us to correlate and understand how the nanohole mask, NW growth, and post-growth device processing impact the overall photovoltaic performance. Through this approach, an NW array solar cell device with a radial p−i−n junction NW geometry was first fabricated showing a high dark-mode leakage current density of ∼120 mA/cm^2 at −1 V, leading to a PCE of only ∼2.1%. The origin of this high leakage current was further investigated by measuring the p−i−n junction properties of individual as-grown NWs in the array utilizing a nanoprobing technique. Measurements on 20 NWs chosen randomly in the array show rectifying characteristics with a very low and a very high leakage current density for 12 and 5 NWs, respectively, whereas completely nonrectifying characteristics for 3 NWs, revealing a high degree of inhomogeneity in the electrical properties of the as-grown NWs in the array. In contrast to this, all of the fabricated planar SNWSCs show rectifying characteristics with a high on/off ratio and a higher PCE of ∼5.6%, indicating a severe leakage path through the substrate contact in the vertical configurations of the NWs. TEM analysis of the fabricated NWASC reveals an off-centered nucleation for the p-GaAs NW core growth with respect to the fabricated hole mask for a large percentage of the NWs in the array, leading to the possibility of a partial or full electrical shortening of the n-GaAs shell to the p-Si substrate. This is predominantly responsible for the high leakage current density and poor PCE measured from the NWASC alongside other artifacts like a high density of (111) twinning planes at the

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bottom of the NW and a high strain and lattice defect density observed close to the NW top. Such leakage current may be reduced if an alternative NW growth and device processing scheme is adopted, in which the bottom part of the NWs are passivated by an ALD dielectric layer after the p-GaAs NW core growth and where the subsequent NW shells can be re-grown afterward. Overall, our findings and approach provide critical insight into how different factors limit the solar cell efficiency of radial junction NWASCs, which will help to optimize and monitor the structural design of the NWs in future in order to further enhance the PCE.

■ ASSOCIATED CONTENT

Supporting Information

The Supporting Information is available free of charge at https://pubs.acs.org/doi/10.1021/acsanm.3c02031.

Simulated energy band alignment of p-Si/n-GaAs interface at equilibrium; semi-log $J-V$ characteristics of single planar NW solar cell in the dark and under 1 sun intensity @ AM 1.5G; semi-log $I-V$ characteristics of type I, type II, and type III vertical single NWs in the dark and under 1 sun intensity @ AM 1.5G; and calculated ideality factor (η) and reverse saturation current density J_0 (dark) for planar and vertical single-NW devices (PDF)

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Author Contributions

A.M. designed, fabricated, and characterized the NWASC and planar single NWSC devices. D.R. designed and grew the NWs. A.B.M. measured the single vertical NWs using the nanoprobing technique under the supervision of T.J.H. P.E.V. performed TEM studies on the fabricated NWASC device. A.M. wrote the manuscript with contribution from all authors. B.O.F. and H.W. supervised the project.

Notes

The authors declare no competing financial interest.

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