

A digital twin–based approach to reinforce supply chain resilience: simulation of semiconductor shortages

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Abstract. Semiconductor shortage adversely impacted industries and stress-tested supply chain (SC) resilience. One of the lessons learned through the semiconductor crisis is that low SC visibility intensifies the severity of the ripple effect caused by chip shortages. Digital SC twins have a high potential to assist resilience analysis in semiconductor SCs because the industry is rich in data and has deployed simulations for a long time. In this study, we examine how chip makers can cope with the ripple effect by the balanced approach combining case study and simulation. The case studies of Intel Corporation and Infineon Technologies reveal that both operational and disruption risks account for chip shortages. Manufacturing flexibility is the key resistance measure that the leading chip makers utilize. Efficient contingency plans, supplier collaboration, and repurposing help them in capacity adaptation. The simulation results underscore the consequences of disruption risks and exemplify an aggravated disruption overlay. We also discuss the **potential** employment of a digital SC twin to remedy ripple effect and deliver trusted solutions in the high time-pressure context.

Keywords: chip shortage, digital supply chain, supply chain resilience.

1 Introduction

Semiconductors are the technological backbone of modern products, and chip shortage is not a new topic. However, the acute chip insufficiency starting in 2021 is different. The automotive industry alone lost its potential sales of \$210 billion [1], urging supply chain (SC) practitioners to rebuild for resilience. Extant research highlighted the Covid-19 pandemic, the China-US trade war, and recent natural disasters as primary drivers of the semiconductor shortage [2, 3]. As adaptations, companies have launched both short-term and long-term measures. While production capacity and product mix variations are typical short-term tactics, investing in new capacity and enabling intertwined supply networks are deployed as long-term solutions [2, 4]. **The combination of short-term and long-term initiatives indicates that the chip deficit is beyond the individual internal or external shock. Besides, previous studies employ**

the qualitative approach [2] or focus particularly on the chip shortages in the automotive industry [3, 5]. This study aims to consider a comprehensive product portfolio from the chip manufacturer's perspective.

As shown by Ramani et al. [3], one of the major reasons for the semiconductor crisis is lack of visibility in SCs. In this setting, a digital SC twin approach deserves further examination. A digital SC twin is a computerized model, representing a physical SC network in real-time [6]. The combination of model-based and data-driven approaches unveils the complexity and interdependencies of different SC policies and hence provides insights to establish better operational strategies [6]. The virtual SC is also a source for experiments and simulations at a low cost and is especially useful in a data-driven context. The major difference between simulation and digital SC twins is the system integration to enable real-time data. Although a digital SC twin is a broader concept as simulation, simulation is an inevitable part of any digital SC twin. The semiconductor industry is rich in data and has deployed simulations in SC and operation management for a long time.

All the considerations above motivate us to investigate the impact of SC risks on semiconductor manufacturers for not only the automotive segment but also other segments and how semiconductor manufacturers cope with disruptions. After conducting case studies and a simulation, the authors utilize the results to describe the potential application of a digital SC twin to improve SC resilience.

2 Literature review

2.1 Ripple effect and disruption overlay

SC risks can be categorized into two groups: operational risks, which induce the bullwhip effect, and disruption risks, which cause the ripple effect [7]. Ripple effect refers to disruption transmission among actors in the SC network inducing material deficit at different echelons, and its related consequences [7]. Unlike bullwhip effect, ripple effect explains low-frequency-high-impact disruption risks [8]. When there is no action plan to remedy the ripple effect, its consequences propagate continuously both upstream and downstream of the SC and tend to accumulate over time [9]. The severity degree of the ripple effect depends on several variables, including network structure and disrupted nodes [9-11]. In the circular flow SC network, disruption inside circular flows ripples more intensively than outside disruption [11]. To boost SC resilience, Llaguno et al. [12] propose a framework with proactiveness measures and reactiveness measures in three pillars of robustness, redundancy, and flexibility.

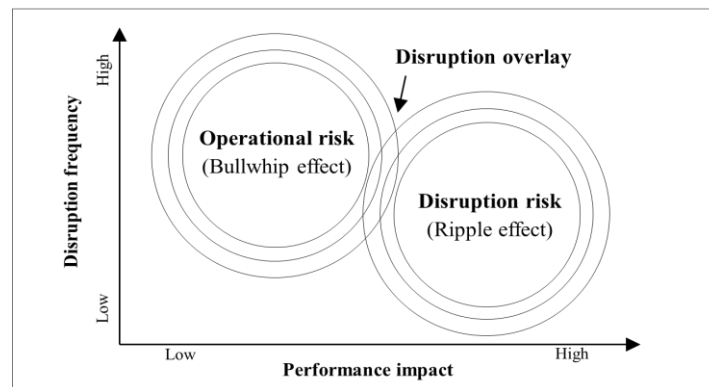


Fig. 1. Concept of disruption overlay.

A disruption overlay happens when operational risks intersect with disruption risks, potentially amplifying disruption propagations [13], see Fig. 1. A disruption overlay can be either reciprocal when one type of risk mitigates the other or aggravating when one type of risk exacerbates the other. To mitigate it, practitioners should focus on SC coordination (e.g., demand smoothing) while being cautious in ramping-up capacity, which is highly dependent on post-disruption demand [13].

2.2 Overview of semiconductor production

Producing chips is one of the most complex technologies with three principal stages: wafer fabrication (Fab), probe, and assembly and test (A&T). While Fab and probe are front-end operations, A&T is a back-end operation. The industry maintains four chronicle characteristics that have implications for SC management [14].

- **High capital intensity and considerable economies of scale.** Producing semiconductors requires specialized machines, lean rooms, and the significant cost of highly skilled labor [15]. For that reason, the industry is highly vertical disintegrated with different business models: fabless, integrated device manufacturer (IDM), and outsourced manufacturer. Besides, the integrated circuit industry depends on a few specialized enterprises. The manufacturing capacity hence relies upon key players and is vulnerable to disruption risks.
- **High level of uncertainty from supply and demand perspectives.** Chip production is low predictable because it requires thousands of steps, hundreds of inputs, and months to finish [15]. Chip performance, a key variable to segregate the finished product, is complex to project and can only be confirmed at the last production stage. Additionally, demand for semiconductors fluctuated around 40% - 70% in 1970-2000 [16].
- **An innovative industry with steeper product life cycles.** The industry has a remarkable variety of products and the product life cycle is getting shorter, increasing the complexity of SC planning process [15]. Although Intel is considered be-

hind its competitors, the company proved that its average time to **launch a higher performance product** has been improved from 2 years to 3.4 months [17].

- **Semiconductor SC is truly international.** While the US, Japan, and European are dominant in machinery, Taiwan, the US, and Japan play significant roles in the Fab processes [18]. A&T factories locate in China, Southeast Asia, and Taiwan due to cost structure and intellectual property protection strategy [18].

2.3 Digital supply chain twin and simulation of semiconductor industry

A digital SC twin is a digital dynamic simulation model of a real-world SC system, and a system can be a whole value network or a subnetwork [6]. The technology enables visibility for manufacturing sites, internal SC, and even a complete end-to-end (E2E) SC. Digital twins can be used to build experiments to observe the properties and attributes of every echelon, test the effectiveness of the business contingency plans, or simply monitor the SC performance. SC simulation in the semiconductor industry has a long history. Fowler et al. [19] proposed four levels in semiconductor SC simulation: tool and work center, manufacturing site, internal SC, and E2E SC. Researchers utilized the E2E simulation to evaluate operation policies and investigate the bullwhip effect in the semiconductor industry with automotive customers [5]. However, we are not aware of published research that deals with ripple effect analysis under long-term disruptions in semiconductor industry – a distinct contribution made by our study.

3 Research methodology

The authors apply the balanced approach comprising a case study and a discrete-event simulation. The method proposed can help avoid the trap of the “empirical elephant”, a metaphor to stress the importance of applying multiple techniques in operations and SC management [20].

Case study is a sound methodology to investigate the insufficient-theorized phenomenon [21]. A case study from a leading business provides practical insights and can be utilized as a benchmarking tool. The authors choose Intel Corporation (Intel) and Infineon Technologies (Infineon) for two reasons. First, the companies are highly representative of the semiconductor industry by offering a wide range of products in the global market. Second, they are IDMs who can offer the E2E SC view.

Simulation is an appropriate method to investigate SC performance over time [19, 22, 23]. The E2E SC simulation model allows for considering multiple elements within one model and examining the dynamic behaviors of a complex SC system [22]. Given that the research questions are to understand the dynamic behavior of semiconductor SCs under disruptions, discrete-event simulation is the appropriate modeling method. Discrete-event simulation (DES) models the system as it progresses over time by describing how the state variables transform instantaneously at separate events in time [19]. The approach is applied to analyze varied aspects related to E2E SC systems, especially in SC configuration with the provided set of SC policies and

operational parameters [23]. The chosen simulation engine in this study is anyLogistix, a proven software to perform DES [6, 23].

4 Case studies

4.1 Case study 1: Intel Corporation

Intel Corporation has a complex SC with six Fabs, four A&T facilities, 30 warehouse facilities, and 16000 suppliers to deliver annually 2 billion chips to approximately 2000 customers worldwide [24]. Gartner recognized Intel in Supply Chain Top 10 for ten consecutive years.

Operational risks. Intel recognized underinvestment. In 2020, the ratio of capital expenditure and cash flow of Intel (40%) was far lower than that of TSMC (62%) [24, 25]. Although its revenue doubled from 2009 (\$34 billion) to 2019 (\$68 billion), Intel did not launch any new Fab in this period. Like other chip makers, the company also depends on suppliers in Japan and Taiwan, who are particularly vulnerable to natural disasters. In its Q1'2022 financial statement, Intel highlighted the scarcity of substrate, dominated by suppliers in Japan and Taiwan [24]. The substrate is an essential material in the assembly process, where a die is bonded into the substrate to have the final product. A new product transition constitutes 20% of forecast volatility in Intel due to the "phantom demand" signals of OEM to secure capacity and maintain technological competitiveness [26].

Disruption risks. One of the most noticeable disruptive events that impacted Intel is the Covid-19 pandemic, which diluted the demand signal and exacerbated the capacity deficit. First, at the beginning of the Covid breakout, the industry had a pessimistic forecast; Intel, therefore, decided to slow down its production. Demand unexpectedly increased thanks to the trend of home-office and online learning. As a result, their saturated client product revenue increased by 12% in 2021 compared to 2020 [24]. Second, in 2021, all Intel A&T factories are in East Asia. Their primary backend production happens in Vietnam and China, which pursued "Zero Covid-19" policies. The policy requires strict measures and shrinks the availability of labor.

Resilience strategies. Intel has multiple resilience practices in place. The company established Pandemic Leadership Team to oversee its operation under disturbance events. Those deep and disciplined procedures are integrated into its operating model. Once the company senses the risk of material shortages, it quickly acquires materials, secures the material's buffer inventory, and improves material consumption. Besides putting the concerned material into the stricter monitor radar, Intel engineers seek possible alternative processes for single source materials. To mitigate the substrate constraints, Intel repurposes its machines innovatively. The company works closely

with its suppliers to determine their capacity bottleneck and configures the capacitor¹ attachment machines to operate constrained processes, avoiding a potential lost sale of \$2 billion [27].

To power its network capacity level optimization and quick ramp-up, the company fosters three principal concepts, "virtual factory," "copy exactly," and "fungibility," to govern its operational activities [28]. While the "virtual factory" ensures that every product is qualified in at least two factories, "copy exactly" is the protocol to maintain consistency between factories. Should any disruption happen, other factories can back up effectively. "Fungibility" refers to a tool's capability to process various products and operations that conventionally require several tools. The three concepts together enable its world-class manufacturing flexibility.

4.2 Case study 2: Infineon Technologies

Infineon Technologies, an automotive chip leader, operates with a global manufacturing footprint. As of September 2022, the company has 19 manufacturing facilities across the globe, including six facilities for front-end production, 12 facilities for back-end production, and one facility (Regensburg, Germany) for both front-end and back-end production [29]. The company interacts with thousands of suppliers headquartered in Asia Pacific (43%), Europe (33%), and the Americas (24%) [29].

Operational risks. Infineon highlights nine operational risks in the 2021 annual report. The top high operational risk includes dependence on individual suppliers and increasingly dynamic demand [30]. First, the recovery of suppliers after the Covid-19 pandemic and the continued supply gap due to hike-up demand in 2021 pose tremendous risks to its operation. Cypress, the largest-ever acquisition of Infineon, relies heavily on external manufacturers. Second, the market dynamic keeps evolving at an unprecedented pace, changing the way customers manage orders. The amount of "ghost orders" increases as customers tend to increase order quantity in the long-term horizon but make more frequent short-term adjustments. Although with a balanced customer portfolio, some products rely heavily on the customers' success.

Infineon classified supply planning and dependence on individual manufacturing sites as medium risks [30]. While ramp-up or transfer production is typically delayed, the high synchronization between front-end and back-end operations is getting more sophisticated due to more customized technology solutions, technology innovation pace, and stringent customer requirements. South-East Asian manufacturing sites are vital to its operations. The increasing political risks and disruptive events exacerbated the disadvantages of an unbalanced SC design.

Disruption risks. Infineon highlights three incidents in 2021. First, the flare-ups of Covid-19 induced capacity loss, particularly in Malaysia [30]. Stringent hygiene measures, the administration of vaccinations, and the pivotal role of semiconductors

¹ Capacitor is a component to mitigate noise and controls the voltage power to the chip.

in Malaysian economics allowed the company to produce. Second, in February 2021, a fabrication facility in Austin suffered a severe winter. The electricity shortage, with the gas and water supply gap, paused production in Austin for more than two weeks. The facility took five months from February 2021 to July 2021 to recover. Third, in September 2021, a power outage occurred in Dresden and interrupted the Fab there. According to Infineon, the site revamped its production in the following weeks.

Resilience strategies. Infineon has deployed a triple-A strategy, Agility – Adaptability – Alignment, to overcome the complexity in the semiconductor industry [5]. The company fuel its flexibility by utilizing both external manufacturing partners and in-house manufacturing [30]. Infineon also deploys “One Virtual Fab” which ensures the same process and practices in defined factories. The company has been deploying SC simulations to make informed decisions for years. Some noticeable works include simulating recovery strategies to enhance resilience, simplifying for changing product mix scenarios, and evaluating SC disruptions in an E2E SC [5].

Beyond simulations, Infineon implements digital twins since 2019 in facility management and training. The new research building in Austria is constructed physically and virtually simultaneously. Training is a fruitful area to deploy digital twins, especially in experiential learning by reducing the stress factor and eliminating the risk of scrapping costly wafers [31]. A digital SC twin can simplify production control in a high-mix-high-volume context [32]. Several communication protocols have been established to cascade information of operational parameters (lot disposal, released quantity...). Digital twins offer seamless and human-free communication flow by computerizing processes and integrating optimizers. An activity like lot disposal no longer relies on the experience of operators and their physical response.

5 Data model and experiment design

5.1 Data model

Our simulation model is inspired by the Infineon case with verifiable assumptions. Fig. 2 depicts the five considered echelons in this study: Fab, substrate supplier, A&Ts, distribution centers (DCs), and customers. Given the complexity of considering all the production facilities into one single model, the authors select one Fab, one substrate supplier, three A&T facilities, and two DCs to unravel the chip deficit. The production flow starts at Fab where wafer materials are transformed into dies. The authors select the in-house Fab in Dresden for this model. In A&T, dies are mounted into substrates, produced by a substrate supplier. There are three chosen back-end facilities: Melaka (Malaysia), Tijuana (the US), and Wuxi (China). Finished good is shipped to DCs and subsequently to customers, who are the original equipment manufacturers (OEM) or distribution partners. DCs in Europe and Shanghai are selected. Regarding the customers, the authors consider the top 10 direct customers in 2021 and group other customers into seven geographical categories.

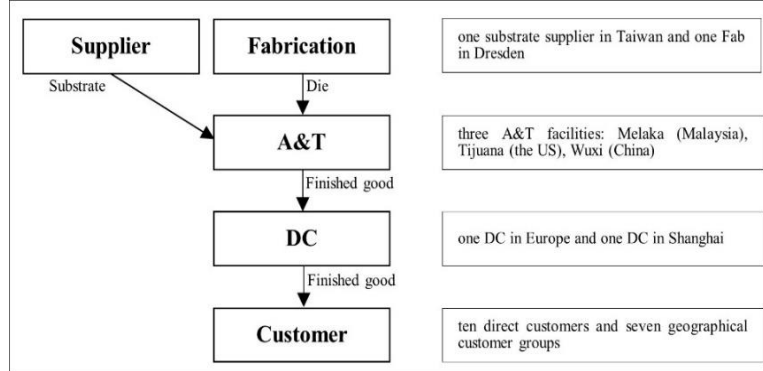


Fig. 2. Overview of DES E2E SC simulation model.

The price is the public price retrieved from Digi-Key Electronics website [33]. To estimate the price, the authors choose three products in each category. Based on the order lot size of 20,000 pieces/lot and the price, the authors calculate weekly demand in Table 1. The industry typically deploys air shipment. The shipment cost per trip ranges from €500 to €3500, and it is retrieved from Airrates.com website [34]. The lead time is one day for one delivery in this model. Other costs in A&T are assumed based on the 2021 annual report [30], see Table 2.

Table 1. Weekly demand per product and customers (in lot).

Product		A	B	C	D
Price per piece		€11.5	€15.2	€27.8	€18.9
Direct customers	Astemo	15	-	-	-
	Bosch	15	-	-	-
	Continental	15	-	-	-
	Delta	-	-	-	156
	Denso	15	-	-	-
	Hyundai	15	-	-	-
	Samsung	-	-	-	155
	Thales	-	46	-	-
	vitesco	15	-	-	-
	zf	15	-	-	-
Other customers	Americas	34	21	44	141
	Germany	34	21	45	144
	EMEA (exclude Germany)	40	25	53	168
	Japan (JP)	30	18	39	123
	Macau & Hong Kong (MC & HK)	86	53	112	358
	China & Taiwan (CN & TW, exclude MC & HK)	27	17	36	114
APAC (exclude JP, MC, HK, CN & TW)	47	29	62	196	

Table 2. Assumed costs per product and A&T facilities.

	Fixed cost (k€/day)	Variable cost (k€/lot)			
		A	B	C	D
A&T Melaka	120	170	230	180	240
A&T Tijuana	180	180	250	190	230
A&T Wuxi	100	170	250	190	240

5.2 Experiment design

Semiconductors suffered tremendous disruptions throughout 2021, and some events lasted for months [2, 3, 30]. Based on those real-world events, the authors design six experiments (Exp.) as follows:

- Exp. 1: Two-week disruption in Fab in 01.02.2021-15.02.2021.
- Exp. 2: Two-week disruption in substrate suppliers in 01.04.2021-15.04.2021.
- Exp. 3: One-month disruption in A&T facilities in 01.05.2021-31.05.2021.
- Exp. 4: All disruptions happened in experiments 1-3.
- Exp. 5: Fluctuating demand of multiple products in 01.02.2021-01.07.2021.
- Exp. 6: All events happened in experiments 1-3 and 5.

6 Results and discussion

6.1 Results of experiments related to disruption risks

Table 3 summarizes key indicators to compare the results of different experiments. Experiment 1 investigates the impact of the two-week shutdown in Fab. Although the incident induces a loss sale of €453 million (4% revenue), the expected lead time (ELT) service level reduces significantly to 78.3%. ELT service level is the ratio of on-time orders to the total number of orders in terms of revenue. On-time orders are the orders delivered within the ELT (30 days in this study). 15% of delivery has lead time longer than 30 days. Moreover, the disruption happens in March, but nine months of operation cannot fully recover the service level.

Table 3. Summary of computational results.

Indicator	Baseline	Exp. 1	Exp. 2	Exp. 3	Exp. 4	Exp. 5	Exp. 6
Revenue (€ million)	11,062	10,609	10,609	10,203	9,777	11,109	9,759
Total cost (€ million)	6,837	6,596	6,596	6,373	6,130	6,838	6,131
Profit (€ million)	4,224	4,013	4,013	3,830	3,647	4,272	3,629
Demand (1000 Orders)	138.9	137.6	137.6	133.9	131.2	140.4	132.8
Backlog (1000 Orders)	7.4	12.6	12.6	12.5	17.6	8.9	19.1
Backlog / Demand	5%	9%	9%	9%	15%	6%	14%
Fulfillment (Late Orders)	-	270	216	950	1,065	-	1,187
ELT service level	100%	78.3%	82.6%	44.2%	35.3%	100%	30.3%
Time-to-survive	-	27	31	29	27	-	27
Min lead time (day)	1.0	1.0	1.0	1.0	1.0	1.0	1.0
Median lead time (day)	7.2	21.2	15.0	8.0	32.0	14.2	44.2
Max lead time (day)	8.0	32.0	32.0	39.0	62.0	21.3	72.0

Experiment 2 examines the substrate shortage alone. The financial impact is not surprisingly the same as that of experiment 1. The possible reasons are that the supply gap time is two weeks and that the consumption rate is the same for die and substrate while the demand is constant. However, the ELT service level reaches 82.6% because

the incident happens in April and the company has four months to accumulate performance before the disruption. The lead time distribution indicates a more predictable performance with half of the delivery within two weeks.

The results of experiment 3 show the impact of one month stop production in A&Ts. Although the disruption lasts one month (6% of the time in one year) and demand is constant, the revenue and profit reduce by up to 10%. The SC in this simulation can survive 29 days after the disruptive event started in experiment 3. Although the time-to-survive varies among experiments, the longest time-to-survive is only 31 days, underscoring the need to take immediate action.

Experiment 4 is the combination of all three experiments above. The series of disruptions constitutes the lost sale of €1.3 billion. The SC realizes its performance degradation since day 60, which is 27 days since the first event happens. Half of the delivery has a lead time of more than 30 days, justifying the low service level.

6.2 Operational risks and disruption overlay

Experiment 5 investigates the impacts of fluctuating demand, which represents operational risk. The financial indicators are slightly improved, and the ELT service level maintains at 100%. Although the delivery time is longer than the lead time in the baseline, all the orders are shipped within the ELT. The results indicate that the chip maker in this simulation can cope with, and even benefit from, the operational risk. **While Jaenichen et. al. [5] successfully describes the behavior of each echelon in the SC under the volatile demand scenario; their results do not include the impact of operational risk. The finding in experiment 5 hence extends the results of Jaenichen et. al. [5].**

Experiment 6 includes all the incidents in previous experiments. It aims to uncover the causes of the chip deficit that started in 2021. While a series of disruptive events generate a lost sale of €1.3 billion, the operational risk induces a gain revenue of €50 million. With conventional knowledge, one would guess that the performance in experiment 6 would be better than that of experiment 4. However, it is counter-intuitive that the financial performance gets even worse despite the potential gain from fluctuating demand. The simulated SC has revenue of €9.76 billion and a profit of €3.63 billion, which is €18 million and €20 million respectively less than the result in experiment 4 as Fig. 3 illustrates. The experiment illustrates the aggravated disruption overlay that happens when operational risks intersect with and amplify disruption risks. In other words, both operational risks and disruption risks constitute the acute semiconductor shortage. This result can help to explain why several companies expand their capacity to reinforce resilience besides geopolitical reasons. **Besides, the result in experiment 6 aligns with the findings from previous studies [2, 3] and underscores the impact of disruption overlay to the semiconductor deficit.**

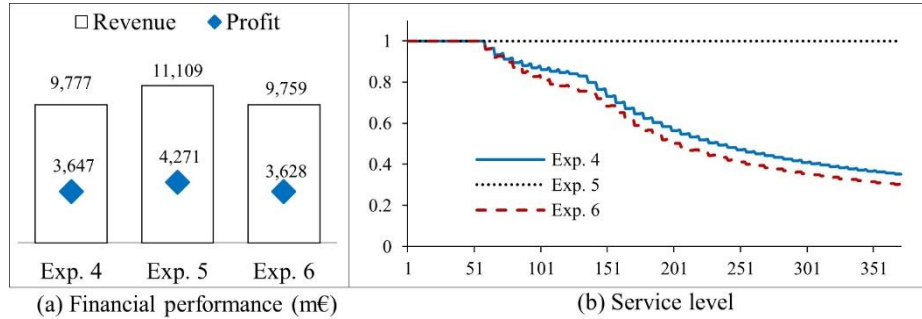


Fig. 3. Chip shortage illustrates an aggravated disruption overlay.

The service performance drops to 30.3%, and the median lead time is 44.2 days in experiment 6. Poor service implies a high risk of losing the market share and challenges for downstream echelons to plan their production. Additionally, with this theoretical performance, the shortage is unlikely to be recovered in a short time.

6.3 The potential role of digital SC twin

Resilience strategies include both proactive preparedness and reactive measures. In business-as-usual scenarios (i.e., no disruptions), a digital SC twin can provide quantitative tools for decision-making and supply network designs. The simulation capability can help assess the right suppliers, the right number of suppliers, or the right risk mitigation inventory in terms of cost and SC resilience. Integrating operational management systems into a digital SC twin can enhance training and learning experiences. Therefore, SC practitioners can deploy the technology to improve their competencies and prepare for disruption events. Several applications based on digital SC twin have been developed to manage complex manufacturing environments. Computerized processes and integrated optimizers simplify sophisticated operations and reduce human dependency. Companies can also build digital SC twin applications to sense SC risks and monitor compliance practices. An integrated machine learning algorithm can scrutinize multiple data sources, check data quality, and assess the impact of potential risks in the early stage. After verifying information, SC managers can quickly develop preventive actions by simulating varied scenarios without the necessity to model repetitive problems.

During disruptions, a digital SC twin can leverage real-time data and trusted algorithms to enable effective decision-making and action plan cascading procedures in a time-sensitive context. The simulation indicates that the time-to-survive depends on the inventory level, which is relatively low in this study (approximately 30 days). Therefore, efficient contingency plans are pivotal. Large-scale organizations like semiconductor manufacturers usually maintain several challenges to addressing short-term issues. Gathering necessary data and getting the solutions approved consume significant time, reducing the solutions' efficiency or even making solutions obsolete. Lower data latency and trusted simulation models empower the solution design process and maximize the potential benefits of the solution. Besides, companies can de-

velop an integrated optimizer to allocate the constraint resources automatically based on the set of prioritization rules. For example, in the substrate shortage experiment, we can build an integrated optimizer to reduce the order batch size, prioritize distributing substrates to high-margin products, and communicate the results to operational systems. The advancement can mitigate the impacts of material shortages while waiting for strategic solutions, which can be made by humans only.

7 Conclusion

We deploy a balanced approach to unravel the impact of ripple effect under long-term disruptions in semiconductor industry. The case studies of Intel and Infineon indicate that both operational risks and disruptive events can lead to semiconductor shortages. To remedy ripple effect, leading chip makers utilize proactiveness measures (e.g., manufacturing flexibility, triple-A strategy) and reactiveness measures (e.g., effective business contingency plan, repurpose). DES E2E SC simulation emphasizes the severity of disruptions, illustrates aggravated disruption overlays, and provides examples of how chip makers can leverage a digital SC twin to cope with ripple effect. The technology empowers trusted solutions in a timely manner. **Additionally, our study contributes an E2E SC simulation model to investigate the ripple effect and delineates use cases to develop digital SC twin solutions.**

The study has two primary limitations. First, the results are low generalized because of the case study method and Infineon-inspired simulation model. Second, the study may not have a superior level of accuracy since the simulation model needs to be simplified to cover multiple SC echelons and some assumptions need to be made based on secondary data. Besides addressing these limitations, future research can explore the challenges to roll out digital SC twins and the measures to accelerate technology adoption.

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