Fault Detection, Localization and Clearance for MMC based on Indirect Finite Control Set Model Predictive Control

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***Abstract*—In this paper, indirect finite control set model predictive control (I-FCS-MPC) is used for detecting, localizing, and tolerating open-circuit failures in the transistors without the use of arm voltage sensors. The fault is detected by the main controller whereas the localization is performed in the local controller which is used for the sorting algorithm. The main controller utilizes the discrete mathematical model to estimate the arm voltages using state measurements from present and previous sampling instants. The arm voltage command given by the main controller in the previous sampling instant is then compared with the estimated arm voltage to detect the fault. The fault signal is sent to the local controller where a counter is increased for the potential faulty submodules (SMs). The fault is then localized to the specific SM whose count first goes above a threshold value. Finally, this SM is bypassed using a bypass switch and a redundant SM is inserted in its place. The proposed fault detection and localization method does not require any additional sensors. Simulation results demonstrate that the fault can be detected, localized, and cleared within one fourth of the fundamental period.**

***Index Terms*—circulating current, capacitor voltage balancing, fault detection, fault tolerance, model predictive control (MPC), modular multilevel converter (MMC)**

I. Introduction

Modular multilevel converters (MMCs) have many excellent features such as modular structure, reduced filter requirements, reduced voltage stress on switches, redundancy, and high-quality output voltage [1]–[5]. These features have made MMCs the most promising technology for high voltage applications such as high voltage direct current transmission systems (HVDC).

One of the main concerns for MMC is reliable operation as it consists of a large number of power semiconductor switches which are the most fragile components in power electronics systems [6]. According to an estimate 38% of the faults in power systems are due to the failure of these power semiconductor devices [7]. It is desirable that MMC operation is not interrupted, in particular for HVDC applications, even if some of the submodules (SMs) fail [9]. Therefore, an efficient fault tolerant control strategy that detects and tolerates the SM faults quickly is required to ensure reliable operation of the MMC. Various methods of fault detection and tolerance for MMCs have been studied in literature [8]–[25]. Some of these methods use redundant SMs for instance [8], [9] and some do not utilize redundant SMs [12], [25] for fault tolerant operation. In strategies that do not utilize redundant SMs, the loss of a faulty SM will generally cause an increase in the voltage of all other SMs to compensate for the faulty SM. These strategies increase the stress on SM components and would not work if this increased voltage is higher than the rated value for SM capacitor voltage. The methods that use redundant SMs simply bypass the faulty SM and insert the redundant SM in its place.

Most of the existing methods on fault tolerant operation of the MMC are proposed for conventional cascade based control of MMCs. In recent years, model predictive control (MPC) has emerged as a promising control technique for MMCs as it can easily handle the MMC's multi-input multi-output (MIMO) nature, the non-linearity of MMCs, as well as time delays and constraints. However, the study of fault-tolerant operation for MMC based on the MPC approach is limited [26] and only a few [6], [22], [24], [25] have considered MPC for fault-tolerant operation. Among these, the MPC techniques for fault detection and tolerance proposed in [6], [22] are based on the switching states. Therefore, its computational complexity would become very high when the number of SMs in each arm of MMC are high such as for HVDC applications, thus making their real time application impractical. The method proposed in [24] tolerates a single SM fault by adding an extra switch in the MMC structure. However, this modification changes the location of arm inductance and thus the mathematical model of MMC. In [25], it is assumed that the fault is detected and only fault tolerant operation is considered without redundant SMs. As it does not consider redundant SMs, the operating range would be limited.

In recent years, many works based on MPC have been proposed for MMC [26]. The main research efforts have been to reduce the computational complexity for making the real-time application of MPC for MMC possible. Therefore, the MPC strategy that is preferred for MMC is indirect FCS-MPC where optimization over voltage levels instead of switching states is performed. In this paper, the fault detection, localization, and tolerance scheme based on indirect FCS-MPC [27] for MMC using redundant SMs is proposed.

The fault detection is performed by the main controller where MPC generates the optimal insertion index (number

of SMs to be inserted). The fault detection is based on the comparison of the estimated arm voltage with the arm voltage commanded by the MPC in the previous sampling instant. The estimated arm voltage using the mathematical model of MMC is calculated from the state measurements in the present and previous sampling instant. The main controller is sending the fault signal to the local controller where sorting is being performed. Once, the fault signal is true, then the counter for the potential faulty SMs is increased. The SM whose count first goes above a threshold value is the faulty one and it is then bypassed using the bypass switch and replaced by some redundant SM. It is further noted that the open-circuit fault in an SM can be due to any of the two switches. Therefore, a separate counter for each type of fault is used. The main contributions can be summarized as:

- A fault detection and tolerance method for open-circuit fault in SM based on indirect FCS-MPC is proposed
- The proposed method does not require any additional sensors.
- The proposed method can be used to detect faults in multiple SMs
- The proposed algorithm can distinguish between faults caused by the two switches of the SM.

The rest of the paper is organized as follows. The basic operation and mathematical model of the MMC is developed in Section II. In Section III, the behaviour of MMC under open-circuit IGBT faults is discussed. The proposed method is presented in Section IV and the indirect FCS-MPC strategy is discussed in Section V. Finally, the performance of the proposed strategy is demonstrated by simulations in Section VI which is then followed by the conclusion section.

II. Model of the MMC

The same model development is followed in this paper as in [27]. The three-phase MMC configuration shown in Fig. 1 is the most common topology for MMCs used in HVDC applications. The MMC consists of three identical phase legs. Each phase-leg of the MMC consists of two arms *i.e.*, an upper arm (denoted by subscript 'u') and a lower arm (denoted by subscript 'l') connected to the positive and negative dc terminal, respectively. Each arm consists of N identical half-bridge submodules (SM), and an inductor. The arm inductor is used to limit the harmonics and fault currents. The arm resistance shown in Fig. 1 is used for modeling the losses of the MMC. Depending on the switching states of S_1 and S_2, each SM can provide two voltage levels *i.e.*, 0 or $v_{\mathrm{Cm_{i,j}}}$ where m=u,l; i=1,2,...,N, j=a,b,c. Moreover, each SM has a bypass switch 'B' which can be used to bypass the faulty SM.

The per-phase mathematical model of the MMC shown in Fig 1, with respect to a fictitious midpoint 'O' can be expressed as:

$$\frac{V_{dc}}{2} - v_{u,j} - Ri_{u,j} - L\frac{di_{v,j}}{dt} + R_c i_{v,j} + L_c\frac{di_{v,j}}{dt} - v_f = 0 \quad (1)$$

$$\frac{V_{dc}}{2} - v_{l,j} - Ri_{l,j} - L\frac{di_{l,j}}{dt} - R_c i_{v,j} - L_c\frac{di_{v,j}}{dt} + v_f = 0 \quad (2)$$

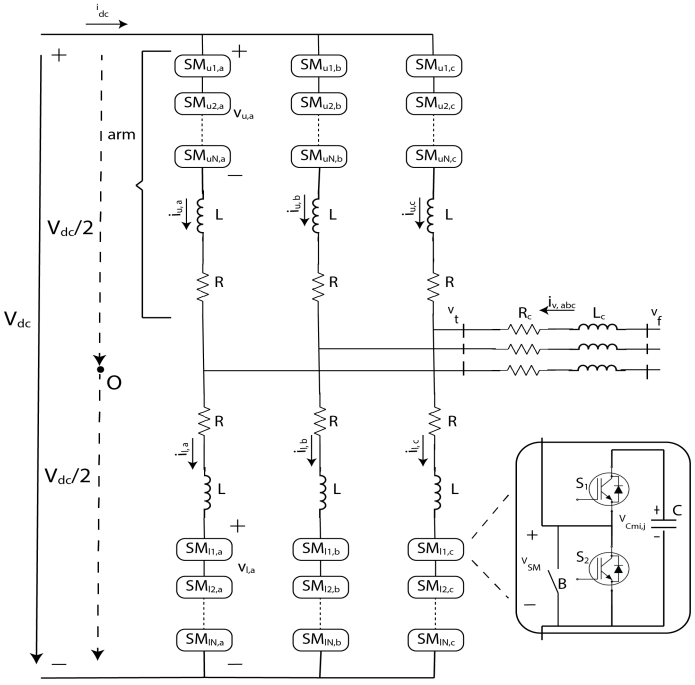

Fig. 1: Circuit Diagram of MMC

where $v_{u,j}$ and $v_{l,j}$ represent the upper and lower arm voltages of phase j, $i_{u,j}$ and $i_{l,j}$ represent the upper and lower arm currents of phase j, $i_{v,j}$ is the ac-side current, V_{dc} is the dc-side voltage, v_f is the grid side voltage, R is the arm resistance, L is the arm inductance, R_c and L_c are the grid side converter resistance and inductance, respectively.

The ac-side current, circulating current and arm currents are given by:

$$i_{v,j} = i_{l,j} - i_{u,j} \quad (3)$$

$$i_{cir,j} = \frac{i_{u,j} + i_{l,j}}{2} \quad (4)$$

$$i_{u,j} = -\frac{i_{v,j}}{2} + i_{cir,j} \quad (5)$$

$$i_{l,j} = \frac{i_{v,j}}{2} + i_{cir,j} \quad (6)$$

where $i_{cir,j}$ is the circulating current.

By subtracting (1) and (2) and using (3) the dynamic equation for the ac-side current is obtained as:

$$\frac{di_{v,j}}{dt} = \frac{-(R+2R_c)}{L+2L_c} i_{v,j} + \frac{v_{u,j} - v_{l,j}}{L+2L_c} + \frac{2v_{f,j}}{L+2L_c} \quad (7)$$

Similarly, by adding (1) and (2) and using (5) and (6), the dynamic equation for the circulating current is obtained as:

$$\frac{di_{cir,j}}{dt} = \frac{-R}{L} i_{cir,j} - \frac{1}{2L}(v_{u,j} + v_{l,j}) + \frac{1}{2L} V_{dc} \quad (8)$$

The arm voltages $v_{u,j}$ and $v_{l,j}$ depend on the number of SMs inserted in that arm. Assuming that SM capacitor voltages are well balanced at their reference values, the arm voltages can be expressed as:

$$v_{u,j} \approx \frac{n_{u,j}}{N} v_{u,j}^{\Sigma} \quad (9)$$

$$v_{l,j} \approx \frac{n_{l,j}}{N} v_{l,j}^{\Sigma} \tag{10}$$

where $n_{u,j}$ and $n_{l,j}$ are the number of SMs to be inserted in upper and lower arm respectively and $v_{u,j}^{\Sigma}$ and $v_{l,j}^{\Sigma}$ are the summation of all capacitor voltages in the upper and lower arm respectively.

The dynamics of the total arm capacitor voltages can be expressed as:

$$\frac{dv_{m,j}^{\Sigma}}{dt} = \frac{i_{m,j}}{C_{m,j}^{e}} = \frac{n_{m,j} i_{m,j}}{C} \tag{11}$$

where $C_{m,j}^{e}$ is the equivalent arm capacitance of inserted SMs in arm m. Now equations (5) and (6) can be substituted into (11) to give the following dynamic equations for total arm capacitor voltages of both arms:

$$\frac{dv_{u,j}^{\Sigma}}{dt} = -\frac{n_{u,j} i_{v,j}}{2C} + \frac{n_{u,j} i_{cir,j}}{C} \tag{12a}$$

$$\frac{dv_{l,j}^{\Sigma}}{dt} = \frac{n_{l,j} i_{v,j}}{2C} + \frac{n_{l,j} i_{cir,j}}{C} \tag{12b}$$

Using the definition of $v_{u,j}$ and $v_{l,j}$ from (9) and (10) into (7) and (8), the dynamic equations for ac-side current and circulating current are modified as:

$$\frac{di_{v,j}}{dt} = \frac{-(R+2R_c)}{L+2L_c} i_{v,j} + \frac{n_{u,j} v_{u,j}^{\Sigma} - n_{l,j} v_{l,j}^{\Sigma}}{N(L+2L_c)} + \frac{2v_{f,j}}{L+2L_c} \tag{13a}$$

$$\frac{di_{cir,j}}{dt} = \frac{-R}{L} i_{cir,j} - \frac{(n_{u,j} v_{u,j}^{\Sigma} + n_{l,j} v_{l,j}^{\Sigma})}{2NL} + \frac{V_{dc}}{2L} \tag{13b}$$

Using (12) and (13) the state space equation of the MMC is shown by (14) where $x = [i_{v,j}, i_{cir,j}, v_{u,j}^{\Sigma}, v_{l,j}^{\Sigma}]^T$ is the state vector and $u = [u_1 u_2]^T = [n_{u,j} n_{l,j}]^T$ is the input vector.

$$\dot{x}(t) = \begin{bmatrix} \frac{-(R+2R_c)}{L+2L_c} & 0 & 0 & 0 \\ 0 & \frac{-R}{L} & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \end{bmatrix} x(t) + \begin{bmatrix} 0 & 0 & \frac{1}{(L+2L_c)N} & 0 \\ 0 & 0 & \frac{-1}{2NL} & 0 \\ \frac{-1}{2C} & \frac{1}{C} & 0 & 0 \\ 0 & 0 & 0 & 0 \end{bmatrix} x(t)u_1 + \begin{bmatrix} 0 & 0 & 0 & \frac{-1}{(L+2L_c)N} \\ 0 & 0 & 0 & \frac{-1}{2NL} \\ 0 & 0 & 0 & 0 \\ \frac{1}{2C} & \frac{1}{C} & 0 & 0 \end{bmatrix} x(t)u_2 + \begin{bmatrix} \frac{2v_f(t)}{(L+2L_c)} \\ \frac{V_{dc}(t)}{2L} \\ 0 \\ 0 \end{bmatrix} \tag{14}$$

Based on (14), and a sampling time of T_s the discrete-time model of the system is given by forward Euler approximation:

$$x(k+1) = \begin{bmatrix} 1 - \frac{T_s(R+2R_c)}{L+2L_c} & 0 & 0 & 0 \\ 0 & 1 - \frac{T_s R}{L} & 0 & 0 \\ 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 1 \end{bmatrix} x(k) + \begin{bmatrix} 0 & 0 & \frac{T_s}{(L+2L_c)N} & 0 \\ 0 & 0 & \frac{-T_s}{2NL} & 0 \\ \frac{-T_s}{2C} & \frac{T_s}{C} & 0 & 0 \\ 0 & 0 & 0 & 0 \end{bmatrix} x(k)u_1(k) + \begin{bmatrix} 0 & 0 & 0 & \frac{-T_s}{(L+2L_c)N} \\ 0 & 0 & 0 & \frac{-T_s}{2NL} \\ 0 & 0 & 0 & 0 \\ \frac{T_s}{2C} & \frac{T_s}{C} & 0 & 0 \end{bmatrix} x(k)u_2(k) + \begin{bmatrix} \frac{2T_s v_f(k)}{(L+2L_c)} \\ \frac{T_s V_{dc}(k)}{2L} \\ 0 \\ 0 \end{bmatrix} \tag{15}$$

Equation (14) & (15) show that the MMC is a bilinear system with multiple inputs and outputs. This introduces non-linearity through the product of the states and inputs.

III. MMC Behavior Under Open Circuit Faults

The SM configuration is shown in Fig. 1. There are two switches, therefore there can be two types of faults *i.e.*, fault due to S_1 and fault due to S_2. The characteristics of SM with and without fault are summarized in Table I. It can be observed from Table I that the S_1 fault impact occurs only when the arm current is negative and S_2 fault impact occurs when the arm current is positive. Both types of faults will result in increased voltage of that SM with respect to normal SMs *i.e.*, during an S_1 fault the capacitor cannot discharge, and under an S_2 fault the capacitor overcharges.

TABLE I: SM capacitor Characteristics under normal and faulty conditions

Operation	$i_{u,l,j}$	SM State	Capacitor	Output Voltage
Normal	>0	Inserted	Charged	v_{SM}
	<0	Inserted	Discharged	v_{SM}
	>0 or <0	Bypassed	Unchanged	0
S_1 fault	>0	Inserted	Charged	v_{SM}
	<0	Inserted	Unchanged	0
	>0 or <0	Bypassed	Unchanged	0
S_2 fault	>0	Inserted	Charged	v_{SM}
	<0	Inserted	Discharged	v_{SM}
	>0	Bypassed	Charged	v_{SM}
	<0	Bypassed	Unchanged	0

IV. Proposed Fault Detection and Fault Tolerance Method

A. Fault Detection

From Table I the following two main observations are used for fault detection:

- Obs1: if the fault is due to S_1 then the actual arm voltage would be less than the commanded arm voltage from the MPC whenever the faulty SM is in inserted state and arm current is negative.
- Obs2: if the fault is due to S_2 then the actual arm voltage would be more than the commanded arm voltage from the MPC whenever the faulty SM is in bypassed state and arm current is positive.

It is noted here that the main controller does not need either the information of arm current direction nor whether an SM was inserted or bypassed to detect the fault.

The proposed method utilizes the mathematical model of the MMC for fault detection. Discretizing (7) and (8) and solving for arm voltages with measurements at present and previous sampling instants, the following expressions are obtained for estimated arm voltage at the previous sampling instant:

$$v_{u,j,est}(k-1|k) = \frac{H_1 - H_2}{2} \tag{16a}$$

$$v_{l,j,est}(k-1|k) = \frac{H_1 + H_2}{2} \tag{16b}$$

where

$$H_1 = (i_{v,j}(k) - i_{v,j}(k-1)) \frac{L+2L_c}{Ts} + Ri_{v,j}(k-1) - 2V_{f,j}(k-1) \tag{17}$$

$$H_2 = (i_{cir,j}(k) - i_{cir,j}(k-1))\,\frac{2L}{Ts} + 2Ri_{cir,j}(k-1) - V_{dc} \tag{18}$$

The estimated arm voltages in (16) are compared with the commanded arm voltage by the main controller (MPC) in the previous sampling instant. The commanded arm voltages are given as:

$$v_{u,j,cmd}(k-1|k) = \frac{n_{u,j}(k-1)v^{\Sigma}_{u,j}(k-1)}{N+M-F_u} \tag{19a}$$

$$v_{l,j,cmd}(k-1|k) = \frac{n_{l,j}(k-1)v^{\Sigma}_{l,j}(k-1)}{N+M-F_l} \tag{19b}$$

where M is the number of redundant SMs and $F_{u/l}$ are the number of faulty SMs in the upper and lower arm.

Based on the observations Obs1 and Obs2, whenever the voltage in (16) is less than that from (19) by at least $V_{dc}/N \pm ripple$ then the fault is detected and it is due to S_1 and whenever the voltage in (16) exceeds that of (19) by at least $V_{dc}/N \pm ripple$ then the fault is detected and it is due to S_2. It is noted here that the difference between (16) and (19) should be at least $|V_{dc}/N \pm ripple|$ for the fault to be valid.

B. Fault Localization and Clearance

Although the fault has been detected by the previous method, the information about which SM is faulty is still unknown and therefore the fault cannot be cleared yet. The fault localization is performed in the local controller where sorting is performed. The fault signal from the main controller with the information about the fault type *i.e.*, due to S_1 or S_2 is sent to the local controller. The local controller maintains two counters for each SM. If the fault was due to S_1 then the counter 1 of each inserted SM in the previous sampling instant is increased. If the fault was due to S_2 then the counter 2 of each bypassed SM in the previous sampling instant is increased. Then the SM whose count first goes above a threshold value is identified as the faulty SM and $F_{u/l}$ is increased. The faulty SM is then bypassed using the bypass switch and is replaced by one of the redundant SMs. Thereafter the counter of each SM is set to zero again so that any other faulty SM can be identified as well. The information about the faulty SM is preserved by keeping an array of bypass switch states.

It is noted here that the MMC is operated in hot reserve mode where the redundant SMs are also equally treated by the control algorithm i.e., kept at V_{dc}/N. The overall flowchart for the proposed method is shown in Fig. 2 where F_{s1} and F_{s2} are fault flags for S_1 and S_2 faults, respectively.

C. Selection of Threshold Value

In this work, the threshold for the counter is fixed to $N/2+3$ where N is the total number of SMs without redundant SMs. Therefore, the SM whose count reaches this threshold first is the faulty one. The threshold value chosen will ensure that no healthy SM is mistaken for a faulty SM. As in the worst case for S_1 fault, the initial fault could happen when the insertion index is equal to N then the insertion index needs to be less than N for at least $N/2$ times under fault conditions so that all the healthy SMs have been put out of operation at least once by the conventional sorting algorithm [5]. As there can be cases when the insertion index remains N for one or two sampling instants under fault conditions so an additional 3 is added to $N/2$. Similarly, for the worst case of S_2 fault, the initial fault could happen when the insertion index is 0 and then the insertion index needs to be more than 0 for at least $N/2$ times under fault conditions so that all the healthy SMs have been put in operation at least once by the sorting algorithm. The additional 3 is added for the same reason that the insertion index can remain 0 for one or two sampling instants under fault conditions.

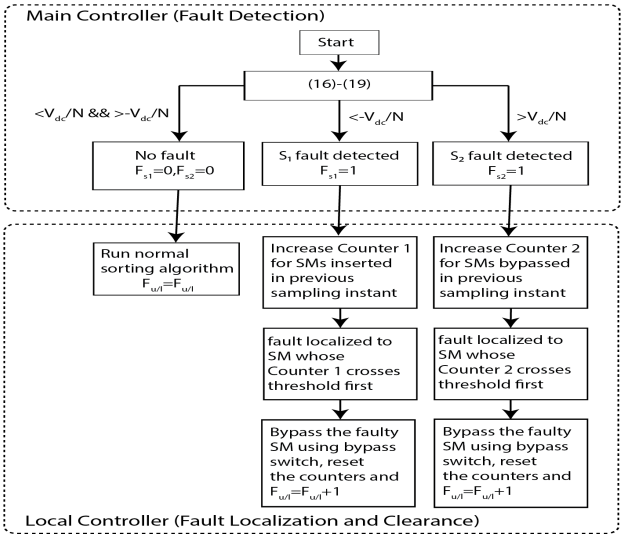

Fig. 2: Flowchart for the proposed method

It is worth pointing out that although the threshold value is dependent on the total number of submodules, the fault can be still detected and cleared within one fundamental period. This is due to the advancement in processor technology which has made possible the realization of much lower sampling times for instance $50\mu s$ which means for an ac wave of 50 Hz a fundamental period will be completed in 400 sampling instants. Typically for high voltage applications the number of SMs ranges from 200 to 400 SMs/arm [2] thus resulting in an $N/2$ of 200 for worst case scenario which is half of the sampling instants required for completing one fundamental period of a 50 Hz wave.

V. INDIRECT FCS-MPC

In this work, the indirect FCS-MPC technique is adopted from [27]. The method presented in [27] is a computationally efficient implementation of indirect FCS-MPC for MMCs and gives an almost identical dynamic response as full indirect FCS-MPC. In full indirect FCS-MPC all the voltage levels are evaluated to perform optimization, whereas in [27] a small neighborhood of voltage levels is considered with respect to the voltage level applied at the previous sampling instant. In addition, this method also allows for larger changes only in

the initial time step within the prediction horizon to react faster to larger disturbances. The changes considered in [27] are 0, ± 1, and ± 5 at the initial time step and 0, ± 1 for all subsequent time steps. The details of the cost function and reference signals follow.

A. Cost Function

The cost function adopted in this work was first introduced in [28]. The advantage of such a cost function is that it eliminates the need for having any kind of additional control over circulating current reference in order to regulate the summation of capacitor voltages. The cost function is given as follows:

$$J_j = \lambda_1(i_{v,j,ref} - i_{v,j})^2 + \lambda_2(i_{cir,ref} - i_{cir,j})^2 + \lambda_3(2v_{dc,ref} - v^{\Sigma}_{u,j,avg} - v^{\Sigma}_{l,j,avg})(i_{cir,ref} - i_{cir,j}) + \lambda_4(v^{\Sigma}_{u,j,avg} - v^{\Sigma}_{l,j,avg})\Delta W \quad (20)$$

The λ's are the weighting factors for setting the relative importance between the control objectives. The first term is to regulate the ac-side current at its reference, the second term ensures that the ac-components in the circulating current are minimized, the third and fourth terms regulate the total leg voltage to $2V_{dc}$ and the arm voltage difference to zero respectively. ΔW is the instantaneous energy difference between the lower and upper arm. The interested readers are referred to [28] for a detailed explanation of how the cost function is working.

B. Reference Signals

In this work, the references for ac-side current are provided in the dq frame. Then the reference current in the abc frame is obtained by dq to abc transformation as follows:

$$i_{v,ref,a} = i_{d,ref}\sin(\omega t) + i_{q,ref}\cos(\omega t) \quad (21a)$$

$$i_{v,ref,b} = i_{d,ref}\sin\left(\omega t - \frac{2\pi}{3}\right) + i_{q,ref}\cos\left(\omega t - \frac{2\pi}{3}\right) \quad (21b)$$

$$i_{v,ref,c} = i_{d,ref}\sin\left(\omega t + \frac{2\pi}{3}\right) + i_{q,ref}\cos\left(\omega t + \frac{2\pi}{3}\right) \quad (21c)$$

where ωt is the phase angle provided by phase locked loop (PLL).

The circulating current reference is based on the assumption of equal input and output power and is given as:

$$I_{dc,ref} = \frac{P}{V_{dc,ref}}, i_{cir,ref} = \frac{I_{dc,ref}}{3} \quad (22)$$

It is noted here that due to the above assumption, the cost function (20) has been used as opposed to the conventional quadratic cost function [27]. This cost function compensates for the above assumption and forces a change in the circulating current. The reference for the average of the sum of the capacitor voltages per arm is equal to the applied dc voltage. The sorting algorithm as described in [5] is used to perform the SM capacitor voltage balancing task where the decision to insert or bypass SMs is based on the SM voltages and direction of arm current.

VI. Comparison with Other Strategies

The comparison of the proposed method with other strategies considering open circuit switch faults is shown in Table II. Only MPC-based strategies are considered to make a fair comparison. The proposed method has one or more advantages over all the existing MPC-based methods. Moreover, the existing MPC based methods do not consider redundant SMs and as a result, the SM capacitors need to be oversized as they have to handle more voltage in fault-tolerant operation. Furthermore, if this higher voltage in tolerant mode becomes more than the rated voltage then the SM capacitors would be damaged and may even explode.

VII. Simulation Results

The performance of the proposed strategy is validated by performing simulations on a three-phase MMC with 18 SMs per arm, as shown in Fig. 3. Among these 16 SMs are used in normal operation and the remaining two SMs serve the purpose of redundant SMs. A dq-frame phase locked loop (PLL) is used to achieve the synchronization of the system with the grid. All the references and measurements are sent to the proposed controller which outputs the optimal insertion index for each phase and generates fault signals if any. These insertion indices and fault signals are then sent to the voltage balancing module which determines the gating signals for the MMC.

The scenario used for simulation is that initially, the converter is operating in normal mode with an active current reference set to 40 A. The parameters used for simulation are summarized in Table III.

TABLE II: Comparison with other MPC based Strategies

Method	Features							
	FD	FL	FT	Overall Computational Burden	Speed	Additional Sensors/Components	Redundant SMs	Distinguish b/w S_1 and S_2 fault
Proposed	Y	Y	Y	Low	within fundamental period	N	Y	Y
[6],[22]	Y	Y	Y	Very High	within fundamental period	N	N	Y
[24]	Y	Y	Y	Low	at least 5 fundamental periods	Y	N	N
[25]	N	N	Y	Low	NA	N	N	N

* FD=Fault Detection, FL=Fault Localization, FT=Fault Tolerance, Y=Yes, N=No, NA=Not Applicable

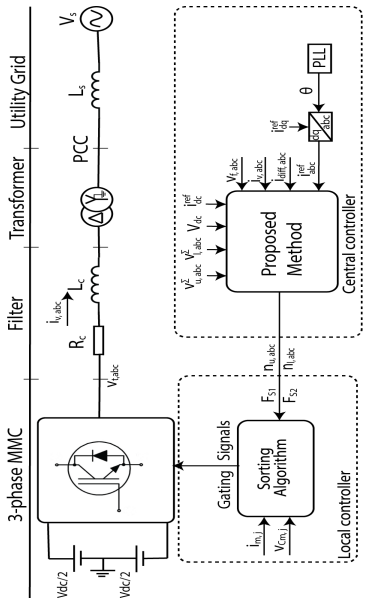

Fig. 3: Control Block Diagram

TABLE III: Simulation Parameters

Parameter	Value
MMC nominal power (base power)	50 kVA
AC system nominal voltage (base voltage)	150 V
Nominal frequency	50 Hz
Arm inductance (L)	1.55 mH
Arm resistance (R)	0.01Ω
Submodule capacitance (C)	20000μF
Transformer voltage rating (T)	400 V / 400 V
Transformer power rating	50 kVA
Transformer inductance	0.04 pu
Transformer resistance	0.006 pu
DC side reference voltage	400 V
Number of SMs per arm (N)	16
Number of redundant SMs per arm (M)	2
Sampling time (Ts)	70μs

In the following discussion, the open-circuit switch faults were generated by emulating the behavior of open-circuit faults as given in Table I. At t=0.23s the S_1 fault is applied to the first SM in the upper arm of phase a. Fig. 4 shows the overall response of all the state variables for both cases *i.e.*, if the fault is left uncleared and if the fault is cleared by the proposed method. The results show that none of the state variables is being tracked accurately if the fault is not cleared *i.e.*, the ac-current and circulating current have distortions, and the resulting summation voltages would create energy imbalance between the upper and lower arm.

Results for the scenario when S_2 fault is applied at t=0.23s, are shown in Fig. 5. In this case, the distortions in circulating current are more severe as the faulty SM capacitor would always be inserted when the arm current is positive. This results in voltage increase at a faster rate for S_2 fault as compared to S_1 fault because in S_1 fault the SM voltage is unchanged on faulty condition whereas under S_2 fault the SM capacitor gets charged and voltage increases (see Table I).

Figure 6 shows individual SM capacitor voltages in the upper arm of phase *a* under both types of faults with and without the proposed method. The faulty SM voltage keeps on increasing for both faults if the faults are not cleared as already discussed in section III. Therefore, if faults are left uncleared then the faulty SM voltage would eventually become higher than the rated voltage of the capacitor and damage the capacitor or might even explode the capacitor if the voltage becomes too large. With the proposed method, as soon as the fault is localized to the faulty SM then it is bypassed using the bypass switch *B* as shown in Fig. 1 and a redundant SM takes its place.

In Fig. 7 the fault detection (denoted by FD) and localization (denoted by FL) signals for both faults are shown for the positive direction of power flow. It can be observed that fault detection and localization for S_2 fault is quicker than S_1 fault. This is due to the direction of power flow which was positive for this simulation scenario. As a consequence, the arm current is more positive during one fundamental period. Therefore, under this scenario, S_2 fault occurs more often as its impact occurs when the arm current is positive (see Table I). So, the count associated with S_2 fault reaches the threshold faster and gets cleared early as compared to S_1 fault. In the case of negative power flow, the arm current would be more negative in one fundamental period. As the S_1 fault impact occurs when the arm current is negative (see Table I), it would occur more often as compared to S_2 fault in this scenario. Therefore, S_1 fault would be detected and cleared early as compared to S_2 fault for this power direction.

It can also be observed that fault detection is very fast *i.e.*, the fault is detected in less than 5ms even for S_1 and is localized to the faulty SM in around 5ms. As soon as the fault is localized, the faulty SM is removed by the bypass switch and is replaced by a redundant SM. Therefore, the fault has been cleared and no fault is detected afterward. It is noted here that the fault detection signal switches between 0 and 1 because the faulty SM is not always inserted/bypassed by the sorting algorithm.

The fault detection and localization signals in the reverse power direction are shown in Fig. 8 under both types of faults. As explained earlier, in this power direction S_1 fault is detected and cleared earlier as compared to S_2 fault.

VIII. Conclusion

In this work, a method for fault detection, localization, and clearance based on indirect finite control set model predictive control is presented for MMCs. It is shown that the proposed method detects, localizes, and clears the fault within just around 5ms i.e., 1/4th of the fundamental period. The proposed method also provides information regarding the fault type i.e., due to S_1 or S_2. Moreover, no additional sensors are required to execute the developed method.

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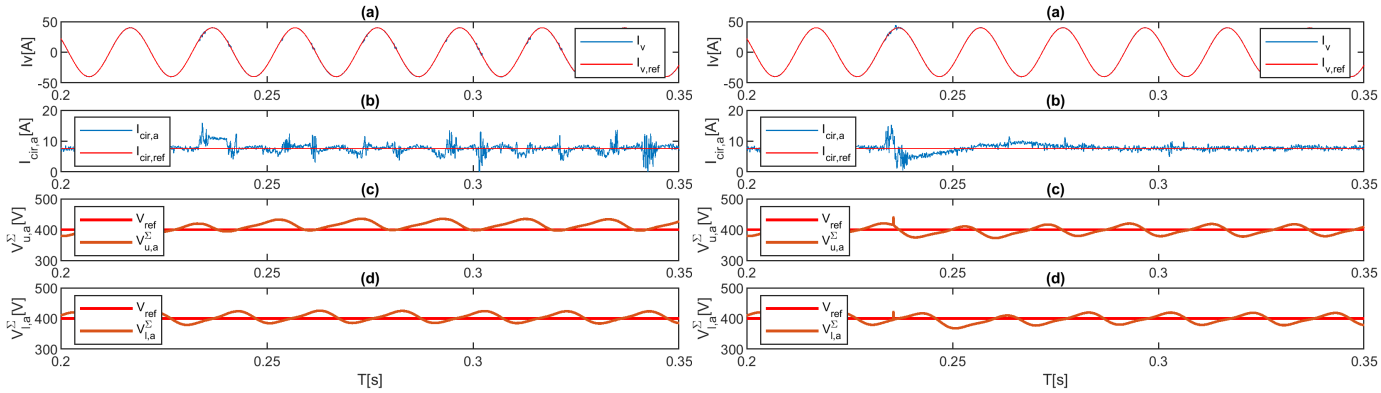
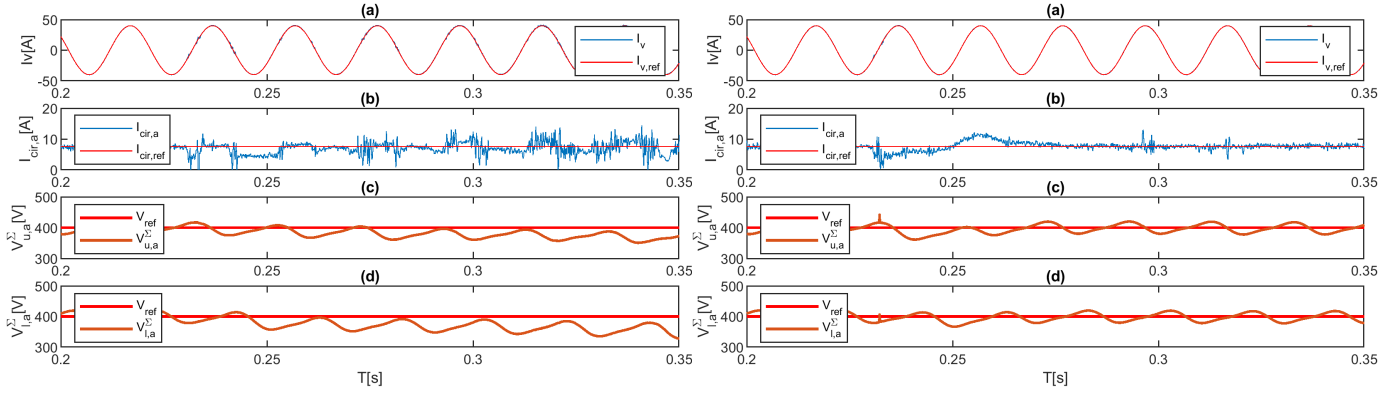


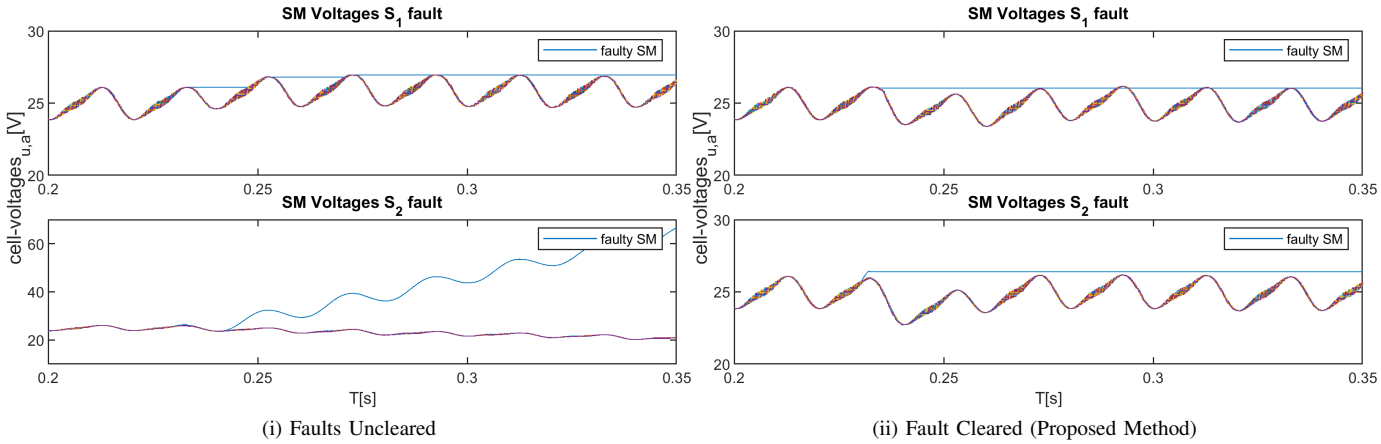
(i) S_1 Fault Uncleared (ii) S_1 Fault Cleared (Proposed Method)

Fig. 4: (a) phase-a current, (b) phase-a circulating current, (c) summation of the capacitor voltages in the upper arm of phase a (d) summation of the capacitor voltages in the lower arm of phase a



(i) S_2 Fault Uncleared (ii) S_2 Fault Cleared (Proposed Method)

Fig. 5: (a) phase-a current, (b) phase-a circulating current, (c) summation of the capacitor voltages in the upper arm of phase a (d) summation of the capacitor voltages in the lower arm of phase a



(i) Faults Uncleared (ii) Fault Cleared (Proposed Method)

Fig. 6: Individual SM Capacitor Voltages under both types of faults with and without proposed method

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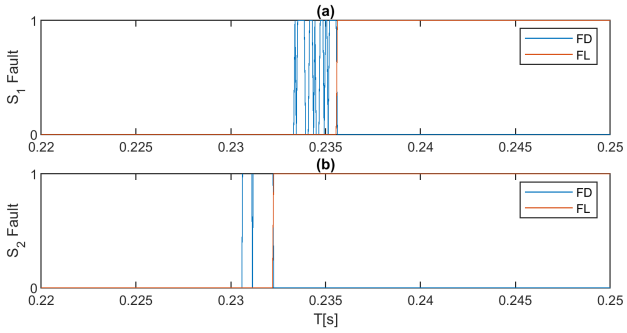

Fig. 7: Fault Detection and Localization Signals (positive power flow) (a) S_1 fault (b) S_2 fault

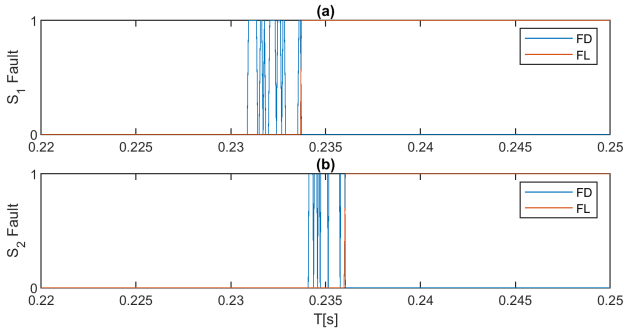

Fig. 8: Fault Detection and Localization Signals (negative power flow) (a) S_1 fault (b) S_2 fault

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