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A Hybrid Current- and Voltage-Source Driver for Active Driving of Series-Connected SiC MOSFETs

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***Abstract*—The series-connection of Silicon Carbide (SiC) Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFETs) is an attractive way of increasing the blocking voltage capability of a switch. However, due to inherent transient and steady-state voltage imbalance issues, such a design imposes challenges, especially at elevated switching frequencies, where increased dv/dt is required. This paper proposes a hybrid gate driver for series-connected SiC MOSFETs, which consists of a turn-on stage with a traditional Voltage Source Gate Driver (VSGD), and a turn-off sequence combining a Current Source Gate Driver (CSGD) and a VSGD. The proposed hybrid gate driver can actively control the turn-off dv/dt and di/dt of the switch by adjusting the amplitude of the gate current in the CSGD stage, as well as balance the voltages of the serialized switches by adjusting the timing delays in the driver. This adaptability enables switching loss control of the devices. The proposed driver has been experimentally validated for two series-connected SiC MOSFETs. From experiments, it is shown that a voltage imbalance below $2\,\%$ can be achieved at direct current (DC)-voltage of $1.5\,\mathrm{kV}$ and that switching speeds can be adjusted between $20\,\mathrm{kV/\mu s}$ to $70\,\mathrm{kV/\mu s}$, while the turn-off switching energy can be reduced by up to $41\,\%$.**

***Index Terms*—Gate drivers, SiC MOSFETs, adaptive driving, series-connection.**

I. Introduction

Silicon Carbide (SiC) Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFETs) exhibit faster switching transitions, lower power losses and higher operating temperatures over their Silicon counterparts in high-voltage and high-power applications [1], [2]. Applications such as medium-voltage (MV) direct current (DC) grids [3], [4] and MV drives [5] will feature improved performance by employing SiC MOSFETs. SiC MOSFETs dies can be designed with higher breakdown voltages for the same conducting performance than Silicon devices. However, fabrication challenges and immature material properties at elevated breakdown voltages currently limit the rated blocking voltage of commercially available SiC MOSFETs to 1.7 kV. SiC MOSFETs rated at $3.3\,\mathrm{kV}$ have started to appear as engineering samples just recently [5]–[7].

The way to reach higher blocking voltages is to series-connect SiC MOSFETs for designing a single switch which can be suitable for MVDC applications. It has been demonstrated that series-connection of two or more SiC MOSFETs exhibit a lower on-state resistance and higher current density compared to a single device with the same voltage blocking capability [8]. However, a major challenge of operating series-connected SiC MOSFETs is to ensure equal transient and steady-state voltage sharing among the devices. Voltage differences among the devices can lead to device failure if they are not controlled [9], [10]. In addition, exploiting the fast switching capabilities of SiC MOSFETs in series connection necessitates the design of poweful gate drivers. However, achieving very short rise and fall switching times is usually hindered by the anticipated transient voltage mismatches.

Transient voltage imbalances might be due to unequal propagation delays in gate signals that are caused by fabrication tolerances in the drive circuit components or circuit layout mismatches [11]. Another reason leading to uneven voltage distribution is MOSFETs' devices parameters spread, such as the threshold voltages and intrinsic device capacitances [12]. Variations in the circuit layout parasitic capacitances from each gate to ground will cause common-mode currents of different amplitudes to flow through each gate to ground since every parasitic capacitance will see a different dv/dt. This will also prohibit synchronous switching of the MOSFETs [13]–[15].

The most straightforward way to ensure voltage balance is to use passive snubber and clamping circuits, which can be designed with varying levels of complexity, such as a standard resistor-capacitor (RC) snubber [16], [17]. In [18] a design of a RC snubber with a coupled inductor that can sense voltage imbalance and add a compensated signal to the gate driving voltage is proposed, and it was shown that the size of the snubber capacitance can be significantly reduced compared to simple RC snubber solutions. Voltage clamping methods limits the overvoltages across the serialized devices by clamping them to a pre-determined level. In [19] the clamping voltage was set using a string of Zener diodes, but the RC snubber was still required for dynamic balancing. Active clamping methods with dv/dt control capabilities are also proposed in literature. These methods exhibit lower losses and control complexity, but have an increased cost due the added components in the clamping circuit [20], [21]. Although passive methods are typically cost-effective and easy to implement, they may result in higher circuit losses [11]. Single gate driver solutions are also investigated in literature. These methods are generally realized with coupling capacitors and require only one external driving circuit to drive all the switches in the series-connection [22]–[25]. They provide the possibility of designing a very compact MV switch. However, their drawback is limited switching speed and that they still rely on passive RC snubbers to achieve balanced voltages.

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On the other hand, active gate control methods are attractive due to their flexibility and accurate voltage balancing control. In [14] voltage balancing is achieved by the means of a small Miller capacitor placed between the drain and gate of the device. This capacitor will provide additional current to the gate of the MOSFET at turn-off and control the switching speed of the top MOSFET to compensate for common mode currents flowing through the parasitic gate-ground capacitors. However, this concept has not been verified for series-connected devices used as an upper switch in a bridge leg and will only control the dv/dt of a single switch. There are several other methods that modify the gate charge profile to control the turn-off transient [26]–[29]. The common characteristic for all of them is that they are often quite complex.

Active gate delay compensation techniques tune the gate delay between the serialized devices to achieve voltage balance [30]–[35], which is achieved at a lower complexity compared to active gate control methods, as only the gate delays are adjusted. However, methods implementing active gate delay compensation still require high-bandwidth measurements that are realized with analog-to-digital converters (ADCs) and processed in a digital signal processor (DSP) to calculate the delay time [30]–[34]. A block diagram of a complete closed-loop active gate driving system is shown in Fig. 1. Such a system consists of the gate-drive circuit which is the actuator, sensors and a DSP that processes measurements and controls the gate-drive circuit. The scope of this paper is on the gate-drive circuit, which remains one of the most important components in the system illustrated in Fig. 1.

Current Source Gate Drivers (CSGDs) can also be used to achieve active voltage balancing due to their ability to control both the amplitude and the time delays of the gate current by means of active switches, and thus adjust the rise and fall rates of voltage and current (i.e. the dv/dt and di/dt) of the entire stack of series-connected SiC MOSFETs [36]. Besides, the possibility to control the switching losses, i.e. by for instance increasing the dv/dt and di/dt of the stack and reducing the switching loss, is enabled [37].

The contribution of this paper is a novel hybrid CSGD and Voltage Source Gate Driver (VSGD) for active driving of series-connected SiC MOSFETs as highlighted in Fig. 1. The proposed driver aims to control the transient voltage balancing at turn-off by the use of a CSGD stage for each individual series-connected SiC MOSFET, while the turn-on stage is realized with a VSGD to reduce the design and operating complexity of the driver. The proposed driver is able to achieve voltage balancing by introducing time shifts between the devices without increasing switching losses, while it can also manipulate dv/dt, di/dt and switching losses under variable loading conditions. The proposed hybrid driver can be classified as an active gate delay compensation scheme, with adaptive driving to optimize the transient performance. Moreover, the proposed hybrid GD, features an inherent voltage isolation. The scope and limitation of this work is shown in Fig. 1. The focus of this paper is on the design, operating methodology and experimental validation of the hybrid active gate driver under various operating conditions, to demonstrate its feasibility in controlling the transient voltage balancing, as well as key electrical parameters such as voltage overshoot, dv/dt etc. Thus, closed-loop control operation is not investigated in this paper. However, the proposed hybrid gate driver can be integrated in any closed-loop driving scheme in switch-mode power converters.

This article is organized as follows. Section II presents the design and operating principles of the proposed hybrid gate driver concept. Section III presents experimental validation of the proposed driver and its various operation modes. The benefits of using the proposed driver are discussed in Section IV. The article is concluded in Section V.

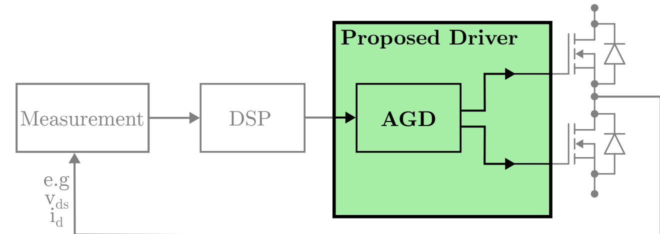

Fig. 1: Diagram illustrating where the proposed driver would be in a complete system.

II. Proposed Adaptive Hybrid Driver

The aim of the proposed hybrid gate driver is to ensure a high degree of voltage balancing in fast-switching series-connected SiC MOSFETs, without adding significant losses to the system. Furthermore, it has the possibility to adjust the dv/dt and di/dt of the switch, so that it can reduce switching losses and be applied in high-frequency MVDC applications. Fig. 2 shows the schematic diagram of the proposed driver, which here is applied to two series-connected SiC MOSFETs. The coupled inductor is indicated by L_{p} on the primary side and with its two secondaries L_{s1} and L_{s2}, while R_{d} is the discharge resistor for the coupled inductor. The CSGD stage consists of the small-signal MOSFET switches Q_{aux} and Q_{p} together with the diodes D_1 and D_2. The turn-on is realized with a VSGD between the small-signal switches Q_+ and Q_- that are connected to their respective positive and negative voltage sources V_+ and V_-. $R_{\mathrm{g(CS)}}$ and $R_{\mathrm{g(VS)}}$ are the gate resistances in the corresponding CSGD and VSGD paths. M_1 and M_2 are the top and bottom side SiC MOSFETs in the series stack.

During the on-state of the power MOSFETs, Q_{1+} and Q_{2+} are turned on, holding V_{gs} at V_+. In the steady-state of the off-state, Q_{1-} and Q_{2-} are on, holding V_{gs} at V_-. At the turn-on transient of the power MOSFETs, Q_{1-}/Q_{2-} are switched off and Q_{1+} and Q_{2+} are switched on, similar to a conventional two-level VSGD. However, during the turn-off switching transient, the power MOSFET gate charge is extracted by means of the built-up magnetic flux in the coupled inductors. The magnetic flux has been built up by turning on the switch Q_{p} on the primary side of the coupled inductors for a specified time interval to charge the inductor to the required current by the voltage source V_{p}. Q_{aux1} and Q_{aux2} open the turn-off path through the coupled inductors L_{s1} and L_{s2} on

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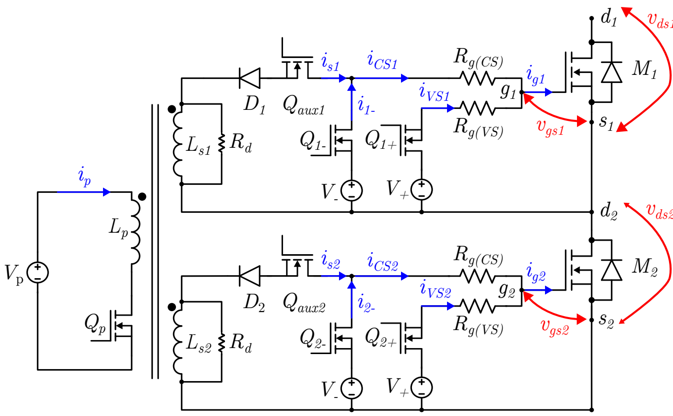

Fig. 2: Schematic of the proposed driver.

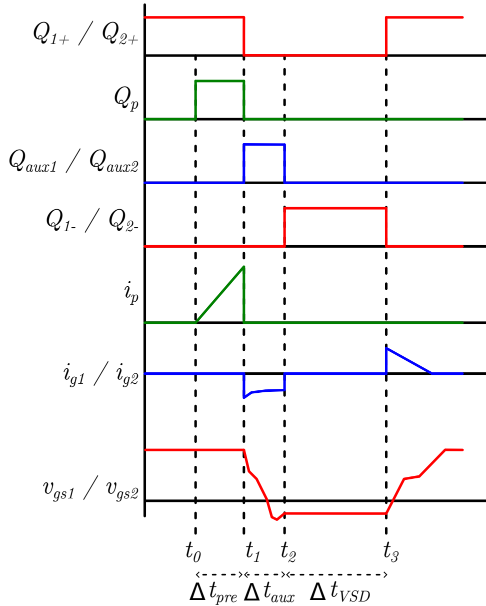

Fig. 3: Timing diagram of the proposed driver.

the secondary sides so that the diodes D_1 and D_2 can conduct during the turn-off transient.

A. Basic Operating Principle of the Gate Driver

The operating principle of the proposed hybrid gate driver will be analyzed by considering the timing diagram in Fig. 3 and the equivalent circuits of the driver for the different time intervals that are depicted in Fig. 4. The operating principle is identical for each secondary side of the gate driver of the serialized stack. Thus, the driver signals, which are programmed in a DSP, and the response of the switches in the gate driver are identical for both of the devices in the stack.

The SiC power MOSFETs are both conducting before t_0. At t_0, the turn-off process is initiated by starting the pre-charging of L_p at the primary side of the coupled inductors as shown in Fig. 4a. The inductor is pre-charged for a time Δt_pre, which depends on the magnetizing inductance of the inductor, leakage inductance, source voltage and amount of charge in the inductor required to discharge the gate capacitance of the SiC MOSFETs [37]. The required energy to discharge the input capacitance of the SiC MOSFET, C_iss, is given by:

$$E_\mathrm{C} = \frac{1}{2} \cdot Q_\mathrm{g} \cdot \Delta V \tag{1}$$

where Q_g is the stored gate charge and ΔV is the difference in driving voltages. The energy stored in the primary side of the coupled inductor is given by:

$$E_\mathrm{L} = \frac{1}{2} \cdot L_\mathrm{p} \cdot I_\mathrm{p} \tag{2}$$

The energy stored in L_p must be at least equal to twice the energy stored in the input capacitances of the SiC MOSFETs (since there are two SiC MOSFETs in series). The amplitude of the primary side current can be derived from the inductor equation:

$$I_\mathrm{p} = \frac{1}{L_\mathrm{p}} \cdot V_\mathrm{p} \cdot \Delta t_\mathrm{pre} \tag{3}$$

A simplified schematic of the coupled inductor is shown in Fig. 5, where n_p, n_s1 and n_s1 are the primary side and top and bottom secondary side turns of the coupled inductor, and φ is the magnetic flux in the inductor core and links all the windings.

The turns-ratio $n_\mathrm{s1} : n_\mathrm{s2}$ must be unity to achieve secondary side currents i_s1 and i_s2 of equal amplitudes. For simplicity, $n_\mathrm{p} : n_\mathrm{s1} : n_\mathrm{s2}$ is also set to be unity. The flux in the core must be continuous and the relationship between the windings is given by Eq. (4).

$$n_\mathrm{p} \cdot I_\mathrm{p} = n_\mathrm{s1} \cdot i_\mathrm{s1} + n_\mathrm{s2} \cdot i_\mathrm{s2} \tag{4}$$

Since $n_\mathrm{p} = n_\mathrm{s1} = n_\mathrm{s2}$, it can be assumed that $i_\mathrm{s1} = i_\mathrm{s2}$ under ideal conditions. Thus, the following relationship between the primary and secondary side current can be derived:

$$i_\mathrm{s} = i_\mathrm{s1} = i_\mathrm{s2} = \frac{I_\mathrm{p}}{2} = I_\mathrm{CS} \tag{5}$$

This is the current that will flow through D_1 and D_2 when, at t_1, the auxiliary switches Q_aux1 and Q_aux2 are turned on for a time period Δt_aux. At the same time, the switches Q_{1+} and Q_{2+} are turned off to disconnect the positive gate voltage source. The gate current is constant during this time interval and is denoted as I_CS. The length of Δt_aux can be calculated by Eq. (6):

$$\Delta t_\mathrm{aux} = \frac{Q_\mathrm{g}}{I_\mathrm{CS}} \tag{6}$$

Not drawn in the timing diagram is a required overlap between $Q_\mathrm{aux1}/Q_\mathrm{aux2}$ and Q_p for safety reasons, as excessive overvoltages may appear across the primary side terminals of the inductor if there is no freewheeling path for the current to flow when Q_p is turned off. This overlap is limited to one DSP clock cycle.

Fig. 4b shows the equivalent circuit during the time interval t_1-t_2. The primary side switch Q_p is turned off. The built-up magnetic flux in the coupled inductor core leads to a current in the secondary windings (L_s1 and L_s2). This current discharges the input capacitance C_iss of each of the power MOSFETs,

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(a) t_0 - t_1 (b) t_1 - t_2

(c) t_2 - t_3 (d) t_3 -

Fig. 4: Equivalent circuits of the proposed driver at different time intervals.

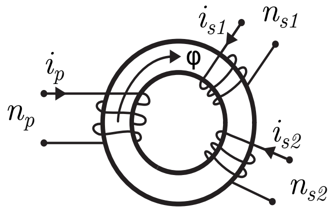

Fig. 5: Illustration of the coupled inductor.

which is the sum of the Miller and gate-source capacitances, and thereby turns the MOSFETs off.

At t_2 (Fig. 4c), Q_{1-} and Q_{2-} are switched on to stabilize the power MOSFET gate source voltage during the off-state period. These switches conduct for a time interval Δt_{VSD} until t_3, when the series-connected SiC MOSFETs are turned on, by turning on the switches Q_{1+} and Q_{2+}, as shown in Fig. 4d. The sum of Δt_{aux} and Δt_{VSD} is the off-time period of the SiC MOSFET and will depend on the duty cycle and switching frequency of the power converter. The turn-on process is carried out with a simple voltage source drive. Dead-times are implemented at t_1 and t_3 between the switch pairs Q_{1+}/Q_{1-} and Q_{2+}/Q_{2-} in order to avoid low resistance paths between the power supplies.

It is important to address how the core is demagnetized during each switching period to avoid saturation. One way to do that is by placing a discharging resistor, R_{d}, across each secondary winding of the inductor as shown in Fig. 2. For simplicity, this resistor has been omitted in Fig. 4.
When Q_{p} and $Q_{\text{aux1}}/Q_{\text{aux2}}$ are off, the remaining energy in the inductor will be dissipated through this resistor, ensuring that the inductor core is fully demagnetized and ready for the next switching period. It is assumed that the discharging resistor has a sufficiently high value and there is not much current flowing through it when $Q_{\text{aux1}}/Q_{\text{aux2}}$ are on. Therefore, its impact on $i_{\text{s1}}/i_{\text{s2}}$ is negligible and it does not interfere with the performance of the driver.

B. Principle of Voltage Balance Control at Turn-Off

The proposed driver has the possibility to control the anticipated transient voltage imbalances at turn-off process. In a complete system, the driver would be equipped with a sensing circuit based on ADCs for measurement of the voltages. The sensing circuit in a switch-mode converter would then detect a drain-source voltage imbalance between the devices in the stack and a DSP takes action to adjust the delays between the gate driver signals to improve voltage balance. This is achieved by introducing a delay between the signals to the Q_{aux} switches. However, the focus of this paper is on the development and experimental evaluation of an

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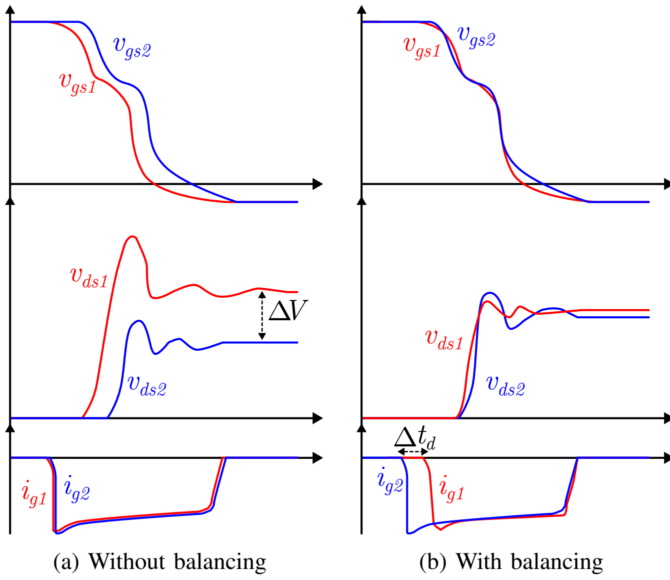

Fig. 6: Waveforms without balancing enabled in (a) and with balancing enabled in (b).

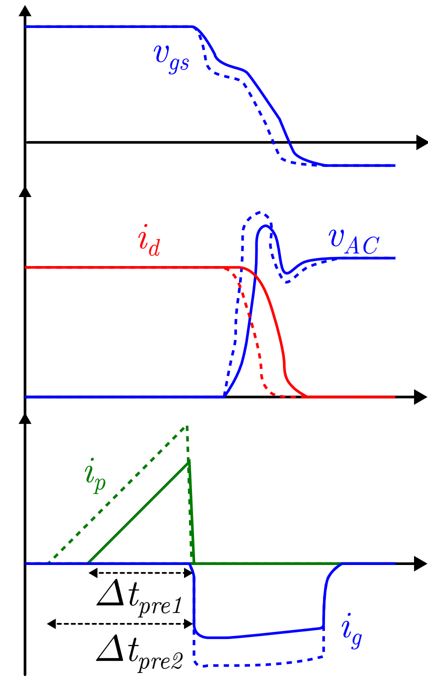

Fig. 7: Theoretical waveforms showing principle of controlling turn-off transient di/dt and dv/dt.

active gate driver that is able to balance the transient voltage distributions in series-connected SiC MOSFETs and adjust switching parameters such as dv/dt and switching losses.

A situation without voltage balancing enabled in illustrated in Fig. 6a. Here, the top SiC MOSFET switches slightly faster than the bottom device in the series-connected stack. This might be due to several reasons. The intrinsic non-linear capacitances of the devices might differ, meaning that the top device will discharge its input capacitance, C_{iss}, quicker than the bottom device. Other parameters of the devices, such as the transfer characteristics and threshold voltage might also differ among the MOSFETs. Another reason might be propagation delay mismatches in the gate driver signals, or common mode current through parasitic capacitances to ground from each gate. Small mismatches in the inductances of the coupled inductor secondaries will also influence which device will switch slightly faster or slower. Ideally, the drain-source voltages of the series-connected SiC MOSFETs, v_{ds1} and v_{ds2}, should be measured during the turn-off transient to take corrective action in the controller. This is in practice difficult to achieve due to the switching speeds involved. However, there is a correlation between the measured imbalance after turn-off is completed and the imbalance during the turn-off transient. This means that if there is an imbalance in the transient voltages, this imbalance will also be visible after the turn-off transient is completed. Thus, it is sufficient to measure the voltage imbalance after the turn-off voltage transients are completed and any oscillations have been damped. These two measured values are then compared to the ideal voltage distribution, i.e. half of the DC bus voltage, and corrective action is taken in the next switching cycle. This is shown in Fig. 6b. Assuming that M_1 switches faster than M_2, instead of turning the switches Q_{aux1} and Q_{aux2} on synchronously, as shown in Fig. 6a, a delay Δt_{d} is introduced to the Q_{aux} switch of M_1 in this case. This means that the CSGD-pulse will be applied to M_1 slightly later than to M_2. The turn-off transient of M_1 is only moved slightly forward in time and it is not slowed down, meaning that the switching losses do not increase. M_2 is synchronized with M_1, and the resulting voltage imbalance is minimized to a desired value, which might be in the range of 2-10 % of the total DC bus voltage.

C. Principle of di/dt and dv/dt Control

The proposed driver can control the di/dt and dv/dt of the AC node (i.e. the sum of v_{ds1} and v_{ds2}) by adjusting Δt_{pre}. This is illustrated in Fig. 7, where i_{d} is the drain current and $v_{\text{AC}} = v_{\text{ds1}} + v_{\text{ds2}}$. Basically, the pre-charge time, Δt_{pre}, of the primary side of the coupled inductors is adjusted to achieve the desired switching speed. Two cases are shown in this figure. The first case for a Δt_{pre1} is shown with solid lines, while the waveforms for Δt_{pre2} are shown with dashed lines, and $\Delta t_{\text{pre2}} > \Delta t_{\text{pre1}}$. A larger Δt_{pre} corresponds to larger built-up magnetic flux in the coupled inductor, which in turn corresponds to more stored energy. This means that when the energy is released on the two secondaries of the coupled inductors as currents i_{s1} and i_{s2} (Fig. 4b), their amplitudes will vary with Δt_{pre} as given by Eq. (3) and (5). A larger Δt_{pre} will cause a larger amplitude of the turn-off gate current and discharge C_{iss} faster, leading to a shorter switching transient with higher di/dt and dv/dt and lower switching losses. This can be explained by the circuit in Fig. 8. The amplitude of i_{s} (which is the same as i_{g} in this interval) can be assumed to be a constant current source with amplitude I_{CS} (Eq. (5)). $R_{\text{g(int)}}$ is the internal gate resistance of the SiC MOSFET, and $C_{\text{gs}}, C_{\text{gd}}$ and C_{ds} are its non-linear intrinsic gate-source, Miller and drain-source capacitances. The gate-source voltage

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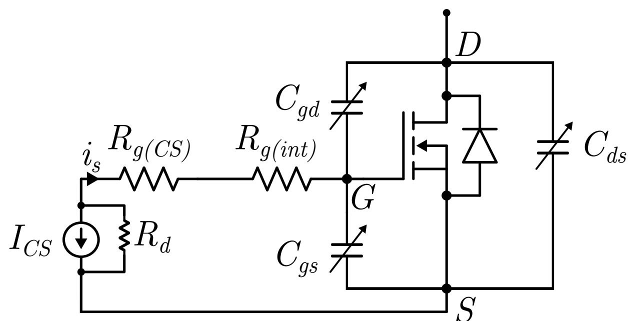


Fig. 8: Simplified circuit of the driver in time interval t_1-t_2 for one of the SiC MOSFETs in the series-connection.

is constant during the Miller plateau, and the switching speed can then be given by:

$$\frac{dv_{\mathrm{ds}}}{dt} = \frac{I_{\mathrm{CS}}}{C_{\mathrm{gd}}} \tag{7}$$

Increasing I_{CS} will increase the switching speed of the SiC MOSFET. The Miller capacitance has a very non-linear value that can vary from several nF at low drain-source voltages to tens of pF at higher drain-source voltages, depending on the device design parameters.

Fig. 7 shows only the theoretical waveforms for one of the SiC MOSFETs in the series-connection, as it is assumed that the waveforms are identical for the other device.

III. Experimental Results

A. Experimental Setup

The performance of the proposed gate driver was experimentally validated in a double-pulse test (DPT) circuit, as illustrated in Fig. 9. The setup consists of a $1.2\,\mathrm{kV}$ SiC MOSFET half-bridge module (device under test (DUT)) and an inductive load. The two internal switches of the half-bridge module are series-connected to form a $2.4\,\mathrm{kV}$-rated switch, and an external diode is used to freewheel the inductor current during the DPT. A photo of the top-side of the printed circuit board (PCB) with the power module is shown in Fig. 10a and with a side-view in Fig. 10b. Photos of the top and bottom side of the proposed hybrid CSGD-VSGD PCB are shown in Fig. 11 and the key components are marked.

The circuit parameters and devices used in the DPT are given in Table I, while Table II summarizes the measurement equipment used during the DPTs experiments.

As shown in Fig. 9 and given in Table I, static balancing resistors, R_{b}, are placed in parallel with each SiC MOSFET. These are used to ensure steady-state voltage balance across the serialized devices, which is caused by uneven drain-source leakage currents among the devices. The size of this resistor can be calculated analytically and will be a trade-off between power dissipation and off-state voltage imbalance. The equation for calculation of R_{b} is given by (8) [23]:

$$R_{\mathrm{b}} < \frac{V_{\mathrm{ds}}}{10 \cdot I_{\mathrm{dss(max)}}} \tag{8}$$

This equation accepts a $10\,\%$ voltage imbalance and $I_{\mathrm{dss(max)}}$ is the maximum drain-source leakage current. The datasheet of the CAB450M12XM3 SiC MOSFET power module gives a maximum leakage current of $200\,\mu\mathrm{A}$ [38]. Thus, Eq. (8) results in a maximum R_{b} of $375\,\mathrm{k\Omega}$, but a balancing resistor of $270\,\mathrm{k\Omega}$ is selected in the experimental setup to keep a safety margin.

The coupled inductor employed on the hybrid gate driver has been designed considering that the magnetization time must be short compared to one switching time period which requires a small primary side magnetizing inductance, i.e., in the range of few hundred nanohenries. This will result

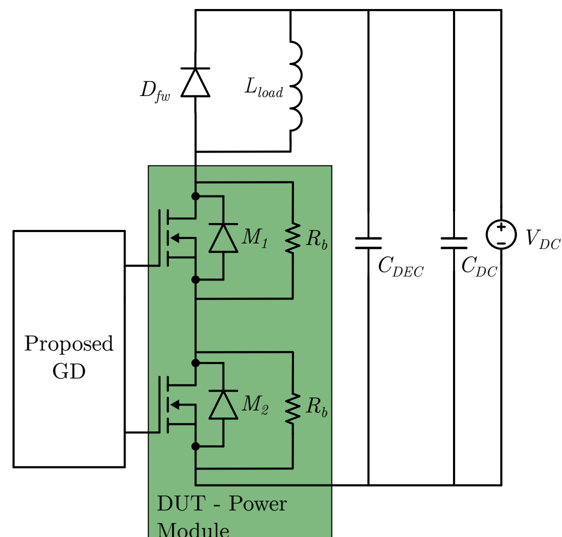
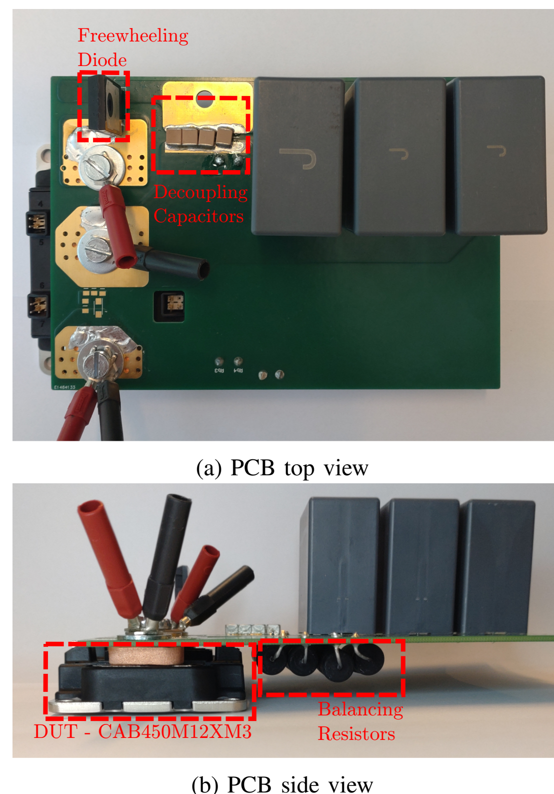


Fig. 9: Schematic diagram of the DPT setup.



(a) PCB top view

(b) PCB side view

Fig. 10: Photos of the DUT PCB.

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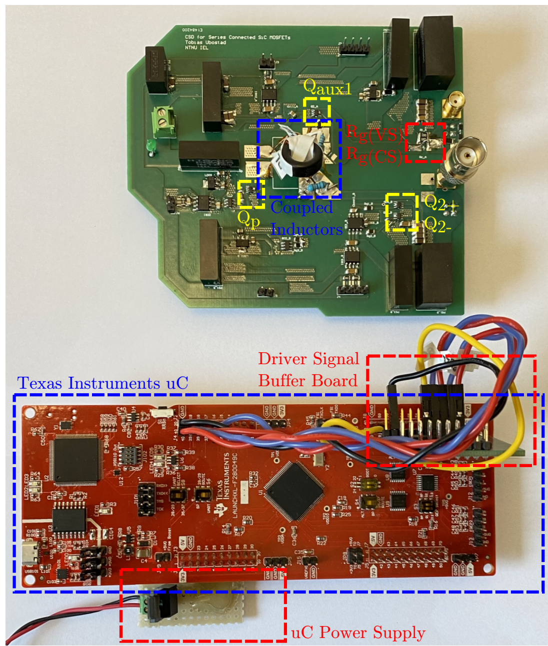
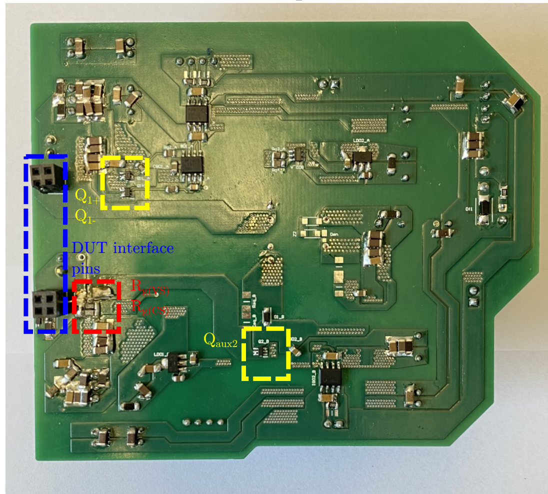


(a) PCB top view



(b) PCB bottom view

Fig. 11: Photo of gate driver PCB and DSP.

in a relatively high current and allow a fast transfer for the required energy into the magnetizing inductor. A Kool Mμ core for high-frequency applications has been chosen, with a low permeability. This means that a low number of turns is required to reach low inductance values. The turns-ratios between the primary winding and the secondary windings have been chosen to be 1:1, with 3 turns on each winding. The designed coupled inductors have been characterized using a Keysight E4990A impedance analyzer and the measured parameters are summarized in Table III. Furthermore, the toroid core has an insulation coating rated for $1250\,\mathrm{V}$, which has been in this case increased by insulating the wire used in the windings with Kapton tape, as the experimental tests are performed for voltages up to $1.5\,\mathrm{kV}$.

The control signals for the small-signal discrete switches in the driver (Q_{aux}, Q_{p}, Q_{+} and Q_{-}) as shown in Fig. 3,

TABLE I: Components in the experimental setup.

Component	Values
SiC MOSFET Module (M_1&M_2)	CAB450M12XM3 (1.2 kV/ 450 A)
SiC Freewheeling Diode (D_{fw})	GC50MPS33H (3.3 kV/ 40 A)
Si MOSFETs ($Q_{\mathrm{aux}}/Q_{\mathrm{p}}/Q_{-}/Q_{+}$)	SI1480DH (100 V/ 2.6 A)
Test Inductor (L_{load})	127 μH
Bus Capacitor (C_{DC})	150 μF
Decoupling Capacitor (C_{DEC})	0.4 μF
VSGD Gate Resistor ($R_{\mathrm{g(VS)}}$)	5 Ω
CSGD Gate Resistor ($R_{\mathrm{g(CS)}}$)	0 Ω shunt
Driving voltages (V_{+}&V_{-})	+15 V/ -5 V
Balancing Resistor (R_{b})	270 kΩ

TABLE II: Measurement equipment

Instrument Type	Model
Oscilloscope	Tektronix MSO56B (500 MHz)
Differential Probe (v_{ds1} & v_{ds2})	THDP0200 (1.5 kV/ 200 MHz)
Differential Probe (v_{gs2})	TIVP05 (50 V/ 500 MHz)
Rogowski Coil (i_{CS1} & i_{CS2})	CWT Ultra Mini 06 (120 A/ 30 MHz)
Rogowski Coil (i_{d})	CWT Mini50HF 1 (300 A/ 50 MHz)

are programmed and implemented in the Texas Instruments TMS320F280049C microcontroller.

The main considerations when selecting the Q_{aux}, Q_{p}, Q_{+} and Q_{-} switches are their voltage and current ratings. Switches rated for at least $50\,\mathrm{V}$ should be sufficient to withstand the low voltages of the gate side circuitry.
Moreover, these switches should be able to handle the RMS currents of the driver. Q_{p} experiences the largest RMS current in the gate driver, since it must charge up i_{p}. Assuming a $\Delta t_{\mathrm{pre}} = 1000\,\mathrm{ns}$ and switching frequency of $10\,\mathrm{kHz}$, the RMS current through the switch can be at worst $1.5\,\mathrm{A}$. In reality, this current will be slightly lower due to the on-state resistance of the switch. As the current i_{p} increases, the voltage across L_{p} will decrease, as the voltage across Q_{p} increases due to its resistance. Thus, the current through L_{p} will not increase linearly with increasing Δt_{pre} and will reach a ceiling. For that reason, a switch with low on-state resistance is preferable, for more controllability of i_{p}.
However, switches with a low on-state resistance are usually rated for higher currents and the drawback of this is that such a switch usually has a quite large footprint, making it increasingly difficult to integrate on an already compact PCB. Such a switch also has a larger device capacitance that slows down its switching speed.
Furthermore, the small-signal switches should have low turn-on delay times, as well as low parameter spread among them to ensure synchronized turn-on. This is especially important for $Q_{\mathrm{aux1}}/Q_{\mathrm{aux2}}$. The selected switch given in Table I satisfies

TABLE III: Measured electrical parameters of the coupled inductors using the Keysight E4990A impedance analyzer.

Parameter	Value
Primary Magnetizing Inductance (L_{p})	456 nH
Top Secondary Magnetizing Inductance (L_{s1})	467 nH
Bottom Secondary Magnetizing Inductance (L_{s2})	448 nH
Coupling Capacitance (C_{iso})	3.9 pF

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all these conditions to a good degree, and has a relatively small footprint for its current carrying capability.

The next section will present some initial calculations needed to set Δt_{pre} and Δt_{aux} and the following sections will show experimental results verifying the working principle of the hybrid active CSGD for series-connected SiC MOSFETs in two different operational modes. These operational modes are:

1) Voltage balance control by adjusting the timing delays between the gate driver signals.
2) Variable di/dt and dv/dt control at turn-off by adjusting the pre-charge time of the primary side of the coupled inductors.

B. Initial Calculation of Gate Driver Timings

The time intervals Δt_{pre} and Δt_{aux} in Fig. 3 will be first calculated to estimate what initial timings are required for the SiC MOSFET module used in the experiments.

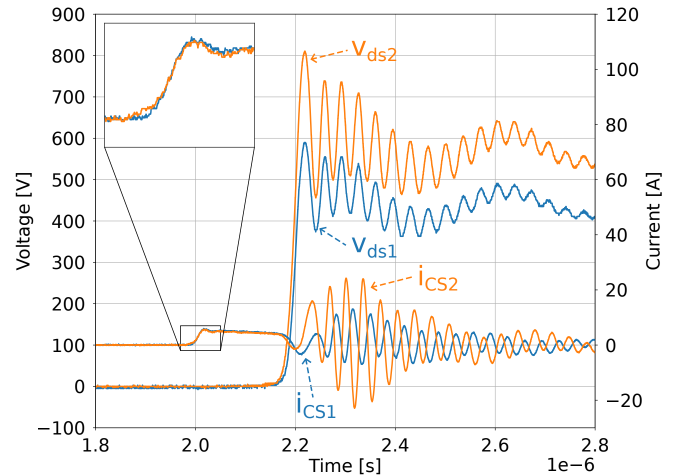
The CAB450M12XM3 module has a total gate charge of $1330\,\mathrm{nC}$ according to its datasheet, measured at a drain-source voltage of $800\,\mathrm{V}$ and driving voltage of +15 V/-4 V. The stored energy in the input MOSFET's capacitance is then $13.3\,\mu\mathrm{J}$ according to Eq. (1). The required energy to be stored in L_{p} must then be twice this energy since there are two SiC MOSFETs in series. Using this together with $V_{\mathrm{p}} = 12\,\mathrm{V}$ and the measured L_{p} value from Table III in Equations (2) and (3), it is found that a Δt_{pre} of at least $410\,\mathrm{ns}$ is needed to turn off the devices.

This Δt_{pre} will theoretically give an I_{p} of $10.8\,\mathrm{A}$ according to Eq. (3). This current will ideally be shared evenly between the two secondary windings (Eq. (5)). From Eq. (6) it is then found that a Δt_{aux} of at least $246\,\mathrm{ns}$ is needed to extract all the gate charge from the input capacitance of the devices.

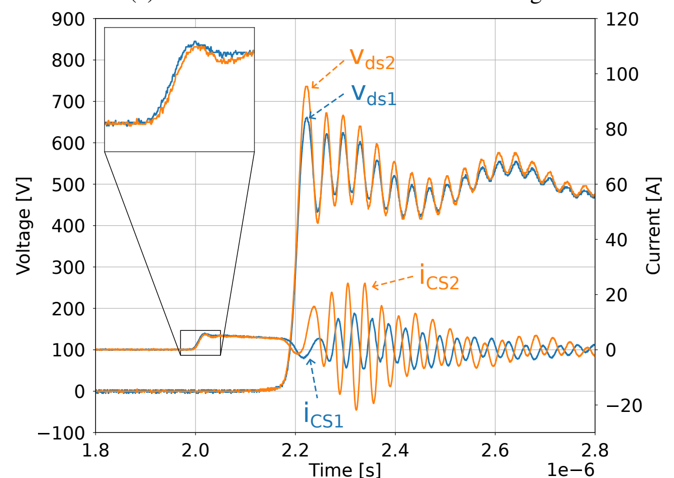
However, it is important to keep in mind that this is the energy required to drive the gate-source voltage down to -5 V. In fact, it is not required to completely remove the full $1330\,\mathrm{nC}$ of charge from the input capacitances of the SiC MOSFETs to turn them off. The drain-source voltage will already start rising when the Miller plateau is reached and the device will fully turn off at the gate threshold voltage, which is typically around $2.5\,\mathrm{V}$ for the CAB450M12XM3 module. Thus, a lower Δt_{pre} can also turn-off the serialized SiC MOSFETs, but at a slightly slower speed, meaning that Δt_{aux} might have to be increased to ensure device turn-off. Thus, the following experiments will be done for Δt_{pre} values between $100\,\mathrm{ns}$ and $1000\,\mathrm{ns}$ to explore the performance of the driver below the calculated minimum Δt_{pre} value from the previous paragraphs. Δt_{aux} will be initially kept at $300\,\mathrm{ns}$ to keep a safety margin that ensures that the devices will be turned off for $\Delta t_{\mathrm{pre}} > 500\,\mathrm{ns}$. For $\Delta t_{\mathrm{pre}} < 500\,\mathrm{ns}$, Δt_{aux} must be increased due to slower rate of charge extraction from the input capacitance of the SiC MOSFETs.

C. Voltage Balancing Control

The voltage balancing control is realized by adjusting Δt_{d} in Fig. 6b, i.e. the turn-on time delay between the two auxiliary switches Q_{aux1} and Q_{aux2}. In a practical converter, this would be accomplished by employing a closed loop control system with measurements of both drain-source voltages, v_{ds1} and v_{ds2}, to estimate the voltage imbalance. If an imbalance above a specific threshold is detected, balancing action would be taken by the control system. Such a system has not been implemented in this paper; however, the purpose of this paper is to demonstrate the operating principle and capabilities of the proposed hybrid active gate driver for achieving minimized voltage imbalance. The DSP in this setup is able to adjust the delays in both low and high resolution steps of $10\,\mathrm{ns}$ and $150\,\mathrm{ps}$, respectively. The steps of $150\,\mathrm{ps}$ are realized using the High-Resolution Pulse Width Modulator (HRPWM) module of the DSP [39], [40]. This allows very fine tuning of the gate signal delays, and precise control of the voltage imbalance can be achieved. An experimental result demonstrating imbalance between the measured drain-source voltages is shown in Fig. 12a. These measurements were performed at an input voltage



(a) Measured waveforms before balancing



(b) Measured waveforms post balancing

Fig. 12: Measured waveforms of both drain-source voltages and turn-off currents in CSGD paths at $V_{\mathrm{DC}} = 1\,\mathrm{kV}$ and current of $250\,\mathrm{A}$ with (a) disabled balancing and (b) enabled balancing.

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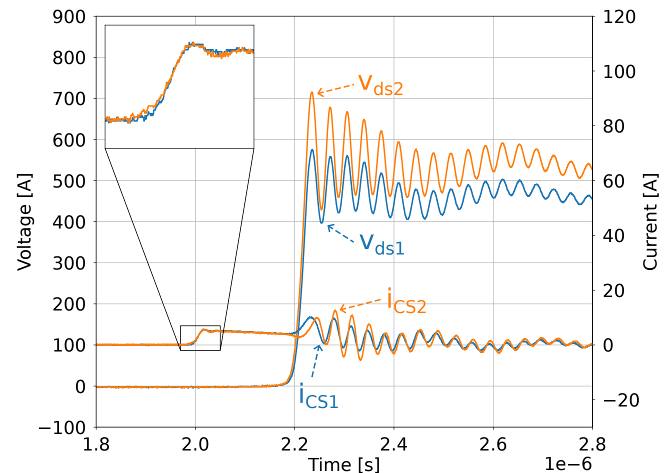
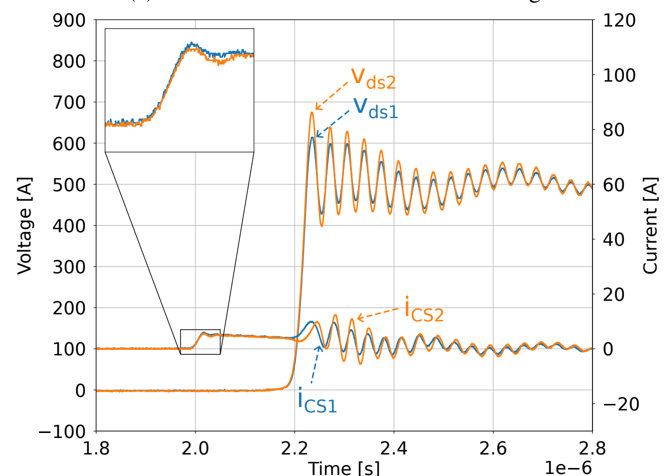
of $V_{\mathrm{DC}} = 1\,\mathrm{kV}$, drain current of 250 A. Δt_{pre} and Δt_{aux} were set to 500 ns and 300 ns, respectively. The gate current shown is not the gate current i_{g1}, but the current in the CSGD path, i_{CS1}, as illustrated in Fig. 2. This is due to compactness of the laboratory setup, that does not allow measurement of i_{g1}.

It is evident that the bottom device, M_2, is switching faster than the top device M_1. This might be due to a larger signal propagation delay in the driver of the top device or mismatch in other parameters, such as the threshold voltage or among the secondary inductances of the coupled inductor measured in Table III. In particular, measurements in Table III show that L_{s1} is 19 nH larger than L_{s2}. The implication of this is that i_{CS2} will start rising earlier than i_{CS1}, and results in faster switching of M_2 since its turn-off process is started slightly earlier. This mismatch in inductances seem to offset the effect of parasitic capacitance, which usually makes the top device switch faster, as explained in Section I. Thus, in this case, a delay should be applied to the bottom device to slow it down. In this example less than 2 % imbalance is the objective. The reason that the objective is set to 2 % is to avoid that the combination of large voltage imbalance and voltage overshoot at faster switching transients will move close to the 1.2 kV-rating of the SiC MOSFET. This is especially important for the following section, where experiments are performed at 1.5 kV. Each switch should then ideally block 750 V. An imbalance of 10 % would mean that one switch would block 900 V. The voltage across the switch would be close to its 1.2 kV-rating when this is combined with the expected voltage overshoot at higher di/dt. Therefore, the imbalance has been tuned to 2 % of the DC voltage. The measurements in Fig. 12b show that this objective is achieved by adjusting the delay of the bottom device to 13 ns. It can be observed in the zoomed views of the gate currents that the bottom-side gate current, i_{CS2}, is now slightly delayed compared to the the top-side gate current i_{CS1}. The result is a voltage imbalance of just 10 V.

The same experiment was performed at the same conditions as in Fig. 12, but for a lower current of 130 A. In similar fashion, the bottom device, M_2, switches faster than M_1. Thus, a delay 7.5 ns is applied to the gate signal of M_2, and the voltages are balanced.



(a) Measured waveforms before balancing



(b) Measured waveforms post balancing

Fig. 13: Measured waveforms of both drain-source voltages and turn-off currents in CSGD paths at $V_{\mathrm{DC}} = 1\,\mathrm{kV}$ and current of 130 A with (a) disabled balancing and (b) enabled balancing.

D. di/dt and dv/dt Control

By varying Δt_{pre}, i.e. the time Q_{p} is on, the amplitude of the gate current can be adjusted. Increasing Δt_{pre} will increase the amplitude of the gate current and discharge the gate faster, resulting in larger di/dt and dv/dt values. A lower Δt_{pre} will, on the other hand, decrease the amplitude of the gate current and slow down the switching transient, and thus increase switching losses. This is shown in Fig. 14 for three different Δt_{pre} values. These measurements were performed at a $V_{\mathrm{DC}} = 1.5\,\mathrm{kV}$ and current of 275 A.

Fig. 14 shows that the amplitude of the gate current increases with increasing Δt_{pre}. More specifically, this current increases from 2 A at $\Delta t_{\mathrm{pre}} = 100\,\mathrm{ns}$ to 7 A at $\Delta t_{\mathrm{pre}} = 1000\,\mathrm{ns}$. This in turn leads to faster switching transients as shown in Figs. 15 and 16. Δt_{aux} is set to 300 ns for $\Delta t_{\mathrm{pre}} > 500\,\mathrm{ns}$ and to 500 ns for $\Delta t_{\mathrm{pre}} < 500\,\mathrm{ns}$, in accordance with the considerations of Section III-B. A significant amount of oscillations can be observed in the i_{CS2} waveforms, especially in the 1000 ns and 500 ns tests. This is due to the fact that for higher Δt_{pre} the dv/dt will be larger during the turn-off switching transient. It can be observed that the voltage starts rising in Fig. 15 at approximately the same time the oscillations in i_{CS1} start. This will lead to a current flowing through the Miller-capacitance of the switch, C_{gd} and couple into the gate driver circuitry. The risk associated with this effect is that it might induce parasitic turn-on of the SiC MOSFET if there are no safety features on the gate-driver circuit. Typically, active Miller clamps are used to clamp the gate-source voltage to 0 V. Another option is to provide a negative supply voltage to increase the margin to the threshold voltage of the device. In this setup, the turn-off voltage of the device is set to -5 V, which provides a safe margin to the threshold voltage and no parasitic turn-on of the DUT is observed in the measurements. The sensitivity of the Rogowski

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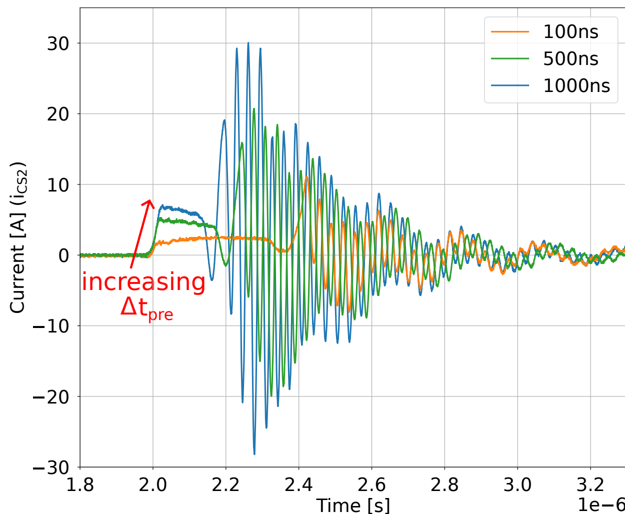

Fig. 14: Measured i_{CS2} for three different Δt_{pre} values at $V_{\mathrm{DC}} = 1.5\,\mathrm{kV}$ and current of $275\,\mathrm{A}$.

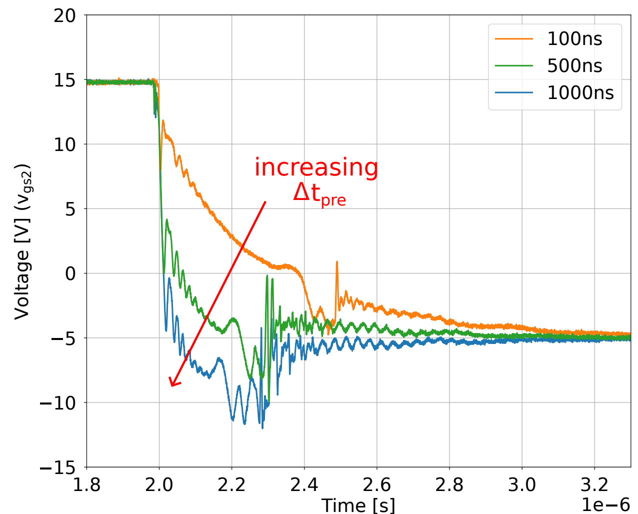

Fig. 16: Measured v_{gs2} for three different Δt_{pre} values at $V_{\mathrm{DC}} = 1.5\,\mathrm{kV}$ and current of $275\,\mathrm{A}$.

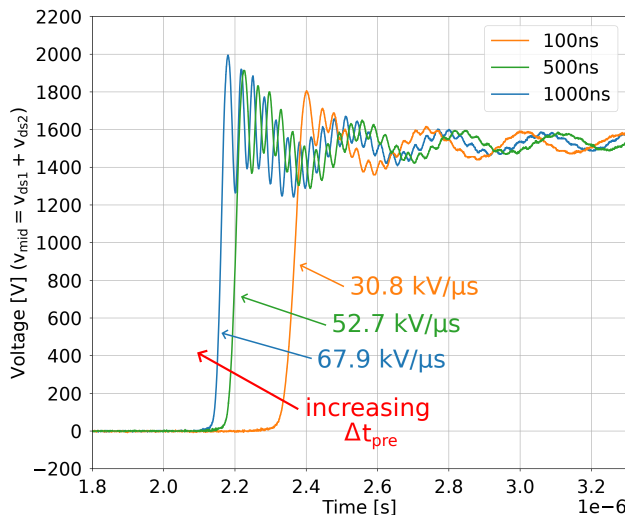

Fig. 15: Measured mid-point voltage v_{mid} for three different Δt_{pre} values at $V_{\mathrm{DC}} = 1.5\,\mathrm{kV}$ and current of $275\,\mathrm{A}$.

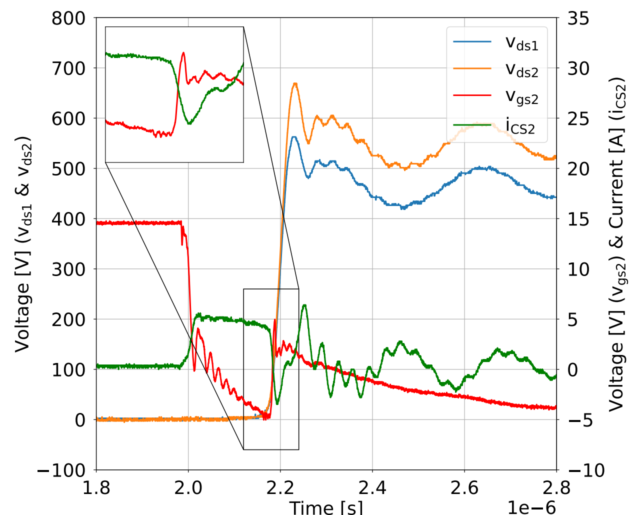

Fig. 17: Experimental waveforms showing the effect of disconnecting the CSGD path before the turn-off transient is completed. Measurement at $V_{\mathrm{DC}} = 1\,\mathrm{kV}$ and current of $250\,\mathrm{A}$.

coil is also of significance, as it will pick up large capacitive coupled interference due to the high dv/dt of the voltage transient [41]. The Rogowski coil used in the experiments for measuring i_{CS2} is not shielded, which makes it prone to low immunity against interference.

Fig. 15 shows the transient mid-point voltage. For larger Δt_{pre} values, the Miller plateau of the gate-source voltage is reached and traversed more rapidly, meaning that the turn-off voltage transient starts earlier and will complete with a higher dv/dt rate.

The same effect can be observed in Fig. 16. Increasing Δt_{pre} leads to a faster fall in gate-source voltage and there is a significant overdrive beyond -5 V in the $1000\,\mathrm{ns}$ case. However, the measured v_{gs2} is the external gate-source voltage of device and not the internal value, which will be different due to internal gate resistance and stray inductance in the internal gate-source loop of the module. Thus, the internal gate-source voltage of the device does not reach values below -5 V, and it is always in its safe operating area (SOA). This is illustrated in Fig. 17. The switches Q_{aux1} and Q_{aux2} are turned off before the turn-off transient is completed (with $\Delta t_{\mathrm{aux}} = 200\,\mathrm{ns}$ and $\Delta t_{\mathrm{pre}} = 500\,\mathrm{ns}$). The CSGD path is disconnected and the VSGD is trying to clamp the gate-source voltage to -5 V. However, it is not powerful enough to immediately supply sufficient current and the measured gate-source voltage bounces up to the internal level. Thus, a proper tuning of the hybrid gate driver is required in order to ensure a stable operation.

The measured drain-source voltages and drain current of

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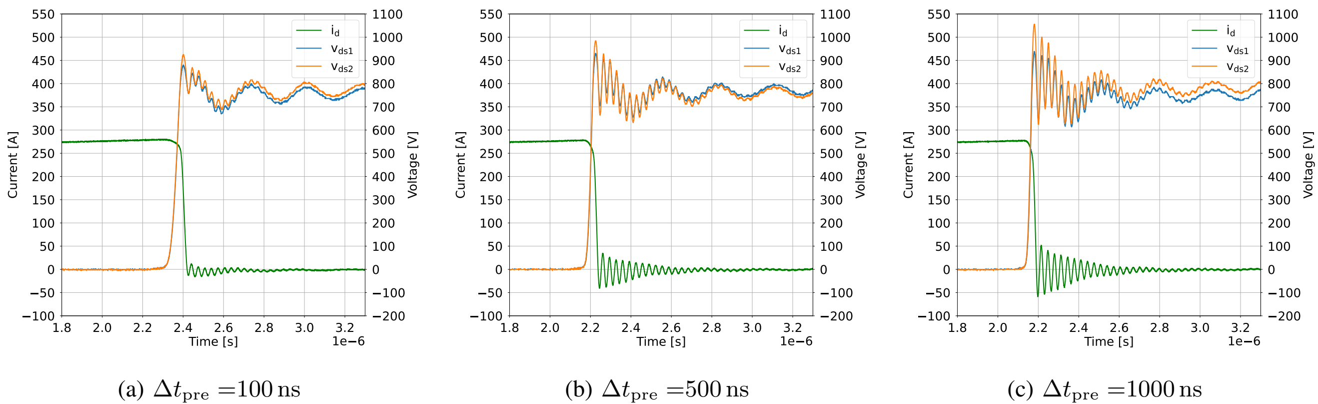

(a) Δt_{pre} =100 ns (b) Δt_{pre} =500 ns (c) Δt_{pre} =1000 ns

Fig. 18: Measured drain-source voltages and drain current for three different Δt_{pre} values at $V_{\mathrm{DC}} = 1.5\,\mathrm{kV}$ and current of 275 A.

the two devices in the stack are shown in Fig. 18 for the three different Δt_{pre} values. The balancing of the devices is tuned to be within 2 % of the total DC bus voltage. The trend is increased voltage overshoot and stronger oscillations with increased Δt_{pre}, which is expected. To limit the voltage overshoot a low-inductive design of the power module itself and PCB is required, or a lower di/dt, as the voltage overshoot, V_{osc}, is a function of Eq. (9). L_{s} is the stray inductance in the switching loop and di/dt is the drain current slew rate.

$$V_{\mathrm{osc}} = L_{\mathrm{s}} \cdot \frac{di}{dt} \tag{9}$$

However, a lower di/dt will increase the switching losses of the SiC MOSFET and thus it is more desirable to reduce L_{s}. This can only be achieved with a design optimized for low stray inductances [16], and the power module is a large part of that. The power module used in these experiments is not optimized for series-connection, and thus larger voltage overshoots are observed compared to power modules that are designed with chip-level series-connected SiC MOSFETs [42]. The results of varying Δt_{pre} are shown in Figures 19 and 20 for a finer resolution of Δt_{pre}. The trend is as expected; increasing Δt_{pre} increases dv/dt_{off}, di/dt_{off} and V_{osc}, while E_{off} is significantly reduced. The definitions to find the transient values are as follows:

- dv/dt_{off} - 40 % to 60 % of v_{mid}
- di/dt_{off} - 60 % to 40 % of i_{d}
- E_{off} - 10 % of v_{mid} to 10 % of i_{d} [43]

The dv/dt of the mid-point voltage is increased by 120 % when Δt_{pre} is increased from 100 ns to 1000 ns. A similar increase is observed in di/dt. The result is that the turn-off switching loss, E_{off}, is reduced by 41 %.

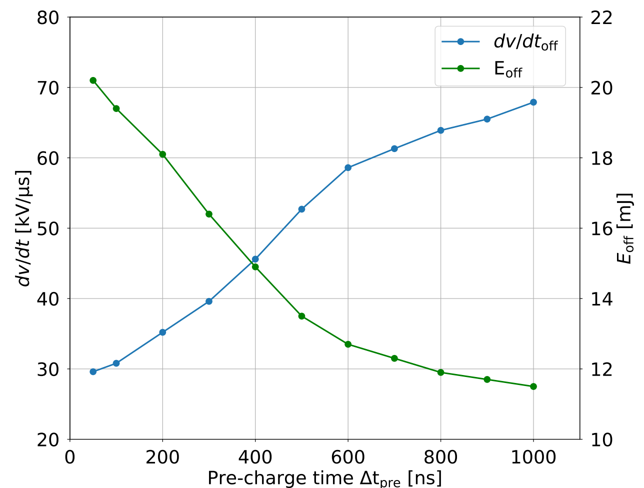

Fig. 19: Experimental results for dv/dt_{off} and E_{off} for different Δt_{pre} values for the turn-off transient at a voltage of 1.5 kV and current of 275 A.

E. Turn-on performance

The turn-on of the hybrid gate driver concept is accomplished with a conventional VSGD stage. The switching speed of the turn-on transient can thus only be adjusted by changing the gate resistors $R_{\mathrm{g(VS)}}$ or by adjusting the driving voltages V_+ and V_-, and no active control is possible. Measured turn-on waveforms are shown in Fig. 21. The turn-on process is independent of Δt_{pre} and will be identical for all the different cases that were assessed above.

F. Gate Driver Power Consumption

The driver was tested under continuous pulse-width modulation (PWM) operation to analyze its power consumption. The current and voltage from the 24 V DC power supply was measured and the range of the switching frequency was varied from 1 kHz to 30 kHz. The measurements were conducted for three different Δt_{pre} values, and are shown in Fig. 22. These measurements show the power consumption of both gate driver stages for both of the series-connected SiC MOSFETs.

The steady-state losses of the driver are slightly below 3 W and are due to losses in the DC/DC converters and linear regulators employed on the hybrid gate driver. The frequency-dependent losses are caused by recharging of the MOSFET gates and are increasing with frequency as expected. Larger Δt_{pre} will increase the power draw, as more energy

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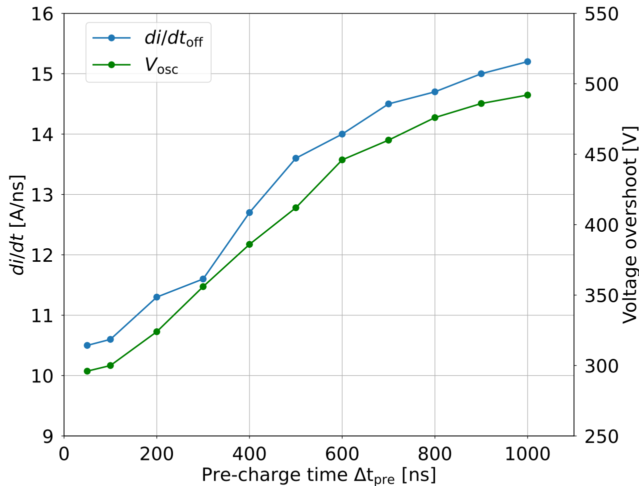

Fig. 20: Experimental results for di/dt_{off} and V_{osc} for different Δt_{pre} values for the turn-off transient at a voltage of $1.5\,\mathrm{kV}$ and current of $275\,\mathrm{A}$.

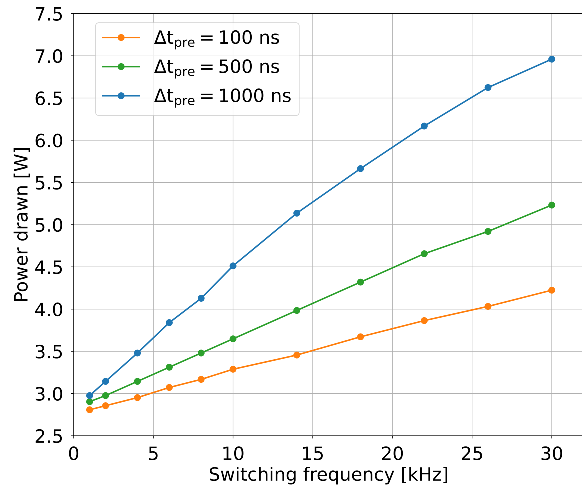

Fig. 22: Power drawn by the driver supply as a function of the driver switching frequency.

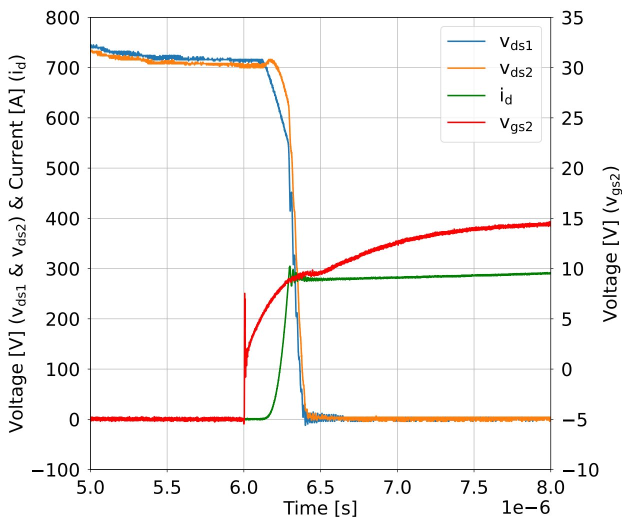

Fig. 21: Measured turn-on drain-source and gate-source voltages, and drain current at $V_{\mathrm{DC}} = 1.5\,\mathrm{kV}$ and current of $275\,\mathrm{A}$.

is required to charge the gate faster and more power is then wasted. However, at $10\,\mathrm{kHz}$, the turn-off switching power loss can potentially be reduced by $79\,\mathrm{W}$ according to Fig. 19 when Δt_{pre} is increased from $100\,\mathrm{ns}$ to $1000\,\mathrm{ns}$. Thus, the increase in driver power consumption from $3.3\,\mathrm{W}$ to $4.5\,\mathrm{W}$ is insignificant.

IV. Discussion

The presented hybrid driver concept for series-connected SiC MOSFETs is able to provide controllable turn-off switching times, and thus adjustable turn-off di/dt and dv/dt rates. This enables turn-off switching loss adjustment. Furthermore, since this is a driver concept for series-connected SiC MOSFETs, it exhibits functionality to balance the drain-source voltages among the power devices. Therefore, the proposed driver is a suitable concept for converters employing serialized devices, where controllable turn-off transients are a desired feature.

A. Advantages of Adjustable Switching Transients

Adjustable switching speeds are not only desirable for reduced switching loss. A reduced size of converter's magnetic components, such as filters, is also possible, as the frequency of the converter can be increased while keeping the switching loss constant due to the reduction in the switching energy of the turn-off transient. Furthermore, it can limit drain-source voltage overshoots, and thus allowing the converter to operate closer to its maximum SOA.

The proposed gate driver can also be advantageous in converters where it is desired to keep the turn-off dv/dt under a specific limit for a number of reasons. Among them is the fact that many digital isolators have a common-mode transient immunity (CMTI) limit of $50\,\mathrm{kV/\mu s}$ or even lower if they are used instead of optical fibers to transmit the gate driver signals. At higher load currents, the di/dt and dv/dt will increase, according to Eq. (10) [44]:

$$\frac{dv_{\mathrm{ds}}}{dt} = \frac{I_{\mathrm{d}} + g_{\mathrm{m}} \cdot (V_{\mathrm{th}} - V_{-})}{C_{\mathrm{gd}} \cdot (1 + R_{\mathrm{g}} \cdot g_{\mathrm{m}}) + C_{\mathrm{ds}}} \tag{10}$$

where I_{d} is the drain current and g_{m} is the transconductance. R_{g} is the gate resistance, and C_{ds} and C_{gd} are the drain-source and Miller capacitances of the MOSFET, respectively. Thus, it will be be necessary to reduce the switching speed by reduction of Δt_{pre} to keep the dv/dt below a specific limit. Similarly, at lower loads the switching speed will be lower and can increase with larger Δt_{pre} to work closer to the set dv/dt limit and thus have a more efficient converter.

Figure 23 summarizes how this can be achieved with the proposed hybrid driver. Assuming that the aim is to operate the switch at a dv/dt_{off} of approximately $25\,\mathrm{kV/\mu s}$ for currents

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between $50\,\mathrm{A}$ and $300\,\mathrm{A}$. This is achieved by tuning Δt_{pre} to the values shown in the figure. An increase in current means that dv/dt_{off} increases according to Eq. (10). Therefore, the switch must be slowed down by reducing the amplitude of the gate current and that is accomplished by reducing Δt_{pre}.

However, to achieve this adaptability, the gate driver must know what kind of timings (Fig. 3) must be executed during operation. A series of equations were developed in Section II, but these cannot reliably calculate the dv/dt due to the non-idealities in the circuit, such as the non-linear Miller capacitance. A suggestion would be to perform a series of similar measurements that were conducted in Section III-D for different current and voltage levels to establish appropriate timings under various switching conditions. The DSP can store these timings either as fitted expressions or in look-up tables in its memory, and then decide on the right operating parameters to achieve the desired performance. An alternative would be to integrate device-level models with the driver's DSP that can estimate the various timings for the desired operation of the gate driver in real time [45]. Measured data can be fed to device models whose outputs could be, for instance, the required gate current to reach a desired switching speed or reduction in switching loss. However, the scope of this paper was only to present the design and operating principles of a novel hybrid gate driver concept, which could be an integral part of serialized SiC MOSFETs.

It is also possible to extend this hybrid gate driver concept to enable control of the turn-on transition of the series-connected SiC MOSFETs. This was not implemented in the proposed driver due to the complexity involved, but it would most certainly extend the controllability of the switching losses. It would also open up for electromagnetic interference (EMI) control [46].

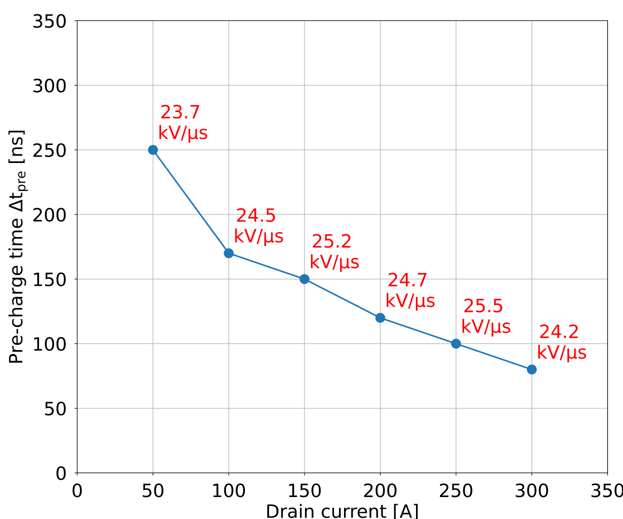

Fig. 23: Experimental results demonstrating the relationship between Δt_{pre} and drain current i_{d} at $V_{\mathrm{DC}} = 1\,\mathrm{kV}$ to keep dv/dt_{off} approximately constant.

B. Comparison of Different Voltage Balancing Techniques with the Proposed Method

The common goal of all the different voltage balancing schemes is to avoid excess overvoltage across the serialized semiconductor power devices so that they are not destroyed. This section of the paper will briefly present a comparison based on both qualitative and quantitative data of the different balancing schemes that can be found in literature today and for the proposed method in this paper.

1) Qualitative Comparison of Voltage Balancing Methods: A summary of the qualitative analysis is based on the following criteria: transient voltage balancing ability, switching loss, complexity in control, feasibility in adaptive control and cost is given in Table IV.

Out of the different methods that can be found in literature today, passive, active clamping and single gate drive methods, exhibit the lowest robustness for transient voltage balancing. Large passive snubbers must be connected across the SiC MOSFETs to achieve better balancing, whereas single drive methods rely on additional passive snubbers to achieve balanced voltages. Out of the different techniques, active gate drivers and gate delay compensation methods have the ability to reliably achieve the smallest voltage imbalances. The proposed method is able to achieve imbalances below $10\,\mathrm{V}$ at voltages beyond $1\,\mathrm{kV}$.

For fast switching SiC MOSFET the passive snubbers can generate losses that are comparable to the losses generated by the power device itself. That makes them the weakest in terms of added losses. Active clamping methods are slightly better than snubbers, but the losses are still increased while the device is being clamped. Some clamping methods also do require parallel snubbers for transient voltage balancing. Single gate drive will often require a secondary method to achieve balance, and those are usually snubbers. The gate delay methods and active gate control methods add the lowest losses to the system. They do not generally add any components to the power side of the device and the switching behavior is not altered significantly. Gate delay method will only add a delay to the turn-off transient, and thus the losses are kept the same. The proposed method in this paper is based on gate delay compensation, and thus it adds little to no additional losses to the system.

The control complexity of passive and active clamping solutions is low, since no measurements and control is needed for these solutions. The same can be said about single gate drive schemes. Gate delay compensation and active gate control methods are ranked higher in complexity. These methods require measurements and fast controllers for continuous operation, which will also be required for the proposed method. However, active gate control methods are also often even more complex than gate delay methods due to how the gate charge profile is modified and several additional controllable switches might be required. Furthermore, the additional ability of the proposed method to adjust the amplitude of the gate-currents during the turn-off of the serialized MOSFETs will increase the overall complexity of the driver, even though it is based on the relatively simple gate delay compensation.

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TABLE IV: Qualitative comparison of different voltage balancing methods for series-connection of SiC MOSFETs.

Type	References	Transient Voltage Balancing	Switching Loss	Control Complexity	Adaptive Control	Cost
Passive Solutions	[9], [16]–[18]	Medium	Poor	Low	No	Low
Active Clamping	[20], [21]	Medium	Poor	Low	Yes	Medium
Single Gate Drive	[22]–[25]	Poor	Poor	Low	No	Low
Gate Delay Compensation	[30]–[35]	Good	Good	Medium	No	High
Active Gate Control	[14], [26]–[29]	Good	Good	High	Depends on method	Medium-High
Proposed Method	-	Good	Good	High	Yes	High

Among the methods given in Table IV, only active gate control methods and the proposed method have the ability to adjust the switching transients for adaptive operation. However, not all active gate control schemes have the ability to control the equivalent switching speed of the entire string of series-connected SiC MOSFETs. For instance, the balancing scheme proposed in [14] will only adjust the switching speed of the device that switches faster, so that the turn-off transients are synchronized. Some active clamping methods are also viable for dv/dt control. These methods are also mostly demonstrated only for currents up to $100\,\mathrm{A}$. The proposed method can easily adjust the switching transient of the entire series-connection and its viability has been demonstrated for currents up to $300\,\mathrm{A}$.

The cost of the passive, active clamping and single driver methods are the lowest due to their simplicity. Gate delay and active gate control methods require high-bandwidth sampling and more powerful processing units, which will significantly increase their cost. Similarly, the proposed method will - in an application- require the same hardware for continuous operation, which makes this solution costly compared to the simpler balancing schemes.

2) Quantitative Comparison of Voltage Balancing Methods: An analysis based on quantitative data has also been performed to compare the proposed gate driver with prior arts. The analysis has been limited to methods based on gate delay compensation and active gate control, as these are the most relevant to the approach presented in this paper. Simulated losses presented in some of the prior arts papers are not considered.

Only references [30], [32] provide enough experimental data on gate delay compensation methods, whereas references [14], [26], [27], [29] provide enough data for active gate control methods. Only the voltage imbalance and turn-off energies are of interest, as well as the used device type and experimental testing conditions at which the switching energies were estimated. The switching energies are normalized by dividing each of them by the power at which they were obtained (i.e. division by the product of the experimental voltage and current). This is done to get a relatively fair comparison between the methods independently of the experimental conditions and the rating of SiC MOSFETs devices employed in the test setup. A summary of the findings is given in Table V.

This table shows that the proposed method results in a voltage imbalance below $2\,\%$, which is generally slightly lower compared to prior arts. However, the main contribution of the proposed method is its adaptability, which can be seen from the normalized switching loss (NSL) parameter. By increasing Δt_{pre}, the NSL can be reduced significantly. Compared to the work done in [14], [30], which are the only two papers that did experimental work on series-connected SiC MOSFET within the half-bridge modules and at higher currents, the proposed method has the advantage of decreasing the turn-off losses. Compared to [32], the proposed method can achieve a similar NSL.

The experimental results of [26], [27], [29] are difficult to compare with the proposed method. These approaches seem to be mostly suitable for low-power applications, and are not demonstrated for higher currents. Furthermore, they are based on devices using single-die packaging, e.g. TO-247.

V. Conclusion

This article proposes a novel hybrid gate driver concepts that employs both CSGD and VSGD stages to improve transient voltage balancing at turn-off process of series-connected SiC MOSFETs. The gate currents of the devices in the series-connection can be independently adjusted to achieve drain-source voltage imbalance below $2\,\%$ of the total DC bus voltage. The gate current amplitude can also be manipulated to control the turn-off di/dt and dv/dt to achieve controllable switching losses, which can be suitable for applications where there is a need to control the dv/dt or for just increasing the converter efficiency.

From experiments on a $1.2\,\mathrm{kV}/\ 450\,\mathrm{A}$ SiC MOSFET half-bridge module ($2.4\,\mathrm{kV}$ in series-connection), it has been shown that the dv/dt_{off} can be controlled in a range of $120\,\%$ and that the di/dt_{off} can be controlled in a range from $10.5\,\mathrm{A/ns}$ to $15.2\,\mathrm{A/ns}$. This gives a switching energy reduction of $41\,\%$ at the given test conditions. These results prove that series-connected SiC MOSFETs can be actively driven for switching loss control and simultaneously achieve voltage balancing within $2\,\%$ of the DC-bus voltage.

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TABLE V: Detailed comparison between prior gate delay compensation and active gate control methods, and the proposed method in terms of voltage imbalance and turn-off switching energy loss based on quantitative data.

Reference	Test Voltage and Current	Device Type	Voltage Imbalance [%]	$E_{\mathrm{off(tot)}}$ [mJ]	Normalized Switching Loss [mJ/(MVA)]
[30]	1500 V/ 135 A	Power Module	5	13.3	65.7
[32]	1800 V/ 15 A	Discrete	3.2	0.82	30.2
[14]	1800 V/ 250 A	Power Module	10	21.1	46.9
[26]	1000 V/ 20 A	Discrete	5	0.26	12.9
[27]	1000 V/ 20 A	Discrete	5	0.25	12.5
[29]	1200 V/ 35 A	Discrete	5	0.95	22.7
This paper	1500 V/ 275 A	Power Module	2	$\Delta t_{\mathrm{pre}} = 100$ ns: 19.4 $\Delta t_{\mathrm{pre}} = 500$ ns: 13.5 $\Delta t_{\mathrm{pre}} = 1000$ ns: 11.5	47.0 32.7 27.9

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