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Daniel Alexander Philipps

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Doctoral thesis

NTNU
Norwegian University of Science and Technology
Thesis for the Degree of Philosophiae Doctor
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Department of Electric Power Engineering

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Abstract

Silicon Carbide (SiC) power Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFETs) bear the potential of revolutionizing power electronic converters in regard to high efficiency, but also high power density converters and converter in harsh environmental conditions. These devices switch at unprecedented speed that can easily cause interference and risk to the surrounding circuitry.

Power MOSFETs require gate driver circuits to be switched on or off. Conventionally, Two Level Voltage Source Gate Drivers (VSGDs) have been used to realize this functionality. However, both the static and dynamic behavior of SiC power MOSFETs strongly depends on the operating conditions, such as DC voltage and load current. Two Level VSGDs cannot account for these changes, which results in suboptimal utilization of the power MOSFETs in a wide range of operating conditions.

Active Gate Drivers (AGDs), as opposed to conventional Two Level VSGDs, can be adjusted during the run time of the converter and therefore adapt the power MOSFET behavior to changing operating conditions. AGDs will therefore be of major importance to optimally utilize the advantages of SiC power MOSFETs in future power converters.

This work presents contributions concerning the accurate dynamic SiC power MOSFET characterization, AGD design and evaluation methodologies by means of two concrete examples, as well as control signal delivery to AGDs. The outcomes in these three subtopics are:

- A Low-Inductive Test Platform for accurate dynamic characterization of SiC power MOSFETs driven by conventional or active gate drivers,
- Two Multilevel Voltage Source Gate Drivers (MLVSGDs) offering switching slope and loss control as well as synchronous rectifier overshoot voltage suppression, and
- A systematic method of Wireless Communication Technology (WCT) adaptation in Power Electronics Systems (PES) demonstrated by the example of Bluetooth Low Energy (BLE) for wireless control of an MLVSGD.

Acknowledgements

The PhD work this thesis is based on, was funded by the Research Council of Norway under the FRIPRO grant 287820 "Adaptive Silicon Carbide Electrical Energy Conversion Technologies for Medium Voltage Direct Current Grids (ASiCC)". I want to say thanks to all the people who supported me. First and foremost my supervisor Professor Dimosthenis Peftitsis and my co-supervisor Professor Roy Nilsen. Detailed and always constructive discussions have helped through the PhD, focusing efforts on what we found important and meaningful. In addition, I want to thank Professor Francesco Iannuzzo, who has never feared clear words and honest opinions, which greatly improved my logic reasoning. Furthermore, I want to thank my colleagues, especially Gard Lyng Rødal, Kaushik Naresh Kumar, Andreas Giannakis, Yoganandam Vivekanandham Pushpalatha, and Tobias Nieckula Ubostad for technical discussions, input for adapting results of my work to their contexts, increasing value for knowledge transfer and reusability, and allowing me to put my mind and sometimes my hands on their work to distract me and collect energy for my own challenges. Thanks also go to the master students I supervised, Halvor Bratvold Ekren, and Mathias Fjeldberg Nerby, who did not hesitate to go the extra mile to produce high quality research results in the laboratory. On the personal side, I want to thank my fiance Anastasia, who, always on my side, keeps up my spirits in difficult times and challenges me to constantly improve. Finally, I want to thank my parents and my brother for being my safe harbor, for always being within sight.

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Nomenclature

Acronyms

AGD	Active Gate Driver
ATC	Active Temperature Control
BLE	Bluetooth Low Energy
CSGD	Current Source Gate Driver
CVR	Current Viewing Resistor
DPT	Double Pulse Test
DUT	Device Under Test
EMI	Electromagnetic Interference
ESL	Equivalent Series Inductance
FD	Free-wheeling Device
FEM	Finite Element Method
FFT	Fast Fourier Transform
IGBT	Insulated-Gate Bipolar Transistor
ITR	Information Transmission Route
LDO	Low-Dropout regulator
LITP	Low-Inductive Test Platform
MCU	Microcontroller Unit
MLVSGD	Multilevel Voltage Source Gate Driver
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
PCB	Printed Circuit Board
PES	Power Electronics System
PWM	Pulse Width Modulation
Si	Silicon
SiC	Silicon Carbide
SMD	Surface Mount Device
VERGD	Variable External Resistance Gate Driver
VNA	Vector Network Analyzer
VSGD	Voltage Source Gate Driver
WCT	Wireless Communcation Technology

Part I

Background

Chapter 1

Introduction

1.1 Motivation

Many European countries are moving away from fossil energy sources in response to international dependencies and the change of Earth's climate. National incentivization programs addressing parts of "The European Green Deal", Section 2.1.2 [1] have lead to a more decentralized and intermittent electric energy supply [2]. Both extracting electrical energy from Renewable Energy Sources (RES) optimally, but also providing electrical energy to many modern applications requires energy conversion, which is realized by Power Electronic Converters (PECs). It is estimated that today, more than 70 % of the entire electrical energy that is consumed, passes through at least one PEC [3].

The selection of PECs is economically driven, balancing investment and operating cost and meeting the required electrical specifications, such as maximum power conversion, system voltage and current. The investment cost is dominated by the cost of all components, i.e. active and passive electrical and thermal components, while efficiency and reliability of a PEC have the greatest impact on its operating cost [4; 5]. Every choice of a specific component is reflected in either of these aspects.

Active electrical components are at the center of every actively controlled PEC. The Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET) is such an active electrical component. Solid-state switches like the MOSFET enable controlling the direction of electric current, and thereby, the flow of electrical energy. This is possible because they comprise internal semiconductor structures that are either conductive or non-conductive depending on the input voltage, the gate-source voltage, of the device, and can therefore be controlled by this voltage [6; 7]. Although MOSFETs were less relevant in high power PECs in the past, they have become more important with the advent of new semiconductor materials and technology [8], which will be explained in detail later on. The focus of this work is therefore on MOSFETs. The input of a MOSFET behaves as a capacitance [6–9]. To change the input voltage, therefore, so-called gate driver circuits are needed to amplify a logic signal to

the corresponding input state of a MOSFET [9].

Operating solid-state switches is associated with losses originating from the non-zero conduction resistance, causing condition losses, and the non-ideal transitions between conducting and non-conducting state, causing switching losses [6; 7]. Recent research has therefore focused on finding semiconductor materials that allow low conduction resistance and low switching losses, so-called wide bandgap semiconductor materials. One of these materials is Silicon Carbide (SiC). The biggest advantage of SiC based power MOSFETs is the faster switching speed compared to their alternatives, i.e. Silicon (Si) Insulated-Gate Bipolar Transistors (IGBTs) [8]. These factors enable both low switching and conduction losses. On the system level, this results in higher efficiency at the same switching frequency. Alternatively, the switching frequency can be increased. For the same electrical performance, i.e. current and voltage ripple that originates from the converter switching, smaller inductors and capacitors are required at higher switching frequencies. Increasing the switching frequency, therefore, enables converters with a higher power density compared to designs with a lower switching frequency.

However, the fast switching behavior of SiC power MOSFETs also causes challenges, especially in regard to Electromagnetic Interference (EMI) [10–12]. The large gradients occurring during the switching transients can result in high voltage and current spikes, as well as high frequency oscillations. This potentially degrades the device performance and reliability, presents a health issue for passive components, introduces additional losses degrading efficiency, and may cause interference with other electronic equipment. To optimize the switching and conduction behavior of a MOSFET after converter fabrication and deployment, Active Gate Drivers (AGDs) enhance control over the gate charging and discharging process compared to conventional Two Level Voltage Source Gate Drivers (VSGDs) [11; 13]. Two Level VSGDs are not reconfigurable during operation, and must be designed to meet dynamic behavior requirements under worst-case operating conditions, which has performance degrading effect on non-worst-case operating conditions. Hence, significant behavioral improvements can be expected from the use of AGDs [11; 13].

1.2 Aim and Scope of this Thesis

In regard to the effective utilization of the improvement potential offered by AGDs, three fundamental challenges emerge:

- Accurate characterization of fast switching power MOSFETs in conjunction with different gate drivers including AGDs and Two Level VSGDs,

- Efficient evaluation of AGDs under varying operating conditions, including but not limited to load current and DC voltage, and
- Implementing AGD control signal delivery infrastructure for use in complex PECs.

The goal of the PhD project summarized in this thesis is to address at least one specific aspect of each of these three challenges. In particular, the objectives of the PhD project are:

1. Development of a Low-Inductive Test Platform (LITP) for accurate dynamic characterization of fast-switching discrete SiC power MOSFETs and AGDs, including high-bandwidth current measurement,
2. Development of an AGD for fast-switching SiC power MOSFETs, and
3. Development of a wireless interface for this AGD and demonstration of a wireless AGD control application.

1.2.1 Limitation of the Scope of this Thesis

Several research topics are closely related but are excluded from the scope of this PhD project. Furthermore, the PhD project does not address closed loop control of switching parameters. Moreover, no specific gate driver recommendations are given for concrete application scenarios. As the PhD project concentrates on AGD characterization, evaluation and control aspects, a comparison between different gate drivers is not in the focus of this thesis either.

1.3 Scientific Contributions

The contributions of the PhD project described in this thesis, are:

- A two-step characterization procedure for high-bandwidth, high-amplitude current sensors, that are suitable for accurate characterization and evaluation of discrete SiC power MOSFETs and AGDs,
- Design, implementation and verification of a Low-Inductive Test Platform (LITP) circuit for discrete SiC power MOSFETs in a TO-247 package,
- Design, implementation, and extensive experimental evaluation of a Four Level Multilevel Voltage Source Gate Driver (MLVSGD),

- Design, implementation, and experimental evaluation of a Three Level MLVSGD for suppressing surge voltages during unclamped inductive turn-off of SiC power MOSFETs operating as synchronous rectifiers,

- Definition of a taxonomy for Information Transmission Routes (ITR) in Power Electronics Systems (PES), and the development and demonstration of wireless,AGD control signal transmission.

1.4 Thesis Structure

This thesis is divided into four parts:

1. The introductory part contains:

   (a) The general motivation for research work on AGDs,

   (b) The scope definition of this thesis, and

   (c) The theoretical background to facilitate the understanding of the further thesis content.

2. The middle part describes the conducted research in three chapters in detail. The contents of the articles that are part of this thesis, are summarized and contextualized within the complete body of research work. However, this presentation is not strictly organized by the publications but rather by related topics because parts of a single publication may address different topics.

3. The work is then summarized, discussed as a whole, and put into the broader picture of ongoing research. The thesis is concluded with a critical reflection, an outlook on future work, and expected developments in the field of AGDs.

4. The articles that this thesis is based on, can be found as preprint versions in the last part of the thesis.

1.5 Research Dissemination

This thesis summarizes most of the scientific work conducted during the PhD project. The research results referred to in this thesis were formed into five main articles submitted for publication in different scientific channels. These five main articles are attached to this thesis in their preprint version:

J1 **Daniel A. Philipps** and Dimosthenis Peftitsis, "Performance Evaluation of High-Power, High-Bandwidth Current Measurement Technologies for SiC Power Devices," submitted to *IEEE Transactions on Power Electronics*, June 2023.

J2 **Daniel A. Philipps**, Peng Xue, Tobias N. Ubostad, Francesco Iannuzzo and Dimosthenis Peftitsis, "Low Inductive Characterization of Fast-Switching SiC MOSFETs and Active Gate Driver Units," accepted for publication in *IEEE Transactions on Industry Applications*, Early Access DOI: 10.1109/TIA.2023.3282930.

C1 Halvor B. Ekren, **Daniel A. Philipps**, Gard Lyng Rødal and Dimosthenis Peftitsis, "Four Level Voltage Active Gate Driver for Loss and Slope Control in SiC MOSFETs," published in *2022 IEEE 13th International Symposium on Power Electronics for Distributed Generation Systems (PEDG)*, Kiel, Germany, 2022, pp. 1-6, DOI: 10.1109/PEDG54999.2022.9923113.

C2 Andreas Giannakis, **Daniel A. Philipps**, Andrei Blinov and Dimosthenis Peftitsis, "A Three-Level Voltage-Source Gate Driver for SiC MOSFETs in Synchronous Rectification Mode," published in *2023 CPE-PowerEng - 17th IEEE International Conference on Compatibility, Power Electronics and Power Engineering*, Tallinn, Estonia, 2023.

J3 **Daniel A. Philipps** and Dimosthenis Peftitsis, "Wireless Control of Active Gate Drivers for Silicon Carbide power MOSFETs," submitted to *IEEE Open Journal of the Industrial Electronics Society*, May 2023.

Apart from the main publications, the following articles were published as part of the PhD project but were not included because they do not fit the scope of the thesis or because of a noteworthy extension in one of the main publications:

C3 **Daniel A. Philipps** and Dimosthenis Peftitsis, "A Flexible Test Setup for Long-Term Dynamic Characterization of SiC MOSFETs under Soft- and Hard-Switching Conditions," published in *PCIM Europe digital days 2021; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management*, Online, 2021.

C4 Tobias Nieckula Ubostad, Andreas Giannakis, Gard Lyng Rodal, **Daniel A. Philipps** and Dimosthenis Peftitsis, "Reduction of Parasitic Inductance and Thermal Management in a Multichip SiC Half-Bridge Module," published in *PCIM Europe digital days 2021; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management*, Online, 2021.

C5 **Daniel A. Philipps** and Dimosthenis Peftitsis, "Smart Universal Parameter Fitting Method for Modeling Static SiC Power MOSFET Behavior," published in *2021 IEEE 8th Workshop on Wide Bandgap Power Devices and Applications (WiPDA)*, Redondo Beach, CA; USA, 2021, pp. 372-377, DOI: 10.1109/WiPDA49284.2021.9645144.

C6 **Daniel A. Philipps**, Tobias N. Ubostad and Dimosthenis Peftitsis, "Low Inductive Platform for Long- and Short-term Dynamic Characterization of SiC MOSFETs," published in *2022 International Power Electronics Conference (IPEC-Himeji 2022- ECCE Asia)*, Himeji, Japan, 2022, pp. 2621-2627, DOI: 10.23919/IPEC-Himeji2022-ECCE53331.2022.9807002.

J4 Gard Lyng Rødal, Yoganandam Vivekanandham Pushpalatha, **Daniel A. Philipps** and Dimosthenis Peftitsis, "Capacitance Variations and Gate Voltage Hysteresis Effects on the Turn-ON Switching Transients Modeling of High-Voltage SiC MOSFETs," published in *IEEE Transactions on Power Electronics*, vol. 38, no. 5, pp. 6127-6142, May 2023, DOI: 10.1109/TPEL.2023.3243951.

C7 Tobias N. Ubostad, **Daniel A. Philipps** and Dimosthenis Peftitsis, "A Hybrid Current and Voltage-Source Gate Driver for Series-Connected SiC MOSFETs," in *11th International Conference on Power Electronics (ICPE 2023-ECCE Asia)*, Jeju, Korea, May 2023

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Chapter 2

Theoretical Background

In this chapter, the theoretical basis of the research work is laid out. The theory presented here is useful for deeply understanding the more advanced contents of this thesis. Basic knowledge in the field of electrical engineering and semiconductor materials is considered a prerequisite. This chapter mainly covers power semiconductor switches, in particular MOSFETs, the half-bridge circuit as the fundamental building block of power electronic converters, the wide bandgap semiconductor material Silicon Carbide, and gate driver basics.

2.1 Power Semiconductor Switches

Power Electronic Converters (PECs) transform electrical energy between different forms such as alternating and direct current, and different voltage and current levels by means of electronic switches. Such electronic switches are mostly made from semiconductor materials nowadays. Semiconductor switches that conduct high currents and block high voltages are referred to as power semiconductor switches.

The conduction state of power semiconductor switches is dependent on the input by a controlling voltage or current, depending on the switch type. Field-effect devices are voltage controlled switches. In Junction-gate Field-Effect Transistors (JFETs), the input voltage forms an electric field that suppresses the generation of majority charge carriers in a richly doped and therefore highly conductive semiconductor region [1; 2]. JFETs are therefore normally-on devices that conduct a current without any input voltage. Normally-on devices are not inherently safe in use with capacitors as energy storage components, as it is the case in the majority of converters. Therefore, JFETs are not further considered in this thesis.

MOSFETs, on the other hand, can be constructed as either normally-on or normally-off devices, the normally-off variants being more common. In MOSFETs, the input voltage induces an electric field that creates (normally-off) or suppresses (normally-on) the formation of a region with a high concentration of free minority charge carriers, the so-called inversion layer [1–3]. The

inversion layer is electrically conductive and thereby enables current flow to the surrounding regions of opposite doping, where the inversion layer charge carriers are majority charge carriers. MOSFETs are referred to as unipolar devices because only one type of charge carriers transports the device current [1–3].

As opposed to unipolar devices, both majority and minority charge carriers conduct current in bipolar devices. In Bipolar Junction Transistors (BJTs), an input current causes an injection of minority charge carriers into a thin semiconductor layer that is surrounded by semiconductor regions with opposite and weak doping [1; 3]. This injection lowers the charge carrier barrier energy of this thin region so far, that a large current can flow through the device. By choosing advantageous doping concentrations, both majority and minority charge carriers are injected into the low doping region, increasing its conductivity. This process is referred to as conductivity modulation [1–3]. In on-state, conductivity modulation lowers the resistance of the so-called drift region of low doping, that has a high intrinsic resistance because of its low doping used to block significant voltages in off-state. A drawback of employing this conductivity enhancing mechanism is that, at turn-off, the injected charge carriers have to be extracted or recombined before the blocking capability of the drift region is restored [1–3]. This severely limits the switching speed of bipolar devices employing conductivity modulation. In BJTs, the input current is amplified almost linearly. That means that a significant input current has to be supplied for keeping the BJT in conducting state. Therefore, the driving circuits providing this current require considerable amounts of energy.

The Insulated-Gate Bipolar Transistor (IGBT) combines a MOSFET and a BJT in a single structure. A MOSFET is used on the input and the MOSFET current is used as input current for a structure similar to a BJT. IGBTs, like power BJTs, employ conductivity modulation [1–3]. This enables high blocking voltages at low conduction losses, but also leads to a severe limitation of switching speed. In addition, a characteristic referred to as "tail current" occurs during the turn-off transition [1–3]. As the device current decreases and the charge carriers have to be extracted from the drift region for it to block the device voltage, the current change rate decreases significantly towards the end of the transition. This small but long-lasting nonzero device current increases the switching losses at turn-off significantly compared to MOSFETs that do not exhibit the same behavior.

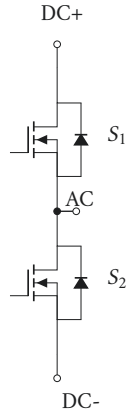


FIGURE 2.1. Half-Bridge circuit consisting of two MOSFETs

2.2 THE HALF-BRIDGE CIRCUIT

An essential building block of most so-called forced commutated converter topologies is the arrangement of two electronic switches in series. This circuit is called a half-bridge circuit. A half-bridge circuit consisting of two MOSFETs S_1 and S_2 is shown in Figure 2.1. The input of the half-bridge circuit consists of the two terminals DC+ and DC-. These terminals carry the input voltage and supply the circuit with power. The output of the half-bridge circuit is the "AC" terminal and can be on the potential of either of the input terminals, DC+ or DC-, depending on the states of the two switches. When realized with reverse conducting switches such as MOSFETs or IGBTs with an antiparallel diode, half-bridge circuits offer a freewheeling path for inductive currents, so that the inductor current is directed safely in every situation, even with both switches in off-state. The control signals of the two switches are inverted in comparison to each other to rule out a state in which the input terminals are shorted by the two switches being in on-state simultaneously. In most applications, a short time interval with both switches in off-state ensures that at no time, both switches conduct at the same time, causing a potentially destructive short-circuit between DC+ and DC-.

2.3 THE METAL-OXIDE-SEMICONDUCTOR FIELD-EFFECT TRANSISTOR

MOSFETs are semiconductor switch components that have three terminals, namely gate, drain, and source. The symbol of a typical power MOSFET (enhancement N-type MOSFET) in a schematic circuit diagram was already shown as part of the half-bridge circuit in Figure 2.1 (S_1 or S_2). Applying a positive voltage between the gate and source terminal of an enhancement N-type power MOSFET provokes the formation of an electric field within the device. With a

large enough gate-source voltage, an inversion layer of minority charge carriers is formed and, thereby, the device is switched on [1–3]. The so-called threshold voltage (V_{th}) is the input voltage at which the concentration of minority charge carriers induced by the field reaches the intrinsic concentration of majority charge carriers in the material hosting the channel (in N-type MOSFETs, this is a region with medium P-doping) [1–3]. This means a significant conductance is observed between drain and source. Applying a negative voltage between gate and source suppresses the conductive channel and thereby switches the device off. A typical specification of the input voltage, i.e. the gate-source voltage V_{gs}, is $-5\,V \leq V_{gs} \leq 20\,V$ [4; 5].

As unipolar devices, MOSFETs do not employ conductivity modulation. This results in both faster switching speed and higher resistance during conduction compared to bipolar devices such as the BJT or the IGBT [1; 2]. Typical power MOSFETs are inherently reverse conducting owing to the internal structure of these devices. This natural reverse conductivity is often modeled as a concentrated component, the body diode.

In many converters, reverse conduction is required. Because of the body diode of MOSFETs, an additional external diode is not strictly required. However, the built-in potential building up a forward voltage causes significant losses when the body diode is utilized. A way to reduce losses without an external antiparallel diode is to turn the MOSFET on. In addition to the natural reverse conductivity, the channel of a MOSFET can conduct currents in both directions in on-state [1]. Conducting a reverse current (from source to drain) in on-state is commonly referred to as synchronous rectification. [C2] elaborates on the application of a Three Level Multilevel Voltage Source Gate Driver (MLVSGD) addressing the turn-off transition of MOSFETs operated in synchronous rectification mode. In MOSFETs with a very high blocking voltage, the large drift region causes a high on-state voltage drop. Here, an additional antiparallel diode can lower the reverse conduction losses if its forward voltage is lower than the voltage drop caused by the MOSFET channel.

2.3.1 MOSFET Semiconductor Structure

MOSFETs can be based on different semiconductor materials. In the scope of this thesis, the semiconductor base material is Silicon Carbide (SiC). As mentioned earlier, the current in a MOSFET is conducted solely by one type of charge carriers, either electrons or hole. Electrons have a significantly higher mobility than holes and therefore, the conduction resistance of NMOSFETs, i.e. MOSFETs in which electrons support the conduction, is typically lower than the conduction resistance of PMOSFETs [1–3]. Hence, power MOSFETs

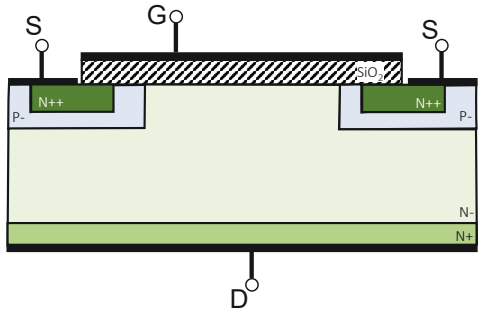


FIGURE 2.2. Idealized semiconductor layer structure of a planar vertical MOSFET

are usually NMOSFETs.

The semiconductor layer structure of a planar power MOSFET cell is shown in Figure 2.2. The gate contact connects to a metal plate referred to as the gate electrode. The gate electrode is isolated from the semiconductor material by a layer of silicon dioxide. The drain contact located at the bottom connects to a high-concentration N-doping layer, followed by a medium-concentration N-doping layer. This layer is the bulk material, and it is doped for good conductivity. Above this layer, there is a region with low concentration N-doping, the drift region. Its purpose is to conduct a current in on-state, but also to block the high drain-source voltage in off-state, thus the low doping concentration. The source contact connects to a high concentration N-doped region which conducts the device current in on-state. This high concentration N-doped region is embraced by a medium concentration P-doped region. The P-doped region is connected to the source contact as well to shorten the bipolar junction between the highly N-doped material, and the P-doped material. Thereby, potentially parasitic NPN-behavior is suppressed by forming a short-circuit between these regions [2; 3].

Multiple cells are arranged in a grid, and scaled to reach the desired maximum device current. Manufacturers deliver MOSFETs in various forms, i.e. different packages, but also as the semiconductor base unit, which is called ”die” and must be connected by the client, mostly by soldering the bottom (drain contact area) to the baseplate carrying thick conductive layers of copper, and wire bonding, soldering, or press contacting on the top (gate and source contact areas, through brackets or spring-loaded contacts) [2].

2.3.2 *Working Principle*

When applying a positive voltage between gate and source, the resulting field shifts the Fermi energy levels in the P-material. With a sufficiently large elec-

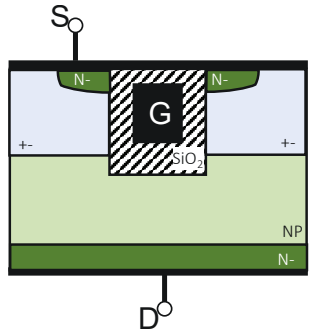


Figure 2.3. Idealized Semiconductor Layer Structure of a Trench MOSFET

tric field and resulting Fermi energy level shift, the minority charge carriers, electrons in the P-material, accumulate near the gate electrode, because there, the electric potential is the highest. The region with accumulated electrons is referred to as the inversion layer, and, in the context of the MOSFET, the conductive channel, or short, channel. This channel conducts the device current in on-state [1–3].

This working principle is identical among different MOSFET structures. The most important alternative power MOSFET structure is the trench-gate MOSFET shown in Figure 2.3. By arranging the silicon dioxide and gate electrode buried inside the semiconductor material, and the N- and P-doped regions accordingly, the channel is oriented vertically instead of horizontally in the case of planar MOSFETs. The main advantage of this structure is that, for one channel, it requires less surface area. Therefore, the amount of channels per square area can be significantly higher than in a planar MOSFET. This means an increased current density is achievable with the same square area, which is proportional to the size of the semiconductor material wafer, and thereby, wafer cost. These cost improvements come at the expense of a more complex production process [1; 2].

As mentioned above, MOSFETs switch significantly faster than IGBTs under identical conditions, as they do not use conductivity modulation. a phenomenon used to lower conduction resistance in bipolar devices. At the same time, the drift region conductivity is significantly lower in a MOSFET than in an IGBT with the same rating as only the majority charge carriers conduct the device current, and the doping concentration of the drift region is only marginally higher.

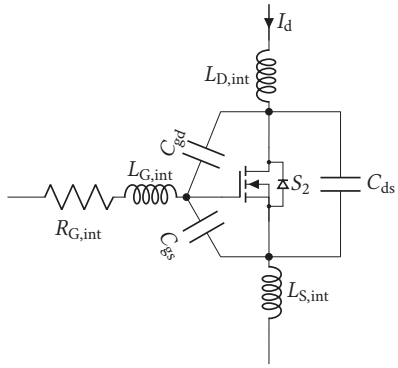


FIGURE 2.4. Typical power MOSFET model structure

2.3.3 *Device Characteristics*

Ideal switches are ideal conductors with zero impedance in on-state, and ideal isolators in off-state with an infinite impedance. Real semiconductor switches are not ideal. In on-state, they exhibit a conduction resistance that depends on the input and output voltages. Apart from that, the various device structures result in capacitances between the terminals that are highly voltage dependent, as the electric field changes the position of capacitive charge accumulations within the semiconductor layers. In addition, the device terminals must be contacted with the semiconductor material through a metallization layer. Bonding wires, conductive sheets, or clips that are used to establish these connections have a finite length and therefore introduce inductance. Equally, the device leads and conductor structures of the device package add inductance [1; 2].

Modeling

To simulate switching devices, their electrical behavior including all above-mentioned characteristics is mathematically modeled. MOSFET models consist of different parts, each reflecting

- The behavior of the channel,
- The reverse conduction, and
- The dynamic device characteristics.

Electrothermal models also include a part that represents the thermal device behavior with an equivalent electric circuit.

Figure 2.4 shows the typical components of a power MOSFET model. S_2 represents both the body diode and the MOSFET channel. The channel is

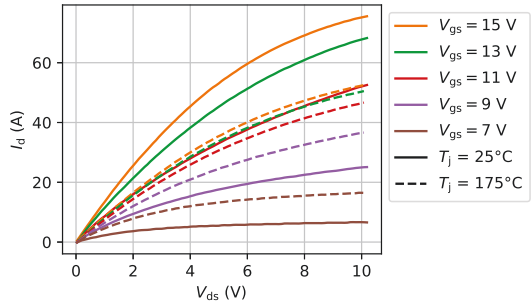


FIGURE 2.5. Exemplary SiC Power MOSFET Static Output Characteristics ($I_d\,(V_{ds}, T_j)$). Data from Wolfspeed C3M0075120D SiC power MOSFET datasheet [7].

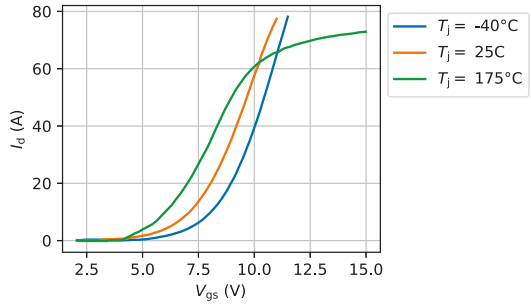


FIGURE 2.6. Exemplary SiC power MOSFET static transfer characteristics ($I_d\,(V_{gs}, T_j)$). Data from Wolfspeed C3M0075120D SiC power MOSFET datasheet [7].

modeled by one or more non-linear equations describing the transconductance of the device. The reverse conduction is commonly modeled as one diode or several diodes in parallel, and the device capacitances and inductances, that influence the dynamic device behavior, are reflected by concentrated components in the model circuit. Some models integrate the output capacitance with the body diode model. In addition to that, C_{gs} is often modeled as a constant capacitor, while C_{gd} is implemented as a voltage dependent capacitor with a nonlinear differential equation [6]. The internal inductances are constant inductors in most models.

Static Device Characteristics

The static device characteristics of a MOSFET are the output characteristic, i.e. the drain current in dependence of the drain-source voltage for varying gate-source voltages, $I_d\,(V_{ds})$, and the transfer characteristic, i.e. the drain current in dependence of the gate-source voltage with a constant drain-source

TABLE 2.1. Extraction parameters according to IEC 60747-8 [8]

Parameter	Meaning
E_{off}	Turn-off Switching Energy
E_{on}	Turn-on Switching Energy
t_{f}	Voltage Transition Time at Turn-off
t_{r}	Voltage Transition Time at Turn-on
$t_{\text{d,off}}$	Delay Time at Turn-off
$t_{\text{d,on}}$	Delay Time at Turn-on

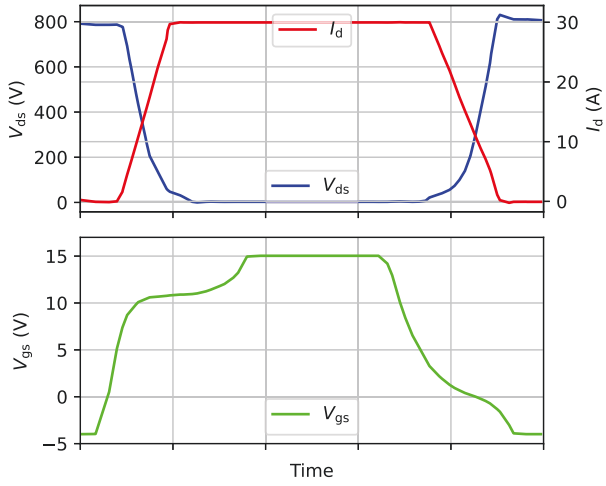


FIGURE 2.7. Schematic power MOSFET switching transition waveforms. Data from Wolfspeed C3M0075120D SiC power MOSFET datasheet [7].

voltage, $I_{\text{d}}\left(V_{\text{gs}}\right)$. These characteristics describe the channel behavior [1–3]. Figure 2.5 shows an exemplary static output characteristic, and Figure 2.6 shows an exemplary static transfer characteristic. The data were derived from a Wolfspeed C3M0075120D discrete SiC power MOSFET datasheet [7].

To obtain the static device characteristics, a Power Device Analyzer (PDA) like the Keysight B1505A is used. The characteristic data are utilized in the development and tuning of MOSFET models to fit experimental data. Model adjustment is a complex topic and not within the scope of this thesis. Employing an efficient adjustment method can significantly improve model accuracy and the adjustment procedure itself, which is a high-order multidimensional, non-linear optimization problem [C5].

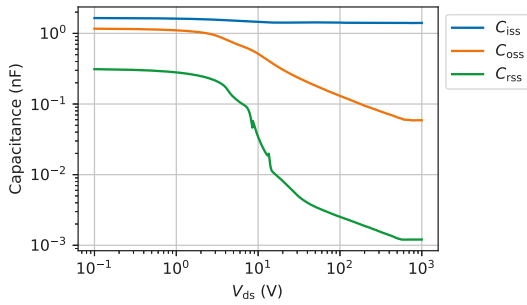


FIGURE 2.8. Input capacitance (C_{iss}), output capacitance (C_{oss}), and reverse capacitance (C_{rss}) under varying drain-source voltage (V_{ds}). Data from Wolfspeed C3M0075120D SiC power MOSFET datasheet [7].

Dynamic Device Characteristics

The IEC 60747 standard defines characteristic switching parameters of various power semiconductor devices. In particular, the IEC 60747-8 part of this standard considers MOSFETs [8]. The parameters defined in the standard are listed in Table 2.1 with their respective meaning. Figure 2.7 displays schematic switching transition waveforms. The data were extracted from the datasheet of the C3M0075120D discrete SiC power MOSFET from Wolfspeed [7].

The switching behavior of a MOSFET is influenced by the parasitic device capacitances and inductances.

Device Capacitances: With a suitable extension, a PDA can be used to measure the capacitances of a device, i.e. the gate-source capacitance C_{gs}, the gate-drain capacitance C_{gd}, and the drain-source capacitance C_{ds}. C_{gs} originates mostly from the Metal-Oxide-Semiconductor section of the device. It is the largest of the device capacitances. C_{gd} and C_{ds} are the capacitances that are formed with gate and source as one electrode, the semiconductor structure as dielectric, and the drain as the opposite electrode. C_{gd} is slightly smaller than C_{ds}, as the oxide layer between the gate and the semiconductor layers adds to the distance between the gate and the drain electrode. Therefore, $C_{gs} >> C_{ds} > C_{gd}$ [1–3].

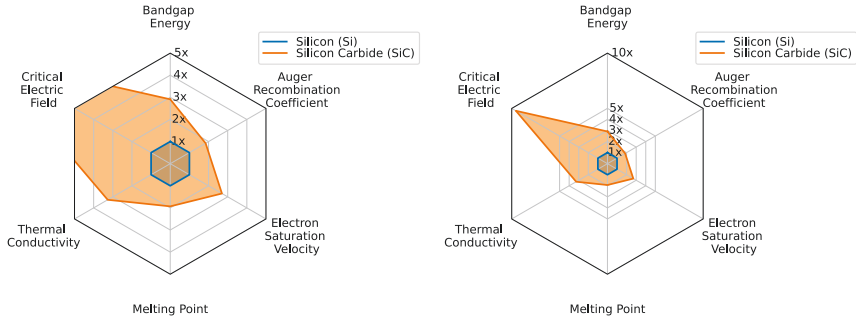
In datasheets, the input capacitance $C_{iss} = C_{gs} + C_{gd}$, the output capacitance $C_{oss} = C_{ds} + C_{gd}$, and the reverse capacitance $C_{rss} = C_{gd}$ are often given instead. An exemplary capacitance characteristic of a Wolfspeed C3M0075120D discrete SiC power MOSFET is shown in Figure 2.8. As can be seen in this figure, the device capacitances vary in dependency of the bias voltage that is applied between drain and source, V_{ds}. C_{iss} is the least dependent on V_{ds}. Since $C_{gs} >> C_{ds}$, $C_{iss} = C_{gs} + C_{gd} \approx C_{gs}$, and because C_{gs} is not strongly influenced by a V_{ds} bias, C_{iss} does not show a strong dependence either. The regions that

form C_{oss} and C_{rss}, on the other hand, are exposed to the entire V_{ds} bias voltage. The electric field provoked by the bias voltage depletes the drift region from charge carriers. Hence, the charge accumulations that form the capacitances C_{gd} and C_{ds} are separated further as V_{ds} increases, which results in a lower capacitance [1–3]. This tendency can be clearly identified in Figure 2.8.

How to use capacitance data for developing highly accurate real-time models has been demonstrated in literature [J4]. The device capacitances primarily slow down the switching transitions. The gate-drain capacitance, called "Miller Capacitance", is the most influential in this regard. During the voltage transitions, the change in voltage across the device output is equally present across gate and drain, while the voltage across gate and source changes only very slowly or remains nearly constant due to the so-called Miller effect. This can be seen in Figure 2.7 looking at the V_{gs} during the transitions of V_{ds}. The considerable voltage dependency of C_{gd} can also be observed in this figure. At the beginning of the V_{ds} transition, V_{gs} is still rising at a comparably large rate. However, with V_{ds} falling below approximately 200 V, V_{gs} rises at a much decreased rate, even with a decreasing slope in V_{ds}. This is caused by the significant increase of C_{gd} towards low bias voltages V_{ds}. For the same reason, the effect of a slowing V_{gs} transition is by far less pronounced during turn-off. The initial change in V_{ds}, where C_{gd} is comparably large, is supported by a high gate current allowed for by a large voltage drop between the low gate driving voltage and the voltage present at the gate. Therefore, this initial charging phase is quickly transitioned, and the voltage rise accelerates as C_{gd} diminishes. Therefore, a steady decrease in V_{gs} can be observed despite the Miller effect.

Parasitic Inductances: The parasitic device inductances usually cannot be determined with a PDA. Instead, either Finite Element Method (FEM) simulations, or switching tests are conducted to arrive at estimates for the device inductances. The main contributors to the parasitic device inductances are the lead inductances introduced by the device package.

A voltage forms across the parasitic inductances whenever the device current changes. Therefore, at turn-off of the power switch, the negative slope of the device current leads to a voltage added to the DC voltage across the switching device, caused by the parasitic inductances of the circuit layout, and the device lead inductances at drain and source. In switching waveforms, this can be identified as a reduction in V_{ds} while I_d increases at turn-on, and a voltage overshoot while I_d decreases at turn-off. The switching waveforms shown in Figure 2.7 are somewhat idealized. As the current and voltage slopes overlap strongly in this figure, it is not possible to see the voltage drop caused by the current slope at turn-on. At turn-off, the voltage overshoot is visible. In reality, however, both inductive voltage drop at turn-on and voltage overshoot at turn-off are more significant than in the idealized waveforms of Figure 2.7.



(A) Critical electric field outside plot area

(B) Critical electric field included

Figure 2.9. Silicon Carbide (SiC) material properties relative to Silicon (Si) based on values from literature [10].

This is shown and described in detail in [J2].

In addition, a part of the source inductance is shared between the gate loop and the power loop, called the common source inductance. Therefore, also a part of the associated voltage drop is injected into the gate loop. This voltage drop changes the effective voltage across the device channel. During both turn-on and turn-off, this leads to a slow-down of the respective switching processes. The voltage drop caused by the common source inductance can usually not be directly observed because it is not possible to measure the gate source voltage at the die level without disassembling a packaged MOSFET. The increase of switching loss energies, however, becomes apparent when comparing the datasheets of two MOSFETs that incorporate the same MOSFET die, but in different packages. For example, the TO-247-3 package is characterized by a very large common source inductance, as the gate loop and the power loop share the same package lead. On the contrary, the TO-247-4 package has two separate source leads, one for the power loop and another for the gate loop, called "Kelvin source" lead. Taking the Wolfspeed C3M0075120D [7] and C3M0075120K [9] as an example, the device in the TO-247-4 package exhibits only approximately 30 % of the switching losses at turn-on, and 48 % of the switching losses at turn-off that occur in the otherwise identical device in a TO-247-3 package. This emphasizes that the common source inductance is a critical parasitic inductance, which should be minimized as much as possible.

2.4 Silicon Carbide

The majority of power switching devices in operating converters today is based on Silicon (Si) as a semiconductor material. However, with 1.12 eV, the bandgap

Table 2.2. Silicon Carbide (SiC) material properties in comparison to Silicon (Si) [10]

Property	Si	SiC
Bandgap	1.12 eV	3.23 eV
Built-in pn-junction Potential	0.9 V	3.25 V
Auger recombination coefficient	3.79×10^{-31} cm^6/s	7×10^{-31} cm^6/s
Electron mobility	1420 cm^2/Vs	1000 cm^2/Vs
Hole mobility	470 cm^2/Vs	115 cm^2/Vs
Electron saturation velocity	1.05×10^7 cm/s	2.00×10^7 cm/s
Critical electric field strength	0.3 MV/cm	3 MV/cm
Melting point	1414 °C	2730 °C
Thermal conductivity	1.5 W/cmK	4.9 W/cmK

of Si is comparatively narrow [10]. The bandgap of a material is the energy difference between the valence and the conduction band. These bands describe electron energy levels. If valence and conduction band are separated, electrons in the valence band are locked to the core of an atom, while electrons in the conduction band can travel through the material and therefore conduct current, and the opposite holds for holes. Materials with a large bandgap are isolators, while materials with no bandgap or an overlap of valence and conduction band are conductors, and materials in between are semiconductors that can conduct a current under certain circumstances, such as elevated temperatures, excitation with light, charge carrier injection, or doping with other materials [2]. Semiconductor materials with a narrow bandgap conduct current more easily, but their blocking capability is limited. As a result, the material width required to realize Si MOSFETs with a high blocking voltage (more than 1.2 kV), would result in a large drift region resistance and subsequently unacceptable conduction losses.

Wide bandgap semiconductor materials have been studied extensively in the past. The most influential wide bandgap material for high power switching devices is Silicon Carbide (SiC). The material characteristics of SiC in comparison with Si are listed in Table Table 2.2 and Figure 2.9 shows a summary of the most relevant material characteristics of SiC relative to Si. The values have been taken from fundamental literature [10]. The critical electric field strength is about an order of magnitude different, therefore, two plots are given for better overview. With 3.23 eV, SiC has a 2.88 times wider bandgap than Si with 1.12 eV. The higher bandgap results in a higher built-in potential of pn-junctions in SiC (approximately 3.25 V at 300 K) compared to Si (approximately 0.9 V at 300 K). As a consequence, the body diode forward voltage is larger in SiC MOSFETs than in Si MOSFETs. The wide bandgap leads to a reduced intrinsic generation of electron-hole-pairs that are located in the conduction (electrons) and valence band (holes) after generation, and support conduction. Therefore, SiC has a significantly higher specific resistance for the same doping

conditions. This is amplified by the higher rate of free charge carrier recombination, quantified by the Auger recombination coefficient (7×10^{-31} cm^6/s in SiC vs 3.79×10^{-31} cm^6/s in Si). In addition, the available P and N doping materials for SiC are located at a large potential difference from the intrinsic boundaries of the valence (P doping material) and conduction band (N doping material) in SiC. This results in a high activation energy requirement for the ionization of the doping materials, which further increases the specific resistance of SiC despite doping. Another set of related material properties are the electron and hole mobility. In SiC both the mobility of electrons (1000 cm^2/Vs) and of holes mobility (115 cm^2/Vs) are lower than in Si (1420 cm^2/Vs and 470 cm^2/Vs respectively), adding to the higher specific resistance of SiC. At the same time, the saturation velocity of electrons in SiC (2×10^7 cm/s) is double that in Si (1.05×10^7 cm/s). Moreover, the wider bandgap induces a considerably higher critical electric field of SiC compared to Si. SiC has a critical electric field of 3 MV/cm, which is ten times that of Si, 0.3 MV/cm. Finally, SiC has a higher melting temperature (2730 °C) than SI (1414 °C) and also the heat conductivity is notably higher in SiC (4.9 W/cmK) compared to Si (1.5 W/cmK).

On the level of switching devices, the material properties of SiC have the following implications: With the same drift region width, SiC devices can achieve a manifold increase in blocking voltage capability compared to Si close to the theoretical factor of 10. Although the specific resistance of the drift region is significantly increased in SiC as was discussed before, the higher critical electric field strength compensates this effect multiple times. This has two major implications:

- For the same blocking voltage specification, SiC devices can be designed with a significantly thinner drift region than Si devices, resulting in a much lower on-state resistance $R_{DS,on}$ and therefore, lower conduction losses.

- For the same conduction loss performance, on the other hand, SiC MOSFETs can support significantly higher blocking voltages than Si MOSFETs. While realistically being limited to blocking voltages of up to 200 V in early stages of the technology [10], technological advances enabled 600 V devices in 1998 [11], and as of today, even 1.7 kV devices are commercially available [12], albeit limited to low load currents (up to 5 A in this example). Realistically, Si MOSFET technology only compete with their SiC equivalent up to 950 V [13], and still require more powerful driver circuitry because the required gate charge is significantly larger than in similar SiC power MOSFETs (for example Wolfspeed C3M0065100K [14]). SiC MOSFETs, on the other hand, are available for notably higher system voltages than 950 V and higher currents, that

were previously only reachable with Si IGBTs.

SiC MOSFETs thus enter the competition with Si IGBTs, that are superior to Si MOSFETs in high power applications due to higher voltage blocking capability and better conduction performance enabled by conductivity modulation, i.e. the injection of both electrons and holes into the low doping drift region [2; 10]. The resulting tail current increases switching losses, barring Si IGBTs from high switching frequency operation. SiC MOSFETs do not utilize conductivity modulation, and the higher saturation velocity of electrons and the higher recombination rate of free charge carriers induce very fast charge carrier dynamics. Therefore, SiC power MOSFETs switch considerably faster compared to Si MOSFETs, and especially, Si IGBTs. The higher temperature stability of SiC cannot be effectively exploited on the device level, as the packaging technologies used today do not support temperatures as high as the semiconductor material limits. However, the higher heat conductivity of SiC enables more effective heat transfer from the top of the semiconductor structure, where the channel and thereby the loss emitting structure is located, to the bottom, where heat is extracted through the baseplate to the heat sink of the converter. Overall, this allows for higher operating temperatures without overheating the junction region and thereby degrading the device.

From a system perspective, the lower switching losses of SiC MOSFETs in comparison with Si IGBTs can be utilized to increase the efficiency, or the switching frequency, or a mixture thereof. Increasing the switching frequency allows reducing the size of passive components, which increases power density, both in terms of volume and weight. Operating at higher system temperatures simplifies converter cooling.

In summary, the material properties of SiC enable SiC MOSFETs to operate in a system voltage range previously dominated by Si IGBTs. The higher switching speed of SiC MOSFETs enables the use of higher switching frequencies and thus higher power density converter designs with the same or better efficiency compared to using Si IGBTs. Due to falling component prices and dwindling concerns about the reliability as production processes improve, SiC MOSFETs are becoming an increasingly interesting replacement for Si IGBTs for the voltages above 1 kV [15; 16].

2.5 GATE DRIVERS

To establish the conductive channel in a MOSFET, the gate-source capacitance C_{gs} must be charged, and to close the conductive channel, C_{gs} must be discharged. These charging and discharging processes require more power than a microcontroller or other signal-level integrated circuit can deliver. In

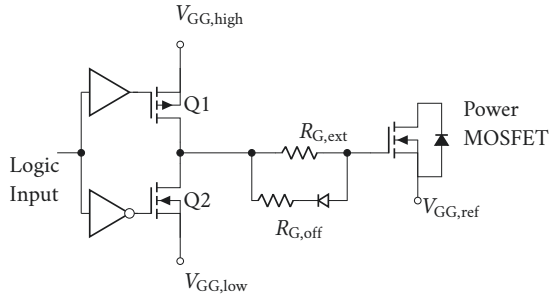


FIGURE 2.10. Two level voltage source gate driver schematic diagram

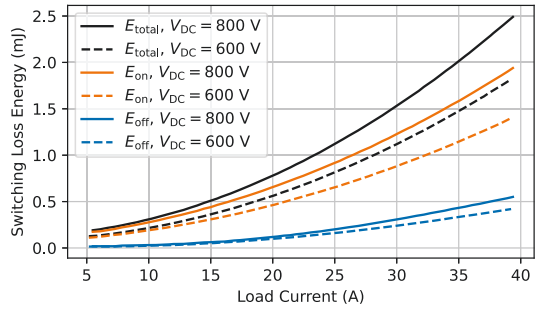


FIGURE 2.11. Switching loss energy for varying $V_{DC} = 600\,V, 800\,V$ and $I_{load} = 5\,A \ldots 39\,A$, but constant $R_{G,ext} = 0\,\Omega$ and $T_j = 25\,°C$. Data from Wolfspeed C3M0075120D SiC power MOSFET datasheet [7].

addition, the gate-source voltages in on- and off-state of the power MOSFET, for example 15 V and −4 V respectively, are outside the range of signal level electronics. Therefore, additional circuitry is required for charging and discharging C_{gs}, which is called "gate driver". Taking the structure of the half-bridge topology presented in Section 2.2 into account, a gate driver is required with the source potential of the upper MOSFET (S_1) as reference potential. This potential equals the DC+ potential when S_1 is conducting and DC-, when S_2 is conducting. Therefore, the gate driver must incorporate some form of galvanic isolation between its signal input and gate and source output terminals. This galvanic isolation is subject to the high switching slopes of the voltage transitions. To avoid large capacitive common mode currents, the coupling capacitance forming across the galvanic barrier must be as small as possible.

Gate drivers, together with the device characteristics, determine how the switching device behaves both dynamically, i.e. during the switching transitions, and statically, i.e. outside the switching transitions. Thereby, gate drivers exert great influence on the switching and conduction losses of the MOSFET, as well as the maximum slope steepness in both device current and voltage.

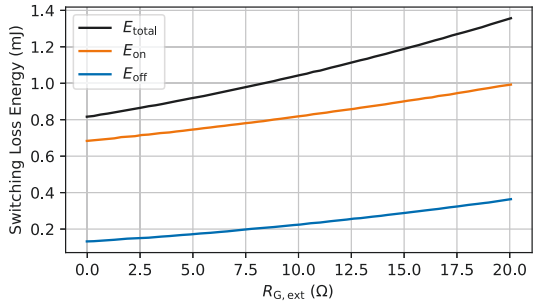


FIGURE 2.12. Switching loss energy for varying $R_{G,ext} = 0\,\Omega \ldots 20\,\Omega$, but constant $V_{DC} = 800\,V$, $I_{load} = 20\,A$,and $T_j = 25\,°C$. Data from Wolfspeed C3M0075120D SiC power MOSFET datasheet [7].

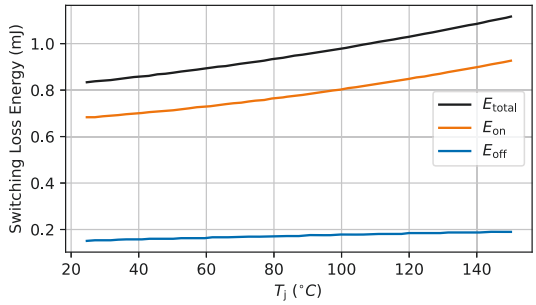


FIGURE 2.13. Switching loss energy for varying $T_j = 25\,°C \ldots 150\,°C$, but constant $V_{DC} = 800\,V$, $I_{load} = 20\,A$and $R_{G,ext} = 0\,\Omega$. Data from Wolfspeed C3M0075120D SiC power MOSFET datasheet [7].

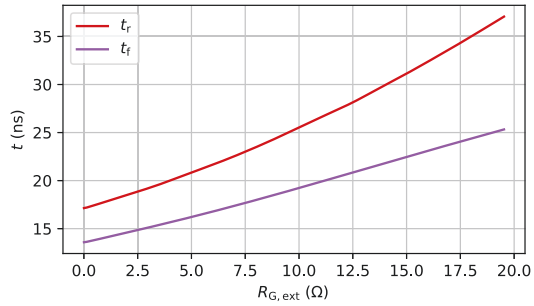


FIGURE 2.14. Voltage transition times at turn-on (t_r) and turn-off (t_f) for varying $R_{G,ext} = 0\,\Omega \ldots 20\,\Omega$, but constant $V_{DC} = 800\,V$, $I_{load} = 20\,A$, and $T_j = 25\,°C$. Data from Wolfspeed C3M0075120D SiC power MOSFET datasheet [7].

2.5.1 The Two Voltage Level Conventional Gate Driver

Conventionally, MOSFETs have been used with level shifters that convert the logic control signal into the required values of V_{gs}. This gate driver type is referred to as Two Level Voltage Source Gate Driver (VSGD). A typical Two Level VSGD consists of a totem pole configuration of an N-type and a P-type MOSFET, driven by a low-power gate driver. A schematic diagram can be seen in Figure 2.10. This low-power gate driver translates the logic control signal into a gate signal for the totem pole circuit, which provides the power MOSFET with the required current to charge it up to $V_{GG,high}$ and discharge it down to $V_{GG,low}$.

The values of $V_{GG,high}$ and $V_{GG,low}$ depend on the individual MOSFET model as well as the desired conduction or blocking properties. The dynamics of switching are determined by a resistor, $R_{G,ext}$ connected between the gate driver output and the MOSFET input. In choosing $R_{G,ext}$, the C_{gs} charging and discharging processes are adjusted to meet external specifications. For example, dv/dt values might be restricted by the passive components of the converter or the load. The choice of $R_{G,ext}$ must then take the entire range of possible converter operating conditions in terms of DC voltage and load current into account to ensure the application requirements are met. Since the dynamics differ between the turn-off and turn-on switching transitions, a second resistor is used with a series connected diode to influence only one of the two transitions.

The influence of changing operating conditions, i.e. DC voltage and load current, but also the device temperature on the switching behavior of SiC power MOSFETs is significant. To illustrate this, switching loss values under variation of the various test parameters were extracted from the datasheet of a C3M0075120D SiC power MOSFET from Wolfspeed. In Figure 2.11, the DC voltage (V_{DC}) and load current (I_{load}) are varied. An increase in either of V_{DC} or I_{load} is reflected in an increase in both switching loss at turn-on and turn-off. Figure 2.12 depicts the switching loss energy under variation of the external gate resistor ($R_{G,ext}$). An increase in gate resistance results in an increase in both switching loss at turn-on and turn-off. Figure 2.13 illustrates the impact of the junction temperature (T_j) on the switching losses. As with the previously mentioned condition parameters, a higher junction temperature results in a higher switching loss energy at both turn-on and turn-off. The graphs emphasize how many factors have a significant and complex influence on the switching losses, if the SiC power MOSFET is driven by a conventional Two Level VSGD.

Data sheets provided by the manufacturer do not give information about the dv/dt during switching in the same detail as for switching losses. Figure

2.14 depicts the voltage fall time at turn-on (t_r) and the voltage rise time at turn-off (t_f) under fixed DC voltage and load current but variation of $R_{G,ext}$. The average dv/dt rates, being inversely proportional to t_r (turn-on) and t_f (turn-off) respectively, show a similar extent of variation as the switching losses shown in Figure 2.14. It is therefore reasonable to expect a large variation in dv/dt with respect to the DC voltage, the load current, and the device temperature as well. That this is a reasonable assumption will be shown in Chapter 4 by means of experimental results.

The variation of switching transients with changing DC voltage and load current presents a major caveat of Two Level VSGDs. To meet external requirements on the switching dynamics, for example regarding a switching loss or a dv/dt requirement, the worst-case operating conditions need to be accommodated since no adjustments can be made during operation. As a consequence, in non-worst-case operating conditions, the switching performance is slower than allowable, which leads to higher losses than necessary and, thereby, worse converter efficiency than possible.

2.5.2 *Active Gate Drivers for SiC Power MOSFETs*

As opposed to Two Level VSGDs, Active Gate Drivers (AGDs) are reconfigurable at converter run time. The most basic principle that all AGD concepts have in common, is the ability to manipulate the gate charging process by altering the gate driver configuration. By changing the speed and the outline of the gate charging process, AGDs enable control of the switching transients in regard to the transition slew rates and, as a consequence, the switching losses. Especially taking the large variation with operating conditions such as DC voltage and load current into account, adapting the switching behavior of SiC power MOSFETs to these changing operating conditions can be used to achieve a variety of objectives. For example, the objective may be loss stabilization for Active Temperature Control, or efficiency optimization by switching speed maximization in keeping with maximum switching speed limitations imposed by external requirements.

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Part II

Research Work

Organization of Part II - Research Work

The chapters in this part of the thesis give an overview of the research work that has been conducted on the main topic of this thesis, being the "Dynamic Characterization, Evaluation and Control of Active Gate Drivers for Silicon Carbide Power MOSFETs". The following line of thought is followed during this presentation.

The aim of Active Gate Driver (AGD) evaluation is to characterize the behavior of AGD driven Silicon Carbide (SiC) power MOSFET, and subsequently determine the potential improvements that can be expected from integrating such an AGD. The behavioral characterization presupposes that reliable measurements of the AGD and SiC power MOSFET in question can be obtained. Such measurements can only be made with a highly accurate characterization test setup. Therefore, Chapter 3 focuses on the accurate dynamic characterization of SiC power MOSFET and AGDs in two steps: First, high-power high-bandwidth current sensors are investigated in both a small- and a large-signal analysis in Section 3.1, giving deeper insight into the properties of such current sensors. This investigation concludes with an informed decision on a specific current sensor that provides highly accurate measurements for the purpose of dynamic characterization of SiC power MOSFETs and AGDs. Second, the design and implementation of a Low-Inductive Test Platform (LITP) is presented in Section 3.2. Enacting low-inductive and measurement-oriented design principles, this test circuit enables the characterization of SiC power MOSFETs driven by conventional or active gate drivers. Chapter 3 addresses Objective 1 of this thesis as defined in Section 1.2, i.e. to create a test platform for dynamic discrete SiC power MOSFET and AGD characterization.

Being equipped with this necessary prerequisite, application, design and implementation, and evaluation aspects of AGDs for SiC power MOSFETs are discussed among two exemplary AGDs in Chapter 4. First, a Four Level Multilevel Voltage Source Gate Driver (MLVSGD) for switching loss and slope control is examined in Section 4.1. Second, a Three Level MLVSGD that can be used for overvoltage suppression at inductive turn-off of a SiC power MOSFET in synchronous rectification mode is investigated in Section 4.2. Chapter 4 applies to Objective 2 as defined in Section 1.2, i.e. addressing aspects of design, implementation, and evaluation of AGDs for fast switching SiC power MOSFETs.

The final objective of this thesis is the development of a wireless interface suitable for AGD control applications, as defined in Section 1.2. Therefore, Chapter 5 focuses on how AGDs can be supplied with control information to realize their improvement potential. In particular, wireless control of AGDs is examined in Section 5.1, proposing a taxonomy for information transmission in Power Electronics Systems (PES). Using the proposed taxonomy, both the merit and the feasibility of using Wireless Communication Technologies (WCTs) for the information transmission between converter and AGD control units is assessed. Subsequently, Bluetooth Low Energy (BLE) technology is used to successfully control the previously presented four voltage level AGD, and thereby prove the accuracy of the previously derived WCT assessment. With this, Chapter 5 deals with Objective 3 as defined in Section 1.2, i.e. to develop a wireless control interface for AGD applications.

Chapter 3

Accurate Dynamic Characterization of Silicon Carbide power MOSFETs and Gate Drivers

As explained in the introduction, Active Gate Drivers (AGDs) can be used to control the dynamic and static behavior of Silicon Carbide (SiC) power MOSFETs. To investigate the improvements that can be expected from using a specific AGD, characterization experiments with both the SiC power MOSFET and the AGD are required. In addition, characterization data can be used to adjust simulations models for more realistic and reliable simulation data that can be used for faster prototyping and converter design. Therefore, this chapter focuses on the accurate dynamic characterization of SiC power MOSFETs and AGDs, and addresses Objective 1 of the PhD project. This objective is the design, implementation and verification of a test platform for the dynamic characterization of fast-switching discrete SiC power MOSFETs and AGDs. The associated contributions are the proposal of a two-step method for evaluating the performance of high-power, high-bandwidth current sensors, as well as the design, implementation and verification of a Low-Inductive Test Platform (LITP) for devices in a TO-247 package.

To accurately capture the fast switching transients of SiC power MOSFETs is a challenge for measurement technologies available today. Hence, the design and implementation of the LITP required a preceding investigation of suitable measurement components as part of the test circuit. Especially the high bandwidth measurement of large currents presents an issue and was therefore investigated in depth in publication [J1]. This publication is summarized in Section 3.1. The publication shows that a coaxial Current Viewing Resistor (CVR) is suitable for accurately measuring the fast switching device currents of SiC power MOSFETs. Subsequently, publication [J2] presents the LITP, a circuit suited for high-accuracy dynamic characterization of fast-switching discrete SiC power MOSFETs and AGDs. This circuit uses the current sensor identified in publication [J1], low-inductive design principles, and high-accuracy probing to produce switching waveforms that accurately reflect the switching device characteristics with a similar performance as a commercial reference setup. Section 3.2 summarizes the parts of publication [J2] in fulfillment of Objective 1 of the PhD project. Section 3.1 and Section 3.2 each comprise a brief intro-

duction, a description of the problem that is to be solved, the applied methods, as well as the results of the applied methods. Finally, an essence of the paper's conclusion is given, as well as the specific contributions as a bullet-point list.

3.1 High-Bandwidth Measurement of Large Currents

The fast switching transients of SiC power MOSFETs are a challenge for acquiring accurate measurements with sensors available on the market. Especially the available current sensors are limited in this regard. In this work, current sensor requirements were formulated and the most common current sensing principles were presented. Subsequently, a two-step characterization method for high-amplitude, high-bandwidth current sensors was developed. First, the small-signal response of the sensor under test was determined with a Vector Network Analyzer (VNA), and then, its high-amplitude behavior was examined when conducting a dynamic characterization Double Pulse Test (DPT) experiment. This DPT experiment is conducted with a Two Level Voltage Source Gate Driver (VSGD) to achieve the fastest possible switching transients as an excitation signal with a broad frequency spectrum and high amplitudes simultaneously. A selection of four commercially available current sensors were investigated with the above-mentioned two-step characterization method, and put into comparison with each other. The value of this study lies in the practicality of the current sensor environment that is close to the desired application.

3.1.1 Problem Description

Voltage and current rise times of SiC power MOSFETs are in the range of 10 ns [1] in the case of discrete devices and 50 ns [2] in the case of power modules. Especially current sensors fall behind the requirements posed by fast switching SiC MOSFETs. For power test circuits operating at high currents, suitable sensors must offer:

- High Maximum Measured Current: SiC power MOSFETs can carry high currents that breach the limits of some available current sensors. A suitable sensor must be rated to withstand the large current amplitude for the duration of the current in the given application. The exact limitation depends on both the applied test method and the current sensor, as discussed in [J1].
- High Bandwidth: To achieve a measurement error below 2 %, the measurement system bandwidth must exceed the bandwidth of the measured signal by at least 5 times [3; 4]. The signal bandwidth equals

$BW_{\text{sig}} = \frac{0.35}{t_{\text{rise|fall}}}$ in good approximation [3; 4]. With current rise and fall times of approximately 10 ns, this results in a measurement system bandwidth requirement of $BW_{\text{meas}} \geq 175\,\text{MHz}$. However, switching transition speed is not the sole interest in dynamic characterization. In the past, the snappy turn-off behavior of antiparallel diodes in Insulated-Gate Bipolar Transistor (IGBT) modules could cause oscillations at frequencies beyond 100 MHz [5]. As the parasitic device capacitances are considerably reduced in SiC MOSFETs compared to Si IGBTs, and because the layout of SiC MOSFET power modules has been optimized for lower parasitic inductance as well, even higher oscillation frequencies can be expected. This emphasizes the interest in yet higher measurement bandwidths for accurate characterization, but potentially also for diagnostics in a converter.

- High Flatness: The switched current of SiC power MOSFETs contains a broad frequency spectrum due to the fast switching transitions. For the simplest possible measurement evaluation, a constant transmission coefficient, in which all frequency components at the input are equally represented at the output, is desirable. However, real sensors distort the input signal. How close the sensor transmission behavior is to being a constant factor is referred to as flatness. Flatness can only be achieved in a limited frequency region.

- High Linearity: In reality, the frequency dependent transmission behavior of current sensors varies with a varying amplitude of the measured current. If at all possible, nonlinear distortion is challenging to compensate. Hence, nonlinear distortion must be negligible for accurate dynamic current measurement purposes.

- Low Insertion Impedance: At fast switching speeds, parasitic inductances exhibit a significant inductive voltage drop, which distorts the characterization results as it does not originate from the device that is to be characterized. As will be discussed later, in power circuits incorporating fast switching SiC power MOSFETs, significant efforts are spent on reducing the test circuit layout to reduce this effect, and this includes the choice of a current sensor with a small insertion impedance.

In current sensor datasheets, the sole indicators of the sensor behavior are often only one scalar value for the sensitivity and the bandwidth each. However, neither the flatness of the sensor sensitivity, i.e. the frequency dependent deviation of the sensor transmission behavior from a constant gain, nor the effects of high amplitude signals on the sensor behavior are specified. Moreover, the insertion impedance is often not included in the datasheet either.

TABLE 3.1. Current sensors subject to the proposed two-step characterization method

Sensor type	Specific model
Rogowski Coil	PEM CWTUM miniHF
Coaxial CVR	T&M Research SDN-414-025
SMD CVR	Bourns CSS4J-4026R-1L00x
Clamp-on Current Probe	Tektronix TCP0030A

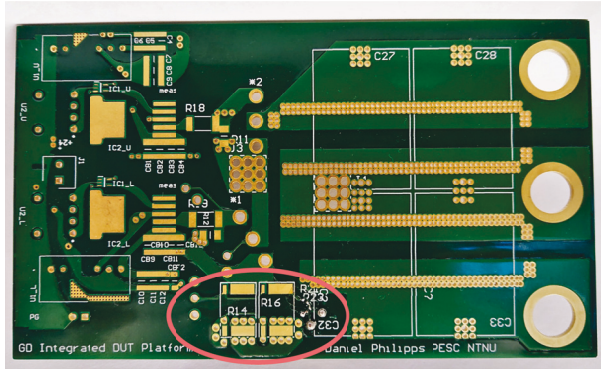


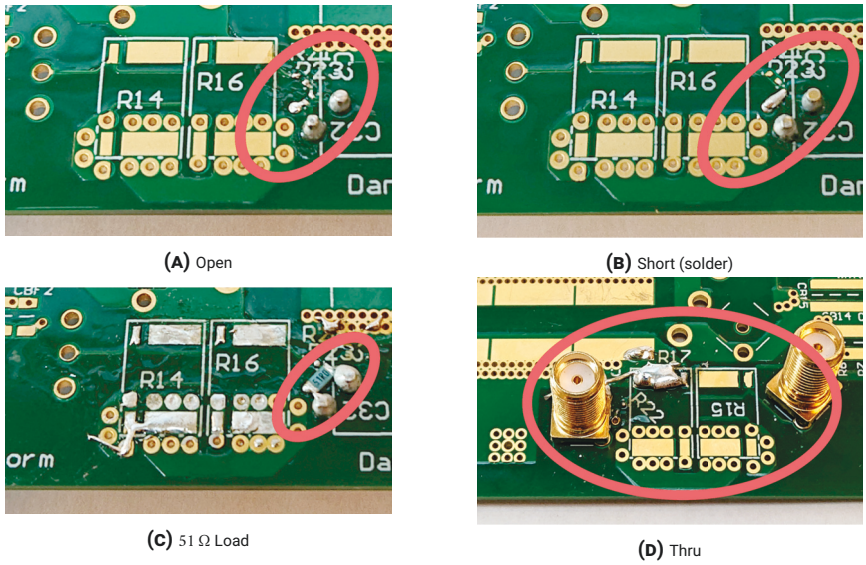
FIGURE 3.1. Low-Inductive Test Platform (LITP) Printed Circuit Board (PCB) without components. Current sensor Surface Mount Device (SMD) pads with injection network (right, SMA connector on the bottom side) in red ellipsoid.

3.1.2 Two-Step Current Sensor Characterization Procedure

To identify suitable current sensors for a range of applications involving fast-switching SiC power MOSFETs, a two-step method for the performance evaluation of current sensors is proposed in this work. The focus is on dynamic SiC power MOSFET characterization, and thus, the previously defined current sensor requirements are used as a basis for the following assessment. The proposed current sensor evaluation method characterizes the linearity, the bandwidth and the effects of the insertion impedance in two separate experiments. Multiple sensors are characterized in this work, namely:

- A Rogowski coil current sensor with integrator,
- A coaxial CVR,
- A Surface Mount Device (SMD) CVR, and
- A clamp-on current probe (in large-signal tests exclusively).

The specific sensors are listed in Table 3.1.



(A) Open (B) Short (solder)

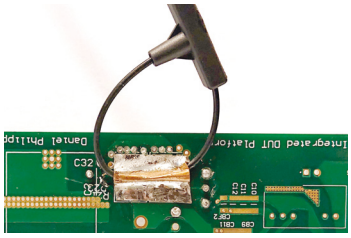
(C) 51 Ω Load (D) Thru

FIGURE 3.2. Calibration fixture detail photos. The region displayed equals roughly the area enclosed by the red ellipsoid in Figure 3.1.

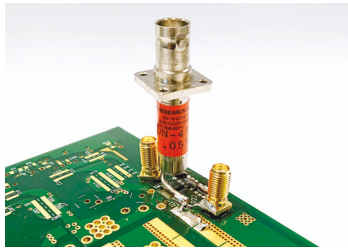
Test Fixture

The test fixture, a Low-Inductive Test Platform (LITP), was designed in earlier work [C6]. This circuit was demonstrated for accurate dynamic characterization of SiC power MOSFETs in a TO-247-3 package. The LITP Printed Circuit Board (PCB) features pads that connect to all current sensors under investigation, and coaxial SMA connectors for signal injection through a pi impedance network and for signal extraction as well [C6]. A photo of the LITP PCB can be seen in Figure 3.1.

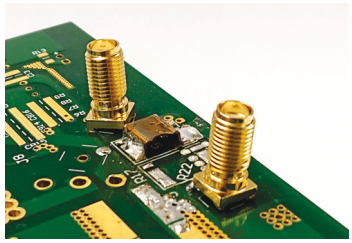
VNA calibration fixtures (open, short, load, thru) are required to correct for the impact of connectors and cables that lead to and from the test fixture. For this purpose, the test fixture features an impedance network with 0403-size SMD components for optimal high frequency behavior, that can be freely configured to represent the required calibration fixture terminations (open, short, load, thru). Using another very high-precision VNA, the calibration fixtures underwent an impedance analysis, resulting in the required equivalent impedance model for the VNA calibration procedure. A detail picture of each calibration fixture is depicted in Figure 3.2. Pictures of all current sensors connected to the test fixture are depicted in Figure 3.3.



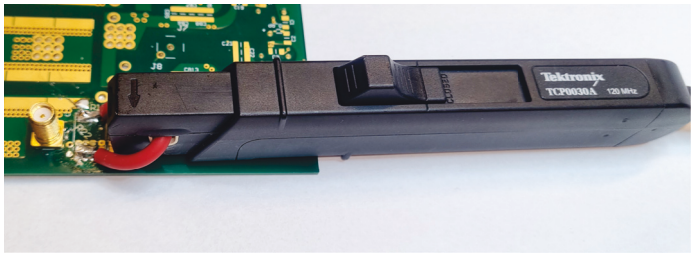
(A) LITP with CWTUM miniHF on top layer



(B) LITP with SDN-414-05 coaxial CVR on bottom layer



(C) LITP with SMD CVR on bottom layer



(D) LITP with TCP0030A current clamp on bottom layer

Figure 3.3. Current sensors mounted on top or bottom layer of LITP

Small-Signal Analysis

VNAs measure the scattering parameters (S parameters) of any two port system. S-parameters describe the linear power flow within such systems. VNAs determine these parameters by injecting a single but variable frequency signal into one port and measuring the signal at the other port. The measurement is restricted to the input signal frequency. Hence, nonlinear distortion that leads to output signal components of frequencies not present at the input cannot be detected.

In the case of a current sensor, the first port is the primary sensor side. Here, the signal coming from the VNA is converted into a current by means of a 47 Ω resistor that is connected in series with the primary sensor side, which is inserted into the commutation loop of the characterization setup.

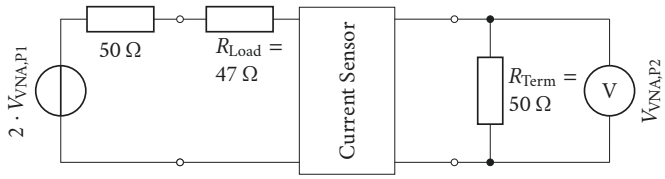


Figure 3.4. Idealized schematic diagram of the experimental VNA setup for transmission coefficient analysis

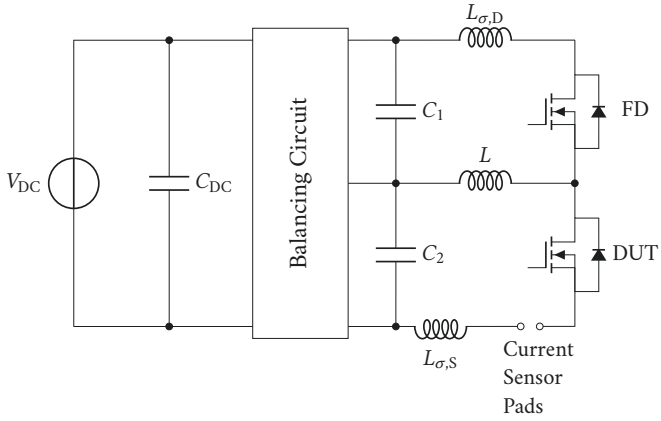


Figure 3.5. Idealized schematic diagram of the experimental VNA setup for transmission coefficient analysis

The secondary sensor side, where the measurement system attached, is the second system port and therefore connected to the receiving VNA port. The S21 parameter describes the transmission coefficient and therefore contains information about the flatness and the bandwidth of the current sensor under investigation with a small-signal input. A schematic circuit diagram of this test setup is shown in Figure 3.4.

Large-Signal Analysis

While the small-signal analysis is a repeatable and very precise method to determine the frequency domain current sensor transmission behavior, amplitude-dependent and nonlinear effects are not detectable in this analysis. Therefore, the small-signal current sensor transmission coefficient analysis is not sufficient to assess the suitability of a current sensor for the purpose of dynamic SiC power MOSFET and AGD characterization. Instead, large-signal tests must be conducted in addition. Hence, DPTs were conducted with each of the current sensors in this work, at a test voltage of 800 V and a test current of 27 A. The measurement results are inspected in both the time and the frequency domain by applying a Fast Fourier Transform (FFT) to the time domain results. To determine the insertion effect of the current sensors, the CWTUM miniHF3

Rogowski Coil was used to measure the switched current together with all other current sensors. Despite the deficiencies of this sensor, i.e. mainly the limited sensor bandwidth, it is an adequate choice for this purpose because it does not have any significant insertion impedance itself and is therefore expected to have only limited influence on the measured current. A schematic circuit diagram of the experimental setup employing DPTs [C6] is shown in Figure 3.5.

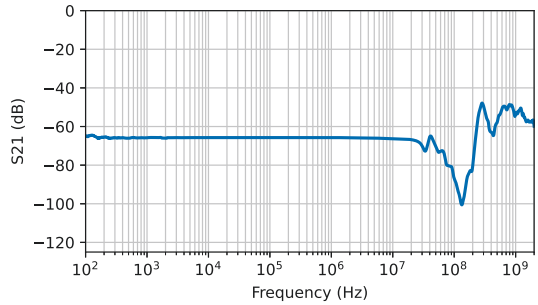
3.1.3 Results

The analysis showed that the proposed two-step current sensor characterization method can be used to effectively determine the suitability of various current sensor approaches for the purpose of dynamic SiC power MOSFET and AGD characterization.

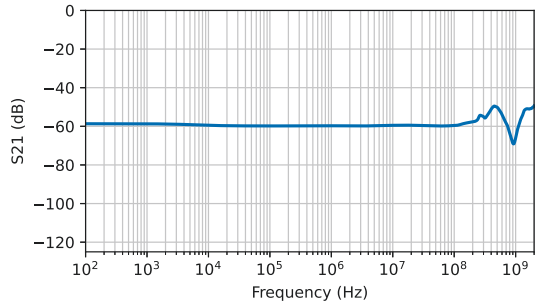
Small-Signal Analysis

The measurement results from the small-signal transmission coefficient analysis are depicted in Figure 3.6. The following outcomes are especially noteworthy:

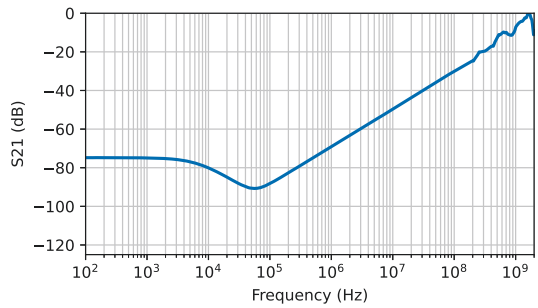
- Despite adhering to the specification, the commercial sensors under investigation show significant deviations from a flat transmission behavior.
- The measurement results obtained from the commercial CWTUM miniHF3 Rogowski coil current sensor are shown in Figure 3.6a. Additional low-pass filtering is strictly recommended for two reasons. First, a significant propagation of very high frequencies far above the bandwidth specification of this sensor was observed. Second, judging by the transmission behavior, it is assumed that the bandwidth limitation of this sensor originates from an internal resonance within the sensor coil. Both of these aspects translate into a falsifying influence on signals above a frequency of 30 MHz, which, therefore, should be suppressed with a suitable filter.
- The coaxial CVR measurement results are depicted in Figure 3.6b. This sensor exhibited the flattest and least bandwidth-limited transmission behavior among all current sensors. However, the elevation of signals with frequencies between 300 MHz and 500 MHz has to be potentially taken into account. Furthermore, the specified bandwidth limit of 2 GHz could not be reproduced in the experiments without accepting the significantly frequency-dependent transmission behavior above 800 MHz.



(A) CWTUM miniHF 3 Rogowski Coil



(B) SDN-414-05 Coaxial CVR



(C) Bourns CSS4J-4026R-1L00x SMD CVR (1 mΩ)

Figure 3.6. S21 Transmission coefficients of the current sensors under investigation

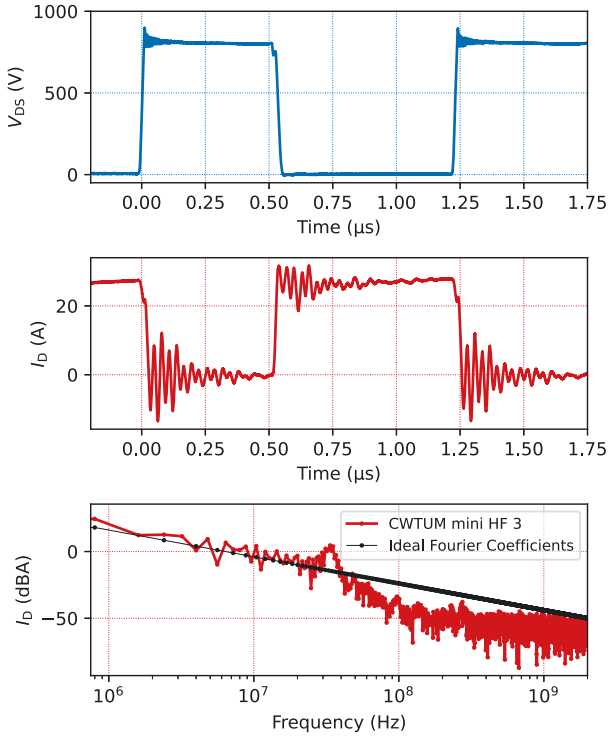


Figure 3.7. CWTUM miniHF 3 Rogowski Coil power measurements reference

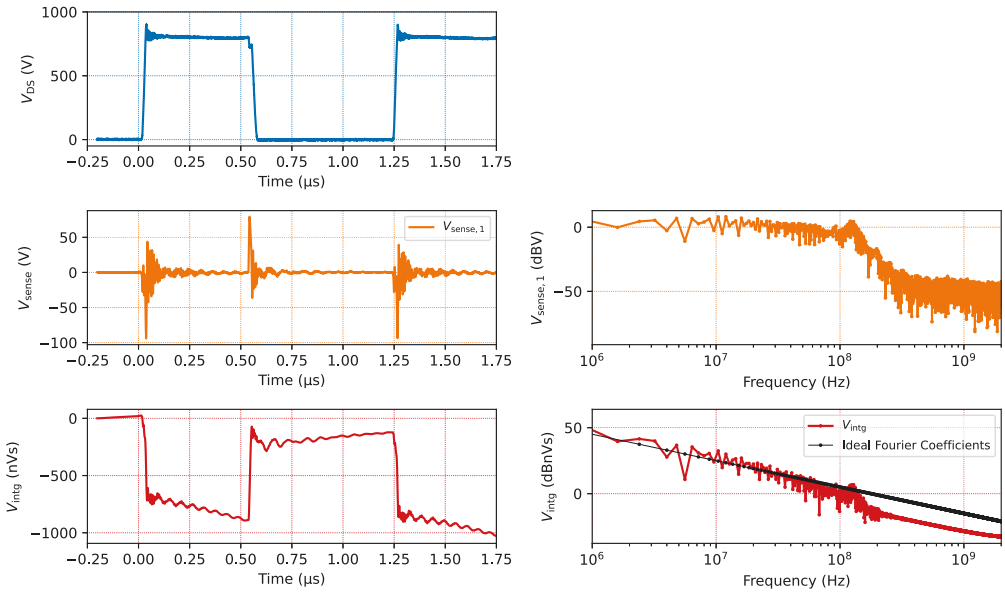


FIGURE 3.8. Bourns CSS4J-4026R-1L00x SMD CVR Power Measurements

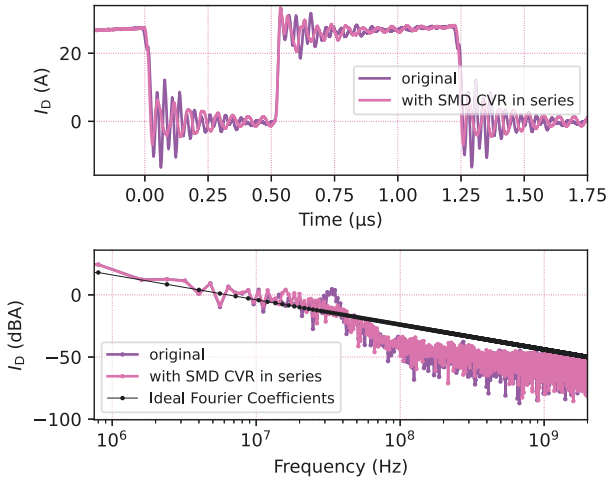


FIGURE 3.9. Bourns CSS4J-4026R-1L00x SMD CVR insertion effect on power measurements with CWTUM miniHF 3 Rogowski Coil

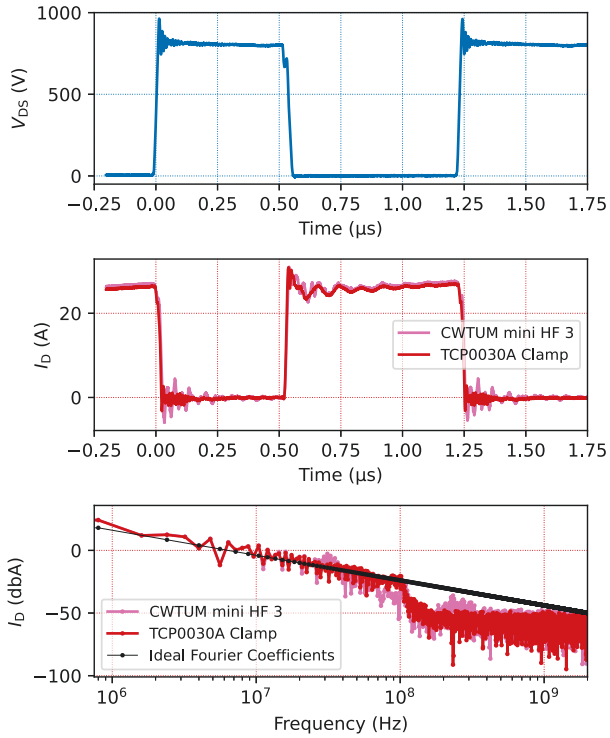


Figure 3.10. TCP0030A current probe power measurements

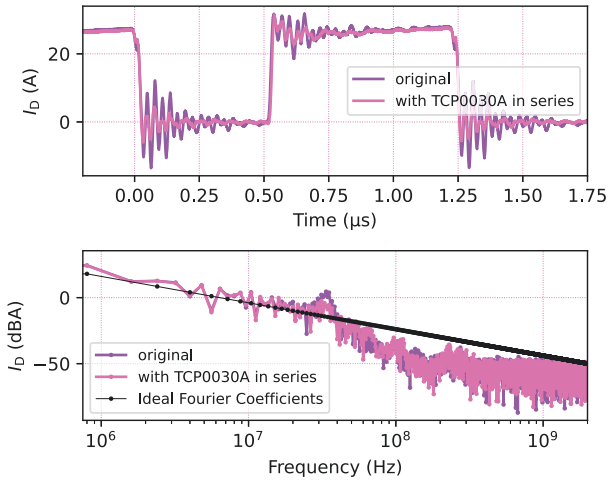


Figure 3.11. TCP0030A current probe insertion effect on power measurements with CWTUM miniHF 3 Rogowski Coil

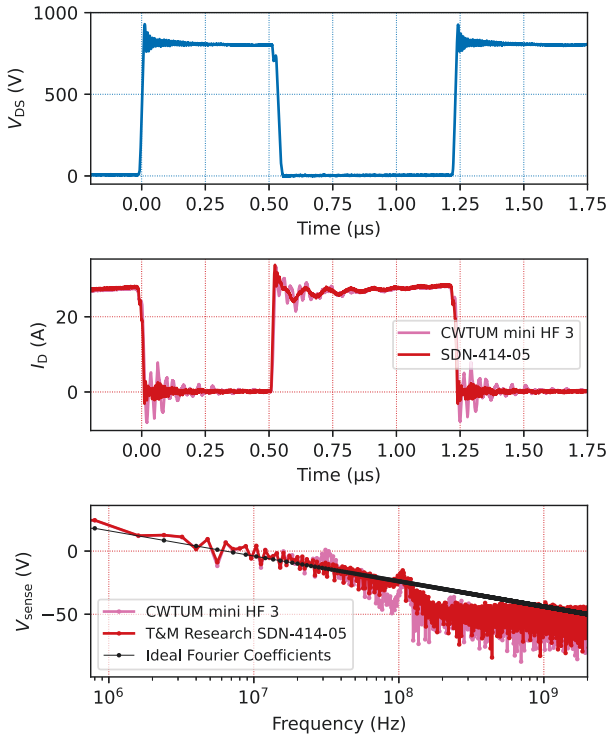


FIGURE 3.12. SDN-414-05 Coaxial CVR power measurements

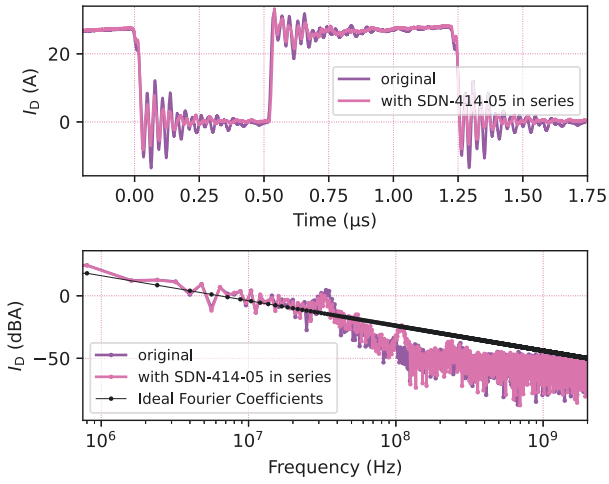


FIGURE 3.13. SDN-414-05 Coaxial CVR insertion effect on power measurements with CWTUM miniHF 3 Rogowski Coil

Partly, this is assumed to result from inserting the sensor into the practical test fixture environment, which is the usual application scenario of a current sensor. This is an important aspect to consider in the application of current sensors: The sensor environment has a significant impact on the sensor characteristics.

- Lastly, the SMD CVR behavior strongly varies with input signal frequency. This results in multiple regions, as can be seen in Figure 3.6c. Elaborated filter designs would be necessary for successfully integrating this sensor for high-bandwidth current measurement. Moreover, as this sensor has a very strongly differentiating behavior for frequencies beyond 100 kHz, high voltage peaks were expected with the large current transition rates observed with fast switching SiC power MOSFETs.

Large-Signal Analysis

The time domain measurements and frequency domain transforms of the DPT experiments are shown in Figure 3.7 to Figure 3.11. The outcomes of this large-signal analysis are:

- The large-signal measurements conducted with the Rogowski coil alone (Figure 3.7) and with all other sensors confirmed the hypothesis that it has a self-resonance between 30 MHz and 40 MHz, close to the specified bandwidth. Significant oscillations with this frequency were measured throughout the experiments, and were not confirmed by any other sensor. Hence, for a practical application, a low-pass filter with a steep roll-off before 35 MHz is necessary to produce reliable measurement results, which effectively limits the usability of this sensor for the characterization of fast switching SiC power MOSFETs.

- The strongly frequency dependent transmission behavior of the SMD CVR can be seen in Figure 3.8. This impedes a direct interpretation of the measured signal and emphasizes the need for elaborate filtering. As expected, the large inductive component of its insertion impedance leads to very high voltages during switching, which might be destructive for cascaded filter hardware. Integrating the signal output (as the inductive behavior has an amplifying effect on the current-derivative) leads to interesting results that are described more in detail in [J1]. However, the persisting sampling hardware offset leads to an unreadable measurement result as a consequence. Comparing the Rogowski coil measurements with and without the SMD CVR in the circuit reveals that the insertion of this current sensor leads to damping of some oscillations, especially

around the main oscillatory mode of the Rogowski Coil. This is best observed in the FFT of the current measurements in Figure 3.9.

- The current clamp has a very flat transmission behavior. The bandwidth limit of the current probe at approximately 120 MHz can be confirmed looking at the FFT of the measurement data in Figure 3.10 and high frequency components are well-represented with little evidence for any strong internal resonance. However, the insertion impedance of this sensor had a significant damping effect on oscillations, which emphasizes the resistive character of the current clamp insertion impedance. This can be observed in Figure 3.11. In addition, the inductive voltage drop at turn-on and the voltage overshoot at turn-off proved that the inductive insertion impedance component is significant.

- As seen in Figure 3.12, the coaxial CVR offers the highest measurement bandwidth and mostly flat transmission behavior that is in good agreement with the current clamp measurements. The resistive insertion impedance component of this sensor lead to a slight damping of oscillations observed in the Rogowski coil output, as can be observed in Figure 3.13. The inductive insertion impedance component leads to a slight increase in both overshoot voltage at turn-off and voltage drop at turn-on.

3.1.4 Conclusion

A two-step analysis of high-power, high-bandwidth current sensors was used to effectively determine the most suitable candidate for the high accuracy characterization of SiC power MOSFETs and AGDs, which is a coaxial CVR. This sensor exhibits the highest bandwidth and flatnesss among the examined sensors. Moreover, the coaxial CVR does not exhibit notable non-linearity in large-signal experiments. It is therefore estimated to represent the measured current most accurately. The insertion impedance of this sensor does have an impact on the measured current. However, considering the studied alternatives and the fact that similar sensors are used in commercial characterization circuits, it is found to be the best current sensor alternative for this purpose. [J1] also presents a table listing various other application scenarios involving fast-switching SiC power MOSFETs and recommends at least one of the investigated current sensors for each application scenario (Table 7.2).

3.1.5 Contribution

The contributions of this work are listed in the following.

1. Current sensors of different types were analyzed in a comparative and practical setting. Challenges that occur using each of the technologies in an environment with high currents and simultaneously fast switching speeds were identified.

2. The proposed two-step current sensor characterization method enables the holistic characterization of the current sensor behavior in a practical circuit from two different and complementary vantage points. A small-signal analysis was used to investigate flatness and bandwidth with a low signal amplitude. The subsequent double-pulse tests verified the transferability of the small-signal analysis result to high power switched current measurements that potentially provoke nonlinear effects.

3. Based on the results of the proposed two-step current sensor characterization method, a sensor selection guide for various applications was derived.

3.2 Low-Inductive Circuit for Flexible Dynamic SiC power MOSFET and AGD Characterization

Having identified the Coaxial CVR as a suitable current sensor for the dynamic characterization of discrete SiC power MOSFET and AGDs, a test circuit was developed for accurately capturing the fast switching transitions of discrete SiC MOSFETs. [J2] documents the development of a test circuit that is later used for

- Dynamic characterization of discrete SiC power MOSFETs in a TO-247-3 package, and
- Verifying the potential of an AGD to manipulate the switching behavior of a SiC power MOSFET in a TO-247-3 package.

The design goals derived to realize these purposes include a low commutation loop inductance and a circuit topology allowing for both hard-switching and soft-switching, i.e. reverse current, DPT experiments. Furthermore, connecting the SiC power MOSFET and the gate driver should be quick and simple. It must neither affect the mechanical integrity of the device or the test circuit, nor degrade the conduction performance significantly because of the added contact resistance. The circuit layout was presented in the publication [J2]. In addition,

a parameter extraction software was implemented. The results of the LITP are compared in depth with a commercial reference test setup that also serves the purpose of dynamic characterization of discrete SiC power MOSFETs in a TO-247-3 package, the PD1500A by Keysight. The self-programmed parameter extraction software was verified with data from this dynamic power device characterizer. DPT experiments were conducted on both setups and then put into comparison. The LITP exhibits comparable performance to the PD1500A power device characterizer. In addition, the LITP was demonstrated to support soft-switching tests.

3.2.1 Problem Description

Many DPT test setups were presented in literature [6–10]. However, these often have shortcomings, such as:

- A high commutation loop inductance. This impedes the use with fast switching SiC power MOSFETs.
- Missing soft-switching capability. Only few test circuits allow testing under soft-switching, i.e. reverse current, conditions.
- Inflexible connection of Devices Under Test (DUTs). The DUTs must usually be soldered to the test circuit, which makes evaluating numerous devices, for example to identify the parameter spread between devices of the same type, time-consuming and strenuous for the characterization circuit.
- Missing information about gate drivers. Seldom, the gate driver itself and its connection to the test circuit is described.

The proposed LITP aims at solving these issues. In particular, the design goals were:

1. A suitable circuit topology for both hard-switching tests and soft-switching tests, i.e. reverse current switching, DPT experiments.
2. Low inductance in the commutation loop. Only with a low parasitic inductance in the commutation loop, the switching behavior is actually determined by the switching device, and not influenced by the circuitry around.
3. Measurement terminals, enabling high-accuracy current and voltage measurements.

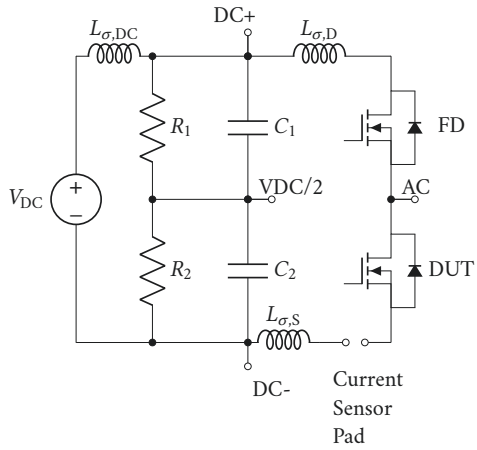


FIGURE 3.14. Idealized schematic diagram of the Low-Inductive Test Platform (LITP)

4. Quick connection and disconnection of Devices Under Test (DUTs), i.e. SiC power MOSFETs in a TO-247-3 package. This allows for testing multiple devices without the need for soldering and thereby avoids damage to the DUTs and the test circuit

5. Flexible and low-impedance connection of gate drivers. This enables the efficient evaluation of different gate driver circuits, including both conventional Two Level VSGDs and AGDs.

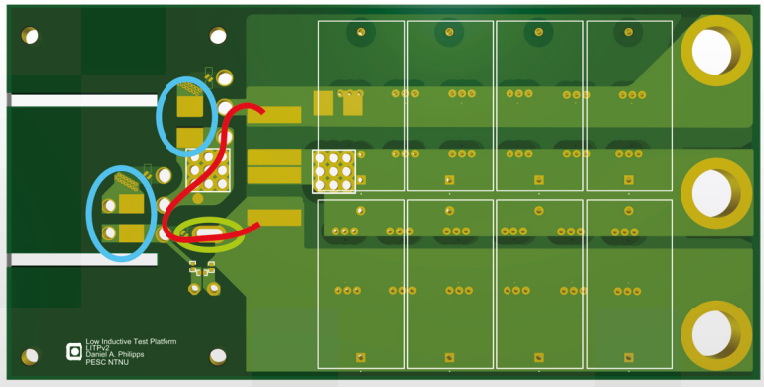
3.2.2 Low-Inductive Test Platform Design and Evaluation

To achieve the design goals, the following measures were enacted:

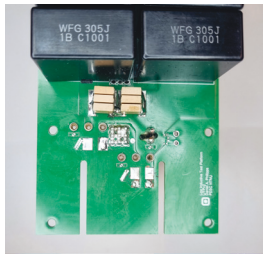
1. The test circuit consists of a half-bridge circuit, in which the lower device is the DUT. A schematic circuit diagram of the circuit is shown in Figure 3.14. The energy for the test is stored in two series-connected capacitor banks with an accessible midpoint. By connecting the test inductor to this terminal instead of the positive supply voltage terminal as it is the case in classic DPT setups, characterization tests can be conducted with a reversed load current, and therefore, a zero-voltage switching transition.

2. The commutation loop inductance was reduced by

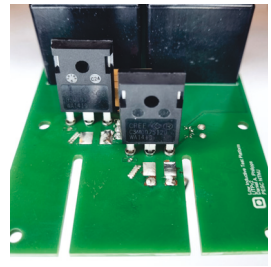
    - Including a sufficiently large capacitive energy storage. Ceramic and foil capacitors were combined to achieve effective filtering and energy storage as close as possible to the switching devices.



(A) Top side CAD view. Markings: Optimized current commutation path (red), current sensor port (light green), and gate pads (blue).



(B) Top front side without DUTs.



(C) Top front side with DUTs.

(D) Bottom from the side without DUTs. Left to right: Coaxial Gate-Source voltage probing point (green), Drain-Source voltage probing point (PCB pin receptacles, blue), coaxial CVR (red).

(E) Side view with DUTs.

Figure 3.15. Low-Inductive Test Platform (LITP) from various angles

- Maximizing the overlap of the PCB layers that supply the DC voltage, and thereby minimizing the path inductance to the switching devices, and
- Circuit miniaturization through track length minimization to further reduce the path inductance to the switching devices.

The resulting commutation loop inductance of approximately 30.7 nH, whereof the PCB layout contributes approximately 15.4 nH, is acceptably low taking into account that the inductance introduced by the TO-247-3 package lead inductances account for up to 9 nH [11].

3. For the gate-source voltage measurement, a coaxial SMA measurement terminal was introduced. The drain-source voltage probe is connected to two pin receptors, one each for the probe tip and the ground spring connector. For the switch current measurement, a universal pad was introduced that can connect to a current sensor of choice. Furthermore, a coaxial port for signal injection is located near the universal current sensor pad and can be connected using a pi-network of 0403-size SMD resistors. This injection port can be used for current sensor characterization as proposed in Chapter 7, but also for deskewing the current sensors. Deskewing is the horizontal alignment of all measurements taken for an experiment. This corrects for varying delay times among different sensor and probe types. This is especially important for the characterization of fast switching SiC power MOSFETs, where only small misalignment can have a significant impact on the extracted parameters.

4. Suitable pin receptacles with a diameter of 1 mm were used as DUT connection terminals, allowing for quick and damage-free exchange of DUTs while the introduced contact resistance is shown to be only marginally larger than that of a solder joint.

5. Exchanging the gate driver is easy and quick because of the universal gate driver pads that are located very close to the switching device on the LITP. This facilitates testing multiple different, and also custom gate drivers, including AGDs.

Figure 3.15 contains photos of the LITP in different configurations. Views of all PCB layers can be found in the publication [J2] for more detailed information on the exact circuit layout.

The LITP was evaluated in five steps:

1. The IEC 60747-8 compliant custom parameter extraction software was verified against parameter extraction results obtained with the PD1500A

Table 3.2. di/dt, voltage drop at turn-on, and corresponding commutation loop inductance estimates for both LITP and PD1500A experiments at two different test currents (I_{Test}) and a fixed $V_{\text{Test}} = 800\,\text{V}$

I_{Test}	$V_{\text{drop,LITP}}$	$V_{\text{drop,PD1500A}}$	di/dt_{LITP}	di/dt_{PD1500A}	$L_{\sigma,\text{LITP}}$	$L_{\sigma,\text{PD1500A}}$
15 A	28.0 V	39.6 V	0.940 A/ns	0.588 A/ns	29.8 nH	67.3 nH
30 A	30.0 V	44.6 V	0.976 A/ns	0.646 A/ns	30.7 nH	69 nH

dynamic power device characterizer from Keysight, using the same input data. This experiment does not compare any hardware components but proves the accuracy of the parameter extraction software against the PD1500A serving as a reference.

2. Hard-switching DPTs with identical SiC power MOSFETs (Wolfspeeed C3M0075120D) were executed on the LITP and the PD1500A. The same test voltage and current values were used. In addition, in both cases, a conventional Two Level VSGD was used with the same external resistance, but different current capability and marginally different driving voltage levels. The resulting switching waveforms of the gate-source voltage V_{gs}, drain-source voltage V_{ds}, as well as the drain current I_{d}, were shown in a comprehensive comparison at varying time scales.

3. The extracted parameters according to the IEC 60747-8 standard are compared between the PD1500A and the LITP.

4. Soft-switching experiments were conducted with the LITP to prove the capability of the test platform to support such tests.

5. A Four Level Multilevel Voltage Source Gate Driver (MLVSGD) was successfully evaluated on the LITP. More information on this can be found in Chapter 4.

3.2.3 Results

The experimental hard-switching measurement results are visualized in Figure 3.16. The extracted parameters from these time-domain waveforms are shown in Figure 3.17. Finally, Figure 3.18 depicts soft-switching measurements. The evaluation results are as follows:

1. The average deviation between the results from the custom parameter extraction software and the PD1500A parameter extraction is less than 1.81 %. This is regarded acceptable and therefore, the custom parameter extraction software was successfully validated against the reference.

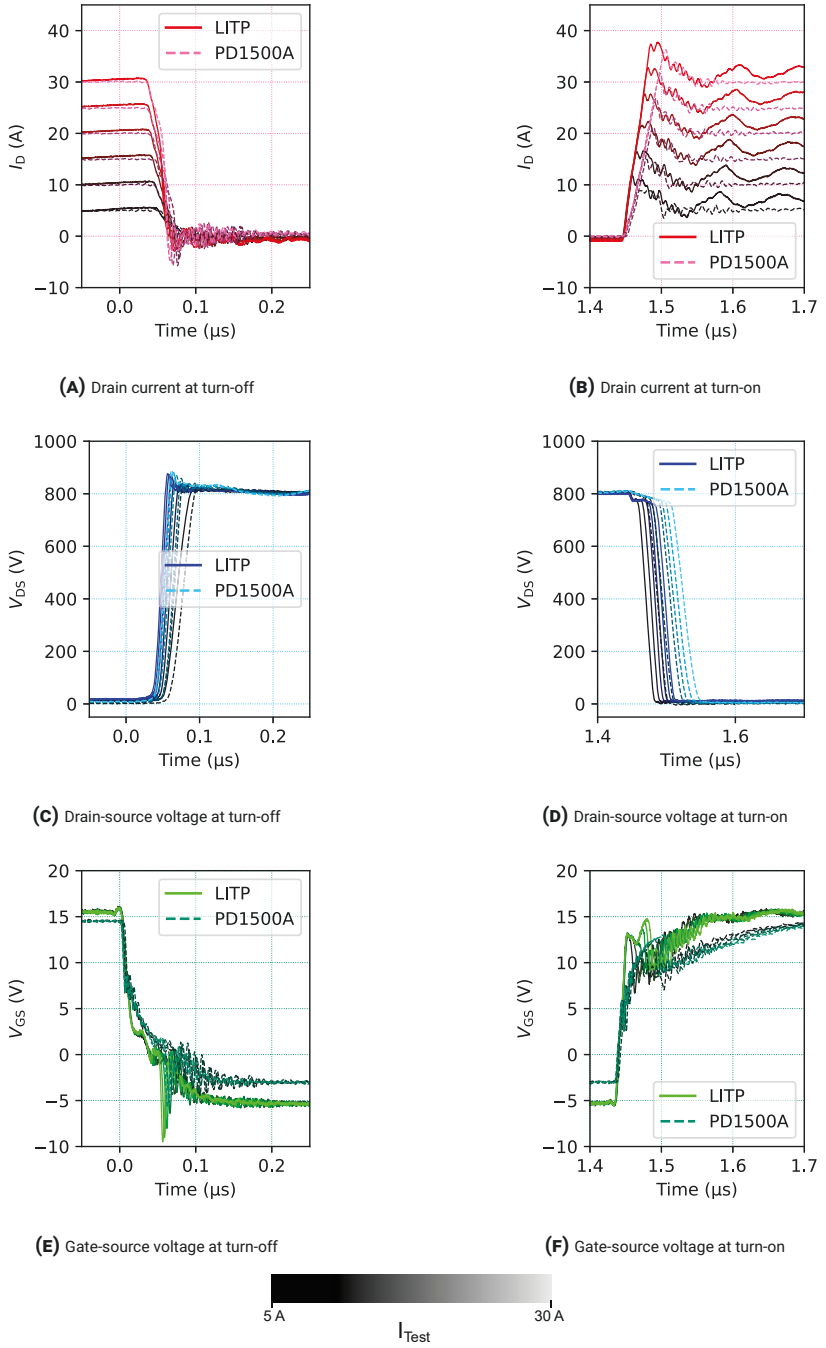
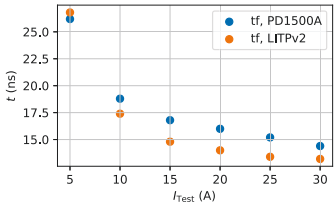
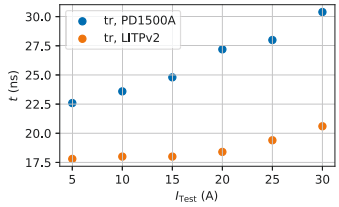


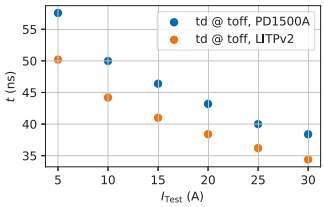
Figure 3.16. Double-pulse test measurement comparison: LITP vs PD1500A. Shades indicate the test current level according to legend.



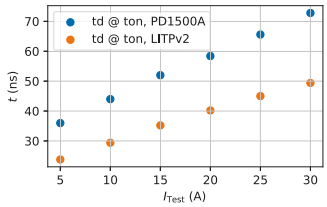
(A) Voltage transition time at turn-off (t_f)



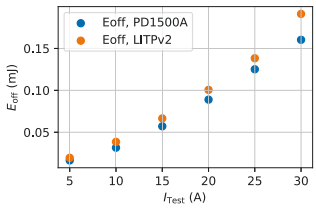
(B) Voltage transition time at turn-on (t_r)



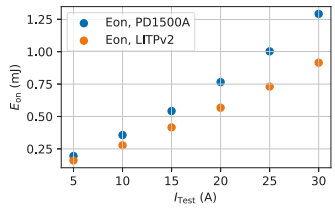
(C) Delay time at turn-off ($t_{d,off}$)



(D) Delay time at turn-on ($t_{d,on}$)



(E) Turn-off switching loss energy (E_{off})



(F) Turn-on switching loss energy (E_{on})

Figure 3.17. Extracted switching parameters in comparison: PD1500A vs LITP

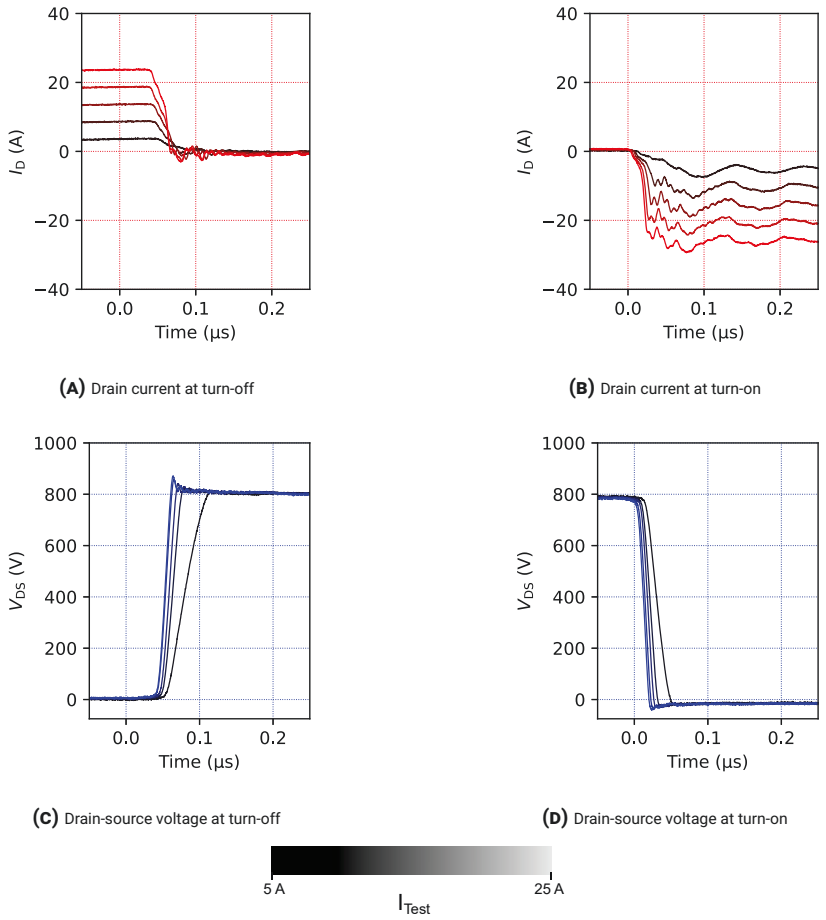


FIGURE 3.18. Soft-switching test measurements at turn-off (a, c) and at turn-on (b, d). Shades indicate the test current level according to legend.

2. At turn-on, an accelerated V_{gs} transition can be observed, leading to a faster slope in I_d, $\frac{dI_d}{dt}$, and a larger initial drop in V_{ds}. However, this inductive voltage drop increase is not proportional to the increase in $\frac{dI_d}{dt}$, which indicates a lower commutation loop inductance of the LITP compared to the PD1500A. At turn-off, the overshoot in V_{ds} is larger in the PD1500A measurements, despite an equivalent or higher $\frac{dI_d}{dt}$ in the LITP measurements. This confirms that the LITP has a lower commutation loop inductance compared to the PD1500A. The data for this conclusion is listed in Table 3.2.

3. The extracted parameters are the voltage transition times at turn-off and turn-on, t_r and t_f, the delay times at turn-off and turn-on, $t_{d,off}$ and $t_{d,on}$, and the switching loss energies at turn-off and turn-on, E_{off} and E_{on}. Due to the higher current capability of the gate driver used wth the LITP, the switching speed is clearly increased compared to the PD1500A, which results in almost exclusively lower t_r, t_f, $t_{d,off}$ and $t_{d,on}$ values. The switching losses at turn-off are very similar in both PD1500A and LITP, while all turn-on switching losses are lower in the LITP owing to the faster switching speed enabled by the lower commutation loop inductance and the higher gate current capability of the gate driver. Figure 3.17 shows the extracted parameters of the equivalent LITP and PD1500A experiments in comparison to each other.

4. The soft-switching test results, discussed more in detail in [J2], prove the capability of the test setup to conduct such tests.

3.2.4 Conclusion

The presented result shows that the LITP is capable of high-accuracy characterization of both fast-switching SiC power MOSFETs and AGDs. The characterization performance was documented on the basis of extensive, both qualitative and quantitative comparisons between switching waveforms and extracted parameters according to the IEC 60747-8 standard. In addition, soft-switching experiments are demonstrated. The low-inductive design principles including commutation loop optimization through inductance reduction and decoupling improvement, as well as the use of suitable measurement equipment, that were applied in the LITP design process were summarized. Besides, [J2] contains more details on which of these design optimization aspects can be transferred to the domain of converter design and how. Moreover, a guideline for adapting the LITP to other package types than TO-247-3 was outlined in [J2].

3.2.5 Contribution

The contributions of this work are listed in the following.

- A Low-Inductive Test Platform (LITP) consisting of a dedicated test circuit design and a parameter extraction software is proposed. The test circuit exhibits a very small commutation loop inductance, which therefore supports very fast switching speeds of SiC power MOSFETs. With the chosen circuit layout, both hard-switching and soft-switching characterization tests can be conducted. Performing high-bandwidth measurements is made possible by the dedicated measurement terminals. In addition, the signal injection port enables probe deskewing which supports highly accurate probe and sensor delay time compensation, which is essential for accurate switching loss measurements. Furthermore, the test circuit design enables the quick and damage-free exchange of both SiC power MOSFETs and gate drivers, and thereby facilitates the characterization of different MOSFETs and gate drivers without the need for soldering and thereby potentially damaging the DUTs.
- The LITP design principles were extracted and transferred to the design of converters, which helps optimize existing and future circuit designs for the integration of SiC power MOSFETs.

3.3 References

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Chapter 4

Multilevel Voltage Source Gate Drivers for Silicon Carbide power MOSFETs

Chapter 3 laid the foundation for accurate Silicon Carbide (SiC) power MOSFET and Active Gate Driver (AGD) evaluation. However, the implications of fast switching transitions as observed with SiC power MOSFETs extend far beyond the previously discussed challenges of characterization and conducting accurate measurements. Very high voltage and current changing rates (dv/dt and di/dt) are observed during fast switching operation of SiC power MOSFETs [1]. Parasitic capacitances and inductances that are exposed to fast transients, introduce significant current and voltage pulses. These can cause severe Electromagnetic Interference (EMI) with other circuits [2; 3] and present potential risks for health and degradation of both active and passive components [1; 4–6]. Severe EMI affecting the gate driver circuit might cause false triggering and an instability of the converter leading to excessive losses, or even destructive converter failure.

By manipulating the gate charging process, numerous AGDs presented in literature actively influence the transient SiC power MOSFET switching behavior. This can be used to alleviate the aforementioned issues. Three groups of AGDs have received major attention in the scientific community:

- Current Source Gate Drivers (CSGDs) can be used to adjust the gate current trajectory [7–13],
- Variable External Resistor Gate Drivers (VERGDs) contain a switchable resistor matrix to achieve a changeable external gate resistance [14–29], and
- Multilevel Voltage Source Gate Drivers (MLVSGDs) provide a set number of intermediate voltage levels for configurable durations and thereby control the gate driving voltage trajectory [C1], [15; 30–34].

MLVSGDs offer simple control and can be designed to be inherently safe during operation. Simultaneously, they offer fast-switching capability for low-loss operation, but also detailed switching transient management for EMI reduction, and switching loss control, for example for Active Temperature

Control (ATC) applications [C1]. Therefore, this chapter addresses design, implementation, and application aspects of AGDs by means of two concrete exemplary Multilevel Voltage Source Gate Drivers (MLVSGDs):

1. A Four Level MLVSGD for switching loss and slope control, and

2. A Three Level MLVSGD for voltage overshoot suppression at inductive turn-off of a SiC power MOSFETs operating as a synchronous rectifier.

The Four Level MLVSGD described in detail in Section 4.1, was first presented in publication [C1], and experimentally verified and evaluated using the Low-Inductive Test Platform (LITP) introduced [J2]. This AGD delivers an intermediate voltage level to the power MOSFET gate during switching. In principle, the values of these intermediate voltage levels can be set to an arbitrary value, respecting the limitations of the topology. One such limitation is that the gate driver switches are MOSFETs and therefore reverse conducting, and have a limited blocking voltage. The publications [J2] and [C1] exclusively address the operation of this gate driver for the purposes of switching loss and slope control. This study is to be understood as an explorative approach to identify the potential benefits of an exemplary AGD concept in an isolated environment. The merit of this approach is to show the general ability of the AGD concept to effectively shape SiC power MOSFET switching transitions.

The subsequent presentation of the Three Level MLVSGD in Section 4.2 is more application oriented. This study was first published in publication [C2]. To achieve a reduction in overvoltage across a SiC power MOSFET acting as synchronous rectifier at an inductive turn-off switching instance, an intermediate voltage level is applied to the power MOSFET gate. The duration of the pulse determines the channel resistance of the device. This resistance damps the resonance between the inductance driving the switching current and the rectifier output capacitance, which causes the high voltage spike.

A similar structure as in Chapter 3 is followed: In both Section 4.1 and Section 4.2, a brief introduction, a description of the problem that is to be solved, the applied methods, as well as the results of the applied methods are given. *Section 4.1 contains an additional discussion part on the gate driver design and implementation. This part contains previously unpublished experimental results demonstrating possible application scenarios for the proposed MLVSGD. Moreover, the design and implementation aspects found in the additional discussion section are highly relevant to the scope of this thesis.* Finally, conclusions are drawn for each of the gate drivers, and the specific contributions are named in a bullet-point list.

4.1 Four Voltage Level AGD for SiC power MOSFET Switching Loss and Slope Control

Power MOSFETs are exposed to varying operating conditions because of the intermittent nature of load profiles in typical applications, such as electric vehicles and renewable energy sources. As was shown in Chapter 2, varying operating conditions, such as DC voltage and load current, lead to a large variation of the associated switching losses. In addition, the switching transitions of current and voltage vary in steepness.

The variation of switching losses results in temperature cycles of the SiC power MOSFETs as the heat generation fluctuates. These temperature cycles have been identified as major contributors to device aging and failure mechanisms [2; 20]. Hence, switching loss manipulation enabling ATC might present an attractive application scenario for AGDs.

In addition, the switching transition rates of fast-switching SiC power MOSFETs may become critical for the health of both active and passive components [1; 4–6]. Two Level VSGDs have to be designed to limit the fastest switching speeds that are expected over the entire range of possible operating conditions, which leads to slower-than-necessary switching in all other cases. Controlling the switching slope steepness, especially dv/dt, with greater flexibility, allows for switching loss reduction in these non-critical operating conditions. Therefore, AGDs offer potential for efficiency optimization.

4.1.1 Problem Description

The control of switching transients can be realized with utilizing different techniques. As was mentioned in the introduction of this chapter, CSGDs, VERGDs, and MLVSGDs are alternative AGD concepts aiming to achieve switching transient control.

CSGDs control the gate current and thereby the state of charge of the power MOSFET gate [7–13]. These gate drivers can be based on an inductor [7–9] or MOSFETs operated in the saturation region similar to a current mirror to produce a controllable current [10–13]. Depending on the switching frequency, the associated gate driver losses of inductor-based CSGDs can be significantly larger than in other gate driver types because of ferrite and copper losses in the inductor. In addition, CSGDs built around an inductor require precise control and careful design of a freewheeling path to avoid unclamped inductive voltage spikes. CSGDs based on circuits similar to current mirrors require high-accuracy and high-bandwidth voltage sources and are difficult to build from discrete components due to fabrication variation.

TABLE 4.1. Gate driver switch states (Q1-Q6) and corresponding gate driver output voltage (VGG)

Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	V_{GG}
1	0	1	0	*	*	$V_{GG,on}$
0	1	1	0	*	*	$V_{int,on}$
*	*	0	1	1	0	$V_{int,off}$
*	*	0	1	0	1	$V_{GG,off}$

VERGDs shape the gate charging process by realizing a variable gate resistor with a high resolution in the time domain [14–29]. VERGDs could theoretically be realized as a conventional Two Level VSGD in conjunction with a switchable resistance array. However, this may introduce a large inductance into the gate path. Moreover, a multitude of reference potentials for the switch array would have to be taken into account. Therefore, all VERGDs referred to above utilize parallel connected two voltage level driver stages that are equipped with different resistor values. Using suitable control signals, the output stages are activated and deactivated according to the desired gate resistance profile. Depending on the desired resolution of the variable gate resistance, elaborate digital electronics (CPLD or FPGA) are required to operate this type of VERGD.

MLVSGDs provide a number of different voltage levels during the gate charging and discharging processes, which are thereby shaped under the influence of the voltage level timings and amplitudes, as well as an optional external gate resistor [15; 30–34]. During switching, the power MOSFET gate is connected to buffer capacitors with an array of small-signal switches. Apart from the number of voltage levels, MLVSGDs differ from each other in regard to the multilevel voltage supply, whether the voltage levels are adjustable or not, and how the switch array is realized. Accordingly, the number and types of control signals required by an individual MLVSGD depend on the specific implementation. The exact working principle depends on the individual gate driver implementation, but in principle, setting the amplitude and duration of the intermediate driving voltage levels results in an accelerated gate charging process if the amplitude is higher than the high driving voltage or lower than the low gate driving voltage. If the intermediate voltage levels are lower than the high gate driving voltage or higher than the low gate driving voltage, on the other hand, the switching process is slowed down instead. The biggest challenges in MLVSGD design are the multilevel voltage source and the array of switches delivering the voltage levels to the gate.

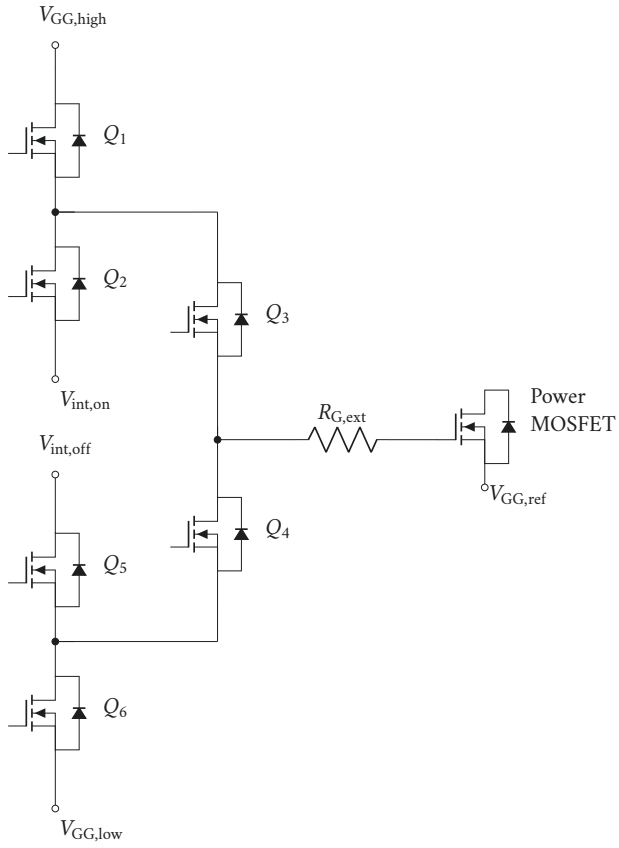


Figure 4.1. Idealized schematic circuit diagram of the Four Level MLVSGD

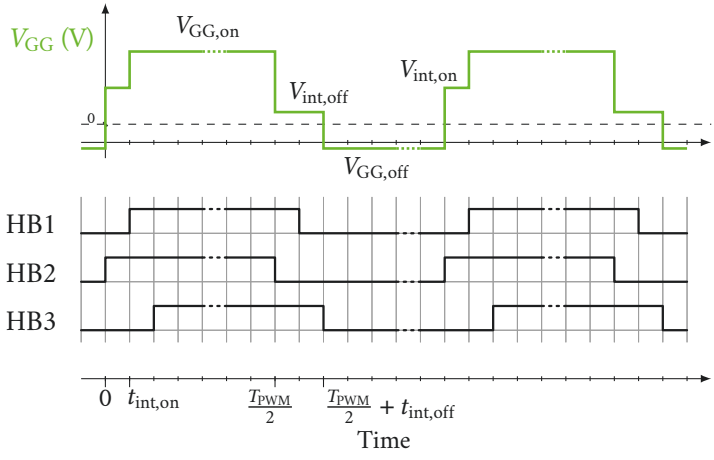


Figure 4.2. Exemplary control signals for the Four Level MLVSGD and corresponding gate driving voltage V_{GG} before $R_{G,ext}$

TABLE 4.2. Circuit parameters used during simulations of the Four Level MLVSGD

V_{DC}	I_{Test}	$R_{g,ext}$	L_t	$L_{p,g}$	$L_{p,p}$	T_{amb}
800 V	20 A	25 Ω	110 µH	1 nH	5 nH	25 °C

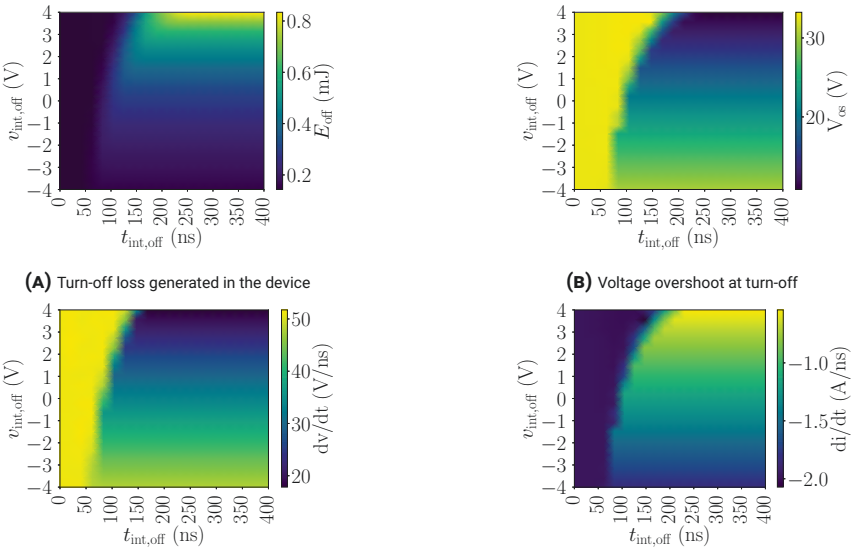
4.1.2 *Four Level MLVSGD*

Compared to CSGDs and VERGDs, MLVSGDs have the advantage of lower control and circuit complexity. The study of design, implementation, and application aspects is therefore based on an MLVSGD that provides four voltage levels.

This AGD consists of three half-bridge circuits, that are connected as shown in the schematic diagram in Figure 4.1. By applying suitable pulse width modulation (PWM) switching control signals to the half-bridge circuits HB1 (Q_1 and Q_2), HB2 (Q_3 and Q_4), and HB3 (Q_5 and Q_6), the gate driver output voltage trajectory can be shaped in various ways. This work concentrates on the simplest multilevel driving pattern supported by this gate driver: The control signals of HB1, HB2, and HB3 have the same frequency and duty cycle. A configurable delay between the control signals determines the duration of the intermediate voltage levels at the switching instances. Table 4.1 summarizes the states of the gate driver control signals and the resulting gate driving voltages. Figure 4.2 illustrates an exemplary control signal trajectory and the corresponding gate driving voltage. Only the control signal of the lower switch is shown for each half-bridge circuit. The upper switch operates synchronously, and a dead time of 20 ns is used to avoid shoot-through conditions inside the half-bridge. Although this dead time is significant compared to the switch timings, the output voltage of the four level MLVSGD is not notably affected by this.

Three of the four voltage levels, $V_{GG,on}$, $V_{int,on}$, and $V_{int,off}$, are supplied by adjustable Low-Droupout (LDO) regulators. Digital potentiometers are used to alter the divider ratio of the voltage dividers connected to each LDO and thereby change their output voltage. The digital potentiometer is configured using the Serial Peripheral Interface (SPI). $V_{GG,off}$ is fixed at −5 V.

The AGD is controlled by a Texas Instruments TMS320F280049C Microcontroller Unit (MCU). This MCU generates both the switching control signals and the SPI messages. It is implemented as a state-machine acting upon commands received from the Universal Asynchronous Receiver Transmitter (UART) interface. The commands have a similar syntax as the Standard Commands for Programmable Instruments (SCPI). During testing, commands were injected using a serial console on a personal computer.



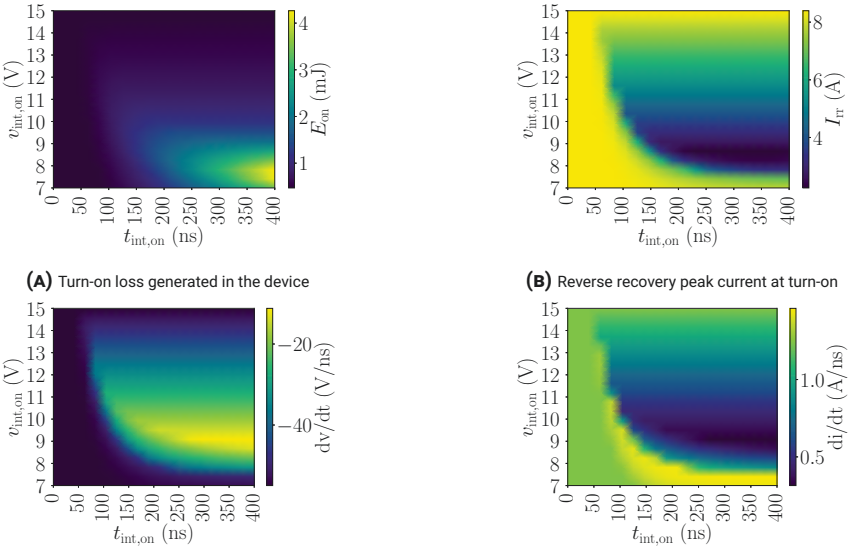
(A) Turn-off loss generated in the device

(B) Voltage overshoot at turn-off

(C) dv/dt at turn-off generated in the device

(D) di/dt at turn-off generated in the device

Figure 4.3. Influence of $V_{\text{int,off}}$ and $t_{\text{int,off}}$ on performance parameters during turn-off



(A) Turn-on loss generated in the device

(B) Reverse recovery peak current at turn-on

(C) dv/dt at turn-on generated in the device

(D) di/dt at turn-on generated in the device

Figure 4.4. Influence of $V_{\text{int,on}}$ and $t_{\text{int,on}}$ on performance parameters during turn-on

4.1.3 Results

Simulation Results

First, a SPICE simulation study was conducted for evaluating the gate driver concept. The simulated circuit is equivalent to the LITP. The manufacturer model of the C3M0075120K SiC power MOSFET was modified to improve convergence behavior [35], and placed in the positions of both the Device Under Test (DUT) and the Freewheeling Device (FD). Corresponding to the LITP circuit parameters, the parasitic inductance of the power loop was represented by one inductor in series with the drain terminals of the power MOSFET model instances in the DUT and FD positions. The gate driver was modeled as a voltage source with an idealized linearized trajectory as shown in Figure 4.2 and a series connected fixed 25 Ω resistor. $V_{\mathrm{GG,on}}$ was fixed at 15 V, and $V_{\mathrm{GG,off}}$ at −5 V. The amplitudes and durations of the intermediate voltage levels $V_{\mathrm{int,on}}$ and $V_{\mathrm{int,off}}$, and $t_{\mathrm{int,on}}$ and $t_{\mathrm{int,off}}$ respectively, were varied to study the impact of these parameters on the transient switching behavior. The test current was set to 25 A, the test voltage to 800 V. To improve the accuracy of the simulation results, a commutation loop inductance ($L_{\mathrm{loop}} = 2 \cdot L_{\mathrm{p,p}} = 2 \cdot 5\,\mathrm{nH}$) and a gate loop inductance ($L_{\mathrm{p,g}} = 1\,\mathrm{nH}$) were included in the simulation circuit, and the inductance of the test inductor L_{t} was set to 110 µH, equivalent to the experimental setup. A summary of the circuit parameters used in the simulation can be found in Table 4.2.

The simulation results are illustrated in Figure 4.3 and Figure 4.4, showing different switching parameters, i.e. the switching loss energy E_{on}, the reverse recovery current peak I_{rr}, and the current and voltage changing rates (di/dt and dv/dt) at turn-on, as well as the switching loss energy E_{off}, the drain-source voltage overshoot V_{os}, and the current and voltage changing rate (di/dt and dv/dt) at turn-off. di/dt and dv/dt are derived with an average over the entire switching transition between 10 % and 90 % of the respective current and voltage transition. These results are evidence for the effectiveness of the proposed gate driver.

Varying the intermediate voltage level amplitudes and durations, switching losses and EMI-relevant switching parameters such as the voltage overshoot and dv/dt can be controlled. Moreover, the data indicate that the controllability of these switching properties varies between different value ranges of the intermediate voltage level amplitude and duration. In particular, very short intermediate driving voltage durations of $t_{\mathrm{int,on}}, t_{\mathrm{int,off}} \leq 50\,\mathrm{ns}$ result in no influence on the switching parameters. Furthermore, the simulations predict a strictly negative correlation between switching losses and current and voltage slope steepnesses at turn-off. At turn-on, however, the simula-

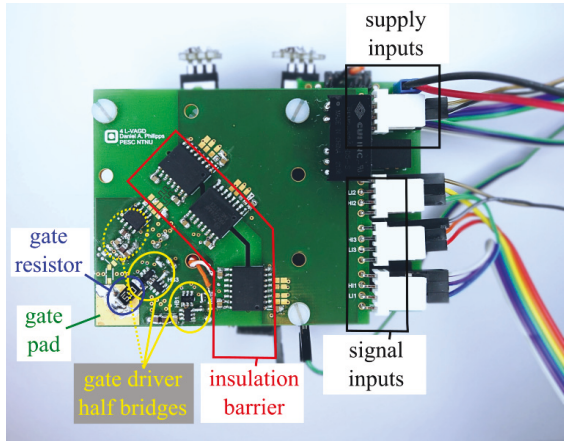


Figure 4.5. Photo of the proposed Four Level MLVSGD. The source pad is located on the back side of the Printed Circuit Board (PCB), directly behind the gate pad.

tion results indicate partly independent E_{on}, di/dt, dv/dt, and I_{rr}. This means that following the simulation results, $t_{int,on}$ and $V_{int,on}$ values can be assigned independently such that the potential for EMI is reduced by limiting dv/dt, and for a set dv/dt value, E_{on} can be optimized within a certain range. Such independence would be highly valuable for a given control objective, as they enable decoupling control objectives.

Experimental Results

To verify the simulation results, a gate driver prototype was built and an experimental study was conducted with the same parameters as in the simulations. A photo of the gate driver prototype is shown in Figure 4.5.

Exemplary time-domain measurements of I_d, V_{ds}, and V_{gs} are shown in Figure 4.6. The two displayed cases, indicated as "Pattern A" and "Pattern B", were configured with an intermediate voltage level duration of $t_{int,on}$, $t_{int,off} = 20$ ns (Pattern A) and $t_{int,on}$, $t_{int,off} = 300$ ns (Pattern B) respectively, and an amplitude of $V_{int,on} = 8.1$ V (Pattern A) and $V_{int,off} = 2.8$ V (Pattern B), respectively. These exemplary configurations showcase the general ability of the MLVSGD to effectively manipulate the V_{gs} trajectory and in turn the SiC power MOSFET switching behavior.

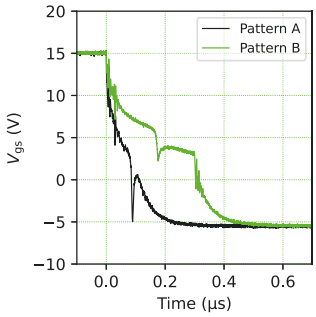
$V_{int,on}$, $V_{int,off}$, $t_{int,on}$, and $t_{int,off}$ were varied in the same value ranges as in the simulation study presented above, but with a lower resolution. The experimental measurements were then evaluated to a subset of the switching parameters obtained from the simulation results, i.e. the switching loss energy E_{on} and the reverse recovery current peak I_{rr} at turn-on, as well as the switching loss energy E_{off} and the drain-source voltage overshoot V_{os} at turn-off. Fig-

(A) Exemplary AGD Experiment Operation Points

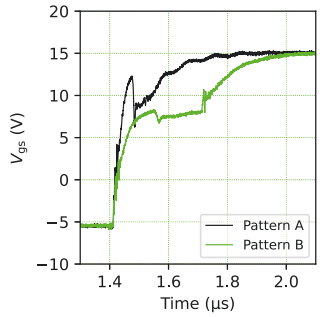
	"Pattern A"	"Pattern B"
$t_{\text{int,off}}$	20 ns	300 ns
$V_{\text{int,off}}$	−4.7 V	2.8 V

(B) Exemplary experimental operation points

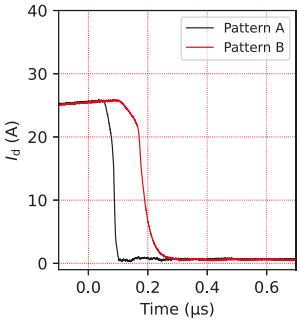
	"Pattern A"	"Pattern B"
$t_{\text{int,on}}$	20 ns	300 ns
$V_{\text{int,on}}$	8.1 V	15 V



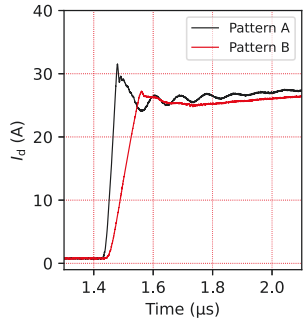
(C) V_{gs} at turn-off



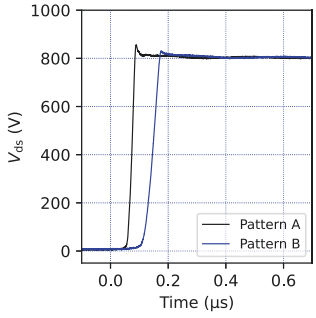
(D) V_{gs} at turn-on



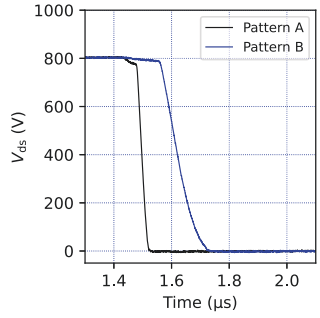
(E) I_d at turn-off



(F) I_d at turn-on

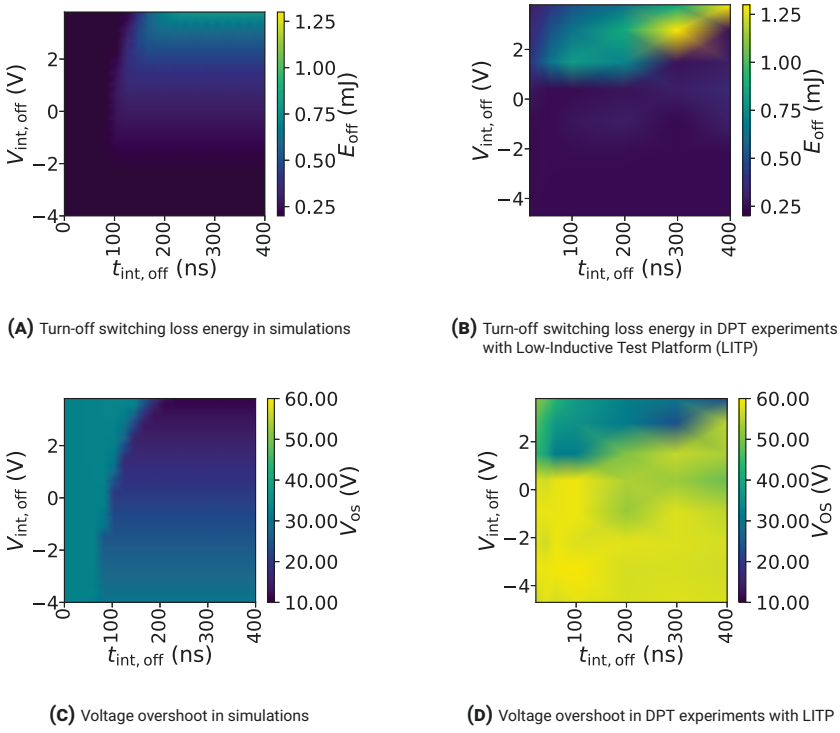


(G) V_{ds} at turn-off



(H) V_{ds} at turn-on

FIGURE 4.6. Exemplary time domain switching waveforms using the Four Level MLVSGD in different configurations.



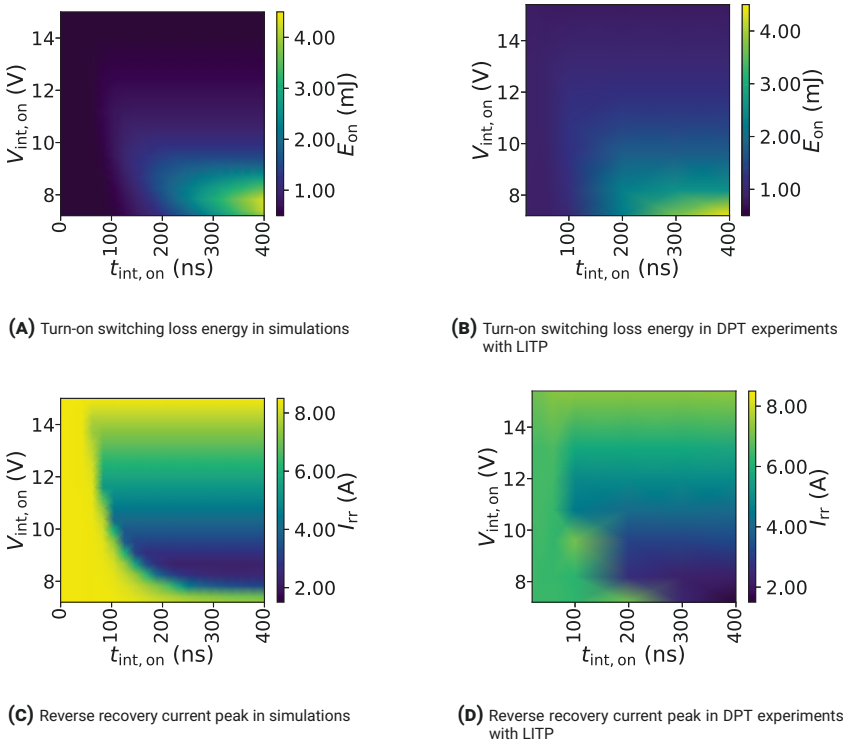
(A) Turn-off switching loss energy in simulations

(B) Turn-off switching loss energy in DPT experiments with Low-Inductive Test Platform (LITP)

(C) Voltage overshoot in simulations

(D) Voltage overshoot in DPT experiments with LITP

Figure 4.7. Simulation and Experiment Result Comparison at Turn-on



(A) Turn-on switching loss energy in simulations

(B) Turn-on switching loss energy in DPT experiments with LITP

(C) Reverse recovery current peak in simulations

(D) Reverse recovery current peak in DPT experiments with LITP

FIGURE 4.8. Simulation and experiment result comparison at turn-on

ure 4.7 and Figure 4.8 put the results from simulations and experiments into comparison.

Only in E_{on}, simulations and experiments are in good agreement in regard to the absolute loss energy values. For all other switching parameters, the absolute values considerably differ between simulations and experiments. This can be explained by the differing circuit parameters between the simulations and the LITP that were described in depth in Section 3.2. This especially concerns the voltage overshoot V_{os} that is mainly dependent on the commutation loop inductance. Moreover, the SiC power MOSFET simulation model does not perfectly represent the actual device characteristics, for example the reverse conduction behavior, which especially affects the reverse recovery current peak. Similarly, the simulation model and the physical device behavior deviate, especially in regard to the gate-drain capacitance. This has a major influence on the timing and the general outline of the switching transition. An artifact caused by this is seen in Figure 4.7a, where a variation of $t_{int,off}$ does not have any impact on E_{off} below approximately 80 ns. Looking at time domain waveforms from this simulation point reveals that the switching transition does not start earlier than 80 ns after the gate voltage at the model terminals started decreasing The switching transitions of V_{ds} and I_d, therefore, almost equal the switching transitions of a Two Level VSGD. This is different in the experimental measurements, where the switching transitions of V_{ds} and I_d follow the V_{gs} transition more closely. The region of independent switching parameters, that had been seen in simulations, could not be reproduced in experiments. Therefore, it is not expected that EMI relevant switching parameters and the switching loss can be controlled independently with this gate driver. This emphasizes the importance of experimentally validating simulation results, but also the need for more accurate device models in future power converter design.

4.1.4 *Discussion*

The design of MLVSGDs is challenging in regard to the multilevel voltage source and the switch array delivering the voltage levels to the gate. The purpose of this section is to elaborate on the Four Level MLVSGD design, showing more experimental results and presenting important application scenarios that have not been part of publication [C1].

Multilevel Voltage Source

In this work, the multilevel voltage source was realized by adjustable LDOs, coupled with a digital potentiometer. The voltage levels could also be supplied by controllable DC-DC converters to reduce the gate driver losses and enabling

a large range of voltage levels. Another alternative is the use of voltage references, like for example Zener diodes, connected in series, and each connected in parallel with a buffer capacitor. One more array of switches would connect the desired voltage reference to the primary buffers to set the desired voltage level. Loading effects on the voltage reference as well as the dynamic response to the high current draw during switching transitions have to be considered when a substantial current is drawn to drive the gate at high switching frequencies.

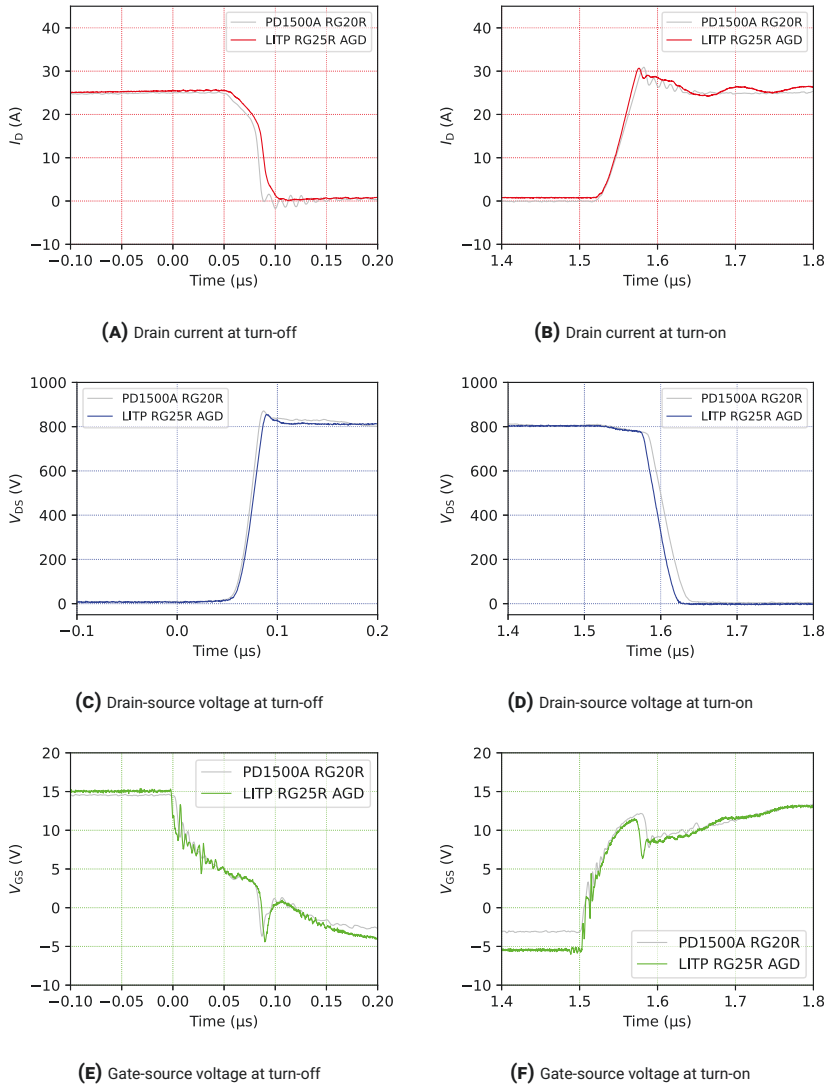
Using adjustable LDO regulators improves the resilience against the noise introduced by the fast switching slopes of the power MOSFETs. In addition, it is simpler to implement than a reference voltage system as described above, and simpler to operate than a DC/DC converter.

Switch Array

With increasing number of voltage levels, the switch array must consist of more switches to connect the various voltage levels to the gate. The approach chosen in this particular gate driver uses double as many switches as voltage levels, minus one, as they are arranged in half-bridge circuits that are pre-selected by another half-bridge circuit. Adding another voltage level would mean to add another half-bridge circuit. This means that the total number of gate driver switches equals twice the number of voltage levels minus one. Alternatively, a circuit could also be designed such that only one switch per voltage level is needed. However, an additional series-connected diode would be required to avoid current flowing between the voltage sources through the antiparallel body diodes of the gate driver switches. Half-bridge circuits are used because of their fast reaction time, and readily available building blocks that could replace them, such as totem-pole gate drivers. Moreover, blocking diodes introduce a larger voltage drop and therefore increase gate driver losses. On the other hand, fewer switches are required, and the circuit can be better optimized for low parasitic inductance. It is an individual decision of the AGD designer to choose either of these strategies or a combination thereof.

Fast-switching Capability of the Four Level MLVSGD

To assess the fast switching performance of the proposed active gate driver, the gate-source voltage measurements of two experiments are compared in Figure 4.9. The first two experiments are the characterization experiments that were conducted on the PD1500A power device characterizer with a Two Level VSGD and an external 20 Ω gate resistor. The second experiment is conducted under the same conditions with the LITP, and using the four level MLVSGD with an external 25 Ω gate resistor in a conventional driving mode, i.e. with the intermediate voltage levels equal to the high and low driving voltage levels



(A) Drain current at turn-off

(B) Drain current at turn-on

(C) Drain-source voltage at turn-off

(D) Drain-source voltage at turn-on

(E) Gate-source voltage at turn-off

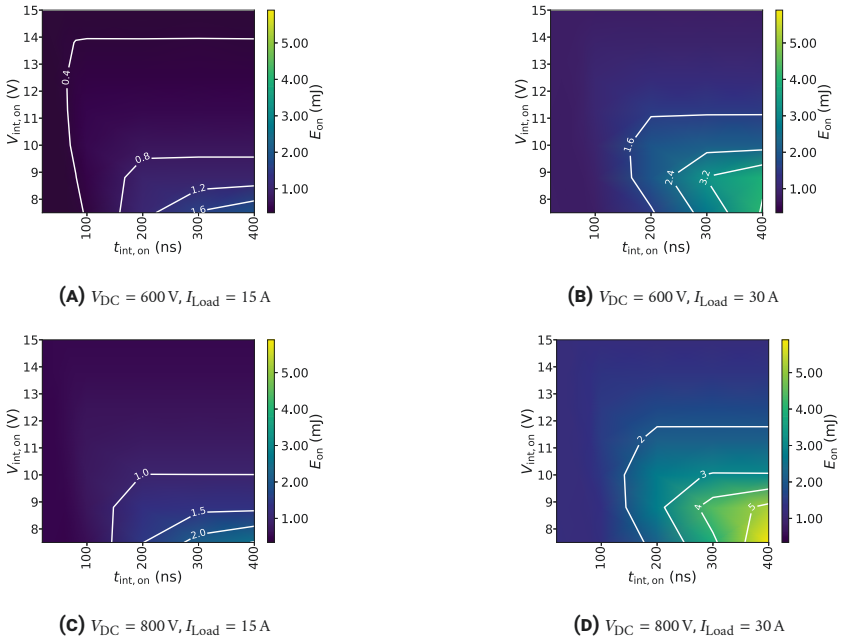
(F) Gate-source voltage at turn-on

Figure 4.9. Double-pulse test measurement comparison: PD1500A and 2LVSGD with $R_{G,ext} = 10\,\Omega$, LITP and 2LVSGD with $R_{G,ext} = 10\,\Omega$, and LITP with AGD in Two Level driving mode with with $R_{G,ext} = 25\,\Omega$.

so that the power MOSFET switching dynamics are not affected by it. The duration of the intermediate driving voltage level was set to $t_{int,on} = 400$ ns as the switching process is finished within this duration, and only the branch supplying $V_{int,on}$ supplies the charging current. If a short duration like $t_{int,on} = 20$ ns were chosen, the gate driver circuit would allow a current flow from both branch supplying $V_{int,on}$ through the body diode of the lower switch of HB1, and the branch supplying $V_{GG,on}$ the upper switch of HB1 that is closed after $t_{int,on}$. This situation is regarded less comparable to a Two Level gate driver behavior than the chosen configuration of $t_{int,on} = 400$ ns.

The results of these two experiments are in very good agreement. The differences can be explained by slight differences between the individual devices and the slightly different external gate resistor values of 20 Ω in the PD1500A experiment and 25 Ω in the LITP experiment. At turn-off, the smaller external gate resistor in the PD1500A experiment results in slightly earlier and faster switching transitions, as well as a higher overshoot voltage (Figure 4.9c). The power MOSFET used for the PD1500A experiment, has a slightly higher threshold voltage and consequently a higher Miller plateau voltage, which is reached earlier during turn-off than the lower Miller plateau voltage of the power MOSFET in the LITP experiment (Figure 4.9e). This explains the earlier onset of the switching transition in the PD1500A experiment. The faster switching speed is caused by the slightly smaller external gate resistor in the PD1500A experiment. Furthermore, the smaller gate resistor in the PD1500A experiment leads to a smaller gate-source voltage drop after the drain-source voltage peak has been reached at approximately 90 ns. The gate-source voltage trajectories deviate after approximately 125 ns due to the different low gate driving voltages, i.e. −5 V in the LITP experiment and −3 V in the PD1500A experiment.

At turn-on, the LITP experiment shows slightly faster switching behavior that is caused by the lower threshold voltage of the power MOSFET in this experiment, which is reached earlier than in the PD1500A experiment. The lower threshold voltage also translates into a lower gate-source voltage in the saturation region for the load current of 25 A compared to the PD1500A experiment Moreover, a lower Miller plateau voltage can also be observed in this experiment. After the voltage transition (after approximately 1.7 µs, Figure 4.9d), the gate-source voltage trajectories are almost identical (Figure 4.9f). To summarize, these results show the ability of the proposed Four Level MLVSGD to achieve fast turn-on and turn-off switching speed compared to the conventional Two Level voltage gate driver used as a reference (Texas Instruments UCC5390EC) with a similar gate resistor.



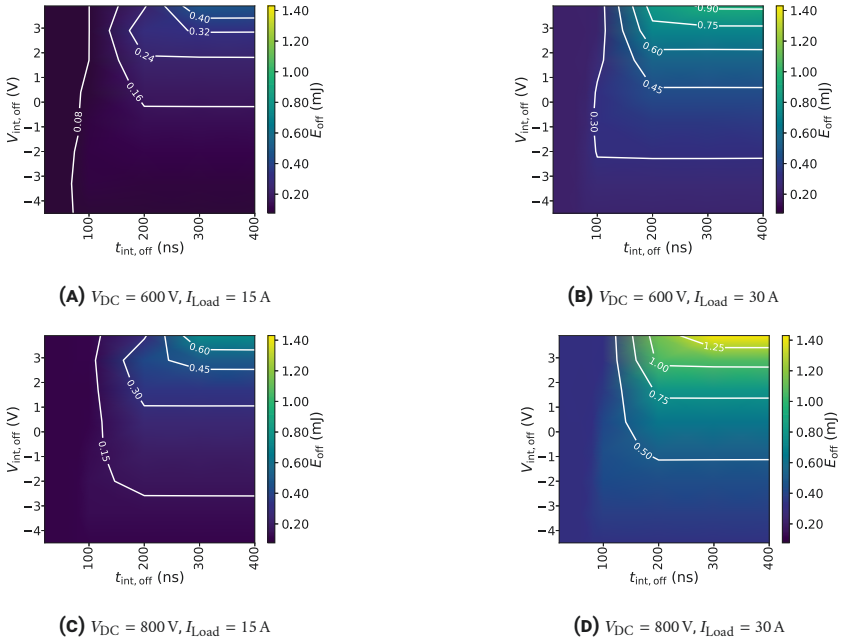
(A) $V_{\text{DC}} = 600\,\text{V}$, $I_{\text{Load}} = 15\,\text{A}$

(B) $V_{\text{DC}} = 600\,\text{V}$, $I_{\text{Load}} = 30\,\text{A}$

(C) $V_{\text{DC}} = 800\,\text{V}$, $I_{\text{Load}} = 15\,\text{A}$

(D) $V_{\text{DC}} = 800\,\text{V}$, $I_{\text{Load}} = 30\,\text{A}$

FIGURE 4.10. Turn-on switching loss in different DC voltage and load current scenarios



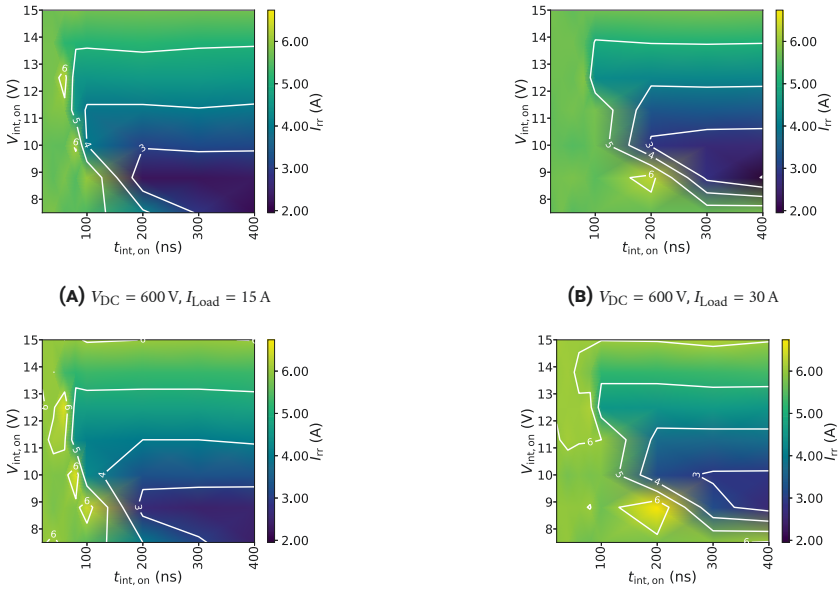
(A) $V_{\text{DC}} = 600\,\text{V}$, $I_{\text{Load}} = 15\,\text{A}$

(B) $V_{\text{DC}} = 600\,\text{V}$, $I_{\text{Load}} = 30\,\text{A}$

(C) $V_{\text{DC}} = 800\,\text{V}$, $I_{\text{Load}} = 15\,\text{A}$

(D) $V_{\text{DC}} = 800\,\text{V}$, $I_{\text{Load}} = 30\,\text{A}$

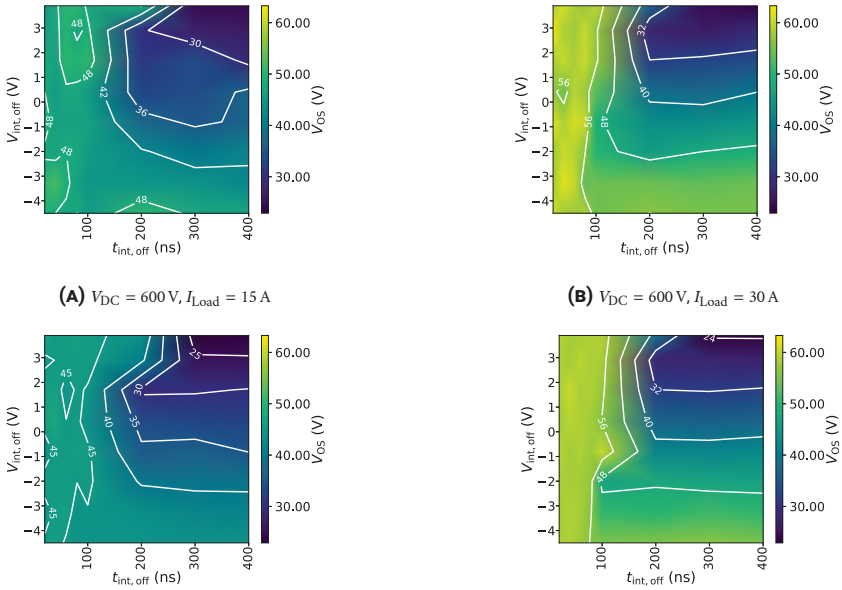
FIGURE 4.11. Turn-off switching loss in different DC voltage and load current scenarios



(A) $V_{DC} = 600\,V$, $I_{Load} = 15\,A$ **(B)** $V_{DC} = 600\,V$, $I_{Load} = 30\,A$

(C) $V_{DC} = 800\,V$, $I_{Load} = 15\,A$ **(D)** $V_{DC} = 800\,V$, $I_{Load} = 30\,A$

FIGURE 4.12. Reverse recovery current peak in different DC voltage and load current scenarios



(A) $V_{DC} = 600\,V$, $I_{Load} = 15\,A$ **(B)** $V_{DC} = 600\,V$, $I_{Load} = 30\,A$

(C) $V_{DC} = 800\,V$, $I_{Load} = 15\,A$ **(D)** $V_{DC} = 800\,V$, $I_{Load} = 30\,A$

FIGURE 4.13. Turn-off overshoot voltage in different DC voltage and load current scenarios

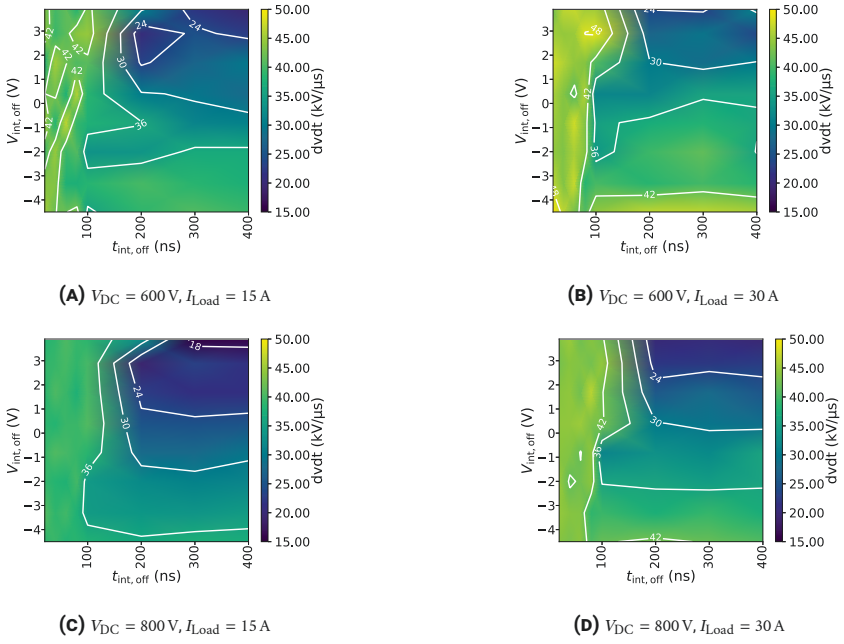


Figure 4.14. Maximum voltage transition slope (dv/dt) in different DC voltage and load current scenarios

Switching Transient Adaptation with the Four Level MLVSGD

The most important advantage over conventional Two Level voltage gate drivers is that the proposed Four Level MLVSGD, as an AGD, offers dynamic control over the switching transients. Thereby, the gate driver enables adapting the SiC power MOSFET operation to changing conditions such as load current variations and thus offers the optimization potential originally introduced in Subsection 2.5.2. Briefly summarized, conventional Two Level VSGDs are locked in their configuration once they are deployed and must therefore be designed to limit the fastest switching dynamics in the worst-case scenario. This leads to low switching speeds and high switching losses in other scenarios. AGDs avoid these unnecessarily slow switching speeds and the resulting high switching losses under operating conditions that do not inherently result in very fast switching dynamics. This can significantly increase converter efficiency.

In comparison to CSGDs, the control of the proposed Four Level MLVSGD is simpler, and the gate driver output remains within safe and predefined limits regardless of the gate impedance. The MLVSGD circuit employing discrete components is significantly more complex than a conventional gate driver. Some CSGDs [] require fewer control signals than the proposed Four Level MLVSGD. Moreover, the circuit complexity increases significantly with the

TABLE 4.3. Exemplary Four Level MLVSGD configurations for switching loss stabilization

V_{DC}	I_{load}	$t_{int,on}$	$V_{int,on}$	E_{on}	$t_{int,off}$	$V_{int,off}$	E_{off}
600 V	15 A	300 ns - 400 ns	7.5 V - 8 V	≈ 1.6 mJ	300 ns - 400 ns	4 V	≈ 450 µJ
600 V	30 A	200 ns - 400 ns	11.2 V	≈ 1.6 mJ	220 ns - 400 ns	0.5 V	≈ 450 µJ
800 V	15 A	300 ns - 400 ns	8.4 V	≈ 1.6 mJ	250 ns - 400 ns	2.8 V - 2.5 V	≈ 450 µJ
800 V	30 A	≤ 80 ns	14 V - 15 V	≈ 1.6 mJ	≤ 80 ns	−2 V - −4 V	≈ 450 µJ

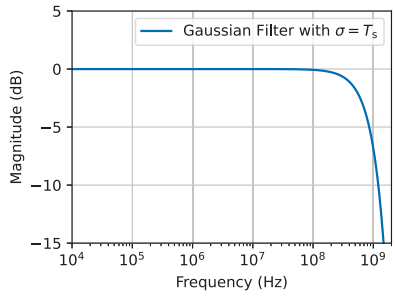


FIGURE 4.15. Filter response magnitude of a Gaussian filter with $\sigma = 0.7 \cdot T_s$. $T_s = \frac{1}{F_s}$ is the sample time, inverse of the sampling frequency F_s.

number of intermediate driving voltage levels. However, half-bridge circuits that have been used to realize the MLVSGD, are a well-known topology, and suitable switches and drivers are commonly available. Furthermore, integrated MLVSGD circuits are becoming commercially available [36]. Integrating the generation and switching of intermediate driving voltage levels reduces the circuit complexity significantly.

To showcase the ability of the proposed Four Level MLVSGD to control SiC power MOSFET switching behavior under varying load conditions, Double Pulse Test (DPT) experiments were executed at DC voltages of 600 V and 800 V, and with load currents of 15 A and 30 A. The experimental measurements were then evaluated to key dynamic switching parameters, i.e. the switching loss at turn-on (E_{on}) shown in Figure 4.10, the switching loss at turn-off (E_{off}) shown in Figure 4.11, the reverse recovery current peak (I_{rr}) shown in Figure 4.12, the voltage overshoot occurring at turn-off (V_{os}) shown in Figure 4.13, and the rate of the voltage transition at turn-off (dv/dt), of which the maximum value is shown in Figure 4.14. Figure 4.11 to Figure 4.14 are heatmap plots. As two variables, $V_{int,on}$ and $t_{int,on}$ or $V_{int,off}$ and $t_{int,off}$ respectively, are varied, the evaluation results are depicted in color as the third dimension that is needed for visualizing the results. A color bar to the right defines the values of the color coding. For comparability reasons, the color bar has not been altered within one of the above-mentioned figures. For some experiments, this reduces readability and therefore, profile lines were added that indicate a constant value

Table 4.4. Two Level VSGD (2L VSGD) vs. Four Level MLVSGD (4L MLVSGD) limited dv/dt operation (35 kV/µs)

V_{DC}	I_{load}	$E_{off,2L\ VSGD}$	$dv/dt_{2L\ VSGD}$	$E_{off,4L\ MLVSGD}$	$dv/dt_{4L\ MLVSGD}$	$V_{int,off}$	$t_{int,off}$
600 V	15 A	160 µJ	30 kV/µs	140 µJ	35 kV/µs	−1 V	300 ns
600 V	30 A	400 µJ	35 kV/µs	350 µJ	35 kV/µs	−1.5 V	120 ns
800 V	15 A	250 µJ	25 kV/µs	150 µJ	35 kV/µs	−3 V	150 ns
800 V	30 A	600 µJ	30 kV/µs	450 µJ	35 kV/µs	−1.5 V	150 ns

within the two-dimensional heatmap plot.

To obtain the maximum dv/dt values for Figure 4.14, the voltage transition was filtered with a Gaussian filter to reduce the influence of noise introduced by the sampling hardware, which is amplified when calculating the derivative of the time series data. According to the Consultative Committee for Space Data Systems (CCSDS) [37], the bandwidth, or cut-off frequency, f_c of the Gaussian filter calculates to

$$f_c = \frac{\sqrt{ln(2)}}{2\pi \cdot \sigma_t}, \tag{4.1}$$

σ_t being the standard deviation in the time domain, i.e.

$$\sigma_t = \frac{1\ \text{sample}}{5\ \text{Gsample/s}} = 200\ \text{ps}. \tag{4.2}$$

Therefore, $f_c \approx 660$ MHz, which would allow for adequately measuring signals with a bandwidth of 66 MHz, or a rise time of 5.3 ns. This is regarded adequate in the context of this work. The filter response is shown in Figure 4.15. The advantage of using a Gaussian filter instead of a moving average filter with a comparable bandwidth is that there are no side-lobes present in Gaussian filters with small values of σ ($\sigma < \frac{1}{F_s}$, F_s being the sampling frequency). Side lobes might cause strongly nonlinear magnitude distortion.

Using the proposed Four Level MLVSGD, the switching losses can be effectively manipulated across all DC voltage and load current operating points. A possible objective could be to stabilize the switching losses as part of an ATC directive. To stabilize the switching losses across these different operating conditions, the switching loss energy at turn-on could be fixed at approximately 1.6 mJ and at turn-off at approximately 450 µJ, by configuring the gate driver according to Table 4.3.

Another application example of the Four level MLVSGD is to limit the maximum dv/dt at turn-off, for example $dv/dt \leq 35$ kV/µs. An AGD such as the proposed Four Level MLVSGD is particularly suitable for this task. Compared to a conventional gate driver, the Four Level MLVSGD can effectively limit the dv/dt and simultaneously optimize for the lowest possible turn-off switching loss. Using a conventional Two Level VSGD, with a high gate driving voltage

of $V_{GG,high} = 15\,V$, a low gate driving voltage of $V_{GG,low} = 0\,V$, and an external gate resistor of $R_{G,ext} = 25\,\Omega$ approximately equals using the Four Level MLVSGD with $V_{int,off} = 0\,V$, $t_{int,off} = 400\,ns$. Both the voltage and current transition are completed at 400 ns if a voltage significantly smaller than the threshold voltage, that means 0 V or less, is applied to the power MOSFET gate for this duration.

Table 4.4 gives a comprehensive comparison between using a Two Level VSGD in the configuration explained above, and the proposed Four Level MLVSGD to limit dv/dt, listing the switching losses at turn-off, E_{off}, and the dv/dt values for both gate drivers in all four operating conditions, and the Four Level MLVSGD configuration to achieve the respective performance. By adapting the gate driver configuration, the power MOSFET is not driven overly conservative, which results in lower switching loss in keeping with the desired dv/dt limitation. This supports the major motivation for using AGDs for the optimization of SiC power MOSFET switching performance in comparison to conventional gate drivers.

Under hard-switching conditions, as it is the case for DPT experiments, the switching losses at turn-off are significantly smaller than the switching losses at turn-on. In soft-switching converters, for example, the Dual-Active Bridge (DAB) converter, soft-switching can be achieved with a certain minimal load current. When using SiC power MOSFET as switches, soft-switching does not necessarily require additional snubber capacitors because the output capacitance may act as an internal snubber [38] which is partly due to the fast dynamics observed in SiC power MOSFETs compared to their Si counterparts. In the case of soft-switching applications, the turn-off losses contribute most to the switching losses. Therefore, the turn-off switching loss optimization potential described above is especially interesting for soft-switched applications.

4.1.5 Conclusion

Conventional Two Level VSGDs cannot adapt to changing operating conditions and must therefore be designed for worst case conditions to ensure that the switching of SiC power MOSFETs stays within safe limits in regard to, for example, voltage overshoot and dv/dt. AGDs can be used to significantly improve the behavior of SiC power MOSFET by adapting to changing operating conditions. MLVSGDs are favorable compared to other types of AGDs because they offer simple control and only minor stability concerns. A Four Level MLVSGD is proposed for enhancing control over the switching dynamics of discrete SiC power MOSFETs. The proposed MLVSGD enables effective switching transient control under varying operating conditions, which was

demonstrated in a comprehensive experimental study.

4.1.6 Contribution

The main contributions of the work presented above are:

- The motivation for using AGDs was solidified and mainly focused on switching loss control and optimization under dv/dt limiting operation.
- The advantages and disadvantages of different active gate driver concepts were pointed out.
- The key design aspects of a Four Level MLVSGD were discussed in detail.
- Using the previously developed Low-Inductive Test Platform, the evaluation of AGDs was demonstrated by means of the proposed Four Level MLVSGD, demonstrating the validity of the fundamental motivation behind using AGDs.
- The insights from design, implementation, and simulation as well as experimental evaluation of the proposed Four Level MLVSGD were summarized and critically reflected.

4.2 Three Level MLVSGD for Overvoltage Suppression in Synchronous Rectifiers

While the previous study was focused on exploring the general ability of the proposed Four Level MLVSGD to meaningfully manipulate the transient switching behavior of SiC power MOSFETs, this work is focused on a more specific application, i.e. the unclamped inductive turn-off procedure of a SiC power MOSFET in synchronous rectification mode. The proposed three-level MLVSGD aims at lowering the overshoot voltage observed across the synchronous rectifier in comparison to conventional gate drivers.

4.2.1 Problem Description

Diode rectifiers introduce significant conduction losses because of the inherent forward voltage of these devices. To increase rectification efficiency, power diodes can be substituted by power MOSFETs.

As a consequence of using one-directional switches in some converter topologies (such as the High-Frequency Link Converter [39]), the current commutation during the turn-off transition of a synchronous rectifier causes a high

TABLE 4.5. Gate driver switch states (Q1-Q4) and corresponding gate driver output voltage (VGG)

Q_1	Q_2	Q_3	Q_4	V_{GG}
1	0	0	1	18 V
1	0	1	0	13 V
0	1	0	1	0 V
0	1	1	0	−5 V

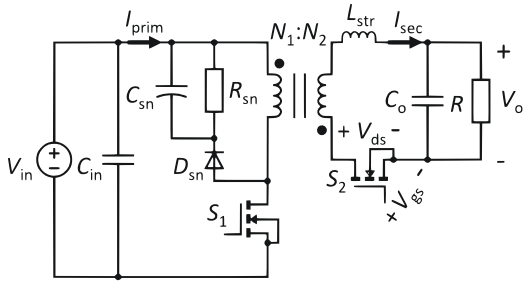


FIGURE 4.16. Schematic diagram of a synchronous DC/DC flyback converter.

overshoot voltage. This overvoltage results from a resonant oscillation between the inductance driving the turn-off current, usually a parasitic inductance, and the rectifier device output capacitance. To withstand this high overshoot voltage, rectifier components have to be notably over-dimensioned in regard to their blocking voltage capability. Snubber circuits can be used to suppress this overvoltage, but they introduce more power components to the circuit and the absorbed energy is ultimately dissipated as heat. This degrades the converter efficiency and additional measures for proper heat dissipation are necessary, depending on the amount of loss energy.

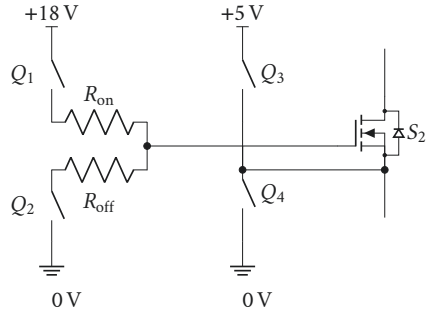


FIGURE 4.17. Three Level MLVSGD and Power MOSFET S_1

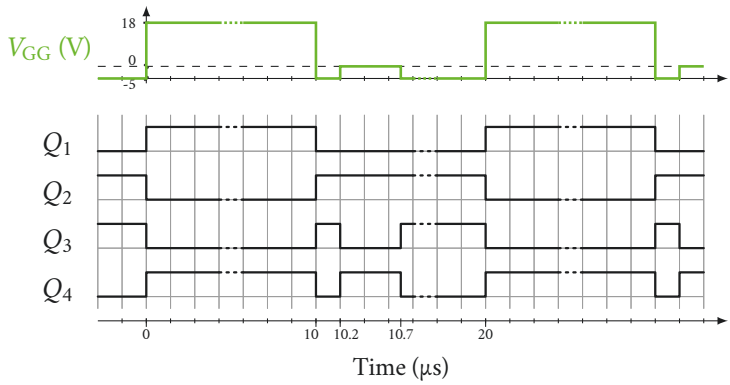


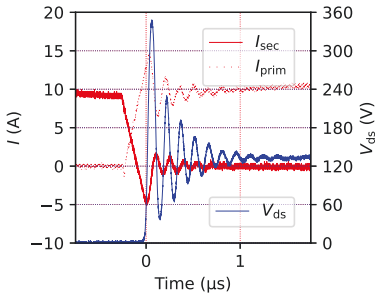
FIGURE 4.18. Idealized three-level VSGD open gate output voltage (V_{GG}) and corresponding digital control signals

4.2.2 *Three Level MLVSGD for Overshoot Voltage Minimization*

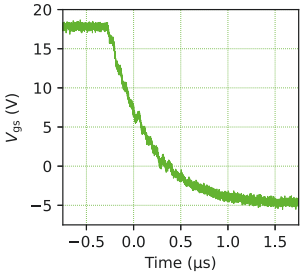
As an alternative to snubber circuits, this work investigates using a three-level MLVSGD to reduce the voltage overshoot and thereby the blocking voltage rating requirement. To study the suitability of this Three Level MLVSGD, a flyback converter was built, and a SiC power MOSFET was used as the rectifier on the secondary converter side. A schematic diagram of the converter is shown in Figure 4.16. The SiC power MOSFET was equipped with the Three Level MLVSGD. The schematic of this MLVSGD is shown in Figure 4.17, and a typical switching pattern is shown in Figure 4.18. Table 4.5 lists the possible gate driver switch state configurations and the associated gate driver output voltage (V_{GG}). The state listed second in Table 4.5 is not used in this study to achieve minimal switching losses at turn-on.

At turn-off of the synchronous rectifier, Q_1 and Q_4 are switched off, and Q_2 and Q_3 are switched on, providing a gate driver output voltage of −5 V before the turn-off resistor R_{off}. This switch configuration is kept for a configurable duration, 200 ns in the case of this work. Afterwards, Q_3 is switched off, and Q_4 is switched on, changing the gate driver output voltage to 0 V. In this work, this state is kept for 500 ns, followed by switching Q_4 off, switching Q_3 on to provide a driving voltage of −5 V while the rectifier is in off-state.

Applying 0 V to the gate after a configurable duration slows down the gate discharging process and leads to a higher gate-source voltage V_{gs} at the zero transition of the secondary current, when the resonant oscillation between the drain-source voltage V_{ds} and the drain current I_d commences. V_{gs} determines the resistance of the power MOSFET channel, which is introduced to the resonant circuit, reducing the oscillatory V_{ds} peak. However, the additional conductive path enables an increase of the drain current, resulting in a larger

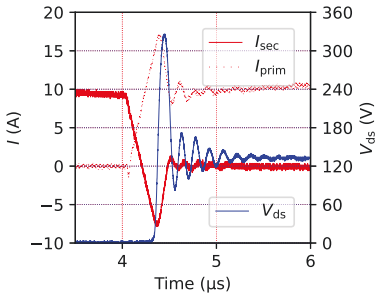


(A) Transformer current on secondary (I_{sec}) and Primary (I_{prim}) side, and rectifier forward voltage (V_{ds})

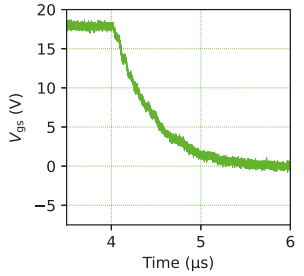


(B) Rectifier gate-source voltage (V_{gs})

FIGURE 4.19. Experimental results for the synchronous flyback converter employing the VSGD pattern A.



(A) Transformer current on secondary (I_{sec}) and Primary (I_{prim}) side, and rectifier forward voltage (V_{ds})



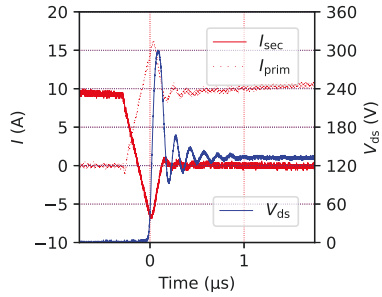
(B) Rectifier gate-source voltage (V_{gs})

FIGURE 4.20. Experimental results for the synchronous flyback converter employing the VSGD pattern B.

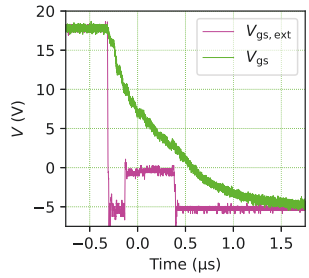
negative secondary current peak. Applying −5 V first ensures a fast transition to the desired gate voltage, reducing the turn-off delay time and accelerating the initial rise of V_{ds}, depending on the duration during which −5 V is applied. Moreover, this duration determines V_{gs} at the onset of the resonant oscillation, and thereby the damping effect introduced by the power MOSFET.

TABLE 4.6. VSGD patterns and associated voltage and current peaks

Experiment	t_{low}	t_{int}	$V_{ds,max}$	$I_{sec,min}$
VSGD A	10 µs	0	348 V	−5.16 A
VSGD B	0	10 µs	326 V	−7.80 A
VSGD C	200 ns	500 ns	300 V	−6.84 A



(A) Transformer current on secondary (I_{sec}) and primary (I_{prim}) side, and rectifier forward voltage (V_{ds})



(B) Rectifier gate-source voltage (V_{gs}) and 3-level VSGD output voltage ($V_{gs,ext}$)

FIGURE 4.21. Experimental results for the synchronous flyback converter employing the VSGD pattern C.

4.2.3 Experimental Results

To verify the capability of this Three Level MLVSGD to reduce the resonant voltage peak, three experiments were conducted using a flyback converter, and equipping the SiC power MOSFET in the synchronous rectifier position with the proposed Three Level MLVSGD. In these three experiments, different driving patterns are studied, characterizing how they influence both the voltage and current peak. The respective configurations are listed in Table 4.6. In addition, Table 4.6 also lists the peaks of the drain-source voltage across the rectifier and the negative peak in the secondary current, that is a positive drain current peak. The measured waveforms of V_{gs}, V_{ds}, and I_d are shown in Figure 4.19, Figure 4.20, and Figure 4.21, respectively.

VSGD pattern A leads to the higher voltage peak. The power MOSFET is turned off as fast as possible in this case, which leads to a resonance that is only very slightly damped by the small residual channel conductivity. Using VSGD pattern B on the other hand, the power MOSFET is almost fully conductive during the resonant oscillation. Therefore, a much larger damping is observed. However, this also leads to the largest increase in current, which contributes to the voltage peak as well. VSGD pattern C, which implements the Three Level MLVSGD, ensures a quick discharge to the desired residual gate-source voltage and accordingly, the desired channel resistance. This leads to a significant damping of the resonant voltage peak compared to VSGD pattern A, while reducing the current peak by optimizing the channel conductivity compared to VSGD pattern B, resulting in the lowest recorded resonant voltage peak. More details about the experimental setup can be found in [C2].

4.2.4 Conclusion

A theoretical model for the high voltage peak occurring across the synchronous rectifier in the case of inductive turn-off was derived. As an alternative to snubber circuits, a Three Level MLVSGD is proposed to reduce this voltage peak. In experiments, the influence of the Three Level MLVSGD on the voltage peak was studied in comparison to two different Two Level VSGD driving patterns. The experimental results support the hypothesis of resonant damping by introducing a V_{gs} dependent resistive component into the resonant circuit, which is achieved by the proposed Three Level MLVSGD and can be influenced by t_{low}. In future work, t_{low} should be varied to optimize for the lowest possible resonant voltage peak, and the study should be continued at higher DC voltages on the secondary side. Furthermore, the increase of the peak in I_d will translate into a higher switching loss (E_{off}) compared to the gate driving pattern, enabling

the fastest turn-off switching speed. Therefore, a future study should also take the E_{off} into account. In addition, the observed resonance might be partly suppressed with an advantageous timing between the primary and secondary switches. Finally, snubber solutions should be added to the comparison, which should be extended to include gross efficiency calculations of all scenarios to determine the practical implications of the different approaches to reduce the voltage peak.

4.2.5 Contribution

This work contributes specifically and generally to explaining AGD adaptation in an application.

- A theoretical model of the voltage peak occurring after inductive turn-off of a rectifier is developed.
- A Three Level MLVSGD is proposed for reducing this voltage peak, and an explanation of the working principle is given.
- Experimental results obtained with a model circuit (flyback converter) verify the effectivity of the proposed MLVSGD.
- The typical steps of AGD evaluation are presented, i.e. problem identification, modeling the problem cause, considering a mechanism through which a suitable AGD can solve the problem, design and implementation of the physical AGD, and evaluation of the physical AGD within the circuit environment, as well as comparison to other approaches determining the merit of using the AGD.

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Chapter 5

Information Transfer to AGDs for SiC Ppower MOSFETs

Chapter 4 presented two different Active Gate Drivers (AGDs) and possible application scenarios. The respective studies concentrated on identifying what influence the AGDs can exert on the controlled Silicon Carbide (SiC) power MOSFET. Especially the proposed Four Level Multilevel Voltage Source Gate Driver (MLVSGD) has been shown to enable adjustments of the switching behavior during the runtime of the converter. Such online re-configurations require a way to communicate a desired configuration to the AGD.

In state-of-the-art converters, the communication between converter control and gate driver is implemented unidirectional with either electrical or optical wires, as it requires high time resolution. Large power converter arrays, like used in distributed Renewable Energy Sources (RES) such as wind turbines or solar parks, are equipped with communication technology to a grid control instance that allows for down-regulation in case of critical power supply surplus in the grid. This communication is mostly established over the internet [1], which is possible because the time resolution of grid planning is low, and it is possible to pre-configure the system ahead of time when a said power surplus is predictable. These two examples illustrate that Information Transmission Routes (ITR) that are present in a Power Electronics System (PES), vary greatly in the information density and type. This is reflected in the requirements on the communication technology that is used to realize an ITR.

Communication and computation technologies have been subject to an impressive evolution over the recent decades, transforming our lives with smartphones, wireless access to the internet and wireless communication between devices. Today, many Wireless Communication Technologies (WCT) rival their wired alternatives. Therefore, it is becoming realistic that mobile network technology can substitute a wired connection to the internet [2] that is prevalent in large RES. With the advancements in fast and accessible mobile networks, the communication between power grid control units and converters is expected to make RES more controllable. This motivates to investigate in how far WCTs are able to support ITRs within a converter, too.

To address this question, the feasibility of adapting Wireless Communi-

cation Technologies (WCT) for the communication with AGDs is assessed in publication [J3]. Starting from a typical PES structure, possible ITRs within this system are identified and categorized conceptually by means of a novel taxonomy that is proposed in this work. Afterward, exemplary WCTs are characterized and investigated as potential implementations for the different ITR classes. Finally, after assessing the merit of implementing all given ITRs by means of suitable WCTs, wireless control of the earlier proposed Four Level MLVSGD is demonstrated in experiments.

5.1 Wireless Control of AGDs for SiC power MOSFETs

Today's electric grid is undergoing a major transformation towards more decentralized generation. This results in increasingly complex power flow problems to be solved in energy markets ahead of time but also in situ, should unexpected faults occur in the power system. The growing number of Renewable Energy Sources (RES) are in majority interfaced to the power grid by means of power electronic converters. To support system stability and enhance controllability, RES increasingly incorporate communication technology to support more advanced and coordinated control, like in wind farms, for example [1].

Simultaneously, WCT advancements in the past decades lead to the assumption that the demand for data transmission in PES can be realized by WCTs in the future. The International Renewable Energy Agency (IRENA) regards communication protocols and interfaces as one major key enabling factor for a higher penetration of RES in future power grids. All the exemplary communication technologies mentioned in their "innovation landscape brief" on the topic of Internet of Things (IoT) are WCTs [3]. IRENA points out that standards for information exchange over these technologies are a work in progress.

Within a converter, using WCTs can have several advantages, including but not limited to

- Reduction of conductive, capacitive and inductive links between the power and the control hardware,
- Increased flexibility in regard to component arrangement, and
- Enhanced modularity of converter building blocks.

5.1.1 Problem Description

The development of WCTs encourages analyzing potential benefits when used in different parts of PES. Several studies have investigated the use of WCTs

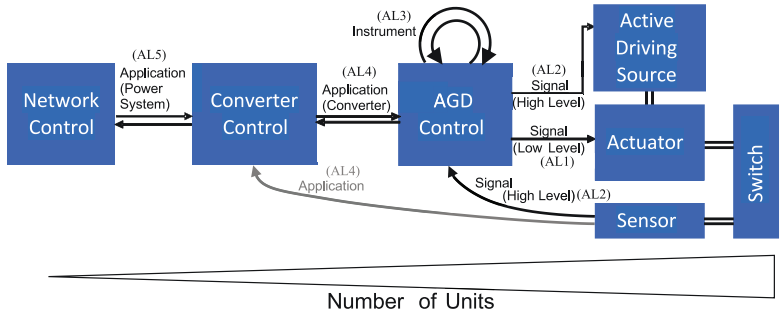

FIGURE 5.1. Power Electronics System (PES) layout employing Active Gate Drivers (AGDs)

for gate driver control [4–8]. However, the merit of using WCTs has not been comprehensively analyzed considering various degrees of abstraction in the information transfer. An approach of systematically defining ITRs on a conceptual level as well as their requirements on potential WCTs has not been presented in literature.

5.1.2 ITR Taxonomy and WCT Merit Analysis

In a first step, therefore, a PES structure is laid out to base the following considerations upon. A conceptual definition of several ITR classes within this PES structure is proposed in this work. This definition includes an abstraction level describing the character of the transmitted information, the potential content of the transmitted information, an estimation of the required data rate and latency. The classification does not take into account whether any of the given ITRs actually is present in any current PES, or whether they are implemented with wired or wireless solutions. The goal is to consider all possible ITRs and describe them in an abstract manner. Subsequently, exemplary WCTs are presented with their characteristics, their suitability to support the various ITR classes in the taxonomy, and whether an implementation of a given ITR is assessed beneficial. This assessment is reinforced with the major advantages and disadvantages associated with realizing an ITR with a suitable WCT. Finally, the communication to the previously proposed Four Level MLVSGD is demonstrated with a Bluetooth Low Energy (BLE) link in experiments to verify the feasibility of wirelessly controlling the behavior of this AGD.

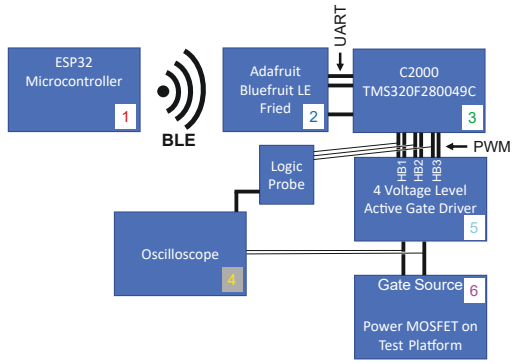

FIGURE 5.2. Schematic diagram of the experimental test setup

TABLE 5.1. Information Transmission Route (ITR) abstraction levels and Wireless Communication Technology (WCT) usage recommendations

Abstraction Level (AL)	Recommendation	Suitable Technology	Reasons
Application (Power System) (AL5)	WCT	Wireless Wide Area Network (WWAN), e.g. 4G	Cost Effectiveness
Application (Converter) (AL4)	WCT	WiFi, Bluetooth LE	Modularity, Adaptability, Flexibility
Instrument (AL3)	Wired Solution	Bi-directional Digital Isolators	Cost Effectiveness, Complexity
Signal (High Level) (AL2)	Wired Solution	Uni-directional Digital Isolators	Cost Effectiveness, Complexity
Signal (Low Level) (AL1)	Wired Solution	Uni-directional Digital Isolators	Cost Effectiveness, Complexity, Reliability

5.1.3 Results

Figure 5.1 illustrates the PES structure on which the ITR taxonomy was based. A key aspect of this structure is that contrary to classical designs in which gate drivers are conceived as binary actuators, AGDs are seen as significantly more complex units consisting of multiple parts. In particular, AGDs feature their own control unit, an MCU with considerable computational power. Compared to many conventional converter designs, this is an additional hardware block. Including this additional hardware block is justified by the fact that the functionality of AGDs exceeds that of their conventional Two Level VSGD counterparts to a large degree. Therefore, a more complex signal generation or processing unit is required anyway to control all gate driver components. Thus, making this control unit largely autonomous, for example by moving the responsibility of generating the Pulse Width Modulation (PWM) signals

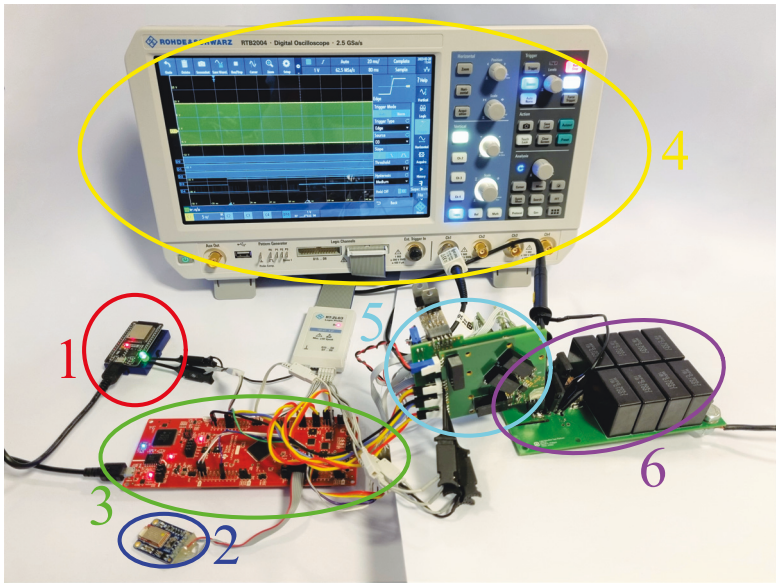

FIGURE 5.3. Wireless AGD control demonstration test setup.
1: ESP32 BLE central, 2: Adafruit BLE Friend BLE peripheral, 3: F28004x LaunchPad, 4: MSO, 5: Four Level MLVSGD, 6: Low-Inductive Test Platform

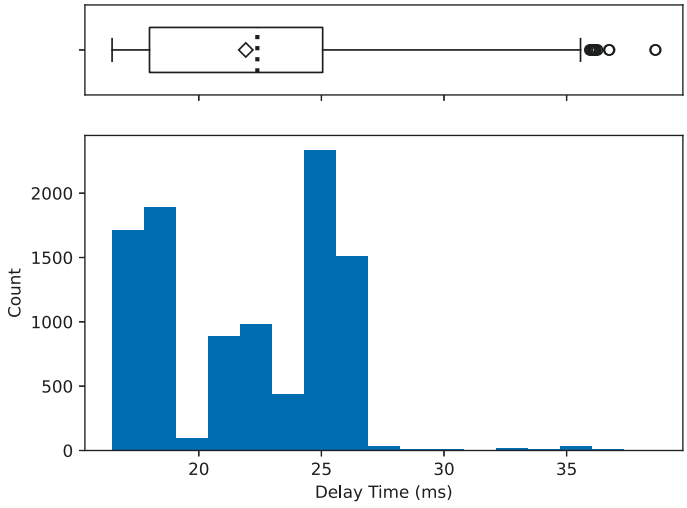

FIGURE 5.4. Information transfer delay measurement result

to it, enhances modularity. Moreover, this enables implementing elaborate, fast and reliable safety features much closer to the SiC power MOSFETs as in conventional systems. A more comprehensive overview of the implications that follow increasing the AGD control autonomy in this manner are given in the publication [J3].

Table 5.1 summarizes the assessment of WCT usage for the ITRs that are part of the PES, including the most important arguments for the individual recommendation. A suitable technology for realizing each ITR is listed as well. For the full description of the decision process leading to this assessment, it is referred to [J3].

On abstraction level AL4, the ITR supplying the AGD with information, the use of WCTs is regarded beneficial and recommended. To verify this assessment, the control of the earlier proposed Four Level MLVSGD was implemented by means of BLE, a WCT that according to the previous results is regarded suitable for this ITR. Many reconfiguration experiments were conducted, with another MCU acting as a BLE central device tethered with a BLE to UART bridge that receives and directs messages further to the AGD control MCU. A schematic diagram of the test setup is shown in Figure 5.2, and a picture of the setup is shown in Figure 5.3.

For the purpose of these experiments, the intermediate voltage level at turn-on ($t_{\mathrm{int,on}}$) was changed from 20 ns to 300 ns as an example, but any of the Four Level MLVSGD configuration parameters can be manipulated in the same way. As has been seen in Section 4.1, changing $t_{\mathrm{int,on}}$ from 20 ns to 300 ns has a significant impact on the turn-on switching transitions at an intermediate voltage level at turn-on of $V_{\mathrm{int,on}} = 8.2\,\mathrm{V}$. The switching loss at turn-on (E_{on}) is increased from 0.92 mJ to 2.56 mJ, the voltage transition rate (dv/dt) is decreased from 21 kV to 7.37 kV, and the current transition rate (di/dt) is decreased from 0.673 A/ns to 0.328 A/ns. These dv/dt and di/dt values were calculated as average over the entire switching transition. For switching transition waveforms, it is referred to the publication [J3].

Before the reconfiguration message is sent, the BLE central MCU pulls a GPIO high, and after a message is received and registered by the AGD control MCU, it pulls one of its own GPIOs high. Thereby, the latency of this particular information transfer, including preparation, sending, receiving, and processing can be simply measured. Repeating this procedure 10000 times and measuring the delay between the two rising edges described above, results in a delay characteristic as shown in Figure 5.4. The longest delay measured is 38.6 ms, confirming that the delay introduced by the BLE-implementation of this ITR is significantly shorter than 100 ms, which was identified as the slowest acceptable latency for ITRs in category AL4. Therefore, the wireless control of the Four Level MLVSGD by means of BLE has been successfully demonstrated.

5.1.4 Conclusion

This chapter presents a systematic approach for analyzing the merit of realizing information transfer within a PES by means of WCTs. Following the proposed ITR taxonomy, requirements for potential WCTs can be easily derived. This makes the taxonomy applicable in future with further advancements of WCTs. Advantages and disadvantages of using suitable WCTs can be weighed against each other, enabling a continuous re-consideration of WCTs.

Exemplary state-of-the-art WCTs were characterized and identified as potential candidates for ITR realization in every category of the proposed taxonomy. Following this analysis, the advantages and disadvantages of these WCTs were assessed and projected on the general usage of WCTs for the given ITRs, resulting in a recommendation for or against the use of WCTs for the given ITRs.

Finally, the ITR supporting information transfer to an AGD control unit was implemented by means of BLE and the latency of this implementation was experimentally characterized. The experimental results confirm the viability of BLE as a WCT realizing an ITR on abstraction level AL4, serving the supply of information to a partly autonomously controlled AGD with a total latency of less than 40 ms.

5.1.5 Contribution

This work

- offers a tool to systematically describe information transfer in different parts of a PES and consequently arrive at requirements for communication technologies to realize the information transfer.
- investigates state-of-the-art WCTs in regard to their ability to realize the various ITRs within a PES, and formulates recommendations for or against the use of these WCTs.
- successfully demonstrates this methodology by the example of BLE for supplying the earlier proposed Four Level MLVSGD with control information at a latency of less than 40 ms.

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Part III

Conclusion and Further Work

Chapter 6

Conclusion and Further Work

6.1 Conclusion

The aim of this thesis is presenting contributions that were made during the PhD project regarding the dynamic characterization, evaluation and control of AGDs for fast-switching SiC power MOSFETs. Chapter 3 dealt with the dynamic characterization of fast-switching SiC power MOSFETs used with either conventional Two Level Voltage Source Gate Drivers (VSGDs) or AGDs. Conducting an in-depth study, a coaxial Current Viewing Resistor (CVR) was determined as a suitable current sensing technology for fast-switching SiC power MOSFET and AGD characterization. The coaxial CVR can deliver accurate measurements at high amplitudes and high signal bandwidth, as present in the switching waveforms of discrete SiC power MOSFETs. Subsequently, a circuit optimized to achieve a very low commutation loop inductance was presented that is capable of dynamic characterization of fast-switching discrete SiC MOSFETs with any gate driver type. In addition, the gate driver terminals can be used to connect different gate driver types to the circuit. This Low-Inductive Test Platform (LITP) fulfills the first objective as defined in Section 1.2.

Chapter 4 discussed both design, evaluation and application aspects by means of two specific Multilevel VSGDs (MLVSGDs). First, a Four Level MLVSGD was analyzed with respect to its ability to perform fast switching transitions, and to manipulate the voltage transition slew rate and consequentially switching losses. Secondly, a Three Level MLVSGD was shown to effectively reduce the peak voltage that is observed in synchronous rectifiers at unclamped inductive turn-off. These two studies comprised both general and application specific evaluation demonstrations of AGD design, implementation and evaluation in accordance with Objective 2 as defined in Section 1.2.

Finally, Chapter 5 focused on the integration of Wireless Communication Technologies (WCTs) in Power Electronics Systems (PES). Within the context of applying a systematic approach of merit analysis, control aspects of AGDs were addressed, following the demonstration of wireless AGD control by means of

Bluetooth Low Energy (BLE). This part of the thesis provided details about the chosen approach of AGD configuration and how it can be put to use from a larger system level perspective.

By addressing these objectives, the thesis lays the groundwork for future investigations of AGDs for SiC power MOSFETs. The two-step current sensor characterization method proposed in [J1] allows the systematic and comparative evaluation of both existing and new current measurement technologies. Thereby, it enables identifying whether a specific current measurement approach is suitable for the dynamic characterization of AGD-driven, fast-switching SiC power MOSFETs. The proposed LITP can be easily adapted to fit discrete SiC power MOSFETs with a different packaging, and even SiC MOSFET power modules. Equally, other types of AGDs can be connected to the circuit, increasing its value for reuse in future work that is not restricted to the specific MLVSGD that was used to demonstrate the AGD evaluation capability. These two aspects make the LITP a powerful tool for further research. The proposed Four Level MLVSGD was evaluated extensively, including varying operating conditions of the SiC power MOSFET. This evaluation has shown that the Four Level MLVSGD enables realizing different control objectives. The complex structure and the multitude of components required for the MLVSGD reveal a weak point in the design. However, with the help of this particular design, it was shown that introducing an intermediate voltage level during switching can enable loss stabilization or efficiency improvements over conventional Two Level VSGDs. With an integrated solution, the complexity of the particular solution in this work would be a minor concern, and the dynamic performance could be even improved. Finally, the proposed taxonomy for the merit analysis of WCT integration presents a useful tool for designers to decide on if and where to use WCTs to improve system modularity, adaptability and performance. The demonstration of AGD control by means of BLE demonstrates the potential of realizing modular and flexible converter solution integrating AGDs using WCTs.

6.2 Future Work

Several research questions related to the topics that were part of this thesis could not be addressed due to time constraints. These research topics are interesting for future work and can be grouped into two categories, i.e. improvements or modifications, and continuation of the work presented in this thesis.

6.2.1 Modifications

- To accommodate different SiC power MOSFETs, the layout of the LITP can be adjusted to fit more packaging types. The TO-247-3 package presents a major limitation for fast-switching operation, as it exhibits a large terminal inductance. The most relevant competing package type is the TO-247-4 package, which features a Kelvin Source connection that almost entirely eliminates the common source inductance shared between the power and the gate loop. Another interesting packaging type with high voltage isolation capability is the D2PAK-7 package. The modifications required to adapt the LITP to these packages are relatively minor but executing them would be valuable, especially considering the good dynamic performance of the circuit.

- The Four Level MLVSGD implementation used to conduct the study presented in Section 4.1 exhibits major optimization potential, especially concerning density of components, level of integration and management of the various intermediate voltage levels. With the release of commercial gate drivers with adjustable voltage levels, this driver type can be designed much more effectively while keeping the advantages presented in this work.

- As mentioned in the publication text, the wireless AGD control presented in [J3] is partly limited by the UART interface speed that is dictated by the specific BLE adapter. Two improvements would decrease the latency and thereby increase its value for closed loop applications:

    1. Optimization of the command alphabet will significantly reduce the required transmission duration over the UART interface. The command alphabet could be as simple as transmitting one letter to identify the target and a numeric value indicating the intended set size.
    2. Using a different type of BLE adapter, for example with an ESP32 microcontroller and potentially with a custom software implementation, can significantly increase the UART interface speed and thereby reduce the latency time.

6.2.2 Continuations

1. With advancements in current sensors, continuous evaluation of new sensors would be interesting to ensure the best alternative is chosen

for the dynamic characterization experiments. In addition, building an independent database for current sensor characteristic data, all derived from the same circuit environment, would simplify the choice of current sensors significantly. In addition, such a database would allow for collaboration between different independent actors in an effort to create a reproducible common knowledge base, fostering knowledge about this important and sensible topic in power electronics. A development toward community maintained component databases is already seen with, for example, datasheet extracted characteristics of power semiconductor switches [1].

2. With the LITP, a framework for AGD evaluation with the flexibility of simple and non-destructive exchange of DUTs in both hardware and software was established. A highly interesting topic for future research is the comparative evaluation of different gate driver configurations and gate driver types, as well as different types of SiC power MOSFETs. As has been seen in the context of a work not attached to this thesis, individuals of the same SiC power MOSFET model vary greatly in their characteristics [C5]. A relevant research question therefore concerns the impact of device parameter spread on the effectiveness of different AGD strategies and control directives. This becomes especially interesting considering the fact that, due to time constraints, the AGD evaluation presented in Chapter 4 was only conducted on a single device. Perhaps, a configurable AGD can be used to compensate for device variation. Apart from that, the external gate resistor is, with 25 Ω, chosen comparatively high. For faster switching, studying the gate driver behavior with a lower resistance is interesting. Moreover, as was mentioned for the current sensors, a database organizing data of different MOSFET types together with commercially available gate drivers performing on the LITP could be of interest for a collaborative independent project.

3. Another use case for the LITP and the accurate dynamic characterization potential it offers, is to develop new and adjust existing simulation models to the characterization data. This includes deriving highly accurate SPICE component simulation models, similar as described for static characterization data in [C5]. Another interesting approach for faster simulation and integration into real-time modeling, as discussed in [C8], would be the development of new models compounding the gate driver and the MOSFET into one unit.

4. So far, the Four Level MLVSGD presented in Section 4.1 has only been tested in an isolated environment and in the context of double pulse

tests. For a more holistic approach, using the gate driver in a converter context, for example a DAB converter, is regarded necessary. This also includes using the gate driver to drive SiC MOSFET power modules instead of discrete devices, requiring higher gate currents with a lower gate resistor, as was already mentioned above. Finally, the temperature dependent device behavior has not been investigated within this work, but according to the datasheets of several MOSFET models, it has a non-negligible influence on the device behavior.

5. The wireless control of the proposed Four Level MLVSGD has been tested in forward control only. Implementing a feedback control incorporating the Four Level MLVSGD and realizing control objectives as introduced in Section 4.1 would verify the Information Transmission Route (ITR) and wireless control concepts presented in [J3] in the presence of fast switching transitions and changing operating conditions, and demonstrate the opportunity of further modularizing converters by using low-cost, commonly available WCTs such as BLE.

6.3 References

[1] Nikolas Förster, Philipp Rehlaender, Oliver Wallscheid, Frank Schafmeister, and Joachim Böcker. An open-source transistor database and toolbox as a unified software engineering tool for managing and evaluating power transistors. In *2022 IEEE Applied Power Electronics Conference and Exposition (APEC)*, pages 1747–1751, 2022. doi: 10.1109/APEC43599.2022.9773701. Cited on page/s 108.

Part IV

Publications

The chapters in this part of the thesis each contain one publication in its full preprint text. The publications were adjusted to fit the layout of this thesis, and some grammatical and orthographical mistakes were corrected. The publication content has not been edited, and neither the figure content.

Chapter 7

Performance Evaluation of High-Power, High-Bandwidth Current Measurement Technologies for SiC Switching Devices

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Submitted to: *IEEE Transactions on Power Electronics*

Contributions

- Two-step current sensor characterization method for analyzing bandwidth, flatness, linearity, and insertion impedance in both time and frequency domain
- Demonstration of the proposed method behavior in a practical circuit with four different commercially available current sensors
- Sensor selection guide for various applications

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Abstract

Silicon Carbide power MOSFETs switch at an unprecedented speed, even at high currents. Therefore, current sensors must measure high currents at a high bandwidth. With increasing switching speed, only small parasitic impedances are acceptable in the commutation loop to ensure high accuracy measurements, and this includes the current sensor insertion impedance. The contribution of this work is the demonstration of a two-step current sensor evaluation method that serves the characterization of high-power, high-bandwidth current sensors. The two steps are a small- and a large-signal transmission behavior analysis. The proposed method is applied to four specific current sensors, arriving at a suitability assessment for different applications utilizing SiC power MOSFETs. The work concludes transferring the knowledge derived in the conducted experiments to a practical, application-oriented sensor selection guide.

7.1 Introduction

Silicon Carbide (SiC) Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFETs) are entering the commercial competition with Silicon (Si) Insulated-Gate Bipolar Transistors (IGBTs) [1–3]. SiC MOSFETs exhibit numerous technological advantages, including a lower on-state resistance compared to Si IGBTs for the same blocking voltage, higher switching speed resulting in lower switching losses and stronger resilience against high temperatures [1; 3; 4].

Discrete SiC power MOSFETs are typically rated for currents of 5 A to 100 A [5–9] and SiC MOSFET power modules have ratings of more than 600 A [10]. Even at high voltage and current levels, the switching speed of SiC power MOSFETs reaches 10 kA/µs and beyond [10–13] and more than 50 kV/µs [5; 14–16]. This highlights one major challenge in characterizing and operating SiC power MOSFETs, that is to accurately measure large currents at high frequencies. In addition, the insertion impedance of the sensor must be minimal because otherwise, oscillations may occur, or the switching transitions might be slowed down because of measurement hardware. Due to the fast switching speed, even small additional impedances in the current path have a large and undesired impact.

Several current sensor review studies have been conducted [17–20]. However, these review studies rely on the manufacturer specification and either do not investigate the frequency response of the sensor, the impact of linearity when measuring high currents or how its insertion impedance affects the switched current trajectory of the power semiconductor device. Studies

analyzing the current sensor frequency response have concentrated on low power levels [21], or consider the frequency response of one particular, custom current sensor [22–27]. Another extensive study compared the behavior of various high-bandwidth current sensors by means of a small-signal analysis in the frequency domain and a large-signal analysis in the time domain, considering both commercial and custom current sensors [28]. The high-current experiments in this study are limited to the time domain and therefore do not serve the identification of nonlinear current sensor characteristics. Similarly, the impact of a given current sensor on the measured current is approximated by the insertion impedance that is measured at small currents and therefore does not represent nonlinear effects.

This work proposes a two-step performance evaluation method for high-bandwidth high-power current sensors that is distinct from the aforementioned studies. In addition to the frequency domain analysis by means of a Vector Network Analyzer (VNA), that is frequently seen in literature [22–28], the proposed method enables frequency-domain analysis with high measured current amplitudes. Moreover, the proposed method is conducted within the context of custom dynamic characterization platform [29], demonstrating its practical applicability. Subsequently, the proposed evaluation method characterizes the insertion effects of the sensors under investigation on the measured quantities. The combination of low- and high-amplitude characterization in both time and frequency domain gives holistic information about the behavior of each current sensor in regard to bandwidth, flatness, linearity, and the effect of its insertion impedance. This knowledge is finally used to derive a sensor selection guide for various application scenarios of fast-switching SiC power MOSFETs, which concludes this work together with a critical review of the proposed current sensor characterization method.

The rest of this paper is organized as follows. Section 7.2 gives an overview of the requirements for current sensors in circuits with fast-switching SiC power MOSFETs. In addition, the four most commonly used current sensor technologies are introduced. In Section 7.3, the proposed current sensor performance evaluation method is presented in detail. This method is subsequently demonstrated in Section 7.4, and all experimental results are described in depth. The observations are interpreted, and the sensors are put in comparison to each other in Section 7.5. Based on the these results, each current sensor type is evaluated with respect to its suitability for a range of application scenarios, resulting in a practical sensor selection guide. The discussion is rounded up with a critical review of the proposed current sensor evaluation method. Section 7.6 concludes the paper.

7.2 Background

In this section, criteria for current sensor assessment will be introduced and a selection of commercially available current sensor technologies will be listed. A current sensor technology chart will compare these technologies.

7.2.1 Current Sensor Requirements

Five main aspects are considered when determining the suitability of a current sensor for a particular application.

Maximum Measured Current: Dielectric and ohmic losses are present in every current sensor and therefore, all current sensors are limited in regard to the maximum measured current amplitude. Depending on the application, either the pulsed current limit, determined by the maximum permissible loss energy, or the continuous current limit, determined by the maximum possible heat power dissipation, has to be considered. In the case of Double Pulse Tests (DPTs), for example, the pulsed current limit must be considered since the measured current only lasts for a few microseconds in one test sequence. For converters, however, the continuous current is decisive. The continuous and pulsed power ratings are listed in the manufacturer datasheet.

Bandwidth: To measure a signal with a measurement error of less than 2%, a system bandwidth of more than five times the signal bandwidth is required [30; 31]. With switching times of the order of 10 ns, the current sensor must have a bandwidth of at least 175 MHz to represent current adequately. This is required for an adequate switching loss estimation, however, nonlinear switching transitions and superimposed oscillations may reach higher frequencies [32], which is also illustrated by the following example: Si IGBT power modules contain antiparallel Shottky diodes to enable reverse conduction. The reverse bias capacitance of this diode and the inductance of the bond wires that connect the diode to the output of the IGBT die, enter a resonant circuit during switching transitions, which results in oscillations exceeding 100 MHz in frequency [33]. In SiC devices, yet higher frequencies can be expected due to the reduced device capacitances compared to Si. Therefore, an even higher measurement system bandwidth is desirable. Many manufacturer specifications state a bandwidth value that can be verified with a VNA, which will be shown later.

Flatness: "Flatness" describes how closely the sensor output signal resembles a simple proportional of the measured current. Flatness is usually analyzed in the frequency domain. To avoid the need for complex filter systems, sensors should have a flat response throughout the desired measurement frequency

range. The transmission behavior and flatness of a current sensor can be characterized with a VNA, which will be shown later.

Linearity: Ideal linear systems act independently on the different input signal components. Moreover, proportional scaling of the input signal is reflected by the same proportionality in its output. The following equation holds for ideal linear systems:

$$f(a_1 \cdot x_1 + a_2 \cdot x_2) = a_1 \cdot f(x_1) + a_2 \cdot f(x_2). \tag{7.1}$$

In reality, most systems are nonlinear because of nonlinear electromagnetic material properties but behave as linear systems within certain boundaries of the input voltage, current, and frequency. Nonlinear distortion can only be detected using a wideband measurement system and an input signal crossing the boundaries of linearity for the given system. Effects of nonlinear distortion that are especially relevant in current sensors include a varying frequency dependent transmission behavior with a varying input signal amplitude, or the presence of signal frequency components in the output that do not occur in the input signal. A current sensor must behave as close as possible to a linear system in the range of expected measured currents.

Insertion Impedance: As current sensors in one way or another interact with the measured current, they introduce a finite and nonzero impedance, referred to as insertion impedance. This insertion impedance can alter the measured current and thereby falsify characterization data or cause disturbances. The influence of the insertion impedance on the switching behavior can be observed in switching waveforms, especially in drain-source voltage time-domain, and frequency domain drain current measurements.

7.2.2 *Current Sensor Types*

To improve orientation in the following overview of current sensor technologies, Figure 7.1 visualizes the bandwidth and maximum measured current specifications of four different current sensor technologies. The data were extracted from datasheets of multiple specific current sensor individuals that are listed in Table 7.3 in the Appendix. In the following, a brief description of each current sensor is given. This description includes the working principle of the sensor technology as well as typical specification in regard to the previously formulated sensor requirements.

Current Transformers consist of a coil that is placed in the magnetic field caused by the current that is to be measured. According to Faraday's law of induction, a voltage is induced in a coil by a changing flux density inside it.

One major current transformer type is the low impedance termination current transformer. According to Lenz's rule, the current induced in the

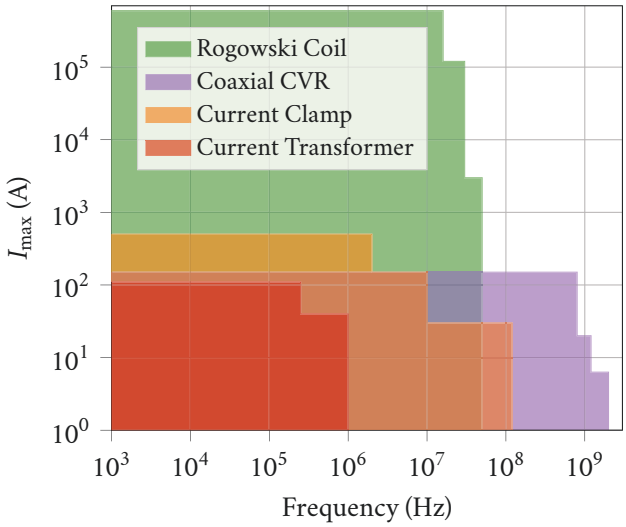


Figure 7.1. Commercially Available Current Sensors

sensor coil is proportional to the measured current, as the flux inside the sensor coil is opposed by the induced current. This principle cannot be used for DC measurements because the induction itself can only be caused by a changing magnetic flux. This type of current sensor is available for power electronics systems from different manufacturers, and currents of up to 100 A can be measured at a frequency of up to several 100 kHz. Depending on the magnetic core material, the behavior of current transformers can be strongly nonlinear as the core losses, but also the permeability, vary with frequency and amplitude of the measured current. The insertion impedance also depends on the given magnetic core material.

Another major type of current transformer is the Rogowski coil, i.e. a high-impedance terminated current transformer with an air core coil placed around a conductor carrying the measured current. The voltage induced in the coil according to Faraday's law is proportional to the derivative of the measured current. Commercial Rogowski coil sensors feature an integrator so that the sensor output is proportional to the measured current. In practice, the integrator is limited to a minimal frequency of a few Hz to a few tens of Hz because of drift and offset issues. Compared to other current sensors, the coupling between the measured current and the sensor is weak, and it is possible to isolate the sensor entirely from the conductor potential. Therefore, Rogowski Coils can be designed for the measurement of very high currents and high bias voltages up to measured current frequencies of several tens of MHz. However, even with very small coils, self-resonance limits the maximum bandwidth

of Rogowski coil current sensors to approximately 50 MHz in commercial products as of to date.

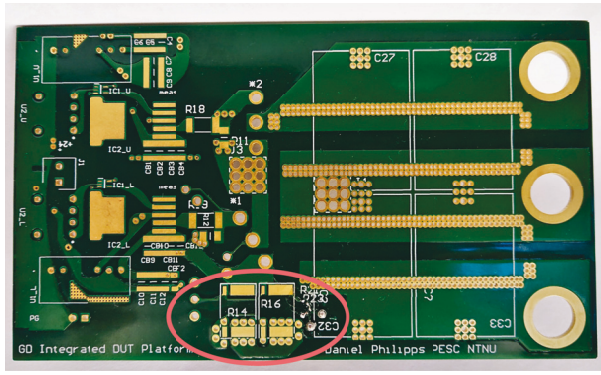
Current Viewing Resistors (CVRs) transform a current into a voltage signal, adhering to Ohm's law. The measured current causes ohmic losses in a CVR, therefore, all CVRs are limited by their maximum pulsed energy and continuous power dissipation capability. Coaxial and Surface Mount Device (SMD) variants are considered in this work. Figure 7.1 contains the maximum continuous current limit for this purpose. Coaxial CVRs have a comparatively low insertion inductance and are available with high bandwidths. SMD CVRs promise a small insertion impedance because of their small size, but a bandwidth specification is seldom given for these current sensors. Neither coaxial nor SMD CVRs are specified with respect to flatness or linearity by the manufacturer.

Current Clamps or also referred to as current probes, are a combination of a hall-effect sensor and a current transformer. In the presence of a magnetic field, the varying degree of diversion between electrons and holes in a semiconductor that conducts an auxiliary current, leads to an electric field that is perpendicular to the auxiliary current direction. This voltage is proportional to the strength of the magnetic field and can therefore be used to measure a current causing that magnetic field. As the semiconductor charge carrier dynamics are limited, this sensor type cannot detect high frequency measured currents. A suitable filter system combines the hall-effect sensor signal with the current transformer signal and thereby creates a high-bandwidth current sensor. The maximum current is limited by the hall-effect sensor, since the maximum diversion of charge carriers is dictated by the physical dimensions of the semiconductor plate. In addition, the current transformer core and termination resistor exclude measuring very high currents. However, the maximum current is largely dependent on the sensor bandwidth. The bandwidth of current clamps is typically limited below 150 MHz. The insertion impedance of current clamps is partly inductive and partly resistive, and highly frequency dependent. A rough estimate is given in the manufacturer datasheet.

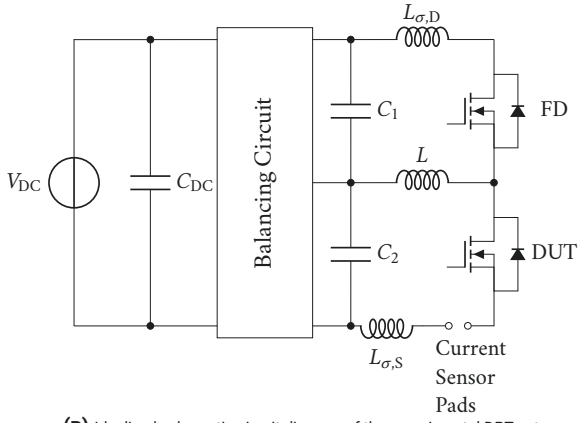
7.3 Current Sensor Performance Evaluation Method

As demonstrated above, multiple current sensor technologies are available commercially. However, the available information is insufficient to check if a particular current sensor meets the previously defined requirements in applications that involve fast-switching SiC power MOSFETs.

Therefore, a two-step performance evaluation method is proposed in this work. This method enables an extensive assessment of bandwidth, flatness,



(A) PCB without components. Current sensor SMD pads with injection network (right, SMA connector on the bottom side) in red ellipsoid.



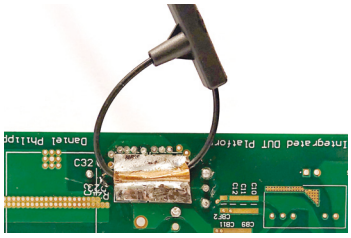
(B) Idealized schematic circuit diagram of the experimental DPT setup

Figure 7.2. Low-Inductive Test Platform

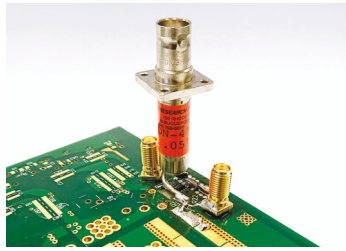
linearity, and insertion impedance of current sensors carrying both low and high currents. The low current analysis is carried out by means of a VNA, and for the high current measurements, a DPT is conducted using fast-switching SiC power MOSFETs.

7.3.1 Test Environment

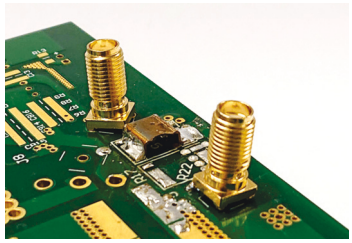
A prerequisite for applying the proposed current sensor performance evaluation method is a suitable circuit on which the current sensors under investigation can be placed. For this purpose, a Low-Inductive Test Platform (LITP) for the dynamic characterization of SiC power MOSFETs in a TO-247-3 housing was used in this work. The LITP features pads for the connection of various



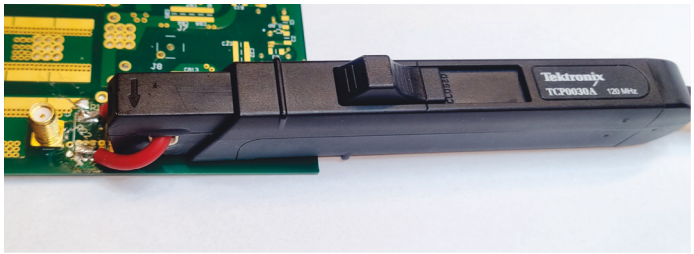
(A) LITP with CWTUM miniHF on top layer



(B) LITP with SDN-414-05 coaxial CVR on bottom layer



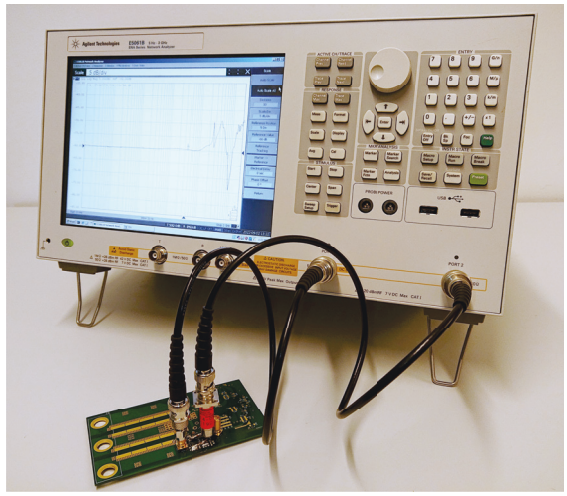
(C) LITP with SMD CVR on bottom layer



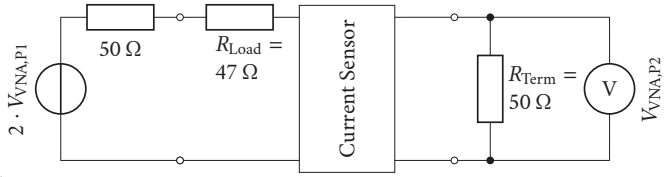
(D) LITP with TCP0030A current clamp on bottom layer

FIGURE 7.3. Current sensors mounted on top or bottom layer of LITP

current sensors, as well as coaxial ports for the injection and extraction of test signals. The LITP was previously presented in literature [29]. With a very low layout related commutation loop inductance of approximately 7.5 nH, the LITP enables highly accurate characterization measurements. A picture of the unpopulated LITP Printed Circuit Board (PCB) and a schematic circuit diagram are shown in Figure 7.2. In the red ellipsoid of 7.2b, the multipurpose current sensor pads can be identified. In addition, an impedance network for signal injection is located next to the pads for an SMA connector on the right of the ellipsoid. Figure 7.3 shows the current sensors under investigation assembled on the LITP PCB, mounted on either the bottom or the top side of the PCB.

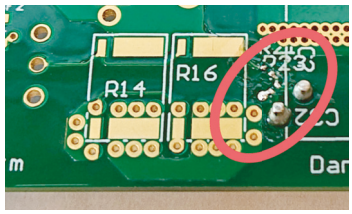


(A) Experimental Setup for S21 transmission coefficient analysis with a VNA (Keysight E5061B). Exemplary LITP PCB with coaxial CVR.

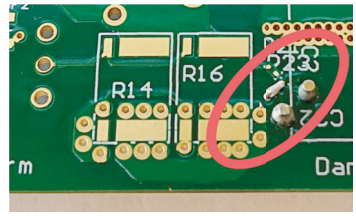


(B) Idealized schematic diagram of the experimental VNA setup for transmission coefficient analysis

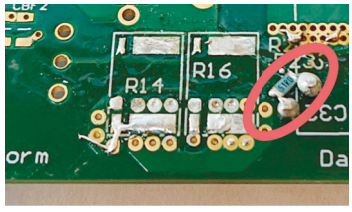
Figure 7.4. Transmission Coefficient Analysis



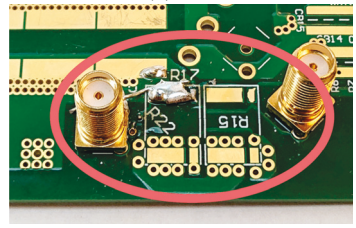
(A) Open



(B) Short



(C) 51 Ω Load



(D) Thru

Figure 7.5. Calibration fixture detail photos. The region displayed equals roughly the area enclosed by the red ellipsoid in 7.2a.

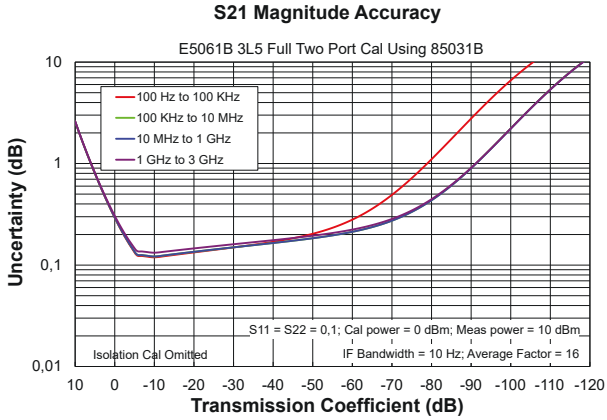


FIGURE 7.6. VNA (Keysight E5061B) uncertainty in a scenario similar to the application in this work. Created with a tool provided by the manufacturer.

7.3.2 *Transmission Coefficient Analysis*

The aforementioned impedance network is used in the small-signal transmission coefficient analysis. Using a Keysight E5061B VNA, the S21 S-parameter is measured. Appendix Section 7.7 contains supplementary information on S-parameters. A picture of the S21 measurement test setup and an idealized schematic circuit diagram are found in Figure 7.4.

A high accuracy voltage source inside the VNA generates a sinusoidal voltage with an amplitude of $2 \cdot V_{\mathrm{VNA,P1}}$ and a constant but configurable amplitude and variable frequency. The signal passes through a source resistor with the system impedance of 50 Ω, to the output port, P1. The current sensors are connected in series with a 47 Ω resistor to achieve impedance matching. The output of the current sensor is connected to port P2 of the VNA. Inside the VNA, a 50 Ω termination resistor is connected in parallel with the measurement unit of $V_{\mathrm{VNA,P2}}$. As described further in Subsection 7.7.1 of the Appendix, S21, is calculated as:

$$S21 = 10\,\mathrm{dB} \cdot \log \frac{P_{\mathrm{VNA,\,P2}}}{P_{\mathrm{VNA,\,P1}}}. \tag{7.2}$$

It must be noted that in most VNAs, the power measurement is achieved by measuring the voltage across the high precision termination resistor. The voltage is filtered, such that only the output signal component with the same frequency as the injected signal is taken into account. In addition, the characterization is conducted at a constant input power level. Hence, this VNA is not suitable for identifying nonlinear distortion, i.e. amplitude-dependent

transmission behavior or the introduction of output signal components at frequencies that are not already present at the input.

To compensate for the influence of the coaxial cables connecting the test fixtures to the VNA, a calibration must be performed before the measurements are taken. A 4-step calibration procedure for the VNA was followed; the steps being Open, Short, Load, Thru calibration. Each of these steps requires one calibration fixture. These calibration fixtures consist of a LITP PCB with SMA connectors at the injection and measurement signal ports. No other components are present in case of the Open, only a soldered short for the Short, only a 51 Ω resistor for the Load and only a wire connection between the two SMA connectors for the Thru calibration fixture. Figure 7.5a shows the Force port configuration for calibrating an Open, Figure 7.5b for calibrating a Short, and Figure 7.5c for calibrating a 50 Ω load. The calibration fixtures were characterized with a high precision VNA and the coefficients of a standard calibration fixture model were calculated. The parameters of this model are given in Table 7.4 in the Appendix. With the calibration fixtures in place, the Keysight E5061B VNA was configured to compensate for the influence of the coaxial cabling as well as the required adapters on the S21 measurements. As the VNA is a non-ideal instrument, it introduces a degree of uncertainty that can be quantified with a tool published by the manufacturer. The amplitude and frequency dependent uncertainty is plotted in Figure 7.6.

The small-signal transmission analysis can be used to estimate the flatness and bandwidth of the sensor under investigation. High signal amplitudes are not accounted for in this part of this work because neither a signal amplifier nor a bias circuit were used. The power level was limited to a maximum output power of 10 dBm, i.e. 10 mW resulting in a Root-Mean-Square (RMS) current of 14.14 mA. The frequency range for the S21 measurements was set to 100 Hz to 2 GHz.

7.3.3 *Time Domain Measurements*

In applications such as dynamic characterization of SiC power MOSFETs, significantly higher currents are measured than in the small signal transmission coefficient analysis. Nonlinear effects that might only occur with high magnetic fields caused by the measured current. Therefore, to complement the small-signal transmission coefficient analysis, DPTs were executed with a Wolfspeed C3M0075120D SiC power MOSFET, rated for 1.2 kV and 30 A. The DPTs were conducted with a test voltage of 800 V and a test current of 27 A. Apart from the sensor output signals, the drain-source voltage across the SiC power MOSFET was measured. The measurements were recorded with

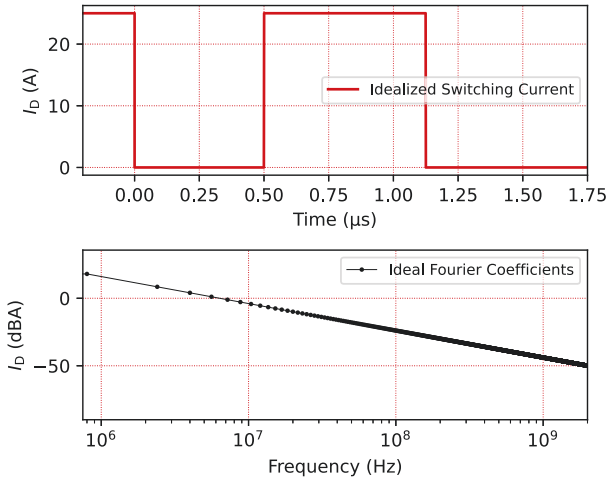


Figure 7.7. Idealized current waveform and resulting reference Fourier coefficients

a Tektronix DPO5104B oscilloscope. For the drain-source voltage measurement, a Keysight 10076C passive high voltage probe was used. To investigate interactions between sensors as well as insertion impedance effects, the PEM CWTUM miniHF 3 Rogowski Coil current sensor is used for reference measurements, as it can be inserted simultaneously with every other current sensor under investigation.

7.3.4 *Frequency Domain Transform of Measurements*

To evaluate the frequency dependent transmission behavior of the investigated sensors when measuring a high current, the Fast Fourier Transform (FFT) algorithm was applied to the measurement data. The time domain signals were reduced to the second pulse of the DPT, using the time interval $0.25\,\mu s \leq t \leq 1.5\,\mu s$ with a duration of $1.25\,\mu s$. This translates to a minimum frequency of 800 kHz. Furthermore, the oscilloscope uses a sampling rate of 5 Gs/s on each oscilloscope channel, resulting in a sampling step of 200 ps. To avoid aliasing, the oscilloscope applies low-pass filtering with a variable corner frequency that depends on the probe attached to it, but that is never higher than 1 GHz. The frequency limits were chosen to be 800 kHz and 2 GHz.

Figure 7.7 shows an idealized square wave current. Applying a Fourier analysis to this square wave current results in non-zero uneven Fourier coeffcients. The magnitude of these Fourier coefficients is also shown in Figure 7.7 and serves as an ideal reference for the current sensor measurements in the

frequency domain.

7.4 Experimental Results

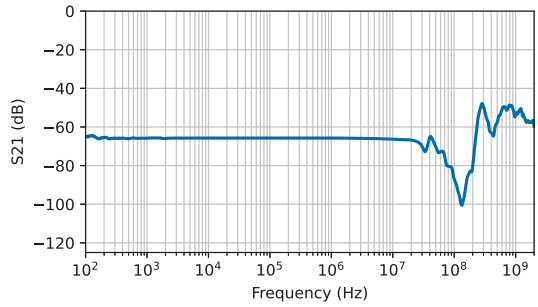
7.4.1 *Transmission Coefficient Analysis*

Figure 7.8 shows the VNA measurement results using the CWTUM miniHF3 Rogowski Coil Current Sensor, the SDN-414-05 coaxial CVR, ad the CSS4J-4026-1L00x SMD CVR. In addition, Figure 7.8d displays a measurement of the VNA with disconnected ports 1 and 2. This experiment shows the noise floor of the instrument, that is highly frequency dependent. The noise floor is approximately −130 dB below 20 MHz, and −70 dB above 200 MHz with a transition within the decade between 20 MHz and 200 MHz. The measurements conducted in this work are all significantly above the noise floor of the instrument, so the measurement results are regarded accurate.

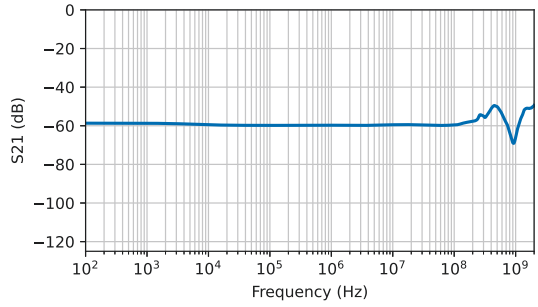
CWTUM miniHF 3 Rogowski Coil

A picture of the CWTUM miniHF 3 Rogowski Coil assembled on the LITP is shown in Figure 7.3a. A Rogowski Coil on its own is a magnetic field change detector, as described earlier. To obtain the actual current value, the output signal of a Rogowski Coil must be integrated. The CWTUM miniHF 3 current sensors is a Rogowski Coil paired with an analog integrator. Therefore, its output is proportional to the measured current in the ideal case, similar to a CVR. In reality, Rogowski Coil type sensors have a limited minimum measurable frequency that ranges between 5 Hz and 10 Hz as has been discussed earlier. For the application in this work, however, this is not a limitation, as all measurement signals have a higher than 5.6 kHz according to Equation 7.13 in the Appendix.

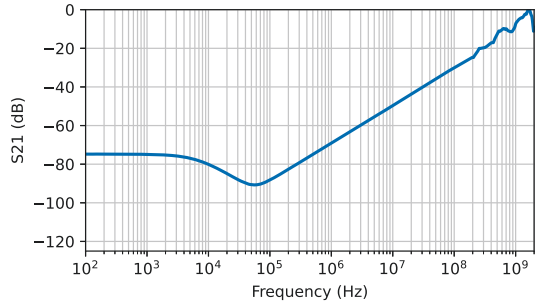
As can be seen in Figure 7.8a, the CWTUM miniHF 3 sensor exhibits a constant transmission coefficient close to the ideal value of −66 dB according to Equation 7.10 at low frequencies. The bandwidth specification of this sensor is 30 MHz. The corner frequency is observed at a little over 35 MHz, implying a conservative manufacturer specification. Strong damping immediately above 35 MHz indicates effective filtering in the integrator stage. At high frequencies, however, the excitation signal penetrates the integrator stage, leading to selective amplification of some high frequencies, and damping of others. When using the CWTUM miniHF 3 therefore, it is recommended to apply additional low-pass filters to obtain reliable measurement data.



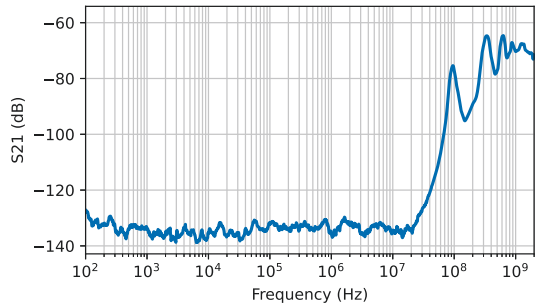
(A) CWTUM miniHF 3 Rogowski Coil



(B) SDN-414-05 Coaxial CVR



(C) Bourns CSS4J-4026R-1L00x SMD CVR ($1\ \mathrm{m\Omega}$)



(D) Insulated Port Reference

FIGURE 7.8. S21 Transmission coefficients of the current sensors under investigation

SDN-414-05 Coaxial CVR

A picture of the LITP with an SDN-414-05 coaxial CVR assembled on it can be seen in Figure 7.3b. The manufacturer has supplied a calibration statement with a high-accuracy resistance measurement, giving a resistance value of 51.19 mΩ. The bandwidth specification of the coaxial CVR is 2 GHz. If the coaxial CVR acted as an ideal low-pass filter, a frequency-independent transmission coefficient of −60 dB would be expected according to Equation 7.8 up to its corner frequency of 2 GHz. The transmission coefficient measurement result is visualized in Figure 7.8b and shows a deviating behavior. For frequencies below 100 MHz, the transmission coefficient is almost ideally flat. At around 300 MHz, a resonance occurs, and for frequencies above 300 MHz, the transmission behavior swings between amplification and damping.

CSS4J-4026R-1L00x SMD CVR (1 mΩ)

According to Equation 7.9 in the Appendix, the expectation of an ideal shunt resistor with a resistance of 1 mΩ would be a steady transmission coefficient of -94 dB. However, the transmission coefficient measurement shows very different behavior. For frequencies above 70 kHz, the large sensor inductance leads to a differentiating behavior with an output signal increase of 20 dB/decade. For frequencies below 50 kHz and above 6 kHz, the inductance in the signal feed path leads to a signal drop of about 20 dB/decade. For signals in the range of 50 kHz and 70 kHz, a transition between these two behaviors can be observed, with a minimum of approximately the ideal transmission coefficient of −94 dB. For very low frequencies, the output signal is proportional to the input signal, with a transmission factor of approximately −75 dB.

This measurement shows a major limitation of the transmission coefficient analysis. If the sensor is small compared to the test fixture, the feeding traces introduce a big series inductance, which leads to a distorted sensor characteristic. However, the high current path on the LITP does not lead through this large feeding inductance. Thus, the low frequency behavior is expected to differ from the small signal transmission coefficients. Nevertheless, the differentiating behavior caused by the SMD CVR inductance would require complicated filtering and an integrator to obtain the current value. The output signal levels are much higher than the output signal levels of all other sensors. This makes the design of an integrator and filtering circuits challenging with respect to overloading and input protection.

Table 7.1. Drain-Source Voltage Overshoot at Turn-off and Drop at Turn-on for the Sensors under Investigation

Current Sensor	$V_{\text{Overshoot}}$	V_{Drop}
CWTUM miniHF 3 Rogowski Coil	100 V	70 V
SDN-414-05 Coaxial CVR	130 V	95 V
CSS4J-4026R-1L00x SMD CVR	103 V	80 V
TCP0030A Current Clamp	164 V	133 V

TCP0030A Current Clamp

The TCP0030A current clamp sensor, seen in Figure 7.3d, uses a proprietary interface that is not compatible with the VNA used in this work. Therefore, a small-signal transmission coefficient analysis was not possible.

7.4.2 *Power Measurement Analysis*

The DPT experiment results are presented in both the time and the frequency domain to identify possibly nonlinear behavior. For each current sensor, except for the Rogowski Coil, two figures illustrate the measurement results.

The first figure consists of three parts. First, the drain-source voltage, V_{DS}, measurement is shown in the time domain. The voltage overshoot at turn-off and the voltage drop at turn-on are an indication of the insertion inductance. Both a larger overshoot voltage and a larger voltage drop are caused by a larger insertion impedance. In addition to the respective figures, the voltage overshoot and drop values are summarized in Table Table 7.1. Below the V_{DS} graph, the current sensor output is plotted in the time domain in the second graph. For a common reference, the output signal of the Rogowski Coil experiment is copied to each of the time domain plots. Finally, a third graph depicts the FFT of the current sensor output. In the case of the SMD CVR, there are two additional graphs that show the integrated sensor output signal and the FFT of this integrated signal, for reasons that will be explained later on.

The second figure consists of two parts. To identify the insertion effect of the coaxial CVR, the current clamp, and the SMD CVR, the Rogowski Coil was connected in series to each of these current sensors. Comparing the Rogowski Coil output signal with and without the sensor allows identifying the effects that the insertion of the current sensor has. Therefore, for each sensor except for the Rogowski Coil itself, a second figure shows the sensor output signal in the time domain in the upper graph and its FFT in the lower graph.

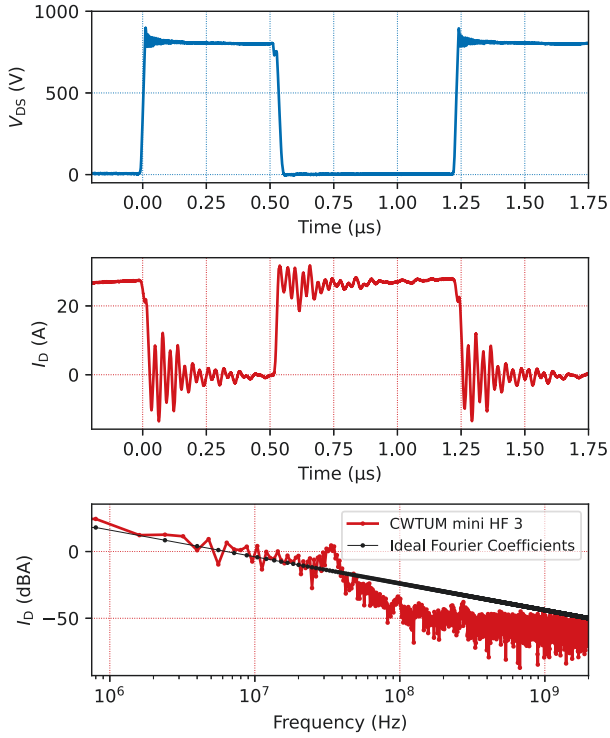


Figure 7.9. CWTUM miniHF 3 Rogowski Coil Power Measurements Reference

CWTUM miniHF 3 Rogowski Coil

The DPT experiment results are shown in Figure 7.9. The sensor was attached to the oscilloscope with a 50 Ω RG58 coaxial cable. The internal 50 Ω termination resistor of the oscilloscope was activated for the measurement. With this configuration, the oscilloscope employs low-pass filtering with a corner frequency of 1 GHz.

The voltage overshoot measured with this arrangement is the smallest among all tested assemblies. This indicates that it has the smallest insertion inductance into the power loop. The current trajectory is characterized by very strong oscillations that can be clearly identified in the frequency domain plot in Figure 7.9. The main oscillation frequency is located at 35 MHz, which is the corner frequency of this sensor according to the observations in 7.4.1. Beyond this limit, the frequency content of the current sensor output signal is reduced significantly below the reference Fourier coefficients. Despite the strongly reduced signal magnitudes above 35 MHz, there are signal components that are clearly above noise level (−50 dB A), one at approximately 100 MHz, another at 140 MHz and generally elevated signal levels between 200 MHz and 300 MHz. In the transmission coefficient analysis in 7.4.1, an elevated and strongly frequency dependent transmission behavior could be observed in the frequency range between 200 MHz and 300 MHz. Taking into account, that no low-pass filter was employed to suppress this transmission range of the sensor, the signal components in this frequency range should be regarded with care.

At frequencies above approximately 300 MHz, the FFT yields nearly constant results that have a magnitude of approximately −50 dB A or lower. This contribution to the measurement data originates from measurement noise that is introduced by the oscilloscope. Above a sensor specific frequency value, this effect can be observed for every sensor in this investigation. The maximum frequency, above which this effect becomes visible, is located at the maximum oscilloscope low-pass filter corner frequency of 1 GHz.

SDN-414-05 Coaxial CVR

The SDN-414-05 coaxial CVR is connected to the oscilloscope using a 50 Ω RG58 coaxial cable. The internal 50 Ω termination resistor of the oscilloscope is activated. Therefore, the oscilloscope applies a 1 GHz low-pass filter.

The voltage overshoot at turn-off and drop at turn-on observed in Figure 7.10 are increased compared to the experiment with the Rogowski Coil alone (7.4.2). This is caused by the higher inductance in the source path of the lower switch due to the leads of the coaxial CVR. The insertion impedance of a similar coaxial CVR, the SDN-414-025, has been characterized by means of an impedance analyzer between 1 kHz and 120 MHz in an earlier work [34; 35].

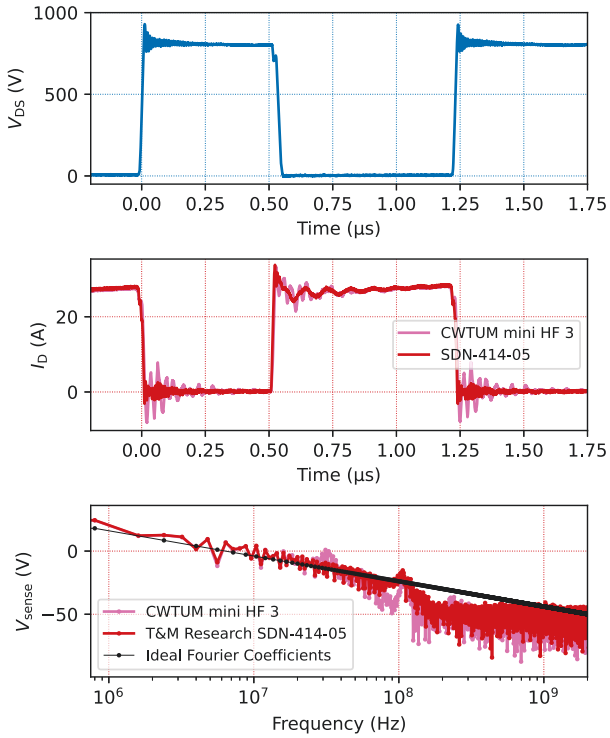


Figure 7.10. SDN-414-05 Coaxial CVR Power Measurements

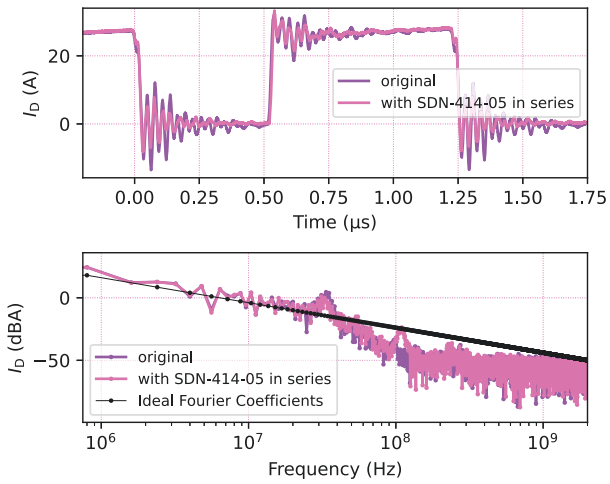


Figure 7.11. SDN-414-05 Coaxial CVR insertion effect on power measurements with CWTUM miniHF 3 Rogowski Coil

It was found that the insertion impedance is mostly inductive. Approximately 5 nH are added into the commutation loop by the coaxial CVR. While the inductive component of the insertion impedance only shows a slight frequency dependency, the trajectory of the resistive component indicates a resonance at a frequency outside the measured range, but close to its boundary, judging by the steepness of the resistance trajectory. The impedance measurement result was therefore reproduced in the measurements above and highlights an important finding of this work. The circuit environment of a sensor and its connection strategy have a notable impact on its behavior, possibly significantly limiting its bandwidth, flatness, and linearity.

The current trajectories using the Rogowski Coil with and without the SDN-414-05 coaxial CVR are shown in Figure 7.11. Especially, the main oscillation mode of the Rogowski Coil at approximately 35 MHz is visibly damped. This damping can be explained by the resistive insertion impedance component of the coaxial CVR.

The output of the coaxial CVR shows significantly lower oscillation magnitudes and higher oscillation frequencies than the Rogowski Coil. The coaxial CVR output signal exhibits large oscillation magnitudes, especially at the frequency range between 100 MHz and 120 MHz. From Figure 7.11, it becomes clear that these components are not only present in the coaxial CVR but also the Rogowski Coil output signal. In addition, the associated magnitude is significantly larger than in the original Rogowski Coil experiment in 7.4.2. Taking into account that the Rogowski Coil exhibits considerable damping above 35 MHz, this indicates a significant signal component of the measured current at frequencies between 100 MHz and 120 MHz.

CSS4J-4026R-1L00x SMD CVR

The SMD CVR has four terminals in the form of soldering pads, two wide terminals for leading the measured current, and two narrow terminals for connecting the CVR to measurement hardware. On the LITP, the measurement terminals are connected to an SMA socket (Figure 7.3c). A 50 Ω RG58 cable is used to connect the sensor output to the oscilloscope. The internal 50 Ω termination resistor is activated and thus, the applied low-pass corner frequency is 1 GHz. Following the transmission coefficient analysis, it was expected that the output voltage of this sensor might be very large due to its strongly inductive behavior. This results into a considerable voltage component that is proportional to the very high current changing rate di/dt of the fast switching SiC MOSFETs. Hence, a 20 dB attenuator was used to lower the signal amplitudes.

The insertion inductance of this sensor is only slightly larger than the original Rogowski Coil experiment, as can be seen by examining the drain-

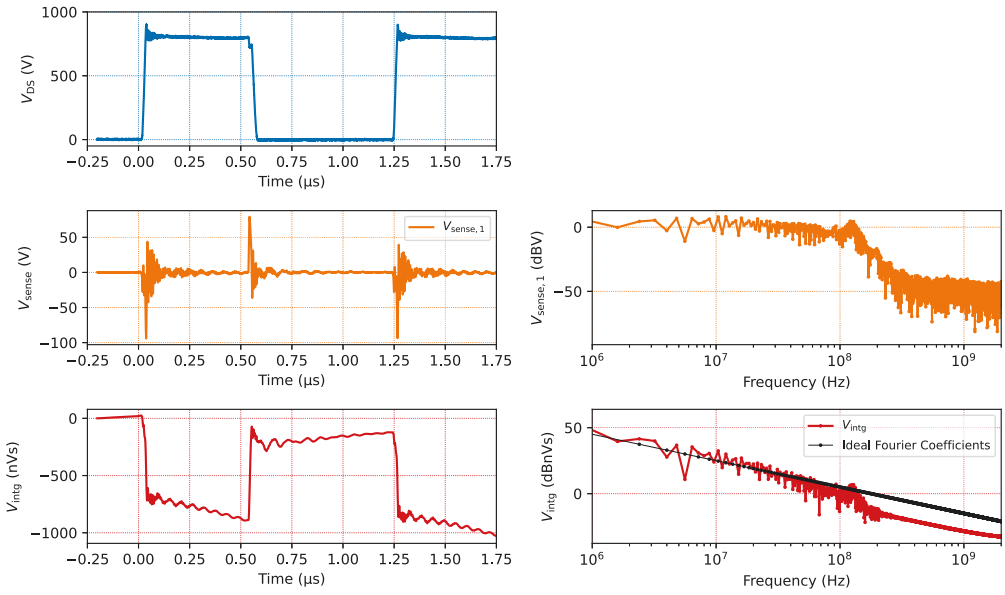


Figure 7.12. Bourns CSS4J-4026R-1L00x SMD CVR Power Measurements

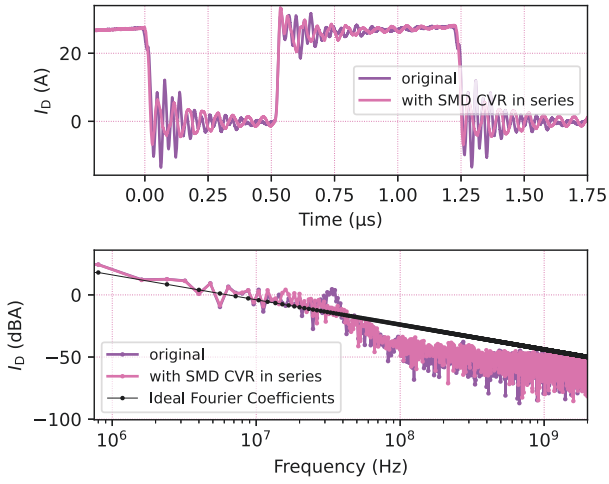


Figure 7.13. Bourns CSS4J-4026R-1L00x SMD CVR insertion effect on power measurements with CWTUM miniHF 3 Rogowski Coil

source voltage waveform in Figure 7.12. Both voltage overshoot at turn-off and voltage drop at turn-on are about the same as in the first experiment in 7.4.2 as can be seen in Table 7.1. The current sensor output shown in Figure 7.12 confirms that this sensor has a complex frequency dependent transmission behavior. The large voltage spikes at the switching instances are caused by the sensor inductance that leads to differentiating behavior. In addition, high frequency oscillations with large magnitudes can be observed in the current sensor output signal, especially, between 100 MHz and 120 MHz. A simple digital integration result is shown on the bottom left of Figure 7.12. The offset issues of the oscilloscope are clearly present in the integration result.

Apart from this, the SMD CVR has an output signal component that is proportional to the current, which is oriented against the specific offset error of the oscilloscope during the second on-pulse of the DPT. This results in a less severe offset error at the second turn-off, which can be observed in Figure 7.12, where the signal level at the second turn-on and the second turn-off instant are almost identical. It is coincidence that the sensor output signal component that is proportional to the load current is exactly as large as the oscilloscope offset, and this cannot normally be expected. On the contrary, this emphasizes the need for elaborate filtering to enable reliable measurement results from this current sensor. Transforming the integration result into the frequency domain yields an almost ideal frequency trajectory up to a frequency of approximately 130 MHz. Beyond 130 MHz, the signal quickly drops below the reference. As in the case of the coaxial CVR, a large signal component located between 100 MHz and 120 MHz can be measured.

As can be observed in Figure 7.13, the insertion of the SMD CVR leads to damping of the main oscillation mode at 35 MHz. The magnitude of lower frequency signal components is increased. Therefore, a down-shift in oscillation frequency can be observed in the Rogowski Coil time domain plot in Figure 7.13. Apart from that, no significant insertion effects can be observed.

TCP0030A Current Clamp

The TCP0030A Current Clamp is assembled on the LITP by attaching a wire loop between the current sensor pads. The proprietary sensor interface provides both filtering and probe termination. A low-pass filter with a corner frequency of 120 MHz is employed by the oscilloscope. However, the type and shape of this filter remain unknown.

The wire loop and the sensor itself add inductance in the commutation loop of the load current, resulting in a higher voltage overshoot at turn-off, as can be seen in Figure 7.14. In addition, a larger voltage drop can be observed during turn-on, which also originates from the higher commutation loop inductance.

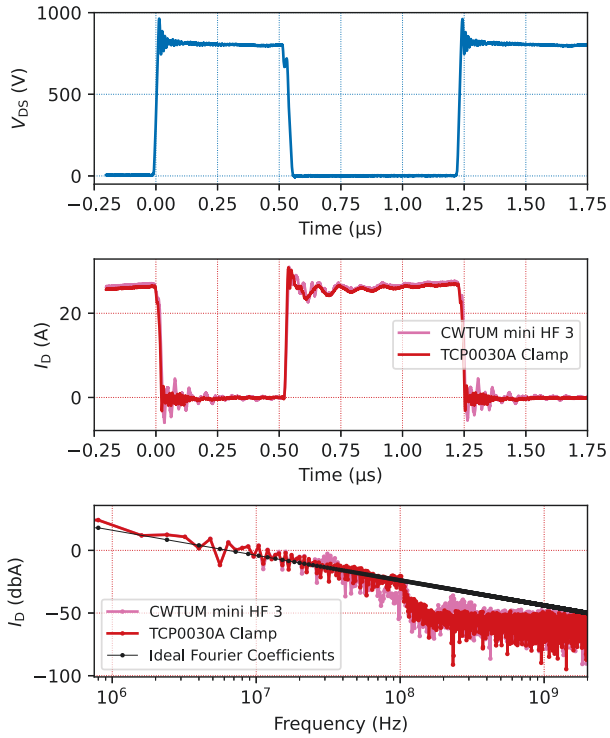


Figure 7.14. TCP0030A Current Clamp Power Measurements

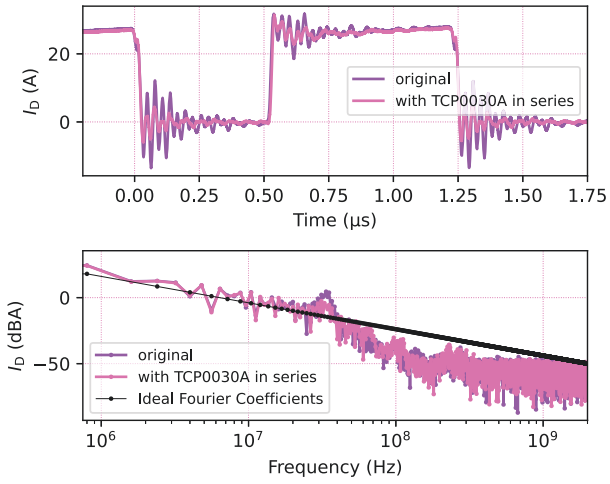


Figure 7.15. TCP0030A Current Clamp insertion effect on power measurements with CWTUM miniHF 3 Rogowski Coil

The extent of the influence of the insertion inductance on the drain-source voltage is comparable to the coaxial CVR experiments described in 7.4.2.

The Rogowski Coil measurements of the two experiments with and without the current clamp are shown in comparison to each other in Figure 7.15. It becomes clear that oscillations in the measurement result are strongly reduced, similar to the coaxial CVR experiment. However, the damping is significantly stronger using the current clamp, which is explained by the larger resistive insertion impedance component that is stated in the datasheet [36].

The time domain current plot in Figure 7.14 shows that besides the lower oscillation magnitude, the oscillation frequency in the current clamp output signal is higher than in the Rogowski Coil output signal immediately succeeding the switching transitions. The frequency domain plot in Figure 7.14 confirms this observation. While, comparably to the experiment in Figure 7.4.2, the frequency content of the Rogowski Coil output is reduced above 35 MHz, the current clamp output signal follows the ideal reference approximately up to 120 MHz, and then quickly drops to the oscilloscope noise floor (≈ -50 dB). This indicates a flat transmission behavior of the TCP0030A current clamp up to its bandwidth specification that coincides with the low-pass filter corner frequency of 120 MHz.

7.5 Discussion

7.5.1 Current Sensors

Both the transmission coefficient analysis and the DPT experiment results support that the SDN-414-05 coaxial CVR is a suitable current sensor for dynamic characterization of discrete SiC power MOSFET. It offers both a flat and high bandwidth frequency domain response. The TCP0030A current clamp could not be evaluated with a VNA because it has a proprietary sensor interface. In DPT experiments, the TCP0030A yields high quality current measurements that are very similar to measurements using the SDN-414-05 coaxial CVR. A drawback of the two sensors is their insertion impedance that contains a significant resistive and inductive component. This resistive component damps oscillations in the measured current, which can be seen as a falsification, as it understates the potential for causing Electromagnetic Interference (EMI). Apart from that, both sensors can withstand only limited currents, as shown in Subsection 7.9.1 and Subsection 7.9.3 in the Appendix. This limits the usage for characterization of high current MOSFETs, especially MOSFET power modules, and long-term tests or current control sensors in DC/DC converters.

The CWTUM miniHF 3 Rogowski Coil has the smallest insertion impedance

of the investigated alternatives. The bandwidth of 30 MHz is the main limitation of this sensor. Applying an external low-pass filter according to this specification is reasonable, taking into account that strong oscillations at a frequency of approximately 35 MHz are observed in the sensor output when measuring high currents. For no other sensor, oscillations are present at this frequency, which points to an internal resonance phenomenon. This can be seen as a falsification and wrong representation of the 35 MHz signal component. In addition, this leads to suppression of higher frequency signal components that can be identified with other current sensors. The CWTUM miniHF 3 is limited to a maximum current amplitude of 120 A. However, the same model is available with a smaller sensitivity for higher measured currents. It is expected that the transmission characteristics are similar to the individual studied in this work. Hence, measurement of high currents is not a limitation with this sensor.

The SMD CVR presents a complicated case. Its robustness and small size make it an excellent candidate for integrated current measurements. However, its transmission behavior is strongly frequency dependent, albeit independent of the current amplitude. Designing a filter system would be challenging due to the high dynamic range of the sensor output signal. However, given that the differentiating behavior of the sensor reaches up to very high frequencies without strong deviations from an ideal differentiator trajectory, developing a suitable filter might enable a high bandwidth sensor system. Overall, the SMD CVR is regarded to be more suitable for low frequency current measurement like supply current measurement or potentially inductor current measurement in combination with a filter to suppress oscillations. The manufacturer includes information about the maximum pulsed power from which the maximum pulsed current can be calculated. A pulse duration of 100 µs results in a maximum pulse current of more than 1000 A. Therefore, the sensor can even withstand the current of very high power MOSFET modules in DPT experiments. Furthermore, the SMD CVR can withstand a maximum continuous current of 63 A according to Subsection 7.9.2 in the Appendix. This limit can be increased by parallelizing multiple SMD CVRs.

TABLE 7.2. Guidelines for application dependent sensor choice

Application	Switching Device	Challenges	Sensor Requirements	Suitable Sensor
Dynamic Characterization in Double Pulse Tests	Discrete MOSFETs	Very High Switching Speed	(Very) High Bandwidth High Linearity	coaxial CVR Current Clamp
	MOSFET Modules	High Switching Speed High Pulsed Current		coaxial CVR Rogowski Coil
Long Term Dynamic Characterization	Discrete MOSFETs	(Very) High Switching Speed	High Bandwidth	Current Clamp
	MOSFET Modules	High Continuous Current	High Linearity	Rogowski Coil
Integrated Current Measurement	MOSFET Modules	High Continuous Current Limited Space	Small Insertion Impedance (esp Resistance) Small Size Overcurrent Ruggedness Low Cost	SMD CVR
Overcurrent Detection	Discrete MOSFETs MOSFET Modules	High Continuous Current Large Overcurrent	Small Insertion Impedance (esp Resistance) High Reliability Overcurrent Ruggedness Low Cost	SMD CVR
EMI Detection	Discrete MOSFETs MOSFET Modules	High Continuous Current	Small Insertion Impedance (esp. Resistance) High Bandwidth Low Cost	SMD CVR
Converter Current Measurement	Discrete MOSFETs MOSFET Modules	High Continuous Current	Small Insertion Impedance (esp Resistance) High Reliability Small Cost	SMD CVR

7.5.2 Current Sensor Application

According to the findings discussed in the previous Subsection 7.5.1, the current sensors are suitable for different application scenarios.

The SDN-414-05 coaxial CVR is a good solution for short-term dynamic characterization of fast-switching discrete SiC power MOSFETs because of the flat and high bandwidth transmission behavior it provides. It can withstand high pulse currents and thus, DPT experiments do not overload this sensor, even with high maximum current values. For long-term tests, however, this coaxial CVR is not suitable because of its limited loss power dissipation capability. Equally, this sensor is not suitable for current control feedback for the same reason.

While high bandwidth current clamp sensors like the TCP0030A also provide a flat frequency response, the maximum current is limited more than coaxial CVRs. Hence, they can only be used with discrete SiC power MOSFETs at short-term test currents of up to 50 A, or continuous currents of up to 30 A. Considering this limitation and its high cost as well as the proprietary interface and physical size, this specific sensor is unsuitable for current control feedback.

The CWTUM miniHF 3 Rogowski Coil sensor is mostly limited in its bandwidth. However, it can be used with slower switching MOSFET power modules in both short- and long-term tests, if a bandwidth of 30 MHz is acceptable and a low-pass filter is applied to suppress the observed sensor resonance at 35 MHz. The high cost of this current sensor speaks against using it in a converter as current control feedback. However, custom integrated Rogowski Coil type current sensors are subject to research [22; 37] and might constitute a viable option for current control in inverters. For DC/DC converters, however, Rogowski Coils are less suitable for current control feedback, since low-frequency and DC current components cannot be captured.

SMD CVRs have a great potential for integration because of low device cost, small size and small insertion impedance. Besides, SMD CVRs can withstand very high current pulses without damage in, for example, fault conditions. Since they behave linearly even at high currents, overcurrents do not present a reliability issue and can be successfully identified. Either analog or digital post-processing is required, but such hardware can be placed at a distance from the sensor. Without such post-processing, SMD CVRs act as differentiators and are therefore well suited to measure high frequency current components that can lead to EMI issues. For low frequencies, the SMD CVR output signal is proportional to the measured current. Therefore, this sensor is very well usable for converter current measurement at low frequencies, combining low cost, no lower frequency boundary, high current carrying capability, and ruggedness resulting in high reliability. Another challenge with CVRs in general that has

not been addressed in this work is that they do not offer galvanic isolation. This complicates the measurement because the CVR must be placed in an advantageous position that shares the same ground as the measurement hardware, or suitable measurement hardware isolated from the converter ground. If the loss power generated by the CVR is acceptable in regard to efficiency and the common mode issue can be overcome, SMD CVRs are a viable option for current control. At least a low-pass filter with a steep roll-off is needed for current control feedback to suppress the strongly differentiating behavior of the sensor at high frequencies. In addition, if very high voltage peaks as a result of steep current slopes are to be expected, the signal processing hardware input must be protected by a fast limiting device or an attenuator.

Table 7.2 lists current sensor application scenarios, the specific challenges, what requirements are imposed for current sensors, and finally current sensors that can fulfill these requirements.

7.5.3 Method Review

The transmission coefficient analysis conducted with a VNA enables precise characterization of current sensors at small signal levels and over a large range of signal frequencies. It is helpful to estimate the bandwidth of a sensor and the flatness of its frequency response. Since it is possible to characterize cascaded systems with this approach, it is possible to perform filter system verification. The drawback of this analysis is that it requires expensive and specialized hardware. A VNA is needed for performing the measurements, and the use of calibration fixtures is advisable to achieve high measurement accuracy and precision. For the characterization of custom calibration fixtures, another very high accuracy VNA is required. Moreover, nonlinear effects cannot be identified with a VNA.

Conducting DPT experiments meaningfully complements the transmission coefficient analysis at small signal level with a VNA. The exposure to magnetic fields with a high field strength changes the transmission behavior of some sensors due to nonlinear electromagnetic properties. Furthermore, the insertion impedance of a sensor can be judged directly by the impact it has on the measured current. These aspects are best studied under the conditions equivalent to the practical sensor application scenario. Transforming the sensor output to the frequency domain facilitates the comparison of various sensors. This frequency domain representation is another signal analysis perspective. Certain phenomena, like resonance and the superposition of signal components with varying frequency, for example, are much more easily identified in the frequency domain than in the time domain.

7.6 Conclusion

In this work, four high bandwidth current sensors have been comprehensively evaluated in the practical application context of a Low-Inductive Test Platform (LITP) for dynamic characterization of SiC power MOSFETs. The evaluation comprises transmission behavior in both time and frequency domain for both small-signal and large-signal currents, and the identification of insertion impedance effects.

A critical review of the method applied in this work has shown that a small-signal analysis with a VNA gives an overview of the sensor flatness and bandwidth, and is especially useful for filter development. To verify the sensor system, however, high-current experiments conducted in the actual application circuit environment of the sensor systems are necessary. These experiments show the impact of both the circuit environment and nonlinear electromagnetic sensor properties occurring because of high measured current levels.

The investigated sensors represent various sensor technologies and thus, this work gives a good overview of the choices a developer has for high-bandwidth high current measurement. Due to their different characteristics, all the investigated current sensors suit at least one application. Therefore, a list of sensor selection guidelines has been developed as an abstraction of the individual experiments based on the analysis results, which is of great usability for characterization and converter circuit designers.

Acknowledgement

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Appendix

Commercially Available Current Sensors

This table contains commercially available current sensors that were used to create Figure 7.1.

TABLE 7.3. Commercially available current sensors.

Sensor Type	Model	Pmax	Emax	Imax	Icontinuous	trise/Bandwidth	Datasheet
Current Clamp	Tektronix TCP0030A				30 A	DC to 120MHz	https://www.tek.com/en/datasheet/30-ac-dc-current-probe
Current Clamp	HIOKI CLAMP ON PROBE 3275				500 A (RMS)	DC to 2 MHz	https://www.hioki.com/global/products/current-probes/wide-band/id_5988
Current Clamp	CLAMP ON PROBE 3274				150 A (RMS)	DC to 10 MHz	https://www.hioki.com/global/products/current-probes/wide-band/id_5957
Coaxial Current Viewing Resistor	TM research 1M-T10 (50mOhm)	20 W			20 A	1200 MHz	http://www.tandmresearch.com/index.php?mact=ListIt2Products,cntnt01,detail,0cntnt01item=series-mcntnt01template_summary=Sidecntnt01returnid=19
Coaxial Current Viewing Resistor	TM research SDN-414-05 (50mOhm)	2 W			6.3 A	2000 MHz	http://www.tandmresearch.com/index.php?mact=ListIt2Products,cntnt01,detail,0cntnt01item=series-sdn-414cntnt01template_summary=Sidecntnt01returnid=19
Coaxial Current Viewing Resistor	TM research R-700-1 (10mOhm)	225 W			150 A	800 MHz	http://www.tandmresearch.com/index.php?mact=ListIt2Products,cntnt01,detail,0cntnt01item=series-rcntnt01template_summary=Sidecntnt01returnid=19
Rogowski Coil	CWT Mini50HF			3 kA		50 MHz	http://www.pemuk.com/products/cwt-current-probe/cwtmini50hf.aspx
Rogowski Coil	CWT MiniHF			120 kA		30 MHz	http://www.pemuk.com/products/cwt-current-probe/cwt-minihf.aspx
Rogowski Coil	CWT			600 kA		16 MHz	http://www.pemuk.com/products/cwt-current-probe/cwt.aspx
Current Transformer	Würth Elektronik 7492540060			40 A		1 MHz	https://no.mouser.com/ProductDetail/Wurth-Elektronik/7492540060?qs=QNEnbhJQKvZ8MAUA%2Ft89JQ%3D%3D
Current Transformer	Triad Magnetics CST206-1A			110 A		250 kHz	https://no.mouser.com/ProductDetail/Triad-Magnetics/CST206-1A?qs=71qcunE5gOOEVhCtjpCDGw%3D%3D

TABLE 7.4. Calibration model parameters for Short fixture.

Short Model Parameter	Parameter Value	Open Model Parameter	Parameter Value	Load Model Parameter	Parameter Value	Thru Model Parameter	Parameter Value
fMax	4.2 GHz	fMax	2.2 GHz	fMax	1 GHz	fMax	600 MHz
Z0	51.59 Ohm	Z0	57.6 Ohm	Z0	53.57 Ohm	Z0	52.5 Ohm
L0	2.580x10^-11 H	C0	3.17786e-16 F				
L1	-1.418x10^-19 H	C1	-3.51177e-23 F				
L2	1.099x10^-28 H	C2	-4.36255e-32 F				
L3	-1.644x10^-38 H	C3	1.01158e-41 F				
Offset Delay	97.5 ps	Delay	99.6 ps	Delay	246 ps	Offset Delay	529 ps
Offset Loss	6.96 GOhm/s	Loss	9.80 GOhms/s	Loss	57.5 GOhms/s	Offset Loss	30.06 GOhm/s

TABLE 7.5. General Two-Port System Scattering Parameters

S-Parameter	Injection Port	Measurement Port	Description
S11	1	1	Reflected Power at Port 1
S21	1	2	Forward Transmission Coefficient
S12	2	1	Reverse Transmission Coefficient
S22	2	2	Reflected Power at Port 2

TABLE 7.6. Relative Delay Time Measurements

Sensor	Relative Delay Time Measurement	Current Sensor Type
Tektronix TPP1000	6.3 ns	Passive Voltage Probe
Keysight 10076C	9.6 ns	Passive Voltage Probe
CWTUM Mini HF 6	16.8 ns	Rogowski Coil (50 Ohm Termination)
CWTUM Mini HF 6	17.8 ns	Rogowski Coil (1 MOhm Termination)
T&M Research SDN-414-05	5 ns	Coaxial CVR
Tektronix TCP0030A	14.5 ns	Current Clamp (Automatic Termination)
Rogowski Tube Sensor	13.2 ns	di/dt Sensor with Digital Integration
Differential Rogowski Tube Sensor	20.7 ns	di/dt Sensor with Digital Integration

7.7 IDEAL TRANSMISSION COEFFICIENT CALCULATION

The definition of the transmission coefficient S21 is

$$S21 = 10\,\text{dB} \cdot \log \frac{P_{\text{VNA, P2}}}{P_{\text{VNA, P1}}}. \tag{7.3}$$

Therefore, for each sensor, this equation is solved.

7.7.1 *Current Viewing Resistors*

For both the coaxial CVR and the SMD CVR, the sensor is approximated by an ideal resistance for this calculation. The injected power can be used to

calculate the voltage across the fixture and thus a current through the sensor. This current results in a sensor voltage which is then picked up by the VNA, transferred into a power value again.

The fixture resistance at the port is chosen equal to the system resistance of $R_F = 50\,\Omega$ for maximum power transfer and to avoid reflection. Therefore, the injected current is

$$I_{CVR} = I_{VNA,P1} = \sqrt{\frac{P_{VNA,P1}}{R_F}}. \tag{7.4}$$

This current flows through the coaxial CVR and causes a sensor voltage across it, which is measured with port 2 of the VNA. Assuming an ideal resistance of 50 mΩ, this voltage is

$$V_{VNA,P2} = V_{CVR} = R_{CVR} \cdot I_{CVR} = R_{CVR} \cdot \sqrt{\frac{P_{VNA,P1}}{R_F}}. \tag{7.5}$$

The power delivered to port 2 of the VNA is

$$P_{VNA,\,P2} = \frac{V_{VNA,P2}^2}{R_F} = \frac{R_{CVR}^2}{R_F^2} \cdot P_{VNA,P1}. \tag{7.6}$$

Then, the transmission coefficient S21 is

$$S21 = 10\,\text{dB} \cdot \log \frac{P_{VNA,\,P2}}{P_{VNA,\,P1}} = 20\,\text{dB} \cdot \log_{10} \frac{R_{CVR}}{R_F}. \tag{7.7}$$

For an ideal resistance of 50 mΩ in case of the coaxial CVR, S21 equates to

$$S21_{\text{ideal, coax CVR}} = 20\,\text{dB} \cdot \log_{10} \frac{50\,\text{m}\Omega}{50\,\Omega} = -60\,\text{dB}, \tag{7.8}$$

and for an ideal resistance of 1 mΩ in case of the SMD CVR, S21 equates to

$$S21_{\text{ideal, SMD CVR}} = 20\,\text{dB} \cdot \log_{10} \frac{1\,\text{m}\Omega}{50\,\Omega} = -94\,\text{dB}. \tag{7.9}$$

7.7.2 CWTUM miniHF 3 Rogowski Coil

The Rogowski Coil of type CWTUM miniHF 3 was used in a version that supports a maximum current of 120 A. Its sensitivity is 50 mV/A if the termination resistance is 1 MΩ or higher. With a termination resistance of 50 Ω, the sensitivity drops to 50 mV/A. In this case, it is therefore equivalent to a CVR with a resistance of 25 mΩ.

Following Equation 7.7, S21 equates to

$$S21_{\text{ideal, CWTUM miniHF 3}} = 20\,\text{dB} \cdot \log_{10} \frac{25\,\text{m}\Omega}{50\,\Omega} \approx -66\,\text{dB}. \tag{7.10}$$

7.8 Double Pulse Test

7.8.1 Frequency Content

For the DPT experiments presented in this paper, an inductance of 110 µH, a voltage of 800 V and a maximum current of 30 A were used. Both the hold-off time between the first turn-off and the second turn-on instance, and the hold-on time between the second turn-on and the second turn-off instance, last 1.5 µs. Therefore, the longest time used in the experiments consists of the magnetization time and two times the hold-off time:

$$t_{\text{max}} = t_{\text{mag}} + t_{\text{hold off}} + t_{\text{hold on}} = t_{\text{mag}} + 2 \cdot t_{\text{hold off}} \tag{7.11}$$

With a magnetization time of $t_{\text{mag}} = 4.125\,\mu\text{s}$, Equation 7.11 results to $t_{\text{max}} = 7.125\,\mu\text{s}$. This translates into a lower frequency boundary of

$$f_{\text{min}} = \frac{1}{4 \cdot t_{\text{max}}} \approx 35\,\text{kHz}. \tag{7.12}$$

Testing power MOSFET modules requires higher test currents and therefore also a longer magnetization time with the same test inductance. Test currents can reach more than 300 A, requiring a magnetization time of $t_{\text{mag, module}} \gtrapprox 40\,\mu\text{s}$, resulting in a lower frequency boundary of

$$f_{\text{min,module}} \approx 5.6\,\text{kHz}. \tag{7.13}$$

7.8.2 Ideal Pulse Current Fourier Coefficients

The complex Fourier coefficients of an infinitely repeated sequence with period T are defined as

$$c_k = \frac{1}{T} \int_{t_0}^{t_0+T} f(t) e^{-j\frac{2\pi k t}{T}} dt. \tag{7.14}$$

With $t_0 = 0$ and the function definition

$$f(t) = i_{\text{square, ideal}}(t) = \begin{cases} \hat{i}, & \text{for } 0 \leq t \leq dT \\ 0, & \text{for } dT \leq t \leq T \end{cases}, \tag{7.15}$$

where $\hat{i}$ is the current amplitude and d the square waveform duty cycle, Equation 7.14 results to

$$c_k = \frac{\hat{i}}{T}\int_0^{dT} e^{-j\frac{2\pi kt}{T}}\,dt \tag{7.16}$$

$$= \frac{\hat{i}}{T}\cdot\frac{1}{-j\frac{2\pi k}{T}}\cdot\left[e^{-j\frac{2\pi kt}{T}}\right]_0^{dT} \tag{7.17}$$

$$= \frac{\hat{i}}{2\pi k}\cdot\left[e^{j\left(\frac{\pi}{2}-2\pi kd\right)} - j\right] \tag{7.18}$$

$$= \frac{\hat{i}}{2\pi k}\cdot\left[\sin(2\pi kd) + j(\cos(2\pi kd) - 1)\right]. \tag{7.19}$$

Only the Fourier coefficient magnitude is used in this work. These equate to

$$|c_k| = \frac{\hat{i}}{2\pi k}\cdot\sqrt{\sin^2(2\pi kd) + \cos^2(2\pi kd) - 2\cos(2\pi kd) + 1} \tag{7.20}$$

$$= \frac{\hat{i}\cdot\sqrt{2}}{2\pi k}\cdot\sqrt{1-\cos(2\pi kd)}. \tag{7.21}$$

With $d = 0.5$,

$$|c_k| = \frac{\hat{i}\cdot\sqrt{2}}{2\pi k}\cdot\sqrt{1-\cos(k\pi)} \tag{7.22}$$

$$= \frac{\hat{i}\cdot\sqrt{2}}{2\pi k}\cdot\sqrt{1-(-1)^k} \tag{7.23}$$

$$= \begin{cases} \frac{\hat{i}}{\pi k}, & \text{for } k \text{ uneven} \\ 0, & \text{for } k \text{ even.} \end{cases} \tag{7.24}$$

7.9 MAXIMUM CURRENT

7.9.1 *SDN-414-05 Coaxial CVR*

The coaxial CVR in question is declared a 2 W unit. This means a maximum continuous current of

$$I_{\text{max, cont}} = \sqrt{\frac{P_{\max}}{R_{\text{CVR}}}} \tag{7.25}$$

$$= \sqrt{\frac{2\,\text{W}}{1\,\text{m}\Omega}} = 6.32\,\text{A}. \tag{7.26}$$

The device specifications contain a maximum loss energy of 2 J. Approximating the current trajectory as a triangle, the current equation results to:

$$i_{\mathrm{L}}(t) = I_{\mathrm{max}} \cdot \frac{t}{t_{\mathrm{rise}}}. \tag{7.27}$$

The loss power during this current trajectory equates to

$$p_{\mathrm{loss}}(t) = i_{\mathrm{L}}^2(t) \cdot R_{\mathrm{CVR}}, \tag{7.28}$$

and the loss energy accordingly

$$E_{\mathrm{loss}} = \int_0^{t_{\mathrm{rise}}} \left(\frac{I_{\mathrm{RMS}}}{t_{\mathrm{rise}}}\right)^2 \cdot t^2 dt \cdot R_{\mathrm{CVR}} = \tag{7.29}$$

$$= \frac{t_{\mathrm{rise}} \cdot R_{\mathrm{CVR}}}{3} \cdot (I_{\mathrm{max}})^2. \tag{7.30}$$

Hence, the maximum current is

$$I_{\mathrm{max}} = \sqrt{\frac{3 \cdot E_{\mathrm{loss}}}{R_{\mathrm{CVR}} \cdot t_{\mathrm{rise}}}}. \tag{7.31}$$

With $t_{\mathrm{rise}} \approx 100\,\mu\mathrm{s}$ (including a safety margin) and $E_{\mathrm{loss}} = E_{\mathrm{loss,max}} = 2\,\mathrm{J}$:

$$I_{\mathrm{max}} \approx 1000\,\mathrm{A}. \tag{7.32}$$

It is still not recommended using this as a safe maximum to operate with. However, it demonstrates that this sensor is suitable for testing discrete MOSFETs and high power MOSFET modules in DPT experiments.

7.9.2 CSS4J-4026R-1L00x SMD CVR (1 mΩ)

The 4 W continuous power rating of the Bourns CSS4J-4026R-1L00x SMD CVR translates into a continuous current rating of 63 A according to Equation 7.26. The manufacturer gives a maximum pulsed loss power which can be translated into a current. According to the datasheet, the sensor can withstand a maximum loss power of 1200 W for a duration of 100 µs, which equals a current of 1095 A.

7.9.3 TCP0030A Current Clamp

The maximum continuous current of the Tektronix TCP0030A current clamp is 30 A. The manufacturer gives a formula for calculating maximum pulse currents that results to 50 A for a pulse width of 10 µs. Towards longer pulse lengths, the given formula loses meaning as the maximum current value drops below the continuous current rating. Due to the low maximum current value, this sensor is not suitable for high power MOSFET module characterization.

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Chapter 8

Low Inductive Characterization of Fast-Switching SiC MOSFETs and Active Gate Driver Units

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Contributions

- Low-Inductive Test Platform (LITP), consisting of a dedicated test circuit design and a parameter extraction software, for accurate and flexible dynamic characterization of fast switching discrete SiC power MOSFETs and Active Gate Drivers (AGDs)

- Extraction and Transfer of low-inductive design principles for successful design of characterization and converter circuits

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Abstract

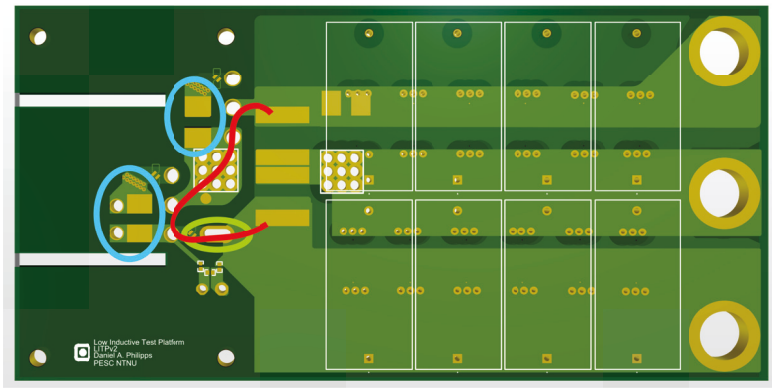
Accurate switching device characterization is necessary for effectively utilizing the technological advantages of Silicon Carbide (SiC) Power Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFETs) over their Silicon (Si) Insulated-Gate Bipolar Transistor (IGBT) counterparts. With switching times of few nanoseconds, the unprecedented switching speed of SiC semiconductor devices challenges today's converter and characterization setup designs in regard to parasitic layout inductances for optimal conversion and reliable characterization data. Furthermore, active gate driving is a key to unlock the potential of SiC MOSFETs, but requires performance assessment prior to integration. This paper presents a Low-Inductive Test Platform for flexible and high-accuracy characterization of fast-switching SiC MOSFET and Active Gate Driver (AGD) evaluation. The test circuit delivers high quality characterization data that is comparable with a commercial dynamic power device characterizer. In addition to the conventional hard-switching double-pulse tests with a Two Level voltage source gate driver, the test circuit offers soft-switching and gate driver evaluation capability in addition. This test platform is a valuable tool for obtaining reliable characterization data to develop more accurate SiC MOSFET simulation models, and evaluate the combination of gate driver and MOSFET prior to the prototyping phase of a converter.

Preceding Work

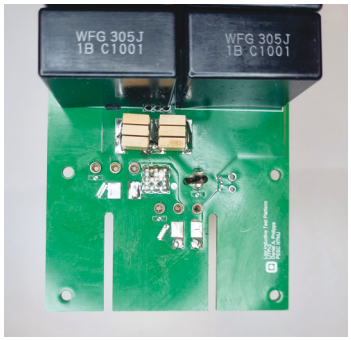
This paper is an extension of another work [1] that was presented at the IPEC Himeji 2022 ECCE Asia conference.

8.1 Introduction

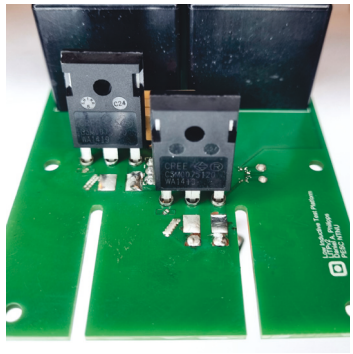
High Power SiC MOSFETs are becoming increasingly attractive for Power Electronic Converter applications because of their superior thermal behavior and faster switching speed compared to Si IGBT counterparts [2–4]. For the successful integration of fast-switching SiC power MOSFETs into converter systems, accurate characterization data are required to build accurate models used in an accelerated, simulation-assisted design process. Components in both converter and characterization circuits must be carefully arranged.



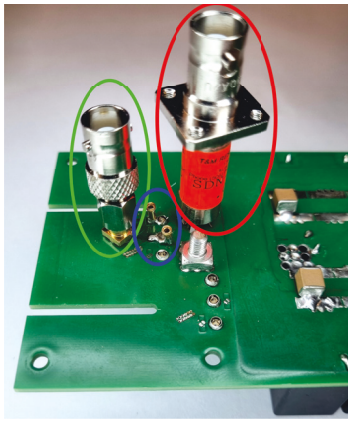
(A) Top side CAD view. Markings: Optimized current commutation path (red), current sensor port (light green), and gate pads (blue).



(B) Top front side without DUTs.



(C) Top front side with DUTs.



(D) Bottom from the side without DUTs. Left to right: Coaxial Gate-Source voltage probing point (green), Drain-Source voltage probing point (PCB pin receptacles, blue), coaxial CVR (red).

(E) Side view with DUTs.

FIGURE 8.1. Low-Inductive Test Platform from various angles

Insufficiently reduced circuit parasitics will dominate the electrical behavior, resulting in suboptimal conversion or unusable characterization data.

AGDs enhance the controllability of the switching device behavior. In various applications, AGDs were demonstrated to

- improve electromagnetic interference of converters [5–8]
- manipulate switching losses for active thermal control [8–10],
- offer control over the switching transitions, i.e. current and voltage slopes [7], and
- protect the MOSFET gate [11] which is essential for reliable long-term operation of SiC MOSFETs.

Moreover, AGDs are evolving into part-autonomous combined sensor-actuator systems that deliver valuable information for device health monitoring, lifetime estimation, and predictive maintenance procedures [12; 13].

Numerous Double Pulse Test (DPT) setups for hard-switching dynamic characterization can be found in literature [14–16]. However, most of the presented designs lack soft-switching test capability. Test setups that offer this function are either voluminous and need many components [17], or use snubber circuits [18]. Snubber circuits cover up the actual behavior of MOSFET and gate driver, counteracting the extraction of standalone device characteristics and effective gate driver evaluation. With the PD1500A dynamic power device characterizer [19], Keysight offers one of the few commercially available dynamic characterization systems. This system allows for an exchange of the test gate driver, but custom circuits like current-source [20] or multilevel voltage gate drivers [10] cannot easily be used with the proprietary soft- and hardware interface, and even using custom values for the Two Level voltage source driver requires a complex calibration procedure.

This paper presents an optimized characterization test platform suitable for SiC power device characterization and the evaluation of various gate driver types, including AGDs. The test platform circuit is optimized for low current-commutation path inductance. Hence, it is referred to as LITP. The LITP offers high flexibility, as both the switching Device Under Test (DUT) and gate driver can be easily exchanged. Dedicated measurement terminals enable high-accuracy, high-bandwidth drain current, drain-source and gate-source voltage measurements. A custom parameter extraction software determines switching parameters according to the IEC 60747-8 standard [21]. The performance of the LITP meets its commercial reference, the PD1500A dynamic power device characterizer by Keysight, in hard-switching tests. Furthermore, the LITP

enables reversed current switching tests that represent the device behavior in a soft-switching converter such as the Dual-Active-Bridge Converter.

The paper is organized as follows. Section 8.2 describes the LITP design goals, how they were met, and what challenges arise in designing and operating SiC MOSFET test circuits. Special attention is paid to the circuit layout and the measures taken to optimize its dynamic behavior. Experimental results are shown in Section 8.3. The performance of the test circuit is compared to a Keysight PD1500A Power Device Analyzer [19]. For this comparison, identical DUTs and test conditions were used, and according to the IEC-60747-8 standard [21], the switching parameters listed in Table 8.2 were calculated. Afterward, exemplary reverse current switching measurement results are shown that represent soft-switching device behavior. Finally, the gate driver evaluation capability of the LITP is demonstrated by the example of a four voltage level active gate driver. Section 8.4 explains how the characterization data obtained with the LITP can be used. Furthermore, detailed guidelines for a successful design of both converter and characterization circuit layouts are presented. Section 8.5 concludes the paper.

8.2 Low Inductive Test Platform Design and Challenges

Accurate dynamic characterization of fast switching devices requires a highly optimized circuit design. At the same time, characterizing multiple DUTs is only possible if device exchange is convenient. In addition, the same circuit should be usable for both hard- and soft-switching tests. Therefore, the following design goals emerge:

1. The circuit layout influence must be optimized for minimal parasitic impedance. The focus is on the current-commutation loop inductance, also referred to as stray power loop inductance.

2. For the highest possible accuracy, both voltage and current probing point integration must be a priority during circuit design. Optimal component placement, routing and shielding are required to achieve high signal quality.

3. Exchanging DUTs must be fast, repeatable and damage-free.

4. To further expand utility, the circuit should support gate driver evaluation. This requires easy gate driver exchange.

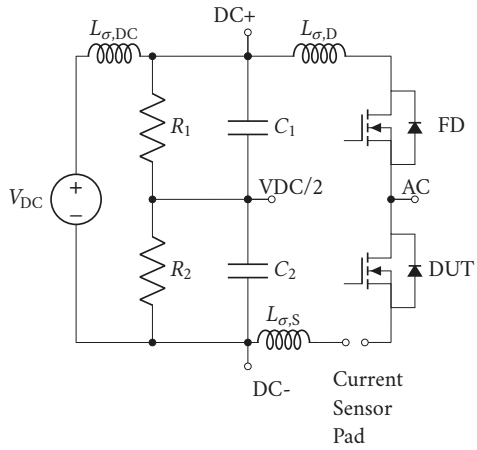
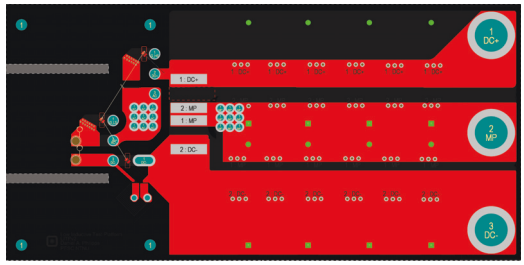
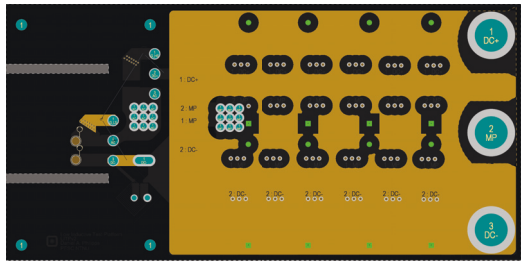


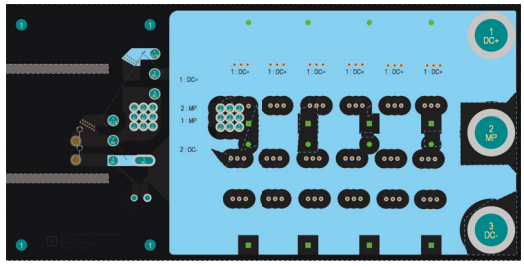
FIGURE 8.2. Idealized schematic diagram of the Low-Inductive Test Platform



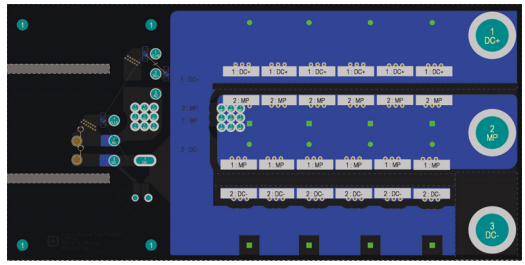
(A) Top Layer



(B) Upper intermediate layer (layer 1)

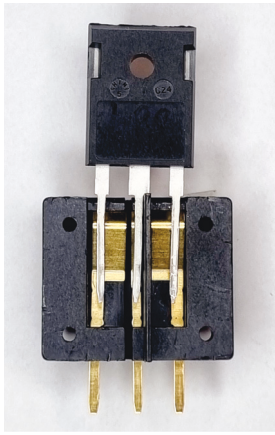


(C) Lower intermediate layer (layer 2)



(D) Bottom Layer

FIGURE 8.3. Low-Inductive Test Platform PCB layers (used in this work)



(A) TO-247-3 MOSFET with one of the two identical halves that form the commercial PTR-1 TO-247-3 device socket (not used in this work)

(B) TO-247-3 MOSFET with PCB pin receptacles used on the LITP and PD1500A (used in this work)

Figure 8.4. Connection style alternatives allowing for fast and non-destructive device exchange.

These design goals were addressed with a dedicated PCB design. Parts of the PCB design were discussed in a previous publication [1]. This paper extends the previous publication by presenting an updated PCB, adding more design details, and presenting more results. The pictures in Figure 8.1 show the updated PCB from various angles. The idealized schematic circuit diagram of the LITP can be seen in Figure 8.2. The circuit is supplied by a high voltage DC source (V_{DC}), that charges the buffer capacitors C_1 and C_2. R_1 and R_2 are balancing resistors, ensuring an equal voltage across each of the buffer capacitors in steady state, so that the middle terminal carries the voltage $V_{DC}/2$ as indicated in Figure 8.2. $L_{\sigma,DC}$ symbolizes the stray inductance of the supply cables connecting the high voltage DC source and LITP. $L_{\sigma,D}$ and $L_{\sigma,S}$ symbolize the aggregated path inductances caused by the PCB layout from AC to DC+ ($L_{\sigma,D}$), and from AC to DC-. Owing to the fast-switching behavior of SiC MOSFETs, common-mode currents are expected flowing through the gate driver power supply of the upper SiC MOSFET acting as a Freewheeling Device (FD) as it is referenced to a rapidly changing potential during switching. However, in the proposed LITP, only the low-side SiC MOSFET is used as the DUT, and all measurements are referenced to the source potential of the DUT. Thus, any occurring common-mode currents are not expected to disturb the measurements. Figure 8.3 shows all four PCB copper layers. To achieve the design goals discussed before, the following measures were enacted:

1. The parasitic effects of the circuit layout were minimized.

(a) Both foil and ceramic capacitors were placed as close as possible to the DUT. The ceramic capacitors have a lower Equivalent Series Inductance (ESL) and can therefore provide energy faster than the foil capacitors. The foil capacitors have a higher capacitance and can supply more energy. In combination, ceramic and foil capacitors provide effective filtering. All capacitors are visible in Figure 8.1b. The black cuboids are the foil capacitors, and the yellow-brown cuboids are the ceramic capacitors, CeraLink B58035 FA3 capacitors from TDK [22]. Figure 8.1d and Figure 8.1e show additional support capacitors on the bottom side of the PCB.

(b) The PCB copper layers were designed for maximum overlap and least space between the switching current paths, minimizing the associated stray inductance. Maximizing the copper layer overlap is limited by the clearance requirements imposed by high voltage operation.

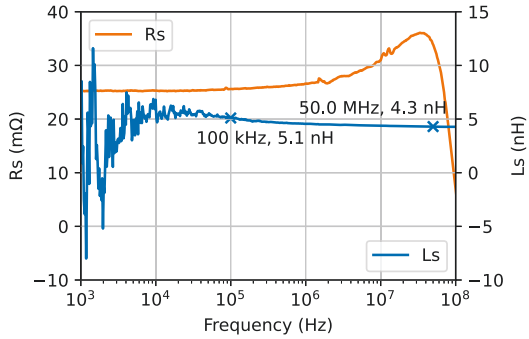
(c) Tracks are kept as short as possible to further minimize stray inductance. The red line in Figure 8.1a represents the current commutation path, which was optimized for minimal length while ensuring component distances required for isolation of the high test voltages.

Finite Element Method (FEM) simulations result in a stray inductance of $L_{\sigma,\mathrm{FEM}} = 15.42\,\mathrm{nH}$ induced by the circuit layout in the power loop. Referring to Figure 8.2, this inductance constitutes the sum of the stray inductances in the current path, $L_{\sigma,\mathrm{D}}$ and $L_{\sigma,\mathrm{S}}$. Two series connected CeraLink B58053 FA3 capacitors from TDK [22] were used as buffer capacitors, clearly visible in Figure 8.1b. According to the datasheet, the capacitors have an ESL of $L_{\sigma,\mathrm{ESL,CeraLink}} = 3\,\mathrm{nH}$. These capacitors are closest to the DUT and FD, and they exhibit the lowest ESL of all capacitors connected in parallel forming C_1, or C_2 respectively. Therefore, the aggregated ESL of C_1, or C_2 respectively, can be approximated as

$$L_{\sigma,\mathrm{ESL,C1}} = L_{\sigma,\mathrm{ESL,C2}} = L_{\sigma,\mathrm{ESL,CeraLink}} = 3\,\mathrm{nH}. \tag{8.1}$$

In experiments, a characteristic voltage drop V_{Drop} can be observed at turn-on as will be shown in Section 8.3. This voltage drop occurs as a result of the associated current change $(\frac{di}{dt})$ in all involved path inductances, i.e. the layout inductances $L_{\sigma,\mathrm{D}}$ and $L_{\sigma,\mathrm{S}}$, the ESL of the buffer capacitors $2 \cdot L_{\sigma,\mathrm{ESL}}$, and the packaging inductance of the upper device, $L_{\sigma,\mathrm{TO247}}$.

(A)



(B)

Figure 8.5. Coaxial CVR Impedance Analysis Test Setup (A) and Result (B)

The coaxial CVR is placed in the source current path of the DUT and therefore adds its insertion impedance into the power loop. To determine this insertion impedance, the coaxial CVR was characterized with an impedance analyzer. A picture of the CVR connected to the impedance analyzer and the measurement result can be seen in Figure 8.5. Depending on the frequency of the measured current, an insertion impedance of $L_{\sigma,\mathrm{CVR}} \approx 5\,\mathrm{nH}$ must be expected. The inductance measurement at low frequencies is not reliable. When the inductive reactance falls below 1 % of the resistance, the measurement of the reactance and subsequently the inductance does not produce accurate results, as can be seen in Figure 8.5b. In this case, the reactance and thus the inductance values are only accurate for the following condition:

$$\omega \cdot L_{\mathrm{CVR}} = X_{\mathrm{CVR}} \geq 0.01 \cdot R_{\mathrm{CVR}} \tag{8.2}$$

$$\implies 2 \cdot \pi \cdot f \cdot L_{\mathrm{CVR}} \geq 0.01 \cdot R_{\mathrm{CVR}} \tag{8.3}$$

$$\implies f \geq \frac{0.01 \cdot R_{\mathrm{CVR}}}{2 \cdot \pi \cdot L_{\mathrm{CVR}}} \tag{8.4}$$

With $R_{\mathrm{CVR}} = 25\,\mathrm{m\Omega}$ and $L_{\mathrm{CVR}} \approx 5\,\mathrm{nH}$, this yields:

$$f \geq \frac{0.01 \cdot 25\,\mathrm{m\Omega}}{2 \cdot \pi \cdot 5\,\mathrm{nH}} \approx 8\,\mathrm{kHz}. \tag{8.5}$$

This explains the instability in the measurements below 8 kHz. However, according to the above calculation, the inductance has a negligible influence compared to the resistance in this frequency range. Therefore, the insertion inductance of the coaxial CVR is approximated as 5 nH in the following. The sum of the inductances described above is referred to as power loop inductance,

$$L_{\sigma,\mathrm{pl}} = L_{\sigma,\mathrm{D}} + L_{\sigma,\mathrm{S}} + L_{\sigma,\mathrm{ESL,C1}} + L_{\sigma,\mathrm{ESL,C2}} + L_{\sigma,\mathrm{TO247}} + L_{\sigma,\mathrm{CVR}}. \tag{8.6}$$

Note that $L_{\sigma,\mathrm{TO247}}$ is not included twice, as the drain-source voltage measurement is taken across the DUT and thus, any potential voltage drop caused by its package inductance cannot be observed in the measurement. The manufacturer provides a SPICE model for the C3M0075120D SiC MOSFET [23] which was used as both DUT and FD. The model contains the drain and source path inductance in separate variables, $L_{\sigma,\mathrm{D,TO247}} = 4.366\,\mathrm{nH}$ and $L_{\sigma,\mathrm{S,TO247}} = 5.5\,\mathrm{nH}$, adding up to

$$L_{\sigma,\mathrm{TO247}} = L_{\sigma,\mathrm{D,TO247}} + L_{\sigma,\mathrm{S,TO247}} = 9.866\,\mathrm{nH}. \tag{8.7}$$

Using Equation 8.7, and assuming $L_{\sigma,\mathrm{D}} + L_{\sigma,\mathrm{S}} \approx L_{\sigma,\mathrm{FEM}}$, Equation 8.6 becomes:

$$\begin{aligned} \mathbb{L}_{\sigma,\mathrm{pl}} &= L_{\sigma,\mathrm{FEM}} + L_{\sigma,\mathrm{ESL}} + L_{\sigma,\mathrm{TO247}} + L_{\sigma,\mathrm{CVR}} && (8.8)\\ &= 15.42\,\mathrm{nH} + 6\,\mathrm{nH} + 9.866\,\mathrm{nH} + 5\,\mathrm{nH} && (8.9)\\ &\approx 36.29\,\mathrm{nH}. && (8.10) \end{aligned}$$

When measuring both switch current and drain-source voltage, $L_{\sigma,\mathrm{pl}}$ can be approximated as follows:

$$L_{\sigma,\mathrm{pl}} \approx \frac{V_{\mathrm{Drop}}}{\frac{di}{dt}}, \tag{8.11}$$

V_{Drop} being the drain-source voltage drop described above. This estimate can be used to verify the FEM simulation results. At a test current of 30 A, a voltage drop of 30 V and a coincidental $\frac{di}{dt}$ of $0.976\,\mathrm{A\,ns^{-1}}$ were determined manually, resulting in a stray inductance estimate of 30.7 nH following Equation 8.11. This estimate is in very good agreement with the approximation resulting from Equation 8.10. The deviation of 5.39 nH

can be explained by the uncertainty of V_{Drop} and $\frac{di}{dt}$ readings that result from measurement noise. In addition, the $L_{\sigma,\text{ESL,CeraLink}}$ stray inductance component is estimated conservatively, and $L_{\sigma,\text{TO247}}$ might be subject to inaccuracy. In the real setup, this stray inductance is lowered by the parallel connection of the additional foil and ceramic buffer capacitors. Finally, approximating $L_{\sigma,\text{CVR}} \approx 5$ nH does not reflect the frequency dependence of the CVR insertion impedance adequately, and might considerably overestimate the actual inductive component of the insertion impedance. To conclude with a conservative approximation, the PCB contributes with a power loop inductance of $L_{\sigma,\text{PCB}} \approx L_{\sigma,\text{FEM}} = 15.42$ nH, emphasizing the low-inductive character of this circuit design.

2. During the PCB design, a major priority was probing points that enable high bandwidth measurements. Minimizing measurement loop inductance, probing point capacitance, and using coaxial probe connections where possible ensures high quality measurement results reflecting the actual device behavior. All probing points are visible in Figure 8.1d without and in Figure 8.1e with cables and probes connected.

   (a) Gate-Source voltage measurement: The gate driver pads are connected to through-hole vias that can accommodate either PCB pin receptacles for passive probing with a ground spring or an SMA connector that can be connected to a probe with an SMA-probe tip adapter. Coaxial probing is preferred as it shields disturbances most effectively. As gate-source voltages do not surpass 50 V, it is safe to use SMA connectors for measurements. In Figure 8.1d, this measurement point is shown on the left and highlighted by the green ellipse, the SMA connector being connected to an SMA-to-BNC adapter. Using a BNC probe-tip adapter, a Tektronix TCP1000 passive voltage probe [24] was connected to this measurement point, which is shown in Figure 8.1e.

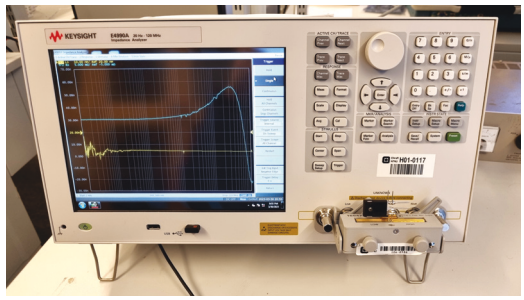
   (b) Drain-Source voltage measurement: Next to the DUT vias, pads allow the connection of PCB pin receptacles for passive probing with a ground spring. Unfortunately, the high voltage between drain and source disqualifies the use of both SMA and BNC connectors. A custom coaxial-like solution was developed. However, its space demand is at odds with the aim of circuit miniaturization resulting from the desire for low current-commutation loop inductance. Hence, using a ground spring is the measurement approach of choice. Figure 8.1d shows the pin receptacles that connect to the passive probe tip and the ground lead originating from the ground spring (in a blue ellipse) between the SMA-BNC connector on the

left (in a green ellipse), and the coaxial CVR on the right (in a red ellipse). In Figure 8.1e, a Keysight 10076C passive high voltage probe [25] is connected to the pin receptacles with a ground spring attachment as described above.

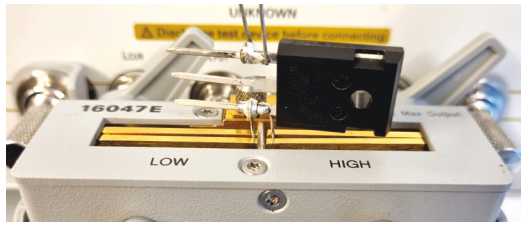
(c) Drain current measurement: The proposed circuit features a multipurpose current sensor pad. Left unmanipulated, a Rogowski Coil can be attached around the current path. Instead, the current path can also be interrupted by applying a rectangular cut to the current sensor pad. The ends of the separated pad can be soldered to a wire loop to connect a current clamp. Alternatively, a CVR can be inserted, as seen in Figure 8.1d and Figure 8.1e.

(d) Auxiliary Current measurement: For future work, pickup-coils similar to the "Infinity Sensor" [26] are included on the PCB, for gate and drain current measurement. However, these sensor structures were not further investigated in this work.

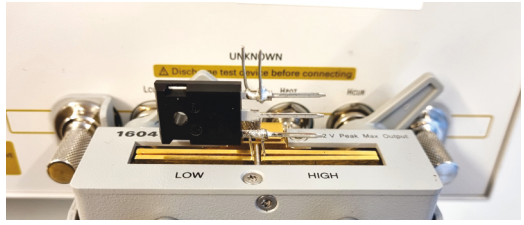
3. In other test circuits, sockets for TO-247-3 devices are used to enable easy DUT exchange. An existing commercial solution is the PTR-1 socket [27]. Figure 8.4a shows this socket from the inside. When connecting a TO-247-3 MOSFET, it would be in the same position as the device shown in Figure 8.4a. The big size of this socket counteracts circuit minimization, and it introduces significant parasitic inductance to the current commutation path as the electrical connection of the circuit is only established at the contacts located at the bottom of the socket. To reduce this inductance, the proposed LITP contains 1 mm wide PCB pin receptacles instead, and thereby follows the example of the PD1500A power device characterizer. This approach allows connecting and disconnecting TO-247-3 MOSFETs easily and quickly, without adding significant inductance. Figure 8.4b shows the PCB pin receptacles slid onto the legs of a TO-247-3 MOSFET. The pin receptacles are located on PCB level and are integrated as through-hole components. This connection style offers flexibility, while the added contact resistance and inductance are very close to soldering the DUTs on the PCB.



(A) Overview of impedance analysis setup



(B) Detail view of MOSFET leg and receptacle connected to measurement terminals



(C) Detail view of MOSFET leg and solder joint connected to measurement terminals

FIGURE 8.6. TO-247-3 MOSFET leg receptacle and solder junction impedance analysis setup

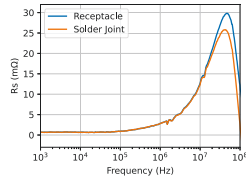


FIGURE 8.7. Measurement results from impedance analysis of receptacle and solder junction

To determine the difference between the contact impedance values using either a pin receptacle or a solder joint on a MOSFET leg, two impedance analyses were conducted. Figure 8.6a shows an overview of the experimental setup with the impedance analyzer (Keysight E4990A) and the measurement fixture to the lower right. One pin receptacle was soldered

to a short lead. Similarly, the leg of a MOSFET was soldered to a short lead directly above the mating point between the MOSFET leg and the pin receptacle. The MOSFET leg was then inserted into the pin receptacle, and the two lead ends were connected to the impedance analyzer measurement terminals. A picture of this arrangement is shown in Figure 8.6b. To put the result into perspective, the resistance introduced by a solder joint was determined in a second experiment. The lead that was previously soldered to the receptacle was now formed into a 2-turn spiral, and soldered to the MOSFET leg in the same position as the receptacle earlier, imitating a PCB solder joint. This arrangement is shown in Figure 8.6c. The measurement results are shown in Figure 8.7. The maximum added resistance of one pin receptacle exceeds the maximum added resistance of a solder joint by 4.0 mΩ. Given the strong frequency dependency of the added resistance, this effect is not negligible but acceptable, taking into account that the on-state resistance ($R_{DS,on}$) equals 75 mΩ for typical discrete 1.2 kV power MOSFETs in the 30 A class.

The pin receptacles can be seen from above in Figure 8.1b without and in Figure 8.1c with MOSFETs plugged connected to the circuit.

4. For convenient and low-impedance connection of gate drivers, wide, general purpose pads were included as close as possible to the DUT on the PCB. These gate pads support high current and low-impedance gate driver connection due to their large width, as well as small distance between each other. The gate pads are highlighted in blue in Figure 8.1a and are clearly visible in Figure 8.1b in front of the empty DUT PCB pin receptacles and Figure 8.1c with the DUT behind.

The circuit enables both hard- and soft-switching tests. Commonly, DPTs are performed with the test inductor connected to the mid-point between the two series-connected power MOSFETs and the positive supply rail. While this is possible with the proposed LITP, only positive inductor currents and thus hard-switching turn-on tests can be realized in this configuration. Alternatively, the test inductor can be connected to the midpoint of the capacitors C_1 and C_2, "VDC/2" (see Figure 8.2). When driving both devices in the half-bridge synchronously with suitable signals, this allows reversing the test current and thereby performing soft-switching tests.

8.3 Results

Table 8.1. Wolfspeed C3M0075120D Parameters [28]

Property	Value
Breakdown Voltage Rating $V_{DS,\,max}$	1200 V
Continuous Drain Current Rating $I_{D,cont}$	32 A
On-state Resistance R_{DS} ($T = 25\,^{\circ}C$)	75 mΩ
Package	TO-247-3

8.3.1 *Hard-Switching Double Pulse Tests*

Test Configuration

Hard-Switching Double Pulse Tests (DPT) were conducted using both the proposed low-inductive test platform and the Keysight PD1500A power device characterizer [19]. The same two individuals of the C3M0075120D 1.2kV-class SiC power MOSFET by Wolfspeed [28] were connected in a half-bridge configuration. The device parameters of this power MOSFET are listed in Table 8.1. Photos of this circuit configuration is shown in Figure 8.1c and Figure 8.1e. The lower device is referred to as Devices Under Test (DUTs). The test voltage was 800 V and the test current was varied from 5 A to 30 A, and a conventional Two Level VSGD was used to charge and discharge the power MOSFET gate. The PD1500A is delivered with a set of gate driver boards provided by the manufacturer. These gate driver boards contain a conventional Two Level voltage driver IC with an external gate resistor. The gate driver board with a 10 Ω external gate resistor was installed.

For the experiments with the LITP, a circuit based on the IXYS IXDN630YI gate driver IC [29] was connected to the general-purpose gate pads. The low gate driver voltage was set to −5 V, and the high gate driving voltage to 15 V. The gate-source voltage was measured using a Tektronix TPP1000 passive voltage probe [24], the drain-source voltage with a Keysight 10076C passive voltage probe [25], and the drain current with a T&M Research SDN-414-025 coaxial current viewing resistor [30]. A Tektronix DPO5104B oscilloscope [31] with an analog bandwidth of 1 GHz was used to record the measurements. The sampling rate was set to 5 GS s^{-1}. Prior to testing, all probes were deskewed with a square-wave signal provided by the AFG3052C Arbitrary Function Generator [32]. The coaxial CVR was deskewed with a 50 Ω resistor in series and using the onboard signal injection port that can be seen in Figure 8.1a underneath the light green ellipsoid indicating the current sensor pad.

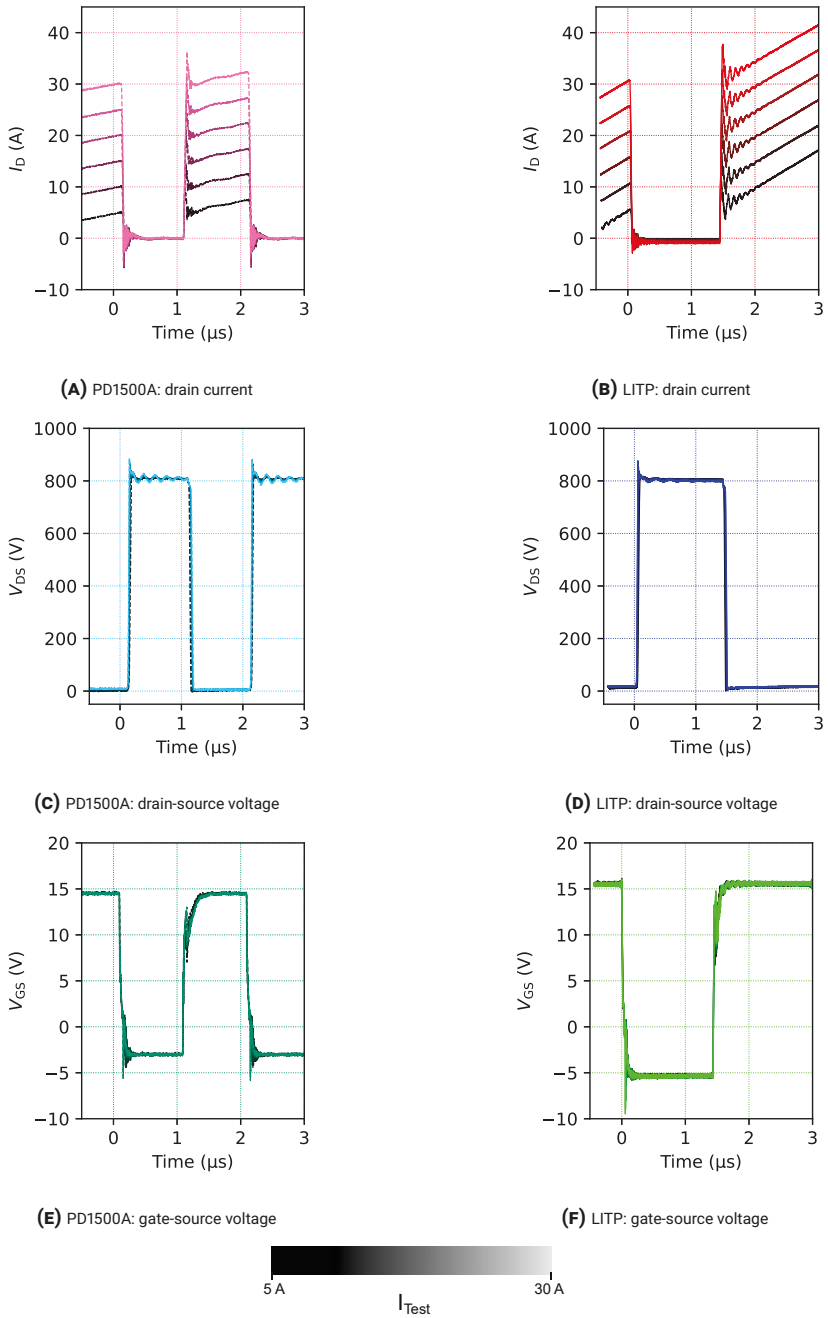


FIGURE 8.8. Double-pulse test measurements in overview. Shades indicate the test current level according to legend.

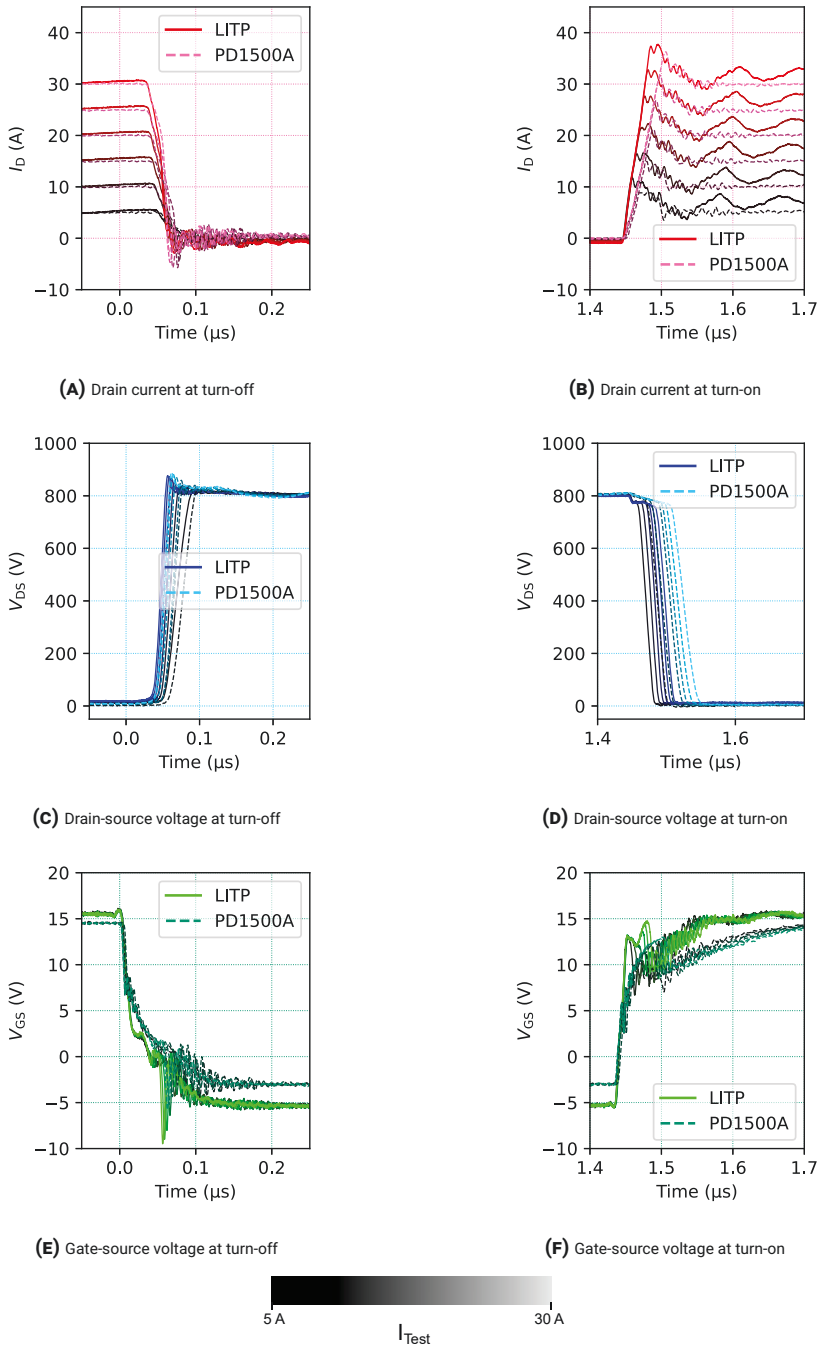
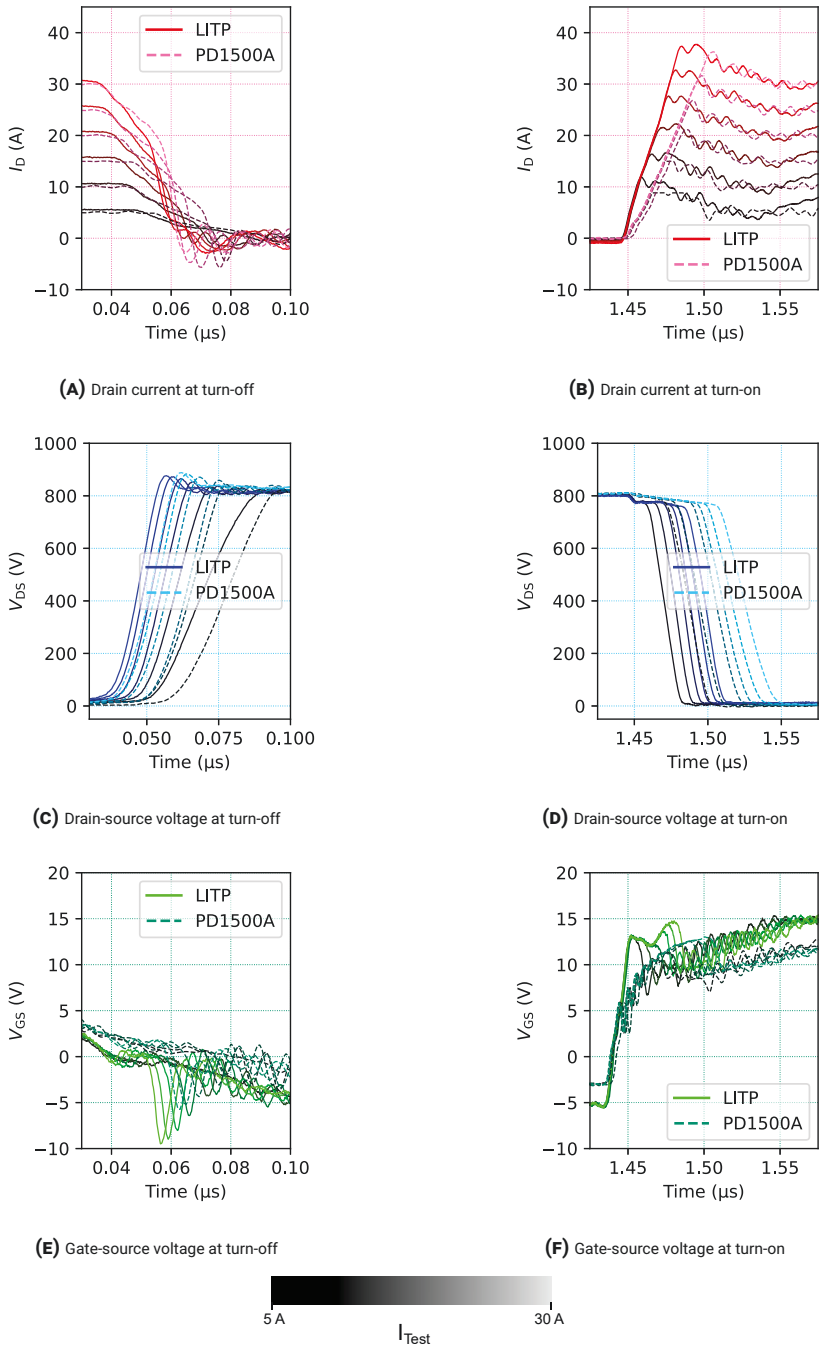


Figure 8.9. Double-pulse test measurement comparison: LITP vs PD1500A. Shades indicate the test current level according to legend.



(A) Drain current at turn-off

(B) Drain current at turn-on

(C) Drain-source voltage at turn-off

(D) Drain-source voltage at turn-on

(E) Gate-source voltage at turn-off

(F) Gate-source voltage at turn-on

FIGURE 8.10. Double-pulse test measurement comparison: LITP vs PD1500A in greater detail. Shades indicate the test current level according to legend.

Figure 8.8 and Figure 8.9 show time domain measurements of the DPT experiments in comparison to each other within varying time intervals. The displayed trajectories differ in the test current and the test setup they were recorded with. Figure 8.10 shows the same waveforms at a smaller timescale for improved comparability. The time scales differ between turn-on and turn-off because of the different switching speeds. The shade of a trace indicates the respective test current level. The lighter its shade, the higher the test current level of the measurement. The color and line style of a trace indicates the test setup. Dashed purple drain current, teal drain-source voltage, and petrol gate-source voltage waveforms originate from the PD1500A power device characterizer, while solid red drain current, blued drain-source voltage and green gate-source voltage waveforms were recorded using the LITP.

General Differences between LITP and PD1500A

Several differences can be observed between the PD1500A and the LITP. The signal timing differs between the experiments, as can be clearly observed in Figure 8.8. However, this difference is not related to the circuit, but instead caused by different signal generation. Changing the timing is a matter of software reprogramming or reconfiguration and does not influence the electrical behavior of the circuit or the DUT significantly as long as it is feasible to reach the desired test current.

Similarly, the test inductor inductance does solely change the signal timing to reach the test current, but not the electrical behavior if it stores sufficient energy to drive the current commutation within the half-bridge, and assuming that the inductor current does not drop significantly between the turn-off and turn-on tests. In practice, both very small and very large inductance values are problematic. Small inductance values require very high control signal resolution and small error margins, large inductors require long magnetization times and thus lead to significant self-heating of the DUT during conduction.

For the experiments, the manufacturer test inductor in the PD1500A was exchanged with a 400 µH inductor, and a ferrite core test inductor with an inductance of 110 µH was chosen for the experiments with the LITP. Therefore, the drain current slope during the magnetization phase is significantly steeper in the LITP experiments. This is visible when comparing Figure 8.8a to Figure 8.8b. However, this does not have a notable impact on the electrical behavior during switching, as self-heating is negligible on the timescale of a few microseconds and with currents well within the device safe operating area. The drain current measurement of the PD1500A shows higher oscillation amplitudes during turn-off (Figure 8.9a), but lower oscillation amplitudes during turn-on (Figure 8.9b). As the figure resolution is partly insufficient to show individual oscillations,

higher frequencies manifest as a higher line density in both Figure 8.8 and Figure 8.9. Except for the drain current, all observed oscillations have a higher frequency, and therefore higher line density, in the LITP experiments as can be seen in Figure 8.9.

Another difference between the two test setups is the drain-source voltage stability. The drain-source voltage observed with the PD1500A is subject to oscillations after the DUT is turned off (Figure 8.8c). In the experiments with the proposed LITP, oscillations can be observed, too, albeit with a significantly lower amplitude and stronger damping (Figure 8.8d). This is mainly because both high-capacitance foil capacitors and low-capacitance ceramic capacitors that have very low Equivalent Series Resistance (ESR) and ESL, and positioned very close to the switching devices. In the PD1500A, solely ceramic capacitors with a low ESR and ESL are placed in the direct vicinity of the switching devices. Oscillations therefore originate from the inductance between these primary capacitors and bigger, secondary capacitors that are located at a greater distance from the switching devices. While the oscillations observed with the PD1500A are not desirable, the switching instances are not significantly influenced as the current energy required for the current commutation is supplied by the ceramic capacitors. The current commutation is therefore driven in a similar manner in both setups.

Gate Driving and Layout Interaction

The biggest differences occur in the gate-source voltage. The gate driver used in the LITP experiments is based on the IXDN630YI IC [29], which is designed for operation with power MOSFET modules. Hence, the LITP experiments exhibit very high switching speeds, especially at turn-on (Figure 8.9b, Figure 8.9d, and Figure 8.9f). These very high switching speeds result in steep current and voltage slopes that can easily excite oscillations in a broad frequency spectrum. As a result, stronger oscillations of lower frequencies can be observed in the LITP drain current measurements (compare Figure 8.8b and Figure 8.8a).

The higher switching speed also leads to a more pronounced voltage drop at turn-on (Figure 8.9d). This voltage drop was investigated numerically in Section 8.2 By providing a high gate current, the gate driver connected to the LITP achieves high gate-source voltages very early in the switching process and thus allows a steep drain current rise that translates into a drain-source voltage drop. This results in a characteristic drain-source voltage step that can be clearly observed in Figure 8.9d and that was previously used to estimate the power loop inductance. The PD1500A gate driver does not reach the same high gate-source voltages and drain-current slopes. Thus, the drain-source voltage does not form a step but a rather flat slope instead.

At turn-off (Figure 8.9a, Figure 8.9c, and Figure 8.9e), the gate-source voltage measured with the LITP contains low amplitude oscillations. The gate-source voltage measured with the PD1500A, on the other hand, shows stronger oscillations that are similar in frequency to the oscillations measured in the drain current, as can be observed best in Figure 8.9. This similarity suggests that the oscillations in the gate loop induce the drain current oscillations.

In addition, the entire transitions of the PD1500A gate-source voltage seem to be superimposed with an oscillation. The LITP gate-source voltage transitions do not show the same behavior, but a straight rising or falling edge at the beginning of each transition. This straight edge is followed by strongly damped oscillations, as well as voltage dips due to the Miller-capacitance currents during the voltage transitions, shown in detail in Figure 8.9e and Figure 8.9f. The two main reasons for oscillations in the gate-source voltage measurement are the gate loop inductance and induced oscillations in the measurement path. Both the distance between the gate driver output and the DUT and the distance between the DUT and the closest, coaxial shielded point for measurement are shorter in the LITP than in the PD1500A, which explains the higher oscillatory content in measurements with the latter.

At turn-off (Figure 8.9e), the PD1500A gate-source voltage measurement drops to a value of 7.5 V approximately 5 ns faster than the LITP, despite the fact, that the low gate driving voltage is only −3 V compared to −5 V in the LITP. This can be explained by the gate-source voltage probe position in the PD1500A, that is closer to the gate driver output than to the device terminals. The gate-source voltage measurement is taken across almost the entire path from gate driver output to the device. The inductance of this path requires a voltage for an increase in gate current. Therefore, the voltage first drops very fast to engage a current that can then discharge the gate. The gate-source voltage probe position in the LITP is very close to the switching device and there is less inductance between the probing point and the power device, resulting in a voltage reading that is closer to the actual gate-source voltage of the power device.

Parameter Extraction According to the IEC 60747-8 Standard

The purpose of a characterization circuit is to accurately determine switching parameters. The PD1500A contains a software package for extracting parameters according to the IEC 60747-8 standard [21]. For this work, software was programmed in python that aims at extracting the same parameters. To verify the precision and accuracy of this software, it was executed with the time domain results obtained from the PD1500A shown above (Figure 8.8 and Figure 8.9) as input data. The results were then compared to the parameter

TABLE 8.2. Extraction Parameters according to IEC 60747-8 [21], and deviation between results from self-coded Parameter Extraction Software and PD1500A reference values using identical raw data

Parameter	Meaning	Mean Deviation
E_{off}	Turn-off Switching Energy	-2.08 µJ (-1.81 %)
E_{on}	Turn-on Switching Energy	+17.9 µJ (+1.67 %)
t_{f}	Voltage Transition Time at Turn-off	+98.6 ps (+0.56 %)
t_{r}	Voltage Transition Time at Turn-on	+328 ps (+1.21 %)
$t_{\text{d,off}}$	Delay Time at Turn-off	-343 ps (-0.77 %)
$t_{\text{d,on}}$	Delay Time at Turn-on	+4.00 ns (+8.21 %)

extraction results of the PD1500A using the same input data. The extracted parameters, their meaning, and the absolute and relative deviation from the PD1500A results averaged over all test current values are listed in Table 8.2. The errors range below 2 %, except for the delay time at Turn-on, $t_{\text{d,on}}$, which shows a systematic and consistent deviation of +4 ns for all current levels as opposed to changing deviation values for all other parameters. Manual $t_{\text{d,on}}$ calculation confirms the results of the self-coded parameter extraction software. Hence, the parameter extraction software was regarded accurate and suitable for further analysis.

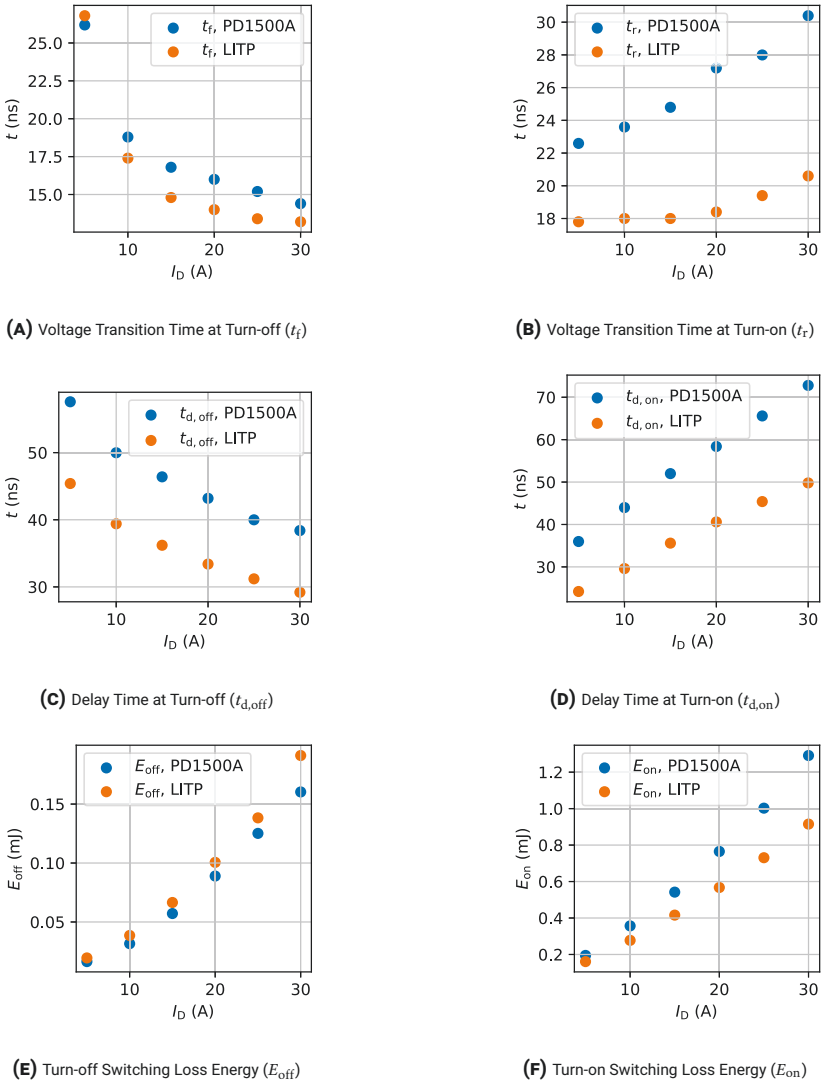


Figure 8.11. Extracted Switching Parameters in Comparison: PD1500A vs LITP

Using the parameter extraction software introduced above, the aforementioned hard-switching DPT experiments were analyzed and switching parameters were extracted from the measurements. The results of this analysis are shown in Figure 8.11. The delay times at turn-on (Figure 8.11d) are considerably shorter in the LITP experiments. These results emphasize that the LITP was tested with a very powerful gate driver that is connected to the power MOSFETs through a low-inductive path. The ability of the driver to provide larger gate currents is also reflected in the clearly accelerated voltage transition

time at turn-on (Figure 8.11b). The faster gate dynamics and the lower stray inductance in the power loop enable a faster current transition, which, in combination with the faster voltage transition, leads to a lower switching loss at turn-on (Figure 8.11f). The turn-off switching process is governed mainly by the load current and the body diode of the upper device. Therefore, very similar switching loss values (Figure 8.11e) and voltage transition times (Figure 8.11a) can be seen at turn-off for both of the test setups.

The IEC 60747-8 [21] standard bears ambiguity because of its idealized switching transition waveforms. In the case of strong oscillations, for example, it is not clear, which transition of the 10 % or 90 % boundaries should be chosen as switching loss calculation boundaries. While it is not the aim of this work to propose a refined definition of the standard, the differences in turn-off switching losses can be explained by the strong drain current oscillations observed in the PD1500A experiments. Such oscillations lead to an earlier first transition of the 10 % current boundary by skewing the current transition steepness. Therefore, the switching losses appear to be lower in the PD1500A experiments. However, oscillations can contribute to the switching losses, if they have a non-zero average, which might be the case for the oscillation periods immediately following the switching transition. These are not registered by the parameter extraction algorithm because the first 10 %-current transition criterion determines the switching loss calculation boundaries. The delay time at turn-off is considerably shorter in the LITP experiments compared to the PD1500A experiments (Figure 8.11c). The reason for this is again the higher current capability of the gate driver, as it is the case for the delay time at turn-on.

8.3.2 *Soft Switching Tests*

One of the main achievements of this work is the capability of the proposed LITP to test the switching behavior of a power MOSFET with a negative current. This represents the switching situation in a soft-switching converter, such as the Dual-Active Bridge Converter. By connecting the test inductor to the midpoint of the power MOSFETs arranged as a half-bridge, "AC" in Figure 8.2, and the midpoint of the capacitors C_1 and C_2, "VDC/2" in Figure 8.2, it is possible to reverse the inductor current using synchronous switching of the two power MOSFETs and suitable switching signal intervals.

To demonstrate the ability of the circuit to perform such soft-switching tests, exemplary experiments were conducted with the same setup as with the DPTs earlier, with the same power MOSFETs, gate driver, test inductor, probes, oscilloscope, and test voltage, but with a different timing and synchronous switching. The test currents were set to 5 A to 25 A in 5 A steps. The turn-

off test is conducted with an inductor current flowing towards "AC", and the turn-on test is conducted with an inductor current flowing towards "VDC/2".

Different test currents require different control signal intervals. This presents a challenge for properly visualizing measurements in an overview, as for the DPT experiments above. Therefore, only the switch current under variation of the test current is given as an overview in Figure 8.12. Turn-off and turn-on switching transitions of current and voltage are shown in greater detail and in proper alignment in Figure 8.13. As can be seen in Figure 8.13, the test setup is capable of measuring soft-switching transitions, that result in highly load-current dependent voltage transitions as the load current charges and discharges the device output capacitances. Hence, a strong $\frac{dv}{dt}$ dependency is visible: The darker the waveform shade is, the lower are I_d and therefore also the $\frac{dv}{dt}$ of the transition.

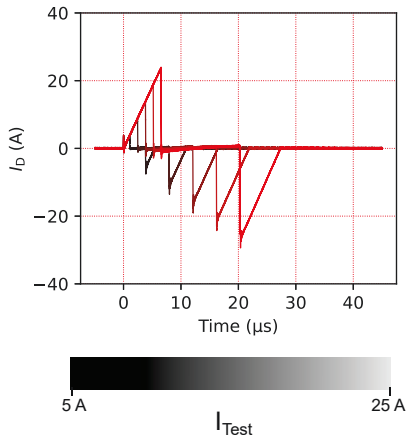


Figure 8.12. Drain current overview under soft-switching test. Shades indicate the test current level according to legend.

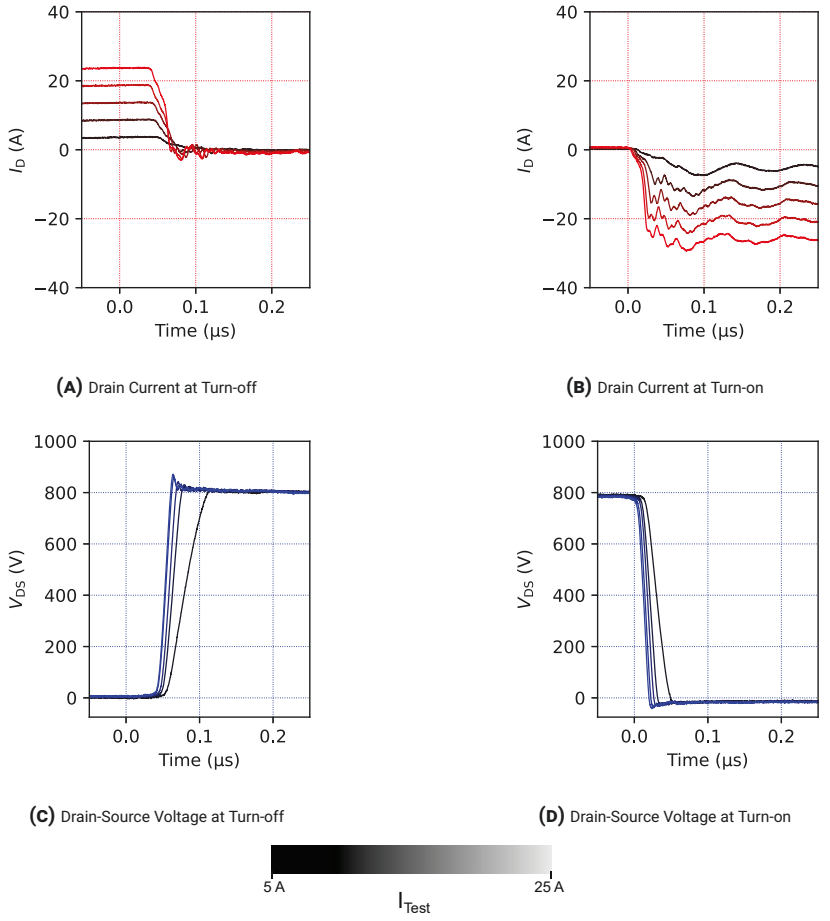
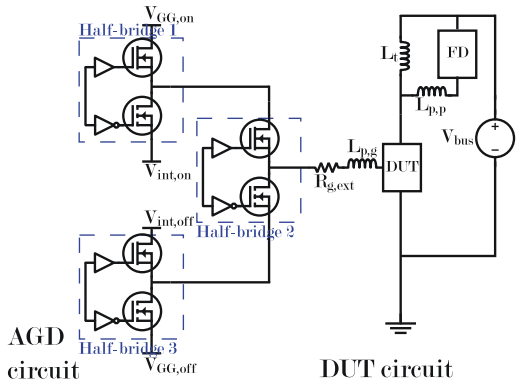
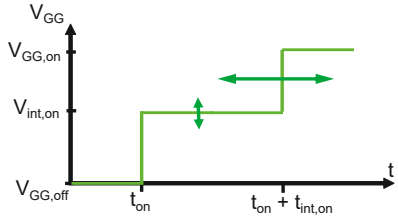


FIGURE 8.13. Soft-Switching Test Measurements at Turn-off (a, c) and at Turn-on (b, d). Shades indicate the test current level according to legend.



(A) Schematic Diagram [10]



(B) Ideal Turn-on Gate Driving Voltage Output of 4VLAGD [10]

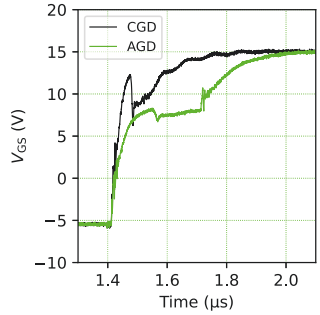
Figure 8.14. 4 Voltage Level Active Gate Driver [10]

8.3.3 *Evaluation of AGDs*

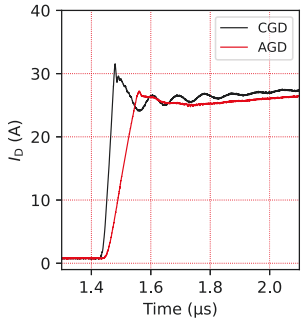
The LITP can be used to evaluate different types of gate drivers, including AGDs. This is enabled by the universal, low-inductive gate pads, which are marked by a green ellipsoid in Figure 8.1a. The only requirement of a gate driver that is to be tested with the proposed LITP is that it fits these gate pads. To demonstrate this, hard-switching DPT experiments were conducted using a Four Voltage Level AGD (4VLAGD) [10]. In contrast to conventional, two voltage level gate drivers, this AGD can provide a variable intermediate voltage level ($V_{\text{int,on}}$, $V_{\text{int,off}}$) during the switching procedures for a variable duration ($t_{\text{int,on}}$, $t_{\text{int,off}}$). Using these two degrees of freedom, the four voltage level AGD can manipulate $\frac{dv}{dt}$, $\frac{di}{dt}$, the reverse recovery current peak at turn-on I_{rr}, overshoot voltage at turn-off V_{os}, and the switching loss of the SiC DUT. Figure 8.14a shows the schematic diagram of this four voltage level AGD. To showcase the evaluation of this AGD, hard-switching turn-on experiments are conducted. The idealized gate driving voltage trajectory at turn-on is shown in Figure 8.14b.

	”AGD”	”CGD”
$t_{\text{int,on}}$	300 ns	20 ns
$V_{\text{int,on}}$	8.1 V	15 V

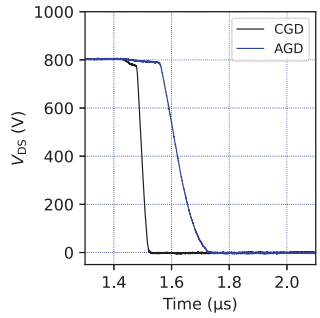
(A) Exemplary AGD Experiment Operation Points



(B) Gate-Source Voltage



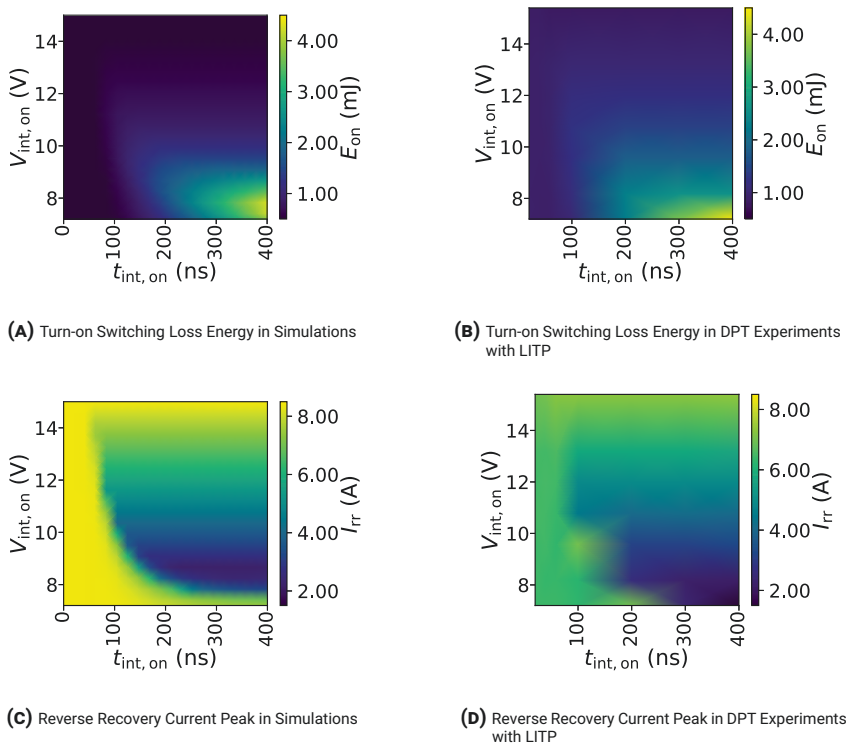
(C) Drain Current



(D) Drain-Source Voltage

FIGURE 8.15. 4 Voltage Level Active Gate Driver Evaluation Measurements at Turn-on, without (CGD) and with Intermediate Driving Voltage Level (AGD)

Exemplary measurement results are shown in Figure 8.15 showing the drain current, drain-source voltage and gate-source voltage for a conventional gate driving scheme in black, and with a 300 ns interval of 8.1 V intermediate driving voltage level during turn-on in green. The measurements clearly show that the gate charging process is significantly slowed down, and the gate source voltage is held at the intermediate voltage until the preconfigured duration of 300 ns has passed, to subsequently charge up to the high gate driving voltage of 15 V. The switching process is slowed down as expected, the reverse recovery peak is lowered visibly, and almost no oscillations can be observed in the drain current (red). Moreover, the $\frac{dv}{dt}$ is reduced from 20.95 kV μs^{-1} to 7.37 kV μs^{-1}, and the $\frac{di}{dt}$ is reduced from 702 A μs^{-1} to 328 A μs^{-1}. In addition, the switching loss is increased from 0.92 mJ to 2.56 mJ.



(A) Turn-on Switching Loss Energy in Simulations

(B) Turn-on Switching Loss Energy in DPT Experiments with LITP

(C) Reverse Recovery Current Peak in Simulations

(D) Reverse Recovery Current Peak in DPT Experiments with LITP

Figure 8.16. Simulation and Experiment Result Comparison at Turn-on

Both simulations and experiments were conducted, varying $t_{\text{int,on}}$ and $V_{\text{int,on}}$. For the simulations, the four voltage level active gate driver was approximated by an ideal voltage source, and a SPICE model of the C3M0075120K power MOSFET was used in both the DUT and FD position. A stray inductance of 5 nH was inserted into the drain path of the DUT and in the source path of the FD in the SPICE circuit model to represent the parasitic inductance caused by the test setup layout. The turn-on switching loss, E_{on} and the reverse recovery current peak, I_{rr} were calculated for every simulation and experiment. In Figure 8.16, the resulting E_{on} and I_{rr} values are visualized as heat maps. Despite slight deviations in both quality and quantity, simulation and experiment show very good agreement in both E_{on} and I_{rr}.

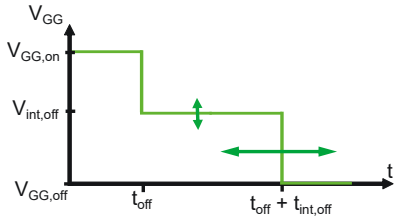
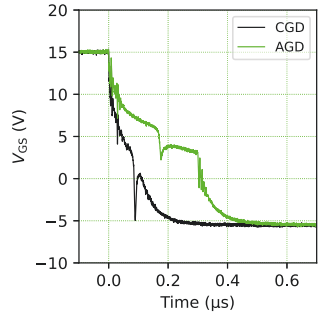


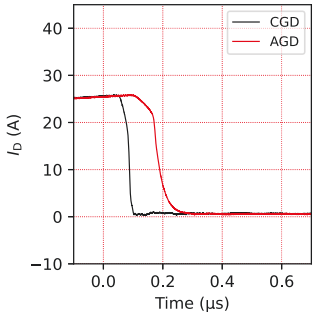
FIGURE 8.17. Ideal Turn-off Gate Driving Voltage Output of 4VLAGD [10]

	"AGD"	"CGD"
$t_{\text{int,off}}$	300 ns	20 ns
$V_{\text{int,off}}$	2.8 V	−4.7 V

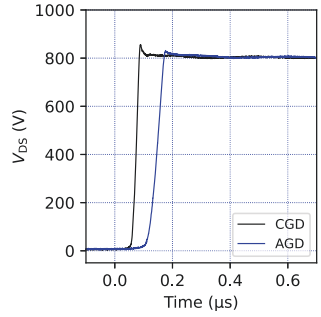
(A) Exemplary AGD Experiment Operation Points



(B) Gate-Source Voltage

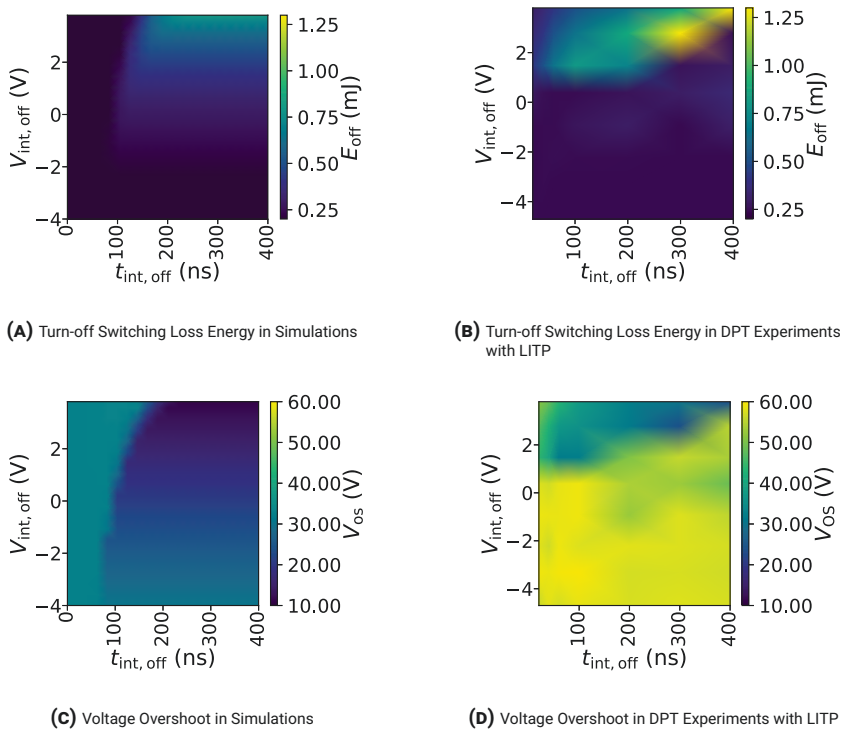


(C) Drain Current



(D) Drain-Source Voltage

FIGURE 8.18. 4 Voltage Level Active Gate Driver Evaluation Measurements at Turn-off, without (CGD) and with Intermediate Driving Voltage Level (AGD)



(A) Turn-off Switching Loss Energy in Simulations

(B) Turn-off Switching Loss Energy in DPT Experiments with LITP

(C) Voltage Overshoot in Simulations

(D) Voltage Overshoot in DPT Experiments with LITP

Figure 8.19. Simulation and Experiment Result Comparison at Turn-on

Analog to Figure 8.14b describing the idealized gate driving voltage trajectory at turn-on, Figure 8.17 shows the idealized gate driving voltage trajectory at turn-off. Exemplary measurement results are shown in Figure 8.18 showing the drain current, drain-source voltage and gate-source voltage for a conventional gate driving scheme in black, and with a 300 ns interval of a 2.8 V intermediate driving voltage level during turn-off in green. The measurements clearly show that the gate charging process is significantly slowed down, and the gate source voltage is held at the intermediate voltage until the preconfigured duration of 300 ns has passed, to subsequently discharge down to the low gate driving voltage of −5 V. The switching process is slowed down as expected, the voltage overshoot is lowered visibly, and almost no oscillations can be observed in the drain current (red). Moreover, the $\frac{dv}{dt}$ is reduced from 30.7 kV μs^{-1} to 19.9 kV μs^{-1}, and the $\frac{di}{dt}$ is reduced from 756 A μs^{-1} to 365 A μs^{-1}. In addition, the switching loss is increased from 250 µJ to 874 µJ.

Varying $t_{int,off}$ and $V_{int,off}$ in both simulations and experiments shows that the AGD can manipulate the switching loss energy at turn-off, E_{off}, and the drain-source voltage overshoot, V_{os}. Figure 8.19 shows E_{off} and V_{os} in comparison between simulations and experiments. Compared to the characteristics at

turn-on, deviations in both quality and quantity are more pronounced. The simulation predicts lower E_{off} than was measured in the experiments. Moreover, E_{off} exhibits a less homogeneous gradient in $V_{int,off}$ in experiments compared to simulations. The same holds for V_{os}. In addition, the absolute values of V_{os} are twice as large as what is predicted by the simulations, which points to an insufficient representation of the stray power loop inductance in the simulation circuit model and potential inaccuracy of the SPICE MOSFET model. Such significant deviations emphasize the need for a physical test setup that is capable of high accuracy dynamic measurements. In a following iteration, the simulation circuit and also the power device model could be improved to yield more realistic simulation results and thus a better estimate of the gate driver utility.

Besides being subject to characterization, AGDs can also be used as a tool to speed up the characterization process. For example, a variable resistor gate drive can be used to characterize the behavior of a switching device with varying external gate resistor values without the need for de-soldering one and soldering another component, which was shown with Si IGBTs in the past [14]. The 4VLAGD, used to produce the results shown above [10], can be used to investigate the switching behavior with various high gate driver voltage levels.

8.4 Discussion

8.4.1 Purpose of Characterization Data

As shown in Section 8.3, the proposed LITP is able to produce high quality characterization data of SiC power MOSFETs. This characterization data can be used to improve SiC power MOSFET simulation models. Previously, an efficient model adjustment method was studied with respect to static characterization data [33]. It is possible to adapt this method to include dynamic characterization data. This would require reducing the characterization data to a small set of specific values first. The right choice of these specific values and how to arrive at these values is an elaborate topic that is out of the scope of this work.

In addition, the LITP enables efficient evaluation of both conventional (two-voltage-level) and more advanced active gate driver units, assessing their ability to manipulate the switching transitions, especially for easier integration and better utilization of fast-switching SiC power MOSFETs. Furthermore, extracted parameters can be used for creating compound models of gate driver and switching device. High level simulation tools such as Matlab Simulink can then be used for efficient system control design, taking the extended control-

lability offered by AGDs into consideration. Finally, AGD-integrated control design can be accelerated using the proposed LITP.

8.4.2 *Guidelines for Low Inductive Circuit Design*

The low inductive design of the proposed LITP for SiC MOSFET characterization follows principles that are vital for reducing the influence of parasitic circuit impedances on measurement data. A circuit designer facing challenges with the reduction of Electromagnetic Interference (EMI), strong oscillations and device performance that falls behind component specification, may revisit the following aspects in their product.

- **Track length.**
  The most important aspect when creating a low inductive circuit is to cut back on what introduces inductance. Tracks on the PCB contribute most to avoidable parasitic inductance. Track length minimization is, however, partly limited by component geometry, as well as clearance and creepage demands depending on the voltage level, especially in converter circuits. Moreover, the power device packaging contributes significantly to the parasitic impedance. For example, the TO-247-3 industry standard packaging exhibits significant inductance caused by internal electrical connections between dies and package terminals.

  Unfortunately, device packaging cannot be improved during circuit design. In the case of a converter, choosing another device might be necessary if the negative effects of parasitic impedances are detrimental to the overall design requirements. Furthermore, in continuous converter operation, the losses generated in the power switching devices must be dissipated through a heat sink. Including a heat sink presents additional spatial restrictions, opposing track reduction and circuit minimization.

- **Decoupling.**
  Measures that decrease or eliminate the impact of disturbances, interference, and other non-ideal effects in a system are commonly referred to as decoupling. In the focus of this work, decoupling concerns the integration capacitors that provide stored energy from the supply close to the DUT and thereby decrease the impact of the inductance between the power supply and the DUTs. Oscillations can be suppressed, if the energy stored in these capacitors is large enough and not separated from the device electrically by a too large inductance. If space constraints impose challenges on capacitor placement close to the DUT, small outline components should be used despite their low capacitance. It is advisable

to use capacitors of different size and technology to balance out their different properties. Placing small capacitors near the DUT will help provide the energy needed for a fast commutation, while larger capacitors further away will act as a larger energy resource for the load current.

In practical converter circuits, space requirements also pose challenges on this inductance reduction measure. However, the LITP design proposed in this paper shows that placing capacitors with different dimensions on the different sides of a PCB can improve the decoupling while leaving space for thermal management.

- **Measurement Equipment.**
  Probes for measuring electrical quantities introduce parasitic capacitance (voltage sensors) and inductance (current sensors). Choosing the right sensor technology is therefore important to increase measurement data quality. Another aspect to take into account is the specification of the sensors, particularly, the sensor bandwidth. Finally, adequate probing points need to be designed. Optimally, probing points are as close as possible to the DUT to reduce measurement inductance. A large measurement inductance falsifies measurement results, as it reduces measurement bandwidth and makes the sensor more prone to induction of undesired signals originating from fast changing fields in the surrounding circuitry. To further improve EMI resilience, shielding is advisable. If available, tip adapters with a coaxial design offer effective shielding and thereby improve the measurement signals.

  In power converters, measurement points can be used for monitoring purposes, but they do not serve the main priority of power conversion. Hence, track length reduction and close placement of decoupling capacitors for parasitic inductance minimization are more important than the optimal inclusion of measurement terminals. However, recent gate drivers that require physical feedback for protection and switching optimization purposes, can only realize these functionalities if the feedback path is properly designed. In this case, this guideline is highly relevant for converter design as well.

8.4.3 Adaptation of the LITP for Different Packages

The LITP can be easily adapted to power devices with a different packaging. The TO-247-4 package has become a popular alternative to the TO-247-3 package. To reduce the common source inductance, the inductance that is shared by the source paths in the power and the gate loop, the TO-247-4

package features two separate source terminals. These terminals have separate wire bond connections to the semiconductor die inside the package. To adapt the LITP to this device, an additional pad with a respective pin connector would have to be included on the PCB, and the existing connection would have to be moved and connected to the copper layers according to the TO-247-4 terminal scheme.

D2PAK7 is another package that has gained popularity for power MOSFETs. This package is a surface-mount technology. This entails de-soldering one and soldering another device for the exchanging DUTs. Including the D2PAK7 footprint on the PCB is the only manipulation that is necessary to adapt the LITP for testing devices in this type of package.

SiC power MOSFET half-bridge modules are commercially available SiC power MOSFET modules in packages that were formerly used for Si IGBT modules. However, the parasitic inductance of the module and especially terminal layout is detrimental for fast-switching applications. Hence, manufacturers have released SiC power MOSFET modules in a variety of unique, low-inductive packages. Adapting the LITP to fit SiC power MOSFET modules would therefore require an individual adjustment of the LITP to a specific module.

8.5 Conclusion

A Low-Inductive Test Platform (LITP) for TO-247-3 devices was developed, comprising a PCB optimized for fast switching devices, and parameter extraction software. Circuit miniaturization through careful component placement and parasitic inductance reduction through track length minimization enable high quality characterization measurements of the drain current, drain-source voltage, and gate-source voltage of a power MOSFET. At the same time, the DUTs can be exchanged quickly and damage-free. General-purpose pads are used to connect a gate driver to the LITP, enabling both gate driver evaluation and power device characterization.

The LITP performance is comparable to the PD1500A dynamic power device characterizer from Keysight, a commercial product serving as the reference for this application. The parameter extraction software is able to determine key power device switching characteristics according to the IEC 60747-8 standard [21] and was verified against the reference. In conjunction to soft- and hardware, the proposed LITP presents a flexible, modular, and high-accuracy characterization tool for both SiC MOSFETs and Gate Driver Units under both hard- and soft-switching conditions, which was verified in extensive experimental work.

8.6 Acknowledgement

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Chapter 9

Four Level Voltage Active Gate Driver for Loss and Slope Control in SiC MOSFETs

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Contributions

- Brief review of various AGD concepts with advantages and disadvantages

- Development and evaluation of a Four Level Multilevel Voltage Source Gate Driver including key design aspects

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Abstract

Silicon Carbide power semiconductors exhibit fast dynamic behavior. This facilitates the design of high efficiency and high power density converters. However, the resulting current and voltage changing rates demand extensive filtering to avoid electromagnetic interference and ensure safe operation. In addition, temperature fluctuations due to varying load currents from renewable energy sources pose challenges for power semiconductor device lifetime and reliability. Active temperature control can reduce temperature fluctuations, but affects switching slopes simultaneously. This leads to variable electrical stress on both device and circuit level. In this paper, a four-level active voltage-source gate driver for SiC MOSFETs is proposed, enabling manipulation of switching and conduction losses. Switching losses are manipulated by controlling the duration as well as amplitude of intermediate gate voltage pulses during switching transients. Conduction losses can be influenced by adjusting the positive gate voltage. Simulations indicate that the proposed gate driver allows decoupling switching loss and slope control. To validate the gate driver concept, a prototype has been built and evaluated in double pulse test experiments.

9.1 Introduction

Silicon Carbide (SiC) based Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFETs) exhibit faster switching dynamics and lower on-state resistance for the same blocking voltages compared to their Silicon Insulate-Gate Bipolar Transistor counterparts [1]. Their fast switching speed means high voltage change rates (dv/dt) and current change rates (di/dt), that can cause strong Electromagnetic Interference (EMI), crosstalk, and potentially, a shoot-trough fault [2].

In addition, renewable energy sources, such as photovoltaics and wind power, have an intermittent power generation profile that translates into a varying converter load current. The resulting switching device loss and temperature fluctuations expedite bond-wire lift-off and solder delamination, which are major failure modes in power semiconductor devices [3]. active temperature control can reduce the amplitude of temperature stress cycles and thereby improve device reliability and lifetime [4; 5].

Several Active Gate Driver (AGD) concepts that enable active temperature control by providing power loss manipulation during switching events as well as the conduction phase, have been presented in literature [2; 4; 5; 5–9]. Current-source gate drivers allow precise gate capacitance charging and

thereby switching transient control [6–8]. However, current control necessitates a high precision variable voltage source and a high bandwidth signal path to control it. This is needed to either set the operating point of a current mirror or saturation current source configuration of a semiconductor switch. As a consequence, current source type gate drivers are complex and prone to parameter drift as well as EMI.

Step-wise gate drivers alter the gate charging dynamics by activating a variable number of parallel output stages with different or identical serial resistors [3; 10; 11]. This approach exhibits an easier control than current source gate drivers because unlike controlled current sources, the paralleled output stages are simple topologies, and high precision resistors are easily available. With emerging digital electronics, a large amount of parallel output stages enables fine grain control of the gate charging process [10]. However, large digital bandwidths or complex digital signal sources such as Complex Programmable Logic Devices (CPLD) or Field Programmable Gate Arrays (FPGA) are needed on the gate driver, increasing EMI vulnerability. Besides, the necessary circuit layouts and components are both complex and costly.

Multilevel voltage gate drivers offer a compromise between power switch controllability and gate driver complexity. Intermediate voltage pulses with an amplitude between the positive and negative gate voltage during the switching transitions are produced by this gate driver type. Either the amplitude [2] or the timing [9] of these intermediate voltage pulses are controlled. This allows for switching loss, switching slope, and voltage as well as current overshoot control. Controlling either intermediate voltage pulse amplitude or timing, however, leaves transient slopes and switching loss coupled and inseparable of each other.

This paper introduces a four level voltage active gate driver capable of manipulating switching losses and transient slopes of a discrete SiC MOSFETs. Variable intermediate voltage levels are supplied to the gate with a configurable duration during turn-on and turn-off. The proposed gate driver can influence the switching losses, switching slopes as well as voltage and current overshoot of SiC MOSFETs, extending the capabilities of earlier presented gate drivers [2; 9]. In addition, conduction losses are controllable by an adjustable positive gate voltage.

The rest of the paper is organized as follows: In Section 9.2, the proposed gate driver is introduced, and the operational principle is explained. Section 9.3 shows the simulation results and Section 9.4 presents the experimental results. In addition, the impact of the gate driver on the SiC MOSFET performance is discussed, and the results are analyzed in these sections. Finally, conclusions are presented in Section 9.5.

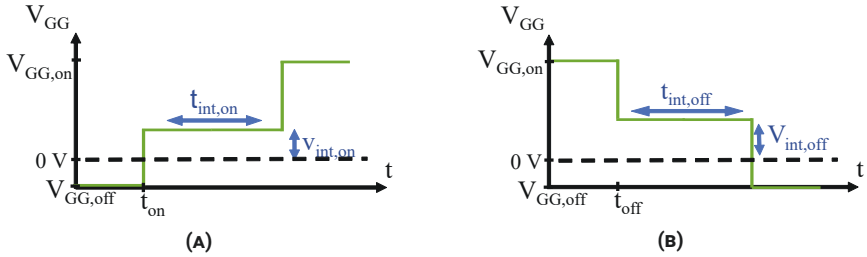


FIGURE 9.1. V_{GG} waveform during turn-on (a) and turn-off (b)

9.2 PROPOSED FOUR LEVEL VOLTAGE ACTIVE GATE DRIVER

The aim of the proposed active gate driver is to control the switching slopes and the switching loss of SiC power MOSFETs. To achieve this goal, a multilevel voltage gate driver applies an intermediate voltage level during switching that is between the positive and negative driving voltages. Thereby, the gate charging process can be controlled, which in turn influences the voltage and current transitions of the switching device and thus, the switching loss.

Figure 9.1a and Figure 9.1b show the proposed turn-on and turn-off gate driver output voltage (V_{GG}) pattern. Before the turn-on switching instance ($t < t_{on}$), V_{GG} equals the turn-off driving voltages $V_{GG,off}$, and the MOSFET is kept in the off state. At $t = t_{on}$, the driver voltage is raised to the intermediate turn-on voltage $V_{int,on}$. This voltage level is held for the duration of the intermediate turn-on voltage level $t_{int,on}$. Afterward, V_{GG} is switched to the turn-on driving voltage $V_{GG,on}$ and held at this voltage value until the next switching instance. At turn-off, this procedure is repeated. Both the intermediate turn-off voltage level $V_{int,off}$ and the duration of the intermediate turn-off voltage level $t_{int,off}$ are chosen independently of their correspondents at turn-on.

In a conventional gate driver, a simple step is applied to the gate. Introducing an intermediate voltage step will add a degree of freedom to the gate charging speed. If, for example, a lower intermediate voltage level than the positive gate voltage is applied to the gate at turn-on, the gate charging process is slowed down. Depending on the duration of the intermediate voltage level, the slower gate charging process will slow down the current and voltage transitions. In addition, the switching loss is increased by prolonging the switching process.

Different operation schemes have been presented in literature [2; 9]. These differ from the proposed scheme of driving the multilevel voltage gate driver. Between the intermediate voltage level intervals and the high driving voltage, an interval of low driving voltage is inserted [2; 9] and varied in duration [9].

Initially, introducing a variable time delay before the intermediate voltage

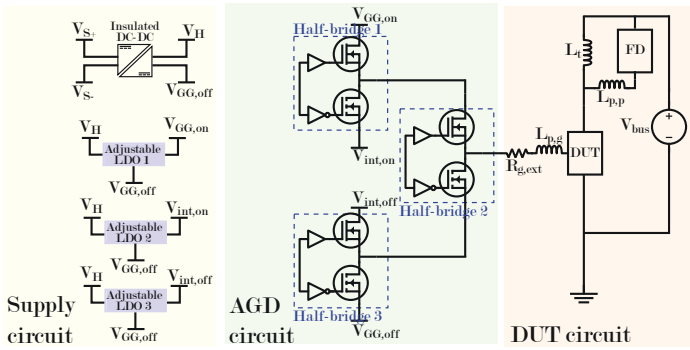


FIGURE 9.2. Schematic diagram of the proposed gate driver

level was considered. However, simulations showed that altering these time delays had a similar impact to altering the duration of the intermediate voltage levels ($t_{\text{int,on}}$ and $t_{\text{int,off}}$ in Figure 9.1a and Figure 9.1b). Therefore, the delay variation was not further investigated.

A circuit that can provide the desired voltage pattern has been derived. The schematic diagram of this proposed gate driver is shown in Figure 9.2. The gate-drive circuit consists of two parts, the AGD circuit and the supply circuit. As can be seen from Figure 9.2, three half-bridge circuits are used to provide the four voltage levels to the gate. Three of the four voltage levels are variable. They are provided by adjustable low-dropout regulators (LDO), which can be seen in the supply circuit part of Figure 9.2. This particularly includes the positive gate voltage, permitting control of the active region of the power MOSFET and thereby conduction losses.

To verify the functionality of the gate driver topology seen in Figure 9.2, a gate driver prototype was built and tested. A photo of the prototype circuit is shown in Figure 9.3. The supply circuit, which is not shown in the picture, is located behind the main gate driver board. The output voltage of each adjustable LDO is controlled using a digital potentiometer inside the LDO feedback loop. This digital potentiometer is controlled over SPI.

Both the signals required to create the desired patterns and the SPI signals to set the intermediate voltage levels are generated by a C2000 series microcontroller by Texas Instruments [12]. This microcontroller also provides the gate signals for the balancing circuit of the test setup that compensates for any imbalances that result from repeated double pulse tests [13].

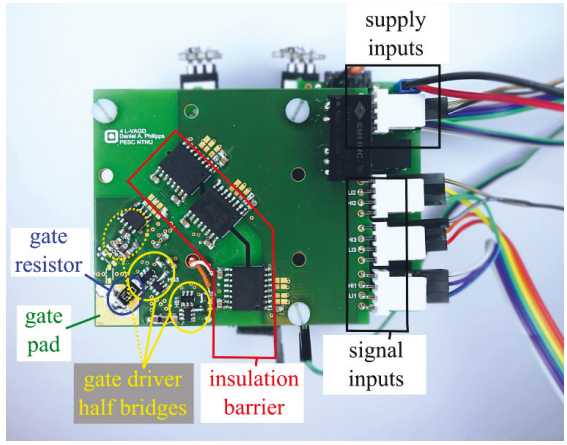


FIGURE 9.3. Photo of proposed AGD. The source pad is located on the back side of the PCB, directly behind the gate pad.

TABLE 9.1. Circuit parameters used during simulations

V_{bus}	I_{load}	$R_{g,ext}$	L_t	$L_{p,g}$	$L_{p,p}$	T_{amb}
800 V	20 A	25 Ω	110 µH	1 nH	5 nH	25 °C

9.3 SIMULATION RESULTS

To investigate the functionality and the electrical performance of the gate driver topology seen in Figure 9.2, a simulation study was conducted. In this simulation study, hard-switching conditions of a double-pulse test were imposed on a MOSFET model that is driven by a model of the gate driver.

9.3.1 Circuit Modelling

The circuit parameters used in the simulation are summarized in Table 9.1. V_{bus} is the DC-link bus voltage, I_{load} the load current and $R_{g,ext}$ the external gate resistance. The load inductance is L_t, while $L_{p,g}$ and $L_{p,p}$ are the parasitic inductances in the gate and power loop respectively. T_{amb} denotes the ambient temperature. A model of the Wolfspeed Silicon Carbide Power MOSFET C3M0075120K was used both as the Device Under Test (DUT) and the Freewheeling Device (FD). This model is a modified version of the manufacturer model, optimized for eliminating convergence errors [14].

9.3.2 Gate Driver Modelling

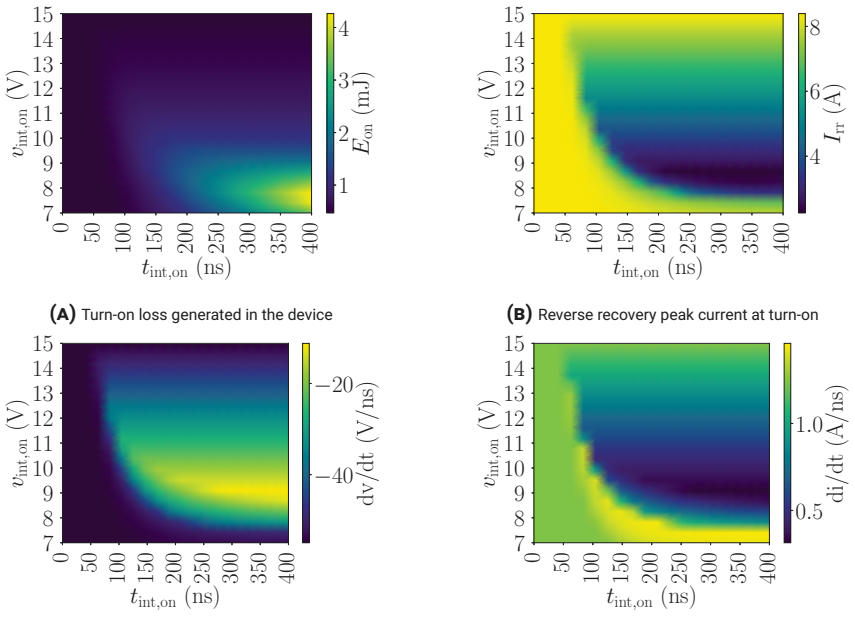
An idealized model of the proposed gate driver was used for the simulations. It consists of an ideal voltage source providing the proposed gate voltage pattern and an external gate resistor. The voltage changing times of the voltage source were set to 1 ns. In a real application, the low power MOSFETs of the output stage are expected to provide slightly slower slopes. However, the power MOSFET input capacitance is so large, that this is expected to dominate the gate voltage dynamics instead of the low power MOSFETs. Hence, modelling the gate driver as described above is considered adequate.

The values of $V_{\text{int,on}}$ were varied from 7 V to 15 V, and $V_{\text{int,off}}$ from −4 V to 4 V. The pulse durations $t_{\text{int,on}}$ and $t_{\text{int,off}}$ were varied from 0 ns to 400 ns. The turn-on driving voltage was set to $V_{\text{GG,on}} = 15\,\text{V}$ and the turn-off driving voltage was set to $V_{\text{GG,off}} = -5\,\text{V}$. The performance of the proposed gate driver was examined by looking at the turn-on switching loss E_{on}, reverse recovery current peak I_{rr}, turn-off switching loss E_{off}, voltage overshoot V_{os}, dv/dt, and di/dt. I_{rr} is calculated from the simulation results as the difference between peak reverse recovery current and load current. Similarly, V_{os} is determined as the peak overshoot voltage minus the DC bus voltage. Turn-on and turn-off transients were investigated separately.

9.3.3 Simulation Results Discussion

Figure 9.4 illustrates various switching characteristics at turn-on under variation of $t_{\text{int,on}}$ and $V_{\text{int,on}}$. From Figure 9.4, the impact of altering $t_{\text{int,on}}$ and $V_{\text{int,on}}$ is clearly visible. For some $V_{\text{int,on}}$ values, changing $t_{\text{int,on}}$ has no significant effect on the presented performance parameter values. For $V_{\text{int,on}}$ values $\lessapprox 12\,\text{V}$, increasing $t_{\text{int,on}}$ leads to higher E_{on}. If $V_{\text{int,on}} \gtrapprox 12\,\text{V}$, altering $t_{\text{int,on}}$ has a negligible impact on E_{on}. The impact of $V_{\text{int,on}}$ and $t_{\text{int,on}}$ on I_{rr} and di/dt is very similar. If $t_{\text{int,on}}$ is below approximately 50 ns, changing $V_{\text{int,on}}$ has almost no impact. For the turn-on switching transient, there is a clear region where the AGD is able to impact I_{rr} and di/dt. This region is where $t_{\text{int,on}} \gtrsim 50\,\text{ns}$ and $V_{\text{int,on}} \in [\,8\,\text{V}, 13\,\text{V}]$. The behavior of dv/dt (Figure 9.4c) is similar to I_{rr} and di/dt, but the impact of $V_{\text{int,on}}$ and $t_{\text{int,on}}$ is inverted.

Figure 9.5 illustrates various switching characteristics at turn-off under variation of $t_{\text{int,off}}$ and $V_{\text{int,off}}$. Altering $t_{\text{int,off}}$ and $V_{\text{int,off}}$ has a similar impact on all four switching characteristics. As can be seen in Figure 9.5, there is a range of $t_{\text{int,off}}$ values where altering $V_{\text{int,off}}$ has a negligible impact on the switching characteristics. This range increases with increasing $V_{\text{int,off}}$. At $V_{\text{int,off}} = -4\,\text{V}$, $t_{\text{int,off}}$ must be greater than approximately 60 ns before a large change



(A) Turn-on loss generated in the device

(B) Reverse recovery peak current at turn-on

(C) dv/dt at turn-on generated in the device

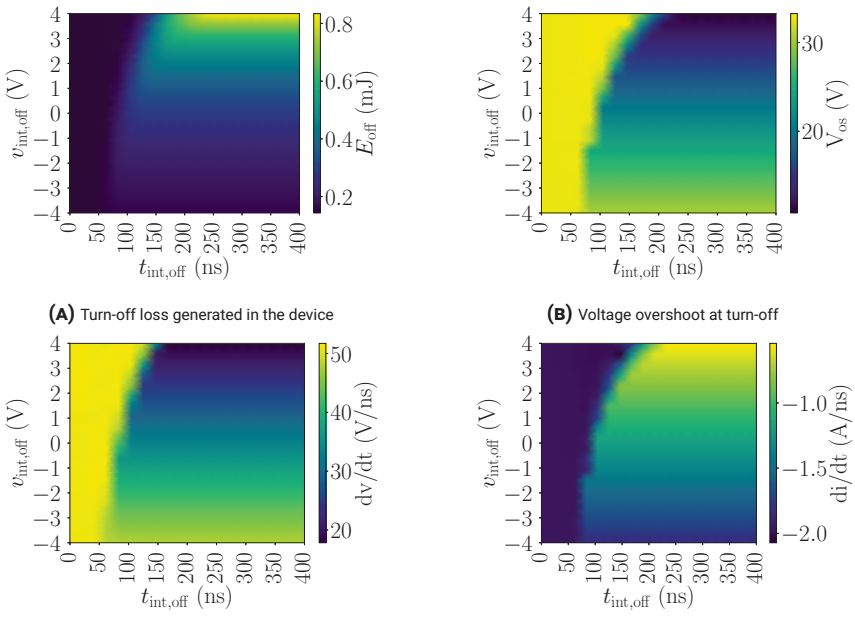
(D) di/dt at turn-on generated in the device

Figure 9.4. Influence of $V_{\mathrm{int,on}}$ and $t_{\mathrm{int,on}}$ on performance parameters during turn-on

in the switching characteristics is observed. When $V_{\mathrm{int,off}} = 4\,\mathrm{V}$ the large change happens when $t_{\mathrm{int,off}} \gtrapprox 175$ ns. In general, E_{off} and di/dt increases by increasing $V_{\mathrm{int,off}}$, while V_{os} and dv/dt decrease by increasing $V_{\mathrm{int,off}}$.

The simulation results show that the proposed AGD enables control of the switching performance of discrete SiC MOSFETs. By introducing an intermediate voltage level during switching, the voltage drop across the external gate resistor can be actively lowered. The result is a lower gate current, charging the MOSFET input capacitance more slowly, and thus the switching transients are slowed down. Since the external gate resistor is fixed, the amplitude of the intermediate voltage level, i.e. $V_{\mathrm{int,on}}$ or $V_{\mathrm{int,off}}$ respectively, determines the gate current and thus, the switching slope. This can be seen in Figure 9.4 for $t_{\mathrm{int,on}} \gtrapprox 75$ ns and $V_{\mathrm{int,on}} \gtrapprox 7.5\,\mathrm{V}$. In this region, changing $V_{\mathrm{int,on}}$ affects the switching slope. Decreasing $V_{\mathrm{int,on}}$ slows down the switching slope, causing increased E_{on} and dv/dt, while reducing I_{rr} and di/dt. Increasing $V_{\mathrm{int,on}}$ has the opposite effect on the switching characteristic.

The intermediate voltage amplitude is not immediately reflected at the gate of the MOSFET since the external gate resistor and the MOSFET input capacitance form a low-pass filter. Varying the duration of the intermediate voltage level therefore determines, for how long the slowdown described above is in effect, if it is shorter than the time constant of the RC low-pass filter mentioned



(A) Turn-off loss generated in the device

(B) Voltage overshoot at turn-off

(C) dv/dt at turn-off generated in the device

(D) di/dt at turn-off generated in the device

FIGURE 9.5. Influence of $V_{\text{int,off}}$ and $t_{\text{int,off}}$ on performance parameters during turn-off

above. If it is significantly longer, it determines the operating point that the MOSFET is held in with the respective $V_{\text{int,on}}$ and $V_{\text{int,off}}$ values. In Figure 9.4 and Figure 9.5, this impact can be seen. If the duration of the intermediate voltage levels ($t_{\text{int,on}}$ and $t_{\text{int,off}}$) are too short, $V_{\text{int,on}}$ and $V_{\text{int,off}}$ have a strongly reduced influence. This can be seen in Figure 9.5, where a short $t_{\text{int,off}}$ value causes $V_{\text{int,off}}$ having a negligible impact on the switching performance. The duration of $t_{\text{int,off}}$ required for $V_{\text{int,off}}$ to have a large impact on switching performance changes based on the value of $V_{\text{int,off}}$. For values of $V_{\text{int,off}}$ closer to $V_{\text{GG,off}}$, already shorter durations of $t_{\text{int,off}}$ lead to large changes in switching performance compared to more positive values of $V_{\text{int,off}}$. That is because more positive $V_{\text{int,off}}$ values slowing down the switching process.

9.3.4 *Switching Transient Control*

For each switching instance, there are two control variables to manipulate the MOSFET switching performance: $V_{\text{int,on}}$ and $t_{\text{int,on}}$ for turn-on; $V_{\text{int,off}}$ and $t_{\text{int,off}}$ for turn-off. In designing an effective and stable control, the following aspects have to be considered. Controlling the MOSFET behavior requires less precision in the control system in regions, where the controlled variable

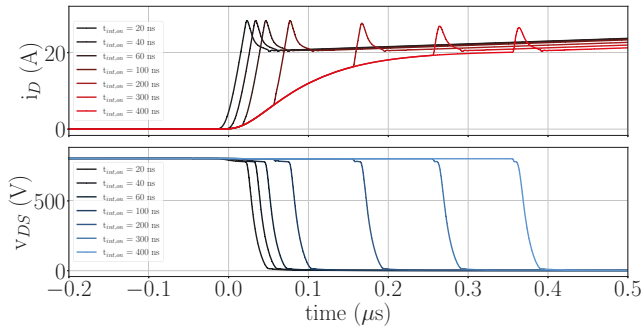


FIGURE 9.6. Simulated drain current I_d and drain-source voltage V_{ds} waveforms under variation of $t_{int,on}$

exhibits small gradients. For example, 9.4c shows that for $t_{int,on} \gtrapprox 250$ ns, varying $V_{int,on}$ from 7 V to 9 V has the same effect as varying it from 15 V to 9 V. However, the gradients are greatly different. As earlier mentioned, high precision voltage control is challenging. Hence, a variation of $V_{int,on}$ between 9 V to 15 V is more desirable for dv/dt control.

On the other hand, to achieve decoupling of the voltage and current slopes (dv/dt and di/dt) and the switching loss, additional requirements on the choice of control variable combinations must be accepted. For the turn-on transient (Figure 9.4), $V_{int,on} \approx 7$ V and $t_{int,on} \in [\,150$ ns, 400 ns$]$, the turn-on energy E_{on} can be altered without large changes in dv/dt and di/dt by varying $t_{int,on}$. If $V_{int,on} \in [\,11$ V, 15 V$]$ and $t_{int,on} \in [\,100$ ns, 400 ns$]$, dv/dt and di/dt can be manipulated without incurring large changes in E_{on}. For the turn-off transient (Figure 9.5), the voltage and current slopes can be changed without large changes in E_{off} if $t_{int,off} \gtrapprox 100$ ns and $V_{int,off} \lessapprox -2$ V.

9.3.5 *Exemplary Time Domain Simulation Data Evaluation*

To investigate the accuracy of the simulations and to directly compare simulations to experiments, exemplary time domain simulation data is shown in Figure 9.6. The $V_{int,on}$ and $t_{int,on}$ values of these simulations equal the configuration of the experiments that will be shown in Section 9.4.

Based on the waveforms in Figure 9.6 E_{on}, I_{rr}, di/dt and dv/dt were calculated in the same way as Figure 9.4 and Figure 9.5. These switching performance parameters can be seen in Figure 9.7.

9.4 EXPERIMENTAL RESULTS

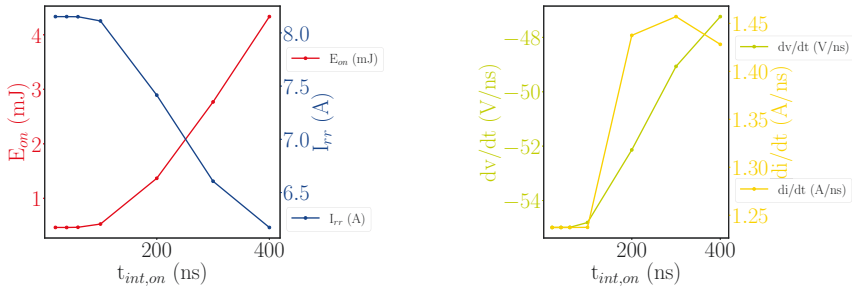


FIGURE 9.7. Simulation MOSFET switching performance parameters

9.4.1 *Description of the Test Setup and Measurement System*

A prototype of the proposed AGD was built and tested with a Wolfspeed C3M0075120D Silicon Carbide Power MOSFET [15]. The DUT and FD were mounted on a low inductive test platform that is optimized for dynamic characterization of high switching speed wide bandgap MOSFETs [16]. This platform has sockets for measuring the gate-source voltage V_{gs} and V_{ds}. V_{gs} was measured using a Tektronix TPP1000 passive voltage probe [17], V_{ds}, using a Keysight 10076C passive voltage probe [18]. I_d was measured using an SDN-414-05 co-axial current viewing resistor from T&M Research Products Inc. [19]. The measurements were recorded with a Tektronix DPO5104B oscilloscope [20].

9.4.2 *Gate-Source Voltage Measurement*

To verify the functionality of the proposed gate driver, experiments were performed with a DC bus voltage of 0 V first. The gate source voltage measurements of these experiments are shown in Figure 9.8. Despite the low-pass filtering effect of the MOSFET input capacitance and the external gate resistor, the AGD prototype is able to generate the proposed gate voltage pattern. $v_{\text{int,on}}$ and $v_{\text{int,off}}$ were varied from low to a high value. $t_{\text{int,on}}$ and $t_{\text{int,off}}$ were varied from a short to a long duration.

9.4.3 *High Power Experiments*

An exemplary full series of $t_{\text{int,on}}$ values and a single $V_{\text{int,on}}$ value were used for the experiments. The experiment parameters are summarized in Table 9.2.

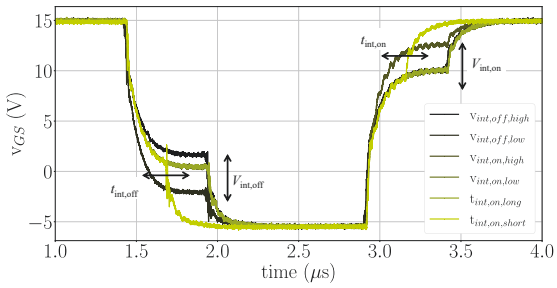


FIGURE 9.8. V_{gs} measurements at $V_{\text{DC}} = 0\,\text{V}$ varying $v_{\text{int,on}}$ and $t_{\text{int,on}}$ with the proposed gate driver

TABLE 9.2. $t_{\text{int,on}}$ and $v_{\text{int,on}}$ values used during experiments

$t_{\text{int,on}}\,[ns]$	20	40	60	100	200	300	400
$v_{\text{int,on}}\,[V]$	7.5						

The experiments were performed at a load current of 20 A, a load inductance of 100 µH, a DC-link bus voltage of 800 V, and an external gate resistance of 25 Ω. Time domain measurements are presented in Figure 9.9. The performance parameters presented in Figure 9.10 are the same as those highlighted in Section 9.3 and were defined and calculated in the same way.

Figure 9.8, Figure 9.9 and Figure 9.10 prove the ability of the proposed AGD to impact the turn-on switching transient of the DUT. The proposed AGD prototype operates as expected.

Increasing the duration of $t_{\text{int,on}}$ has a clear impact on V_{gs} and I_{d}. Especially for higher values of $t_{int,on}$ (300 ns and 400 ns), the proposed AGD significantly reduces voltage and current slopes.

9.4.4 *Experiment and Simulation Results Comparison*

Comparing Figure 9.6 and Figure 9.9, some differences become clear. In simulations (Figure 9.6), the intermediate voltage level at $V_{\text{int,on}} = 7.5\,\text{V}$ has a purely delaying effect on the voltage commutation, dv/dt remains constant in good approximation. Meanwhile, in experiments (Figure 9.9), V_{ds} has a delaying effect on the voltage commutation for small values of $t_{int,on}$, but also reduces dv/dt for higher values of $t_{int,on}$. The drain current, I_{d} is relatively similar in Figure 9.6 and Figure 9.9 except from excessive oscillations in the experimental results and a higher I_{rr} in the simulations. This is caused by differences between the simplified circuit model and the real circuit, as well as the SPICE MOSFET and switching device. The circuit parasitics are reduced to a single power loop

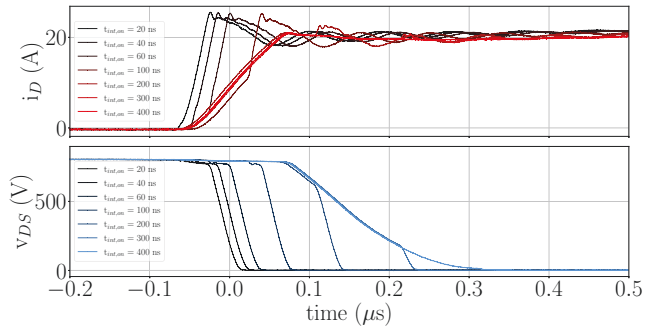


FIGURE 9.9. Experimental turn-on I_d and V_{ds} waveforms showcasing impact of altering $t_{int,on}$

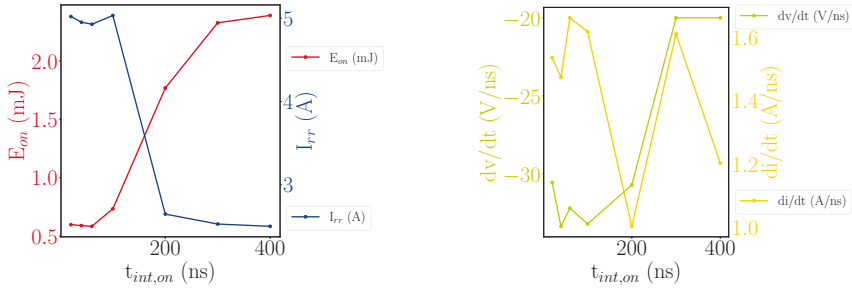


FIGURE 9.10. Experimental MOSFET switching performance parameters

inductance for the simulation, whereas in reality, multiple parasitic inductances and capacitances are distributed throughout the circuit and interact with each other. Previous work has shown that, among other aspects, especially the quasi-saturation and saturation regions are not well represented in manufacturer SPICE models [21]. Simulated saturation currents are therefore lower than what can be found in experiments. This can explain the deviation between simulation and experiment.

9.5 CONCLUSION

This paper presents an active variable four-level voltage gate driver for SiC MOSFETs. Intermediate voltage pulses, that are configurable in amplitude and duration, can be applied to the gate during switching and thereby control the switching transients. An extensive simulation study has demonstrated the potential of the proposed gate driver to decouple voltage and current slopes (dv/dt and di/dt) and the switching losses (E_{on} and E_{off}) to a certain degree, if the control variables ($V_{\text{int,on}}$, $V_{\text{int,off}}$, $t_{\text{int,on}}$ and $t_{\text{int,off}}$) are chosen accordingly.

A prototype of the proposed gate driver has been built and tested on a Wolfspeed C3M0075120D Silicon Carbide Power MOSFET. Sample measurements have been presented in this paper. Both simulation and experimental results show that the AGD is able to control E_{on}, I_{rr}, dv/dt and di/dt in the DUT during switching.

9.6 Acknowledgement

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Chapter 10

A Three-Level Voltage-Source Gate Driver for SiC MOSFETs in Synchronous Rectification Mode

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Contributions

- Theoretical model of the voltage peak occurring after inductive turn-off of a synchronous rectifier
- Three Level MLVSGD for voltage peak reduction in synchronous rectifiers succeeding inductive turn-off
- Experimental validation with a model circuit (flyback converter)

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Abstract

The fast-switching behavior of Silicon Carbide (SiC) Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFETs) has made these devices an ideal technology for high-frequency converters. However, parasitic circuit layout and other stray inductances in combination with the high di/dt and the device output capacitance cause excessive voltage overshoot across the MOSFETs. This paper presents a three-level voltage source gate driver suitable for minimizing the voltage overshoot in SiC MOSFETs operating in synchronous rectification mode. The operating principle of the driver relies on the trajectory of the gate-source voltage of the SiC MOSFET, which is adjusted in order to operate the device in the active region. The driver's performance has been experimentally validated on a synchronous DC/DC flyback converter rated at 70 V and 500 W. From the experiments, it is observed that using the proposed gate driver, the overvoltage across the SiC MOSFETs is minimized by approximately 13 % compared to a conventional Two Level gate driver.

10.1 Introduction

Silicon Carbide (SiC) Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFETs) have shown to outperform the efficiency of Silicon technology in a variety of applications [1–3]. In power converters requiring synchronous rectification, switching devices need to be reverse conductive. SiC MOSFETs are capable of reverse current conduction, not only through the intrinsic body diode, but also through the channel. Under high-current operation, the conduction losses in conventional power diodes become excessive [4]. Reverse current conduction through the power MOSFET channel can therefore significantly reduce conduction power losses [5]. However, when using SiC MOSFETs in synchronous rectification mode, switching transients and their inherent loss as well as voltage overshoot need to be considered.

Switching loss and overshoot voltage minimization in SiC MOSFETs have been previously investigated in literature [6; 7], with focus on forward conducting operation. When used in synchronous rectification mode, however, the SiC power MOSFETs conduct reverse currents.

The turn-off transition of the SiC power MOSFET in the synchronous rectifier position exhibits a significantly larger overvoltage than in forward conduction. This originates from a resonant oscillation between the output capacitance of the MOSFET and the stray inductances of the flyback transformer, as well as PCB track inductances.

To withstand this overvoltage, SiC power MOSFETs are therefore over-dimensioned with respect to their breakdown voltage. Compared to devices with a lower blocking voltage, both investment cost and conduction losses are higher, as the longer drift region needed to block higher voltages requires more material and introduces a higher drift resistance.

One approach to mitigate the voltage overshoot of a SiC power MOSFETs is to utilize passive snubber circuits [8]. However, passive snubber circuits introduce additional losses and increase the size and the cost of the rectifier due to the use of additional capacitors and diodes. Alternatively, Active Gate Drivers (AGDs) can be used to reduce the overshoot voltage while providing a smaller rectifier footprint and considerably reducing losses compared to passive clamping methods at the cost of increased drive circuitry complexity.

As opposed to conventional gate drivers that provide either of two fixed voltages to the gate of a MOSFET to turn it on or off, AGDs offer precise control over the MOSFET switching transitions. This control is achieved by manipulating the input capacitance charge trajectory either directly applying gate current control with a Current Source Gate Driver (CSGD), or indirectly with either a Multilevel Voltage Source Gate Driver (MLVSGD) or a Variable External Resistor Gate Driver (VERGD).

CSGDs are based on a low-voltage MOSFET driven in the saturation region and acting as a current source [9] (referred to as CSGD type 1a below), a current mirror [10; 11] (referred to as CSGD type 1b below), or an inductor releasing part of its stored energy into the switching device input capacitance [12; 13] (referred to as CSGD type 2 below). CSGDs enable effective switching behavior control, and CSGDs of type 2 are suitable for fast switching. However, CSGD types 1a and 1b require high-precision, high-bandwidth voltage or current sources, and CSGD type 2 might introduce high losses in the inductor and requires complex control. Furthermore, type 2 CSGDs are potentially unstable, e.g. in case of open power device terminals. VERGDs have been shown to effectively control the switching trajectory of MOSFETs [14] without the need for a high-precision voltage or current source. However, numerous active and passive components are required for this gate driver type, as well as a Complex Programmable Logic Device (CPLD), Field Programmable Gate Array (FPGA), or an Application Specific Integrated Circuit (ASIC) to realize the variable resistor.

MLVSGDs have been demonstrated for di/dt, dv/dt, and switching loss control, but also for limiting surge voltages during switching [15–17]. Implementations of this gate driver type require one or more controllable voltage sources that increase gate driver losses [16; 17], while others only need a fixed third voltage supplied by a suitable low-power, low-cost DC/DC converter [15]. With a suitable choice of voltage levels, MLVSGDs can be also used to

increase switching speed and thereby enable fast switching [18]. AGDs and AGD driving strategies found in literature focus on applications under forward conduction. This study, however, focuses on improving the operating conditions of switching devices operated as a reverse conducting synchronous rectifier.

This paper proposes a three-level MLVSGD suitable to minimize the voltage overshoot across SiC MOSFETs operating in synchronous rectification mode. In comparison to conventional Two Level gate drivers, the proposed gate driver provides an additional gate voltage level to slow down the switching process, aiming at minimizing overvoltages. The paper is organized as follows. Section 10.2 analyses the mechanism that causes the observed overvoltages across the synchronous rectifier by considering a flyback converter as an example. Subsequently, the design and operation of the proposed three-level MLVSGD for overvoltage minimization is presented. Section 10.3 presents the experimental validation of the proposed gate driver applied in a synchronous flyback converter. Finally, Section 10.4 summarizes the key conclusions of this work.

10.2 ENHANCING SYNCHRONOUS RECTIFICATION WITH A THREE-LEVEL MLVSGD

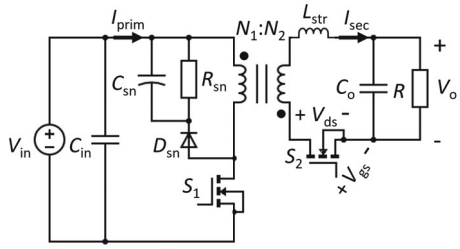


FIGURE 10.1. Schematic diagram of a synchronous DC/DC flyback converter.

The operating principle of the proposed three-level MLVSGD will be analyzed in a synchronous flyback converters, as shown in the schematic diagram in Figure 10.1. The secondary switch S_2 operates in synchronous rectification mode, and it is the device considered for this investigation. With its output capacitance C_{oss}, the synchronous rectifier introduces a considerable capacitance in the secondary side of the converter. C_{oss} comprises the terminal capacitances

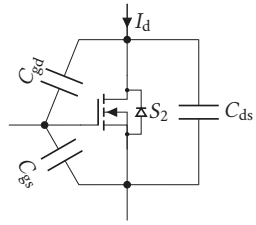


FIGURE 10.2. Power MOSFET device capacitances

as indicated in Figure 10.2:

$$C_{oss} = C_{ds} + \frac{C_{gs} \cdot C_{gd}}{C_{gs} + C_{gd}} \tag{10.1}$$

$$\implies C_{oss} \approx C_{ds} + C_{gd} \text{ as } C_{gs} >> C_{gd}. \tag{10.2}$$

This added capacitance leads to a high overshoot voltage during turn-off, especially at elevated di/dt values, as described in the following:

When the primary switch S_1 is switched on to initiate the subsequent magnetization phase, the secondary current (I_{sec}) declines. The power MOSFET in the rectifier position (S_2) is conducting I_{sec}. I_{sec} is seen as a negative drain current (I_d) by S_2. Either the conductive channel or the body diode of S_2 conducts this current, depending on the value of the gate-source voltage of S_2 (V_{gs}).

When the secondary current reaches zero, the drain-source voltage of S_2 (V_{ds}) is either zero (in case of channel conduction) or close to zero (in case of body diode conduction) because I_d, previously negative, could not establish a positive drain-source voltage V_{ds} across C_{oss} up to this point. As a result, the superposition of the reflected input voltage and the output voltage is present across the stray inductance L_{str} of the secondary transformer winding. This leads to the buildup of a negative I_{sec}, i.e. a positive I_d in S_2.

If V_{gs} is larger than the threshold voltage, this current is split between C_{oss} and the conductive channel of S_2. Hence, V_{gs} has a major influence on V_{ds}. With a high V_{gs}, the channel has a low resistance, conducting a large portion of the secondary current. However, this also increases I_d by counteracting the buildup of a demagnetizing voltage across the secondary transformer stray inductance L_{str}. With a low V_{gs}, the current rise is limited by the voltage building up across the power MOSFET in its output capacitance. However, this voltage reaches very high values quickly, as the device output capacitance is comparatively small. Seen from another perspective, the system forms a resonant circuit when I_{sec} crosses zero. This resonant circuit is subject to an excitation voltage formed by the reflected input voltage and the output voltage. V_{ds} can therefore

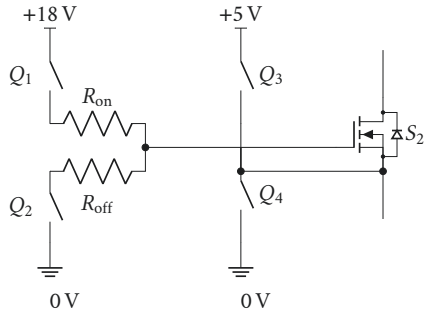


FIGURE 10.3. Three Level MLVSGD and Power MOSFET S_1

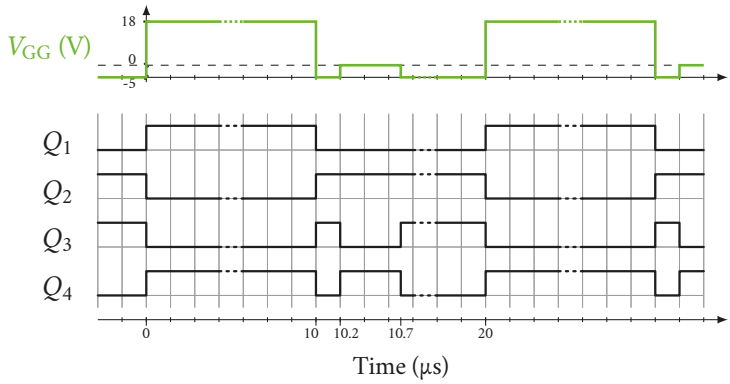


FIGURE 10.4. Idealized three-level VSGD Output Voltage with open Gate Terminal (V_{GG}) and According Digital Control Signals

theoretically reach values of up to $\sqrt{2}$ of this excitation voltage. By controlling the trajectory of V_{gs}, a resistive component is added to this resonant circuit, damping the overshoot voltage. To realize control over V_{gs}, this paper proposes using a MLVSGD.

The three voltage levels of this MLVSGD are 18 V, −5 V, and 0 V. An idealized schematic diagram of the MLVSGD is shown in Figure 10.3. While in on-state, S_2 carries a current in its conductive channel, V_{gs} equals $V_{GG,on} = 18$ V, the high gate driving voltage. While in off-state, S_2 does not form a conductive channel, and V_{gs} equals the low gate driving voltage $V_{GG,off} = -5$ V. In off-state, a negative I_d can still be conducted by the body diode of the power MOSFET.

At turn-off, i.e. the transition of V_{gs} from $V_{GG,on}$ to $V_{GG,off}$, V_{gs} follows the trajectory presented in Figure 10.4 between 10 µs and 10.7 µs. The exact timings shown in Figure 10.4 are only exemplary. In on-state, the gate driver switches Q_1 and Q_4 conduct. The turn-off is initiated by Q_1 and Q_4 turning off, and Q_2 and Q_3 turning on. This applies $V_{GG,off} = -5$ V to the gate of S_2 through the resistor R_{off}. After a configurable time interval of $t_{low} = 200$ ns, Q_3 turns off and Q_4 turns on, applying $V_{GG,int} = 0$ V to the gate of S_2 through R_{off}.

After another configurable time interval of $t_{int} = 500\,ns$, Q_4 turns off again, and Q_3 turns on, applying a voltage of $V_{GG,off} = -5\,V$ throughout the off-state of the device.

Applying this intermediate voltage level of $V_{GG,int} = 0\,V$ slows down the discharging of the power MOSFET input capacitance. By choosing suitable t_{low} and t_{int} values, the input capacitance discharge trajectory of S_2 can be actively controlled, which in turn adds a resistive component to the rectifier behavior. Thereby, the three-level MLVSGD can be used to damp the oscillations provoking the high V_{ds} overshoot voltage by adding a resistive component to the resonant circuit formed by the secondary transformer stray inductance and the output capacitance of S_2. As suggested earlier, choosing an advantageous timing is the key to minimize the overshoot voltage. If V_{gs} is too low during the zero crossing of I_{sec}, the introduced resistance is too large to have a noteworthy damping effect, and if V_{gs} is too high, I_{sec} will increase significantly, leading to a higher overshoot voltage in the later phase of the turn-off trajectory.

10.3 EXPERIMENTAL STUDY

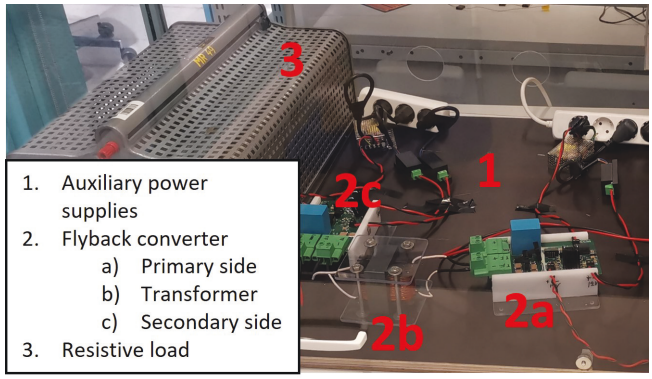


FIGURE 10.5. Photograph of the experimental test circuit

A laboratory prototype of a flyback converter with output synchronous rectification has been built in order to experimentally validate the performance of the proposed gate driver. The schematic diagram of the test setup is illustrated in Figure 10.1. Two SiC MOSFETs from Toshiba (TW048N65CS1F) $S_{1,2}$ were used in the setup, with the S_2 operating as a synchronous rectifier. Additionally, a snubber circuit has been connected in parallel to the primary winding of the transformer in order to mitigate the overvoltage across the primary-side switch S_1. This snubber consists of a resistor R_{sn}, a capacitor C_{sn} and a diode D_{sn}. A photograph of the test setup is illustrated in Figure 10.5.

TABLE 10.1. Parameters of the experimental setup and gate driver

Parameter / Component	Value
Input voltage, V_{in}	70 V
Output voltage, V_{o}	70 V
Primary switch, S_1	SiC MOSFET 650V, 40A, TW048N65CS1F (Toshiba)
Secondary switch, S_2	SiC MOSFET 650V, 40A, TW048N65CS1F (Toshiba)
Load, P	500 W
Switching frequency, f_{sw}	50 kHz
Input/Output capacitors, $C_{\text{in,o}}$	50 µF, B32776G4506K000 (EPCOS/TDK)
Snubber diode D_{sn}	DPG30I400HA (IXYS)
Snubber resistor R_{sn}	3.3 kΩ, SMF53K3JT (TE Connectivity)
Snubber capacitor C_{sn}	0.88 µF, CKC33C884KCGLC7805 (KEMET)
Transformer turns ratio, $N_1 : N_2$	11 : 11
Auxiliary switches in VSGD	Si MOSFETs, ZXMN3A01E6TA (Diodes Inc.)
Gate drivers for auxiliary switches	LM25101AMR/NOPB (Texas Instruments)

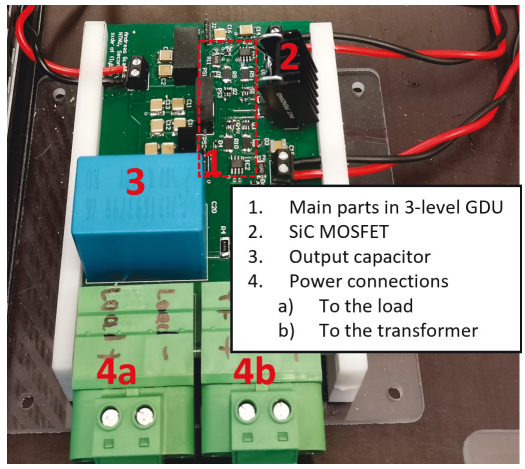


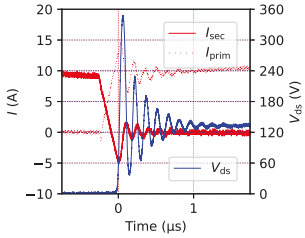
FIGURE 10.6. Photograph of the secondary side of the flyback converter with the three-level VSGD

TABLE 10.2. Maximum Voltage Across Rectifier ($V_{ds,max}$) and Minimum Secondary Current ($I_{sec,min}$)

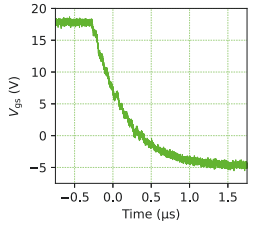
Gate Driver	$V_{ds,max}$	$I_{sec,min}$
VSGD A	348 V	−5.16 A
VSGD B	326 V	−7.80 A
VSGD C	300 V	−6.84 A

Three Voltage Source Gate Driver (VSGD) driving patterns to drive the synchronous rectifier S_2 have been considered and tested using the same experimental setup. All patterns were realized with the gate driver introduced in Section 10.2, but with differing control signal patterns which are generated by a Texas Instruments LAUNCHXL-F280049C evaluation board.

The first driving pattern, VSGD pattern A, is a Two Level VSGD pattern with a turn-on voltage of 18 V and a turn-off voltage of −5 V according to the manufacturer's datasheet. The second pattern, VSGD pattern B, is identical to VSGD pattern A, but with a turn-off voltage of 0 V. Finally, a three-level VSGD pattern was applied in the third case, VSGD pattern C. The gate voltage was set to 18 V during conduction operation similar to the two previous cases, while at turn-off, the gate voltage decreased initially to −5 V for a period of 200 ns, then to 0 V for approximately 500 ns and finally, back to −5 V for the rest of the turn-off time interval. This case is described in Section 10.2 and visualized in Figure 10.4. A photograph of the secondary side of the synchronous flyback converter along with the three-level gate driver is shown in Figure 10.6. The considered parameters of the experimental test circuit and the gate driver are summarized in Table Table 10.1.

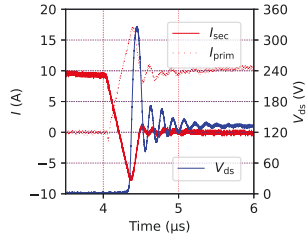


(A) Transformer Current on Secondary (I_{sec}) and Primary (I_{prim}) Side, and Rectifier Forward Voltage (V_{ds})

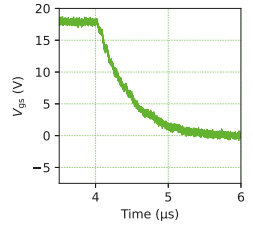


(B) Rectifier Gate-Source Voltage (V_{gs})

FIGURE 10.7. Experimental results for the synchronous flyback converter employing the VSGD pattern A.

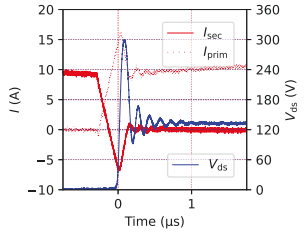


(A) Transformer Current on Secondary (I_{sec}) and Primary (I_{prim}) Side, and Rectifier Forward Voltage (V_{ds})

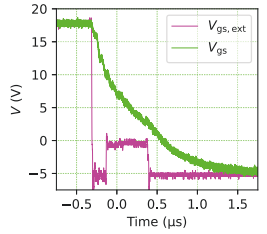


(B) Rectifier Gate-Source Voltage (V_{gs})

FIGURE 10.8. Experimental results for the synchronous flyback converter employing the VSGD pattern B.



(A) Transformer Current on Secondary (I_{sec}) and Primary (I_{prim}) Side, and Rectifier Forward Voltage (V_{ds})



(B) Rectifier Gate-Source Voltage (V_{gs}) and 3-level VSGD Output Voltage ($V_{gs,ext}$)

FIGURE 10.9. Experimental results for the synchronous flyback converter employing the VSGD pattern C.

The results of the synchronous flyback converter operation employing the three investigated VSGD patterns can be seen in Figures Figure 10.7, Figure 10.8 and Figure 10.9. Table Table 10.2 lists the maximum value of V_{ds} measured across the rectifier, as well as the minimum value of I_{sec}.

Figure 10.7 shows the primary current I_{prim}, the secondary current I_{sec}, as well as the gate-source voltage V_{gs} and the drain-source voltage V_{ds} when VSGD pattern A is used. It can be seen that the peak voltage across the SiC MOSFET operating in synchronous rectification mode (S_2) is 348 V.

With the use of VSGD pattern B, the peak drain-source voltage of S_2 is limited to 328 V as shown in Figure 10.8. The gate-source voltage is set at 0 V for turning-off S_2 in this case, which means that V_{gs} is considerably larger than the threshold voltage when the V_{ds} transition occurs. Therefore, the oscillation causing the V_{ds} overshoot is subject to stronger damping compared to VSGD pattern A.

Finally, in the case of VSGD pattern C, the V_{ds} overshoot decreases further to 302 V, a reduction of approximately 13 % compared to VSGD pattern A and 8 % compared to VSGD pattern B. The reason for this reduction is that utilizing VSGD pattern C, V_{gs} falls faster in the beginning of the transition compared to VSGD pattern B (for the time interval of 200 ns), leading to a lower gate-source voltage of the SiC MOSFET. Thus, the channel of the device is less open and hence, its ON-state resistance increases. As described earlier, the channel resistance of the power MOSFET damps the oscillations observed after turn-off. Depending on the duration of t_{low} and t_{int}, this ON-state resistance can be manipulated. In the case depicted in Figure 10.9, the power MOSFET channel resistance that results from using VSGD pattern C in the previously described configuration achieves a higher damping factor of the oscillations between the device output capacitance and the leakage inductance of the transformer and thus, a lower drain-source voltage overshoot than VSGD pattern A and VSGD pattern B.

The advantages mentioned above come at the cost of a higher driver and control signal complexity compared to VSGD pattern A and VSGD pattern B. In addition, VSGD pattern C introduces higher switching losses in comparison to VSGD pattern A.

10.4 Conclusion

This paper presents a three-level voltage source gate driver for minimizing the anticipated overvoltage during switching of SiC MOSFETs operating in the synchronous rectification mode. The performance of the proposed gate driver and driving pattern has been assessed during the turn-off process of the SiC

MOSFET employed on the secondary side of a synchronous flyback converter. The paper analyses in detail both how this voltage overshoot occurs and how the proposed gate driver actively reduces it. From the experimental validation, it has been shown that the proposed gate driver reduces the overvoltage by approximately 13 % compared to a conventional gate driver with two voltage levels.

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Chapter 11

Wireless Control of Active Gate Drivers for Silicon Carbide power MOSFETs

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Submitted to: *IEEE Open Journal of the Industry Electronics Society*

Contributions

- Hierarchical model of information transfer in Power Electronics Systems (PES)
- Requirements definition regarding Wireless Communication Technologies (WCTs)
- Suitability assessment of WCTs for Information Transfer Routes (ITRs) in PES
- Application of this assessment to information transfer from converter control to AGD control by means of Bluetooth Low Energy (BLE)

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Abstract

Active Gate Drivers (AGDs) enhance controllability and switching device monitoring, especially for fast switching Silicon Carbide (SiC) power Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFETs). To support information flow between gate driver, converter, and grid control units, high-performance digital infrastructure is required. This paper provides a practical approach to assess the benefits of using Wireless Communication Technologies (WCTs) in Power Electronics Systems (PES). First, Information Transmission Routes (ITRs) are identified and located within a PES employing AGDs. Second, a taxonomy for the classification of these ITRs is proposed, describing application scenarios and requirements for every ITR class. After laying out general advantages of WCTs over wired alternatives, seven specific WCTs are individually characterized. Subsequently, the benefits of using WCTs are evaluated for each ITR class, resulting in a specific recommendation for or against the use of WCTs, and at least one appropriate WCT for each ITR. In addition, experimental results demonstrate that wireless control of AGDs for SiC power MOSFETs is feasible using the Universal Asynchronous Receiver Transmitter interface over Bluetooth Low Energy (BLE). It has been shown that the exemplary Multilevel Voltage Source Gate Driver (MLVSGD) can be effectively controlled with an information transmission delay of less than 40 ms.

11.1 Introduction

Wide-bandgap switching devices have gained popularity in the past years. Properly harnessed, their technological advantages allow high-efficiency, high-power-density, and high-temperature converter designs, even under varying load conditions [1]. To exploit the low switching loss potential of Silicon Carbide (SiC) MOSFETs, a powerful gate driver is required.

Active Gate Drivers (AGDs) can manipulate the gate charging process [2–10]. As opposed to conventional gate drivers, AGDs are online-reconfigurable circuits. AGDs have successfully activated the technological advantages of SiC MOSFETs by providing effective, yet fine-grain control of switching transitions [2–10]. In addition, many AGDs incorporate sensors that enable key switching device parameter monitoring. AGDs support fast switching and low switching losses, but also alleviate negative side effects of fast switching, mainly Electromagnetic Interference (EMI) [5; 6; 8; 11; 12] and elevated device stress due to overshoot voltages and currents compared to conventional gate drivers at the same operating points [6; 8; 11–13]. Furthermore, AGDs have been used

to slow down voltage slopes [6–8] to lower the associated risks for the health of coil windings [14] in electrical machines or transformers. AGD topologies vary in the physical principles, i.e. circuitry and operating principles, employed to achieve switching transient control. As a result, the operating complexity of the interface between the gate driver and the converter control varies among different AGD types as well. The majority of AGDs require timed multichannel digital signals [5; 7; 13; 15; 16], and in addition to that, some need another digital or analog configuration signal [4; 6; 17].

Recent advances in both high-bandwidth wireless communication and data processing technology reveal great potential for converter and grid control. Today's localized, reaction-driven and often maximum-power oriented approach will evolve into an intelligent, both grid- and demand-optimized solution that features self-monitoring in the future. Hence, new approaches to classify information transmission are required to make an informed decision about the usage of Wireless Communcation Technologies (WCTs) and system component autonomy. Numerous digital AGD concepts include various sensors [15; 16; 18; 19]. Gate drivers will use these sensors to collect operational data and monitor the health of switching devices. Thus, AGDs will play a key role in the transformation of converters to intelligent, partly autonomous units, supporting energy availability and security [2].

Several wireless gate drivers have been presented recently [20–24]. These gate drivers predominantly rely on a binary transmission mode to control the state of a single switch per wireless signal [20–22; 24]. They mainly differ in the Radio Frequency (RF) located either in the High Frequency (HF) [21; 22; 24], the Ultra High Frequency (UHF) [25; 26], or the Extremely High Frequency (EHF) [20] International Telecommunication Union (ITU) band respectively. In case of receiver or transmitter failure, these binary transmission modes will not ensure system stability, but rely on additional safety measures to avoid shoot-through conditions. Furthermore, as SiC MOSFETs switch very fast, disturbances and EMI can be expected in the HF band. The UHF and EHF bands are located significantly above the expected EMI frequencies (below approximately 250 MHz)[27; 28] and are therefore not susceptible to disturbances from the converter. However, the hardware needed to broadcast and receive EHF signals requires careful RF design, and restricts the placement of components in a converter, especially, if directional antennas are required. A wireless gate driver control using EHF frequency and digital signals [23] improves both wireless communication efficiency and reliability by using digital information encoding. Furthermore, it enables simple error correction. With this gate driver, however, each switching action requires one message. As a consequence, system stability cannot be guaranteed in case of receiver or transmitter failure. In addition, the encoding and decoding of the wireless signal

requires bulky and costly hardware using Field Programmable Gate Arrays (FPGAs) or Application Specific Integrated Circuits (ASICs).

To summarize, the most important advantages of wireless AGD control are:

- The benefits of using AGDs are enabled while at the same time, common mode interference is reduced to a minimum because conductive and/or capacitive paths to the converter control are effectively eliminated.
- As will be shown later, the integration of certain WCTs requires a higher degree of autonomy in converter subsystems. This can improve the system reliability and be used to implement advanced protection features.
- Flexibility is added to the system, for example regarding the placement of components.
- Converters are made more modular using WCTs, as the different functional units are both electrically and mechanically separated.

The contribution of this work is to facilitate the decision process of WCT adaptation in a converter design by addressing the following objectives:

1. Determine where in a converter system the above-mentioned advantages of wireless information transfer can be utilized most effectively,
2. Identify suitable WCTs for these locations, and
3. Demonstrate wireless AGD control in an experimental setup.

To achieve these objectives, a taxonomy for ITR classification is derived, and suitable WCTs for every ITR class are identified. Moreover, a recommendation for or against the usage of WCT in each of the ITR classes will be given, and related consequences for system safety will be laid out. With the help of the proposed methodology, benefits and challenges of using WCTs can be weighed against each other on a conceptual level, leading to a multifaceted conclusion about whether and where WCTs constitute a valuable part in a converter design. In addition, experimental results demonstrate the successful wireless control of an MLVSGD for SiC power MOSFETs using BLE as WCT.

The rest of the paper is structured as follows: Section 11.2 examines the flow of information within a PES. The information structure of a PES employing AGDs is presented and ITRs are identified. Subsequently, a taxonomy for classifying these ITRs is proposed. Section 11.3 first elaborates on the advantages of WCTs over alternative wired technologies. Seven exemplary WCTs are introduced with their specific characteristics. Then, the process of assessing the suitability of WCTs for realizing an ITR is introduced and demonstrated

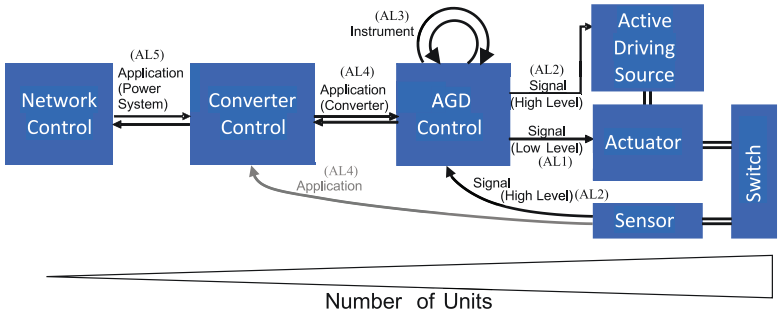


FIGURE 11.1. PES Layout employing AGDs

for all previously defined ITRs. Section 11.3 closes with an analysis of the safety implications of using wireless control of AGDs. Experimental results demonstrate the successful application of UART over BLE for controlling a MLVSGD for SiC power MOSFETs are presented in Section 11.4. Section 11.5 concludes the paper.

11.2 INFORMATION TRANSMISSION IN PES

11.2.1 PES Information Structure

To facilitate evaluating the use of WCTs in a PES employing AGDs, the ITRs within this system are identified and classified in the following. Figure 11.1 shows the structure of a PES incorporating AGDs. It consists of:

- System components, conceptual units, symbolized by named rectangles,
- Physical, i.e. electrically conductive, links shown as thick lines, and
- Directed ITRs as arrows.

The Network Control represents the grid operator control instances, which can be manifold and, depending on the network structure, more or less complex. The Converter Control symbolizes the local control units, ensuring compliance with the Network Control directive. At the same time, the Converter Control governs the converter state. Apart from (real and reactive) power output, the Converter Control also incorporates temperature control. Moreover, the Converter Control can potentially feature health monitoring and predictive maintenance. The AGD Control translates commands given by the Converter Control into command and PWM switching signals. These signals are directed towards the Actuator, i.e. the gate driver switches, and the Active Driving

TABLE 11.1. Information Transmission Route (ITR) Classification and WCT Recommendations

Abstraction Level (AL)	Exemplary Information Content	Data Rate Requirement	Latency Requirement
Application (Power System) (AL5)	Power Flow control (P/Q), Digital Filtering	Low/Mediocre	Low ($< 10\,\mathrm{s}$)
Application (Converter) (AL4)	EMI control, Active Temperature Control	Low/Mediocre	Low ($< 100\,\mathrm{ms}$)
Instrument (AL3)	$\frac{dv}{dt}, \frac{di}{dt}, \frac{d\theta}{dt}$	High	Mediocre ($< 1\,\mathrm{ms}$)
Signal (High Level) (AL2)	AGD Source Configuration (Voltage/ Current/Resistance)	Very High / High	Very High ($<< 100\,\mu\mathrm{s}$)
Signal (Low Level) (AL1)	Gate Driver Timing, Gate Signal	Extremely High	Extremely High ($<< 100\,\mathrm{ns}$)

Source, i.e. the part of the gate driver that makes it online-configurable. In a MLVSGD for example, the Active Driving Source is the configurable voltage source supplying the gate driver voltage levels. The sensor block symbolizes one or multiple sensors of any possible type. To name examples, this could be a current sensor, a voltage or current slope (dv/dt or di/dt) sensor, a temperature sensor, etc. The sensor block is an optional part of the AGD, and it will in most cases communicate back to the AGD Control. In safety critical sensor applications, or for control purposes implemented on a higher level like, for example, active temperature control, the communication might also be established with the Converter Control unit directly. A tree structure with a single Network Control at the root and multiple branches for each new instance would describe an actual PES better, as it does not consist of only one of the depicted structures. To avoid redundancy, this is represented by the triangle on the bottom of Figure 11.1. The width of this triangle indicates the number of involved components and information links.

11.2.2 Information Transmission Route (ITR) Taxonomy

Each ITR within this PES structure is assigned a level of abstraction describing the physical distance of that ITR to the switching devices it has an impact on. With increasing level of abstraction, an ITR is located at a greater distance from the switching devices it impacts, and it has an impact on more switching devices. In this work, an ITR is not distinguished from the information or signal passed through this ITR, and these are therefore classified identically, and as one unit. In the case of the PES structure presented in Subsection 11.2.1, the proposed taxonomy yields six classes, i.e. abstraction levels.

Abstraction Level 1 (AL1) between the AGD Control and the Actuator: This ITR is assigned the lowest abstraction level, named "Signal (Low Level)" as it has an immediate effect on the gate-source voltage of a single power switch

or potentially few parallel connected power switches. Therefore, the ITR has a distance of at most few centimeters to the switching device it controls. This results in a low level of abstraction, the lowest in the context of this work, AL1. The signals of this ITR must have a very high resolution in time. Depending on the AGD architecture, only very short delays are acceptable, down to the range of 500 ps and even below. Some AGDs require multiple channels of this signal type. Although only binary information is required on this route and the average information entropy is low as the information is highly repetitive, the high time resolution, possibly required on multiple channels simultaneously, leads to an extremely high data rate.

Abstraction Level 2 (AL2) between AGD Control and Active Driving Source: All AGDs are realized with a configurable unit that is separate from the gate driver switches (Actuator), and, in the context of this work, is referred to as Active Driving Source. In current and multilevel voltage source AGDs, this is the configurable power supply, and in the case of variable external resistor AGDs, this is the resistor configuration, for example. The distance to the switch is increased compared to AL1, as the Active Driving Source is located "behind" the Actuator seen from the switching device(s). The required data rate depends on the controllability requirement. A fast response is desired because control loops utilizing AGD functionality could be potentially limited by the latency introduced in this path. However, the Active Driving Source itself has a minimum reaction time tied to its digital (digital isolators, digital potentiometers, microcontrollers, etc) and analog components that determine its dynamics, for instance the output response of a variable voltage source in the case of an MLVSGD. In addition, as opposed to the Actuator signals, it is not necessary to transmit at every switching instance. The data rate is therefore significantly lower than in the case of AL1, but still significantly higher than in higher abstraction levels. Reaction times range below 100 µs.

Abstraction Level 3 (AL3) within an AGD Control: With the PES layout in Figure 11.1, the AGD Control block can have multiple responsibilities. The Converter Control will provide abstract information about, for example, the allowed voltage overshoot and maximum slope in the context of an EMI control. The AGD control unit now has four responsibilities, i.e.:

- Given the command received from the Converter Control and with the knowledge of the current AGD state, check for deviance from the Converter Control command.

- Then, determine the necessary sequence of switching condition commands that bring the state of the switch into compliance with the Converter Control command immediately or over a period of time. These switching condition commands are, for example, the voltage slope dur-

ing switching $\frac{dv}{dt}$, the current slope during switching $\frac{di}{dt}$, the desired temperature gradient $\frac{d\theta}{dt}$, etc.

- With the knowledge of how switching device and AGD together behave, translate the sequence of switching condition commands into a sequence of AGD configurations.

- Send this sequence of AGD configurations to the Active Driving Source and Actuator via ITRs on AL2 and AL1.

The computational power of one Microcontroller Unit (MCU) might not be sufficient to realize all of these tasks. Therefore, task 1 and 2 might be implemented in two separate MCUs, which communicate over an ITR on AL3. The amount of information exchanged on this ITR is again significantly lower than on AL2, as only single numerical values need to be transferred, but because a high degree of repetition is required, the data rate qualifies as "High". To achieve fast control, the latency introduced by this ITR should not surpass 1 ms. The two ends of this ITR are located within the AGD control unit. As has been mentioned earlier, this ITR can therefore be regarded internal to the AGD Control block. In the AGD example presented in the experimental part of this work, Section 11.4, this ITR does not exist separately because the associated information is handled within the MCU.

Abstraction Level 4 (AL4) between Converter Control and AGD Control: This ITR transmits information that is specific to the application of the AGD in question. In the context of EMI control for example, boundary values of the voltage and current overshoot and slope could be transmitted, or a desired junction temperature or temperature range in the case of Active Temperature Control. Thermal systems exhibit slow dynamics in the range of many seconds. Therefore, for this application, a reaction time below 100 ms is regarded sufficient. The very fast switching speeds observed with SiC pose challenges in the health of inductor and especially electrical machine windings [14]. By limiting the maximum voltage slope steepness through EMI control, this issue can be softened and the lifetime of windings prolonged, indicated by the comparing winding lifetime tests with 5-level and 2-level inverters [29]. With a maximum failure rate of 2 %, a twisted-pair lifetime of approximately 3000 s has been observed in a 2-level converter test with voltage rise times of 60 ns [29]. When detecting a high dv/dt condition that might deteriorate the lifetime of the winding insulation material, taking action by reconfiguring the AGD within 100 ms is therefore regarded sufficiently fast to achieve major lifetime improvements.

Abstraction Level 5 (AL5) between Network Control to Converter Control: This signal can, for example, contain output power commands, (active and

reactive) output power slope commands, etc. It affects all switches in a converter or even multiple converters, and can be located at a distance of multiple meters or even kilometers from the switches it finally affects. It is therefore assigned the highest abstraction level in the context of this work, AL5. Delay requirements for this information type are far more relaxed, as power system reserves buffer short-term misalignment. Moreover, electric energy market planning may allow converter pre-configuration in the future, so that the continuous, time-critical information flow can be optimized. Altogether, this results in only mediocre or even low average rate of data transmission.

11.3 WCTs for PES

11.3.1 Advantages of WCTs over Wired Alternatives

WCTs exhibit major advantages over wired alternatives, i.e., digital signal isolators, and fiber-optic cables. SiC MOSFETs accelerate the trend towards faster switching speeds to reduce associated losses and filter size. This leads to steadily increasing requirements in regard to high voltage isolation, $\frac{dv}{dt}$ immunity, and common mode rejection. While this is a major issue for the use of digital isolators, these requirements are easily fulfilled by WCTs and fiber-optic cables. In addition, both fiber-optic cables and WCTs operating in the UHF band or at even higher frequencies, are not equally affected by EMI as wired solutions because less conductive cables are required. EMI frequencies are usually limited to 250 MHz [27; 28], and WCTs, e.g., BLE or Wi-Fi, commonly operate at frequencies well above 2 GHz.

In comparison to both digital isolators and fiber-optic cables, WCTs significantly enhance the modularity of PES. This modularity facilitates the mechanical placement of subsystems, allowing for optimal filter locations and thereby improved electrical behavior. Apart from that, the increased modularity simplifies maintenance procedures as subsystems are more easily connected and disconnected, and made more accessible. In addition, WCT-enhanced converters can be scaled more easily, for example, by adding converter building blocks to increase the converter power rating. Finally, WCTs on high abstraction level ITRs such as BLE or Wi-Fi inherently enable two-way communication. Bidirectional digital isolators are widely available. Enabling two-way information transfer with fiber optic cables requires twice as many cables and a significant amount of available power on the secondary side, which would be the AGD or AGD control unit, for example. However, AGDs are limited in the power available for this purpose. Increasing the AGD power supply would lead to increasing the coupling capacitance and thereby degrade the common mode

TABLE 11.2. Wireless Communication Technologies (WCTs) by Example

Wireless Technology	Data Rate Limit	Latency (excl. Propagation Delay)	Spatial Range	Advantages	Disadvantages
SHF/EHF CW	Spectral Bandwidth and Sampling Frequency Dependent, >> 2 Gbps	≤ 100 ns	Implementation Specific	Noise Immunity	Efficiency, Hardware Cost and Complexity (RF) No Error Correction
SHF/EHF PSK	Spectral Bandwidth and Sampling Frequency Dependent, ≤ 1 Gbps	≤ 1 μs	Implementation Specific	Noise Immunity	Hardware Cost and Complexity (De-/Modulation + RF) No Error Correction
BLE	Hardware and Service Dependent, ≤ 1 Gbps	≤ 100 ms	≤ 10 m	Hardware Cost, Availability	Latency, Data Rate
WiFi	Hardware Dependent, ≈ 1 Gbps	≤ 10 ms	≤ 1000 m	Hardware Cost, Availability, Security	Latency
WWAN (e.g. 4G)	Location Dependent, ≤ 100 Mbps	Location Dependent, ≥ 100 ms		Hardware Cost, Network Integration, Availability, Security	Latency, Operating Cost, Dependence on Telecom. OPs

interference rejection. These factors discourage enabling bidirectional data transfer with fiber optic cables, which is a burden for the implementation of enhanced monitoring features that AGDs could be used for.

11.3.2 Characteristics of Exemplary WCTs

The three main characteristics of WCTs are data rate, latency, and range. Data rate describes the amount of information that can be transmitted in a fixed time interval, latency is the delay caused by preparation, transmission, reception, and interpretation of information, and range refers to the distance over which information transmission is reliable at the specified data rate and latency. Table 11.2 contains these characteristics for seven exemplary WCTs. Moreover, the greatest advantages and disadvantages of each WCT are mentioned. These exemplary WCTs were chosen because they are either commonly available (Wi-Fi, BLE, 4G), have been demonstrated in literature (EHF Continuous Wave (CW)), or present an interesting alternative to what has been studied in literature (Super High Frequency (SHF)/EHF Phase-Shift Keying (PSK), SHF CW).

These technologies can be divided into two groups: Low-level WCTs (SHF/EHF CW/PSK) that transmit information in the form of single bits, and higher level WCTs that provide abstracted transmitted information (Wi-Fi, BLE, 4G). Low-level WCTs can be seen as a direct substitute for wired signal lines and the associated line drivers because both transmit binary signals. Just as wired signal lines, low-level WCTs do not have an inherent ability of correcting errors. Higher level WCTs are a substitute for wired signal lines, line drivers, and the integrated circuits implementing a communication protocol (UART,

TABLE 11.3. ITR Abstraction Levels and WCT Usage Recommendations

Abstraction Level (AL)	Suitable WCT	Wired Alternative	Recommendation
Application (Power System) (AL5)	Wireless Wide Area Network (WWAN), e.g. 4G	Wired Internet Connection (fiber optic, coaxial, etc.)	WCT
Application (Converter) (AL4)	Wi-Fi, Bluetooth LE	Bi-directional Digital Isolators	WCT
Instrument (AL3)	SHF/EHF PSK	Bi-directional Digital Isolators	Wired Alternative
Signal (High Level) (AL2)	SHF/EHF PSK	Uni-directional Digital Isolators	Wired Alternative
Signal (Low Level) (AL1)	SHF/EHF PSK, SHF/EHF CW	Uni-directional Digital Isolators	Wired Alternative

FSI, I2C, ...). Instead of information in the form of bits, these WCTs deliver aggregated information packets, encapsulating and abstracting the wireless hardware. Higher level WCTs typically implement error correction. However, this comes at the cost of processing time and demand for control information, that result in a significantly larger latency and reduced maximum data rate.

11.3.3 WCT Suitability Assessment and Decision Procedure

The analysis shows that wireless solutions exist to support all presented ITR classes. To help to decide on the use of WCTs for a given ITR, three aspects must be considered:

1. The WCT must fit the application requirements under normal (nominal) operating conditions and the advantages should outweigh the disadvantages.

2. In a worst-case scenario, the failure of the WCT in question must have deterministic consequences that are acceptable from the perspective of system safety.

3. The implementation of a WCT must be worthwhile considering wired alternatives in regard to cost, complexity, operation safety and reliability.

These questions have to be answered individually for every abstraction level as the WCTs take different roles, and different WCTs come into question for realizing these roles. This decision process for all abstraction levels is described hereafter.

Abstraction Level 1 (AL1): As already mentioned, wireless AGDs have been proposed for controlling PWM switching signals [20–22; 24]. However, potentially unstable converter states in case of transmitter or receiver failure raise safety concerns when using CW that does not support inherent error correction, or digital modes that require one signal per switching event. PSK has a

slight advantage over CW in this regard, as it requires a constant carrier signal. Losing RF contact or transmitter failure could be easily detected by a missing or faulty carrier signal. However, digital isolators and wired signal lines do not have the same disadvantages, cost significantly less, and result in a much reduced design complexity. The major challenge when using digital isolators and wired signal lines for this ITR is common mode current injection caused by steep voltage slopes. This type of disturbance is caused by capacitive coupling of jumping potentials to the converter ground through the gate driver power supplies and the digital isolators that are referenced to a jumping potential. For effectively suppressing common mode current injection, capacitive coupling needs to be minimized. This is achieved by circuit minimization reducing the cross-sectional area of the parasitic coupling capacitance, and widening the galvanic barrier.

A power supply is required irrespective of using wired signal connections or WCTs, so this path cannot be eliminated. While using WCTs for these ITRs clearly introduces a galvanic barrier, it counteracts circuit minimization as it requires complex reception and processing hardware that is potentially vulnerable to common mode currents. Small circuits realizing the ITRs with wired signal lines, however, enable circuit minimization and by shifting the responsibility of galvanic isolation to an upper abstraction level ITR, common mode current injection can still be effectively reduced. Hence, the usage of WCTs for the AL1 ITR is not recommended.

Abstraction Level 2 (AL2): Concluding from the preceding explanation, the use of WCTs is not recommended for ITRs on AL1. When implementing a wired connection between AGD Control and Actuator, the connection to the Active Driving Source should be implemented as a wired connection too. Apart from that, the considerations for AL1 ITRs are valid for AL2 ITRs as well. Since the requirements in regard to data rate and latency are lower, less complex WCTs could be used. However, none of the previously characterized WCTs fits this purpose, except for those that can support AL1 ITRs but were ruled out because of the disadvantages listed above. Therefore, the use of WCTs for ITRs on AL2 is not recommended.

Abstraction Level 3 (AL3): With the yet reduced requirements of ITRs on AL3, more WCTs, that lie outside the scope of this work, come into question for the realization of information transfer. As mentioned before, AL3 ITRs are located within the AGD Control block. Using WCTs adds unnecessary cost and complexity where either the use of a more capable MCU as AGD Control unit or a wired connection accelerates control, reduces system complexity, and increases reliability. Therefore, it is recommended not to use WCTs as ITR implementation on AL3.

Abstraction Level 4 (AL4): The further reduced latency requirement to

100 ms for ITRs on AL4 makes BLE and Wi-Fi viable WCT candidates, that are widespread, well documented, and cheaply available. Both BLE and WiFi support the required data rate at the range required for the communication within a converter.

Adding WCTs at AL4 has positive effects aside from improving galvanic isolation. AGD control units are implemented for half-bridge or full-bridge circuits as fundamental converter subsystems. When realizing AL4 ITRs with WCTs, these fundamental subsystems are made electrically and mechanically separable from each other. This enhances modularity, adaptability, and flexibility by increasing subsystem autonomy, without introducing a higher cost and more complexity as it would be the case on lower abstraction levels. The main challenges for wireless technology integration in this communication path are the added hardware cost and ensuring safe, secure and reliable communication in the presence of fast switching slopes. Apart from that, synchronization of series- and parallel-connected switches will become a challenge depending on the converter architecture.

Overall, the use of WCTs for AL4 ITRs is recommended. An example for AGD control using BLE will be demonstrated experimentally in Section 11.4.

Abstraction Level 5 (AL5): As mentioned earlier, today's power system does not yet have the structure laid out in Figure 11.1, so there is no wired infrastructure present. For economic reasons, the installation of a direct wired connection over several kilometers of distance and to multiple reception points is not realistic, while connecting to a Wireless Wide Area Network (WWAN) either directly or via an internet connection is simple and associated with a significantly lower investment cost. Considering that viable options fulfilling the requirements exist without detrimental disadvantages, using WCTs for this ITR is recommended. All recommendations are summarized in Table 11.3.

Especially when transferring information on a high abstraction level, multiple WCTs might be able to realize a specific ITR from the perspective of data rate, latency, and range. The system designer can base their choice between them on multiple factors.

- Operability. Switching devices emit electromagnetic radiation. Choosing between viable solutions in regard to data transmission must include a consideration of possible interference. For that, the datasheet of WCT hardware includes Signal-to-Noise Ratio (SNR) requirements. With a simple Software Defined Radio, the noise within the WCT RF frequency range present at the AGD control unit can be estimated. Furthermore, the signal level can be estimated by the RF transmitter power and the line-of-sight distance to the AGD control unit. These two estimates can be used for assessing the operability of a WCT.

- Structural Integrity. Depending on the desired hierarchy of transmitters and receivers (e.g. mesh vs radial networks), certain WCTs are more desirable than others (e.g. BLE for mesh vs Wi-Fi for radial networks).
- Development Time. Another difference between the WCTs is the existence of applications. To name an example, for BLE, both hardware and software already exist that can encapsulate the wireless information transfer and interface it to a control MCU with little additional effort. The experimental part of this work presented in Section 11.4 demonstrates that with suitable hardware and a compatible software implementation, adding a wireless interface is simple and convenient.
- Hardware Cost. Hardware prices vary greatly by manufacturer and change quickly and continuously, thus, no numbers are given in this work. However, numerous MCUs have integrated Wi-Fi and BLE modules (such as the ESP32). Such integrated solutions are usually cheap and easily integrated with the AGD control MCU. Choosing between the different WCTs that are available simultaneously must then be decided on by other factors as laid out before.

The choice between different WCTs is then made according to all of these factors.

11.3.4 Safety Implications of Using Wireless AGD Control

As mentioned above, realizing wireless AGD control on AL4 requires carefully considering the safety, security, and reliability of the wireless connection. Abstract information is transmitted through this ITR, and not PWM switching signals. Applications that can be supported by this information include efficiency optimization, EMI management, and Active Thermal Control. Any possible interruption in this ITR is therefore not detrimental for the immediate stability of the converter, as switching signals continue to be generated (or safely shut down) by the AGD control unit.

Using an independent Microcontroller Unit (MCU) as AGD control unit, as proposed in this work, effectively increases the gate driver autonomy. This added autonomy can enhance system safety, since the free computational power can be used to perform system monitoring tasks, and integrate safety features. This includes classic protection features like desaturation detection, but also advanced monitoring and protection features like EMI or parameter drift detection are feasible. The choice of the MCU as AGD control unit is especially important in this regard. It is recommended to use MCUs with functional safety certificates that are available from the major MCU manufacturers, and the

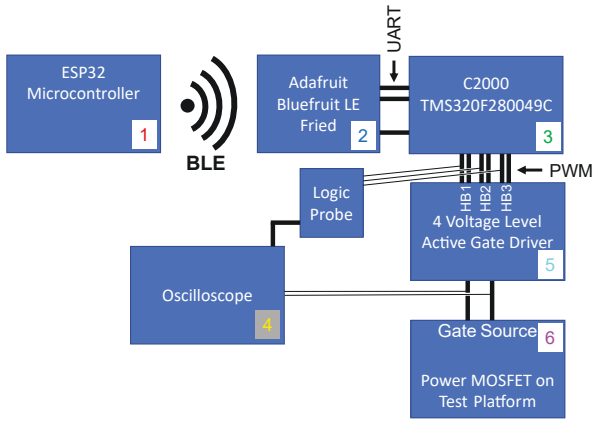


FIGURE 11.2. Schematic Diagram of the Experimental Test Setup

recommendations of the IEC 61508 standard have to be followed for adequate functional safety of the PES.

In regard to cybersecurity, BLE has been shown to have exploitable pairing procedures. A way to tackle this problem is the usage of encrypted information exchange instead of human-readable messages. By using suitable encryption technology, the injection of false information into the AGD control MCU becomes less feasible. Since the information routes are assumed to be bidirectional, a warning about possible interception attempts can further enhance awareness of this issue.

11.4 WIRELESS AGD CONTROL VALIDATION EXPERIMENTS

11.4.1 Test Setup

To demonstrate the usage of UART over BLE for AGD control, an experimental test setup was assembled. A schematic diagram of this test setup is shown in Figure Figure 11.2 and a photo is shown in Figure 11.3. The test setup consists of

- an ESP32 MCU (1) acting as a BLE central device,
- a BLE-UART bridge (2) [30] acting as a BLE peripheral device,
- a TMS320F280049C MCU (3) [31], the control unit of a
- four level MLVSGD (5) [4],

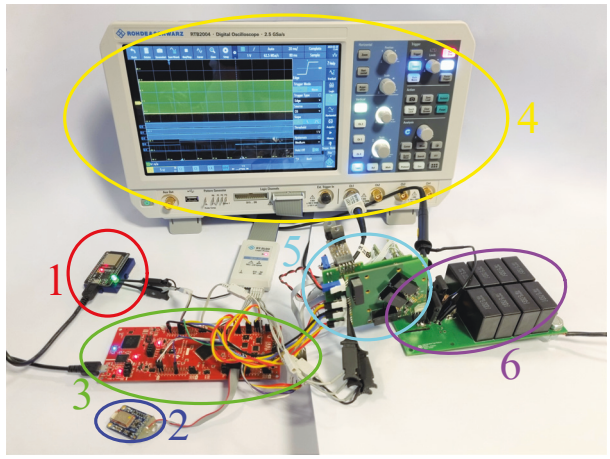


FIGURE 11.3. Wireless AGD control demonstration test setup.
1: ESP32 BLE central, 2: Adafruit BLE Friend BLE peripheral, 3: F28004x LaunchPad, 4: MSO, 5: Four Level MLVSGD, 6: Low-Inductive Test Platform

- a Mixed-Signal Oscilloscope (MSO) (4) to capture all control signals, as well as the gate-source voltage, and
- a low-inductive test platform for dynamic SiC MOSFET characterization (6) [32].

The schematic circuit diagram of the AGD controlled by the TMS320F280049C MCU is shown in Figure 11.4a. Figure 11.4b depicts the idealized gate driver output voltage V_{GG} and half-bridge circuit control signals required to achieve this output voltage. The AGD applies a configurable Intermediate Driving Voltage Level (IDVL) to the gate at turn-on ($V_{int,on}$) and another configurable IDVL at turn-off ($V_{int,off}$). The IDVLs are each provided by an adjustable linear regulator equipped with a digital potentiometer that is controlled by the TMS320F280049C MCU using the Serial Peripheral Interface (SPI). The high driving voltage $V_{GG,on}$ is configurable as well. The low driving voltage $V_{GG,off}$ is fixed at −5 V. Besides controlling these voltage levels, the TMS320F280049C MCU generates a timed pulse pattern consisting of three Pulse Width Modulation (PWM) signal channels, one for each half-bridge circuit of the gate driver, denoted as HB1, HB2, and HB3 in Figure 11.4a. The delay between the PWM signals of HB1 and HB2 determines the IDVL duration at turn-on ($t_{int,on}$), and the delay between the PWM signals of HB3 and HB2 determines the IDVL duration at turn-off ($t_{int,off}$) as can be seen in Figure 11.4b. The TMS320F280049C MCU supports serial communication over UART, and the self-programmed AGD control software is equipped with a Standard Commands for Programmable Instruments (SCPI) command interpreter accepting

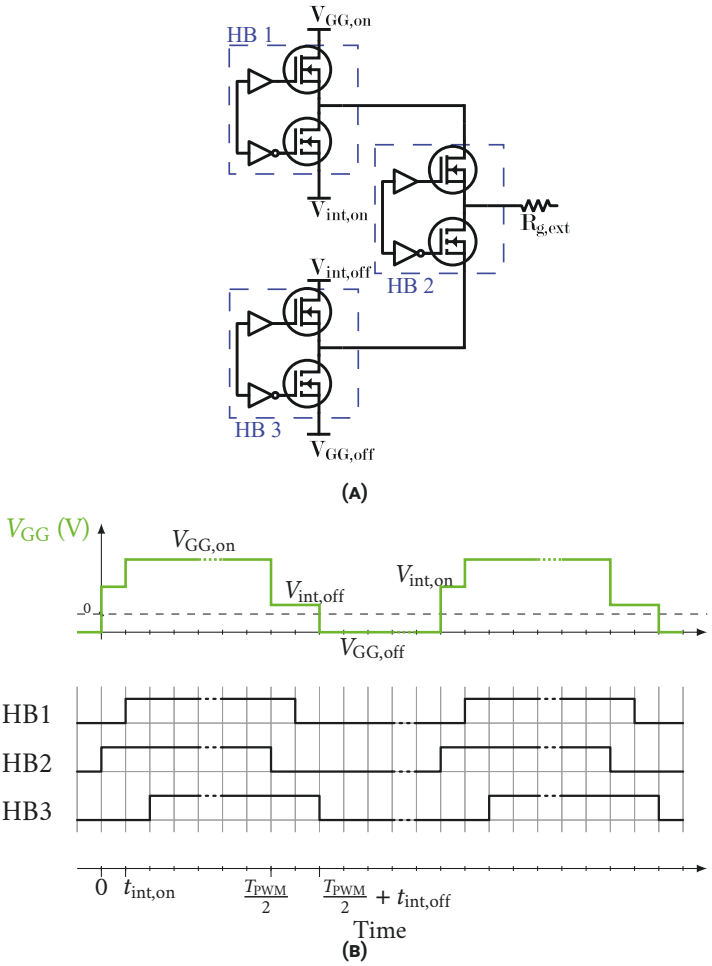


FIGURE 11.4. Four Level MLVSGD [4]:
(A) Schematic Diagram,
(B) Idealized Gate Driver Output Voltage V_{GG} and corresponding Control Signals for the half-bridge circuits HB1, HB2, and HB3 of the AGD

TABLE 11.4. Initial Gate Driver Parameters

Parameter	Value
$V_{GG,on}$	15 V
$V_{int,on}$	8.2 V
$t_{int,on}$	20 ns
$V_{int,off}$	0 V
$t_{int,off}$	20 ns
f_{PWM}	25 kHz

inputs from the UART interface. Sending correctly formatted commands over this serial interface therefore, the parameters mentioned above can be set manually or automatically using suitable software. Connecting the BLE UART bridge to the respective terminals of the TMS320F280049C MCU makes the UART interface available over BLE and thereby enables wireless AGD control.

The specific AGD was chosen for practical reasons, as it was studied in earlier work [4]. However, the only requirement that has to be fulfilled by an AGD so that the proposed wireless control is applicable to it, is that it implements control over a UART interface that can be connected to the BLE UART bridge. With this addition, other AGDs like active current source, variable resistor, and other multilevel voltage gate drivers [2; 3; 5–7; 7–9; 15–18; 20] could be used with the proposed wireless AGD control.

11.4.2 Experiment Procedure

The following experiment was repeatedly executed to determine the properties of the delay caused by signal transmission by means of UART over BLE. The TMS320F280049C MCU is initialized as the AGD control unit. It sends out three PWM signals to the AGD continuously at a PWM frequency of $f_{PWM} = 25$ kHz, and one of its SPI ports is connected to the supply section of the AGD. The initial gate driving parameters are listed in Table 11.4. The ESP32 MCU first pulls up an output, hereafter referred to as "Initiate", that is connected to a green LED which then lights up. Then, the ESP32 MCU immediately proceeds to send out a human-readable SCPI message, ":TEST:TDON 300", to the BLE-UART bridge, commanding to set $t_{int,on}$ to 300 ns. The message reaches the TMS320F280049C MCU through the gray ribbon cable between the markings 2 and 3 in Figure 11.3. The TMS320F280049C MCU reacts by changing its PWM output signals according to the received command. Immediately after that, the TMS320F280049C MCU pulls up an output, hereafter referred to as "Acknowledge". The delay between the rising edges of the "Initiate" and "Acknowledge" signals is the information transfer delay including information preparation, transmission, reception, and interpretation, as it

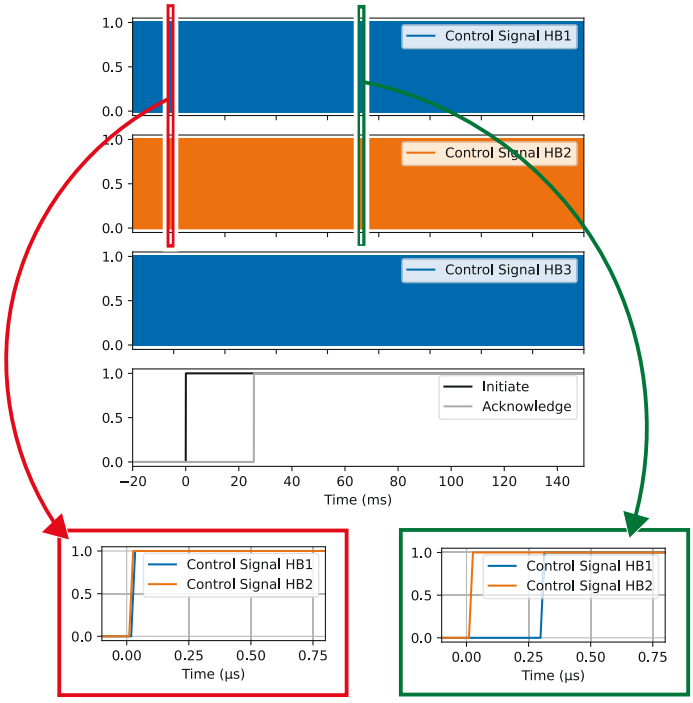


FIGURE 11.5. Four Level MLVSGD control signals during UART over BLE command transfer. The rising edge of the "Initiate" signal coincides with the initiation, and the rising of "Acknowledge" with the gate driver successfully enacting the command sent and received over BLE.

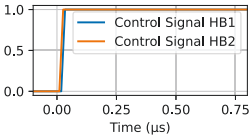
was defined earlier. By connecting the respective outputs of the ESP32 and TMS320F280049C to the MSO, measuring this information transfer delay can be practically determined.

11.4.3 Experimental Results

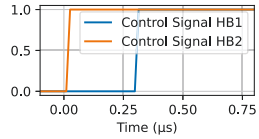
An exemplary measurement result of one experiment following the procedure described above is visualized in Figure 11.5. It depicts the control signals at 25 kHz provided to the three half-bridge circuits of the AGD, and the "Initiate" and "Acknowledge" signals that indicate the information transmission initiation and completion. The control signal periods are not clearly visible, as the PWM frequency is very high compared to the scope of delay introduced by the information transfer. To emphasize the influence of the transmitted command on the gate driver output, two zoomed-in views of the control signals of HB1 and HB2 that determine the gate driver output voltage at turn-on are shown in addition. This particular experimental result exhibits an information transfer delay of 25.7 ms.

As explained above, wireless control of the AGD is used to provide high-level control signals to the AGD, such as the change of $t_{\text{int,on}}$ or $t_{\text{int,off}}$ in the given AGD example. Thus, control of switching performance in regard to, for example, the switching loss energies, can be achieved. In particular, increasing $t_{\text{int,on}}$ for a given value of $V_{\text{int,on}}$ will result in increased switching energy during turn-on process. To show the impact of the control signal change on the behavior of four level MLVSGD and the SiC power MOSFET, more measurements are visualized in Figure 11.6. Figure 11.6a and Figure 11.6b again show the control signals of HB1 and HB2 at turn-on before and after the command has been transmitted. In addition, Figure 11.6c, Figure 11.6d, Figure 11.6e, and Figure 11.6f show gate-source voltage, as well as drain-source voltage and drain current measurements obtained from double pulse tests using identical AGD control parameters. A change of $t_{\text{int,on}}$ from 20 ns to 300 ns results in an increase in switching losses at turn-on from 0.92 mJ to 2.56 mJ. Manipulating the switching losses is a way to control the junction temperature of the power MOSFET, which can be used as part of an active temperature control directive [4]. Furthermore, in the presented demonstration case, the current slope was reduced from 0.673 A/ns to 0.328 A/ns, and the voltage slope was reduced from 21.0 kV/µs to 7.37 kV/µs. Finally, the drain current oscillation intensity and reverse recovery current peak could be decreased significantly, as can be seen in Figure 11.6e and Figure 11.6f.

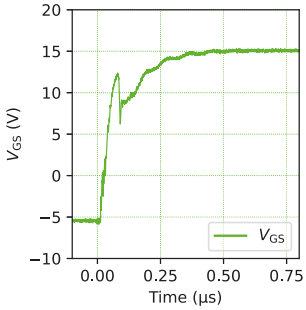
Similar to this demonstration example, the high-level wireless control of the AGD can also be used for adjusting other AGD parameters, such as the



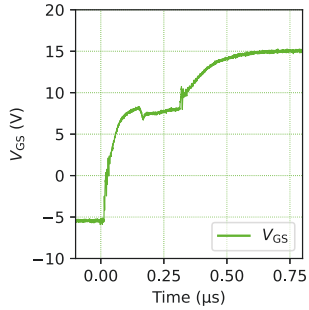
(A) Half-bridge control signals at turn-on before command ($t_{\text{int,on}} = 20\,\text{ns}$)



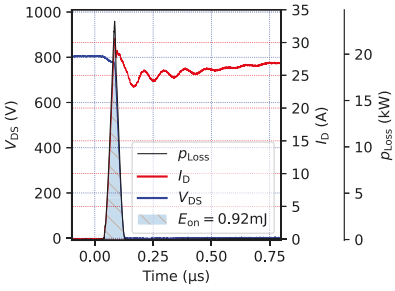
(B) Half-bridge control signals at turn-on after command ($t_{\text{int,on}} = 300\,\text{ns}$)



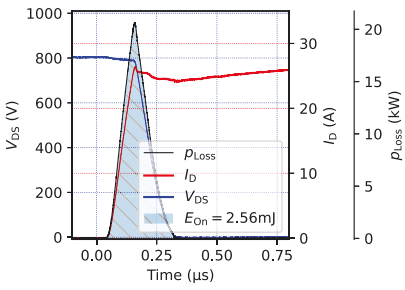
(C) Gate-source voltage at turn-on before command ($t_{\text{int,on}} = 20\,\text{ns}$)



(D) Gate-source voltage at turn-on after command ($t_{\text{int,on}} = 300\,\text{ns}$)



(E) Drain-source voltage, drain current, and instantaneous loss power at turn-on before command ($t_{\text{int,on}} = 20\,\text{ns}$)



(F) Drain-source voltage, drain current, and instantaneous loss power at turn-on after command ($t_{\text{int,on}} = 300\,\text{ns}$)

FIGURE 11.6. Double pulse test results using the control signal configuration shown (A) and (B). Gate-source voltage measurements (C) and (D), as well as drain-source voltage, drain current, and loss power as well as energy (E) and (F) before and after command transmission.

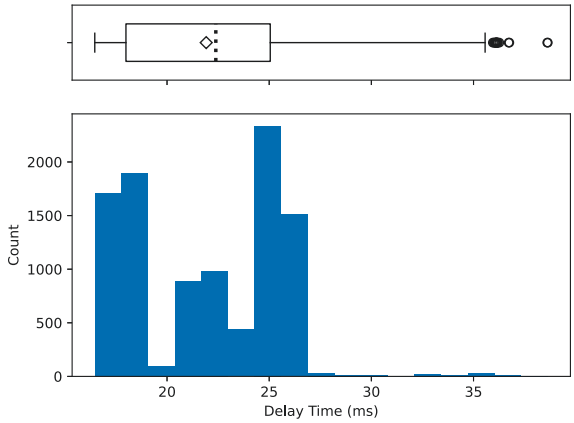


Figure 11.7. Information Transfer Delay Measurement Result

values of $V_{\text{int,on}}$ and $V_{\text{int,off}}$, and thereby manipulate the switching behavior of the SiC power MOSFET. In addition, the wireless control is not limited to this specific AGD, but can also be used with other AGDs.

The experiment described above demonstrates the general possibility of using BLE for wireless AGD control. However, only a large number of experiments can serve as evidence showing that the delay introduced by BLE is acceptable for the intended applications. Therefore, the information transfer delay measurement experiment was repeated for 10000 times, so that a statistically based delay characteristic could be derived. The delays measured throughout these experiments are visualized in Figure 11.7. The average information transfer delay is 21.9 ms, the median 22.4 ms, and the extremes are 16.5 ms and 38.6 ms. This confirms that the latency introduced by BLE is significantly shorter than 100 ms as stated in Table 11.2, even in a practical scenario for AGD control as the one presented in this work.

The string ":TEST:TDON 300" consists of 15 characters plus 2 end-of-line characters. The information transmitted over UART equals $17 \cdot 8$ Bit $= 136$ Bit. With a symbol rate of 9600 Baud, which is the maximum recommended for the BLE-UART bridge [30], and a symbol length of 1 Bit, the transmission of this string takes 14.2 ms. Optimizing the command alphabet could therefore significantly improve the information transfer delay.

The experimental results show that the wireless connection between the ESP32 and TMS320F280049C MCUs over BLE can be realized with a information transfer delay below 40 ms. This enables control over, for example, the switching losses and voltage and current slopes in the AGD driven SiC MOSFET. As laid out earlier, possible applications include Active Temperature

Control and EMI control.

11.5 Conclusion

This paper provides a practical approach for assessing the use of Wireless Communication Technologies (WCTs) for information transfer in Power Electronics Systems (PES). A basic future PES structure that incorporates AGDs and incorporates Information Transmission Routes (ITRs), is presented and the characterization of ITRs is systematized with a novel ITR taxonomy. Seven specific WCTs are characterized with respect to their latency, range, and data rate. For every ITR, a recommendation for or against using WCTs is given, and suitable WCTs among the previously presented are indicated. In particular, the ITR between converter and AGD control receives special attention by examining safety implications in greater detail.

With its focus on converter level signal transmission, the proposed taxonomy is a great tool for power electronics engineers who consider using wireless ITRs to improve the converter design, and it also helps to coordinate efforts between design engineers that each are responsible for different components within a PES. In addition, the taxonomy helps to define an interface to grid control for the interconnected electrical network of the future.

Experimental results demonstrate the control of a four level MLVSGD by means of UART over Bluetooth Low Energy (BLE). The results show that using this WCT, a remote MCU can exert full control over the features of an AGD. For example, the switching losses of the SiC MOSFET driven by the Four Level MLVSGD can be manipulated with an associated information transmission delay below 40 ms which is sufficient for applications such as Active Temperature Control.

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