Master's thesis

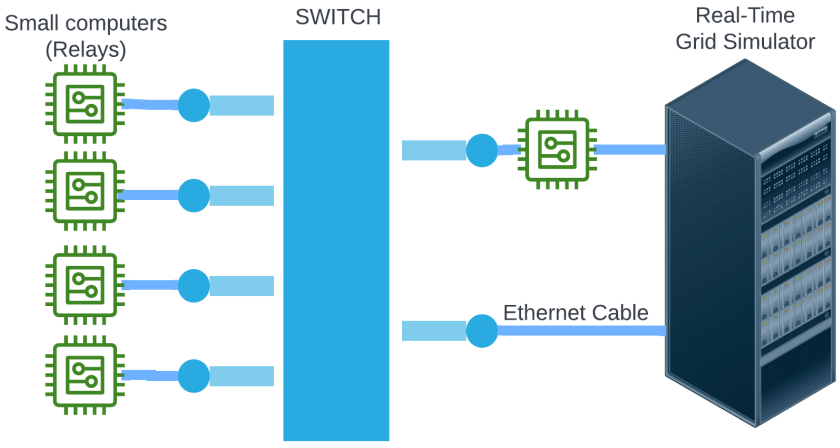
NTNU
Norwegian University of Science and Technology
Faculty of Information Technology and Electrical Engineering
Department of Electric Power Engineering

Karl Fredrik Anker Wirgenes

Proposal and Evaluation of a New Short Circuit Protection Algorithm for Active Meshed Distribution Grids

Harnessing IEC61850 communication and Hardware In the Loop simulation

Master's thesis in Energy and Environmental Engineering
Supervisor: Hans Kristian Høidalen
Co-supervisor: Tesfaye Amare Zerihun, Thomas Treider
June 2023



NTNU
Norwegian University of
Science and Technology

SINTEF

Karl Fredrik Anker Wirgenes

Proposal and Evaluation of a New Short Circuit Protection Algorithm for Active Meshed Distribution Grids

Harnessing IEC61850 communication and Hardware In the Loop simulation

Master's thesis in Energy and Environmental Engineering
Supervisor: Hans Kristian Høidalen
Co-supervisor: Tesfaye Amare Zerihun, Thomas Treider
June 2023

Norwegian University of Science and Technology
Faculty of Information Technology and Electrical Engineering
Department of Electric Power Engineering

NTNU
Norwegian University of Science and Technology

Preface

This master's thesis concludes my MSc degree in Energy and Environmental Engineering at the Norwegian University of Science and Technology (NTNU). It was written at the Department of Electrical Energy, in collaboration with SINTEF, through the Center for Intelligent Electricity Distribution (CINELDI). The thesis is the continuation of my project report [1], which was an extensive literature review.

I would like to thank my supervisor Hans Kristian Høidalen (NTNU), Co-Supervisor Tesfaye Amare Zerihun (SINTEF), and Co-Supervisor Thomas Treider (NTNU/SINTEF) for providing good assistance throughout the year. I would also extend thanks to the ProDig project for letting me use the real-time simulator at NTNU. Furthermore, without the Raspberry Pis from the Department of Information Security and Communication Technology (IIK) and the Department of Engineering Cybernetics, this master's thesis would not be possible. I would also like to thank Pål Sturla Sæther (NTNU) and Ergys Puka (NTNU) at IIK for introducing me to the 5G laboratory.

Karl Fredrik Anker Wirgenes
Trondheim, June 2023

Abstract

Meshing the high voltage distribution network (DN) is a strategy to address future challenges related to voltage and overload issues caused by increased load and distributed generation (DG) in the DN. However, due to economic and algorithmic limitations, standard protection methods have reliability problems in an active meshed DN. Particularly in the case of islanded mode with only inverter-interfaced DG. Therefore, this thesis's primary objectives were to *propose* a phase-fault protection scheme for an active meshed distribution network, to *build* a Hardware In the Loop (HIL) test bench, and to *evaluate* the proposal using the HIL test bench.

The proposed algorithm was to run the existing CCA and IJump schemes in parallel. Both schemes utilize changes in positive sequence (PS) current during fault to locate the fault. IJump was expected to locate faults in radial conditions, while CCA was expected to locate faults in meshed conditions. The thesis also proposed additional settings, a hierarchical structure of relays, and the use of a non-traditional PS phasor calculation method.

The HIL test bench consists of an OPAL-RT and five credit card-sized computers called Raspberry Pi (R-PI). The OPAL simulates the DN with DG in real-time. It communicates IEC61850 current samples to the R-PI, which emulates the relay. The relay was implemented with C-code. In the event of a potential fault, the R-PI communicates an IEC61850 GOOSE message back to the OPAL. The GOOSE message can result in a circuit breaker opening in the simulation.

The proposed algorithm is reliable during normal operating scenarios. The thesis's main finding is that running IJump in parallel to CCA on meshed lines increased the number of faults seen and reduced the time to trip. The performance improvement stemmed from IJump's unexpected ability to sometimes locate faults on meshed lines. The suggested additional settings and requirements for a crude frequency estimator also improved reliability. The non-traditional method of PS phasor calculation did not reduce reliability but was not recommended due to reduced speed and insignificant advantages. While the current public 4G/5G network has too large maximum delay, the future public 5G network is expected to be a feasible solution for long-distance GOOSE communication. Three operating scenarios were found to have decreased reliability: cross-country fault, pre-fault line flow with a power factor near zero, and when the pre-fault line current is less or comparable to the line charging current.

Sammendrag

Masket drift av det høyspente distribusjonsnettet (DN) er en måte å motvirke fremtidig spenning og overbelastning-problematikk i DN grunnet økning i last og distribuert produksjon (DG). På grunn av økonomiske og algoritmiske begrensninger har imidlertid standard beskyttelsesmetoder pålitelighetsproblemer i et aktiv masket DN. Spesielt i seperatdrift med kun omformerbasert produksjon. Derfor var denne oppgavens primære mål å *foreslå* en fasefeil beskyttelsesalgoritme for et aktivt masket DN, å *bygge* en Hardware In the Loop (HIL) testbenk, og å *evaluere* forslaget ved hjelp av testbenken.

Mitt forslag var å kjøre de eksisterende CCA og IJump algoritmene parallelt. Begge algoritmene benytter endringen i positiv sekvens (PS) strøm under feil for å lokalisere feilen. Forventningen var at IJump lokaliserer feil i radielle forhold, mens CCA lokaliserer feil i maskede forhold. Oppgaven foreslo også ytterligere innstillinger, en hierarkisk struktur av reléer, og å benytte en utradisjonell måte for å beregne PS strøm.

HIL-testbenken besto av en OPAL-RT og fem datamaskiner i kredittkortstørrelse kalt Raspberry Pi (R-PI). OPALen simulerer DN med DG i sanntid. Den kommuniserer IEC61850 strømverdier til R-PI, som fungerer som relé. Relét var implementert med bruk av C-kode. Dersom et relé ser en mulig feil, vil den sende en IEC61850 GOOSE melding til OPALen. GOOSE meldingen kan medføre åpningen av en effektbryter i simuleringen.

Den foreslåtte algoritmen var pålitelig i normaldrift. Hovedresultatet til avhandlingen var at parallellkjøring av IJump og CCA på maskede linjer økte antall lokaliserte feil og reduserte frakoblingstiden. Forbedringen skyldes IJump uventede evne til å av og til lokalisere feil på maskede linjer. Mine foreslåtte tilleggsinnstillinger og krav til en frekvensestimator økte også antall observerte feil. Den utradisjonelle metoden benyttet for å beregne PS strøm påvirket ikke påliteligheten. Metoden er derimot ikke anbefalt, da den økte frakoblingstiden og har ingen vesentlige fordeler. Mens det nåværende offentlige 4G/5G-nettverket har for stor maksimum tidsforsinkelse, forventes det fremtidige offentlige 5G-nettverket å være en gjennomførbar løsning for langdistanse GOOSE-kommunikasjon. Det ble oppdaget at tre driftsscenarier har redusert pålitelighet: doble jordfeil, når linjestrøm før feil har effektfaktor nær null, og når linjestrømmen er på samme nivå, eller lavere, enn linjens ladestrøm.

Table of Contents

List of Figures

List of Tables

Abbreviations

ASDU	Application Service Data Unit
CCA	Change in Current Angle
CDF	Cumulative Distribution Function
CINELDI	Centre for Intelligent Electricity Distribution
CR	Central Relay
DFT	Discrete Fourier Transform
DG	Distributed Generation
DN	Distribution Network
DNR	Distribution Network Reconfiguration
DR	Distributed Relay
GC	Grid Connected
GOOSE	Generic Object Oriented Substation Event
HIL	Hardware in The Loop
ICD	IED Capability Description
IIDG	Inverter Interfaced Distributed Generation
LAN	Local Area Network
LL	Line to Line
LLG	Line to Line to Ground
LLL	Line to Line to Line
LVRT	Low Voltage Ride Through
PCC	Point of Common Coupling
PI	Proportional Integral
PLL	Phase Locked Loop
R-Pi	Raspberry Pi
SGDG	Synchronous Generator Distributed Generation
SV	Sample Value
TN	Transmission Network
URLLC	Ultra-Reliable and Low-Latency Communication
WAN	Wide Area Network

1 Introduction

The CINELDI project, which this master is a part of, focuses on the distribution network (DN) in the years 2030-2040 [2]. Therefore the proposed algorithm considers components that may not be feasible/practical with existing technology, yet it complies with prevailing trends. A key trend is the evolution of the smart grid, which is characterized by a proliferation of measurement points that require communication. Consequently, the proposal assumes a significant number of measurement points, with a 5G network in place for effective communication.

1.1 Motivation

A meshed high voltage (22 kV) DN is one way to mitigate the impact of voltage and overload problems due to increased distributed generation (DG) and load in the future DN. However, standard protection methods are not capable of protecting an active meshed DN that can operate in islanded mode with only inverter interfaced distribution generation (IIDG). To address this, the master thesis proposes a new protection algorithm for both two and three-phase line faults. As the Norwegian grid code now specify low voltage ride-through requirements (LVRT) for large DG units, the proposal should also react fast enough not to impede LVRT.

1.2 Objectives and approach

The thesis has three objectives: propose, build, and evaluate. I will propose a protection scheme, build a Hardware In The Loop (HIL) test bench, and evaluate the proposed protection scheme.

The first objective is to propose a protection scheme that shall work for an active DN. The scheme shall work for two and three-phase line faults in both meshed and radial operations. Earth faults are not considered, and the protection response shall be fast enough to not impede DG LVRT. My novel approach is to run the existing IJump and CCA schemes in parallel. I also propose additional settings, use a hierarchical structure of relays and test a non-traditional method of calculating the PS current.

The second objective is to build a HIL test bench which shall work as a proof of concept. The proposed scheme requires relays to be implemented on microprocessors and to use IEC61850 communication. To be a proof of concept, the proposed relays are therefore implemented on microprocessors, and actual IEC61850 communication over ethernet cables is used. To prove that the microprocessor is fast enough, the relays run in real time. To achieve this, an OPAL-RT is used to output measurement from a real-time grid simulation. As the literature review will identify many challenges associated with IIDGs, an IIDG controller satisfying the Norwegian grid code is also implemented.

The third objective is to evaluate the protection scheme using the HIL test bench. The evaluation has two goals. The first goal is to quantify and evaluate the factors affecting reliability. The second goal is to quantify and evaluate the factors affecting the protection system response time. With regards to the second goal, emphasis will be put on if public mobile networks are fast enough to not impede LVRT capability. The evaluation approach is split into a result and a discussion. In the results, aggregate results are used for quantifying the reliability and speed. While the discussion is used to explain the quantitative results.

1.3 Structure of the thesis

Between the introduction and the summary remarks, there are 7 chapters. These seven chapters go into the three objectives of propose, build and evaluate.

Propose

- **Section 2 (Background)** goes into the typical topology and protection of a DN. It then goes into the benefits of an active DN, what the protection problems are, and which protection solutions exist. It identifies the possibility of running IJump and CCA in parallel.
- **Section 3 (Theoretic analysis on the proposed method)** gives the theoretic proposal of the protection algorithm . Then it analyzes different subjects of the proposal, which must be understood before building a test bench.

Build

- **Section 4 (Modeling Grid and Generators for HIL simulation)** Goes into the system description and the implementation of the Grid, IIDG, and SGDG.
- **Section 5 (Modeling communication network and relays)** Goes into the implementation of CR in the Opal-RT, DR in the R-PI and the simple 4G/5G emulation. It also goes into how to set up IEC61850 communication between different computers.

Evaluate

- **Section 6 (Aggregate results)** Shows aggregate results of the protection scheme reliability and speed.
- **Section 7 (Discussion on the aggregated results)**. Explains the aggregate result by going into specific operating scenarios. It also discusses if there are operating scenarios that are not taken into account by the aggregate results.

It should be remarked that the theoretic analysis of Section 3 is an analysis of the theory needed to build the HIL testbench. It is not until Section 7 that the theory behind the protection response for different scenarios is presented. This is because this theory was developed by understanding the simulation results.

There are also appendixes. Appendix A gives code, grid parameters, and relay parameters, while Appendix B gives additional explanation and context for the interested reader.

2 Background

This chapter aims to first explain the current DN topology in Section 2.1, and then Section 2.2 explains the current status of short circuit protection in the DN. Chapter 2.1 and Chapter 2.2 are copies of the project report [1]. Section 2.3 will then do a literature review to explain that a meshed DN will help mitigate voltage and overload problems due to increasing load and generation in the DN. The problem, however, is how to protect this network cost-effectively. The literature review is a condensed version of the project report [1].

2.1 The Current Distribution Network

The Norwegian high voltage DN is operated at 1 kV to 22 kV and is either isolated or Peterson coil earthed. The DN connects to the subtransmission grid via the HV-MV transformer, as shown in Figure 2.1 for a 22 kV DN. Moreover, the DN is operated radially but often constructed with a ring/mesh topology. The network in Figure 2.1 has a mesh topology, but as the normally open (NO) tie switches are normally open it is operated radially. The normally open tie switches can be closed after a permanent fault to restore the supply to the load. Nonetheless, the new topology is still radial.

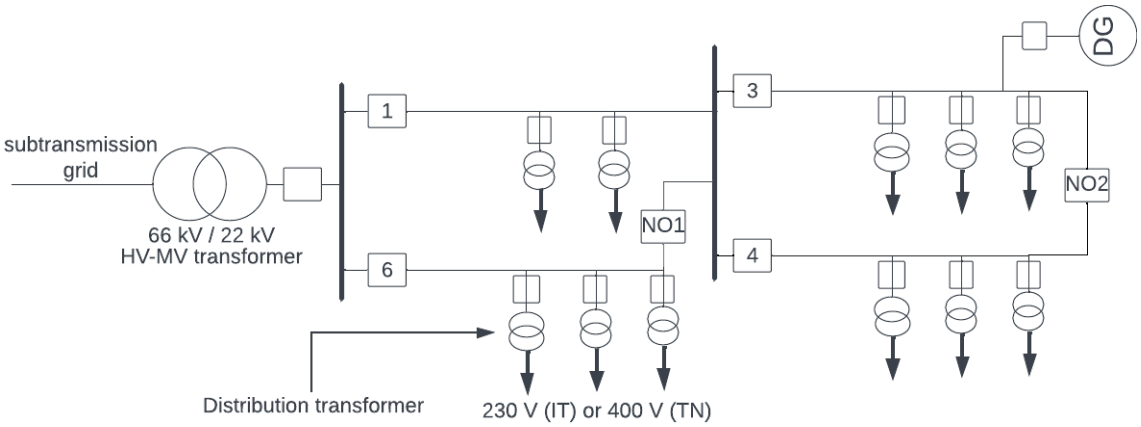


Figure 2.1: A typical distribution network constructed meshed but operated radially by using normally open (NO) switches.

Loads in the DN are typically interfaced through a distribution transformer and a fuse, see Figure 2.1. The loads are typically tapped loads meaning that at the interface of the distribution transformer, only the tapped line has a device to interrupt fault current, not the two-line ends as shown in Figure 2.2.

Most generation is connected to the transmission or sub-transmission grid, but there is an increasing amount of DG connected to the DN. DG units are typically photovoltaic, wind turbine generators, small-scale Hydropower, combined heat and power, diesel generators, or fuel cells. The DG definition has no standardized power limit, but typically DGs are much smaller than conventional production. Common power rating is less than 10 MW and typically no more than 1-2 MW [3]. Conventional production is interfaced through three CBs as shown in Figure 2.2. In comparison, DGs are often interfaced through a single CB, see Figure 2.1. This causes infeed inside a primary protection zone (intermediate infeed). During a fault, an undervoltage relay automatically disconnects the DG. In Norway, this typically occurs when the voltage is less than 0.8 pu for 0.2 s [4]. Hence, DG-LVRT is not utilized, and DGs don't need to be considered for protection studies.

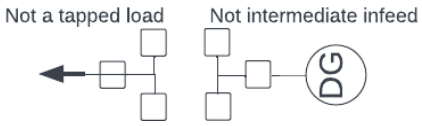


Figure 2.2: Shows an example of what is not a tapped load and not intermediate infeed.

2.2 Short circuit protection in the current distribution network

For the radial DN, non-directional overcurrent is used. Overcurrent provides selectivity, reliability, and moderately fast response for three and two-phase faults while being inexpensive and simple. One of the reasons it is inexpensive is that the relays can only see the fault current going in the downstream direction, so no voltage measurement for direction determination is needed. It is a simple scheme as the uni-directional fault current means that the relays only need to coordinate in the upstream direction (blue lines in Figure 2.3).

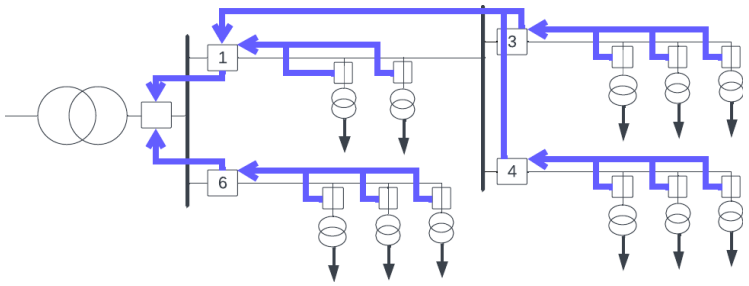
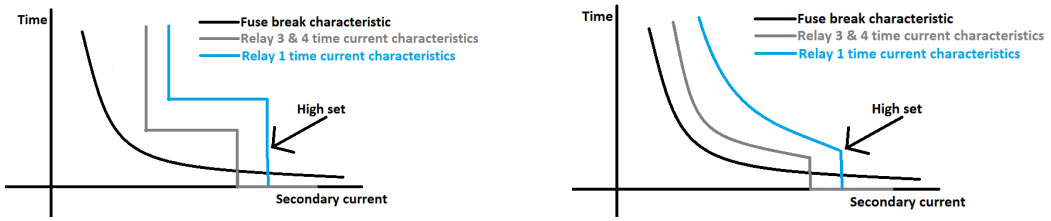


Figure 2.3: Which protective elements needs to directly coordinate in a radial DN.

Because the subtransmission grid has a large short circuit capacity, there is a big difference between load and fault current in the DN. This is advantageous as then it is easy to use the RMS-current as a fault indicator. However, the RMS-current cannot be used alone for coordination. For example, for a fault close to relay 3 in Figure 2.3 most fault currents through relay 3 will also go through relay 1. This is why time grading, as shown in Figure 2.4, is needed. Time grading means that as one moves in the upstream direction, each successive protective-element/relay adds a 0.2-0.3 s time delay/coordination time interval (CTI) [5]. The



(a) Definitive time

(b) Inverse time

Figure 2.4: Time-current characteristic of protective elements of the upper feeder. All fuses have the same characteristic, and R3 and R4 have the same characteristic

additional time delay results in long trip times for faults at the start of the feeder. To lower tripping times, a high set element is used, see Figure 2.4. The high set trips instantly for faults with the highest currents inside the primary protective zone.

To summarize, the significant difference between load and fault current means that a pickup current can be chosen so that most upstream relays can see the fault. An increasing time delay as one moves upstream means that the first relay upstream of the fault trips first (selectivity), but if it fails the next upstream relay is

backup. Therefore, a relay in this protection scheme will always trip when supposed to (dependability), but never when not supposed to (security).

2.3 Literature review

To goal of this section is to do a literature review to arrive at my proposed protection scheme. The review is split into three reviews on the benefits of the DN in Section 2.3.1, challenges in Section 2.3.2, and solutions in Section 2.3.3. The subchapter ends with Section 2.3.4, which puts my proposal in the context of the literature review. Note that the literature review is only based on the major findings of the project report [1].

2.3.1 Why mesh the grid and use DGs

Figure 2.5 shows the benefits of a meshed DN with DGs. Observe that most of the benefits of meshing and DG are similar. Additionally, [6] shows that a meshed grid has higher DG capacity creating a positive feedback loop. Keep in mind that if the DG amount becomes too large, the benefits of DG generally become drawbacks [7]. For example, high DG penetration could mean significant export on the high resistive lines of the DN, causing a higher total power loss. The next paragraphs will go into the benefits shown in Figure 2.5.

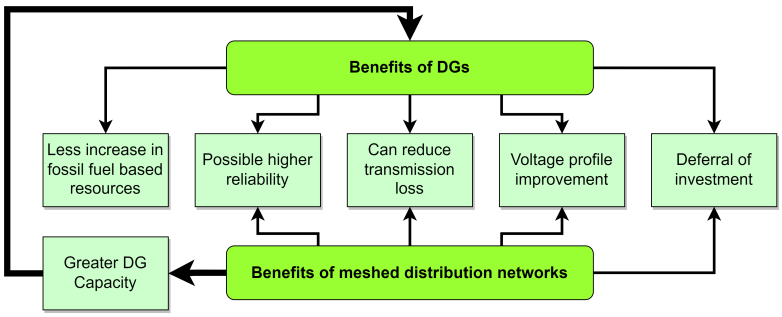


Figure 2.5: Benefits of meshed distribution networks containing distributed generation. Made by me in [1].

DGs improve reliability by being able to supply the loads in islanded mode. This requires at least one of the DGs in the islanded grid to provide frequency and voltage control. To harvest these benefits, the protection scheme must be able to tackle adverse frequency events associated with islanding, and the protection system must isolate the fault fast enough to ensure that the DG does not trip due to low voltage. On a system level, DGs increase reliability as the Norwegian Energy Directorate (NVE) has identified DGs as one of the solutions to prevent a future (instantaneous)power deficiency [8]. A meshed/ring grid provides increased reliability as a line disconnection in the meshed grid does not interrupt the power flow to the load.

According to [9], 45% of all losses are in the distribution system. DGs can reduce this loss by limiting reactive and active power transport by producing it locally [10]. [11] points out that local active power generation only reduces active power transport/loss in the DN if: the load and generation profile intersects, the penetration level of DG is low enough (not excessive export), and load centers in the DN are close the DG location (very resistive lines in the DN). Lastly, theory and real-life tests in [7, 12, 13] show that a meshed grid naturally balanced out power flows resulting in lower loss than a radial configuration. As meshing reduces loss for a given current injected into the DN it also increases DN capacity. This is beneficial as NVE points out that EV charging can, in 2030, cause overloads of cables in the high-voltage DN [14]. If the future DN topology will changes continuously to always have optimal load flow, so-called distribution

network reconfiguration (DNR), a meshed system will have more possible solutions.

DGs and meshing of the grid are expected to cause a more flat voltage profile [7, 10, 15]. Norwegian DSO is already experiencing voltage problems due to DG. For example, as stated by Norwegian DSO Agder Energi Nett (now Glitre Nett), distributed power production (solar) currently causes voltage profile problems [16]. This is because the typical tap changer of a Norwegian distribution transformer has been manually adjusted for large voltage drops on the radials during high winter loads[17].

To summarize, a meshed DN has many benefits, and it can be a part of the solution for accommodating a greater amount of generation and load in the DN while handling voltage and overload problems. It has also been pointed out that another benefit is that the DN is already often constructed meshed. In the upcoming text, the disadvantage will be highlighted. It will point out that a meshed grid has economic and algorithmic problems with regard to protection.

2.3.2 Summary of the root protection challenges of an active meshed DN

In chapter 2.2 of the project report, nine root protection challenges of an active meshed DN were identified. This subchapter will go over them and identify how they apply to overcurrent and distance protection.

Bi-directional power flow is caused by both meshing of the grid and the use of DG. With a possible energy flow in both directions, standard overcurrent must be equipped with a voltage measurement for direction identification. To avoid faulty direction identification, unit protection schemes such as differential can be used.

Active meshed DN will also cause greater fault current variation meaning that the same fault will give rise to a larger variation in fault current depending on when it occurs. A meshed grid with varying fault levels makes especially overcurrent hard to coordinate. Fault current variation can be caused by dynamic topology changes caused by the DNR, or it can be due to a DG connection status that varies. A connected DG will typically increase the fault current into the fault, but relays upstream of the fault will typically experience less fault current. This effect is called protection blinding, and it also effect distance protection through overreach.

Coordination with lateral protection, which is typically the fuse before the distribution transformer, is also a challenge in a meshed DN. Additionally, coordination with tapped loads and intermediate infeed is problematic as then there is an outfeed/infeed inside the primary protective zone. For typically meshed transmission grids, infeed/outfeed occurs in the backup protective zone, which makes coordination easier. The problem of intermediate infeed and outfeed can be solved by detailed studies and settings, such as in the few multi-terminal lines in the transmission network. However, the DN is much bigger, and doing frequent detailed studies would require a lot of resources. Another option is to avoid infeed/outfeed in the primary zone by having a transducer and protective devices at all interfaces (typical for transmission grid). Taking tapped loads into account, this would be very costly in the DN.

DGs present further complications due to DG-LVRT and the IIDG control system. Because maintaining DG-LVRT requires that there is a fast protection system. Furthermore, compared to the traditional generation, the IIDG control system is what decides the fault contribution right after a fault. It will typically cause low fault currents and symmetric currents even for unsymmetrical faults. Furthermore, [18] discusses how the IIDG fault current can cause the directional element of overcurrent and distance protection to respond incorrectly. Keep in mind that overcurrent and directional protection failure is expected when there is no traditional generation to dominate the fault current. A typical case could be islanded operation with IIDG. Another case could be a large IIDG placed on a radial and a fault occurring on the radial upstream of the

IIDG.

Due to Norwegian DN being either ungrounded or Peterson coil earthed, earth faults are a big challenge for active meshed DN. Norwegian regulation requires that in the DN, earth faults are isolated within 10 s [19]. Currently, this is no problem as there are automatic earth fault relays for radial systems. For the non-directly earthed regional and transmission grid, which is often meshed, the same law stipulates 120 min. In the author's experience, it is not unheard of that in the regional and transmission grid. This limit is frequently surpassed. This is because while the voltage measurement easily identifies that there is an earth fault, there are no reliable automatic methods that identify the earth fault location in meshed operation. Instead, manual sectionalizing is used [20]. Thus if there shall be an active meshed DN that is isolated or Peterson earthed, it also necessitates the development of an algorithm that can satisfy the 10 s limit for earth fault. Single-earth faults will not be the topic of this thesis as the thesis focuses on three-phase faults, two-phase faults, and cross-country faults.

To summarize, in an active meshed DN, it is hard to coordinate overcurrent relays. Distance protection can be used, but to solve infeed/outfeed challenges, more measurement points are needed. Additionally, during islanded mode with only IIDG, the directional element of overcurrent and distance protection can be prone to failure.

2.3.3 What are the protective solutions

The main part of my project report was the discussion of a large literature review discussing new protection algorithms for an active meshed DN. This subsection will condense the main findings into four parts. The four parts cover modification to existing overcurrent, distance, and differential schemes, and then the last part will look into novel protection schemes.

Modifications to overcurrent:

In the literature, the coordination of overcurrent in an active meshed grid is solved through an optimization problem. Coordinating overcurrent in a meshed grid is not easy, and therefore the solution to the optimization problem is long tripping times. A large focus of the literature is, therefore, to reduce tripping times. Examples are fault current limiters to restrict the influence of DGs [21–24], dual setting relays with separate current characteristics in forward and backward directions [25–29], and a time-current-voltage characteristic [28, 30]. Adaptive solutions involve changing relay settings groups dynamically, either online [31] or offline [32–35], with triggers based on DG status, output, or CB status. Adaptive protection reduces tripping times as the coordination problem is solved for only one grid situation. Other approaches include dual operation mode [36–39] where grid-connected has traditional overcurrent, but islanding triggers a new protection algorithm such as purposely using IIDG to inject harmonics which is then used for fault localization [39].

The main problem with all overcurrent solutions is that even if direction identification during IIDG-dominated fault current was not a problem, the solutions still have a slow protective response which impedes DG-LVRT. Furthermore, the articles did not take into account tapped loads which means that there must be VT, CT, Relay and CB at all interfaces, including tapped loads. Therefore, this thesis does not use overcurrent.

Modifications to distance protection:

Assuming the correct working function of the directional feature during IIDG-dominated fault currents, the inherent directionality, a reach less dependent on the current, and the ability to handle high resistive faults

is the argument for using distance protection for active meshed DNs [40, 41]. The challenge with using distance protection is intermediate infeed, tapped loads, and coordination with lateral protection. Solutions to tapped loads include installing VT/CT at tapped loads and communicating a temporary blocking signal when they detect a downstream fault [42]. The use of intertripping signals such as blocking, permissive, and direct is a common way to improve relay coordination [41, 43, 44]. To solve the challenge of DG-infeed, a proposal is to use infeed correction where the DG output is either estimated or communicated [45, 46]. A challenge with DG infeed correction is that the correction should not be applied if the fault is between the DG and relay, but when the correction takes place, the fault location is unknown. Instead of correcting the current, another proposal is to communicate a change of settings/reach when the DG connects/disconnect [44].

[47] had a problem with DG blinding distance protection in meshed configuration and therefore proposed ”loose coupling”. Loose coupling means that specific CBs are triggered during fault to make the grid radial where protection is easier. This leads to slow response as current interruption takes time. There were also articles such as [48, 49] where impedance measurement on the ”fault component” makes the impedance measurement *ideally* independent of the pre-fault condition. Lastly, it was seen in the project report that most distance protection schemes did not take into account tapped loads. The possible failure of the directional element and the need for many new CTs and VTs is why distance protection was not used in this thesis.

Modifications to differential protection:

Traditional differential protection would require many measurement points, including at tapped loads. Therefore, the main problem of differential protection is economic rather than due to algorithmic problems [18, 50]. While this is correct in theory, I would point out that in practice, most of the proposed overcurrent/distance protection schemes required a similar amount of measurement locations. Nevertheless, the focus of the differential protection schemes in the literature is to reduce economic costs and incorporate backup protection.

[39, 51] reduces economic cost by having one or a few IEDs/agents taking measurements and coordinating the protection response for multiple protective zones instead of the traditional master-master [52, 53] or master-slave coordination [36]. [54] proposes a further reduction in the economic cost by having the protective zones to be larger. They find the optimal zone size by minimizing the cost of outages and equipment. A further reduction in cost is achieved by accepting open zones meaning that not all zone interfaces are measured [51, 55, 56]. This creates a challenging coordinating problem as zones need to be coordinated against each other. With regards to backup, [51] proposes overlapping zones. In this thesis, differential protection was not used as it necessitates continuous communication over long distances.

Novel solutions:

A novel protection solution is the use of Artificial Intelligence (AI) such as Fuzzy Logic (FL) [57], Decision Tree (DT) [58, 59], Support Vector Machining (SVM) [60], and Artificial Neural Networks (ANN) [61]. In FL measured quantities are converted into fuzzified variables, which are then put up against explicit human-made rules. A more advanced AI is DT or SVM. In DT and SWM, data mining on simulation results is used for the automatic generation of explicit tripping conditions/rules, which are then used for protection. An ANN can also train on simulations, but the output is a neural network, not explicit rules, so it is more difficult for the relay engineer to understand what occurs ”under the hood”. There are also other novel solutions, such as [39], which use only communicated voltage measurements for fault identification.

Other schemes, such as those proposed by [50, 62], look at the change in positive sequence current angle at a given point over a time period. They argue that if fault current can be fed from both line ends, then the faulty line is uniquely identified by the fact that only one line end has a significant change in positive sequence (PS) angle. Because, at a healthy line, the current into the line and out of the line is similar. Therefore the healthy line will either have a significant angle change at both line ends or at none. Accordingly, in the event of a significant change in angle, [50, 62] communicates this binary information across the line to potentially result in a tripping decision. This scheme will be referred to as CCA, and a significant change in PS angle during a cycle is referred to as a CCA-condition.

Due note that CCA differs from the traditional phase comparison scheme (ANSII 87PH), where either the current angle [63] or the time of current zero [64] is continuously communicated across the line. It is different because, in CCA, it is only in the event of the seldom sudden change in angle that information is communicated. This is why CCA will be used in the master thesis.

A problem with CCA is that in radial operation with no current infeed on the far end, the scheme does not work. Therefore a scheme that observes the fault when the fault current is fed from one is needed. A recent trend is to use the rate of change of the current magnitude as in [65]. If a fault occurs on a radial line without DG. Then the start of the faulty line is expected to be identified by a sharp current increase (Jump up) at the start of the line, and a sharp current decrease (Jump down) at the end of the line. Therefore if the PS current magnitude has a sharp increase or decrease during a cycle, this is communicated. From now on, a sudden increase or decrease in PS current magnitude is referred to as an IJump-condition. A scheme using a sudden increase or decrease in the current magnitude will be referred to as IJump.

2.3.4 My proposal in the context of the literature review

My novel proposal is to run CCA and IJump in parallel. At each line interface, there will be a CT and a small microprocessor acting as a distributed relay (DR). The DR detects if there is a CCA or IJump condition and then communicates a GOOSE message to the Central Relay (CR). There is only one CR in the grid, and based on the incoming GOOSE message and IJump/CCA principals, it locates the fault. How the literature review influences this proposal is given below.

- Long-distance communication which is between DR and CR is seldom and only occurs when there is a possible fault. Not continuously, as in differential protection.
- There is a need for many new measurement points at all line interfaces. However, the advantage is that only current measurements are needed, not also VTs, as in overcurrent and distance protection. Installing current measurements at existing T-junctions will be costly, and new CT technology is probably necessary.
- Most of the schemes in the literature review used CB at all line interfaces. My proposal will not. The next chapter will explain why the CR knowing the current topology, facilitate that the number of relays is decoupled for the amount of CBs. The hierarchical structure of relays was not used in the referenced schemes on CCA and IJump, but was inspired by the already referenced scheme [39, 51], which did it on differential protection.
- The literature review defined adaptive schemes and dual operation mode. Running IJump in parallel is neither. Parallel operation means that both schemes are *always* activated. In dual operation, schemes are activated and deactivated during operation. While in adaptive protection, the settings of the protection scheme are changed during operation.

- CCA and IJumps rely on the transition between faulty state and healthy state. This has the advantage that the scheme detects the fault fast. The disadvantage of relying on the transition to the faulty state is that the algorithm does not see the fault after the transient state. This is a major disadvantage compared to the standard, overcurrent, distance, and differential schemes.

2.4 Background on communication network performance

Before going into the theoretic analysis of the protection scheme proposal, the background will be given on communication networks. Because to facilitate long-distance communications, it will be proposed to do GOOSE communication from DR to CR and from CR to CB through a public mobile network (4G or 5G). This is a cost-saving measure as it avoids the installation of dedicated fiber cables or equipment for Power-line communication. On the downside, a public mobile network is expected to have lower communication performance. The next paragraphs will therefore do a survey on the service availability, latency, and jitter of public 4G and 5G networks. Service availability is the percentage number of packets arriving at the destination while satisfying the quality of service, latency is the average communication delay, and jitter is the standard deviation of communication delay (how much the delay varies).

[66] showed that the current public mobile network in Norway does not have the 99.9999 % service availability required in [67] by the 3GPP standard organization.

Regarding latency and jitter, [66, 68, 69] emphasized that the primary concern lies with jitter, not latency. This is illustrated in [66], which reviewed measurements from Austrian public 4G and 5G networks. For the 4G network, the average round trip latency was 29 ms with 220 ms being the 99.9 percentile. The 5G network measurement had similar results. As the 99.9 percentile value considerably exceeds the latency, maintaining consistently low communication delay poses a challenge. In some studies, such as [70], 5G networks had inferior performance compared to 4G. 5G inferiority can be due to 5G networks is still a developing technology. Because as [71] points out, most service provider adopts a non-standalone 5G approach. Meaning in a transition period, only the radio/wireless part is 5G while the core/cabled part is still 4G. Nevertheless, none of the studies saw public 4G or 5G networks meeting the 10 ms maximum one-way delay requirement of IEC TR 61850-90-12:2020 for inter-tripping using WAN communication [72].

While service availability, latency, and jitter requirement cannot be met by the current public 4G/5G networks, the studies propose solutions. [66] concludes that 4G networks can meet the 3GPP requirements if the 4G network is reconfigured. [68, 69] points out that configuring a 5G network for a specific purpose is easier. Because 5G network *will* supports network slicing, which 4G does not. Network slicing means that a single physical 5G network can consist of multiple virtual 5G networks, each designed reliability, latency, and security requirements of a specific application. As explained in [69], 5G networks of the future will also allow for URLLC, meaning that the networks, according to 3GPP, shall have a latency of less than 1 ms and service availability of over 99.999 % [73].

3 Theoretic analysis on the proposed method

This section starts with a thorough description of the proposed protection algorithm in Section 3.1. During the explanation, it will be found that the following key subjects need to be analyzed to develop the protection scheme: Section 3.2 (Positive sequence phasor calculation), Section 3.3 (Simple frequency estimation), Section 3.5 (Communication using IEC61850), Section 3.6 (Measurement accuracy of Current Transformers), Section 3.7 (Distributed Generation control and low voltage ride through)

3.1 Proposed protection algorithm

The section will go over the *theoretic* proposal for the protection scheme. Each part will go over the parts of the proposed algorithm presented in Figure 3.1, and will end with a paragraph describing how my proposal is different from the schemes on which the article is based upon.

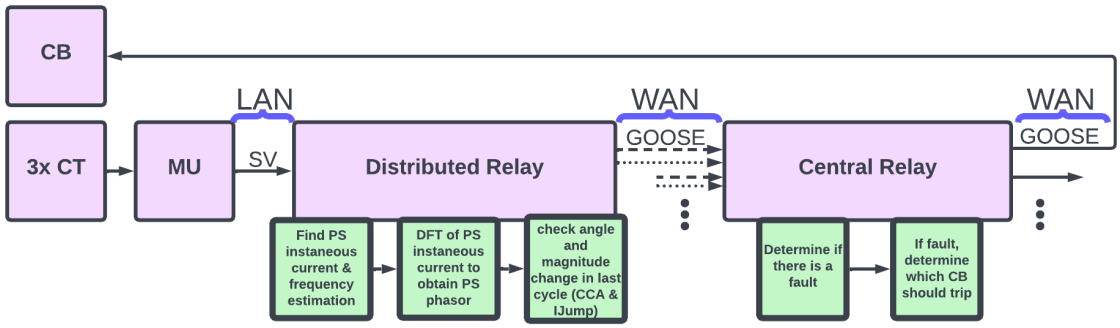


Figure 3.1: Theoretical proposal of the protection scheme. Blue boxes are physical elements, while green boxes are algorithms executed by the physical elements. MU = Merging Unit, PS = Positive Sequence, DFT = Discrete Fourier Transform, LAN = Local Area Network, WAN = Wide Area Network.

The main takeaway of this section is that:

- My proposal combines IJump and CCA in *parallel*. CCA is expected to identify faulty lines fed from both sides while IJump is expected to detect faults being fed from one side.
- My proposal introduces the positive sequence instantaneous current to see if the computational benefit of one DFT rather than three was great enough to outweigh the protection disadvantages.
- My proposal introduces a single central relay to facilitate less CB than relays in a dynamically changing topology.

3.1.1 From currents to communicated digital signals

Starting at the three CT in Figure 3.1, the currents are sampled 20 times per cycle which are then digitized by a merging unit. These sampled values are then communicated over a process bus to the distributed relay (DR). The communication will satisfy the communication protocol IEC61850-9-2 which from now on is referred to as Sample Value (SV) communication.

The article on which this thesis is based did not take into account IEC61850-9-2, as I will do in this thesis. IEC61850 communication will be further discussed in Section 3.5.

3.1.2 Working function of the distributed relays

As seen in Figure 3.2, at each line interface, including at tapped loads, there will be a DR accompanied by a CT. The DRs are in charge of communicating a GOOSE message to the Central Relay (CR) when there *potensially* is a fault (CCA or an IJump condition). The goal is that the DR is small and can be implemented on a microprocessor. In Figure 3.1 it is seen that the DR has three separate sub-steps that will now be gone through.

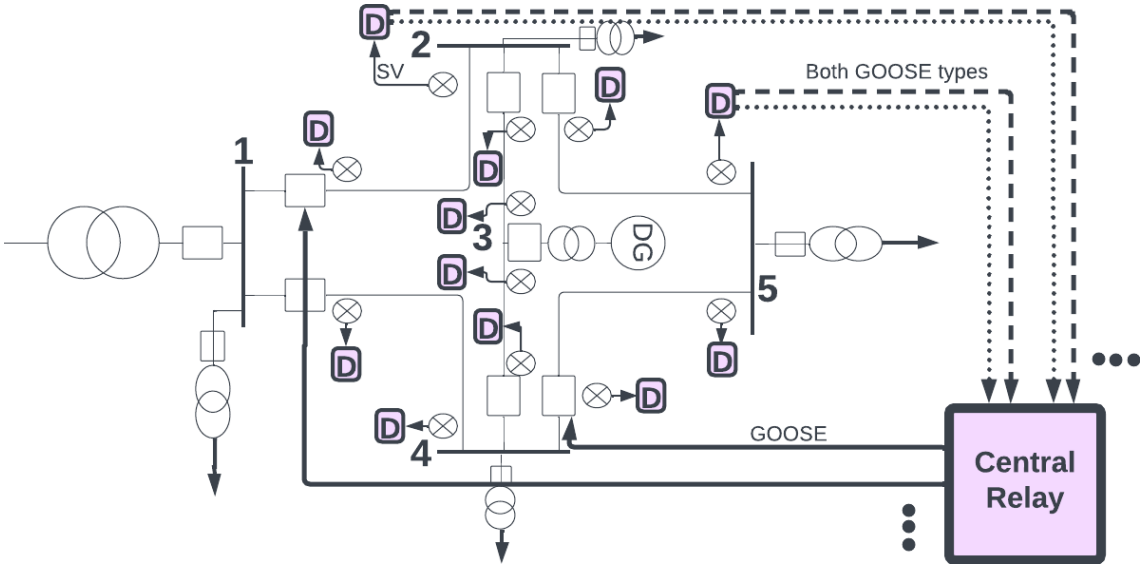


Figure 3.2: Location of the distributed relays, D. X symbols contain CT and MU. The central relays receive goose from ALL DR and can trip ALL CBs.

Step 1 of the DR. Frequency estimation and phasor calculation:

The DRs achieve their objective by taking in the SV every 1 ms and passing them through a low-pass filter, and then doing a crude estimation of the frequency. The SV is then used to calculate the instantaneous positive sequence current in Equation 1. The instantaneous positive sequence current is equal to the generalized positive sequence component in [74]. With the exception that the expression below has excluded the zero sequence part used in [74].

$$i_{PS}(t) = \frac{1}{3}(i_a(t) + i_b(t - \frac{2}{3}20\,\text{ms}) + i_c(t - \frac{1}{3}20\,\text{ms})) \tag{1}$$

Step 2 of the DR. DFT to obtain PS current:

The DFT is then applied to the positive sequence instantaneous current to obtain an estimate of the positive sequence phasor. I will refer to this estimate as the ”instantaneous method”. The method is given a specific name as the traditional method of calculating the PS current phasor is not the DFT of Equation 1, but rather:

$$\mathbf{I_{PS}} = \frac{1}{3}(\mathbf{I_a} + a\mathbf{I_b} + a^2\mathbf{I_c}) \tag{2}$$

The instantaneous method is used because it is expected to be more computationally efficient as it requires one DFT instead of the three DFTs. More computationally efficient means that it is simpler to implement the algorithm on the proposed microprocessor. It must be evaluated if the instantaneous method gives a good protection response.

Step 3 of the DR. Check for CCA and IJump condition:

After estimating the positive sequence phasor, the DR will store it inside a buffer. The buffer is used to compare the current PS-current to the value one cycle ago (t_{cycle}). t_{cycle} depends on the measured frequency. If the comparison indicates a CCA or IJump condition, it will send a GOOSE message according to IEC61850-8-1 to the CR indicating this. The GOOSE communication will be through a public 4G or 5G network.

The definition of a CCA-condition uses the CCA-angle in Equation 3. The angle will be mapped to $(-180°, 180°]$:

$$\textbf{CCA-angle} = \angle \mathbf{I}_{PS}(t) - \angle \mathbf{I}_{PS}(t - t_{cycle}) \tag{3}$$

Then a CCA-condition is when the absolute value of the CCA-angle is greater than ϕ_{CCA}. In the evaluation of the scheme ϕ_{CCA} will be set to 90°. The communicated GOOSE message will then have a Boolean value set to "true", which turns to "false" as soon as there is no CCA condition. The discussion of this thesis will identify that at a current of $I_{CCA-disable}$ or less, the CCA scheme must be disabled in the DR. It will be explained that this is due to the large capacitive line charging current compared to the line current.

Let the IJump-magnitude be the current PS magnitude divided by the PS magnitude a cycle ago:

$$\textbf{IJump} - \textbf{magnitude} = \frac{|\mathbf{I}_{PS}(t)|}{|\mathbf{I}_{PS}(t - t_{cycle})|} \tag{4}$$

There is then an Ijump condition if the IJump-magnitude is greater than ϵ_{up} or less than ϵ_{down}. These values will be set to 1.1 and 0.9, respectively. The GOOSE message indicating an IJump condition will contain a "1" or "-1" if it was activated by ϵ_{up} or ϵ_{down}, respectively. When there no longer is an IJump-condition the value is "0".

Additional comment on the distributed relays

Compared to the articles on which the scheme is based, $I_{cca-disable}$ is a setting proposed by me. Additionally, they did not use frequency estimation. I do frequency estimation because I want the scheme to work in the transition between grid-connected and sudden islanding when great frequency deviations are known to occur. Lastly, compared to the referenced articles, I will implement the GOOSE communication, and I will implement the DRs on several microprocessors called Raspberry-Pi (R-Pi) to confirm that the computational requirements are low.

3.1.3 Working function of the central relay

The single CR in the grid takes in the time-stamped GOOSE messages from all DRs in the grid. According to Figure 3.2, the GOOSE message is used to determine if and which line is faulty. If there is a fault, it finds the correct set of CBs to isolate the fault. The CR runs its algorithm every 1 ms.

Step 1 of the CR. Find if and which line has a fault:

If a line can be fed with fault current from both ends, it will be referred to as operating in "meshed condition". On the other hand, if a fault current is fed from only one end, it is called a "radial condition". Keep in mind that a radial line section with DGs on the far end will be in "meshed condition".

When a line is operating in "meshed condition", it is expected that the faulty line is *uniquely* identified by

only one line end having a CCA condition. In other words, that the CR only receives the CCA GOOSE message from one end of the line. If this is the case continuously for a period of t_{CCA} the CR diagnoses the line as faulty. t_{CCA} was not used in the references and it will be set to 4 ms. If $t_{DR->CR,communication,max}$ is the maximum time-delay of communication between the DR and CR, then the CR can only decide if the CCA indicates a fault at time $t_{DR->CR,communication,max} + t_{CCA}$ ago. Because for a more recent time, it can just be that there has been a CCA condition on both sides of the healthy line where the GOOSE signal from one line end has a longer communication delay. To not trip a healthy line, this potential GOOSE message must always be waited for as it will *block* the tripping. CCA is, therefore, a blocking scheme.

When a line is operating in "radial condition", it is expected that the faulty line is *uniquely* identified by one line end having an IJump condition due to ϵ_{up} and the other line end having an IJump condition due to ϵ_{down}. The CR diagnoses the line to be faulty if this is the case continuously for a period of t_{IJump}, this variable was not used in the references and it will be set to 4 ms. IJump scheme will also be delayed by communication, but compared to CCA, it will seldom have a delay of $t_{DR->CR,communication,max}$. Because in IJump, when the second signal arrives from the faulty line, it *permit* the trip rather than block. Therefore, IJump is a permissive scheme instead of a blocking scheme.

The design of the scheme is such that IJump is expected to be dependable (locates the fault) for radial conditions, while CCA is expected to be dependable for meshed conditions. For healthy lines, the current is equal at both ends, and no matter the operating conditions, neither IJump nor CCA should produce a trip. As a result, both schemes will always be on and running in parallel. Parallel operation is very advantageous compared to adaptive operation. Because if a meshed line trips and the network becomes radial, the network is instantly protected in parallel operation. Lastly, running IJump and CCA in parallel means that the term "meshed conditions" and "radial condition" is something only used when explaining the scheme. It does not need to be identified by the DSO.

As a foreshadowing of the results, IJump will often be dependable in meshed operation, contrary to expectations. In a few of the cases where IJump is dependable in meshed operation, CCA will be seen to not be dependable. Therefore, the strength of my proposal of running IJump and CCA in parallel is not only that they use the same quantity but also that it increases the number of faults identified in meshed conditions.

Step 2 of the CR. Find which CB to trip:

When the CR finds the faulty line, it will send GOOSE messages to CBs that will isolate the fault. The reader is advised to go back to Figure 3.2 and observe that, as proposed, there are fewer CBs than DRs. Implying that the amount of CBs is decoupled from the number of points with relays. If the DN grid of the future also changes dynamically, it means that the set of CBs that trips a specific line might change with time.

This problem was my motivation to move the tripping decision to a central relay. Because the CR is assumed to monitor the positions of all switches in the grid. Therefore it knows the current topology, which enables it to find the correct CB that selectively isolates a fault. An algorithm that finds the correct CB for a given fault was therefore invented and implemented. The algorithm is applicable for an arbitrary topology (with some limitations), and the interested reader can read about it in Section B.1.

3.2 Positive sequence phasor calculation

As the proposed trip algorithm needs the positive sequence current, it must be investigated how it should be calculated in the test bench.

Let $\mathbf{I_a}$, $\mathbf{I_b}$, $\mathbf{I_c}$ represent the three current phasors in a three-phase system and $i_a(t)$, $i_b(t)$ and $i_c(t)$ be their corresponding instantaneous values. Furthermore, let "a" be the complex operator that rotates a phasor 120° counter-clockwise without changing its magnitude ($a = 1\angle 120°$). Section 3.1 said that Equation 5 was the traditional method of phasor calculation, but in this thesis, the "instantaneous" method in Equation 6 is used for computational efficiency. Keep in mind that the time delay in i_b and i_c does not require extra storage as the DFT already stores samples from every 1 ms. However, the instantaneous method requires two linear interpolations based on the 1 ms values.

$$\mathbf{I_{PS}} = \frac{1}{3}(\mathbf{I_a} + a\mathbf{I_b} + a^2\mathbf{I_c}) \tag{5}$$

$$\mathbf{I'_{PS}} = \mathrm{DFT}[\frac{1}{3}(i_a(t) + i_b(t - \frac{2}{3}20\,\mathrm{ms}) + i_c(t - \frac{1}{3}20\,\mathrm{ms}))] \tag{6}$$

The differences in the methods occur between obtaining the sampled current and calculating the phasor. As seen in Figure 3.3 only the instantaneous method requires two interpolations on the stored SV values and then a sum of three real values to obtain the PS instantaneous current. In return, the traditional method has three DFTs instead of one. The traditional method also requires two complex products and a sum of three complex values.

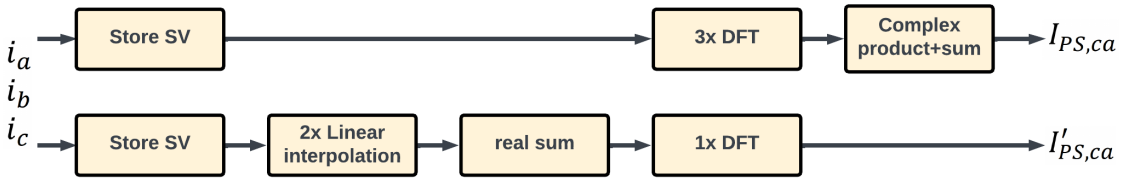


Figure 3.3: Algorithms in DR between receiving SV and obtaining the PS-phasor. The upper row is the traditional method, and the lower row is the instantaneous method.

This subsection will first explain the DFT algorithm and then its recursive implementation To avoid confusion, the frequency component the DFT filter tries to calculate is called f_{DFT}, the nominal power system frequency is f_n, the actual power system frequency is f_{act}, and the DFT sampling frequency is f_s.

3.2.1 Understanding frequency dependent DFT

The phasor representing the input signal of frequency f_{act} can be calculated using the DFT formula provided in [75], shown in Equation 7. The equations use the last N recorded samples referred to as $x_0, ..., x_{N-1}$. Furthermore, "j" is the complex operator, and "k" is a positive integer giving the frequency bin.

$$\mathbf{X_{f_{DFT}}} = \sum_{n=0}^{N-1} x_n e^{-j2\pi k \frac{n}{N}} \tag{7}$$

The frequency bin "k" specify which frequency component the DFT filter calculates:

$$f_{DFT} = k\frac{f_s}{N} \tag{8}$$

In the equation f_s is the sampling clock frequency of the DFT filter which is how many samples the DFT receives per second. In my implementation the currents are sampled every 1 ms meaning that the sampling clock frequency is 1000 Hz. To store the minimum amount of samples (N), Equation 8 yields that for f_{DFT} to be 50 Hz then $k = 1$ and $N = 20$.

If f_{act} deviates from f_{DFT}, say f_{act} is 50.1 Hz, the DFT will give a slight calculation error when estimating the phasor. The error is referred to as spectral leakage, and it increases with the greater deviation between f_{DFT} and f_{act}. Section 3.7.3 remarks that sudden islanding can cause great frequency deviation and, thereby, great spectral leakage. A remedy is that instead of using f_{DFT} equal to f_n, one could rather change N dynamically so f_{DFT} tries to achieve the value of f_{act}.

To demonstrate how to change the N value dynamically, understand that if $k = 1$, $N = 19$ and $f_s = 1000$ Hz then Equation 8 yields $f_{DFT} = 52.63$ Hz. Therefore, if N is decreased by one to 19 and $f_{act} = 52.63$ Hz, there is no spectral leakage. Consequently, to minimize spectral leakage, the approach is if the frequency rises above the midpoint of 50 Hz and 52.63 Hz, then change N from 20 to 19.

Table 3.1 generalize the approach, where the second column gives the frequency band for a given "N" value and the third column gives the frequency with no leakage. The approach requires the buffer of stored samples to always be greater than any expected N value. In the method, the R-PI will use Table 3.1. In the results, some simulations will be conducted at a system frequency of 57.2 Hz. Because, in the range [40 Hz, 60 Hz] it is the frequency furthest away from a frequency with no leakage. Lastly, the reader might think that specifying 60 Hz is ridiculous for a 50 Hz system. However, in the event of sudden islanding Section 3.7.3 explains why it is not ridiculous.

Table 3.1: The table used to choose "N" for the DFT filter. Based on expected frequency deviations a limited number of N values are shown.

N	f_{act} **For N Value** [Hz]	**Frequency With No leakage,** f_{DFT} [Hz]
25	[39.2, 40.8)	40
24	[40.8, 42.6)	41.67
23	[42.6, 44.5)	43.5
22	[44.5, 46.6)	45.5
21	[46.5, 48.8)	47.6
20	[48.8, 51.3)	50
19	[51.3, 54.09)	52.6
18	[54.09, 57.19)	55.6
17	[57.19, 60.65)	58.8

3.2.2 Recursive implementation of the DFT

As the DR estimates the phasor for each new sample a recursive implementation of Equation 7 every 1 ms, instead of applying Equation 7 every 1 ms, is more computationally efficient. This is because even though the recursive approach gives the same output it does not iterate over all the N last samples. A recursive DFT only utilizes the most recent sample (x_n), the sample from N samples ago (x_{n-N}), and the current value of the phasor X_{n-1}. Various recursive DFTs exist. Some approaches will have a phasor that rotates one time per cycle (does not affect CCA or IJump) [76]. However, a constant angle under balanced condition facilitate an easier post-fault analysis. Therefore the DFT of [77], reproduced in Equation 9, will be used.

$$X_{f_{DFT},n} = X_{n-1} + \frac{2}{N} e^{-j2\pi \frac{n}{N}} (x_n - x_{n-N}) \tag{9}$$

3.3 Simple frequency estimation

The objective now is to give an approach to estimate the frequency. The frequency estimate will influence the ”N” used in Equation 9. As the frequency bands in Table 3.1 are a few Hz wide, only a low precision estimate is needed.

A simple way to estimate the frequency is to measure the time between consecutive zero crossings. As stated by [78], voltage measurements are typically used for frequency detection. One of the reasons for not using the current measurement is when there is a short-circuit, and there is a sudden change in the current direction, a current zero (CZ) can be skipped. Nevertheless, the current will be used in my application as the DRs only have current measurements, and only a crude frequency estimation is needed.

The first step in the frequency estimation is to pass the most recent sampled value i_n through a low pass (LP) filter. The LP filters out the noise to avoid false zero crossings. The implemented LP filter will be a single-pole infinite impulse response filter which, according to [79], has the following function:

$$x_n = x_{n-1} + \alpha(i_n - x_{n-1}) \tag{10}$$

x_n is the filtered current at the current sample. α is a filter constant. As α is reduced from the max value of 1, the cut of frequency reduces.

After signal filtering, the next step is to check if there has been a CZ between time step ”n” and ”n-1”. In other terms check if the following logical statement returns true:

$$(x_{n-1} \geq 0 \quad AND \quad x_n < 0) \qquad OR \qquad (x_{n-1} \leq 0 \quad AND \quad x_n > 0) \tag{11}$$

If the statement is true a linear interpolation is done to estimate when the CZ was between the two samples:

$$t_{CZ} = t_{n-1} + \frac{x_{n-1}}{x_{n-1} - x_n} 1\,\text{ms} \tag{12}$$

In the equation 1 ms is used because it is the time between two samples. The frequency estimate is then obtained every fourth CZ by using the fact that there are two fundamental periods every fourth CZ:

$$f_{current-estimate} = \frac{2}{t_{CZ-now} - t_{CZ-4-times-ago}} \tag{13}$$

For reasons that will soon become clear, $f_{current-estimate}$ is not used as the final estimation. Rather the median of the three last frequency estimations is used.

To test the frequency estimator, a series of samples were fed offline to the implemented estimator. The set of samples corresponds to a worst-case scenario where the current suddenly changes direction (due to a fault), and at the same time, the frequency *unrealistically* jumps from 50 Hz to 52 Hz. These samples were fed offline to the estimator, and the results are shown in Figure 3.4.

In Figure 3.4, the blue is the input signal while the black line is the filtered and sampled response. The yellow dots show the recorded CZ every fourth time. The number on the bottom shows the most recent frequency estimate, and the number on the top shows the median of the last three frequency estimates. Observe that the median is needed, as when the CZ is skipped the frequency estimate right after fault goes down to 44.9 Hz. The 100 ms it takes after a fault to arrive at a correct estimate is of little problem. Because the islanded grid will have some inertia meaning that the frequency changes gradually, not instantaneously as in the example. The noise due to simulated measurement inaccuracy, caused the estimate to be off by 0.2 Hz. For a generator governor, 0.2 Hz deviation would render the estimate useless. However, in my application,

this is no problem as 0.2 Hz deviation produces minimal spectral leakage.

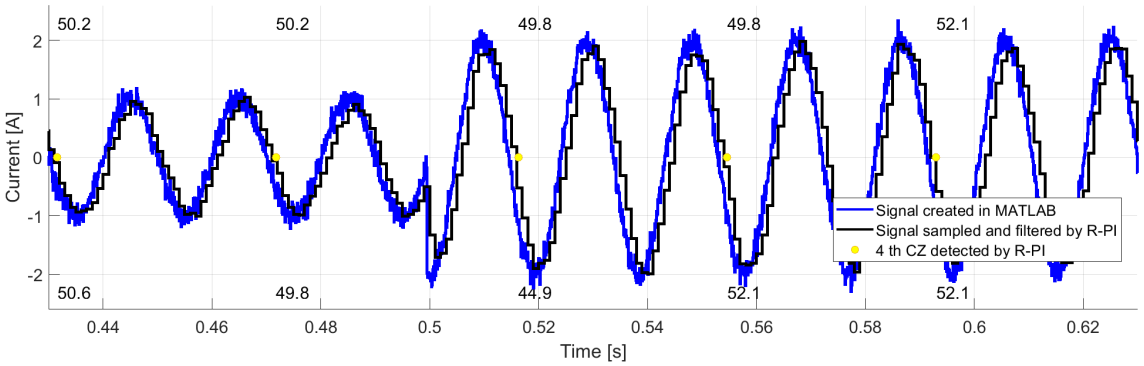


Figure 3.4: Performance evaluation of the frequency estimator. Values in the lower part of each figure are the frequency based on the last two cycles. The upper value is the median of the three last estimates which is used as the final estimate. Signal to Noise Ratio = 20 dB

3.4 Equations for comparing positive sequence phasors using traditional and instantaneous methods

Before introducing the test bench, it must be verified that the instantaneous method of phasor calculation can work. Therefore, the objective of this chapter is to develop and compare equations that express $\mathbf{I_{PS}}$ and I'_{PS} as a function of the ideal phase phasors. The calculations for the instantaneous method ($\mathbf{I'_{PS}}$) were not found in the literature and therefore had to be derived, which was not the case for $\mathbf{I_{PS}}$.

3.4.1 Instantaneous vs. Traditional Method of PS phasor calculation at Steady State Ignoring Spectral Leakage

First, remember the definition of the instantaneous method in Equation 6:

$$\mathbf{I'_{PS}} = \mathrm{DFT}[\frac{1}{3}(i_a(t) + i_b(t - \frac{2}{3}20\,\mathrm{ms}) + i_c(t - \frac{1}{3}20\,\mathrm{ms}))] \tag{14}$$

[80, p. 61] states that the DFT is a linear transformation, which results in:

$$3\mathbf{I'_{PS}} = \mathrm{DFT}\{i_a(t)\} + \mathrm{DFT}\{i_b(t - \frac{2}{3}20\,\mathrm{ms})\} + \mathrm{DFT}\{i_c(t - \frac{1}{3}20\,\mathrm{ms})\} \tag{15}$$

In steady state, [80, p. 64] specify that DFT has the following property called ”time shifting”/”circular shift of a time sequence”:

$$\mathrm{DFT}\{i(t - t_{delay})\} = e^{-j(2\pi)(f_{DFT}+\Delta f)t_{delay}}\mathrm{DFT}\{i(t)\} \tag{16}$$

Now assume that the time domain currents are pure sinusoids and have a frequency deviation of Δf relative to f_{DFT}. Also, assume that the grid is in a steady state operation. The steady-state operation can be an unbalanced steady state post-fault. Applying the time shift theorem to Equation 15 and assuming $f_{DFT} = 50\,\mathrm{Hz}$ for explanatory purposes:

$$3\mathbf{I'_{PS}} = \mathrm{DFT}\{i_a(t)\} + e^{j120^\circ}e^{-j2\pi\Delta f\frac{2}{3}20\,\mathrm{ms}}\mathrm{DFT}\{i_b(t)\} + e^{-j120^\circ}e^{-j2\pi\Delta f\frac{1}{3}20\,\mathrm{ms}}\mathrm{DFT}\{i_c(t)\} \tag{17}$$

Now use that $a = e^{j120^\circ}$ and calculate the values in the complex exponential:

$$3\mathbf{I}'_{\mathbf{PS}} = \mathrm{DFT}\{i_a(t)\} + ae^{-j4.8^\circ\Delta f}\mathrm{DFT}\{i_b(t)\} + a^2e^{-j2.4^\circ\Delta f}\mathrm{DFT}\{i_c(t)\} \tag{18}$$

Neglecting the effect of spectral leakage results in (this point will become important later):

$$3\mathbf{I}'_{\mathbf{PS}} = \mathbf{I_a} + ae^{-j4.8^\circ\Delta f}\mathbf{I_b} + a^2e^{-j2.4^\circ\Delta f}\mathbf{I_c} \tag{19}$$

Comparing Equation 19 with Equation 5 it is evident as long as there is steady state operation at $f_{DFT} = f_{act}$ then $\mathbf{I}'_{\mathbf{PS}} = \mathbf{I_{PS}}$. However, when the power system frequency deviates from the DFT frequency then $\mathbf{I}'_{\mathbf{PS}} \neq \mathbf{I_{PS}}$. The deviation is due to the extra -4.8° and -2.4° extra rotation of the b and c phase phasor per 1 Hz deviation.

3.4.2 Instantaneous vs. Traditional Method of PS phasor calculation at Steady State with Spectral Leakage

So far, the effect of spectral leakage has not been taken into account. As spectral leakage causes a calculated phasor error when $f_{DFT} \neq f_{act}$, the correct way to express Equation 19 is to express that the phase phasors are calculated (”ca”) phasors.

$$3\mathbf{I}'_{\mathbf{PS,ca}} = \mathbf{I_{a,ca}} + ae^{-j4.8^\circ\Delta f}\mathbf{I_{b,ca}} + a^2e^{-j2.4^\circ\Delta f}\mathbf{I_{c,ca}} \tag{20}$$

The goal now is to understand how spectral leakage works so that the calculated phasors can be expressed as a function of the actual ideal phasors. In [77] a general formula is given which expresses the calculated phasor $\mathbf{I_{ca}}$ as a function of the actual phasor ($\mathbf{I}$) and four variables:

$$\mathbf{I_{ca}} = b_1e^{j\alpha_1}\mathbf{I} + b_2e^{j\alpha_2}\mathbf{I}^* \tag{21}$$

$$b_1 = \frac{\sin\frac{\pi\Delta f}{f_d}}{N\sin\frac{\pi\Delta f}{Nf_d}}e^{j\frac{\pi(N+1)\Delta f}{Nf_d}} \tag{22}$$

$$\alpha_1 = n\frac{2\pi\Delta f}{f_dN} \tag{23}$$

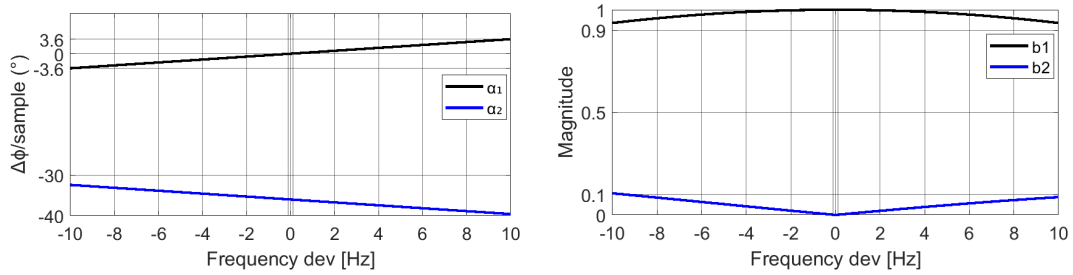
$$b_2 = \frac{\sin\frac{\pi\Delta f}{f_d}}{N\sin(\frac{\pi\Delta f}{f_dN} + \frac{2\pi}{N})}e^{-j\frac{\pi(N+1)\Delta f}{Nf_d}} \tag{24}$$

$$\alpha_2 = -n * (\frac{2\pi\Delta f}{f_dN} + \frac{4\pi}{N}) \tag{25}$$

Observe that of the four variables in Equation 21 only α_1 and α_2 are time-dependent as they are functions of sample ”n”. Furthermore, observe that α_1 and α_2 are only in the complex exponential meaning that they only cause a rotation of $\mathbf{I}$ and $\mathbf{I}^*$, respectively. By setting α_1 and α_2 equal to 2π it can be found that α_1 cause a clockwise rotation with a frequency of Δf. α_2 cause a anti-clockwise rotation with a frequency of $2f_n + \Delta f$. In Figure 3.5a, the amount of rotation per new sample caused by the two constant are shown as a function of the frequency when $N = 20$.

On the other hand, b_1 and b_2 are time-independent at a given frequency deviation. As seen in Figure 3.5b, with greater frequency deviation b_1 decreases, the impact of the actual phasor $\mathbf{I}$ on the calculated. b_2 increases the impact of the actual complex conjugate I^* on the calculated phasor.

When the power system frequency is near f_{DFT} say 1 Hz deviation then the figure shows that $b_1 \approx 1$ and $b_2 \approx 0$ meaning that $\mathbf{I_{a,ca}} \approx e^{j\alpha_1}\mathbf{I}$. Then the effect of spectral leakage would only be a calculated rotation of 7.2° rotation per cycle. If the deviation was just 0.1 Hz, which the Nordics TSO does not want to exceed



(a) Phase shift per sample due to α_1 and α_2

(b) Magnitude of b_1 and b_2

Figure 3.5: Value of constants used to calculate spectral leakage. Calculations are done assuming N=20

[81], then the effect would only be 0.72° rotation per cycle. Clearly, the effect of spectral leakage is only there for very great frequency deviations such as 5 Hz.

Now the impact of spectral leakage is understood and the goal is to find $\mathbf{I_{PS,ca}}$ and $\mathbf{I'_{PS,ca}}$ as a function of the ideal phasors. In [82] this was done and for $\mathbf{I_{PS,ca}}$. They found that the calculated PS phasor is a function of the ideal positive sequence phasor, the ideal negative sequence phasor, and the four defined constants.

$$\mathbf{I_{PS,ca}} = b_1 e^{j\alpha_1}\mathbf{I_{PS}} + b_2 e^{j\alpha_2}\mathbf{I^*_{NS}} \tag{26}$$

A similar expression was not found for $\mathbf{I'_{PS,ca}}$, and it is therefore derived by adopting the approach in [82]. Continue with Equation 20, and express the three calculated phase phasors using Equation 21.

$$\begin{aligned} 3\mathbf{I'_{PS,ca}} &= b_1 e^{j\alpha_1}\mathbf{I_a} + b_2 e^{j\alpha_1}\mathbf{I_a}^* \\ &+ a e^{-j4.8°\Delta f}(b_1 e^{j\alpha_1}\mathbf{I_b} + b_2 e^{j\alpha_1}\mathbf{I_b}^*) \\ &+ a^2 e^{-j2.4°\Delta f}(b_1 e^{j\alpha_1}\mathbf{I_c} + b_2 e^{j\alpha_1}\mathbf{I_c}^*) \end{aligned} \tag{27}$$

Now reorder the elements of Equation 27:

$$\begin{aligned} 3\mathbf{I'_{PS,ca}} &= b_1 e^{j\alpha_1}(\mathbf{I_a} + a e^{-j4.8°\Delta f}\mathbf{I_b} + a^2 e^{-j2.4°\Delta f}\mathbf{I_c}) \\ &+ b_2 e^{j\alpha_2}(\mathbf{I_a}^* + a e^{-j4.8°\Delta f}\mathbf{I_b}^* + a^2 e^{-j2.4°\Delta f}\mathbf{I_c}^*) \end{aligned} \tag{28}$$

Take the complex conjugate out of the last parenthesis in Equation 28:

$$\begin{aligned} 3\mathbf{I'_{PS,ca}} &= b_1 e^{j\alpha_1}(\mathbf{I_a} + a e^{-j4.8°\Delta f}\mathbf{I_b} + a^2 e^{-j2.4°\Delta f}\mathbf{I_c}) \\ &+ b_2 e^{j\alpha_2}(\mathbf{I_a} + a^2 e^{j4.8°\Delta f}\mathbf{I_b} + a e^{j2.4°\Delta f}\mathbf{I_c})^* \end{aligned} \tag{29}$$

The goal has now been achieved as Equation 26 and Equation 29 express $\mathbf{I_{PS,ca}}$ and $\mathbf{I'_{PS,ca}}$ as a function of the ideal phase phasors. Observe that the only difference is that the instantaneous method has four additional complex exponentials that contain $2.4°\Delta f$ and $4.8°\Delta f$. Meaning that as long as there is not a large deviation between f_{DFT} and f_{act}, the steady-state response (also unbalanced steady state) is similar, and the response is equal when there is no frequency deviation. Nevertheless, with increasing deviation, the two methods give more dissimilar results.

By expressing Equation 29 with an approximate NS and PS current, the next paragraphs will explain the dissimilarity in the calculated phasors at an off-nominal frequency.

$$\mathbf{I'_{PS,ca}} = b_1 e^{j\alpha_1}\mathbf{I_{\approx PS}} + b_2 e^{j\alpha_2}\mathbf{I^*_{\approx NS}} \tag{30}$$

3.4.3 Understanding the difference between the traditional and instantaneous method at steady state

Figure 3.6 are used to explain the behavior of $\mathbf{I}'_{\mathbf{PS,ca}}$ when the power system frequency does not equal the DFT frequency. The sum of the blue and red arrows is the calculated phasor. The blue arrow in the figure corresponds to the blue part in Equation 30. Therefore the blue arrow represents the approximated PS phasor. Due to α_1, it rotates anti-clockwise with a frequency of Δf. With a larger frequency deviation, it is scaled down to b_1. The red arrow in the figure corresponds to the red part in Equation 30. Therefore the red arrow represents the conjugate of the approximated NS phasor. Due to α_2, it rotates clockwise with a frequency of $2f_n + \Delta f$. With a larger frequency deviation, it has more impact as the b_2 value increases from zero.

With respect to the blue arrow, the red arrow rotates anti-clockwise at a frequency of $2f_n + 2\Delta f$. Therefore the NS current causes oscillations in the calculated angle and magnitude at the inter harmonic frequency of $2f_n + 2\Delta f$. The oscillations are worse for the instantaneous method. Because even though it is a balanced state, the approximated NS component will not be zero when there is a frequency deviation.

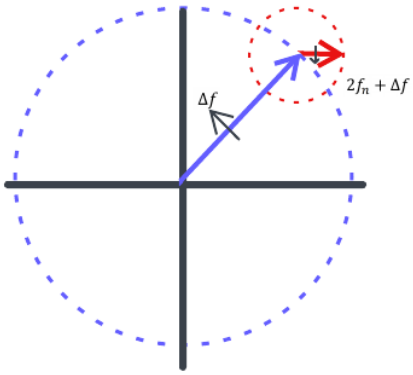
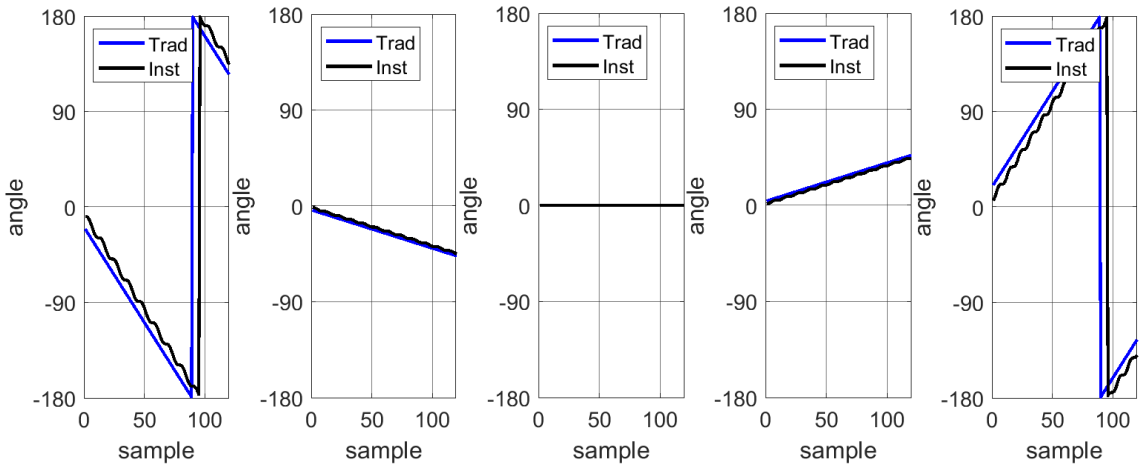


Figure 3.6: Phasor plot used to visualize $\mathbf{I}'_{\mathbf{PS,ca}} = b_1 e^{j\alpha_1}\mathbf{I}_{\approx\mathbf{PS}} + b_2 e^{j\alpha_2}\mathbf{I}^*_{\approx\mathbf{NS}}$.

Referenced Equation 26 and derived Equation 29, show the equation for the traditional and instantaneous method as a function of ideal phase phasors. Figure 3.7 and Figure 3.8, plots the angle and magnitude output of the equation with three unity balanced phasors as input. The goal is to confirm the explanation above.

Figure 3.7 shows PS current angle as a function of sample number ”n”. As expected from theory, when the frequency of the power system equals that of the DFT filter, the angle is constant in both methods. When the power system frequency deviates from the DFT filter, the impact of α_1 is the constant rotation, while α_2 causes oscillations. Oscillations are only seen in the instantaneous method as the input was a balanced set of phasors.

In Figure 3.8, the upper surface is the PS current magnitude of the traditional method, while the lower is that of the instantaneous method. With greater deviation, both methods show a large steady-state deviation from unity. This is due to b_1. and it does not have an impact on $IJump$. This offset is different in the methods due to the instantaneous method using $I_{\approx PS}$, not I_{PS}. For IJump, the trouble is the inter harmonic calculated oscillations seen on the lower surface.



(a) 45 Hz **(b)** 49 Hz **(c)** 50 Hz **(d)** 51 Hz **(e)** 55 Hz

Figure 3.7: The effect of spectral leakage on the PS-angle when with no frequency estimation. Balanced three-phase input signal at different frequencies. The calculated angle is a function of a sample (N=20).

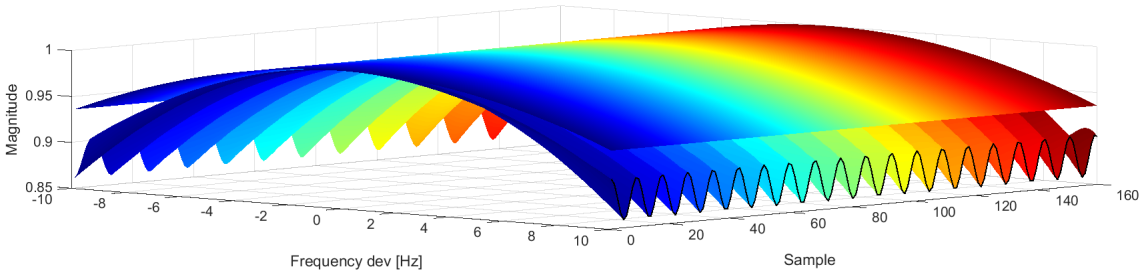


Figure 3.8: The effect of spectral leakage on the PS-magnitude with no frequency estimation. Magnitude in the traditional method (upper surface) and instantaneous method (lower surface). Input is three phase symmetrical signal at different frequencies (N=20).

It should be remarked that the oscillations impact CCA and IJump as $2f_n + 2\Delta f$ is an inter harmonic frequency. Therefore, the phase on the oscillations one cycle ago at the DFT filter frequency is not the current phase. In Figure 3.9 this is illustrated by showing the location on the phase 20 ms ago as a function of the power system frequency, when the DFT frequency is constant 50 Hz. Observe how as the frequency deviation increases, the phase 20 ms becomes more unfavorable. With crude frequency estimation, the phase now and one cycle ago becomes similar.

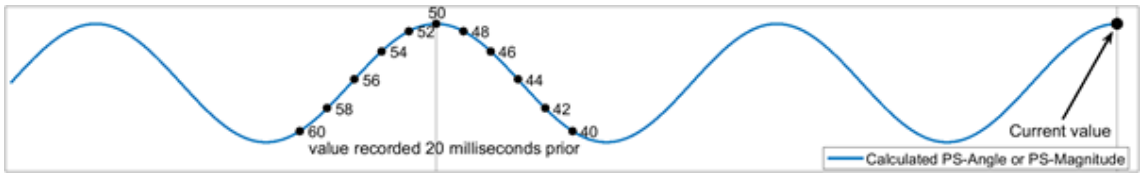


Figure 3.9: Current phase of the inter harmonic introduced by spectral leakage, and the phase a cycle ago. Values in the plot are the power system frequency. No frequency estimation.

3.5 Communication using IEC61850

The test bench uses ICD files, GOOSE communication, and SV communication, and these topics are now explained. IEC61850 specify how GOOSE and SV communication should occur. The standard also defines the ”device model” which is a way to describe a substation, including the communication network, in an object-oriented way.

3.5.1 The device model

The left side of Figure 3.10 shows the name of the hierarchy stages of the device model with the right showing CB as an example. As shown in the figure the uppermost layer is the network address, which corresponds to one or possibly several logical devices (LD) [5]. An LD can for example be an IED, CB, or a Merging unit, it must have a unique name. In Figure 3.10 the example is a CB with the name CB_1.

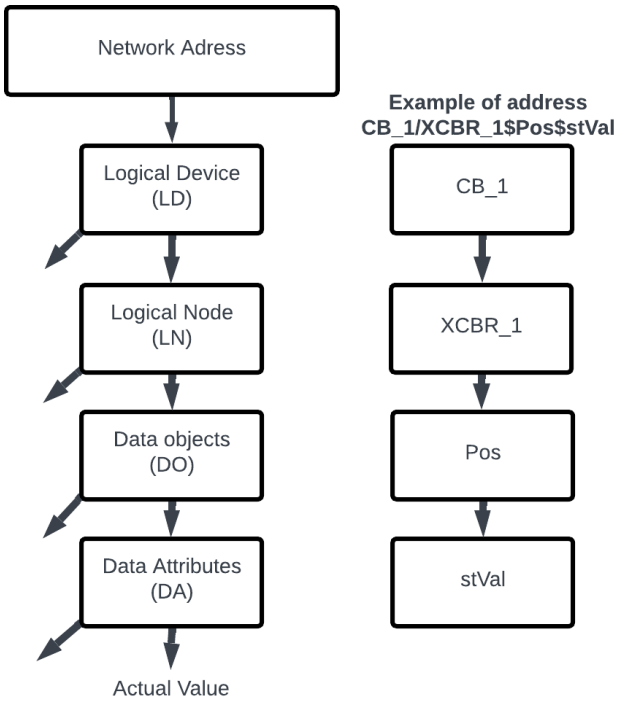


Figure 3.10: The device model in IEC61850. Arrows to the left indicate that there can be several of the type to the right.

Each logical device can have several logical nodes (LN). The LN is standardized in IEC61850-5 and divided into groups based on their function. The groups are identified by their first letter. For example, protection is identified by ”P” and switch gear is identified by ”X” (table 7 in IEC61850-7-1). Two examples of LN are PDIS for distance protection and XCBR for a circuit breaker. In the figure, XCBR is shown with a _1 to give it a name.

Going further down in the hierarchy, each LN will have several data objects (DO). The data objects, which are standardized, are divided into seven groups and can all be found in IEC61850-7-4. For example, the data object pos describe the position of the CB.

The last step in the hierarchy is the data attributes (DA) which correspond to a DO. As with the other steps for each DO, there can be several DAs. For example, is that the DO ”pos” can have stVal as DA. During operation, the value assigned to stVal gives the current CB status.

The important takeaway is that there is a unique address describing the position of the CB. This address can have a value say either ”1” or ”0” describing the state of the CB. Similarly, in the method, the DR will have an address that has the value ”1” or ”0” depending on if it is a CCA condition or not. The value will be monitored, and if it changes a GOOSE message is automatically published. Therefore the ICD file not only gives an address to a value, but it also specifies that when this value changes a GOOSE message shall be published.

3.5.2 Implementing the device modeling in ICD files

In the preceding section, the structure of an LD was presented. IEC61850-6 then present several files on how this information can be stored and combined with the communication solution for the particular substation(s). The standard specifies several file formats called SSD, ICD, IID, SCD, and CID which are all written in the System Configuration Description Language (SCL). A full description of all files can be found in chapter 7 of IEC 61850-6. However, the reader ought to understand that it is possible to only use ICD files when setting up a simple IEC61850 communication system. The method chapter will explain the ICD files used.

3.5.3 GOOSE and SV communication protocols in IEC61850

In the thesis, GOOSE and SV are used for the three steps requiring communication. The first is SV of the current between the CT and DR placed near one another. The second is long-distance GOOSE communication between CR and DR. The third is long-distance GOOSE communication between CR and breaker IED. The next paragraph will explain the particularities of SV and GOOSE communication.

IEC61850-8-1 GOOSE (Generic Object Oriented Substation Event) is typically used for communicating trip signals between protection IEDs or between protection IEDs and breaker IEDs. IEC61850-9-2 SV (Sampled Values) are used to communicate digitized current/voltage measurements at a high sample rate, typically between MU and protection IED. Compared to client/server-based communication, both GOOSE and SV use the publisher/subscriber type of communication.

A publish/subscriber type of communication means that when the packet is published on the Local Area Network (LAN), the packets will go to all devices on the LAN. However, only the pre-configured subscribers will process the information. Furthermore, the recipients of the information will send no acknowledgment that they have received the information. Therefore, after a GOOSE message with new information is published, it will be continuously re-broadcast with decaying frequency [83].

GOOSE and SV map directly to the ethernet layer in the OSI model enabling fast communication [5]. In a public mobile network, the GOOSE packets communicated would also need a layer for routing the packet on the network and for cyber-security. In the research done by [70] this caused an additional delay of 4.4 ms-7.2 ms. The variation in delay was due to different security protocols.

3.6 Measurement accuracy of Current Transformers

To achieve the objective of building a test bench, it must be known that the proposed settings of ϕ_{CCA}, ϵ_{down} and ϵ_{up} can work. In order to do this, the maximum expected error introduced by the CT must be evaluated. To evaluate the maximum error, this subsection looks into: CT-rating, standardized error definitions, and errors when measuring short circuit faults. This section concludes that CT error is not expected to cause problems. Therefore CT error will not be included in the test bench.

3.6.1 Explaining the ratings of a CT

"5P30 300/1 30 VA" is an example of a CT rating. "30 VA" refers to the rated burden, "300/1" refers to the rated primary and secondary current (max load current), and in "5P30" the "5P" classify it as a Protection core with a maximum of 5% composite error while "30" is the Accuracy Limit Factor (ALF). The composite error rating should be satisfied at rated burden for a primary current equal to the "rated accuracy limit primary current". The "rated accuracy limit primary current" is the current which is the product of the rated primary load current and ALF (300*30).

3.6.2 Standardized measurement error

As a result of measurement errors, even if the physical current at the start and end of the line is exactly equal the current measured might be different. This is why IEC 61869-1 and IEC 61869-6 define errors called Phase error (ϕ_e), Ratio error (ϵ), and Composite error (ϵ_r) [84, 85].

To explain the errors let $\mathbf{I_p}$ be the primary current-phasor, $\mathbf{I_s}$ be the current-phasor into the burden (what is measured), and $\mathbf{I_0}$ be the magnetization current-phasor referred to the secondary. Lastly, let " ' " indicate that the value referred to the primary side by using the ideal turns ratio. Then:

$$\mathbf{I_p} = \mathbf{I_s'} + \mathbf{I_0'} \tag{31}$$

In the standards, the phase error, also called the displacement error, is the angle between $\mathbf{I_p}$ and $\mathbf{I_s'}$:

$$\phi_e = \angle\mathbf{I_p} - \angle\mathbf{I_s'} \tag{32}$$

The ratio error can be interpreted as the percentage difference between the measured RMS value and the actual RMS value, i.e.

$$\epsilon(\%) = (\frac{I_s'}{I_p} - 1) * 100 \tag{33}$$

Lastly, Equation 34 gives the composite error which is the RMS of the difference between the primary and secondary current (referred to the primary) divided by the primary RMS current. Keep in mind that both a phase and ratio error will cause a composite error.

$$\epsilon_r(\%) = \frac{1}{I_p}\sqrt{\frac{1}{T}\int_0^T (i_s'(t) - i_p(t))^2} * 100 \tag{34}$$

Based on IEC 61869-2 and IEC 61869-10, Table 3.2 gives the limits for phase error, ratio error, and composite error for conventional CT and LPCT. The limits are given for protection classes 5P and 10P. Observe that the ratio error and phase error are given at the rated load current. For the relay setting, the errors are at the maximum possible short circuit currents are needed.

Table 3.2: Limits on errors for protection class 5P and 10P for conventional CT and LPCT. For class 10P no explicit phase error is defined. Values are taken from IEC 61869-2 and IEC 61869-10 [86, 87].

Class	Ratio error at rated primary current	Phase error at rated primary current	Composite error at rated accuracy limit primary current
5P	±1%	±1°	±5%
10P	±3%		±10%

3.6.3 Finding maximum phase and ratio error at maximum short circuit current

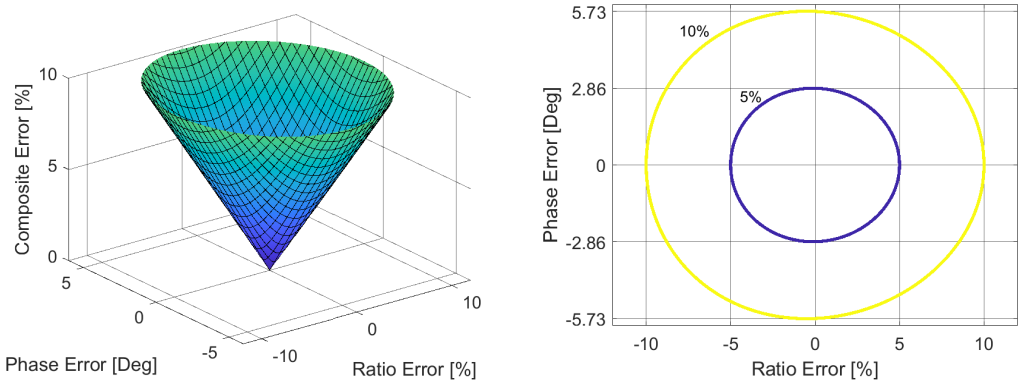
To evaluate the ratio error and phase error at maximum short circuit current I have done a simple estimation. First assume the measured current to be a sinusoidal value at the fundamental frequency;

$$i_p(t) = \sqrt{2} I_p \sin \omega t \tag{35}$$

Assuming the CT is operating in the linear domain, then the magnetization current does not cause harmonics. Then Equation 36 can be used to express the secondary current as a function of phase and ratio error.

$$i_s'(t) = (\frac{\epsilon(\%)}{100} + 1)\sqrt{2} I_p \sin \omega (t - \frac{\phi_e}{360} T) \tag{36}$$

Now use the expression for $i_p(t)$ and $i_s'(t)$ in Equation 34 to obtain the composite error as a function of the phase error and ratio error. The results are shown in Figure 3.11a. As expected, when the phase or ratio error deviates more from zero it causes an increase in the composite error. Figure 3.11b is a contour plot of Figure 3.11a where the solid lines say which combination of phase error and ratio error gives 5% and 10% composite error. From the contour plot one can observe that for 5P and 10P the maximum ratio error is ±5% and ±10%, respectively and the maximum phase error is ±2.86° and ±5.73°, respectively. The



(a) Surface plot

(b) Contour Plot for 5% and 10% composite error

Figure 3.11: Approximation for composite Error as a function of phase error and ratio error. Assuming both the primary and secondary CT current to be a perfect sinusoid. My own derivation.

maximum phase error occurs when the ratio error is zero and vice versa. However, the ratio and phase error is caused by many of the same effects, such as magnetization current [5]. Accordingly, it will not occur that only one of the errors is zero. Additionally, it is expected that the phase error is low [5]. Thus what I have obtained is an estimate of the *theoretic* upper limit of errors which I can use to justify the relay settings.

3.6.4 Consequences for the relay settings

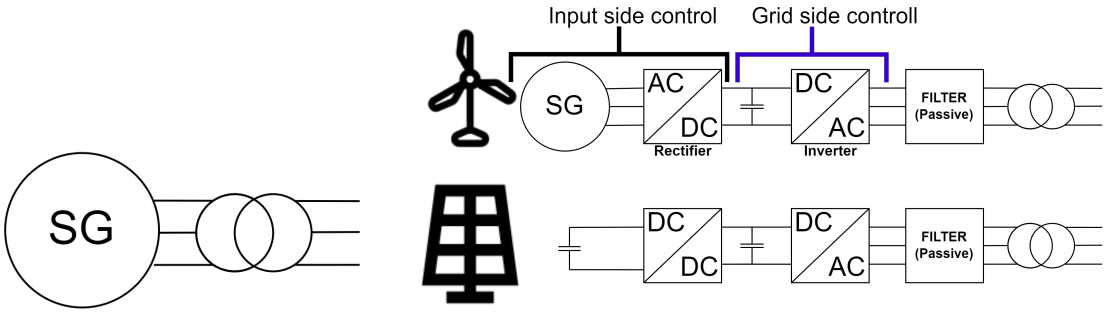
It has been said that in the evaluation phase, the main settings of the relays are ϕ_{CCA}, ϵ_{up} and ϵ_{down}, They have the values of 90°, 1.1 and 0.9, respectively. During steady-state operation, the error is expected to be constant and therefore does not impact the CCA-angle or IJump-magnitude.

However, if the fault current is very high, the error can increase. Then the difference in error pre and post-fault will cause a false CCA-angle/IJump-magnitude. Nevertheless, the errors at max short circuit current are small. Additionally, the simulation results will demonstrate at a large short circuit current, the IJump-magnitude deviates most from unity, and the CCA-angle with CCA-conditions is closest to 180°. CT errors are therefore expected to not cause issues and are therefore not included in the test bench.

3.7 Distributed Generation control and low voltage ride through

The objective of this section is to find out what requirements the implemented DG on the test bench must satisfy. Section 3.7.1 will highlight that compared to Synchronous Generator Distributed Generation (SGDG), the Inverter Interfaced Distributed Generator (IIDG) control system must be modeled in detail. Section 3.7.2 explains that LVRT considerations for DG are relevant. Section 3.7.3 shows through actual grid measurement that the test bench must take into account large frequency deviations.

Figure 3.12 is taken from the project report, where it was used to explain the difference between IIDG and SGDG. As can be seen in Figure 3.12a, SGDG has the terminals of the generator connected to the grid. As depicted in Figure 3.12b, an inverter between the electrical-power generator and the grid. A typical example of an SGDG is small-scale hydro-power, while IIDG can be solar-power or type four wind turbines.



(a) SG interfaced (SGDG)

(b) Inverter interfaced (IIDG)

Figure 3.12: Shows inverter interfaced and non-inverter interfaced DG. Taken from project report [1].

3.7.1 IIDG control system must be included in the test bench

The SGDG response right after fault is dominated by the physical characteristic of the generator, not its control system characteristic [88, 89]. Thus, in the simulations, the reference value fed to the governor and Automatic Voltage Generator can be kept constant.

The IIDG response right after fault is dominated by the Grid Side Controller, which controls the inverter [88]. Hence for an IIDG, it is the action of the control system that dominates its fault contribution. In the project report, it was stated that the IIDG controller results in a very quick response, low fault current contribution, and some control schemes will contribute with nearly balanced currents for unbalanced faults [1].

In Figure 3.13, the fast IIDG response is exemplified by showing the line current for a real-life terminal short circuit test on a 1 MW inverter done by National Renewable Energy Laboratory [90]. Observe how after fault, the current quickly reaches a new steady state where the current is capped at 1.2 pu. Clearly, to properly evaluate the proposed algorithm the testbench must include an IIDG control system capable of operating in grid-connected and islanded mode. But as specified in the project report [1], the slow-acting input side control, shown in Figure 3.12b, can be modeled through a stiff DC-voltage.

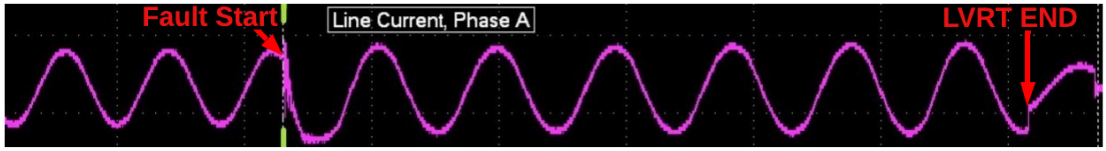


Figure 3.13: 1 MW Inverter fault current recorded during real-life terminal short circuit. Done by the National Renewable Energy Laboratory. The figure is taken from [90], red text was added by me.

The grid side control of the inverter is typically classified as either grid-forming or grid-following [91]. Grid-forming schemes try to control the system frequency and the voltage at the PCC. If the grid is operating in islanded mode, with only inverter-interfaced resources, at least one of them must be using a grid-forming scheme. Two examples of grid-forming schemes are V/f control and droop control. In Grid-Following schemes, the inverter does not try to control the voltage or the frequency but rather uses them to achieve their own controller objectives. Typical grid-following schemes are PQ control or constant current control. In PQ control, the controller tries to achieve a given power setpoint.

In the simulations presented in this thesis, PQ-control will be used in the grid-connected operation while V/f control will be used in the islanded operation. In the method Section 4.3, the theory and implementation of the controller are given.

3.7.2 Low Voltage Ride Through requirements are relevant for DG

In 2019 EU-wide regulation caused the Norwegian Grid Code to add LVRT requirement for DGs. The requirements are based on the rated power output for all units connected to a grid voltage of 110 kV or less [92]. Meaning that when it comes to LVRT for units connected to a grid of less than 110 kV, the requirement is only dependent on the power rating. The requirement does not depend on if the unit is connected to the regional or distribution grid.

For power stations connected to a network of less than 110 kV the Norwegian grid code now says that units larger than 1.5 MW are required to have Low Voltage Ride Trough (LVRT) capability [92, 93]. The specific LVRT requirements of both IIDG and SGDG are given in Figure 3.14. Observe that for the same per-unit voltage at the point of common coupling, an IIDG is required to stay synchronized for a longer time compared to the SGDG. Also, observe that if the protection system shall not impede on LVRT capability it must be the case that the fault is isolated and the voltage is recovered before 150 ms after the fault.

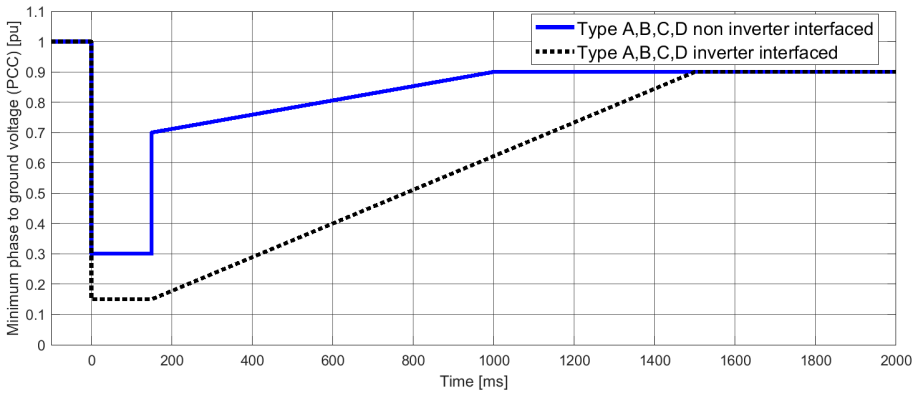


Figure 3.14: Norwegian LVRT requirement at $\leq$ 110 kV for type B,C,D, a recommendation for type A. Values not seen on the axis is 0.15 pu, 150 ms and 1500 ms. The plot was created by me in the project report with values from [93].

DG units greater than 0.8 MW, but less than 1.5 MW are not required to have LVRT according to the Norwegian Grid Code. However, for those units, the grid code recommends following IEC recommendations [93]. IEC NEK EN 50549-2019 says they ”should”, but not ”shall” have LVRT capability [94]. The reason for using ”should” instead of ”shall” is that requiring it could cause a legal issue with the EU-Law (RFG-NC) [1, 94].

Until now the LVRT requirement has only been valid for three-phase faults. For unbalanced faults, the Grid code remarked LVRT capability should not be purposefully limited. However, the draft for the 2023 version

specifies that the requirements shall be valid for both symmetric and unsymmetrical faults [95].

3.7.3 Large transient frequency excursions must be considered

During steady-state grid-connected mode and islanded mode, the Norwegian grid code stipulates that the frequency deviation is max ±0.1 Hz and ±1 Hz, respectively [81]. However, it will now be explained that in the transient period occurring during sudden islanding between grid-connected and islanded mode, the deviation can become much higher. This is especially true if the pre-fault situation was a distributed hydro generator injecting surplus active power into the upper grid pre-fault. Additionally, small-scale hydro-generator should not disconnect during large-frequency excursions. To facilitate a transition to islanded mode. The test bench must include relays capable of operating during large frequency deviations.

The current grid code specifies that hydropower units (type B, C, D) should be capable of operating at 47.5 Hz or 52.5 Hz for up to 30 minutes [95]. Moreover, the grid code specifies that the capability of the units to tackle frequency deviations should not be restricted unnecessarily. The system operator also specifies that: ”System operator assumes that hydroelectric power plants can be operated normally at least within the frequency ranges of 45-60 Hz, and usually even wider” (English translation by me). Consequently, to be a proof of concept, the test bench relays are made to handle transient frequencies reaching up to 60 Hz.

Before ending this chapter, Figure 3.4 demonstrated that my frequency estimator is quite slow. Using cycles to correct the estimate. I want to illustrate that this is not a problem. Looking in Figure 3.15, which is an actual measurement from a part of the Norwegian grid that went into sudden islanding. Observe how the frequency took 4 s (200 cycles) to reach the max deviation of 11.4 Hz. Therefore using some cycles to correct the estimate is no problem, as some spectral leakage is no problem. The reader should also remark on how the islanded grid was able to recover from the frequency excursion.

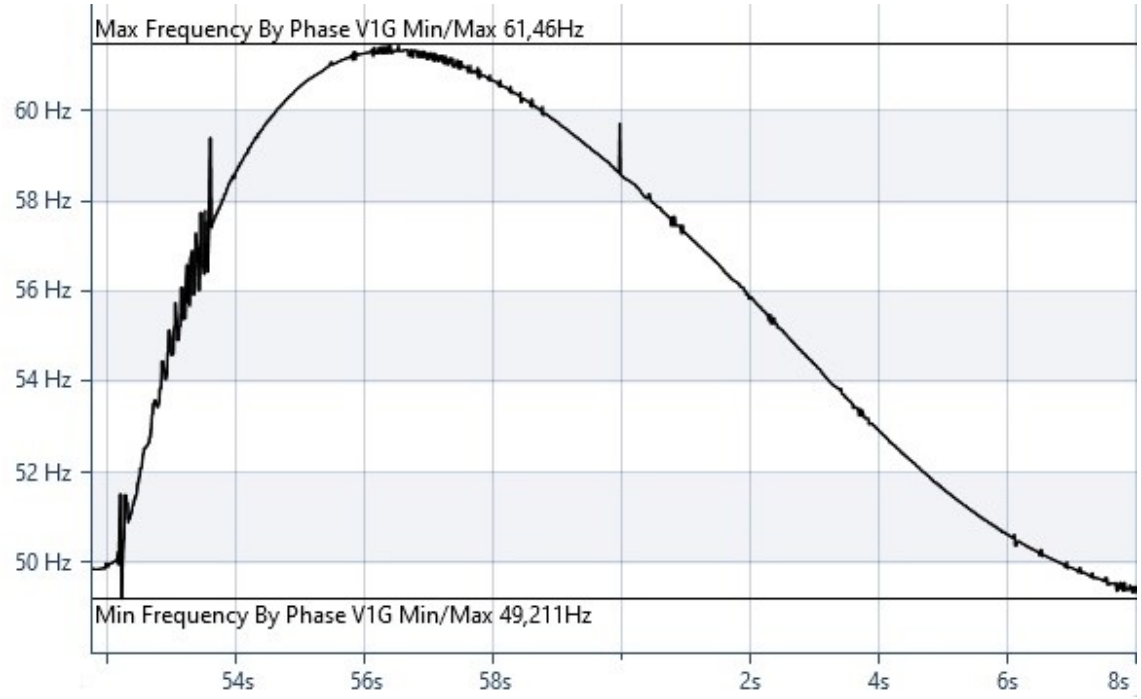


Figure 3.15: Frequency excursion during recent sudden islanding in the actual Norwegian Grid. The oscillations/noise in the graph is only due to measurement/calculation error. Measurement data are anonymized. Figure obtained by me through my part-time work.

4 Modeling Grid and Generators for HIL simulation

The testbench consists of five Raspberry Pi (R-Pi) and an OPAL-RT (OP5600). Four R-Pi emulate the 12 DRs. One R-Pi emulates the mobile communication network. The OPAL-RT simulates the grid, DG and CR in real-time. All 6 computers are connected through a switch and 7 ethernet cables. This chapter will go into the grid topology and DG. Section 5 will go into the DR, CR, and communication network.

As there should be back-and-forth communication between the simulation and Raspberry-PI, the simulations must be in real-time, meaning that simulating 1 s takes 1 s. OPAL-RT (OP5600) computer achieves real-time simulation by running c-code. The RT-LAB software compiles the c-code from a Simulink file. To facilitate real-time simulation, computational performance will be emphasized in the modeling.

The implemented simulation topology in Simulink is shown in Figure 4.1. The three subsystems correspond to the IIDG controller, grid/circuit, and relays & communication. The Relays & Communication subsystem contain blocks to publish the grid current and blocks to subscribe to GOOSE messages. The subsystem also contains the CR, which uses the GOOSE message to determine which switch gear signals to send to the grid subsystem. The second output of the grid system is the current and voltage measurements required by the IIDG controller. The IIDG controller sends back the reference voltage of the IIDG.

Computational performance is increased as the three subsystems run on three CPU cores in parallel. Parallel computation requires the input to subsystem ”A” from subsystem ”B” at timestep ”n”, to not be dependent on what occurs at timestep ”n” in subsystem ”B”. Therefore, the outputs from the three subsystems are delayed by a single time step using the ”memory” block in Simulink. The time-step is 0.1 ms and the solver is ”ode5”.

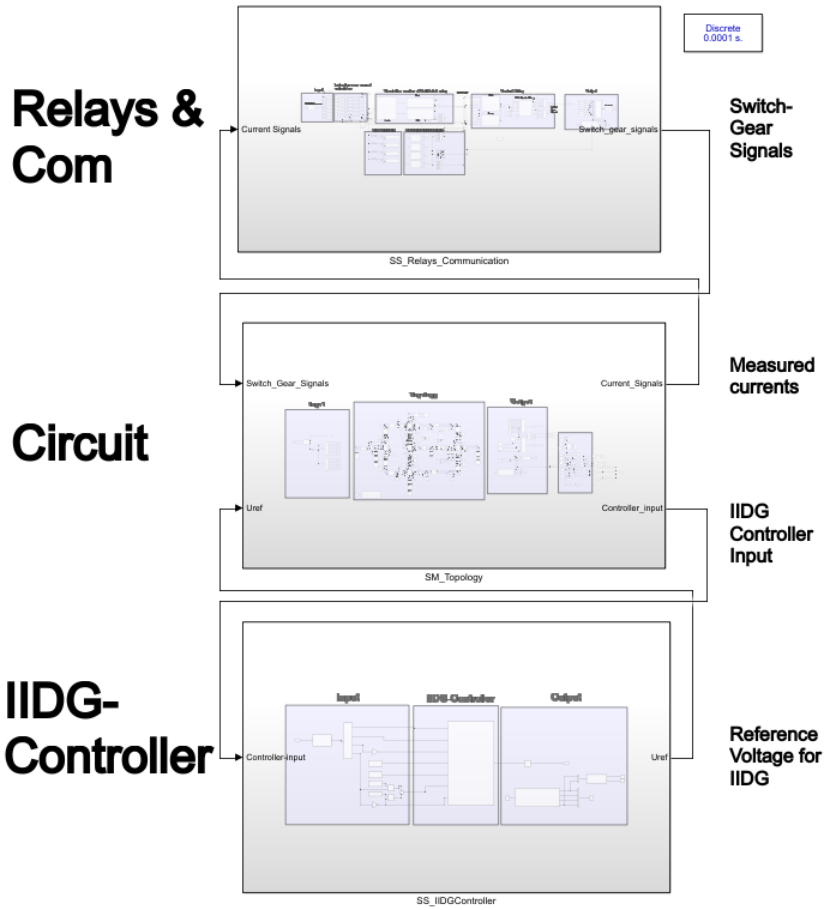


Figure 4.1: Simulation model implemented in Simulink. The CR, Grid and IIDG-controller.

4.1 System description

In Figure 4.2, the meshed 22 kV ungrounded grid implemented in Simulink is shown. The white squares are CBs, and the circle with X is a CT. Remember that each CT has a corresponding DR. Also, remember that the scheme works for any placement of the CBs. The loads at buses 1, 2, 4, and 5 are aggregated loads. The load at bus 5 represents a tapped load. If the radial case should be simulated, CB/LBS at the points marked with red ”X” is opened. This creates the radial feeder 4-5-2. If nothing else is remarked, grid-connected operation will always be with IIDG. Islanded operation is either with IIDG or SGDG at bus 3. In islanded operation, there is no connection to the upper grid at bus 1. To refer to a specific DR, the text ”DRXY” will be used. ”DR12” refers to the DR at bus 1 looking towards bus 2.

Ideally, the grid would contain more buses and loads. However, during breaker operation, the simulation time per timestep is near the physical time per timestep. Implying no remaining computational capacity to expand the grid. For convenience, the grid figure is appended on the last page of the report.

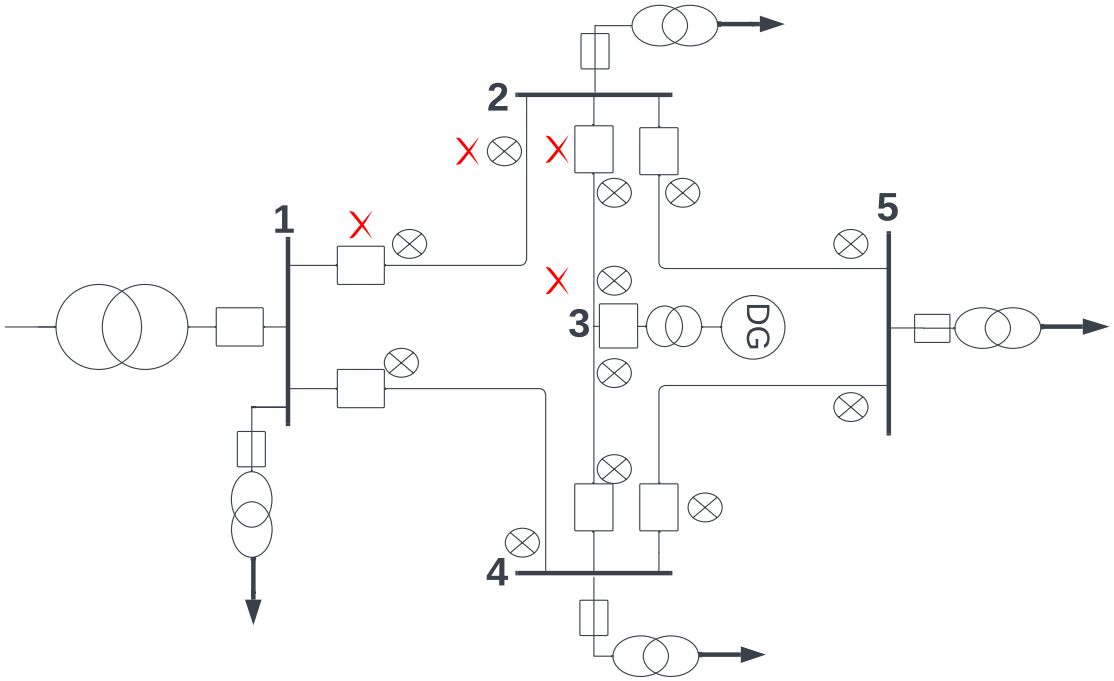


Figure 4.2: 22 kV DN implemented in Simulink

4.1.1 Line modeling

The line and cable parameters used in the PI-line model are given in Table 4.1. As expected, the R/X ratio is much greater than in the transmission system. The large R/X ratio will cause only a small DC component. There is no zero sequence series impedance for the cable in the table as it was not given in the source [96]. This is of little concern because if nothing else is said, all connections are overhead-lines. When cables are used, it will be specified, and then the zero sequence component will be of little influence.

Table 4.1: Parameters for the used 24 kV rated overhead line and XLPE cable [96].

	R[Ω/km]	**X**[Ω/km]	**Cd**[nF/km]	**R0**[Ω/km]	**X0**[Ω/km]	**Cj**[nF/km]	$\mathbf{I_{rating}}$[A]
24 kV Overhead-line	0.514	0.384	9.493	0.66	1.569	4.78	331
24 kV XLPE-Cable	0.727	0.15	140			140	145

The length between buses is 10 km with the exception of lines 2-3 and 3-4 being 5 km. Due to capacitance, a long overhead-line/cable is the worst case.

4.1.2 Load modeling

As seen in Figure 4.3 The load model consists of a distribution transformer feeding a constant impedance load.

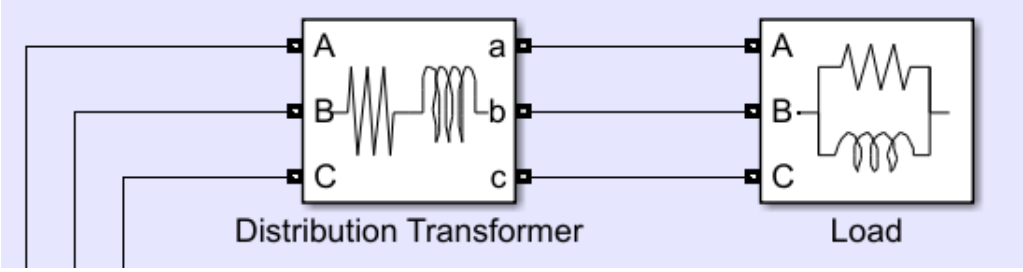


Figure 4.3: Load model in the simulation model

In the project report [1], I used the parameters for 11 typical distribution transformers from [96] and the least square method. The result was a linear approximation for the transformer positive/negative sequence short circuit impedance. In the equations below, the approximation is given as a function of transformer kVA rating:

$$r_{k,\%} = 1.24 + 0.0004 * \text{kVA}_{rating} \quad [\%] \tag{37}$$

$$x_{k,\%} = 3.07 + 0.0021 * \text{kVA}_{rating} \quad [\%] \tag{38}$$

For computational speed, the transformer is just modeled by a constant impedance with the values given by the above equation. The kVA rating is given directly by the load rating. To ensure that the zero sequence transformer impedance seen from the HV is infinite, the series load seen in Figure 4.3 is not earthed.

If the opposite is not specified all loads will have the same rating, as then the power flow is intuitive. The chosen rating for each constant impedance load is 1.6 MW with 0.525 MVar. The discussion will remark that only using constant impedance loads is a limitation of my research.

4.1.3 Sub-transmission grid modeling

The subtransmission grid is modeled by the same Thévenin equivalent as used in the project report [1]. The 66 kV/22 kV transformer is modeled by a constant impedance for computational performance. To obtain infinite zero sequence impedance as seen from the low voltage side the Thévenin voltage source is ungrounded.

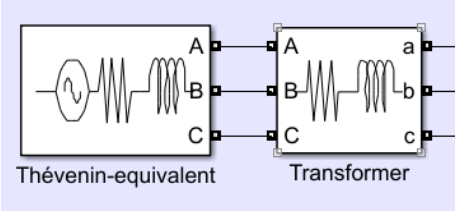


Figure 4.4: Subtransmission grid model

The short circuit capacity, rated voltage, and X/R ratio of the Thevenin equivalent are given in Table 4.2. The short circuit capacity was chosen so that a terminal fault on the low voltage side of the transformer gave a 25 pu current with respect to the nominal load flow. In the table the power transformer parameters are also given with values obtained from [96].

Table 4.2: Positive/Negative sequence data for the Thévenin equivalent and the series transformer. Modified table from the project report [1].

Thévenin equivalent				**Transformer** 66 kV/22 kV		
$\mathbf{S_k}$	$\mathbf{V_n}$	**X/R**		$\mathbf{S_n}$	$\mathbf{r_k}$	$\mathbf{x_k}$
350 MVA	22 kV	10		20 MVA	0.3%	10.35%

4.2 SGDG implementation

The SGDG implementation shown in Figure 4.5 is done using the "Synchronous Machine pu Standard" block in Simulink. The parallel resistor is for simulation stability. In Gird-connected, the generator supply 1 MW at a power factor of 0.9. In Islanded, it supplies the rated load. Observe that the field voltage (V_f) and input mechanical power (P_m) are constants. An automatic voltage controller and governor do not control them. Because as explained in Section 3.7.1, the SGDG control system has little impact on the fault response *right after* a fault. In Table A.3 all parameters for the SGDG are given. As there are no AVR or Governor, the SGDG will be unstable post-fault if the simulation runs long enough.

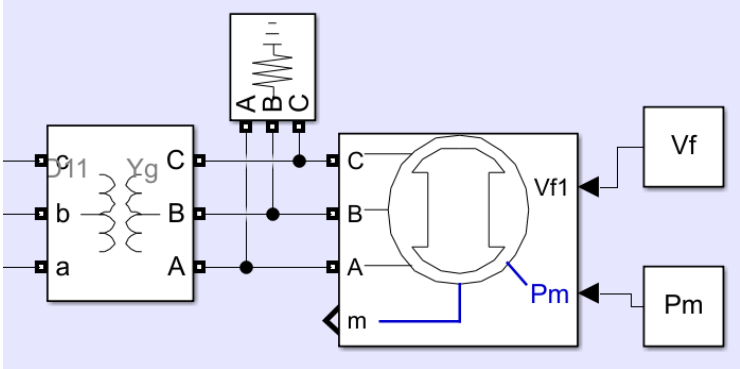


Figure 4.5: SGDG model used in the simulation model

4.3 IIDG and IIDG controller in Simulink

If the SGDG is not used, the IIDG will be used. For the master thesis, a new version of the IIDG and IIDG controller found in the project report was implemented. A voltage controller was added to support islanding, and the Phase Locked Loop (PLL) was updated to improve performance. In addition, the current limiter has been reworked to satisfy the grid code in all scenarios. Lastly, the inverter was simplified to reduce computational requirements, facilitating real-time simulation. This subsection aims to explain the IIDG controller that I implemented with the settings given in Table A.2.

Figure 4.6 is a flow chart of the implemented IIDG controller in the dq-reference frame. Measured quantities are colored red, and they are the inverter current, the Point Of Common Coupling (PCC) voltage, and the transformer current. In the grid code, the PCC is at the HV side of the transformer [93]. For simpler implementation, I defined the PCC to be at the LV side of the transformer. Thus, when setting the reactive power setpoint, the reactive consumption of the transformer must be taken into account.

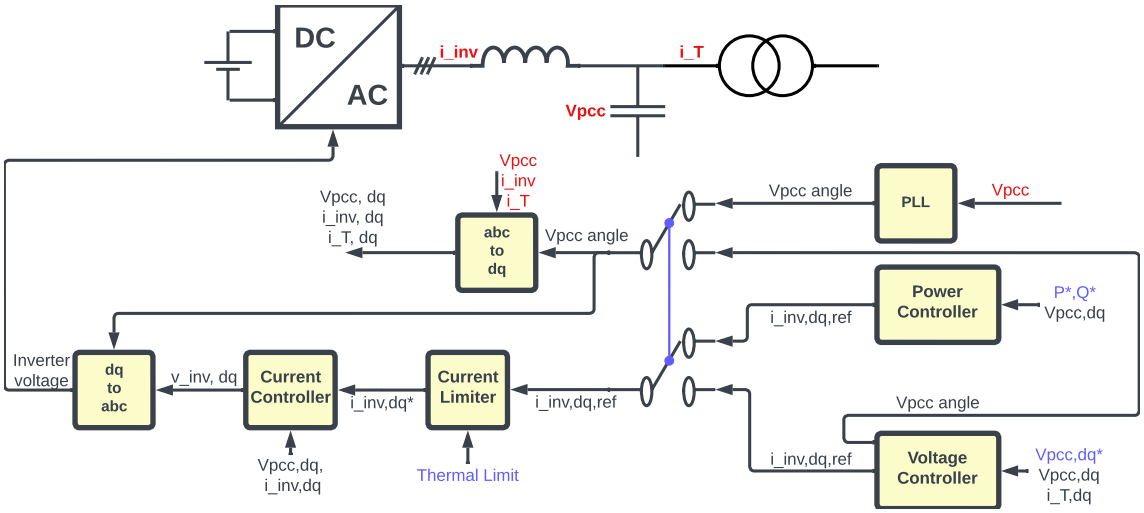


Figure 4.6: Flowchart of my IIDG controller implementation. Blue variables are constant values defined by the user, red variables are variables based on measurements (see single line diagram) and black are values derived in the controller. The switches are in the ”up” position in grid-connected mode.

Starting at the left in Figure 4.6, it is seen that the control objective is to find an inverter voltage reference. The current controller finds the inverter dq voltage reference as the voltage which achieves the inverter dq current reference. Before reaching the current controller, the inverter dq current reference is passed through the current limiter. When the current exceeds the thermal limit (1.2 pu) of the inverter transistors, the current limiter limits the current. It ensures that the proportion of active (i_d) and reactive (i_q) current satisfies the grid code.

The above paragraph was the ”inner control loop”. Now the ”outer control loop” will be explained. The inverter dq current reference fed to the limiter is obtained differently for islanded and grid-connected operations. If grid-connected, the inverter current reference is found by the power controller. The power controller uses the PCC voltage to find the current to achieve the complex power setpoint. It produces a current at the correct angle/pf as the PLL tracks the PCC voltage angle. In islanded mode, the two switches in the figure go to the ”down” position. The controller then goes from the grid following PQ control to the grid forming V/f control. The voltage angle is then created in the voltage controller, and the rate of change of the angle is the frequency of the created voltage. The inverter current reference from the voltage controller is the inverter current that achieves the user-defined voltage setpoint at the PCC.

The upcoming text will go into each specific component of the IIDG and its controller. The uninterested reader can skip to Section 5. Due to that in islanded with IIDG, it supplies the whole load. In grid-connected, it supplies 1 MW at a pf of 0.9. Nevertheless, both cases are called 1 pu. Because I will unrealistically change the absolute value of the thermal limit depending on islanded or grid-connected operation.

4.3.1 PLL (used when grid-connected)

In the above explanation, dq quantities were frequently used. To calculate the dq quantities of a three-phase signal, a reference angle is needed. In grid-connected, the reference angle is obtained by the PLL. In islanded, it is created by the voltage controller. In any case, the reference angle corresponds to phase A of the voltage at the PCC.

By receiving the measured PCC voltage, the PLL tracks the phase A PCC voltage angle. The rate of change of this angle is the frequency. To suppress the influence of harmonics, a Duble Second-Order Generalized Integrator (DSOGI) PLL was used. [97] explains the DSOGI PLL, and they made one available for download at [98], which I used in my simulations.

4.3.2 ABC to dq0 calculation

For the ABC to dq calculation, the ”ABC to dq0 transformation” block in Simulink was used. Equation 39 is the formula used by the block where ”ωt” is the reference angle. The equation is defined so that a d-axis component corresponds to a signal in phase with the reference angle. This means that the PCC voltage only has a d-axis component at a balanced steady state. It also means that a d-axis current corresponds to a current in phase with the PCC voltage. Therefore a d-axis current at the PCC is a measure of active power flow at the PCC, while q-axis current at the PCC is a measure of reactive power flow at the PCC.

$$\begin{bmatrix} x_d \\ x_q \\ x_0 \end{bmatrix} = \frac{2}{3} \begin{bmatrix} \sin(\omega t) & \sin(\omega t - 2\pi/3) & \sin(\omega t + 2\pi/3) \\ \cos(\omega t) & \cos(\omega t - 2\pi/3) & \cos(\omega t + 2\pi/3) \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} \begin{bmatrix} x_a \\ x_b \\ x_c \end{bmatrix} \tag{39}$$

4.3.3 Power controller (used when grid-connected)

The power controller takes in the user-defined complex power setpoint. The setpoint refers to the power flow into the PCC. Based on the calculated dq PCC voltage, the power controller outputs the dq inverter current, which achieves the power setpoint at the current voltage.

It can do this by utilizing the PCC power flow given by [99]:

$$\begin{aligned} p_{\text{pcc}} &= \frac{3}{2}(v_{\text{pcc},d} i_{\text{inv},d} + v_{\text{pcc},q} i_{\text{inv},d}) \\ q_{\text{pcc}} &= \frac{3}{2}(v_{\text{pcc},q} i_{\text{inv},d} - v_{\text{pcc},d} i_{\text{inv},q}) \end{aligned} \tag{40}$$

I added the 3 divided by 2 as I have *not* implemented the controller with per-unit values. Utilizing that at a balanced steady state, the q-axis PCC voltage is zero simplifies the equation above.

$$\begin{aligned} i_{\text{inv},d,ref} &= \frac{2}{3} \frac{P_{\text{ref}}}{v_{\text{pcc},d}} \\ i_{\text{inv},q,ref} &= -\frac{2}{3} \frac{Q_{\text{ref}}}{v_{\text{pcc},d}} \end{aligned} \tag{41}$$

Left part of Figure 4.7 shows how the Simulink implementation utilizes Equation 41. In the right part of the figure, there is logic for ramping up the power setpoint at the simulation start. In retrospect, the ramping was unnecessary.

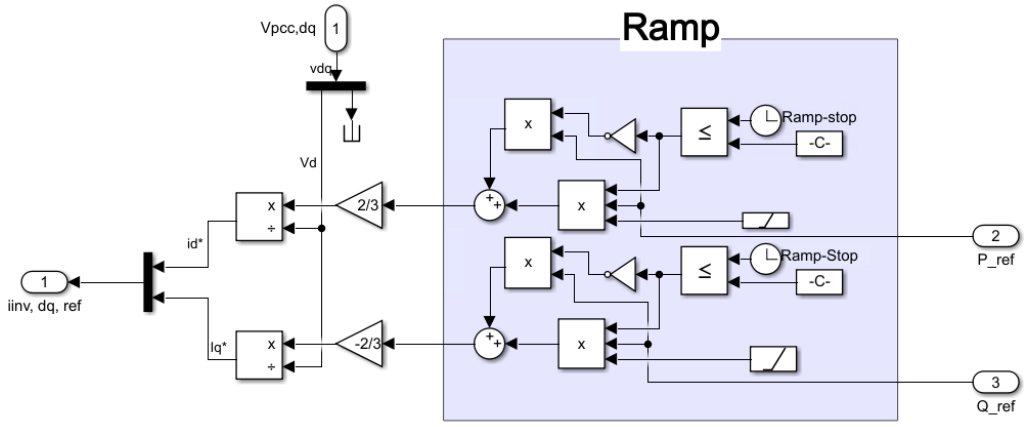


Figure 4.7: Power controller in the IIDG-controller.

4.3.4 Voltage controller (used when islanded)

Figure 4.8 shows the grid forming V/f controller used in islanded mode. It takes in the user-defined dq PCC voltage setpoint, and based on the measured transformer current, calculated filter capacitor current, and two PI-regulators, it finds the inverter current to achieve the setpoint. The voltage controller is an implementation of the one shown in [100]. A full theoretic explanation of it is given in [101], but now an intuitive explanation follows.

The middle branch, with the parameter C_f, estimates the filter capacitor current using the PCC voltage. Due to the 90° phase shift by the capacitor, a d-axis voltage causes a q-axis capacitor current. Now look at the two sums to the left. The bottom value is the capacitor current, and the top is the measured transformer current. According to Kirchhoff's Current Law, the sum of these two values are just the estimated inverter current. Suppose the measured voltage equals the voltage setpoint. The sums to the right then yield zero. Then the input of the PI controller is zero, and the PI output becomes zero (The PI output can also be a constant value as the estimated inverter current is not perfect). In that case, the output of the left sum is just the estimated inverter current meaning no controller action.

On the other hand, if the voltage is less than the setpoint, the input to the PI controller becomes positive. The output of the left sum would then be an additional current on top of the current inverter current. The consequence is that if the voltage falls below the setpoint. The voltage controller will command an increase in current output, thereby increasing the voltage.

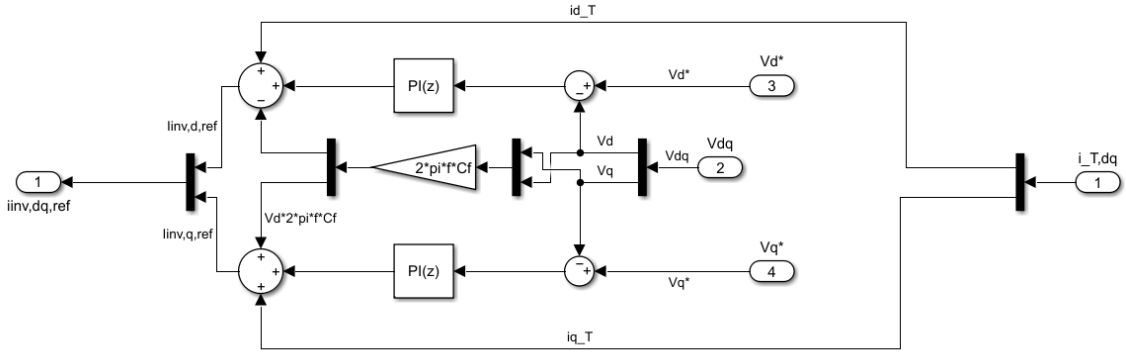


Figure 4.8: Voltage controller in the IIDG-controller. Voltages in the figure are from the PCC.

Figure 4.9 shows the part of the voltage controller producing the reference angle and, thereby, the frequency. In the figure, the output to the left is a sawtooth function that goes from 0 to 2π and repeats every 20 ms. As the function has a constant slope and repeats every 20 ms, the frequency is 50 Hz. As the slope of the function is positive, the phase sequence is ABC.

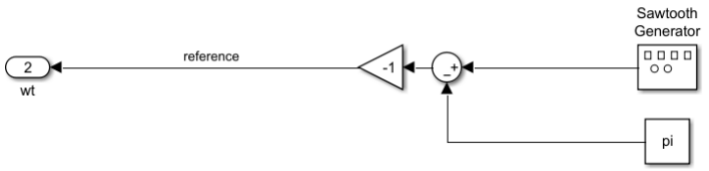


Figure 4.9: Part of voltage controller controlling the reference angle.

4.3.5 Current Limiter

The current controller, implemented in a Matlab function block, receives the current reference from either the voltage or the power controller. It uses a user-defined thermal limit for the inverter RMS current, which is typical 1.2 pu. Its purpose is first to cap the current to the thermal limit. Second, it will ensure that the proportion of the d- and q-axis during fault follows the grid code specification.

To understand the implemented logic, denote the reference current into the limiter as ”pre”. Depending on the reference RMS current in Equation 42 and the value of d- and q-axis current, there are three possibilities.

$$I_{inv,ref,rms} = \sqrt{i^2_{d,inv,ref} + i^2_{q,inv,ref}} \tag{42}$$

- **Possibility 1** is that the inverter reference RMS current does not exceed the thermal limits of the switches, then:

$$\begin{aligned} i_{d,inv,ref} &= i_{d,inv,ref,pre} \\ i_{q,inv,ref} &= i_{q,inv,ref,pre} \end{aligned} \tag{43}$$

  This option can occur during a fault when the pre-fault power reference is low. For example, say there is a grid-connected operation with a complex power setpoint of 0.2 pu active power and 0 pu reactive power. If the pre-fault voltage is 1 pu, then the pre-fault current reference is $i_d = 0.2$ pu and $i_q = 0$ pu. After a fault the PCC voltage drops to 0.2 pu and the PQ controller achieves the power reference by using $i_d = 1$ pu and $i_q = 0$ pu. This current does not exceed the thermal limit so no limitation is necessary. In cases with voltage decreases seen in this example the Norwegian grid code can require the $i_{q,inv,ref}$ to be increased until the inverter hits the thermal limit [93]. However, no such logic is implemented as it *can* only be required for units greater than 10 MW.

- **Possibility 2** is that the thermal limit is exceeded and the d axis component is greater or equal to the thermal limit ($i_{d,inv,ref,pre} \geq I_{thermal}$). As the grid code specify that the active power contribution should not be un-purposefully limited [93]. The d-axis current should then be the only current, and it should be set to the thermal limit:

$$\begin{aligned} i_{d,inv,ref} &= I_{thermal} \\ i_{q,inv,ref} &= 0 \end{aligned} \tag{44}$$

  This response is depicted in Figure 4.10 where the solid line is the input to the current limiter and the dotted lines are the output. Figure 4.10 is a result of a simulated fault later in this thesis.

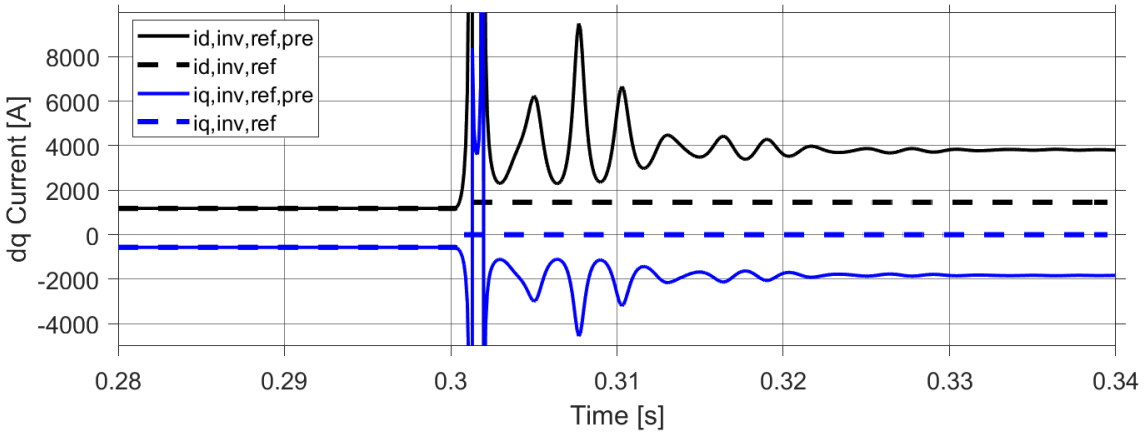


Figure 4.10: Example response of the implemented current limiter. The dotted lines are the output.

- **Possibility 3** means that the thermal limit is exceeded, but the d-axis current does not by itself exceed the limit. Again the grid code is followed as priority is given to the d-axis current, but what remains

to hit the limit is allocated to the reactive component:

$$\begin{aligned} i_{d,inv,ref} &= i_{d,inv,ref,pre} \\ i_{q,inv,ref} &= \sqrt{I^2_{thermal} - i^2_{d,inv,ref,pre}} \end{aligned} \tag{45}$$

In the right of Figure 4.11, the current limiter is shown. It is a Matlab function block where Matlab code written by me implements the logic described above. In the added folder, the code can be found.

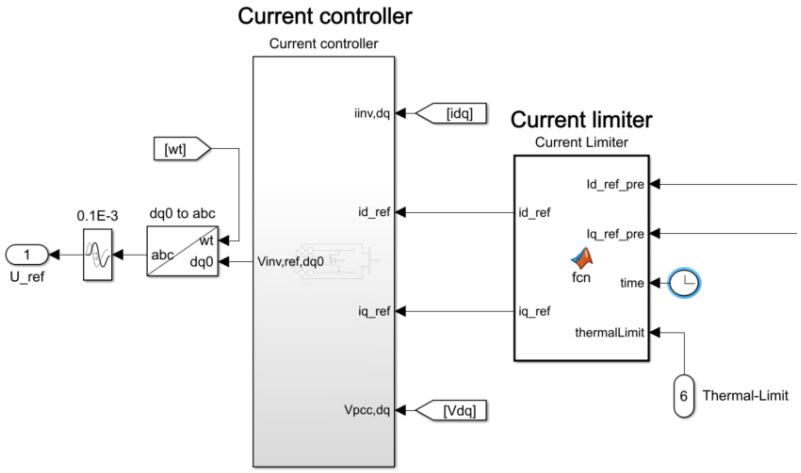


Figure 4.11: Current limiter in IIDG-controller. The limiter is a Matlab Function Block with my code.

4.3.6 Current Controller

The current controller takes in the PCC voltage, inverter current measurement, and inverter current reference. It then uses two PI controllers to yield an inverter voltage reference that shall cause the inverter current reference to flow out of the inverter. The implementation in Figure 4.12 is an implementation of the controller given in [100]. For a full theoretic explanation, the reader is again referred to [101], and now an intuitive explanation follows.

The working functions of the current controller are similar to the voltage controller. Looking at the sums to the left, the top value is the measured PCC voltage. The bottom value is the estimated voltage over the filter inductor. According to Kirchhoff's voltage law, the sum of the top and bottom values is the estimated inverter voltage. If the inverter current is less than the reference, the input to the PI controller is positive. In that case, the controller's output would be the current estimated voltage plus an additional value. Thus, as expected, the voltage reference is raised when the current should increase.

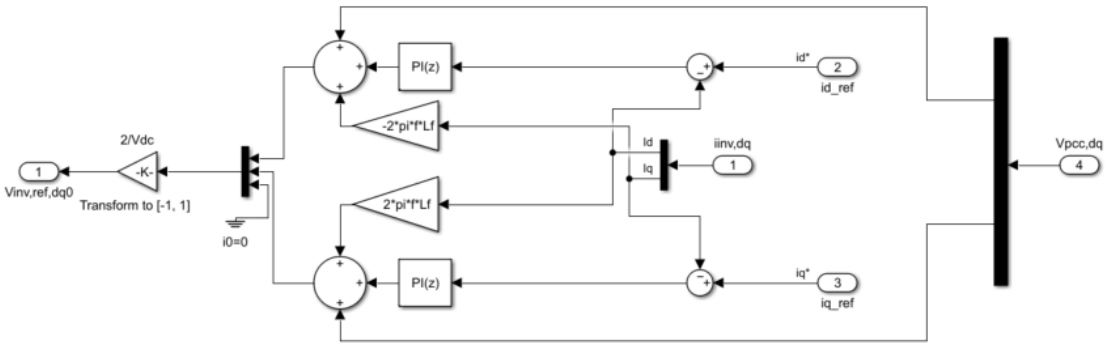


Figure 4.12: Current controller in IIDG-controller

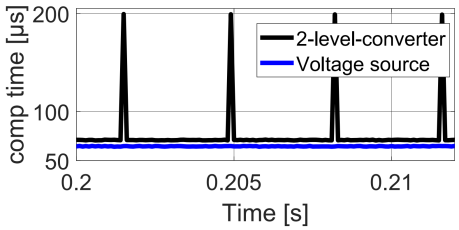
4.3.7 dq0 to ABC

The current controller output is the inverter ”dq0” voltage scaled by the value of DC voltage so that it is between -1 and 1. After this leaves the current controller, it will be transformed to the inverter ”ABC” voltage by using the ”dq0 to abc transformation” block. Equation 46 shows the formula implemented by the block.

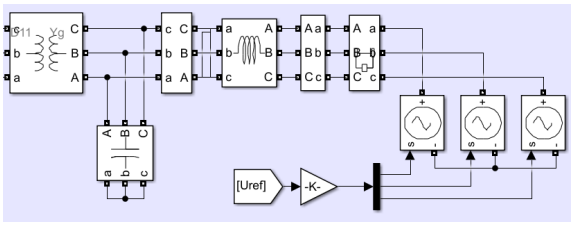
$$\begin{bmatrix} x_a \\ x_b \\ x_c \end{bmatrix} = \begin{bmatrix} \sin(\omega t) & \cos(\omega t) & 1 \\ \sin(\omega t - 2\pi/3) & \cos(\omega t - 2\pi/3) & 1 \\ \sin(\omega t + 2\pi/3) & \cos(\omega t + 2\pi/3) & 1 \end{bmatrix} \begin{bmatrix} x_d \\ x_q \\ x_0 \end{bmatrix} \tag{46}$$

4.3.8 Inverter modeling

For the project report, the ”2-level-converter” block with the average function was used. An average model means that the switches themselves are not modeled. When using this block the black lines in Figure 4.13a show that every 3.33 ms, during commutation, there are spikes in computational time. As the spikes exceed/overshoot the timestep (0.1 ms), it renders the simulation non real-time. Therefore in the master thesis, the average inverter model is simplified to three controlled voltage sources. Observing Figure 4.13b the voltage-controlled sources realize the inverter reference voltage from the IIDG controller. Keep in mind that the gain block in the figure scales the voltage reference back up from [-1, 1]. Observing the blue line in Figure 4.13a it is seen that this solution does not cause overshoot.



(a) Computational time per time-step in OPAL-RT



(b) Average model of the inverter. (Transformer current measurement not shown)

Figure 4.13: Computational time of OPAL-RT and average model of the inverter.

4.3.9 IIDG Model tuning and verification

Figure 4.14 shows the full IIDG controller. The only block not explained is the ”Grid-connected or islanded”. As islanded detection is not a focus of the master thesis, this block just uses the CB status of the CB connecting the DN to the sub-transmission to determine if it is grid-connected or islanded. In the preceding paragraphs, it was clarified that both the ”Current Controller” and the ”Voltage Controller” incorporate a pair of PI controllers, yielding eight parameters that can be adjusted. To limit the degrees of freedom to four, each pair of PI controllers will have the same proportional and integral constant.

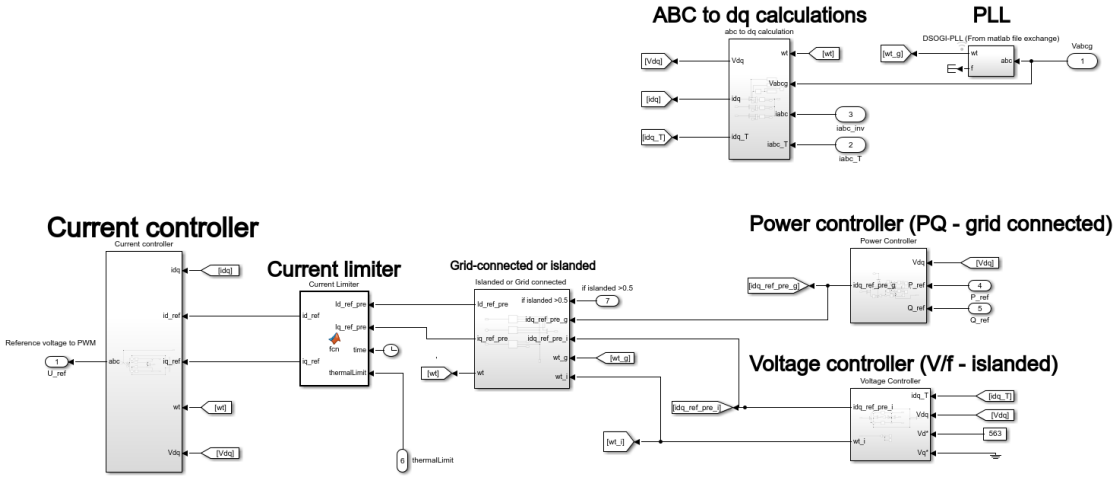
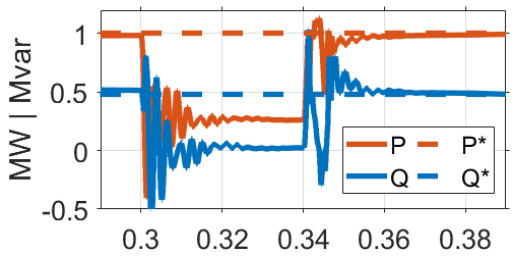


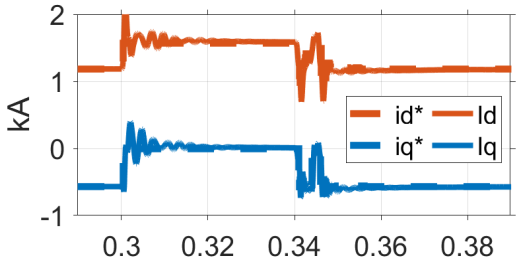
Figure 4.14: IIDG controller implemented in Simulink.

The full approach to finding the PI control parameters is given in Section A.2. In short terms, first, the parameters for the inner-control loop (current controller) were found. This was done running in grid-connected mode. Then the parameters of the outer-control loop (voltage controller) were found. This was done by running in islanded mode and using the already found parameters for the inner control loop.

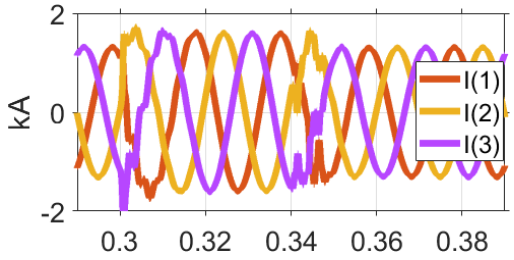
In Figure 4.15, the response of the inverter during a grid-connected fault is shown. Observe from Figure 4.15a that during a fault, it prioritizes active current. This is also shown by looking at the d and q-axis current in Figure 4.15b. Lastly, looking at the inverter terminal current in Figure 4.15c. Observe that very quickly after the fault. It reaches a new steady state limited to 1.2 pu.



(a) Power measurement compared to reference



(b) dq Current measurement compared to reference



(c) Inverter terminal current measurements

Figure 4.15: IIDG response in Grid-connected for a fault. The fault is initialized 0.3 s and then removed at 0.34 s.

5 Modeling communication network and relays

In Figure 3.1, the flow chart of the theoretic implementation was given. Figure 5.1 shows the flowchart of the implementation done to evaluate the scheme. The reader should note that the only difference is that the PS instantaneous currents are calculated inside the merging unit, instead of in the DR. This was done to lower communication bandwidth as all DRs are on the same LAN in the evaluation. Also, observe in Figure 5.1 that the text on the bottom gives on what physical device or software the implementation occurs.

Building a test bench is an objective/result of the thesis. Therefore, after giving an overview of the test bench I built. The objective is to describe the implementation of DR, CR, and communication networks in detail. All settings used for the relays can be found in Table A.4.

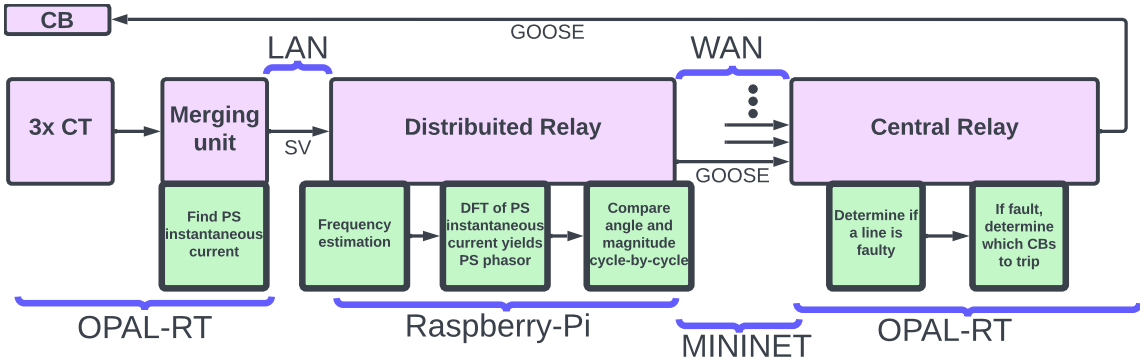


Figure 5.1: Flowchart of the implemented protection algorithm

5.1 Overview of the test bench

In Figure 5.2, illustrates the test bench. Blue lines are ethernet cables, the wifi symbol indicates wifi communication, and the microprocessors are R-Pis. Starting from the right, the grid is made offline in RT-LAB. The project is then compiled to c-code and uploaded to the OPAL-RT. All relays and the WLAN emulation are initiated through a laptop. The laptop remote controls all five R-Pi using the application "VNC-viewer". The HIL simulation starts by initiating the real-time simulation on the OPAL-RT.

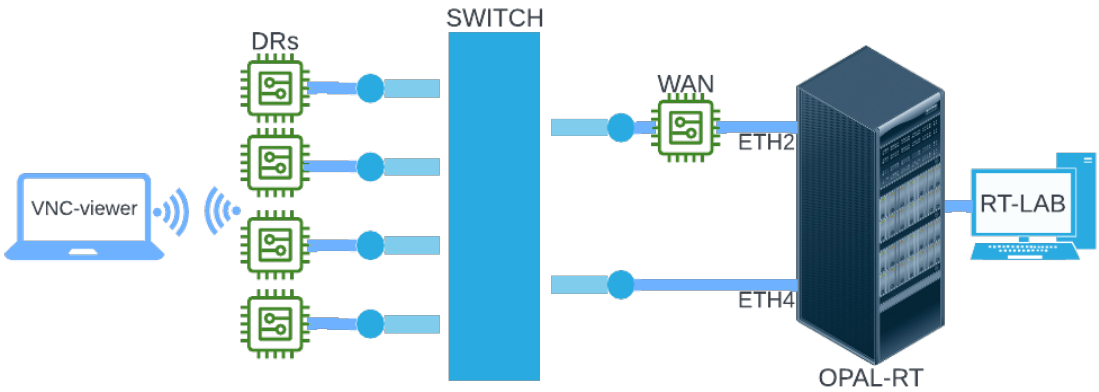


Figure 5.2: Illustration of the physical lab setup. Blue lines are ethernet cables. Microprocessors are Raspberry-Pis.

In Figure 5.3, the actual test bench is depicted. Starting on the right, the OPAL-RT runs the grid introduced in Section 4. Every 1 ms the OPAL-RT publishes 4 packets, each with 3 instantaneous positive sequence samples on "ETH4". The packet satisfies IEC61850-9-2, and this step will be further described in Section 5.2.

After going into the switch, the SV packets reach the four R-PI to the left. Each R-PI receives all four packets every 1 ms, but only subscribes to one of them. Each R-PI will then emulate three out of the twelve DRs. I used 4 R-PIs instead of 12 because I only had four available. Emulating multiple DRs within a single R-Pi does not make the setup less credible. Because each R-PI emulates three DRs from three distinct line sections. Nevertheless, the R-Pi uses the SV for the CCA and IJump algorithms. If the algorithm detects either a change in CCA or IJump status, it triggers a publication of a GOOSE message. SV-subscription, DR-algorithm implementation, and GOOSE publication are described in Section 5.3.

The published GOOSE message first goes to the switch. It will then go to all terminations on the switch, including the R-PI emulating the WAN (middle of the figure). This R-Pi emulates a WAN with the MININET software and applies a time delay. The MININET implementation is explained in Section 5.4.

The MININET emulation then publishes the time-delayed GOOSE message on the other ethernet port of the R-Pi. The ETH2 ethernet port of the OPAL-RT is configured to subscribe to this incoming GOOSE message. This process is explained in Section 5.5.

Finally, the OPAL-RT now has the GOOSE message. In the simulation, there is also the CR and it uses the incoming GOOSE messages to identify if there is a fault and which CB to trip. If a CB should trip, the signal from the CR to the CB has no applied time delay. However, the consequences of the actual time delay will be commented on. Section 5.6 describes the CR implementation.

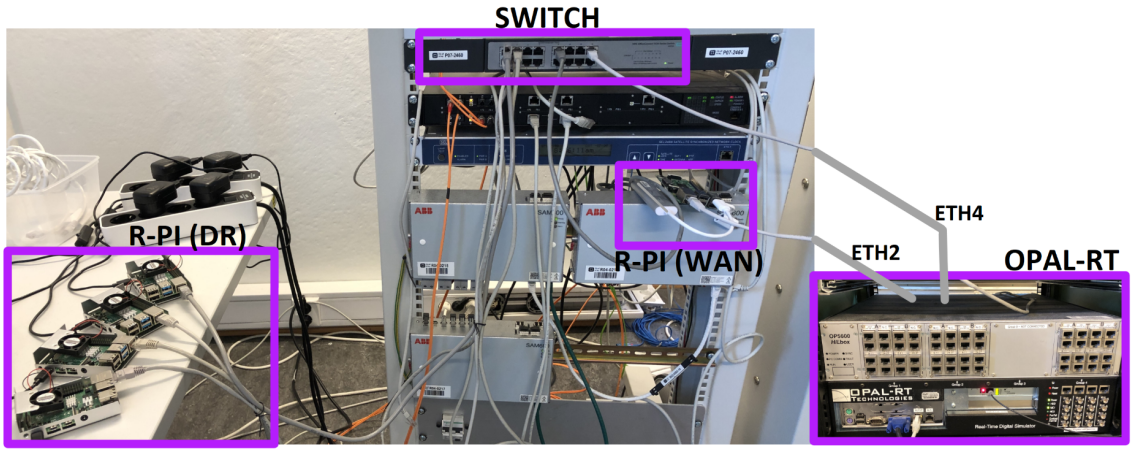


Figure 5.3: My built Hardware in the loop setup in the laboratory.

5.2 Sample value communication to Raspberry Pi

In the actual grid, the communication between each MU and corresponding DR are on separate LANs. However, when testing, they are all on the same LAN. Therefore to reduce the communication burden, two simplifications are made. Firstly, the instantaneous PS current is calculated inside the OPAL-RT instead of the R-Pi/DR. A line end will then only have to communicate one value instead of three per 1 ms. Secondly, each SV packet has three instantaneous PS currents from three distinct lines instead of them being sent separately. With 12 line ends, this results in 4000 distinct packets per second. In retrospect, it was discovered that modifying the ICD file so that each packet has three sets of three-phase measurements. Would not have caused a significantly larger bandwidth requirement.

To set up the communication system the following approach is used. In the OPAL-RT SV are fed to transport delay blocks each ms to obtain the 6.67 ms and 13.3 ms delayed currents. Taking a sum, results in the instantaneous positive sequence current which is passed to an RT-LAB ”OpOutput” block in Simulink.

Separately, in the IEC61850 configurator in RT-LAB, four ICD files are added. The ICD files are based on the IEC61850 example in RT- LAB, but modified for my purposes. Each ICD file is made to specify the APP-ID and Mac broadcast address for a specific set of three instantaneous PS currents. In Figure 5.4, the view in RT-LAB IEC61850 configurator after importing the ICD files is shown. So far, the instantaneous

#	SCL file	IED	SV ID	Ethernet Adapter	Clock	Nominal Frequency	Sampling Rate	Number of ASDUs	AppID	MAC address
1	models\Master_simulink_2019b\iec61869...	MU1	karl-R1	eth4	INTERNAL	50 Hz	1000 Samples Per Second	1	0x4001	01-0C-CD-04-00-01
2	models\Master_simulink_2019b\iec61869...	MU2	karl-R2	eth4	INTERNAL	50 Hz	1000 Samples Per Second	1	0x4002	01-0C-CD-04-00-02
3	models\Master_simulink_2019b\iec61869...	MU3	karl-R3	eth4	INTERNAL	50 Hz	1000 Samples Per Second	1	0x4003	01-0C-CD-04-00-03
4	models\Master_simulink_2019b\iec61869...	MU4	karl-R4	eth4	INTERNAL	50 Hz	1000 Samples Per Second	1	0x4004	01-0C-CD-04-00-04

Figure 5.4: RT-LAB view after importing ICD files for SV communication

PS current is passed to an OpOutput block. Additionally, the ICD file, containing DAs (Data Attributes), specifying what and how SV should be communicated, is uploaded to RT-LAB. The last step is to create an association between an OpOutput block and a DA. This step is done through ”Drag and Drop” in the ”configurator”.

The code below shows a small code snippet of the ICD file. In line 1, it is seen that there is 1 DO with two corresponding DA in line 2 and line 3. Line 2 shows the DA ”instMag”, the SV. Looking at the same line, it specifies that ”instmag” is of type ”AnalogValue”. In lines 5 and 6, the type ”AnalogValue” is specified to be a 32-bit integer. The other DA is ”sVC”, and line 3 specifies that it is of the type ”AmpScaledValueConfig”. Lines 8-10 specify that this type is a scale factor of value 0.001. What all this means is, say that the actual instantaneous current is 100.1234 A. The scale factor specifies that it should be scaled by 1000 and the 32-bit integer specifies it should then be converted to an integer. The communicated value is 100123 A.

```
1  <DOType id="AmpSAV" cdc="SAV">
2        <DA name="instMag" bType="Struct" type="AnalogueValue" fc="MX"/>
3        <DA name="sVC" bType="Struct" type="AmpScaledValueConfig" fc="CF"
             dchg="true"/>
4
5  <DAType id="AnalogueValue">
6        <BDA name="i" bType="INT32"/>
7
8  <DAType id="AmpScaledValueConfig">
9        <BDA name="scaleFactor" bType="FLOAT32">
10         <Val>0.001</Val>
```

5.3 Distributed relay: SV-subscription, DR-algorithm and GOOSE-publication

All Raspberry PIs: run the Raspberry Pi OS, are controlled by VNC-viewer, have Wireshark to monitor the packets, and use c-code written by me to act as a DR. Furthermore, the open source software called libiec61850 is installed on them to facilitate IEC61850 communication [102]. In Section B.6, I have written a guide on how to set up the R-PI for IEC61850 communication. With my help, two PHD-candidates used this guide to solve their problems in half an hour when they had been stuck for two days. In the file ”DR.c”, see Section A.1, the code I made is implemented. The DR.c structure is shown in Figure 5.5. The following paragraphs will explain how the code does SV-subscription, DR-algorithm, and GOOSE-publication.

In the upper left corner, the ”#includes” reveals that my code relies on the ”static_model.h” and ”DFT.h” files. The static model is the result of compiling the ICD file for GOOSE communication into c-code. In the DFT.h

file, I have implemented a frequency estimator, recursive DFT, and logic to determine if there is a CCA- or IJump-condition. In the same upper left box, observe that two global variables/arrays are initialized. DFTs is a variable used to aid the DFT calculation, and f_estimators is a variable used to aid the frequency estimation.

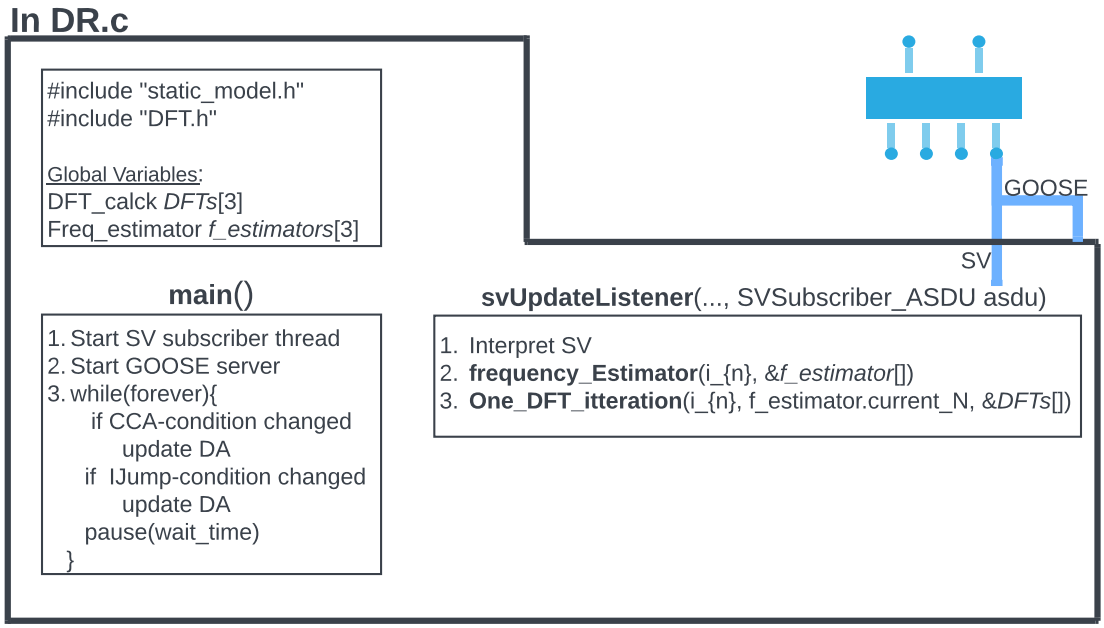


Figure 5.5: C-code structure in the Raspberry-Pi that emulates the DR.

The DR is turned on by calling the ”main” function in the lower left corner one time. It first creates a *thread* for SV subscription. The thread is the box to the right, and it can be thought of as another program running in parallel to the main() function. Continuing with the main function, it then creates a GOOSE server for GOOSE publishing and starts an infinite loop. The loop runs every 0.1 ms. In the loop, it is checked if ”DFTs” has a different value for CCA and IJump condition than the DA specified by the ICD file. If they differ, the DA is updated to the value specified by ”DFTs”. Due to the content of the ICD file, changing the DA automatically triggers the publication of a GOOSE message.

The main function neither does nor calls a function that does SV interpretation, frequency calculation, DFT calculation, or checks if there is a CCA- or IJump-condition. This is all done by the thread in parallel. Because when the thread is made, it is specified to subscribe to packets with a certain MAC-Broadcast address. When a packet with the specified MAC address reaches the Ethernet port of the raspberry-PI, it will *automatically* cause the svUpdateListner function in the right box to be called. svUpdateListner takes out the SV, runs frequency estimation by using the frequency_estimator function, and does DFT with the One_DFT_iteration function. The DFT function will also check for an IJump or CCA condition. Also, observe that the frequency-estimator and DFT function receive a c-code *pointer* to the global variables DFTs and f_estimator. In the global variables, buffers of the previous values of frequency, current, current magnitude, and current angle are stored.

There are now two threads/programs running in parallel, represented by the main and svUpdateListner functions. The main function never calls the svUpdateListner function, so how does it know if there has been a CCA- or IJump-condition? The answer is that both functions share access to the global variable DFTs. If there is a CCA- or IJump-condition, svUpdateListener will update a variable in DFTs that indicate this. Moreover, the main function will read the status of DFTs and therefore know if there is a CCA- or IJump-condition.

The DR implementation has now been explained. In Simulink/OPAL-RT, I have also implemented the DR

to verify the scheme and to do tests when communication has no influence. I will specify when the DR made in OPAL-RT is used. In the upcoming text, the particularities of the DR-code on R-PI are given. For the reader that is not interested in the details, skip to Section 5.4.

5.3.1 Creating a parallel thread for SV subscription

In the code below, the part of the main() function that creates a parallel thread for SV subscription is shown. None of the functions called are created by me, and the code is based on the ”sv_subscriber_example” in libiec61850. Observe that line 4-5 creates a receiver that looks at ethernet port ”eth0” of the R-PI. Line 6 creates a subscriber which looks for packets with the ethernet_adress and appID specified in line 1-2. This appID and ethernet_adress corresponds to merging unit 1 in Figure 5.4. Furthermore, line 7-8 specifies that if the receiver detects a packet with this address. Then it shall call the function svUpdateListner.

```
1 uint16_t appID = 0x4001;
2 uint8_t ethernet_address[6] = {0x01, 0x0C, 0xCD, 0x04, 0x01, 0x01};
3
4 SVReceiver receiver = SVReceiver_create();
5 SVReceiver_setInterfaceId(receiver, "eth0");
6 SVSubscriber subscriber = SVSubscriber_create(ethernet_address, appID);
7 SVSubscriber_setListener(subscriber, svUpdateListener, NULL);
8 SVReceiver_addSubscriber(receiver, subscriber);
9 SVReceiver_start(receiver);
```

5.3.2 Interpreting SV packets

An argument of svUpdateListner is the Application Service Data Unit (ASDU), containing the SVs. The code below shows how ”SVsubscriber_ASDU_getINT32(asdu, i*8)” is used to take out the SV, Observe:

- The for loop goes from i=0 to i=3, because there are three SV from the grid simulation and one used for debugging.
- The ICD file specifies that the SV is stored as an INT32 an INT32 is extracted.
- In line 3 ”i*8” specify the byte position of the starting byte of the SV in the ASDU. For every new SV extracted by the for loop, the starting byte is iterated by 8 bytes. Because the SV itself takes 4 bytes and each SV has corresponding quality bits taking 4 bytes.
- As the ICD specified that the SV was scaled by 1000 before transmitting, the SV is divided by 1000.

```
1 float i_samp[4] = {0};
2 for (int i = 0; i < 4; i++) {
3     i_samp[i] = SVSubscriber_ASDU_getINT32(asdu, i*8)/1000.0f;
4 }
```

5.3.3 LP filter and frequency estimation

The frequency estimation and the LP filter are implemented by me according to the description in Section 3.3. As explained the function relies on manipulating a global variable of type Freq_estimator. Freq_estimator is a struct defined in DFT.h below, observe the variable ”Current_N” which is the N to be used by the DFT filter.

```
1 typedef struct {
2     float prev_output;              //last filter output
3     int   Every_4_counter;          //Counts: 1, 2, 3, 4, 1, 2, 3, 4
4     float last_recorded_cz;         //time of last recorded CZ
```

```
    int   index;                    //current timestep/ms 1,2,3, ...
    int   index_next_estimate;      //where in the vector_of_estimates
    float vector_of_estimates[AMOUNT_ESTIMATE];//last three frequency estimates
    float current_estimate;         //Current frequency estimate
    float current_N;                //N to be used by the DFT filter.
} Freq_estimator;
```

In the code below the function created by me in DFT.c that has the LP filter and frequency calculation is shown. Pay attention to how the code takes in a pointer to a Freq_estimator. The reader is encouraged to read the comments in the code.

```
float frequency_Estimator(float new_sample, Freq_estimator* Freq_e){
    float LP_prev = Freq_e->prev_output; //last output of LP filter
    float LP_now  = LP_prev + LP_CONSTANT*(new_sample-LP_prev); //LP filter

    //Check for current zero crossing
    if (LP_prev >= 0 && LP_now <0 || LP_now > 0 && LP_prev <=0){

        //Update the circular counter (1, 2, 3, 4, 1, 2,...)
        Freq_e->Every_4_counter = (Freq_e->Every_4_counter % 4)+1;

        //For every fourth CZ do the frequency estimation
        if (Freq_e->Every_4_counter == 4){
            //linear interpolation to find the CZ
            float where_crossed = -(LP_prev)/(LP_now-LP_prev);
            float point_of_cz = (float)(Freq_e->index) +where_crossed -1;

            //estimate frequency. "2" due to comparing over 2 cycles
            float estimate = 2/(INTERVALL*(point_of_cz-Freq_e->last_recorded_cz));

            //place the estimate in the vector of estimate and update index
            Freq_e->vector_of_estimates[Freq_e->index_next_estimate] = estimate;

            //Median av vector_of_estimate gir det endelige estimatet
            //findMed is a function created by me
            Freq_e->current_estimate = findMed(Freq_e->vector_of_estimates);

            //find_N uses the table provided in theory to find N based on f
            Freq_e->current_N = find_N(Freq_e->current_estimate);

            //update the time of recorded cz and index of next estimate
            Freq_e->last_recorded_cz = point_of_cz;
            Freq_e->index_next_estimate = (Freq_e->index_next_estimate+1) %
    AMOUNT_ESTIMATE;
        }
    }

    //update index and update LP output
    Freq_e->index = Freq_e->index+1;
    Freq_e->prev_output = LP_now;
}
```

5.3.4 Phasor calculation

The phasor calculation and checking of the CCA- and IJump-condition are implemented according to Section 3.1 and Section 3.2. As with the frequency calculation, the approach was to create a struct and a function to manipulate the struct. Below is my declaration of the struct DFT_calck in DFT.h. Observe that the struct stores SVs, phasor angle, and phasor magnitude in a circular buffer of size 30. As per

Section 3.2, 30 is much bigger than any expected N. Complex X is a struct that contains the most recent phasor calculation. The change_signal and jumped_signal indicate the current status of IJump and CCA, and it is these variables that are used by the main() function to check if the GOOSE ICD DA needs to be updated.

```
typedef struct {
    char name[3];                                   //Name of DR
    float circular_buffer_sample[BUFFER_SIZE];      //Store samples
    float circular_buffer_angle [BUFFER_SIZE];      //Store angles
    float circular_buffer_magnitude[BUFFER_SIZE];   //Store magnitudes
    Complex X;          //Latest value of the phasor, contain X.A (Re) and X.B (Im)
    int not_first_run;  //1 if a Buffer_size iteration is done, else 0
    int current_index;  //Current index in the circular buffer [0, BUFFER_SIZE]
    int history_index;  //Index "N" samples ago. "N" is decided by the frequency
    int change_signal;  //1 if there is a CCA-condtion else 0.
    int jumped_signal;  //1 = when jump up, -1 = when jump down, Else 0
    int current_n    ;  //Itterates in the range [0, N-1)
} DFT_calck;
```

In the code below, the function created by me in DFT.c that does the DFT iteration and checks for CCA- and IJump-condition is given. Observe that the code takes in a pointer to the DFT struct and the SV. It also takes in the "N" value, which the frequency estimator found. Observe the following:

- Line 3 uses the modulus operator to find the index in the circular buffers where values from N samples ago are stored. For example, if n=10, N=20, and BUFFER_SIZE=30, it will output 20. Lines 5-8 use the index to extract the current and PS phasor from N samples ago.
- In lines 11 to 17, a recursive DFT iteration is done. The function used is the one in Equation 9, split into a real and imaginary part to avoid using complex variables.
- In lines 21 to 31, the CCA-angle is extracted and normalized to be in the range $(-180°, 180°]$. Lines 33-37 will ensure that if the absolute value of the CCA-angle is greater than 90°, then change_signal equals 1. Else it is zero.
- In lines 40 to 49, it is checked if there is an IJump condition and the jumped_signal variable is updated.
- The remainder part of the code updates the circular buffers, and the current index (n) is iterated. Furthermore, there is logic to check if one buffer size amount of iterations is done because until then, the DFT output is not reliable, and there shall be no CCA-condition or IJump condition.

```
void one_DFT_itteration(DFT_calck* DFT_c , float new_sample, float N){
    //find history_index, which is the index N samples ago
    int history_index = (DFT_c->current_index - (int)N + BUFFER_SIZE) % BUFFER_SIZE;

    //find the current sample, phasor angle, and phasor magnitude N samples ago
    float old_sample =  DFT_c->circular_buffer_sample[history_index];
    float old_angle  =  DFT_c->circular_buffer_angle[history_index];
    float old_mag    =  DFT_c->circular_buffer_magnitude[history_index];

    //DFT start.
    //Find the Re and Im part that should be added to the history term of re
    float updateA = (2.0/N)*cosf(2.0*PI*(DFT_c->current_n)/N)*(new_sample-old_sample);
    float updateB = (2.0/N)*sinf(2.0*PI*(DFT_c->current_n)/N)*(new_sample-old_sample);

    //Obtain the Re and Im part of the new phasor using the history terms
    DFT_c->X.A += STABILITY*updateA; //stability is approx 1
    DFT_c->X.B += STABILITY*updateB;

    //DFT is done. Now check for CCA-Condition
```

```
    //calculate current angle. Set to zero for the first Buffer_size iterations
    float new_angle = atan2f(DFT_c->X.B, DFT_c->X.A)*DFT_c->not_first_run*RAD2DEG;
    float CCA_angle = new_angle - old_angle; //find angle change

    //correct so that the angle diff is between -180 and 180
    //for example if new_angle = 175 and old_anlge = -175 then
    //angle difference should be 10, not 175-(-175) = 350
    if (CCA_angle > 180){
        CCA_angle-=360;
    } else if(CCA_angle <= -180){
        CCA_angle+=360;
    }
    //check if there is a CCA-condition
    if (CCA_angle>=TRIP_ANGLE || CCA_angle<=-1*TRIP_ANGLE){
        DFT_c->change_signal = 1;
    } else {
        DFT_c->change_signal = 0;
    }

    //CCA is done. Check for IJump-condition
    //calculate the current magnitude of the current.
    float new_mag = sqrt(pow(DFT_c->X.A, 2) + pow(DFT_c->X.B, 2))*DFT_c->not_first_run;
    float Ijump_magnitude = new_mag/(old_mag);
    if (Ijump_magnitude >= Ijump_upper){
        DFT_c->jumped_signal = 1;
    } else if (Ijump_magnitude <= Ijump_lower){
        DFT_c->jumped_signal = -1;
    } else {
        DFT_c->jumped_signal = 0;
    }

    //update the buffers
    int current_index = DFT_c->current_index;
    DFT_c->circular_buffer_sample[current_index] = new_sample;
    DFT_c->circular_buffer_angle[current_index]  = new_angle;
    DFT_c->circular_buffer_magnitude[current_index] = new_mag;

    //iterate index and "n" by one. If size 30 then ...->28->29->0->1->2->...
    DFT_c->current_index = (current_index+1) % BUFFER_SIZE;
    DFT_c->current_n     = (DFT_c->current_n+1) % (int)N;
    //If a buffer size amount of iterations is done let not_first_run=1
    if (DFT_c->not_first_run == 0 && DFT_c->current_index == 0){
        DFT_c->not_first_run = 1;
    }
}
```

5.3.5 GOOSE publishing

The last part of the DR implementation is GOOSE publishing. GOOSE publishing is done through code in the main() function. The code for GOOSE publishing and the accompanying four ICD files (one per DR) is based upon the "server_example_goose.c" in libiec61850. Keep in mind that for libiec61850 to be able to read ICD files, the ICD file must be compiled into .c and .h files as described in Section B.6.

Each ICD file has two goose control blocks, and each of them has a unique MAC address, a unique AppID, and a corresponding dataset. Each dataset corresponds to either the CCA or IJump algorithm, and in both datasets, there are three DAs to store the current status of the CCA or IJump condition.

After creating a GOOSE server for GOOSE publication in the main() file, the main function enters an infinite loop. The code below is a snippet from this loop, and this code shows how the CCA condition

at DR54 is monitored. In lines 1-4, a helper variable is created. The variable is a Boolean value called bool_now containing the status of the CCA condition based on the value in the DFT struct. Then in line 7, it is checked if bool_now is different than the boolean "IEDMODEL_GenericIO_GGIO1_SPCSO3_stVal". "IEDMODEL_GenericIO_GGIO1_SPCSO3_stVal" is a DA attribute specified in the ICD file, and is used to store the current status of the CCA algorithm for DR54. If bool_now is different, then the DA is updated with the value of bool_now in line 11. Now the GOOSE control block in the ICD file specifies that when this DA changes, there should be a GOOSE published. This is exactly what occurs and explains why there is no function "Publish_GOOSE_meesage".

In line 9, before updating the DA, a DA containing a discrete/integer millisecond with the timestamp is updated. The timestamp is obtained from the R-PI, which is synced using the Network Time Protocol. Additionally, at the start of the simulation, the initial packets from the OPAL-RT were set to define $t = 0$. The DA with the timestamp is a part of the published GOOSE message.

```
1  bool_now = false;
2  if (DFTs[2].change_signal == 1){
3    bool_now = true;
4  }
5
6  //If sentence to check if the CCA condition has changed
7  if (IedServer_getBooleanAttributeValue(iedServer, IEDMODEL_GenericIO_GGIO1_SPCSO3_stVal)
       !=bool_now){
8      //Add a timestamp to when the CCA condition occurred
9    IedServer_updateInt32AttributeValue(iedServer, IEDMODEL_GenericIO_GGIO1_SPCSO1_stVal,
       TimeRelative+add)
10     //CCA condition has changed, update the value in the events dataset to new boolean
11   IedServer_updateBooleanAttributeValue(iedServer, IEDMODEL_GenericIO_GGIO1_SPCSO3_stVal
       , bool_now)
12 }
```

The OPAL-RT will use the same ICD files for GOOSE subscription. For the full Raspberry-PI code and ICD files navigate to Section A.1.

5.4 Mininet implementation on Raspberry Pi

A GOOSE message has now been sent from the R-PI/DR and has arrived at the R-PI, emulating the WAN. Emulation of the WAN communication network is done through the MININET software. In Figure 5.6, the communication network topology implemented in MININET is shown.

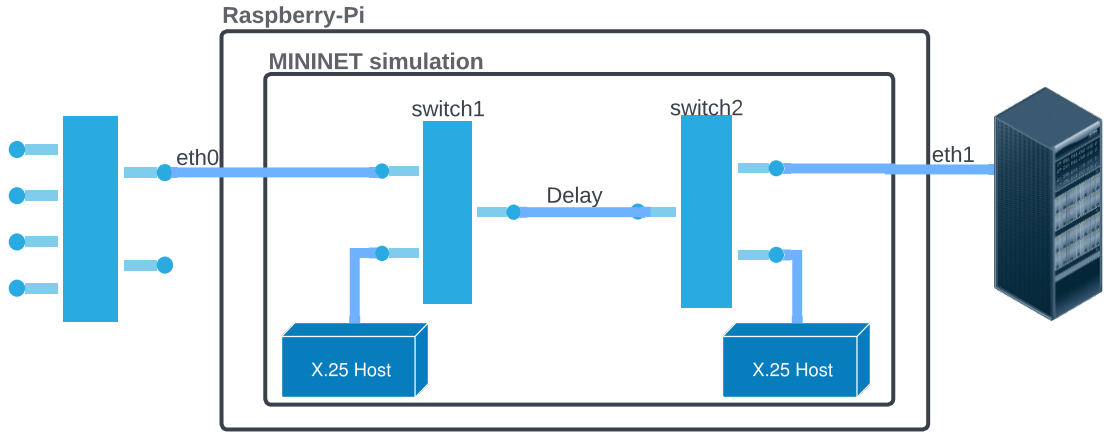


Figure 5.6: Illustration of Mininet implementation on Raspberry Pi

Observe that the emulated communication network consists of two switches, switch1, and switch2. Switch1 is connected to the physical ethernet port ”eth0” which is connected to the physical switch. Switch2 is connected to the physical ethernet port ”eth1” of the Raspberry PI (USB adapter), which is connected to the OPAL-RT. The working function is that all packets arrive at switch1. Switch1 will dump all SV packets, but GOOSE messages are passed to switch2 with a varied fixed delay. The application of the fixed delay is the very simple emulation of the public 4G/5G network. The figure also shows that each switch has a corresponding host. The hosts were used for debugging purposes.

In the discussion, measurements obtained at the 5G laboratory at NTNU will be used. It is important to clarify, that these measurements were just ping measurements where the R-PI was connected to a router in the 5G network. Meaning that the 5G laboratory was not used in the HIL simulation.

5.5 OPAL-RT GOOSE subscription

For the OPAL-RT to subscribe to the GOOSE message, the same four GOOSE ICD files used in the Raspberry-PI are imported into OPAL-RT. This results in the following view in the IEC61850 configuration. $events_{v1}$ (CCA) and $analog_{v1}$ (IJump) correspond to the two goose control blocks per ICD file. Observe that, as previously explained, each control block has a unique AppID and MAC address.

#	SCL file	IED	GOOSE ID	Ethernet Adapter	AppID	MAC address
1	models\Master_simulink_2019b\lib61850....	simpleIO	events_v1	eth2	0x1001	01-0c-cd-01-00-01
2	models\Master_simulink_2019b\lib61850-...	simpleIO	events_v2	eth2	0x1002	01-0c-cd-01-00-02
3	models\Master_simulink_2019b\lib61850-...	simpleIO	events_v3	eth2	0x1003	01-0c-cd-01-00-03
4	models\Master_simulink_2019b\lib61850-...	simpleIO	events_v4	eth2	0x1004	01-0c-cd-01-00-04
5	... karl_master_files\migrate25.02\lib61850...	simpleIO	analog_v1	eth2	0x2001	01-0c-cd-01-00-21
6	models\Master_simulink_2019b\lib61850-...	simpleIO	analog_v2	eth2	0x2002	01-0c-cd-01-00-22
7	... karl_master_files\migrate25.02\lib61850...	simpleIO	analog_v3	eth2	0x2003	01-0c-cd-01-00-23
8	... karl_master_files\migrate25.02\lib61850...	simpleIO	analog_v4	eth2	0x2004	01-0c-cd-01-00-24

Figure 5.7: View in RT-LAB after importing the four ICD-files for GOOSE communication.

For retrieving the GOOSE signal in the Simulink model, an RT-LAB ”OpInput” block is used. The association between the OpInput block and the specific DA in the ICD file is done in the configurator in RT-LAB.

5.6 Central-Relay Implementation

GOOSE messages have now arrived back into the Real-Time simulation where the CR is. Remember that the CR shall find out if there is a fault and then which CB should trip. Figure 5.8 shows the overview of the CR implemented in Simulink. Starting from the left, CCA and IJump GOOSE data is received from the OpInput block. The data is fed into two Matlab function blocks along with the CR settings. The settings are t_{cca}, t_{IJump} and $t_{DR->CR,communication,max}$. The two Matlab function blocks determine if a line is faulty according to the CCA and IJump schemes.

The code to implement these schemes is not as simple as it sounds. For example, as CCA is a blocking scheme it was explained it can only make tripping decisions at a time $t_{cca} + t_{DR->CR,communication,max}$ ago. Therefore the ”Does CCA indicate fault” has a matrix of 12 rows (amount of DRs) and 54 columns (equal to $t_{cca} + t_{DR->CR,communication,max}$ ms). This matrix acts as a large circular buffer keeping track of the CCA-condition. The buffer is updated by using the time stamps of the CCA-GOOSE messages.

Every 1 ms, the CCA and IJump block will output a vector of 6 rows. Each respective row is a boolean

value indicating if a specific line is faulty. The output is passed through an ”OR” block in Simulink which makes the scheme run in parallel. The output of the ”OR” block is then fed into another MATLAB function block. This block uses my proposed algorithm in Section B.1 to determine which CB to trip and then output the correct switchgear signals. The initial values given to this block are the three matrices for the initial topology, CB positions, and LBS positions. The output of the block is switch gear signals. The switch gear signal can open CBs in the simulation with no communication delay. The delay in the communication between CR and CB will therefore be added to the delay between the DR and CR.

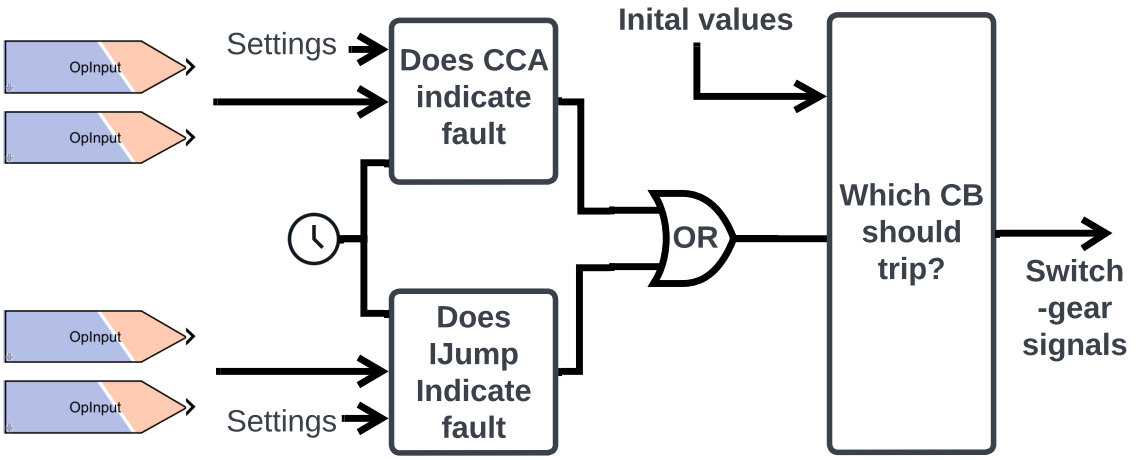


Figure 5.8: Flowchart of the Central-Relay

The CR was coded by me and the interested reader can find the 131 code-lines for the CCA block, 43 lines for the IJump block, and 174 lines for the ”which cb to trip” in the folder ”Code” added to this thesis. Lastly, a picture of the actual CR implementation is shown in Figure 5.9.

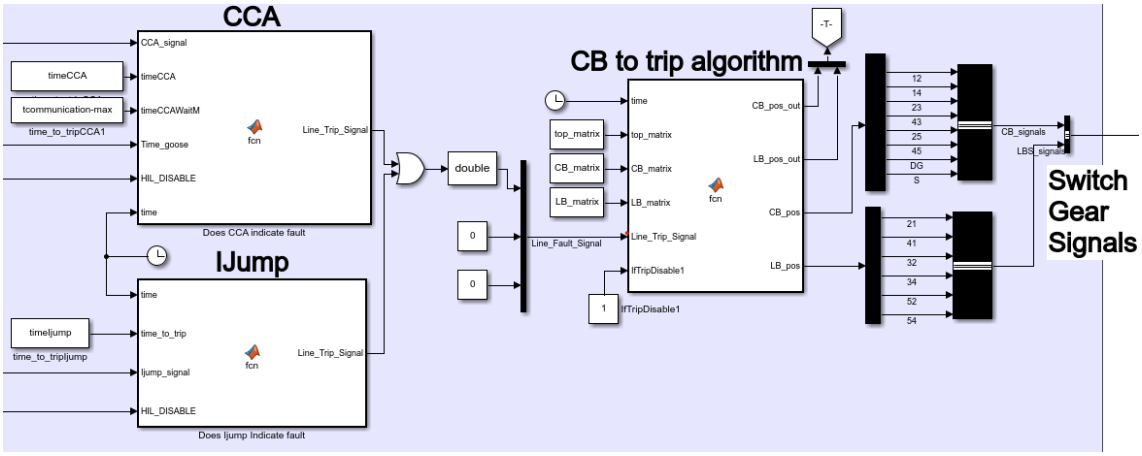


Figure 5.9: Picture of central-relay implementation in Simulink

6 Aggregate results

This section is the first of two chapters representing the evaluation phase. Aggregate statistics for three-phase, two-phase, and cross-country faults will be presented. The aggregated statistics are based on the result of #3420 distinct simulations and are used to quantify the reliability and speed of the proposal. Section 7 will use curve forms to explain and discuss the quantitative results.

Reliability will be evaluated using the terms dependability and security. Dependability is the probability that a faulty line is identified as faulty [103]. Security is the probability that a healthy line is *not* identified as faulty. Logic time will be referred to as the time it takes to *localize* the fault, disregarding WAN delay.

The key result of this section is that. Without IJump in meshed operation, not all faults would be identified and the speed would be slower. Therefore, My proposal of using CCA and IJump in parallel increased dependability and speed in meshed operation compared to using CCA alone. It was unexpected that IJump frequently localizes faults in meshed conditions. In meshed operation, IJumps fault detection capability improves as short-circuit levels decrease, whereas CCA's capability improves as short-circuit levels increase. Consequently, IJump and CCA complement each other.

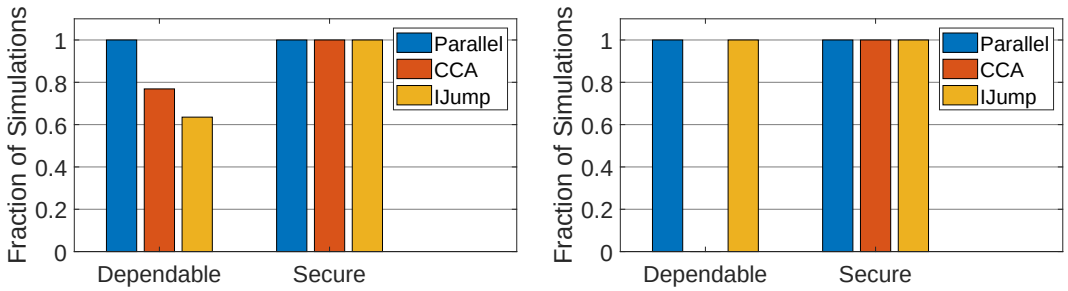
A base case including 120 simulations is defined. The base case includes faults at the start, middle, and end of all 6 lines in the grid presented in Section 4.1. An ABC, AB, BC, and CA fault is simulated at each fault location. LLG faults are not simulated as Section B.3 shows that an LL and LLG fault with the same fault resistance, in an ungrounded system, has a similar PS current. In the base case, all faults are simulated for meshed and radial operation. The base case has WAN emulation turned off, and the load is nominal.

6.1 Varying fault resistance

This subsection presents results corresponding to the base case simulated in grid-connected with IIDG, islanded with IIDG, and islanded with SGDG. The fault resistance will be 0.1 Ω, 1 Ω, 10 Ω or 20 Ω. Resulting in a total of 1440 different fault-scenarios/simulations. Section B.2 explains why 20 Ω is chosen as an *upper limit* for fault resistance and why the value is not realistic for normal conditions.

6.1.1 Low resistance faults and instantaneous phasor

Figure 6.1 shows the dependability and security of the lines operating in "meshed-condition" and "radial-condition" for 0.1 Ω and 1 Ω fault resistance. In radial conditions, parallel operation exhibits 100% dependability due to IJump alone, and it also has 100% security. In meshed conditions, there is also 100% dependability and security. **However, CCA only results in ≈80% dependability. Fortunately, IJump frequently and unexpectedly locates the fault, also when CCA does not.**



(a) "Meshed-Condition" **(b)** "Radial-Condition"

Figure 6.1: Reliability analysis with 0.1 Ω or 1 Ω fault Resistance. #720-sims.

Figure 6.2 shows for which fraction of simulation a given combination of schemes sees the fault in meshed operation. Simulation from Grid-Connected, Islanded with SGDG, and Islanded with IIDG are separate columns. The arrow points toward decreasing fault current level. The top of the red section reveals that CCA's capability to see faults decreases with decreasing short circuit levels. However, the bottom value of the red section reveals that IJumps' ability to see the fault in meshed conditions increases with lower short circuit levels.

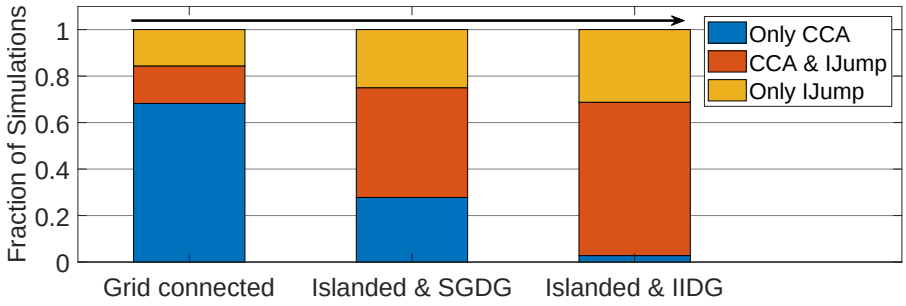


Figure 6.2: Which scheme sees the low resistive fault on a meshed line. Arrow=reducing fault current. #480.

Figure 6.3 shows the logic time (no WAN delay). Bars represent the average time, and diamonds are the max time. The left and right columns are parallel operations. The two middle columns are a specific scheme. The max logic time in parallel operation is 28 ms. **A comparison between the two left columns demonstrates that running the schemes in parallel reduces logic time in meshed operation.** If WAN emulation were activated, the reduction would be larger due to the blocking nature of CCA. The spikes in logic time for BC faults will not be seen in the traditional phasor calculation.

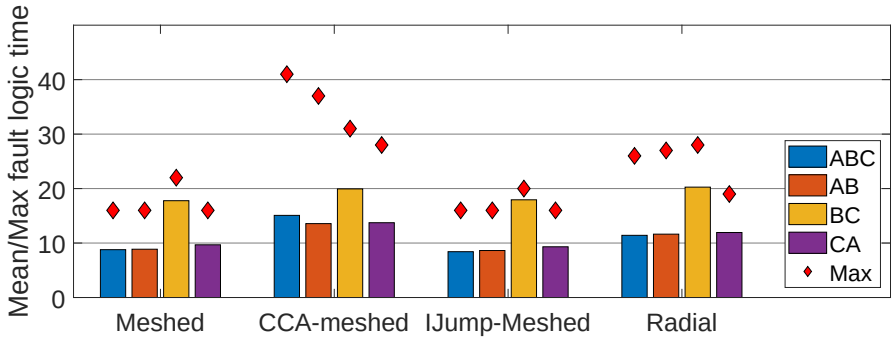
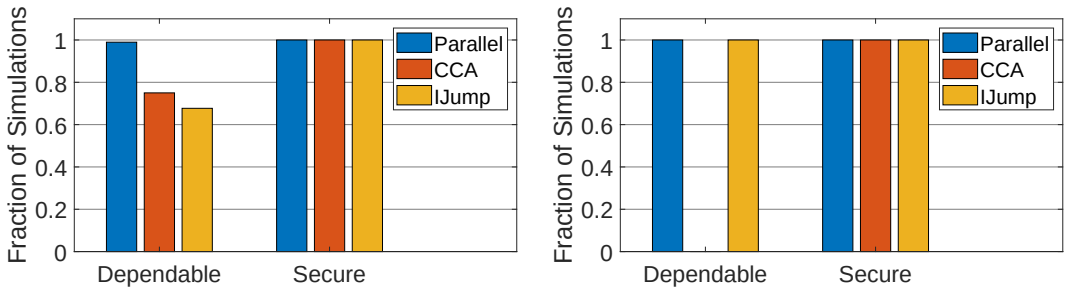


Figure 6.3: Mean and max trip time for meshed and radial elements. Low resistive faults. #720.

6.1.2 High resistance faults and instantaneous phasor

The fault resistance is now 10 Ω or 20 Ω. Compared to the low resistance case, the dependability is only 99 % in meshed conditions. CCA-failure was during grid-connected for fault closest to bus 1. The discussion will conclude that the dependability loss is due to an unrealistic high resistance.



(a) "Meshed-Condition" **(b)** "Radial-Condition"

Figure 6.4: Reliability analysis with 10 Ω or 20 Ω fault resistance. #720.

Concerning the instances of successful operation under meshed operation, Figure 6.5 shows which scheme sees the fault. Compared to the case of low resistance, IJump sees more of the faults. This is yet another case where IJumps fault detection capability in meshed condition improved for lower short circuit levels.

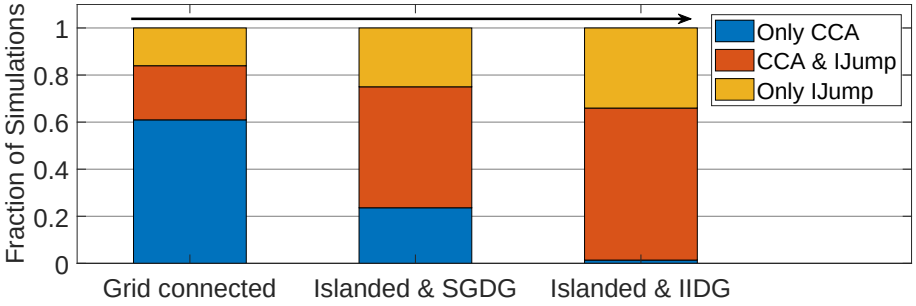


Figure 6.5: Which scheme see the high resistive fault on a meshed line. Arrow=reducing fault current. #480.

Figure 6.6 shows logic time for high resistive fault. Compared to low resistive faults, high resistive fault exhibits a slight rise in average logic time. The maximum value remains at 28 ms.

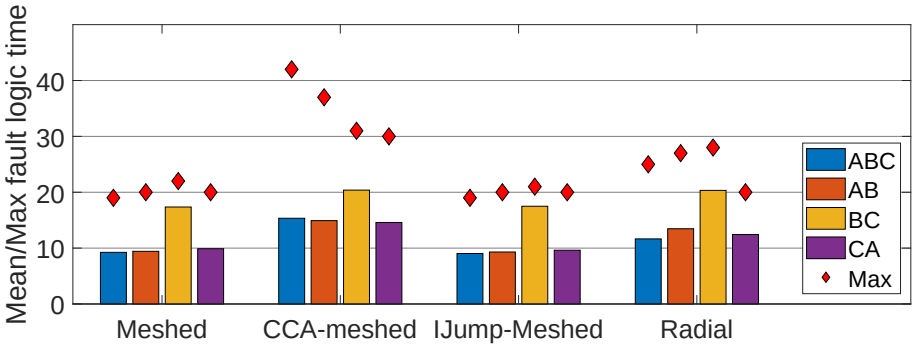
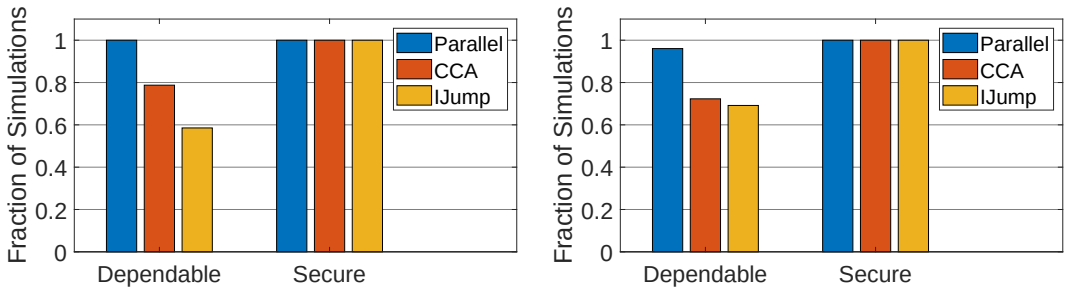


Figure 6.6: Mean and max trip time for meshed and radial elements. High resistive faults. #720.

6.2 Using traditional phasor calculation

Now simulations are conducted with the traditional method of phasor calculation. Keep in mind that this simulation's results are non-HIL, and therefore the DR is located in the OPAL. Concerning reliability in radial and meshed conditions, the traditional method gave no significant difference. CCA is still not seeing all the faults in meshed condition, and CCA is still not 100% dependable for the high resistive case. Therefore, these two phenomena are not due to using a non-traditional phasor calculation method.



(a) "Meshed-Condition", 0.1 Ω and1 Ω

(b) "Meshed-Condition", 10 Ω and 20 Ω

Figure 6.7: Reliability analysis using the traditional method of phasor calculation. #960.

While the reliability results were similar in the traditional and instantaneous methods, the logic time is seen to be very dissimilar. This is noticed in Figure 6.8 where logic time is shown for low resistance faults. Observe how compared to Figure 6.3 the max logic time is only, 18 ms, compared to 28 ms. Additionally, the mean delay for the BC fault does not exhibit a spike as observed in the instantaneous method. Nevertheless, the two columns to the left still demonstrate that parallel operation in meshed conditions decreases logic time.

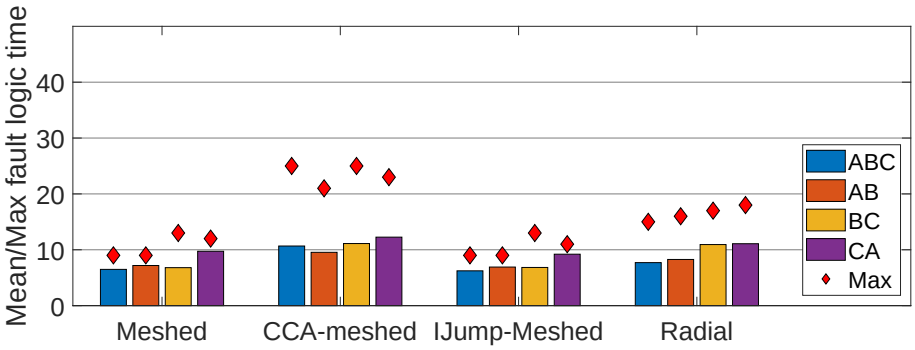


Figure 6.8: Traditional method of phasor calculation. Mean and max trip time for meshed and radial elements. Low resistive faults. #720.

Figure 3.3 in Section 3.2 showed the difference in calculation steps between the instantaneous and traditional methods. The execution times of this calculation steps are given in Table 6.1. The values were obtained by implementing the linear interpolation, the real sum, and the complex sum on the Raspberry PI in C-code. For the DFT algorithm, the already implemented C-code was used. The *average* time measurement was then done during HIL execution for the base case with the timing function in the ”clock.h” library.

The values to the left of the black bar in the table show the average execution time for the individual algorithms. It is seen that the DFT is the most computationally intensive step. The time needed for each algorithm in the traditional and instantaneous method is shown to the right of the black bar. Observe how the instantaneous method is 2.5 µs faster.

Table 6.1: Average time needed for the algorithms that are different in the instantaneous and traditional methods. To the left of the black bar are measurements and the right values are derived from the measurements.

Algorithm	**Time [µs]**		**Time needed for traditional [µs]**	**Time needed for instantaneous [µs]**
2x interpolation + real sum	0.7		0	0.7
1x DFT iteration	1.1		3.4	1.1
1x complex weighted sum	0.8		0.8	0
Total			4.3	1.8

6.3 Large frequency deviation

The base case is now run with: 57.2 Hz, islanded with IIDG, and a fault resistance of 1 Ω and 5 Ω. 57.2 Hz is used because, within the range [40 Hz, 60 Hz], Section 3.2.1 identified it as the worst case frequency when frequency estimation is enabled. Only islanded mode is simulated as Section 3.7.3 explained that it is only then so large deviation can occur.

The results exhibit 100% dependability and 100% security for both meshed and radial operation with the crude frequency estimator turned on. When turning off frequency estimation at this frequency, the scheme was 100% secure and only 97% dependable in meshed operation. Additionally, pre-fault, it continuously sent GOOSE messages.

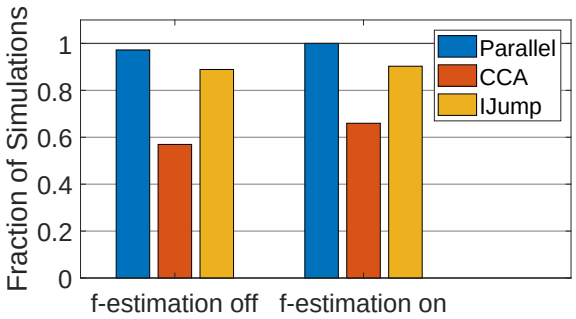


Figure 6.9: Dependability with & without f-estimation at meshed islanded IIDG operation at 57.2 Hz. #240.

6.4 Pre-fault line flows with low power factor

To evaluate the reliability when pre-fault line flow has a pf near unity, the base case is run for grid connect and islanded mode with IIDG. The fault resistance is 1 Ω. The load at bus five is updated to inject a reactive power equal to what was the active power, and it will consume an active power previous to what was its reactive power consumption. Hence, bus 5 acts like a capacitor bank with a pf of 0.1. Due to the symmetry of the simulated topology, this is also the pf of the flow through line-section 2-5 and 4-5. The results of the simulation are shown in Figure 6.10. The important difference, compared to the other result, is the dependability in meshed conditions. Observe how the dependability in meshed conditions is less than 100%. The dependability loss is for faults at lines 4-5 and 2-5. These are also the lines with near unity pf flow.

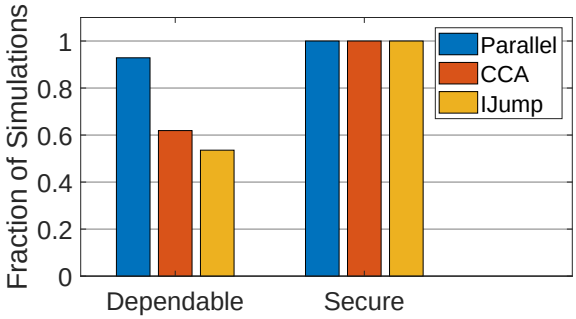


Figure 6.10: Dependability in meshed conditions with a near unity power flow at line 4-5 and 2-5. #240

6.5 Cross country faults

A situation with two earth faults on different phases at different lines/buses in the grid is known as a cross-country fault. To evaluate the reliability of cross-country faults, faults are simulated at the *locations* of the base case. Furthermore, faults are simulated for grid-connected and islanded & IIDG operation in both radial and meshed configurations. An A-Ground, B-Ground, and C-Ground faults are simulated in consecutive simulations. Additionally, a fault on another random line and another random phase are simulated for each simulation. The above case was simulated using fault-to-ground resistances of 10 Ω and 20 Ω. In Figure 6.11, the results are shown. In 99 % of the simulations, at least one of the faults is observed. Regrettably, only 55 % of the simulations detected both faults, which falls below the desired level of 100 %.

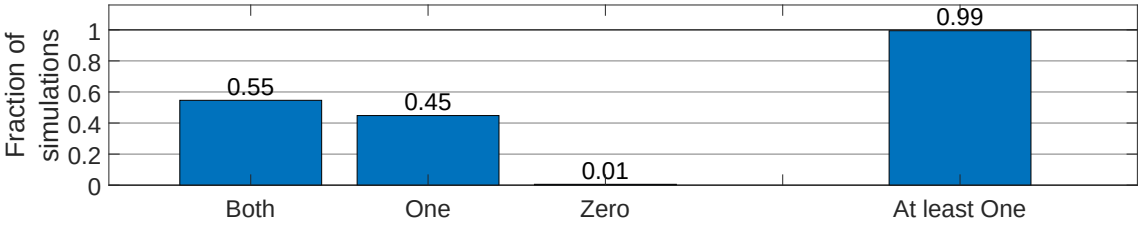


Figure 6.11: Fraction of simulations detecting both, one, or zero faults in a cross-country fault. #540.

7 Discussion on the aggregated results

In this phase of the evaluation, an explanation and discussion of the aggregate results are conducted. The discussion is divided into factors that affected the aggregate result and those that did not. For each factor, the approach will show curve forms from specific faults to develop a theory of how the scheme works. To achieve this objective, the discussion is extensive. As the meshed operation had the most unexpected results, the focus is on the meshed operation. Emphasis is also put on how my proposals increased performance. Furthermore, each subchapter will start with a recap of relevant observations from the results. The chapter consists of the following subsections:

Factors that did affect the aggregate results

- **Section 7.1**. Transient or a steady-state drop in current magnitude is why IJump localizes faults in meshed conditions. Transient drops decrease logic time, and steady-state drops increase reliability.
- **Section 7.2** Compares the instantaneous and traditional method of phasor calculation. Concluding that the traditional method is the most beneficial.
- **Section 7.3**. My requirement and implementation of a crude frequency estimator is the reason for 100 % dependability during large frequency excursions.
- **Section 7.4**. Without my proposed t_{CCA} and t_{IJump}, the reliability results would be worse. They handle unsynchronized sampling and clock, measurement error, and small line charging current.
- **Section 7.5**. Observed reduced reliability in meshed operation was because of too high fault resistance.
- **Section 7.6**. Load modeling cause uncertainty with respect to the IJump-magnitude on the far end.
- **Section 7.7** For line flows with a pre-fault power-factor near unity, the scheme has reduced reliability.
- **Section 7.8** Only one fault in a Cross-Country fault is detected due to the current transiting towards the other faults. Per-phase implementation solves this issue.

Factors that did <u>not</u> affect the aggregate results

- **Section 7.9**. Identifies that very large capacitive charging current relative to the line current will decrease reliability. To prevent false trips, $I_{CCA,disable}$ is proposed.
- **Section 7.10** 4G/5G networks are a feasible solution. However, using them in a plug-and-play manner will cause a communication delay that can impede DG-LVRT capability.

7.1 IJump sees meshed operation faults from transient/permanent magnitude drop

The aggregate result in Section 6.1 established that IJump frequently and unexpectedly locates the fault in meshed operation. IJump behavior during meshed conditions increased reliability and speed. It was seen that IJumps fault detection capability in meshed conditions improves as short-circuit levels decrease, whereas CCA's capability improves as short-circuit levels increase. Section 6.2 established that the unexpected IJump behavior has nothing to do with using the instantaneous method. The objective of this subchapter is to explain why IJump sees faults in meshed conditions.

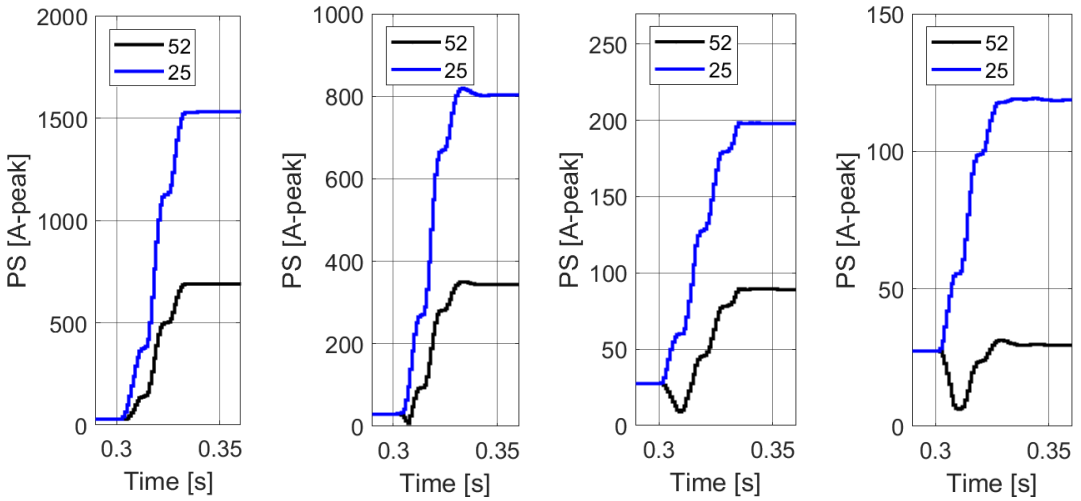
At the faulty line end, with pre-fault energy flowing into the line, no CCA is expected. At this line end, the post-fault current is expected to be larger than the pre-fault. However, it will now be explained that the current *can* reduce and activate IJump in meshed conditions at the faulty line end with the anticipated CCA-condition. For this line end, three possible scenarios are introduced in the bullet points below. Scenario I is the expected scenario. Scenario II and Scenario III are unexpected and will be explored further.

- **Scenario I:** At the end with an anticipated CCA-condition, a high short circuit level cause the post-fault magnitude to increase continuously to the new steady-state condition. CCA sees the fault. IJump does not see the fault.
- **Scenario II:** At the end with the anticipated CCA-condition, the short circuit level is now lower. There is a sufficient CCA-angle, but there is also a *transient* decrease in the current magnitude. CCA and IJump typically see the fault. Parallel operation cause reduced tripping time.
- **Scenario III:** The short circuit at the line end with the anticipated CCA condition is very low. The *PS current magnitude*, not necessarily the current magnitude, has a steady-state value post-fault that is less than pre-fault. Only IJump sees the fault, not CCA.

7.1.1 Scenario II: Examples of the transient decrease in calculated PS current magnitude

To demonstrate scenario II, faults are simulated at the midpoint of line-section 2-5 in meshed operation. In Figure 7.1, the resulting PS current magnitudes on both ends of the faulty line are shown. The figures are arranged in descending order based on the short circuit level. Observe:

- In Figure 7.1a, the 3ph fault in grid-connected mode caused both sides of 2-5 to have increased PS current immediately after the fault. Therefore, IJump doesn't detect the fault.
- In Figure 7.1b, the 2ph fault in grid-connected mode caused the side near bus 5 to have a transient decrease in PS current. IJump did not detect the fault as the period under ϵ_{down} was shorter than t_{IJump}.
- In Figure 7.1c, the 3ph fault in islanded mode caused the side near bus 5 to have a transient decrease in PS current. IJump detected the fault before CCA.
- In Figure 7.1d, the 2ph fault in islanded mode caused the side near bus 5 to have a transient decrease in PS current. IJump detected the fault before CCA.



(a) ABC. Grid connected **(b)** AC. Grid connected **(c)** ABC. Islanded & IIDG **(d)** AC. Islanded & IIDG

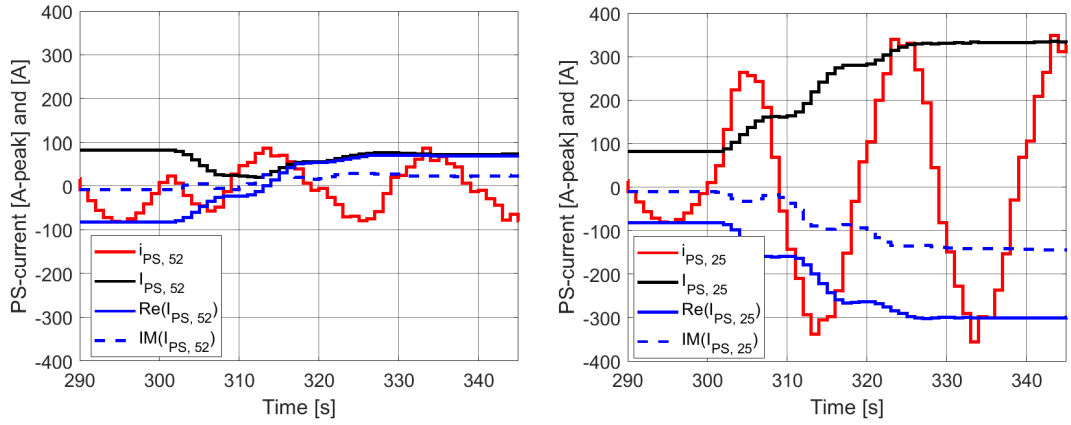
Figure 7.1: PS-Current magnitude at a faulty line in meshed conditions. ABC, Meshed, IIDG, 2-5 midpoint faults, Measuring at 25 and 52.

From the figures, it is the line end with the anticipated CCA-condition, which has the transient decrease in current. The transient decrease in current is the most substantial for lines with lower short circuit levels. Both of these factors are fundamental when understanding the explanation of the transient decrease.

7.1.2 Scenario II: Explaining why the transient decrease occurs on the line end with the anticipated CCA-condition and low fault current

The faulty line end with a CCA-condition experiences a rotation in the PS phasor. If the rotation is substantial, the real and imaginary parts of the current phasor change polarity. When this occurs, the phasor's real and imaginary values go through zero. During the period in which they approach zero, the calculated current magnitude can be low. Furthermore, according to Equation 9 in Section 3.2.2, the quantity driving this change is $x_n - x_{n-N}$. Therefore for a greater fault current (greater $x_n - x_{n-N}$), this transition occurs faster. Thereby lesser transient drop with increasing post-fault current magnitude.

Figure 7.2a illustrate the above explanation. It shows the DFT calculation done in the Raspberry-PI for DR-52 for the fault in Figure 7.1d. As DR52 has a CCA-condition, it is seen that the red line, which shows the instantaneous PS current, skips a positive polarity amplitude around 300 ms. Furthermore, the blue solid and dotted lines show the imaginary part and real part of the PS phasor. Observe how both the real and imaginary part change polarity. At the time of polarity change is when the current magnitude drops (black line). Now, look at the other line end in Figure 7.2b, which did not have a substantial change in PS current angle. Therefore it does not have a polarity decrease so that the phasor magnitude continuously increases.



(a) At 25. CCA-condition.

(b) At 52. no CCA-condition.

Figure 7.2: PS instantaneous current and magnitude at a DR with and without CCA-condition. ABC, Meshed, Islanded & IIDG, 2-5 midpoint faults, Measuring at 25 and 52.

The reader should remark that the explanation required a significant rotation of the PS-phasor for the transient decrease in PS current magnitude. Therefore scenario II is not the scenario that increases the amount of fault seen (dependability). However, the aggregate result showed that when IJump sees faults in meshed conditions, it is typically faster than CCA. Therefore, the transient decrease in calculated current causes reduced tripping times. Additionally, as explained in Section 3.1.3, because of the permissive nature of IJump and the blocking nature of CCA, the reduction in tripping times will be even more substantial when considering the WAN communication delay.

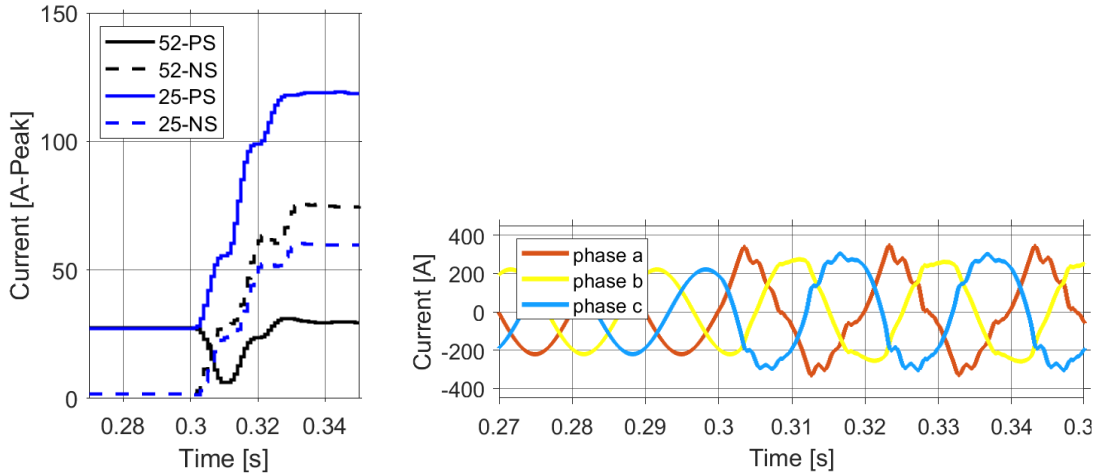
7.1.3 Scenario III: Explaining PS magnitude reduction does not imply, current magnitude reduction of the faulty phases

Scenario III requires a PS current magnitude that is lower at a post-fault steady state compared to pre-fault in meshed conditions. As meshed conditions imply that both faulty line ends can be supplied by fault current, this scenario is counter-intuitive. However, In the context of an unbalanced fault, a diminished PS current does not imply a reduction in the current magnitude of the faulty phases. Rather, it also depends on the

value of the NS current. This possibility explains why scenario III was mainly seen for two-phase faults.

Consider, for instance, Figure 7.1d, which illustrates equal magnitudes of pre and post-fault positive sequence current for DR52. In Figure 7.3a, the PS and NS for DR52 in this scenario are shown. Clearly, there is an increase in current, evidenced by the substantial increase in the NS current. As the two faulty phases experience a change in direction at this line end, an NS current greater than PS is not unexpected. What is unexpected is that the current level can be so low that the PS current does not increase.

Note that the negative sequence current seen is attributable to the topology, not the IIDG contribution. The IIDG supplies a symmetric PS current even though it is an unsymmetrical fault, as demonstrated in Figure 7.3b. To avoid reader confusion, it's worth noting despite pre-fault IIDG with 1 pu current, the post-fault is much higher than 1.2 pu (thermal limit). This is because the voltage drop cause less of the current to flow through the loads, as witnessed by Figure 7.3b showing the IIDG to be limited to 1.2 pu.



(a) PS and NS for the AC fault

(b) IIDG current injected into 22 kV grid.

Figure 7.3: PS and NS current magnitude at 25 and 52, and IIDG fault contribution. AC, Meshed, Islanded & IIDG, 2-5 midpoint faults, measuring at 25, 52, and at IIDG.

7.1.4 Scenario III: Why did non of the referenced scheme observe CCA failure?

An important question is why non of the referenced scheme on CCA report on the failure of CCA. One reason might be that CCA failure was only witnessed under scenario III. It has been explained that for scenario III to occur, the line-end with the anticipated CCA condition must have a low fault current level. For example, Figure 6.5 shows that islanded with IIDG and islanded with SGDG are the most common situations with CCA failure. These two cases only have one fault current source in the meshed grid. However, [104] only included a single line with power generation at both ends. [50, 62] had a ring system of three buses with all the buses having power infeed. Therefore, I hypothesize that the referenced articles did not experience CCA failure as they had higher short circuit levels.

There are three comments I want to make. First, the referenced article would have performed better with IJump in parallel because they would still experience scenario II, where IJump causes faster tripping times. Second, while not observed, it cannot be excluded that scenario II could cause a CCA failure. Say if the CCA-angle reaches only 89°. Third, the case of only one source of fault current is particularly relevant for Norway. Due to the many large distributed hydro generators capable of feeding a significant local community.

7.2 Instantaneous method versus the traditional method of phasor calculation

The aggregated results demonstrated that the instantaneous method exhibits similar reliability as the traditional method. However, the instantaneous method had a noticeable increase in fault logic time, with a maximum additional delay of 10 milliseconds compared to the traditional method. In terms of computational performance, the absolute difference was negligible.

The goal of this subchapter is to use these findings to discuss if the instantaneous or traditional method of phasor calculation should be used. This will be accomplished by examining both transient and steady-state performance, as well as considering computational efficiency. The transient state refers to the period between pre-fault and post-fault steady states. Post fault steady state is important, as in the interval between fault initiation and CB arc extinction, no healthy lines should be tripped.

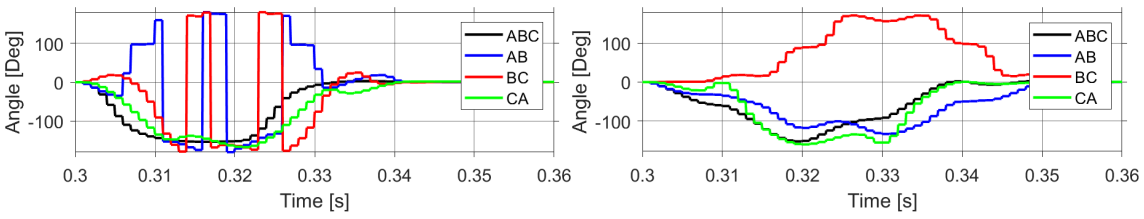
7.2.1 Difference in transient performance in the instantaneous and traditional method

The reason why the aggregated result showed that the instantaneous method has longer trip times, is because Equation 6 shows that phases B and C are time-delayed in the PS instantaneous current calculation.

Furthermore, the time delay also explains why only the instantaneous method had spikes in fault logic time for BC faults. Because BC-fault is the only two-phase fault where both the faulty phases have a delay. In the traditional method, a BC fault has an immediate impact on the PS-phasor. However, in the instantaneous method, the PS-phasor is not affected by the faulty phases until 6.66 ms after fault initiation.

While the evaluation showed equal reliability, I expected the instantaneous method could perform worse. This is because at 50 Hz power system frequency, Section 3.4 explains that the pre and post-fault steady state PS current phasor is equal in both methods. Therefore the change in PS angle and magnitudes between the pre and post-fault steady state is equal in both methods. However, due to the time delay, the transition between the steady states is slower in the instantaneous method, which yields a smaller cycle-by-cycle angle and magnitude change. A smaller IJump-magnitude and CCA-angle lowers the sensitivity in the instantaneous method, but it did not reduce the reliability. The reason why the sensitivity reduction in the instantaneous method did affect the reliability might be that in both methods, the CCA-angle and IJump-magnitude surpass ϕ_{CCA}, ϵ_{up} and ϵ_{down} with a large margin.

Figure 7.4 is used to show the lower sensitivity. It shows the CCA-angle on a line end with a CCA-condition. Both calculation methods and the four fault types are shown. As expected, observe the lower sensitivity in the instantaneous method demonstrated by the lower absolute CCA-angle in the right subplot.



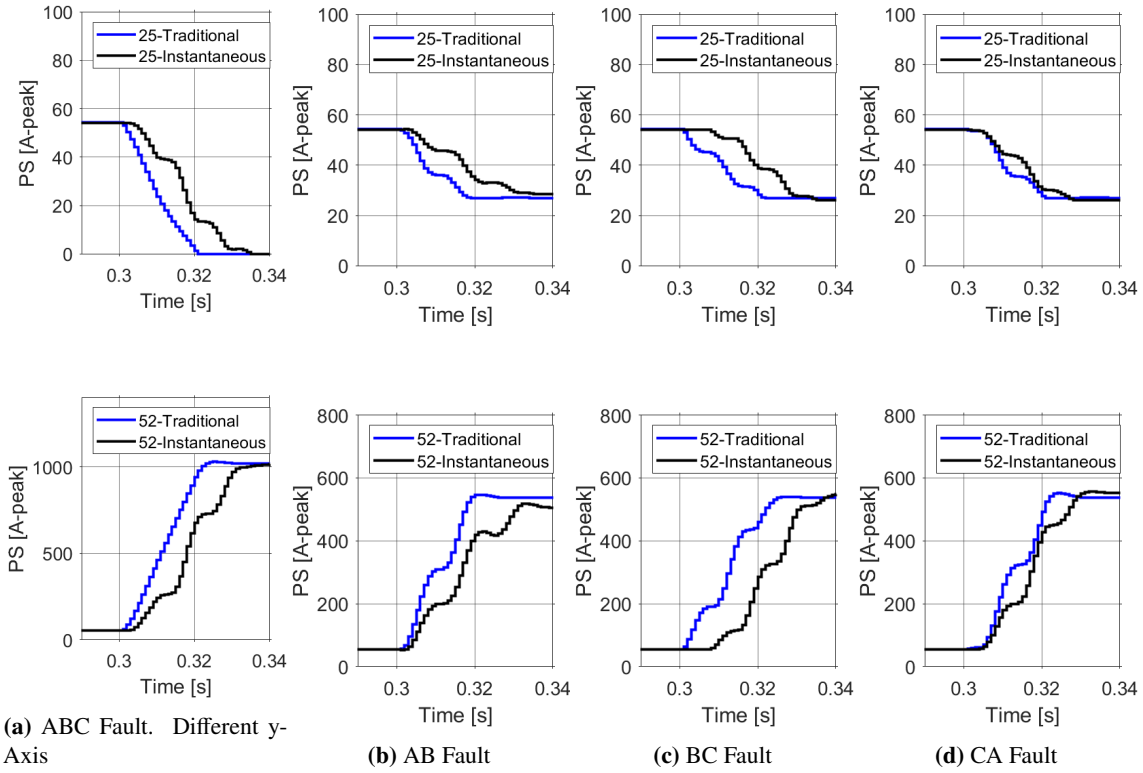
(a) CCA-angle (Traditional)

(b) CCA-angle (instantaneous)

Figure 7.4: CCA-Angle in the traditional and instantaneous method. All fault types, meshed, grid-connected, 4-5 midpoint faults, measuring at 54.

As was the case for CCA, Figure 7.5 shows the instantaneous method causes IJump to have lower sensitivity. First, observe how the black line (instantaneous) is a time-delayed version of the blue line (traditional). Also, the magnitude difference between pre-and post-fault steady is equal in both cases. Except for the BC fault, the PS magnitude is affected right after the fault in both methods, but in the instantaneous method, it

settles at the same value later. Therefore, IJump has lower sensitivity in the instantaneous method.



(a) ABC Fault. Different y-Axis **(b)** AB Fault **(c)** BC Fault **(d)** CA Fault

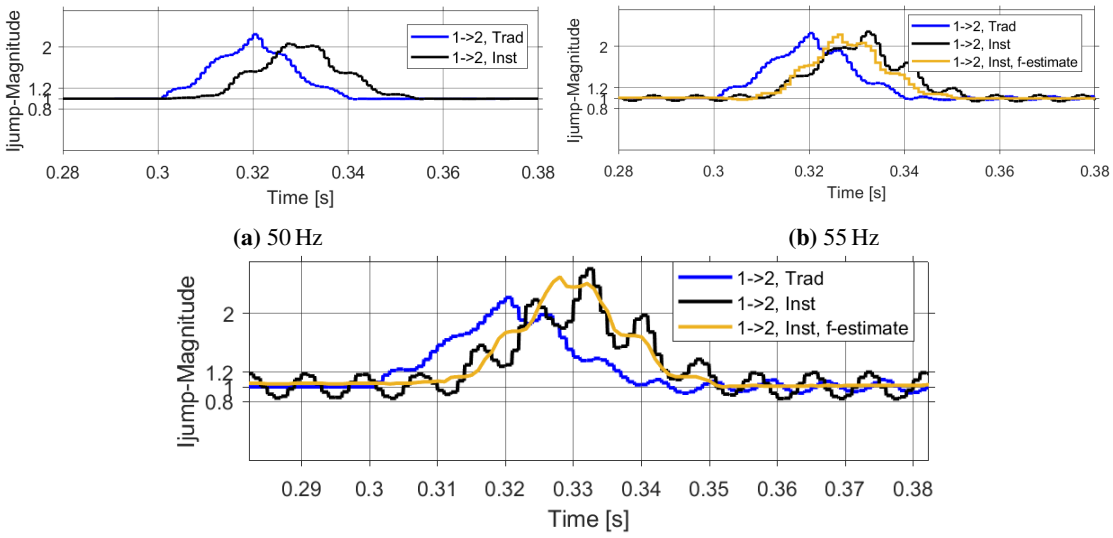
Figure 7.5: PS magnitude in the traditional and instantaneous method. All fault types, radial, grid-connected, 2-5 midpoint faults, measuring at 25 and 52.

7.2.2 Difference in pre-fault and post-fault steady-state performance

Steady-state performance is about not tripping healthy lines. The aggregates results had 100 % security at nominal and at off-nominal frequency. However, it was pointed out that in the off-nominal case, the instantaneous method, without frequency estimation, sent a continuous stream of GOOSE messages pre-fault for large frequency deviation. Now the continuous stream of GOOSE messages will be explained to be a result of the *calculated* oscillations caused by spectral leakage. Section 3.4.3 showed that the oscillations worsen with increasing frequency deviation and that they are caused by $\mathbf{I}^*_{\approx\mathbf{NS}} \neq 0$.

To illustrate that the theory is true, BC faults are now simulated at different pre-fault frequencies, and IJump-magnitude at a healthy line is shown in Figure 7.6. Keep in mind that the focus is on what occurs pre-fault and after the fault transient. At 50 Hz in Figure 7.6a, there are as expected, no oscillations either pre or post-fault due to $\mathbf{I}^*_{\approx\mathbf{NS}} = 0$. Furthermore, only the traditional method never has any oscillations pre-fault as the equation, in theory, giving the calculated phasor value in this method uses the actual NS current ($\mathbf{I}^*_{\mathbf{NS}} = 0$). In Figure 7.6c, the oscillation in the instantaneous method surpasses ϵ_{up} and ϵ_{down} both pre-fault and post-fault. For the traditional method, this only occurs post-fault in 60 Hz. When surpassing the limit, all line ends will send false goose messages.

These goose messages will not cause a trip, but they will break with the principle that GOOSE should only be communicated in case of a potential fault. As expected, the plots show acceptable performance when using the crude frequency estimator.

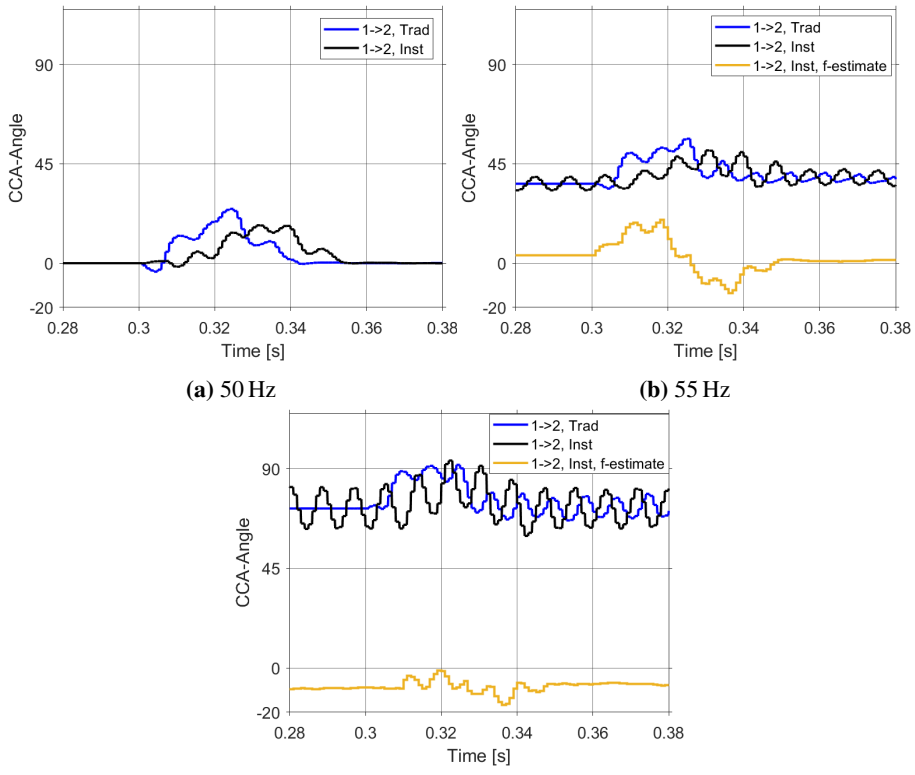


(a) 50 Hz **(b)** 55 Hz

(c) 60 Hz

Figure 7.6: Observing spectral leakage in IJump-magnitude by simulating different power system frequencies. With and without f-estimation. BC, radial, Islanded & IIDG, 1-4 midpoint faults, measuring at 12.

For CCA, the oscillations in the calculated PS current caused by the NS current are not the problem. The major problem is rather that in both methods α_1, introduced in Section 3.4, causes a 7.2° *calculated* angle rotation per Hz deviation per cycle. α_1 is common to both calculation methods so that at a sufficient frequency deviation, the CCA-angle in both methods at steady is either close or surpasses 90°. Nevertheless, Figure 7.7c shows that with the required frequency estimation, α_1 is of no problem.



(a) 50 Hz **(b)** 55 Hz

(c) 60 Hz

Figure 7.7: Observing spectral leakage in CCA-Angle by simulating different power system frequencies. With and without f-estimation. BC, meshed, Islanded & IIDG, 1-4 midpoint faults, measuring at 12.

7.2.3 Difference in Computational performance

The result showed the difference in execution time of the steps that are different in the methods. The findings were that the instantaneous method calculates the PS-phasor only 2.5 µs faster. As the method has a total of 1000 µs between samples, the 2.5 µs time save is negligible.

7.2.4 Conclusion: Use the traditional method

Compared to the traditional method, the instantaneous method causes longer trip times and has less sensitivity. The sensitivity loss did not impact reliability. As frequency estimation is required for both methods, their steady-state performance is similar. With the exception of negligible better computational performance, the instantaneous method lacks advantages. Consequently, further research should use the traditional method.

7.3 Large Off-nominal frequency conditions requires crude frequency estimation

In Section 6.3, it was seen that without frequency estimation, the scheme is not dependable in meshed operation. The reason for this is illustrated in Figure 7.8. In the figure, a three-phase fault is simulated at DR14, which should have a CCA condition. The pre-fault condition is a large frequency deviation of 5 Hz. The dotted blue lines show that without f-estimation, DR14 does not detect the fault. Accordingly, the fault is not recognized. However, the solid lines, which are the result of using frequency estimation, have an ideal performance.

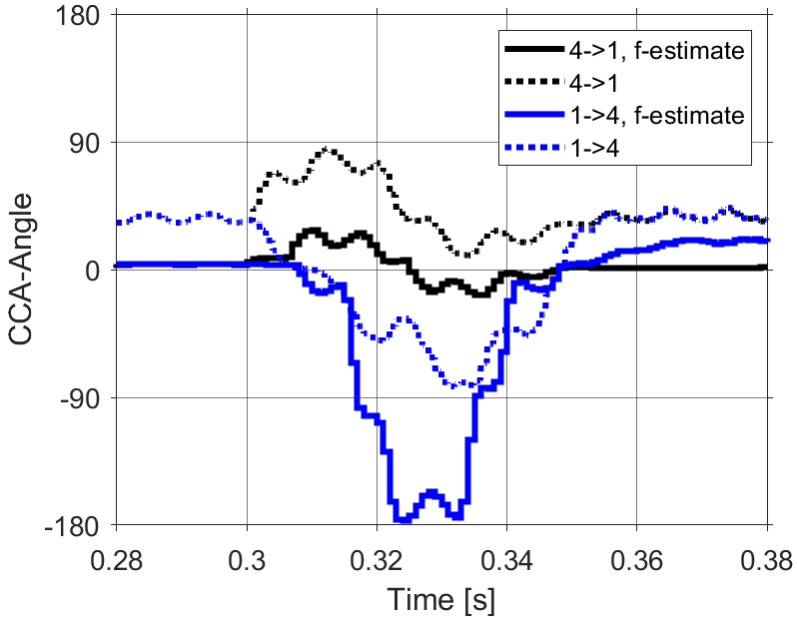


Figure 7.8: CCA-angle with and without frequency estimation on a faulty line where f=55 Hz. ABC, Meshed, Islanded & IIDG, 1-4 midpoint fault, measuring at 14 and 41.

The reader should be well acquainted with the reasons for bad behavior during no f-estimation. In this case, it is the α_1 in that results in CCA-angle of 7.2° per Hz deviation per cycle. As the frequency deviation was positive for the obtained result, the calculated error in the CCA-angle is 7.2° and not −7.2° per Hz deviation. This clarifies why, in the absence of frequency estimates, the dotted lines appear elevated compared to the solid lines in Figure 7.8.

7.4 Unsynchronized sampling and clock, measurement error and small line charging current

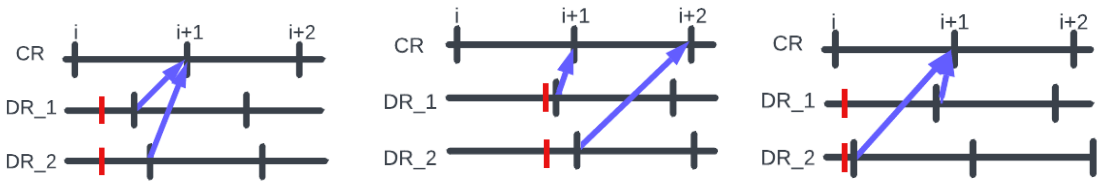
In Section 3, I proposed the use of t_{CCA} and t_{IJump}. They specify that CCA- or IJump-condition must be true for the specified time to cause a fault classification. It will now be seen that these two settings solve the issue of unsynchronized sampling, unsynchronized clocks, measurement error, and small-line charging current. Measurement error was not modeled, but the three other factors would have reduced the obtained reliability in the aggregated results if not t_{CCA} and t_{IJump} were used.

7.4.1 Why DRs having unsynchronized sampling times is a problem without t_{CCA}

Section 5 remarked that the CR does its algorithm every 1 ms. The DR does its algorithm every time a new sample comes in, which is approximately every 1 ms. Unsynchronized sampling times mean that even though the time between samples is equal for DRs and CR, non of them samples at the exact same time. Now it will be explained why this can cause CCA to trip healthy lines if t_{CCA} is not used.

Figure 7.9 illustrates the timeline of the sampling processes. The top row represents the CR, while the two bottom rows represent two DRs across the same line. The x-axis is the time axis and the black bars represent the time of sampling. The vertical red line is the physical time the CCA condition occurs, which, in this instance, is simultaneous for both DRs. The blue arrow starts when a DR detects the CCA condition and extends to the earliest possible instance the CR can sample the published GOOSE message. Consider:

- In Figure 7.9a the DRs timestamp the moment of CCA at the same time, and the GOOSE message arrives at the CR at the same time. Correct working function ensues independent of t_{CCA}.
- In Figure 7.9b the DRs timestamp the event at the same ms value, but the GOOSE message is sampled by the CR at different times. Therefore at the timestep ”i+1” it sees a CCA condition. However, the setting t_{CCA} means that it can never trip for a time earlier than t_{CCA} ago. Therefore it waits for a time t_{CCA}, and then it looks back to see if it should trip. During that time, the second GOOSE message arrives, blocking the trip of the healthy line.
- Figure 7.9c illustrate the GOOSE message arriving at the same moment in the CR. However, due to DR sampling, they have different ms precise time-stamp. Nevertheless, as $t_{CCA} > 1$ ms this does not cause a trip of the healthy line as the CR detects the CCA-condition to be true only for 1 ms.



(a) t_{CCA} is not needed. **(b)** t_{CCA} is needed. **(c)** t_{CCA} is needed.

Figure 7.9: Illustrating the effect of unsynchronized sampling. The CR sample subscribed GOOSE from both ends of the healthy line at different times or at the same time with different GOOSE-timestamp.

When the point of sampling is *independent* between DRs, the situation in Figure 7.9c would occur 50% of the time. However, in the HIL simulation, it occurred very seldom. This is explained by the fact that the OPAL-RT publishes all SV packets at the same time. Therefore the sample time of the R-PIs is *dependent*

and occurs simultaneously. This is seen in Figure 7.10 where Wireshark is used on the Ethernet port of R-PI1. The right box shows that the four distinct packets should be subscribed by R-PI1, R-PI2, R-PI3, and R-PI4, respectively. The left box in the figure shows that all four packets arrive at 118.03 ms.

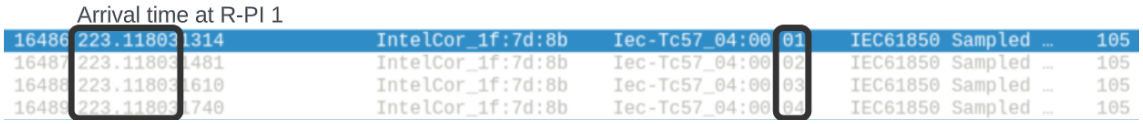


Figure 7.10: Wireshark on R-PI1 showing the arrival of SV from the OPAL-RT. All four arrive with less than a 0.01 ms time difference.

Lastly, it was seen that the problem here was the delay of the second signal that should block the operation. As IJump is a permissive scheme, it does not encounter this problem. Nevertheless, the algorithm must be aware that a GOOSE with the same timestamp can arrive at different times in the CR. Using t_{IJump} takes this into account.

7.4.2 Why unsynchronized clock is a problem

In my implementation, it is assumed that the clock in the DRs has a ms precision. Two events occurring at the same time can then, in theory, be timestamped with 2 ms difference. If a line with CCA condition on both ends then has a GOOSE message with a timestamp difference of 2 ms, $t_{CCA} > 2$ ms is required to prevent trips of healthy lines.

7.4.3 The effect of measurement error and small capacitance line charging

Measurement errors and small capacitive line charging currents can also cause lines with CCA on both ends to have different timestamps. HIL simulation with non-secure trips due to a small capacitive line charging current made me discover the need for t_{CCA}.

Measurement errors and capacitance line charging leads to a slight variation in the current at either end of the line. As a result, there will be a difference in the calculated positive sequence angle at both ends. During a fault, this means a different calculated CCA-angle. In the case of a CCA condition on both ends of a healthy line, it might mean that the DR gives different ms precise time stamps even though they sample at the same time. Figure 7.11b exemplify this and without t_{CCA} it would result in trip.

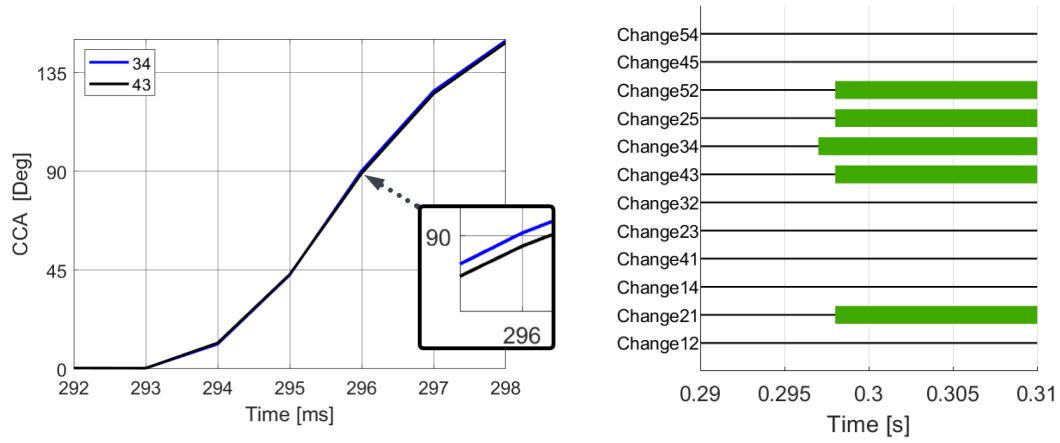
(a) t_{CCA} is not needed

(b) t_{CCA} is needed

Figure 7.11: Explaining the effect of small-capacitive line charging. DRs from the same healthy line.

Lastly, simulation results will be presented to show that my solution works. Figure 7.12a, depicts the CCA-angle on a healthy line taken from two raspberry-PI after HIL simulation. Figure 7.12b, depicts the fault logger in the CR. The simulated fault is at line 1-2, and the healthy line 3-4 should have a CCA on both

ends. In the left figure, the blue line shows that at sample point 296, a CCA condition is detected for DR34, not DR43. This is due to capacitive line charging included in the grid. DR43 only becomes aware of the CCA conditions at sample point 297. In the right figure, this is reflected by the fact that the CR recorded a CCA-angle for 34 before 43. Observe this by looking at "Change34" and "Change43". Nevertheless, as I have used t_{CCA} equal to 4 ms, it did not cause a trip and therefore did not show up as reduced security in the aggregated results.



(a) CCA-Angle recorded by DR34 and DR43.

(b) CR fault logger. Green = CCA-Condition.

Figure 7.12: Line charging current cause the DRs of healthy line 3-4 to detect CCA-condition at different times. t_{CCA} prevents trip in the HIL simulation. ABC, meshed, 1-2 midpoint fault, measuring at 34 and 43.

7.5 How fault resistance influence CCA

The aggregate results showed high reliability for a wide range of simulated fault resistance. However, there were a few cases where high resistance faults near bus 1 in grid-connected resulted in a loss of dependability. The objective of this section is to first explain that the cases with loss of dependability had unrealistically high fault resistance. The second objective is to explain how CCA is impacted by increasing fault resistance, thereby explaining the reason why the unrealistic high fault resistance caused CCA failure.

7.5.1 Explaining that the simulation with CCA failure had unrealistically high fault resistance

The maximum fault resistance was calculated in Section B.2. When finding the max fault resistance, emphasis was put on the low fault current levels during Islanding with IIDG. The found max fault resistance was used in the aggregate result for the grid-connected faults near bus 1. However, grid-connected faults near bus 1 have the largest fault currents, thereby the smallest fault resistance.

To test the hypothesis of unrealistically high fault resistance, the arc equation given in Section B.2 was implemented in the simulation using a "Variable Resistor". As specified in the appendix, the arc length was 2 m. Then a CA fault at line 1-4 was simulated in meshed grid connected. This fault resulted in a non-dependable operation when using the constant resistance of 10 Ω. With the arc-equation, the post-fault steady state yielded a resistance of 0.73 Ω and had a dependable operation. Clearly, the reason for the non-dependable operation was that I specified an unrealistic large fault resistance.

Interestingly, Warrington himself, the person who proposed the famous equation for fault resistance, remarked, according to [105], that using a too-wide range for assumed fault resistance is a typical pitfall in relay studies. Therefore instead of using different fault resistance in the aggregate results, I should have

modeled the equation for fault resistance directly in the simulation.

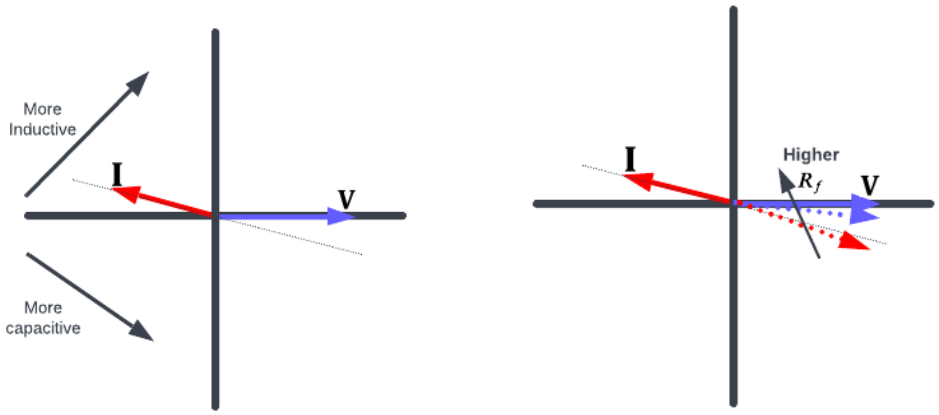
The rest of this section will explain how fault resistance impacts CCA. First, the expected performance during low and high fault resistance will be presented. The explanation provided doesn't offer definitive arguments. However, following the explanations, there are results from simulations that support the explanations.

7.5.2 Expected performance of CCA for fault with small fault resistance

Figure 7.13a show the pre-fault phasor of the voltage and the current *into* a line. This line will have a fault, and the line end is referred to as location "A". Location A is the line end where the energy flow is out of the line, which is why the current phasor into the line is over 90° displaced from the voltage phasor. Due to the pre-fault energy flow, this line end will have a CCA-condition when the fault occurs.

Now the fault occurs. As the grid is not completely stiff, the voltage angle at location A will change. In the simulations, it was seen that when the R/X ratio was greater than unity, the post-fault voltage lagged the pre-fault by a small angle. For increasing fault resistance, it lagged less. Figure 7.13b show the post-fault situation by using dotted lines. Observe how the post-fault PS voltage lags the pre-fault PS voltage.

In the figure, it can also be seen that post fault. The PS current lags the PS voltage by a small angle. This is due to the small fault resistance, which means that the PS current angle at location A is then given by the voltage at location A and the impedance to the fault. The impedance to the fault includes the line and fault impedance. Remember that for the DN, the R/X ratio is typically greater than unity, meaning that this impedance sum is resistive, which is why the Figure 7.13b the post-fault PS phasor lags the voltage phasor by only a small angle. Now as the CCA angle is the angle between the two red arrows, the CCA angle is much greater than 90°.



(a) Pre-Fault **(b)** Post fault, $\frac{R}{X} > 1$

Figure 7.13: Pre and Post fault phasor diagram at the end with expected CCA-condition. Nominal pre-fault line flow. Phasors are scaled to the same length

Now if the fault resistance is still small but increasing, there are two main effects. The impedance sum is more resistive so that the post-fault PS current lags the post-fault PS voltage less. Additionally, as mentioned, the post-fault voltage phasor lags the pre-fault voltage phasor by a smaller angle. Both of these factors cause the post-fault PS current phasor to rotate towards the pre-fault voltage for small but increasing fault resistance. Therefore, there can be a case of some fault resistance causing a large CCA angle than no-fault resistance.

7.5.3 Expected performance of CCA for fault with large fault resistance

Now the expected performance for the high resistive fault will be explained. High resistive faults are when the fault infeed on the opposite end starts impacting the other end's current angle.

Chapter 2.5.7 of the project report, which is copied to Section B.4, explains that the fault current at an arbitrary point in the grid is the superposition of the load component (not influenced by the fault) and a fault component (which only has a source given by the pre-fault voltage at the fault point), i.e.:

$$\mathbf{I_{ps}}(t) = \mathbf{I_{ps,load-comp}}(t) + \mathbf{I_{ps,fault-comp}}(t) \tag{47}$$

The goal of the next paragraph is to find the phase of the fault component current at the faulty line ends. All quantities in the argument are PS quanta ties. Let Z_{th} be the pre-fault Thévenin impedance at the fault point and $\mathbf{V_{pre}}$ be the pre-fault voltage at the fault point, [106] gives the current into a three-phase fault to be Equation 48. As the R/X ratio is greater than unity and it is a large resistive fault, this means that the current into the fault is in phase with the pre-fault voltage at the fault point

$$\mathbf{I_{ps,into-fault}}(t) = \frac{\mathbf{V_{pre}}}{Z_{th} + R_f} \tag{48}$$

Remember that the line's reactance causes the phase shift in voltage across a line. As the DN has short lines with low reactance, the angle difference in voltage across buses is small. This low phase shift is illustrated in Figure 7.14, where the pre-fault phase to ground waveform in grid-connected at bus 1 and 4 is shown. The load at bus 5 was increased by 10 to see the difference. The takeaway here is that $\mathbf{V_{pre}}$ is approximately in phase with the voltage at both line ends. *Therefore, the current into the fault is approximately in phase with the pre-fault voltage at both line ends.*

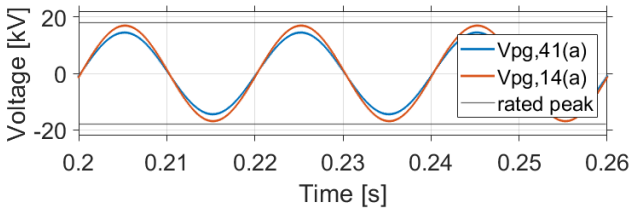


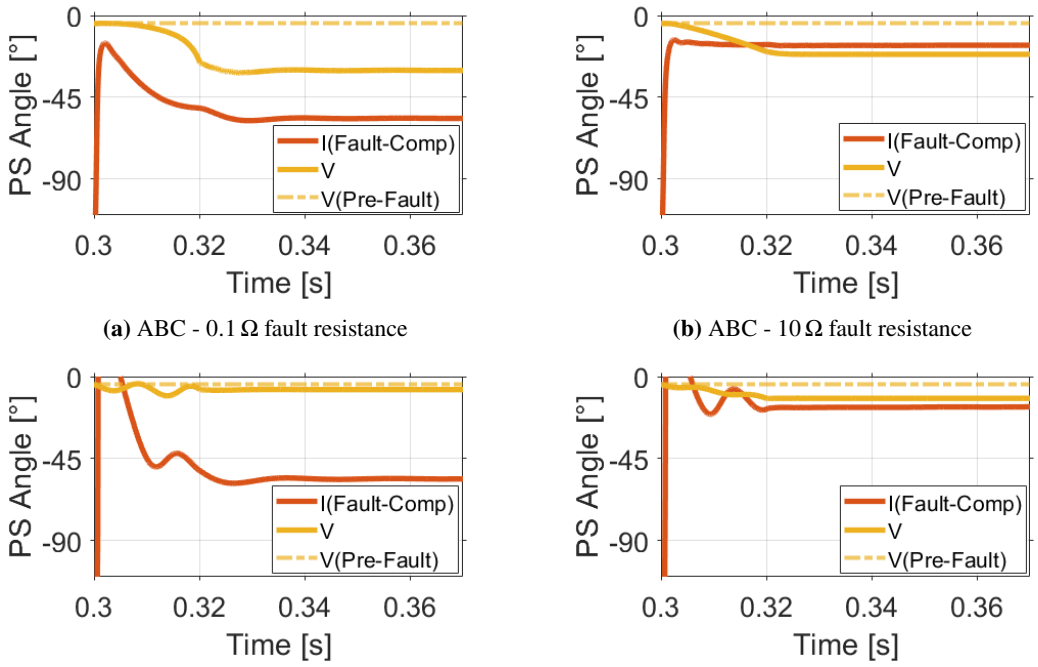
Figure 7.14: Pre-fault phase to the ground voltage waveform. Meshed, grid-connected measuring at 14 and 41. Load at bus 5 increased by a magnitude.

It has been mentioned that when the fault resistance increases, the difference between the pre-fault voltage angle and the post-fault voltage angle is small. In other words, the post-fault voltage angle is approximately in phase with the load component of the voltage angle. As the post-fault voltage magnitude is reduced compared to the pre-fault this must mean that the fault component voltage is 180° phase shifted from the load component. As this is true for both adjacent buses to the fault, *the fault component voltage at the adjacent buses is nearly in phase*.

The fault component voltages at the faulty line ends are in phase, and the impedance per meter of the lines included is equal. Then the fault component currents into the faulty line are in phase with the current into the fault. As the current into the fault is in phase with the pre-fault voltage, the current into the faulty line is in phase with the pre-fault voltage. *The conclusion is that for large resistive faults, the phase of the PS fault component current into the fault line is approximately in phase with the pre-fault voltage at the line ends.*

As stated earlier, the argument is not definitive. However, Figure 7.15 showing PS angles after a midpoint fault at line 1-4 supports my conclusion. In the figure, the PS fault component current at DR41 and the PS voltage at DR41 is shown. Observe that in the case of a large resistance fault, the angle between the pre-fault

angle and the fault component's current is approximately the same. Not that both quantities were calculated in the OPAL, where the fault component was calculated by subtracting the current PS phasor by its value 100 ms ago. Also, observe that while not explained, the conclusion is also valid for two-phase faults.



(a) ABC - 0.1 Ω fault resistance

(b) ABC - 10 Ω fault resistance

(c) AB - 0.1 Ω fault resistance

(d) AB - 10 Ω fault resistance

Figure 7.15: Angle of PS quantities at DR41. For high resistive faults, the fault component angle and pre-fault PS voltage angle are similar. ABC/AB, Meshed, grid-connected, measuring at 41.

As the angle of the fault component into the line is now understood, the CCA-angle for increasing fault resistance can be explained. The CCA-angle is the cycle-by-cycle change in PS angle. Right after the fault, the current value is the sum of the load and fault components, and the value a cycle ago is the load component:

$$\text{CCA-angle} = \angle[\mathbf{I}_{\mathbf{ps,load-comp}}(t) + \mathbf{I}_{\mathbf{ps,fault-comp}}(t)] - \angle\mathbf{I}_{\mathbf{ps,load-comp}}(t) \tag{49}$$

In Figure 7.16, the phasor diagram of Equation 49 is displayed. The diagram is valid for a line end that should have a CCA-condition. The red solid line is the load current, and the blue line is the pre-fault voltage. The green line is the fault component current, as derived, it is in phase with the pre-fault voltage. The red dotted line is the PS current. It is obtained by taking the sum of the fault component (green) and load component (solid-red). According to Equation 49 the CCA-angle is the angle between the red dotted and red solid line.

As the fault resistance increases from an already large value. The red dotted line will rotate towards the load component. Thereby decreasing the CCA-angle. This is because, for increasing resistance, the angle of the load (red) and fault (green) component stays the same, while the magnitude of the fault component reduces.

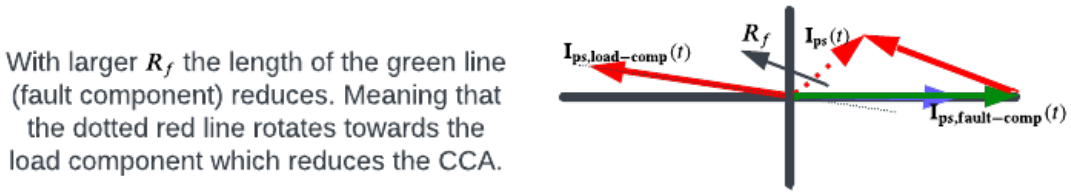


Figure 7.16: Phasor diagram for large resistive faults. At end with CCA-condition and a near unity pf.

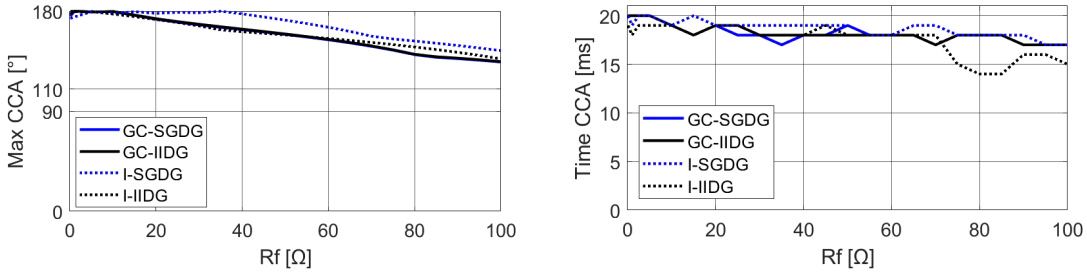
The explanation above clarify why a large fault resistance only at line 1-4 and 1-2 caused dependability failure. Because in grid-connected, line 1-4 and 1-2 has the largest load component. Additionally, the fault near bus 1 will cause a little short circuit current from the upper grid to go around to DR41 or DR21, which should have a CCA. The large load component, compared to a small fault component, results in a small CCA angle.

An interesting observation is made with regard to further work. If the CCA-angle would rather be defined as in Equation 50, then it would be the angle between the load and fault component. In the phasor diagram, this is the angle between the red solid and green line. As this angle is constant and large for all high resistive faults, it could have better performance than the CCA-angle. However, its performance for low-resistive faults and other operating scenarios is unknown.

$$\Delta\theta = \angle[\mathbf{I_{ps}}(t - t_{cycle})] - \angle[\mathbf{I_{ps}} - \mathbf{I_{ps}}(t - t_{cycle})] \tag{50}$$

7.5.4 Simulated performance of CCA during resistive faults

The text above remarked that for low fault resistance faults, some resistance might be needed for max CCA-angle. While for high resistive faults, increasing fault resistance gradually reduces the max CCA-angle. This will now be shown through GC and islanded operation with either IIDG or SGDG and fault at line 2-5. Figure 7.17 present the max CCA-angle and time the CCA-condition is true for an ABC fault. As expected for small fault resistance, the CCA-angle is close to 180° for time much longer than t_{CCA}. Additionally, for the unrealistic high fault resistance level, the max CCA-angle gradually reduces.

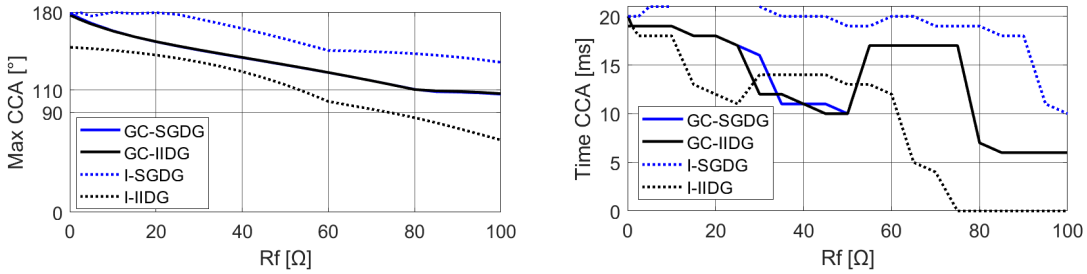


(a) Max CCA-angle at 52

(b) Time the CCA-condition is true at 52

Figure 7.17: ABC, Meshed, GC or Islanded & IIDG/SGDG, 2-5 midpoint fault, measuring at 52.

The three-phase fault is replaced by a two-phase fault. The result below again shows how increasing fault resistance reduces the CCA angle. Additionally, for faults at other points in the grid, the slope of the curves would be different. For example, for a fault close to bus 1, it must reduce quicker as we know it gave CCA failure. The large difference between SGDG and IIDG islanded is expected. Because for an unsymmetric fault, the IIDG currents are symmetric, while the SGDG currents are unsymmetric. Therefore for the IIDG, it's non-faulty phase current that does not have a CCA will also have a current increase.



(a) Max CCA-angle at 52

(b) Time the CCA-condition is true at 52

Figure 7.18: AB, Meshed, GC or Islanded & IIDG/SGDG, 2-5 midpoint fault, measuring at 52.

7.6 How fault resistance influence IJump

The aggregated results of Section 6.1 shows IJump being reliable for high resistive faults. This section will discuss how IJump behaves during increasing fault resistance. In the next paragraph, a quick theory will be shown. Then Section 7.6.1 gives the performance examples for different fault resistance. Section 7.6.2 discuss the impact of load modeling.

As the aggregated results show good performance, the theory will be brief. Nevertheless, keep in mind that as all loads were modeled through a constant impedance, the decrease in current at the far end, $\mathbf{I_2}$ in Figure 7.19. Is proportional to the reduction in voltage at the far end, as specified by Equation 51. In the equation, P stands for pre-fault, F for during fault, and Z_{res} for the impedance at and after bus 2:

$$\frac{\mathbf{I_{2,F}}}{\mathbf{I_{2,P}}} = \frac{\mathbf{V_{2,F}}}{\mathbf{V_{2,P}}} \frac{Z_{res,P}}{Z_{res.F}} \tag{51}$$

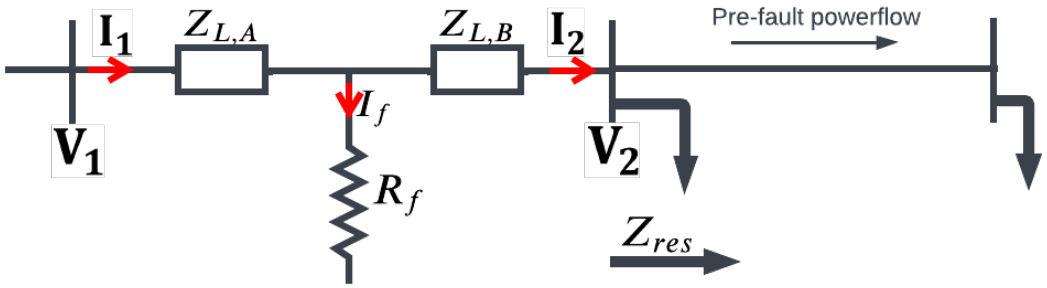


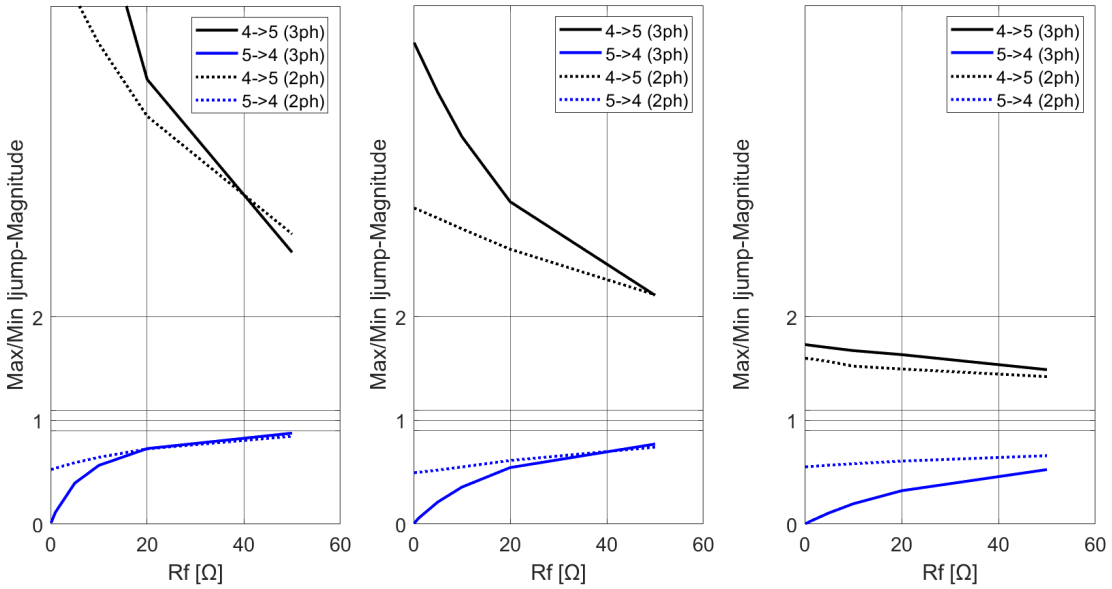
Figure 7.19: PS diagram for a radial line during fault. In LL/LLG, R_f is also connected to the NS diagram.

7.6.1 How IJump behaves for increasing fault resistance

The objective now is to explain how IJump performs for different fault resistances. The simulation result for a midpoint fault at line 4-5 in radial operation is shown in Figure 7.20. The max IJump-magnitude value is shown for DR54, and the minimum for DR45. Each subplot shows both three-phase and two-phase (BC) faults, while the different subplot shows what type of grid operation it is. The two horizontal lines neighboring ”1” is the y-values 1.1 and 0.9. Observe:

- Increasing fault resistance cause less fault current. Therefore as fault resistance increases IJump-magnitude on both ends of the faulty line converges towards ”1”. In line with the aggregate result, the performance is reliable for realistic fault resistance levels.
- GC mode and islanded mode with SGDG has greater fault current levels than islanded with IIDG. Therefore the IJump-magnitude increase seen by DR45 is the lowest/worst for islanded with IIDG. In comparison, as islanded with IIDG has the smallest fault current, it also gets the highest voltage drop. As stipulated by Equation 51, this means the DR54 has the lowest/best IJump magnitude in islanded with IIDG.
- Two-phase faults have, in all cases, less IJump-magnitude deviation from unity. This is due to two-phase faults generally having less PS current than three-phase faults.
- Compared to the other cases, at the end with the current increase, islanded with IIDG have very similar two and three-phase responses. This is because of the symmetric current contribution of the IIDG during unsymmetrical faults, see Section 3.7. Conversely, at the end with the current decrease. Islanded

with IIDG have the most dissimilar two and three-phase fault responses. This is also explained by the symmetrical current of the IIDG during unsymmetrical faults. As this causes a current increase in the healthy phase at the end with an expected current decrease. Thereby limiting the PS current decrease.



(a) Grid connected **(b)** Islanded with SGDG **(c)** Islanded with IIDG

Figure 7.20: IJump-magnitude for varying resistance. ABC/BC, radial, GC or Islanded & IIDG/SGDG, 4-5 midpoint fault, measuring at 45 and 54.

7.6.2 Discussion on load modeling

As explained in Section 4.1.2, all simulations for this thesis have utilized constant impedance loads. As noted in the theory presented in this subchapter, constant impedance loads result in a current decrease at the far end of the faulty radial line section. This decrease is proportional to the voltage decrease.

Real-world loads exhibit greater complexity. For instance, ZIP loads represent a load as a combination of constant impedance (Z), current (I), and power (P) loads. When voltage decreases, a Z load draws less current, an I load theoretically draws the same current, and a P load theoretically draws more current. Clearly, Z loads yield the most beneficial impact on the magnitude of the IJump at the far end of the faulty line.

Future DN will have more inverter-interfaced loads such as heat pumps, battery storage, and electric vehicle charging, introducing additional complexity to load modeling. For example, while traditional resistive heating is constant impedance, in the laboratory experiment in [107], the heat pump was seen to be of constant power. In *theory*, the constant constant power load would draw a higher current during the fault, thereby preventing the correct working function of IJump. In reality, the voltage drop might cause the load downstream to disconnect. The important point is that there is uncertainty as to how the algorithm would respond with more realistic load models.

To illustrate the uncertainty, consider a case with a significant amount of induction motors downstream of the fault. Following the voltage collapse right after the fault, the induction motors would want to draw a higher current to maintain the torque [108]. If this causes a short increase in the current before the IM disconnect, this might impede IJump, that are only able to see the fault during the transition to the faulty state. If this is found to be a problem, a possible solution would involve comparing phasor across several cycles ago instead of evaluating on a cycle-by-cycle basis.

7.7 Pre fault line flow with near zero power factor impede CCA

The aggregate results of Section 6.4 show that lines with a pre-fault line flow with a near zero pf can experience a loss in dependability in meshed operation. The reason why will now be explained.

Figure 7.21 is valid for a line end that is anticipated to have a CCA. The left subfigure shows the phasor-diagram pre-fault. Then as the fault occurs, the dotted lines in the right figure show the post-fault phasor diagram. Observe that the CCA angle, which is the angle between the red solid and dotted line, is reduced compared to the case of close to unity pf presented in Section 7.5.

(a) Pre-fault very capacitive power factor.

(b) Post fault $\frac{R}{X} > 1$.

Figure 7.21: Pre and Post fault phasor diagram at the end with expected CCA-condition. Pre-fault line flow with near zero power factor. Phasors are scaled to the same length

To illustrate the phenomenon, the grid is in grid-connected with IIDG. The load at bus 5 is modified as in Section 6.4 so that the pre-fault line flow at lines 4-5 and 2-5 have a capacitive power factor of 0.1. Figure 7.22 is a result of the fault at the midpoint of 2-5. DR52 should detect a CCA condition, but due to the pre-fault factor, the CCA-angle is insufficient.

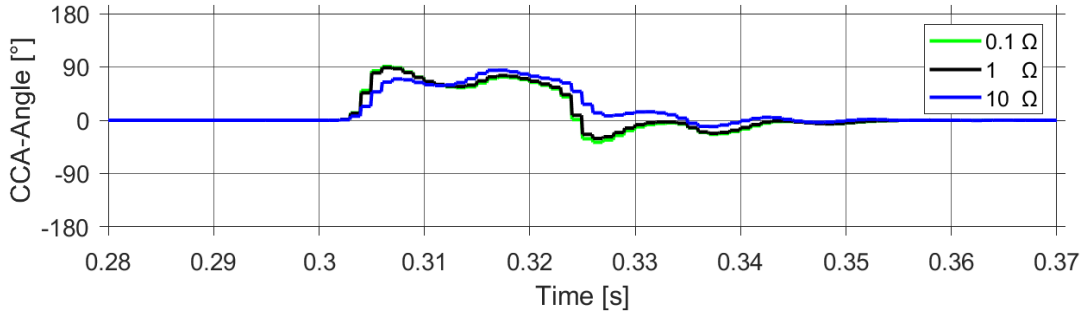


Figure 7.22: Line flow at 2-5 has near zero power factor. CCA-angle on the line end that should cause a CCA-condition. Meshed, grid-connected, 2-5 midpoint fault, measuring at 52.

Note that reducing ϕ_{CCA} is an unsuitable solution. It would increase the likelihood of correct operation of the end with an anticipated CCA increases, but also increases the probability that the end that should not have a CCA has a CCA.

The above example, which is the example from the aggregated result, is a worst-case scenario. It is worst-case because there is little active consumption at bus 5, and the grid symmetry means that the line flow obtains the pf at bus 5. Furthermore, a capacitor bank in the middle of the DN is not expected. Other scenarios, such as an unloaded distribution transformer, might be more likely to cause this problem. Nevertheless, it is important to be aware that if the pre-fault line flow is very capacitive/inductive, the scheme can fail, and future work should look into additional settings to fix this scenario.

7.8 Cross-Country faults

The aggregated results of Section 6.5 demonstrated that during a cross-country fault, the proposal typically detects only one of the faults. Only observing one of the faults presents an issue in the case the residual earth fault does not self-extinguish. Because as discussed in Section 2.3.2, the residual fault requires disconnection within 10 s. The goal of this section is to therefore analyze two typical cases where the expected scheme sees only one of the faults. It will be remarked that if the scheme were implemented on a per-phase basis, rather than using PS quantities, then it would have seen both faults.

7.8.1 CCA Failure during Meshed operation with high fault current

The upcoming example illustrates the typical case of CCA failure in meshed conditions. The example will be an earth fault at the middle of line 1-2 (A-Earth) and line 4-5 (C-Earth). The expected performance is that DR21 and DR54 detect a CCA-condition, while DR12 and DR45 do not. Looking at the fault logger in Figure 7.23a, the upper two rows show correct performance for line 4-5. However, looking at "Change21" it is seen that DR21 does not detect a CCA. Consequently, faulty line 1-2 is not identified as faulty.

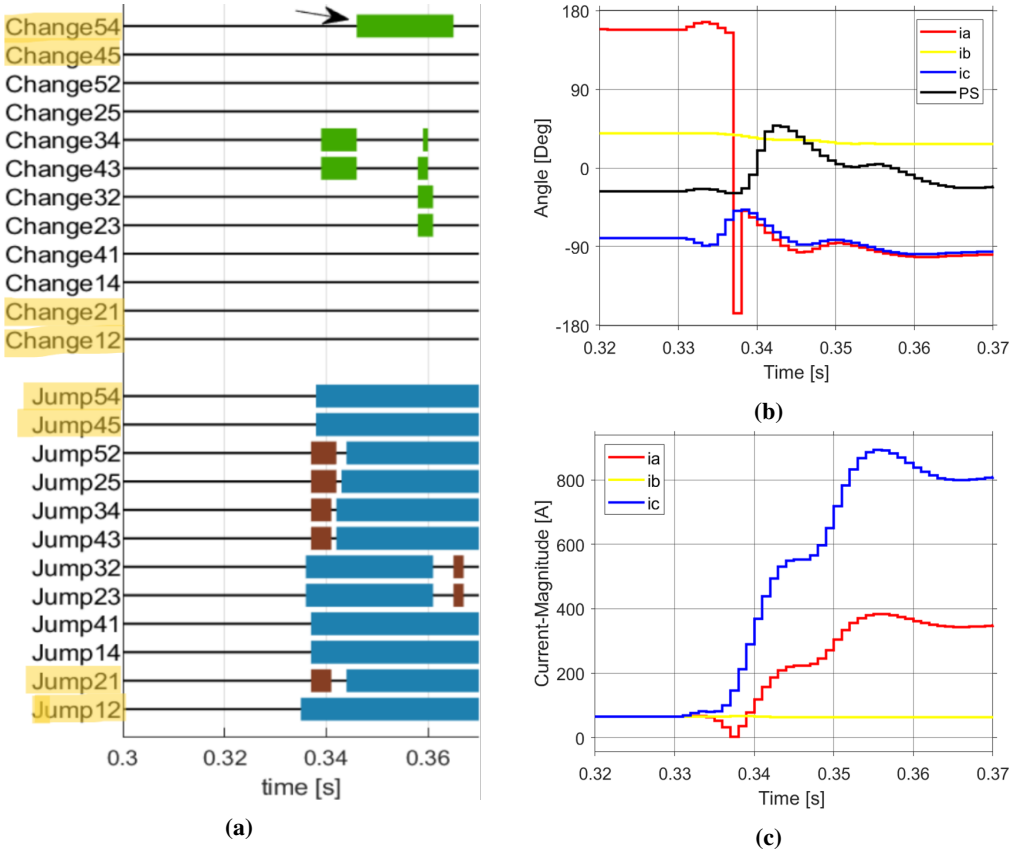


Figure 7.23: Cross-Country fault. (a) shows when the CR detects a CCA or IJump condition. blue color means IJump-magnitude is greater than ϵ_{up} (b) shows the per phase current angle at 21 (c) shows the per phase current magnitude at 21. "Jump21" is not under ϵ_{down} for a time of t_{IJump}. 1-2 A-Earth and 4-5 C-Earth, meshed, grid-connected, measuring at 21.

To explain why DR21 does not detect a CCA, the right subfigures show phase current angles and magnitudes seen by DR21 (calculated in the OPAL). As expected at DR21, there is a CCA for phase A, but not phase C (A fault on line 1-2)). Moreover, there is no significant fault current source behind DR21. Therefore at DR21, the largest current is the phase C current. Consequently, as the current transiting toward the other fault are dominant, the expected CCA of phase A is not reflected in the PS current angle calculated at DR21.

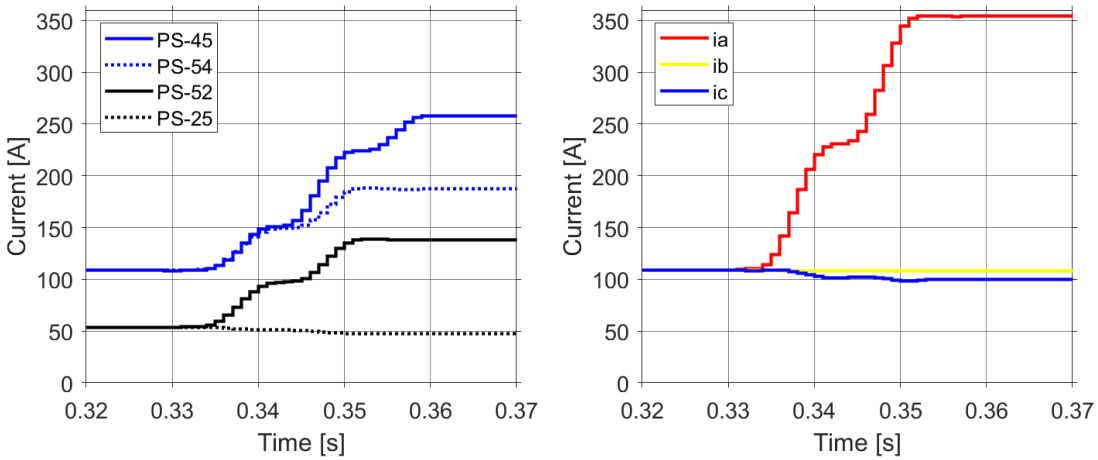
7.8.2 Failure during Radial operation both faults on the same feeder

The typical case of dependability loss in radial conditions is now discussed. The typical case of failure in radial operation is also due to fault current transiting to another fault. For radial operation with faults on the same feeder, it causes only the far-end fault to be localized.

Grid-connected operation with an earth fault at line sections 4-5 (C-Earth) and 2-5 (A-Earth) will be used to illustrate the phenomena. Both faults have a large earth fault resistance of 40 Ω.

The black lines in Figure 7.24a show the current measurement of the far-end fault. Observe that there is a 10% increase seen by DR52 while a greater than 10% decrease is seen by DR25, causing a correct trip of 2-5.

The blue lines in Figure 7.24a show the current measurement of the near-end fault. For the near-end fault, DR45 has the expected current increase. However, DR54, which is expected to have a decrease in current, actually has an increase in PS current magnitude (blue dotted line). As expected, the current of phase C has a current decrease at 54 (phase C is the 4-5 fault). However, the problem is that at 54, the phase A current is dominating. The phase A current is high as this is the current going towards the far-end fault. Therefore the decrease in the current of phase C is not reflected in the PS current magnitude calculated by DR54.



(a) PS current at 45, 54, 52, 25.

(b) RMS of each phase at 54

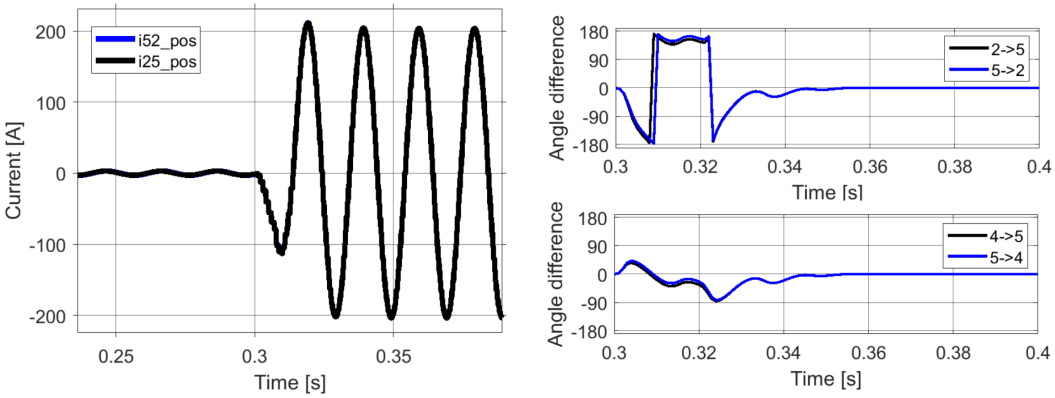
Figure 7.24: Cross-Country fault on a single radial feeder. 4-5 C-Earth and 2-5 A-Earth, radial, grid-connected, measuring at 21. Calculated in the OPAL.

7.9 Line current comparable to line charging current

The aggregate results did not include the situation where the line charging current is comparable to the line flow. The situation will be explained to cause reliability reduction. It is especially relevant for cables.

7.9.1 Discussing why large capacitive line charging cause loss of reliability

Figure 7.25a is the result of a three-phase fault at lines 1-2. The figure shows the current into 2-5 at bus 2 and out of 2-5 at bus 5. As with all other simulations so far, an overhead line was used. Load at bus 5 was decreased so that the pre-fault current is only 1.5% of the line rating. Observe that pre-fault, the current on both line ends are equal. As the pre-fault current overlaps, the capacitive line current is small compared to the line flow. Therefore, the right figures show the correct performance of two healthy lines.

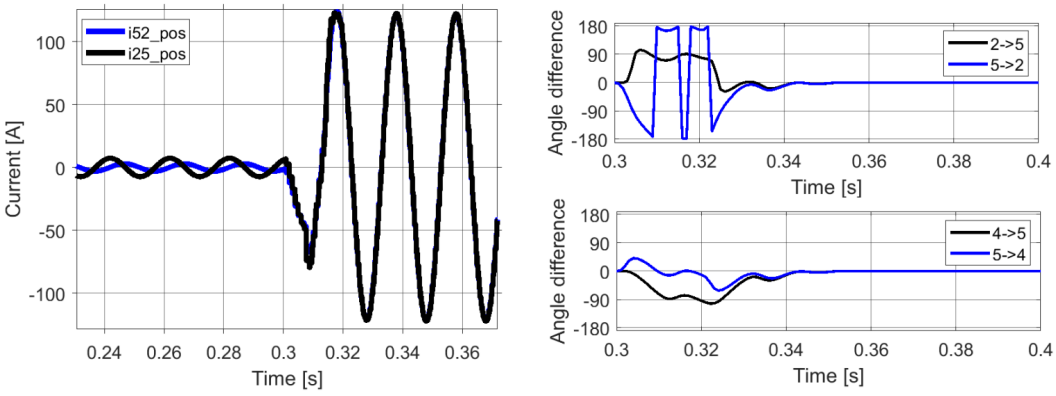


(a) PS instantaneous current at 2-5

(b) CCA-angle for healthy line 2-5 and 4-5

Figure 7.25: Overhead line with a line charging current that is not comparable to the line flow. Pre fault line 2-5 flow is 0.015 pu. ABC, Meshed, Grid-Connected, 1-2 midpoint fault, measuring at 2-5 and 4-5.

Figure 7.26 depicts the same scenario as above but with a 10 km XLPE cable replacing overhead lines 2-5 and 4-5. Based on the cable parameters in Section 4.1.1, the cable operates at 3% of the rated thermal load. The high cable-to-earth capacitance cause the pre-fault currents on line 2-5 to have a 90° discrepancy. Post-fault, the currents have a similar phase. This is due to increased line current from the fault and reduced charging current due to voltage drop. As DR25 and DR52 have different phase pre-fault but equal phase post-fault, the DRs of the same healthy line calculate different CCA-angel. Figure 7.26b depicts that this resulted in a trip of healthy lines 2-5 and 5-4.



(a) PS instantaneous current at 2-5

(b) CCA-angle for healthy line 2-5 and 4-5

Figure 7.26: Cable with a line charging current that is comparable to the line flow. Pre fault line 2-5 flow is 0.03 pu. ABC, Meshed, Grid-Connected, 1-2 midpoint fault, measuring at 2-5 and 4-5.

Above, the loss of security was triggered by a fault. However, other scenarios, such as sudden loss of load, will have the same effect. In Figure 7.27, a trip occurred due to a sudden loss of load at bus 4 and 5.

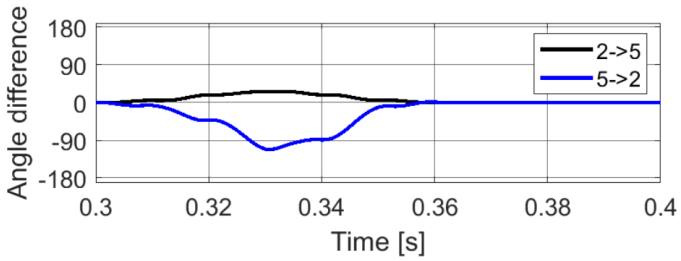


Figure 7.27: Trip of cable due to sudden loss of load. The line charging current was comparable to the line flow. Meshed, Grid-Connected, load at 4 and 5 disconnects, measuring at 25 and 52.

Evidently, a capacitive current comparable to line flow reduces reliability. The loss of reliability was due to different pre-fault phase angel. Consequently, the subsequent text will derive a formula for the pre-fault angle difference (δ) in currents across a healthy line. A PS current magnitude ($I_{CCA,disable}$) will then be found where the scheme must be disabled. The derivation will utilize what could be observed in Figure 7.26b. Which is that for DR25, a CCA-Angle of 180° was expected, but a CCA-angle of 90° was measured. The 90-degree discrepancy equals the pre-fault phase difference between the line end currents.

7.9.2 Maximum angle difference in currents across a line, steady state

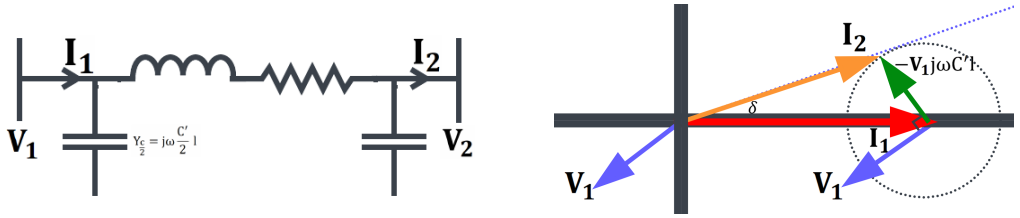
Figure 7.28a is the PI-line model of an arbitrary cable/line, and Figure 7.28b is the corresponding phasor diagram. The active energy flow is in the opposite direction of the defined current phasors, and the power factor is exaggerated. A derivation of the approximate maximum angle between $\mathbf{I_1}$ and $\mathbf{I_2}$ will now be presented. The formula is independent of the power factor and power flow direction. The first objective is to understand the phasor diagram. Start by expressing $\mathbf{I_2}$ using the operating capacitance:

$$\mathbf{I_2} = \mathbf{I_1} - (\mathbf{V_1} + \mathbf{V_2}) j\omega C_d^{'} \frac{l}{2} \tag{52}$$

Here $C_d^{'}$ is the operating capacitance per length unit and l is the length of the line. Simplify the above equation by neglecting the series voltage drop across the line:

$$\mathbf{I_2} \approx \mathbf{I_1} - \mathbf{V_1} j\omega C_d^{'} l \tag{53}$$

Using chosen phasor angles for $\mathbf{V_1}$ and $\mathbf{I_1}$ combined with Equation 53 the phasor diagram can be drawn. δ is the angle between $\mathbf{I_2}$ and $\mathbf{I_1}$. The dotted blue circle shows all possible endpoints of $\mathbf{I_2}$ for a given set of $|\mathbf{V_1}|, \omega C_d^{'}, l$ and $|\mathbf{I_1}|$, but with a varying power factor. Therefore for a given set of $|\mathbf{V_1}|, \omega C_d^{'}, l$ and $|\mathbf{I_1}|$, the maximum δ (δ_{max}) must be defined by the straight line that goes through the origin and is tangential to the circle. In the phasor diagram, this is the blue dotted straight line. The next objective is to find this angel.



(a) PI-line model. **(b)** Phasor diagram. No series voltage drop.

Figure 7.28: PI line model and corresponding phasor diagram

In Section B.5, Equation 54 is obtained by only using mathematical steps to derive the angle between the dotted line and x-axis. This is the maximum angle difference when the power factor is unknown.

$$\delta_{max} = \arctan \frac{1}{\sqrt{(\frac{1}{\frac{V_{rated}}{\sqrt{3}I_1}\omega C_d' l})^2 - 1}} \tag{54}$$

The implications of the formula are in line with expectations. For a given current, higher line capacitance results in a greater angle. As cable has much greater capacitance, cables are more liable to encountering issues with this scenario. have the most problems with this scenario. Furthermore, under normal conditions, the voltage remains relatively constant while the current varies. Therefore, it is the situation of low loading that is most liable to this scenario.

7.9.3 Finding an expression for $I_{CCA,disable}$

The explanation above described that as the line current decreases, δ increases. If the value of the angle that caused un-reliability was known, then the current magnitude that caused scheme failure could be found. This PS current magnitude is referred to as $I_{CCA,disable}$ (introduced earlier). The scheme should be disabled as long as the DR detects a current equal to or lower than $I_{CCA,disable}$.

The challenge is that the angle causing un-reliability is unknown. Preliminary simulations show reliable operation for δ equal to 20°, but this conclusion is based on a limited number of simulations and lacks analytical derivation. Therefore, further research is required to establish more definitive limits. Still, the 20-degree value will be employed as an example of how $I_{CCA,disable}$ can be found. Expressing Equation 54 with current on the left-hand side results in:

$$I = \frac{(\frac{V_{rated}}{\sqrt{3}})\omega C_d' l}{\sqrt{\frac{1}{\tan^2(\delta_{max})} + 1}} \tag{55}$$

$I_{CCA,disable}$ is then Equation 55 at a 20°. Furthermore, the cable voltage is not measured and must therefore be assumed to be the worst case. 1.1 the rated voltage is the maximum permissible deviation to the end consumer according to Norwegian law [109]. Which results in the following:

$$I_{CCA,disable} = \frac{(1.1\frac{V_{rated}}{\sqrt{3}})\omega C_d' l}{\sqrt{\frac{1}{\tan^2(20°)} + 1}} \tag{56}$$

$I_{CCA,disable}$ can be computed during relay installation. If the PS current magnitude falls below this calculated value, the CCA scheme is deactivated by the DR. Now the typical value of capacitance for cables and lines with specific current and voltage ratings provided in [96] will be used. Figure 7.29 uses Equation 56 to show what % of the load current the scheme must be disabled. The x-axis is the cable/line rating. The y-axis gives the maximum distance the line/cable can be if $I_{CCA,disable}$ should be 1%, 5%, or 10% of the rated current.

Notice that an overhead line with the lowest current rating can extend up to 20 km between junctions if the scheme is to operate for all currents exceeding 1% of the thermal rating current. Conversely, a cable can only span 1-2 km for the scheme to be disabled at 1%. However, if it can be disabled at 5%, the figure illustrates that the cable can extend 5-8 km. The most likely candidate for a meshed DN is an urban system with substantial loads. While this network is typically cabled, it has short distances between DN junctions, which is beneficial. XLPE cables are assumed in the figure as it is a common cable type in the DN nowadays.

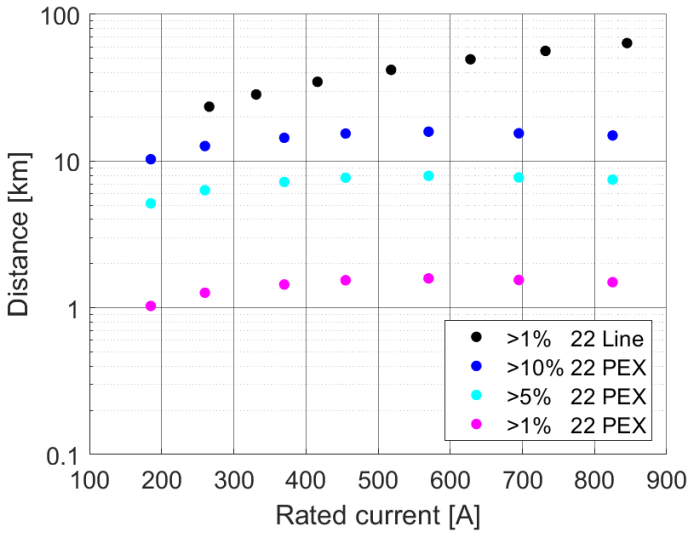


Figure 7.29: The max distance between DRs if CCA should not be disabled for ¿X% of the thermal rating. X-axis is the *rated* current of a specific XLPE-cable or overhead line. Line/Cable data is from [96].

7.9.4 Remarks on the need to disable the CCA scheme

Further considerations are warranted. Firstly, this issue reveals two bigger issues with the scheme. Secondly, is the situation realistic? Thirdly, what actions should be taken when CCA is disabled?

The two bigger issues. As remarked in Section 2.3.4, the scheme relies on detecting the transition between healthy and faulty phases. Therefore it is not unable to detect a fault if closing onto a fault, i.e in the case the pre-fault situation is 0 A. A more precise definition with regard to the CCA scheme is that it is unable to reliably detect fault until the current is $I_{CCA,disable}$. Secondly, there is a concern regarding the ability of the protection CT to accurately measure current when it is extremely low.

Is the situation realistic? Several operating scenarios can give rise to the described situation. One such example is a cable located in a radial section where there the load at the far end of the cable is suddenly disconnected.

What actions should be taken when CCA is disabled? As the aggregated results indicated reliable radial operation due to IJump, disabling the CCA scheme in radial operation has no repercussions. The challenge lies in disabling the scheme in meshed operation, where CCA is required for dependable operation. One possible solution in such a scenario is to employ a slower traditional backup scheme. However, this would imply that the backup protection system becomes the primary protection. When the current is so low, there are fewer benefits of meshed operation. Therefore, in the future, another approach is to utilize DNR to convert the line with low current to radial operation.

7.10 Is public mobile 4G/5G network feasible for the protection scheme

The goal of this section is to evaluate if public mobile networks are feasible to use in a plug-and-play manner. A feasible communication network means here the communication delay does not impede DG-LVRT or reduce reliability. Section 3.7.2 specified that to not impede DG-LVRT, the protection system should isolate the fault in less than 150 ms. Therefore there exists a time, $t_{Max,com,delay,LVRT}$, which is the maximum communication delay that does not impede DG-LVRT. Moreover, Section 3.1.3 explained that the blocking nature of CCA can reduce reliability. Because CCA must always wait for an additional $t_{DR->CR,communication,max}$ before tripping due to CCA. Where $t_{DR->CR,communication,max}$ is the maximum WAN communication delay between the DR and CR.

Assuming that the WAN delay is equal between the DR to CR and CR to CB. Then a communication network is feasible if it provides a $t_{DR->CR,communication,max}$ that is less than half of $t_{Max,com,delay,LVRT}$. In light of this, the upcoming text will evaluate if this criterion is true. If this criterion is false and a public mobile network had actually been used. Then the aggregated results would have had reduced reliability.

7.10.1 Finding the value of $t_{Max,com,delay,LVRT}$

The time it takes for the scheme to trip can be divided into three distinct values $t_{logictime}$, $t_{communication}$, and $t_{interruption}$. To satisfy the 150 ms constraint with a 8 % margin, the three values must satisfy the below inequality. In the inequality, the new quantity $t_{interruption}$ is the CB interruption time.

$$t_{logic-time} + t_{communication,WAN} + t_{interuption} \leq 138\,\text{ms} \tag{57}$$

The maximum logic time of the 1440 simulations in Section 6.1 was 28 ms. Remember that the logic time is the time time to trip, disregarding WAN communication delay.

The upper limit of CB interruption time is the rated interruption time. IEEE standard C37.04-2018 defines it to be the *maximum* time between energizing the trip coil and interrupting the current [110]. For DN level voltages, the vacuum circuit breakers offered by ABB, General-Electric, and Siemens offer a rated interruption time of three cycles (60 ms) [111–113]. As Siemens points out, the average interruption time is much less than the max interruption time, and the CB opening time (25-41 ms) is greater than the arching duration (2-17 ms) [114].

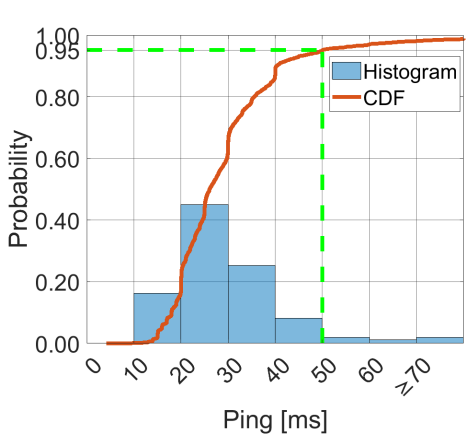
Using the maximum value of $t_{logictime}$ and the rated value of $t_{interuption}$ in Equation 57 results in $t_{Max,com,delay,LVRT}$ be 50 ms. To not impede DG-LRVT, the CR setting $t_{DR->CR,communication,max}$ is set to 25 ms. If the actual communication delay between the DR and CR is larger than 25 ms, the CCA scheme can trip healthy lines with CCA-condition on both ends.

7.10.2 Investigating the value of $t_{DR->CR,communication,max}$ for public 4G/5G mobile networks

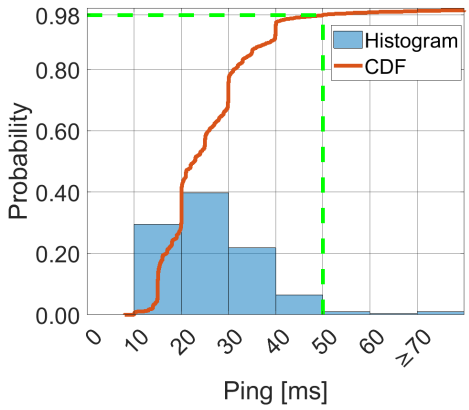
Until now, it has been found that a communication network is feasible if it provides a max round-trip communication of 50 ms (max one way is 25 ms). The literature review in Section 2.4 noted that communication latency using public mobile 4G or 5G networks falls short compared to the 3GPP standard and the technical report IEC TR 61850-90-12:2020. However, if these standards were met, such as the one-way max delay of 10 ms for inter-tripping using WAN communication in IEC TR 61850-90-12:2020, the scheme's speed would be more than sufficient.

However, as pointed out in the review current public mobile communication network does not satisfy the IEC requirement. Figure 7.30 substantiates this argument for my scheme. The figure depicts ping measurements, which are akin to the total delay from DR to CR and then to CB. Subfigures (a) and (b) use publicly available measurements from real-world 4G and 5G measurements in Austrian public networks [115]. Subfigure (c) was obtained at the NTNU 5G laboratory by me, see Section 5.4. Because the goal is to check if current public mobile networks can be used in a ”plug and play” fashion, detailed analyses of the networks are not presented or conducted. Keep in mind that the actual round-trip delay for a GOOSE message would be 4.4-7.2 ms larger than the ping as the GOOSE packet would need to be encapsulated with an IP address, see Section 3.5.3.

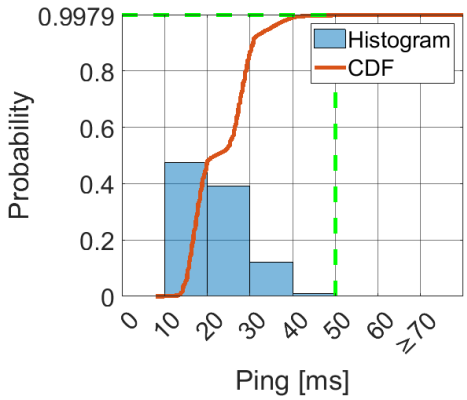
In all scenarios, the round trip latency (median) is significantly less than the required 50 ms delay. The issue, however, lies in the jitter as the communication delay frequently surpasses 50 ms. To understand why jitter is the problem, consider the cumulative distribution function (CDF). The y-axis value corresponding to the green dotted line represents the probability that the ping will be equal or less than 50 ms. For example, the 4G network would result in the tripping of a healthy line 9.5 % of the times a CCA occurs on healthy lines (2*0.95*0.05). Although the Austrian public 5G network and the NTNU 5G network demonstrate better performance, their performance is still unacceptable for the scheme. For instance, with the NTNU network, a healthy line would be tripped 0.4 % of the times it has a CCA at both ends. In reality, the percentages would be even larger due to the time it takes to encapsulate the packets.



(a) 4G, median=26.1 ms, (#22197)



(b) 5G (expected to have a 4G core), median=22.8 ms, (#9965)



(c) 5G (At NTNU), median=21.9 ms, (#195205)

Figure 7.30: Delay/ping in public mobile 4G and 5G networks. (a) & (b) open source data from real Austrian networks between 2023-03-08 and 2023-04-08 [115]. (c) My ping measurement at NTNU 5G laboratory.

Observing the steepness of CDF in Figure 7.30c versus Figure 7.30b, it is apparent that the 5G measurement at NTNU exhibits less jitter compared to the 5G Austrian network. There can be multiple explanations for this. Firstly, the NTNU 5G network is a private 5G network with less background traffic. Secondly, based on the literature review, it's expected that the cabled component of the current public 5G network has a 4G core/cabled component. The 5G network used at NTNU has a 5G core.

While utilizing existing public 4G and 5G networks in a plug-and-play manner for the protection scheme isn't feasible, it doesn't mandate the use of fiber cables. As stated in the literature review, current 4G networks can be reconfigured to meet essential requirements. Furthermore, the emergence of 5G network slicing and URLLC suggests that as 5G technology matures, the feasibility of using existing public or privately owned 5G networks for the protection scheme increases.

8 Conclusion

The objective of this thesis was to *propose* a phase-fault protection scheme for a future active meshed distribution network (DN), *build* a hardware in the loop (HIL) test bench, and *evaluate* the proposal using the test bench.

The objective of the evaluation was to evaluate the proposed protection system reliability and speed. At nominal load conditions, the proposed scheme located all 1440 simulated faults without tripping any healthy lines. My novel proposal of running the existing CCA and IJump scheme in parallel increased reliability and speed for meshed lines. The performance improvement stemmed from IJump's unexpected ability to sometimes locate faults on meshed lines. Opposite to CCA, IJump's ability to see faults on meshed lines increases with decreasing fault current level. The increased speed occurred due to IJump locating the fault due to a transient decrease in *calculated* current magnitude. In those cases, CCA also saw the fault. The times IJump saw faults on meshed lines, but not CCA, coincided with decreased *Positive Sequence* magnitude post-fault.

The evaluation also revealed other sides of the proposal. While the proposal of using a non-traditional method of phasor calculation did not impact reliability, it reduced speed, and it had negligible computational benefit. The non-traditional method is not recommended for my scheme or other schemes in the future. Other proposals saw more value. For large frequency excursions that can occur during islanded. My requirement and implemented crude frequency estimator were necessary to see all faults. The proposed setting t_{CCA} was the solution to prevent CCA tripping due to unsynchronized relay sampling, measurement error, time stamping error, and small capacitive line charging.

The evaluation also revealed reliability limitations. Using an unrealistically high fault resistance was a modeling error resulting in scheme failure. Therefore, it is recommended to directly model the arc equation instead. Regarding cross-country faults, a per-phase implementation must be used if the scheme should reliably detect both faults. A significant limitation of the scheme is that it relies on the transition between a healthy and faulty state. Therefore, the scheme cannot see faults after the transition, it fails to protect when energizing lines with a fault, and it struggles when line flow is comparable to line charging current. It also encounters reliability reduction for pre-fault line flow with a near zero pf.

The objective of the testbench was to be a proof of concept. The microprocessor was fast enough to work as a relay in real-time operation. The testbench was also able to handle time-delayed IEC61850-GOOSE packets through time stamping. However, it was found that current public mobile 4G/5G network cannot be used in a plug-and-play manner due to large spikes in the delay. If DG-LVRT capability should not be impeded, these spikes in delay can trigger the tripping of healthy lines due to CCA's blocking nature. As 5G networks mature, they are anticipated to overcome this limitation.

Zooming out. To facilitate a meshed DN in Norway, new earth fault relays also have to be developed. Further, the need to measure the current at all line interfaces implies a significant cost. However, compared to existing literature, the number of measurement points is not high. Perhaps, if the advantages of a meshed DN should be harvested, more measurements and switch gears are needed. This will entail significant expenses, but innovative solutions can lessen these expenses. This thesis reduced the expected expense by using a central relay to decouple the switch gear from the relay.

9 Further Work

The case of further work is divided into further work needed on the protection algorithm and the work needed on the test bench.

Further work on the protection algorithm:

- The protection algorithm should use the traditional method of positive sequence phasor calculation instead of the proposed instantaneous method. Because in Section 7.2, it was seen that the traditional method results in a faster response with higher sensitivity, less problem with spectral leakage, and negligible computation disadvantage.
- The CCA-angle was defined as the angle between the load component and the PS instantaneous current. Section 7.5.3 identified the possibility of rather using the angle between the load component and the fault component. This means to use Equation 58 instead of Equation 59. It was remarked that the new definition might have advantages with regard to a fairly constant CCA-angle for various fault resistance. However, the behavior for low resistance faults is unknown. If both methods don't reduce security, a possibility is to run both calculation methods in parallel.

$$\text{CCA-angle-new} = \angle[\mathbf{I_{ps}}(t - t_{cycle})] - \angle[\mathbf{I_{ps}} - \mathbf{I_{ps}}(t - t_{cycle})] \tag{58}$$

$$\text{CCA-angle-used} = \angle[\mathbf{I_{ps}}(t)] - \angle[\mathbf{I_{ps}}(t - t_{cycle})] \tag{59}$$

- Instead of comparing on a cycle-by-cycle basis, compare several cycles back. This will mean that the fault is detected for a longer time, and the scheme is also able to see the faults after the transient has settled. The reason why I didn't do this from the start is that I initially thought the problem of spectral leakage could be handled without frequency estimation. Because without estimation, there will be a false CCA-angle of 7.2° per 1 Hz deviation *per cycle*. However, frequency estimation was required.
- How to handle cross-country fault, near unity power factor line flow, and low line flow compared to line charging current should also be investigated. The problems with cross-country faults were seen solved by implementing the scheme on a per-phase basis.

Further work on the test bench:

- Section 5.2 pointed out that communicating three sets of SV per measurement point only requires a simple modification of the existing ICD file. It also pointed out that it will not cause a significant increase in the necessary communication bandwidth. Lastly, this is now a requirement as the traditional method of positive sequence phasor calculation has been recommended.
- Section 7.6.2 pointed out that modeling loads as constant impedance results in uncertainty with regard to the IJump performance at the far end of a faulty radial line. Therefore more accurate load models are necessary. "2781-2022 - IEEE Guide for Load Modeling and Simulations for Power System" is a good starting point [108].

Bibliography

[1] Karl Fredrik Anker Wirgenes. *Project Report - Challenges and solutions for short circuit protection in an active meshed distribution network*. Dec. 2022.

[2] Centre for Intelligent Electricity Distribution (CINELDI). *Pilot Projects*. Accessed: 2023-05-21. 2023. URL: https://www.sintef.no/projectweb/cineldi/pilot-projects-in-cineldi/.

[3] R.C. Dugan and T.E. McDermott. 'Operating conflicts for distributed generation on distribution systems'. In: *2001 Rural Electric Power Conference. Papers Presented at the 45th Annual Conference (Cat. No.01CH37214)*. 2001, A3/1–A3/6. DOI: 10.1109/REPCON.2001.949511.

[4] Astrid et al. *Tekniske retningslinjer for tilknytning av produksjonsenheter med maksimum aktiv effektproduksjon mindre enn 10 MW*. 2006.

[5] Simon Richards et al. *Network protection and application guide*. en. Stafford, England: Alstom Grid, May 2011.

[6] Marie-Cécile Alvarez-Herault et al. 'Investigation of new distribution grid architecture for accomodating higher dg penetration rate'. In: *CIRED Workshop* (June 2010).

[7] G. Celli et al. 'Meshed vs. radial MV distribution network in presence of large amount of DG'. In: *IEEE PES Power Systems Conference and Exposition, 2004.* 2004, 709–714 vol.2. DOI: 10.1109/PSCE.2004.1397664.

[8] Norges vassdrags- og energidirektorat. 'Norsk og nordisk effektbalanse fram mot 2030'. In: (May 2022). URL: https://publikasjoner.nve.no/rapport/2022/rapport2022_20.pdf.

[9] T. Bruckner et al. *Energy Systems*. Ed. by O. Edenhofer et al. Cambridge, United Kingdom and New York, NY, USA: Cambridge University Press, 2014.

[10] Henrik Kirkeby. *Beste praksis for trinnkobler i krafttransformator og spenningsregulator i DG-enheter*. Tech. rep. 2017.

[11] V.H.M. Quezada, J.R. Abbad and T.G.S. Roman. 'Assessment of energy distribution losses for increasing penetration of distributed generation'. In: *IEEE Transactions on Power Systems* 21.2 (2006), pp. 533–540. DOI: 10.1109/TPWRS.2006.873115.

[12] R.J.W. de Groot, J. Morren and J.G. Slootweg. 'Closed-ring operation of medium voltage distribution grids : theory meets practice'. English. In: July 2015, pp. 1–5.

[13] R. J. W. de Groot, J. Morren and J. G. Slootweg. 'Investigation of grid loss reduction under closed-ring operation of MV distribution grids'. In: *2014 IEEE PES General Meeting — Conference Exposition*. 2014, pp. 1–5. DOI: 10.1109/PESGM.2014.6938810.

[14] Christer Heen Skotland, Eirik Eggum and Dag Spilde. *Hva betyr elbiler for strømnettet?* Tech. rep. 74. Norges vassdrags- og energidirektorat, 2016. URL: https://www.nve.no/Media/4720/elbil_str%C3%B8mnett_rapport.pdf.

[15] F. Provoost, D. Harmsen and S. Lamboo. 'Meshed operation of MV networks using intelligent RMU and innovative fault location'. In: *CIRED 2021 - The 26th International Conference and Exhibition on Electricity Distribution*. Vol. 2021. 2021, pp. 1597–1601. DOI: 10.1049/icp.2021.1534.

[16] Øyvind Zambrano Lie. 'Solkraft kan tvinge lavtspentnettet på Agder i kne'. In: *Energiteknikk* (Dec. 2022). URL: https://energiteknikk.net/2022/12/solkraft-kan-tvinge-lavtspentnettet-pa-agder-i-kne/.

[17] Atle Abelsen. 'Mye sol skaper spenningstrøbbel'. In: *Energiteknikk* (Dec. 2022). URL: https://www.energiteknikk.net/2022/12/mye-sol-skaper-spenningstrobbel.

[18] Ali Hooshyar and Reza Iravani. 'Microgrid Protection'. In: *Proceedings of the IEEE* 105.7 (2017), pp. 1332–1353. DOI: 10.1109/JPROC.2017.2669342.

[19] Justis- og beredskapsdepartementet. *Forskrift om elektriske forsyningsanlegg § 4-3.* https://lovdata.no/forskrift/2005-12-20-1626/Âğ4-3. 2005.

[20] T. Treider, B. Gustavsen and H. K. Høidalen. 'Analysis of transient earth fault relays in meshed resonant grounded networks'. In: *16th International Conference on Developments in Power System Protection (DPSP 2022)*. Vol. 2022. 2022, pp. 350–355. DOI: 10.1049/icp.2022.0965.

[21] Ehsan Dehghanpour et al. 'Optimal Coordination of Directional Overcurrent Relays in Microgrids by Using Cuckoo-Linear Optimization Algorithm and Fault Current Limiter'. In: *IEEE Transactions on Smart Grid* 9.2 (2018), pp. 1365–1375. DOI: 10.1109/TSG.2016.2587725.

[22] Hassan Eid, H.M. Sharaf and Mostafa Elshahed. 'Optimal Coordination of Directional Overcurrent Relays in Interconnected Networks utilizing User- Defined Characteristics and Fault Current Limiter'. In: *2021 IEEE PES/IAS PowerAfrica*. 2021, pp. 1–5. DOI: 10.1109/PowerAfrica52236.2021.9543303.

[23] Walid El-Khattam and Tarlochan S. Sidhu. 'Restoration of Directional Overcurrent Relay Coordination in Distributed Generation Systems Utilizing Fault Current Limiter'. In: *IEEE Transactions on Power Delivery* 23.2 (2008), pp. 576–585. DOI: 10.1109/TPWRD.2008.915778.

[24] Mojgan Ghanbari, Majid Gandomkar and Javad Nikoukar. 'Protection Coordination of Bidirectional Overcurrent Relays Using Developed Particle Swarm Optimization Approach Considering Distribution Generation Penetration and Fault Current Limiter Placement'. In: *IEEE Canadian Journal of Electrical and Computer Engineering* 44.2 (2021), pp. 143–155. DOI: 10.1109/ICJECE.2020.3018876.

[25] H. H. Zeineldin et al. 'Optimal Protection Coordination for Meshed Distribution Systems With DG Using Dual Setting Directional Over-Current Relays'. In: *IEEE Transactions on Smart Grid* 6.1 (2015), pp. 115–123. DOI: 10.1109/TSG.2014.2357813.

[26] Amin Yazdaninejadi et al. 'Dual-Setting Directional Overcurrent Relays for Protecting Automated Distribution Networks'. In: *IEEE Transactions on Industrial Informatics* 15.2 (2019), pp. 730–740. DOI: 10.1109/TII.2018.2821175.

[27] Hebatallah Mohamed Sharaf, Hatem H. Zeineldin and Ehab El-Saadany. 'Protection Coordination for Microgrids With Grid-Connected and Islanded Capabilities Using Communication Assisted Dual Setting Directional Overcurrent Relays'. In: *IEEE Transactions on Smart Grid* 9.1 (2018), pp. 143–151. DOI: 10.1109/TSG.2016.2546961.

[28] Lucheng Hong et al. 'User-Defined Dual Setting Directional Overcurrent Relays with Hybrid Time Current-Voltage Characteristics-Based Protection Coordination for Active Distribution Network'. In: *IEEE Access* 9 (2021), pp. 62752–62769. DOI: 10.1109/ACCESS.2021.3074426.

[29] S T P Srinivas and K. Shanti Swarup. 'Optimal relay coordination and communication based protection for microgrid'. In: *2017 IEEE Region 10 Symposium (TENSYMP)*. 2017, pp. 1–5. DOI: 10.1109/TENCONSpring.2017.8070034.

[30] Khaled A. Saleh et al. 'Optimal Coordination of Directional Overcurrent Relays Using a New Time–Current–Voltage Characteristic'. In: *IEEE Transactions on Power Delivery* 30.2 (2015), pp. 537–544. DOI: 10.1109/TPWRD.2014.2341666.

[31] Meng Yen Shih et al. 'An Adaptive Overcurrent Coordination Scheme to Improve Relay Sensitivity and Overcome Drawbacks due to Distributed Generation in Smart Grids'. In: *IEEE Transactions on Industry Applications* 53.6 (2017), pp. 5217–5228. DOI: 10.1109/TIA.2017.2717880.

[32] Vasileios A. Papaspiliotopoulos et al. 'Hardware-In-the-Loop Design and Optimal Setting of Adaptive Protection Schemes for Distribution Systems With Distributed Generation'. In: *IEEE Transactions on Power Delivery* 32.1 (2017), pp. 393–400. DOI: 10.1109/TPWRD.2015.2509784.

[33] Z. Liu et al. 'A Multiagent System-Based Protection and Control Scheme for Distribution System With Distributed-Generation Integration'. In: *IEEE Transactions on Power Delivery* 32.1 (2017), pp. 536–545. DOI: 10.1109/TPWRD.2016.2585579.

[34] Ekta Purwar, D. N. Vishwakarma and S. P. Singh. 'A Novel Constraints Reduction-Based Optimal Relay Coordination Method Considering Variable Operational Status of Distribution System With DGs'. In: *IEEE Transactions on Smart Grid* 10.1 (2019), pp. 889–898. DOI: 10.1109/TSG.2017.2754399.

[35] Ekta Purwar, S. P. Singh and D. N. Vishwakarma. 'A Robust and Fast Solving Approach to improve Relays Coordination considering variable sizes of DGs and their outages'. In: *2022 IEEE International Conference on Power Electronics, Smart Grid, and Renewable Energy (PESGRE)*. 2022, pp. 1–6. DOI: 10.1109/PESGRE52268.2022.9715950.

[36] Xindong Liu et al. 'Protection Scheme for Loop-Based Microgrids'. In: *IEEE Transactions on Smart Grid* 8.3 (2017), pp. 1340–1349. DOI: 10.1109/TSG.2016.2626791.

[37] Hannu Jaakko Laaksonen. 'Protection Principles for Future Microgrids'. In: *IEEE Transactions on Power Electronics* 25.12 (2010), pp. 2910–2918. DOI: 10.1109/TPEL.2010.2066990.

[38] M. Amin Zamani, Amirnaser Yazdani and Tarlochan S. Sidhu. 'A Communication-Assisted Protection Strategy for Inverter-Based Medium-Voltage Microgrids'. In: *IEEE Transactions on Smart Grid* 3.4 (2012), pp. 2088–2099. DOI: 10.1109/TSG.2012.2211045.

[39] Eric Sortomme, S. S. Venkata and Joydeep Mitra. 'Microgrid Protection Using Communication-Assisted Digital Relays'. In: *IEEE Transactions on Power Delivery* 25.4 (2010), pp. 2789–2796. DOI: 10.1109/TPWRD.2009.2035810.

[40] David Martin et al. 'Distance protection in distribution systems: How it assists with integrating distributed resources'. In: *2012 65th Annual Conference for Protective Relay Engineers*. 2012, pp. 166–177. DOI: 10.1109/CPRE.2012.6201231.

[41] Aristotelis M. Tsimtsios, George N. Korres and Vassilis C. Nikolaidis. 'A pilot-based distance protection scheme for meshed distribution systems with distributed generation'. In: *International Journal of Electrical Power Energy Systems* 105 (2019), pp. 454–469. ISSN: 0142-0615. DOI: https://doi.org/10.1016/j.ijepes.2018.08.022. URL: https://www.sciencedirect.com/science/article/pii/S0142061518310305.

[42] Rohan Perera and Bogdan Kasztenny. 'Application considerations when protecting lines with tapped and in-line transformers'. In: *2014 67th Annual Conference for Protective Relay Engineers*. 2014, pp. 84–94. DOI: 10.1109/CPRE.2014.6798996.

[43] Aristotelis M. Tsimtsios and Vassilis C. Nikolaidis. 'Towards Plug-and-Play Protection for Meshed Distribution Systems With DG'. In: *IEEE Transactions on Smart Grid* 11.3 (2020), pp. 1980–1995. DOI: 10.1109/TSG.2019.2945694.

[44] Hengwei Lin et al. 'Adaptive distance protection for microgrids'. In: *IECON 2015 - 41st Annual Conference of the IEEE Industrial Electronics Society*. 2015, pp. 000725–000730. DOI: 10.1109/IECON.2015.7392185.

[45] Shuchismita Biswas and Virgilio Centeno. 'A communication based infeed correction method for distance protection in distribution systems'. In: *2017 North American Power Symposium (NAPS)*. 2017, pp. 1–5. DOI: 10.1109/NAPS.2017.8107226.

[46] Fahd Hariri and Mariesa Crow. 'New Infeed Correction Methods for Distance Protection in Distribution Systems'. In: *Energies* 14 (July 2021), p. 4652. DOI: 10.3390/en14154652.

[47] M. Biller et al. 'Protection systems in distribution grids with variable short-circuit conditions'. In: *13th International Conference on Development in Power System Protection 2016 (DPSP)*. 2016, pp. 1–5. DOI: 10.1049/cp.2016.0086.

[48] Nikhil Kumar Sharma and Subhransu Ranjan Samantaray. 'PMU Assisted Integrated Impedance Angle-Based Microgrid Protection Scheme'. In: *IEEE Transactions on Power Delivery* 35.1 (2020), pp. 183–193. DOI: 10.1109/TPWRD.2019.2925887.

[49] Nikhil Kumar Sharma and Subhransu Ranjan Samantaray. 'A Composite Magnitude-Phase Plane of Impedance Difference for Microgrid Protection Using Synchrophasor Measurements'. In: *IEEE Systems Journal* 15.3 (2021), pp. 4199–4209. DOI: 10.1109/JSYST.2020.2999483.

[50] Jerome Nsengiyaremye, Bikash C. Pal and Miroslav M. Begovic. 'Microgrid Protection Using Low-Cost Communication Systems'. In: *IEEE Transactions on Power Delivery* 35.4 (2020), pp. 2011–2020. DOI: 10.1109/TPWRD.2019.2959247.

[51] Tohid Soleymani Aghdam, Hossein Kazemi Karegar and Hatem H. Zeineldin. 'Variable Tripping Time Differential Protection for Microgrids Considering DG Stability'. In: *IEEE Transactions on Smart Grid* 10.3 (2019), pp. 2407–2415. DOI: 10.1109/TSG.2018.2797367.

[52] C. Yuan et al. 'Multilayered Protection Strategy for Developing Community Microgrids in Village Distribution Systems'. In: *IEEE Transactions on Power Delivery* 32.1 (2017), pp. 495–503. DOI: 10.1109/TPWRD.2016.2544923.

[53] Zhiren Liu et al. 'Differential Protection of Active Distribution Networks Based on 5G Communication Technology'. In: *2022 IEEE 5th International Electrical and Energy Conference (CIEEC)*. 2022, pp. 4639–4644. DOI: 10.1109/CIEEC54735.2022.9846621.

[54] E. Sortomme, J. Ren and S. S. Venkata. 'A differential zone protection scheme for microgrids'. In: *2013 IEEE Power Energy Society General Meeting*. 2013, pp. 1–5. DOI: 10.1109/PESMG.2013.6672113.

[55] Haifeng Li et al. 'An adaptive fault-component-based current differential protection scheme for distribution networks with inverter-based distributed generators'. In: *International Journal of Electrical Power Energy Systems* 128 (2021), p. 106719. ISSN: 0142-0615. DOI: https://doi.org/10.1016/j.ijepes.2020.106719. URL: https://www.sciencedirect.com/science/article/pii/S0142061520342630.

[56] Vassilis C. Nikolaidis et al. 'A Coordinated Multi-Element Current Differential Protection Scheme for Active Distribution Systems'. In: *IEEE Transactions on Power Delivery* 37.5 (2022), pp. 4261–4271. DOI: 10.1109/TPWRD.2022.3148209.

[57] Syed Basit Ali Bukhari et al. 'An interval type-2 fuzzy logic based strategy for microgrid protection'. In: *International Journal of Electrical Power &amp Energy Systems* 98 (June 2018), pp. 209–218. DOI: 10.1016/j.ijepes.2017.11.045. URL: https://doi.org/10.1016/j.ijepes.2017.11.045.

[58] Debi Prasad Mishra, Subhransu Ranjan Samantaray and Geza Joos. 'A Combined Wavelet and Data-Mining Based Intelligent Protection Scheme for Microgrid'. In: *IEEE Transactions on Smart Grid* 7.5 (2016), pp. 2295–2304. DOI: 10.1109/TSG.2015.2487501.

[59] Susmita Kar, S. R. Samantaray and M. Dadash Zadeh. 'Data-Mining Model Based Intelligent Differential Microgrid Protection Scheme'. In: *IEEE Systems Journal* 11.2 (2017), pp. 1161–1169. DOI: 10.1109/JSYST.2014.2380432.

[60] Vinod V. Vijayachandran and U. Jayachandra Shenoy. 'Implementation of Support-Vector-Machine-Based Relay Coordination Scheme for Distribution System With Renewables'. In: *IEEE Journal of Emerging and Selected Topics in Industrial Electronics* 2.3 (2021), pp. 324–333. DOI: 10.1109/JESTIE.2020.3014875.

[61] James J. Q. Yu et al. 'Intelligent Fault Detection Scheme for Microgrids With Wavelet-Based Deep Neural Networks'. In: *IEEE Transactions on Smart Grid* 10.2 (2019), pp. 1694–1703. DOI: 10.1109/TSG.2017.2776310.

[62] Jerome Nsengiyaremye, Bikash C. Pal and Miroslav M. Begovic. 'Low-Cost Communication-Assisted Line Protection for Multi-Inverter Based Microgrids'. In: *IEEE Transactions on Power Delivery* 36.6 (2021), pp. 3371–3382. DOI: 10.1109/TPWRD.2020.3039176.

[63] Hany F. Habib et al. 'Multi-Agent-Based Technique for Fault Location, Isolation, and Service Restoration'. In: *IEEE Transactions on Industry Applications* 53.3 (2017), pp. 1841–1851. DOI: 10.1109/TIA.2017.2671427.

[64] B. Kasztenny, I. Voloh and E.A. Udren. 'Rebirth of the phase comparison line protection principle'. In: *59th Annual Conference for Protective Relay Engineers, 2006.* 2006, 60 pp.-. DOI: 10.1109/CPRE.2006.1638704.

[65] Hariss Nicorescu, Lucian Toma and Mircea Eremia. 'Fast Detection of Grid Faults using Synchronized Measurements'. In: *2019 11th International Symposium on Advanced Topics in Electrical Engineering (ATEE)*. 2019, pp. 1–6. DOI: 10.1109/ATEE.2019.8724912.

[66] Henrik Lundqvist, Jan Erik Håkegård and Arne Lie. 'Mobile Networks for Smart Grid Revisited'. In: *2020 6th IEEE International Energy Conference (ENERGYCon)*. 2020, pp. 882–887. DOI: 10.1109/ENERGYCon48941.2020.9236595.

[67] 3rd Generation Partnership Project (3GPP). *3GPP TS 22.104 V19.0.0: Service requirements for cyber-physical control applications in vertical domains; Stage 1 (Release 19)*. Tech. rep. 650 Route des Lucioles - Sophia Antipolis, Valbonne - FRANCE: 3GPP, Mar. 2023. URL: https://portal.3gpp.org/desktopmodules/Specifications/SpecificationDetails.aspx?specificationId=3528.

[68] P. Hovila et al. 'CELLULAR NETWORKS PROVIDING DISTRIBUTION GRID COMMUNICATIONS PLATFORM'. In: *CIRED 2021 - The 26th International Conference and Exhibition on Electricity Distribution*. Vol. 2021. 2021, pp. 1207–1211. DOI: 10.1049/icp.2021.1981.

[69] Petri Hovila et al. '5G NETWORKS ENABLING NEW SMART GRID PROTECTION SOLUTIONS'. In: June 2019.

[70] Peyman Jafary, Antti Supponen and Sami Repo. 'Network Architecture for IEC61850-90-5 Communication: Case Study of Evaluating R-GOOSE over 5G for Communication-Based Protection'. In: *Energies* 15.11 (2022). ISSN: 1996-1073. DOI: 10.3390/en15113915. URL: https://www.mdpi.com/1996-1073/15/11/3915.

[71] Konstantinos Kousias et al. 'Coverage and Performance Analysis of 5G Non-Standalone Deployments'. In: WiNTECH '22. Sydney, NSW, Australia: Association for Computing Machinery, 2022, pp. 61–68. ISBN: 9781450395274. DOI: 10.1145/3556564.3558233. URL: https://doi.org/10.1145/3556564.3558233.

[72] International Electrotechnical Commission. *Communication networks and systems for power utility automation - Part 90-12: Wide area network engineering guidelines*. Technical Report IEC TR 61850-90-12. IEC, July 2020.

[73] 3rd Generation Partnership Project (3GPP). *Study on Scenarios and Requirements for Next Generation Access Technologies*. Tech. rep. 38.913 V17.0.0. Release 17. Technical Specification Group Radio Access Network, Mar. 2022. URL: https://portal.3gpp.org/desktopmodules/Specifications/SpecificationDetails.aspx?specificationId=2996.

[74] Paolo Tenti et al. 'Generalized symmetrical components for periodic non-sinusoidal three-phase signals'. In: *Electrical Power Quality and Utilisation Journal* 13.1 (2007), pp. 9–15.

[75] Eric Jacobsen and Richard Lyons. 'The sliding DFT'. In: *Signal Processing Magazine, IEEE* 20 (Apr. 2003), pp. 74–80. DOI: 10.1109/MSP.2003.1184347.

[76] Eric Jacobsen and Richard Lyons. 'An update to the sliding DFT'. In: *Signal Processing Magazine, IEEE* 21 (Feb. 2004), pp. 110–111. DOI: 10.1109/MSP.2004.1516381.

[77] Hatem A. Darwish and Magdy Fikri. 'Practical Considerations for Recursive DFT Implementation in Numerical Relays'. In: *IEEE Transactions on Power Delivery* 22.1 (2007), pp. 42–49. DOI: 10.1109/TPWRD.2006.874642.

[78] Karel Máslo and Martin Procházka. 'Frequency measurement in the power system'. In: *2018 19th International Scientific Conference on Electric Power Engineering (EPE)*. 2018, pp. 1–5. DOI: 10.1109/EPE.2018.8395979.

[79] wavewalkerdsp. *Single Pole IIR Filter Frequency Response*. Accessed: 2023-04-05. July 2022. URL: https://www.wavewalkerdsp.com/2022/07/06/single-pole-iir-filter-frequency-response/.

[80] Duraisamy Sundararajan. *Discrete Fourier transform, the: Theory, algorithms and applications*. Singapore, Singapore: World Scientific Publishing, May 2001.

[81] *Veileder til leveringskvalitetsforskriften*. Standard. Oslo: Norges vassdrags- og energidirektorat, 2018.

[82] A G Phadke and J S Thorp. *Synchronized phasor measurements and their applications*. en. Power Electronics and Power Systems. New York, NY: Springer, July 2008.

[83] Wei Huang. 'Learn IEC 61850 configuration in 30 minutes'. In: *2018 71st Annual Conference for Protective Relay Engineers (CPRE)*. 2018, pp. 1–5. DOI: 10.1109/CPRE.2018.8349803.

[84] *Instrument transformers Part 1: General requirements*. Standard. Geneva, CH: International Electrotechnical Commission, 2007.

[85] *Instrument transformers Part 6: Additional general requirements for low-power instrument transformers*. Standard. Geneva, CH: International Electrotechnical Commission, 2006.

[86] *Instrument transformers Part 2: Additional requirements for current transformers*. Standard. Geneva, CH: International Electrotechnical Commission, 2012.

[87] *Instrument transformers Part 10: Additional requirements for low-power passive current transformers*. Standard. Geneva, CH: International Electrotechnical Commission, 2017.

[88] Songzhe Zhu et al. 'Modeling Inverter-Based Resources in Stability Studies'. In: *2018 IEEE Power Energy Society General Meeting (PESGM)*. 2018, pp. 1–5. DOI: 10.1109/PESGM.2018.8586157.

[89] Machowski. *Power system dynamics - stability and control, 3rd edition*. 3rd ed. Hoboken, NJ: Wiley-Blackwell, Mar. 2020.

[90] J Keller and B Kroposki. 'Understanding Fault Characteristics of Inverter-Based Distributed Energy Resources'. In: (Jan. 2010). DOI: 10.2172/971441. URL: https://www.osti.gov/biblio/971441.

[91] Md Alamgir Hossain et al. 'Overview of AC Microgrid Controls with Inverter-Interfaced Generations'. In: *Energies* 10.9 (2017). ISSN: 1996-1073. DOI: 10.3390/en10091300. URL: https://www.mdpi.com/1996-1073/10/9/1300.

[92] European Commission. *Implementation of the Network Code on Requirements for Grid Connection of Generators*. 2021. URL: https://op.europa.eu/en/publication-detail/-/publication/ee9ecda7-6788-11eb-aeb5-01aa75ed71a1/language-en (visited on 18/10/2022).

[93] *Nasjonal veileder for funksjonskrav i kraftsystemet*. Standard. https://www.statnett.no/for-aktorer-i-kraftbransjen/nyhetsarkiv/statnett-publiserer-i-dag-oppdaterte-retningslinjer-for-utovelsen-av-systemansvaret/. Oslo: Statnett, 2022.

[94] *Requirements for generating plants to be connected in parallel with distribution networks Part 1: Connection to a LV distribution network Generating plants up to and including Type B*. Standard. Geneva, CH: International Electrotechnical Commission, 2019.

[95] *HØRINGSUTKAST @ NVF 2023 Nasjonal Veileder for Funksjonskrav i kraftsystemet*. Standard. https://www.statnett.no/globalassets/for-aktorer-i-kraftsystemet/systemansvaret/retningslinjer---horinger/22-01071-1-horingsutkast-nvf-2023---horing-desember-2022.pdf. Oslo: Statnett, 2022.

[96] SINTEF. *Planleggingsbok for kraftnett, Tekniske data*. Norwegian. SINTEF Energi AS. 37 pp. January 01, 2010.

[97] Nalla Lokesh and Mahesh K. Mishra. 'A Comparative Performance Study of Advanced PLLs for Grid Synchronization'. In: *2020 IEEE International Conference on Power Electronics, Smart Grid and Renewable Energy (PESGRE2020)*. 2020, pp. 1–6. DOI: 10.1109/PESGRE45664.2020.9070288.

[98] Lokesh Nalla. *DSOGI based PLL*. GitHub repository. 2023. URL: https://github.com/NallaLokeshReddy/Matlab-Simulink/releases/tag/1.0.1.

[99] Joan Rocabert et al. 'Control of Power Converters in AC Microgrids'. In: *IEEE Transactions on Power Electronics* 27.11 (2012), pp. 4734–4749. DOI: 10.1109/TPEL.2012.2199334.

[100] Zhikang Shuai et al. 'Fault Analysis of Inverter-Interfaced Distributed Generators With Different Control Schemes'. In: *IEEE Transactions on Power Delivery* 33.3 (2018), pp. 1223–1235. DOI: 10.1109/TPWRD.2017.2717388.

[101] Amirnaser Yazdani and Reza Iravani. *Voltage-sourced converters in power systems*. en. Wiley - IEEE. Hoboken, NJ: Wiley-Blackwell, Mar. 2010.

[102] *libIEC61850 / lib60870 open source libraries for IEC 61850 and IEC 60870-5-101/104*. Mar. 2022. URL: https://libiec61850.com/.

[103] Stanley H Horowitz, Arun G Phadke and James K Niemira. *Power System Relaying*. en. 4th ed. Nashville, TN: John Wiley & Sons, Jan. 2014.

[104] Qian Li et al. 'Analysis and verification of a novel current comparison pilot protection'. In: *2017 IEEE Conference on Energy Internet and Energy System Integration (EI2)*. 2017, pp. 1–5. DOI: 10.1109/EI2.2017.8245260.

[105] Glenn Swift, Dave Fedirchuk and Tom Ernst. 'Arcing Fault 'Resistance' (It Isn't)'. In: *Georgia Tech Fault and Disturbance Analysis Conference*. NxtPhase Corporation and Minnesota Power. Atlanta, GA, May 2003. URL: https://truc.org/wp-content/uploads/2014/08/09fda_2003_swift_arcingfault.pdf.

[106] Hadi Saadat. *Power System Analysis*. 3rd ed. Psa Pub, Mar. 2011.

[107] Aurora Marie Fosli Flataker. 'Voltage-dependency of loads and its role in voltage control strategies'. MA thesis. Norwegian University of Science and Technology, June 2019.

[108] 'IEEE Guide for Load Modeling and Simulations for Power Systems'. In: *IEEE Std 2781-2022* (2022), pp. 1–88. DOI: 10.1109/IEEESTD.2022.9905546.

[109] Olje- og energidepartementet. *Forskrift om leveringskvalitet i kraftsystemet § 3.3*. https://lovdata.no/forskrift/2004-11-30-1557/Âğ3-3. 2019.

[110] 'IEEE Standard for Ratings and Requirements for AC High-Voltage Circuit Breakers with Rated Maximum Voltage Above 1000 V'. In: *IEEE Std C37.04-2018 (Revision of IEEE Std C37.04-1999)* (2019), pp. 1–122. DOI: 10.1109/IEEESTD.2019.8726456.

[111] Siemens. *Types 3AH3 and 3AHc vacuum circuit breaker operator modules: 4.16 kV to 38 kV Installation operation maintenance*. Siemens. URL: https://assets.new.siemens.com/siemens/assets/api/uuid:33735c53-822c-4ad4-bdca-7c90d5008912/ansi-mv-ovcb-3ah3-im-en.pdf.

[112] *R-MAG Magnetically Actuated Dead Tank Outdoor Vacuum Circuit Breaker Instruction Manual*. ABB. URL: https://search.abb.com/library/Download.aspx?DocumentID=1YEPMSR0020E001&LanguageCode=en&DocumentPartId=&Action=Launch.

[113] GE Energy Connections. *SecoGear Medium-voltage Switchgear Application and Technical Guide DET-882*. General Electric, 2016.

[114] Siemens Power Transmission & Distribution, Inc. *TechTopics No. 6: 3-Cycle vs. 5-Cycle Interrupting Time*. Apr. 2001. URL: https://npeinc.com/manuals/Adobe%5C%20E-Manuals/AC%5C%20Stuff%5C%20from%5C%20Voyten/Tec%5C%20Topics/interrupting%5C%20time.pdf.

[115] *Open Data Interface Specification*. Webpage. [Retrieved on April 10, 2023]. A-1060 Wien, Mariahilfer Straße 77-79. URL: https://www.netztest.at/en/Opendata.

[116] A R van C. Warrington. *Protective relays*. en. New York, NY: Springer, Feb. 1968.

[117] V.V. Terzija and H.-J. Koglin. 'On the modeling of long arc in still air and arc resistance calculation'. In: *IEEE Transactions on Power Delivery* 19.3 (2004), pp. 1012–1017. DOI: 10.1109/TPWRD.2004.829912.

[118] Houlei Gao and P.A. Crossley. 'Design and evaluation of a directional algorithm for transmission-line protection based on positivesequence fault components'. In: *Generation, Transmission and Distribution, IEE Proceedings*- 153 (Dec. 2006), pp. 711–718. DOI: 10.1049/ip-gtd:20050379.

[119] Tai-Ying Zheng et al. 'Protection algorithm for a wind turbine generator based on positive- and negative-sequence fault components'. In: *2011 International Conference on Advanced Power System Automation and Protection*. Vol. 2. 2011, pp. 1115–1120. DOI: 10.1109/APAP.2011.6180548.

[120] loldrup. *Given circle and point, where does the tangential line through the point touch the circle?* [https://math.stackexchange.com/questions/913239/given-circle-and-point-where-does-the-tangential-line-through-the-point-touch-t]. Sept. 2014.

A Code, Grid parameters, and Relay parameters

A.1 Code

The Grader can find the code in the attached files. External readers can ask the author for the code not included in the method chapters.

A.2 IIDG parameters and tuning

Parameters for the IIDG are given in Table A.1. Keep in mind that the DC value was only used to find the gain to have before the controlled voltage sources. The gain was found to be 697.08.

Table A.1: Parameters for IIDG. Table from project report [1].

IIDG	$\mathbf{V_{DC}}$ [V]	$\mathbf{V_{inv}}$ [V]	$\mathbf{L_f}$ [mH]	$\mathbf{C_f}$ [µF]
Values	1200	690	0.101	1.671

Table A.2 gives the IIDG controller parameters.

Table A.2: IIDG control parameters

Controller Type	**Parameter**	**Value**	**Units**	**Comments**
Voltage Controller	KP	4	-	-
	KI	60	-	-
	f	50	Hz	-
	vd_{ref}	563	V	Peak phase to earth (LL-RMS 690 V)
	vq_{ref}	0	V	-
Power Controller	P_{ref}	1	MW	-
	Q_{ref}	0.48	MVAR	-
Current Limiter	$I_{thermal,grid-connected}$	1311*1.2	A	1.2 factor can be varied to 2
	$I_{thermal,islanded}$	6900*1.2	A	1.2 factor can be varied to 2
Current Controller	KP	0.5	-	-
	KI	40	-	-

When tuning, the approach was to first tune the parameters of the inner-control loop. This was done by automating 500 simulations in grid-connected mode so that the voltage controller has no impact. Each simulation had a different set of PI constants, and each simulation had a close in three-phase fault to test simulation stability. After 50 ms, the fault was removed/extinguished, and after an additional 100 ms, the steady-state deviation between the reference and actual inverter dq current was calculated. To end the process, the 5 simulations with the lowest steady-state deviation were manually evaluated, and the parameters yielding the ”best” response were chosen.

A similar process was repeated for tuning the parameters of the outer control loop. Now the operation is islanded, and the parameters of the inner control loop is the one found in the paragraph above. Instead of calculating the steady-state deviation in current, now the steady-state deviation of voltage is plotted. After running 500 simulations and manually evaluating the 5 with the lowest steady-state deviation the parameter for the voltage controller was found.

A.3 SGDG Parameters

As was the case in the project report [1], parameters for the SGDG are found in [5].

Table A.3: Parameters for SGDG (salient poled small scale hydro generator). Since salient poled $x_q = x'_q$ and $T'_q = 0$. Table from project report [1].

SGDG	**Vt**[kV]	[$\mathbf{x_d}$ $\mathbf{x'_d}$ $\mathbf{x''_d}$ $\mathbf{x_q}$ $\mathbf{x''_q}$ $\mathbf{x_l}$] [pu]	**[Tdt, Tdst, Tqst]** [s]	**H** [s]	**Friction factor** [pu]	**Pole pairs**
Values	0.690	[1.65, 0.3, 0.2, 0.9, 0.21, 0.04]	[0.6, 0.006, 0.07]	3	0.1178	8

As the AVR or governor have little impact right after the fault, they were not included. The field voltage and mechanical power are therefore found automatically by steady-state analysis in Simulink. As there are no AVR or Governor, the SGDG will be unstable post-fault. Therefore, When using SGDG, the simulation is stopped 50 ms post-fault.

A.4 Relay Parameters

Table A.4 gives the parameters for the relay. A setting of $t_{DR->CR,communication,max}$ equal to 50 ms was used as all WAN time-delay was modeled between the DR and CR.

Table A.4: Parameters used for the DR and CR.

	Parameter	**Value**	**Comment**
DR	frequency-estimator	'on'	
	ϕ_{CCA}	90°	
	$I_{CCA,disable}$		Implemented according to Equation 56
	ϵ_{up}	1.1	
	ϵ_{down}	0.9	
CR	t_{CCA}	4 ms	
	t_{IJump}	4 ms	
	$t_{DR->CR,communication,max}$	50 ms	Set to zero before taking WAN into account

B Explainers

B.1 Algorithm in the central relay that finds CB to trip given the fault location

This part explains the algorithm used in the CR that takes in the faulty line and finds which CB to trip using the current grid topology. Keep in mind that the algorithm is necessary as in a future where only a few CBs are used and DNR is used, the CBs that selectively isolate a given line fault might change with time as the grid topology changes. The problem can be formulated as follows:

Given the knowledge of the topology, the positions and states of the CBs, and the positions and states of LBs, the objective is to determine which CBs to trip in order to selectively isolate a specified faulty bus or line. The result of the algorithm is the updated status of the circuit breakers.

The author is not aware of any algorithm that can effectively address the issue. In light of this, a novel algorithm has been devised by the author to address this problem.

Information about the topology and switch gears

The information regarding the current topology, the positions and states of the CBs, and the positions and states of the LBs is stored in three distinct matrices, respectively referred to as the topology matrix, CB matrix, and LB matrix. They are all square matrices with the dimension equal to the number of buses in the grid. Additionally, the element on the diagonal is always zero. The next paragraph will explain what conditions need to be true for there to be non-zero elements in the matrices.

The rules for the topology matrix are explained in Figure B.1 for a 9-bus system. Observe that the upper triangular elements represent if two buses are directly connected through a line/cable, and the lower triangular elements say if the line section is located along a bus with power generation.

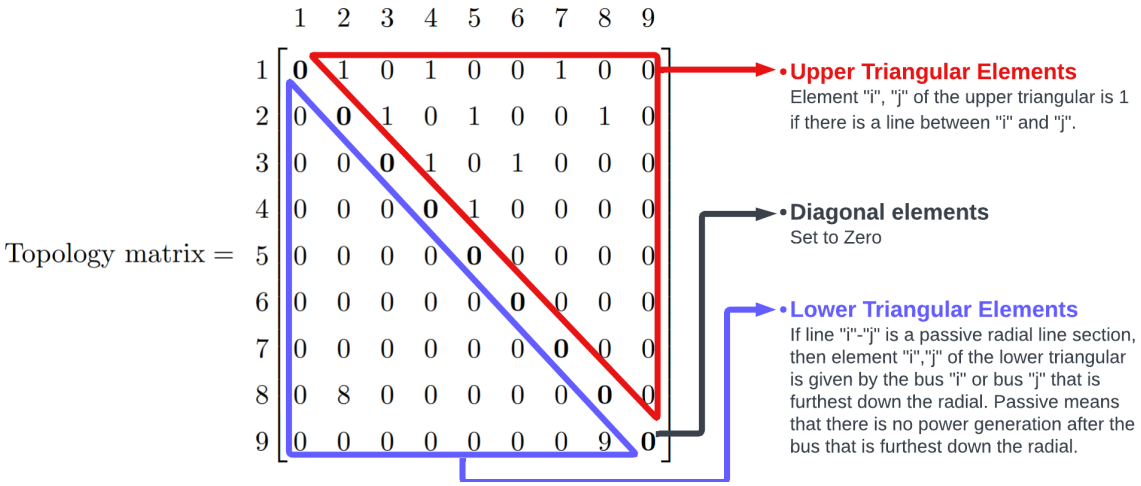


Figure B.1: Shows the rules for the Topology matrix with the example of a system with 9 buses.

The rules for the CB matrix are depicted in Figure B.2. For the CB matrix, the element at row ”i” and column ”j” is ”1” if there is a closed circuit breaker at bus ”i” towards bus ”j”. If the circuit breaker is open the element has the number 2.

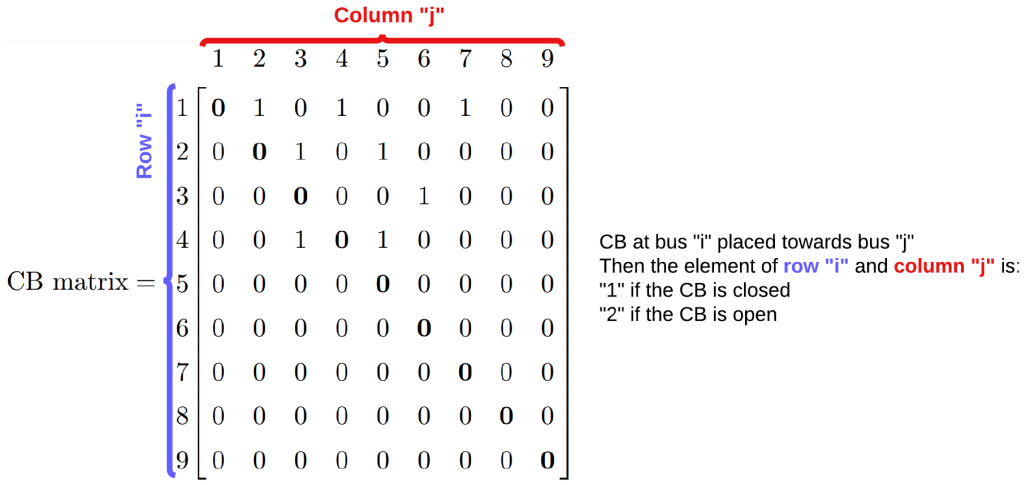


Figure B.2: Shows the rules for the CB matrix with the example of a system with 9 buses.

The LB matrix is similar to the CB matrix, but it uses the status of the load break switches.

Algorithm to locate the CB

The input to the algorithm is the line status, topology matrix, CB matrix, and LB matrix. The output of the algorithm is the updated CB matrix. The updated CB matrix can then be used to send control signals to CBs. The flowchart/pseudocode for the algorithm is shown in Figure B.4 it will now be explained in steps corresponding to the numbers in the figure. The central concept is that the algorithm tries to isolate a bus by opening a CB in the fault direction (step 4) if this does not work it tries to open a CB in the direction of the connected neighbors (step 5) if this does not work it will jump to isolate the neighbors and repeat this steps. Keep in mind that it takes into account if any CB/LBS is already open or if it is along a radial line, and that the algorithm uses large pre-allocated vectors with zero padding to avoid expanding them during execution.

Step 1: Examine the input to identify if a line has *become* faulty. If multiple lines exhibit a detected fault, the remaining algorithm will execute one time for each faulty line.

Step 2: Create three vectors called ”isolate”, ”direction” and ”has_been”. ”isolate” contains the designated buses for isolation, and ”direction” denotes the corresponding direction/bus that leads to the fault. An ”index” variable tracks the index before the zero padding. Finally, the ”has_been” vector denotes the buses visited by the algorithm, initialized with a value of zero, and an index (not depicted) tracking the element preceding zero padding. In Figure B.4 an example is shown where line element A-B is faulty.

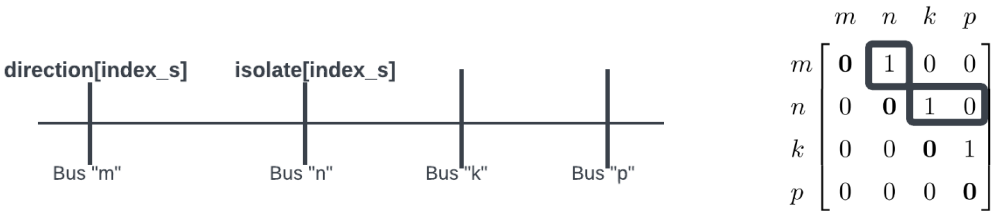
Step 3: index_s is made equal to ”index”. It contains the index of the bus to be isolated in this iteration. Furthermore, append isolate[index_s] to the has_been vector (bracket notation means the ”index_s” element of the vector).

Step 4: The buses isolate[index_s] direction[index_s] are denoted as n and m, respectively (see Figure B.3a). The goal of the step is to check if there can flow a fault current from bus n toward bus m, if it can then try to open a CB. If there is no available CB identify neighboring buses. This is done in the following four operations. If an operation returns ”yes” skip to step 7.

- Check if bus n is a passive radial bus by using the lower triangular elements with index m and n in the topology matrix.
- If not radial check if row n and column m of the CB and LBS matrix has a number 2 indicating an open CB/LBS at bus n in the direction of m.
- If not open CB/LBS check if row n and column m of the CB matrix is equal to 1. This indicates a closed CB at bus n in the direction of bus m. If a CB is a closed update the CB matrix to ”2” at row n and column m.
- Identify the neighbors to the current bus (bus n). The neighbors of bus n are given by the non-zero elements of the upper triangular elements of row ”n” and column n of the topology matrix, see the three elements in the boxes of Figure B.3b.

Step 5: Iterate through all identified neighbors ”k” and identify if there can be a fault current from bus k towards bus n. If there can be a fault current, check if a CB at bus n can interrupt the current. The step uses four operations and only proceeds to the next if the preceding gave ”no”.

- If ”k” has been in the vector ”isolate” before then skip k to avoid infinite loops.
- If the bus k for line n-k is a radial bus it does not need to be isolated by CB.
- If there is an open CB or LBS at the line-section n-k.
- If there is a CB at bus n towards bus k, then update the CB_matrix



(a) Topology **(b)** Topology matrix

Figure B.3: Example Topology and Topology matrix used to explain the algorithm.

Step 6: There are no CB at bus n to interrupt the fault current from bus k towards bus n. Therefore bus ”k” needs to be isolated in the direction of bus ”n”. Increment ”index” by 1 (index++) and at this index in the isolate and direction vector place ”k” and ”n”, respectively.

Step 7: Delete the index_s element from the isolate and direction vector. Decrement the ”index” by 1.

Step 8: If the ”index” is zero there are no more buses that need isolation and the algorithm is finished. The CBs will receive in accordance with the updated CB_matrix

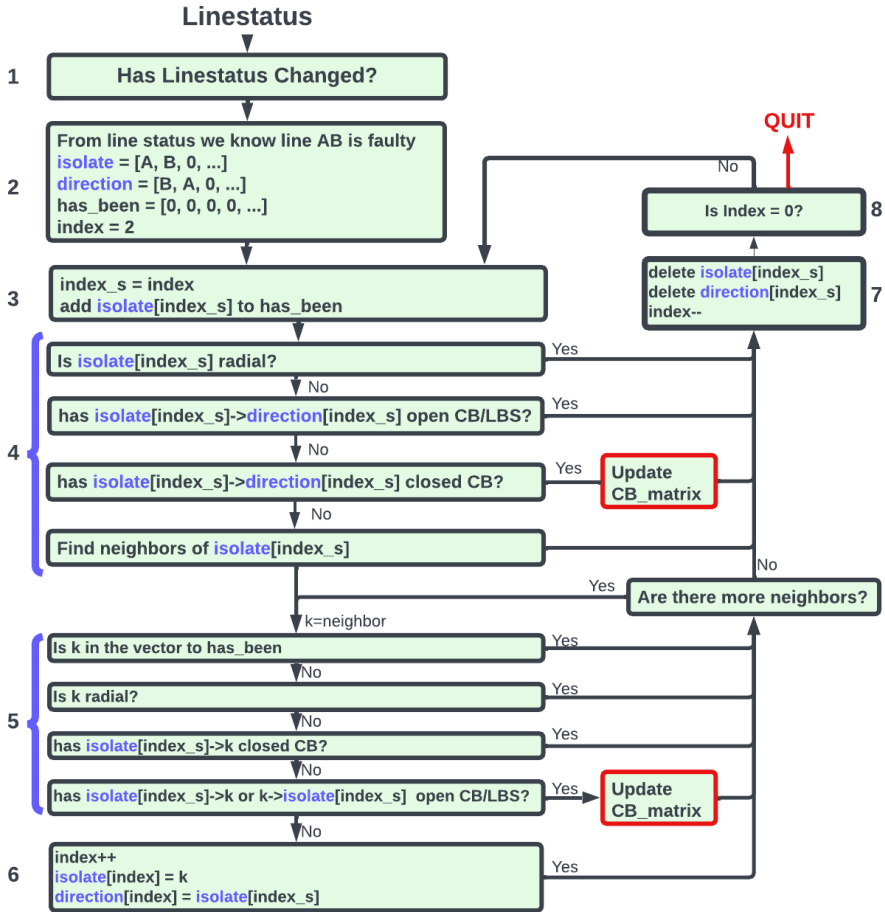


Figure B.4: Flowchart for the algorithm that finds which CB to trip based on the line-status input.

B.2 Expected maximum fault resistance for two and three-phase faults

In the ungrounded network during two and three-phase faults it is the impedance of the arc, typically modeled as a resistance, that must be considered.

Based on experiments of less than 1000 A Warrington constructed a empirical relation for the arc resistance [116]:

$$R_f = \frac{28707}{I^{1.4}} L \tag{60}$$

In the equation, L is the arc length in meters and I is the RMS current in the arc. Keep in mind that in a 22 kV network the distance between phases is typically 1-2 meter [96], but the arc can be curved and its length can vary with time. However, in our case, the protection scheme should work right after fault meaning that the arc has no time to expand and therefore 2 m is used as an upper limit.

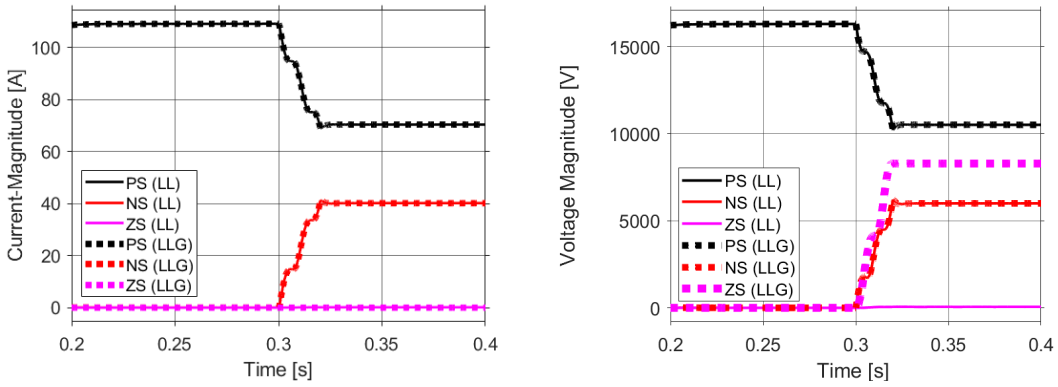
It is hard to provide a minimum fault current as the fault current is dependent on the fault resistance. Nevertheless, the short circuit level during islanded with only IIDG the IIDG provides 6.7 MVA to cover all the loads resulting in an IIDG RMS current of 175 A on the 22 kV side. If the max IIDG current is 1.2 times the nominal current and if all current went to the fault (unrealistic) Warrington's would give 32.3 Ω. At this point, the scheme approaches a situation where simulation results show that the scheme can fail. However, more recent lab measurement done by [117] indicates that the Warrington formula might give too large resistance for low current faults and their results give only 10 Ω at this current level.

To build an understanding of how the scheme work and to take into account the uncertainty of the fault resistance faults will be conducted at a wide range of fault currents, but keep in mind if the updated laboratory experiment is taken into account a fault resistance of 20 Ω can be taken as an upper limit (corresponds to 2 m and fault current of only 100 A in [117]).

B.3 LL versus LLG fault in an ungrounded network

A LL and LLG fault in an ungrounded network will ideally have the same per-phase currents and the same PS/NS voltage, however, an LLG will in comparison to a LL fault have a ZS voltage. As the protection algorithm only uses the positive sequence current, a LL and LLG fault gives the same protection response and only LL faults are done in the simulation. The same currents and PS/NS voltage is due to the infinite value of the zero sequence Thevenin impedance at the fault point resulting in the ZS networks do not influence the PS or NS network. The ZS voltage is due to the LLG fault causing a neutral point shift, but due to the infinite impedance, it does not cause a current.

In Figure B.5a the PS, NS, and ZS currents are shown for an LL and LLG faults as the dotted line (LLG) overlaps the solid lines (LL) of the same color it is confirmed that the currents are equal. Keep in mind that in the figure it is the current downstream of a fault on a radial section that is shown the impedance between the phases are 5 Ω. In Figure B.5b the lines that do not overlap are the lines representing the zero sequence voltage showing that in an LLG fault, there is substantial ZS voltage and as earlier explained this is because the neutral point shift caused by the ground fault causes the phase to earth voltage of the healthy phase to attain line voltage.



(a) Currents **(b)** Voltage

Figure B.5: Sequence components after LL and LLG fault. Measurement is done downstream of the fault on a passive radial section.

B.4 Explanation of the Fault component

This subsection is a direct copy of the project report [1]. Figure B.6 illustrates that the actual circuit during a fault can be thought of as a superposition of the load and fault component. As described in [118], the pre-fault voltage at the fault point is the only source in the fault component. Therefore, the fault component's currents and voltages are largely independent of pre-fault loading. If the fault component currents and voltage are known, the idea is that it should be easier to create protection schemes for the fault component due to its load independence. It is however challenging to obtain the fault component currents and voltages. Let $x(t)$

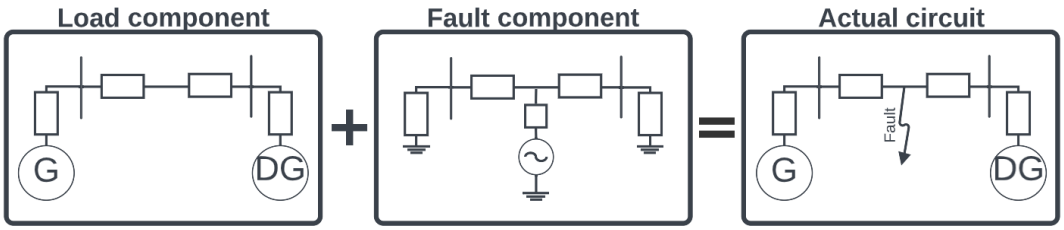


Figure B.6: Illustrates the idea of the fictional "fault component" circuit.

be the measured value, $\dot{x}(t)$ be the fault component and $x_L(t)$ be the load component. The superposition principle gives (61) which can be used to express the fault component in (62).

$$x_L(t) + \dot{x}(t) = x(t) \tag{61}$$

$$\dot{x}(t) = x(t) - x_L(t) \tag{62}$$

In (62) only $x(t)$ can be measured. $x_L(t)$ cannot be measured, but it varies slowly and is therefore approximated by a time-delayed pre-fault measurement [119]. This yields the fault component $\dot{x}(t)$

$$\dot{x}(t) \approx x(t) - x(t - T * k), \tag{63}$$

Where T is the fundamental power cycle and k is a positive integer.

B.5 Deriving equation for maximum pre-fault angle difference across a line

Assume there is a circle with radius "r" on the positive x-axis with a center given by c_x. r is less than c_x. There is also a line that goes through the origin and is tangential to the circle. The goal is to find the x_t and y_t which gives the coordinate where the line touches the circle and use this to find the angle between the line and the x-axis. According to the formula in the forum post in [120], which was verified by me, the x_t value is given by:

$$x_t = \frac{c_x(p_x - c_x)^2 + r^2(p_x - c_x)}{(p_x - c_x)^2} \tag{64}$$

In our case, the points that the line should cross is the origin meaning $p_x = 0$:

$$x_t = c_x - \frac{r^2}{c_x} \tag{65}$$

For simplicity of the continued derivation, this can be written as:

$$x_t = c_x(1 - \frac{r^2}{c_x^2}) \tag{66}$$

The equation for the circle is:

$$(x - c_x)^2 + y^2 = r^2 \tag{67}$$

Solving for y_t:

$$y_t = \sqrt{r^2 - (x_t - c_x)^2} \tag{68}$$

Now inserting the expression for x_t found in Equation 66, one obtains:

$$y_t = \sqrt{r^2 - (c_x(1 - \frac{r^2}{c_x^2}) - c_x)^2} \tag{69}$$

Simplifying the expression one gets:

$$y_t = \sqrt{r^2 - c_x^2(\frac{r^2}{c_x^2})^2} \tag{70}$$

this gives:

$$y_t = \sqrt{r^2 - \frac{r^4}{c_x^2}} \tag{71}$$

Which gives:

$$y_t = r\sqrt{1 - \frac{r^2}{c_x^2}} \tag{72}$$

To find the angle one takes the inverse tangent of y_t divided by x_t:

$$\delta_{max} = \arctan \frac{r\sqrt{1 - \frac{r^2}{c_x^2}}}{c_x(1 - \frac{r^2}{c_x^2})} \tag{73}$$

This simplifies to:

$$\delta_{max} = \arctan \frac{1}{\frac{c_x}{r}\sqrt{(1 - \frac{r^2}{c_x^2})}} \tag{74}$$

Which finally yields the following:

$$\delta_{max} = \arctan \frac{1}{(\frac{c_x}{r})^2 - 1} \tag{75}$$

Now according to Section 7.9.2 the radius is given by the magnitude of the capacitive current and the center of the circle is given by the magnitude of the line current, yielding:

$$\delta_{max} = \arctan \frac{1}{(\frac{I_1}{V_1 \omega C'_d l})^2 - 1} \tag{76}$$

The final step and the equation used in the main body are to express the equation by using the rated line voltage:

$$\delta_{max} = \arctan \frac{1}{\sqrt{(\frac{1}{\frac{V_{rated}}{\sqrt{3}I_1} \omega C'_d l})^2 - 1}} \tag{77}$$

B.6 Setting up Raspberry Pi for IEC61850 Communication

B.6.1 Installation of Raspberry Pi OS

First, install an operating system on the Raspberry Pi. We used Raspberry Pi OS (32-bit). The application Raspberry Pi Imager (https://www.raspberrypi.com/software/) can be downloaded on your Windows or Mac PC. Then, with an SD card reader, the Raspberry Pi OS is downloaded onto the SD card. The Imager also has a settings button (southeast corner) where the password and username can be configured.

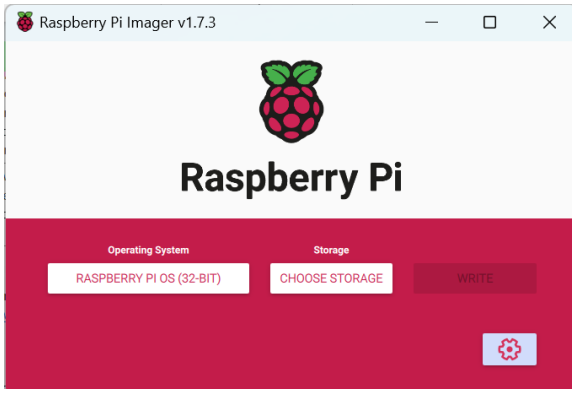


Figure B.7: Raspberry PI Imager

B.6.2 Connecting the Raspberry Pi to the Internet

Subsequent installations require an internet connection. The simplest approach is to use an Ethernet cable, but it is often reserved for IEC61850 communication. In that case, NTNU has an NTNU-IOT internet for Wi-Fi connection of IoT devices.

NTNU-IOT is a hidden SSID network without a password, meaning that it will not automatically show in the Wi-Fi dropdown menu. But once the IT department has added the MAC address of the Raspberry Pi to their list, the Pi will automatically connect to this network (with some extra configuration). The MAC address is found by running the ”ifconfig” command and extracting the WLAN MAC address, which in the example below is e4:5f:01:bd:76:c0:

For the Raspberry Pi to connect to the hidden ssid, you need to change the content of the $wpa\_supplicant.conf$ file. This is done by using the following command:

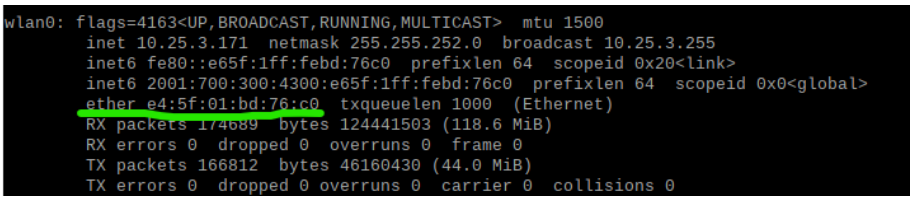


Figure B.8: WLAN MAC address found by using the ifconfig command

```
sudo nano /etc/wpa_supplicant/wpa_supplicant.conf
```

Then edit the file to be:

```
ctrl_interface=DIR=/var/run/wpa_supplicant GROUP=netdev
update_config=1

network={
ssid="NTNU-IOT"
scan_ssid=1
key_mgmt=NONE
}
```

Finally, reboot the machine.

B.6.3 Installing tools (Wireshark, VNC and Java)

Navigate to the command window and run these two commands:

```
sudo apt update
sudo apt upgrade
```

Then install Wireshark, which is needed to see the packets going in and out of the Ethernet port. Wireshark is downloaded by running:

```
sudo apt install wireshark
```

Press ”Yes” to both prompts. Then, to be able to see the Ethernet port traffic, write this in the command window:

```
sudo usermod -a -G wireshark PI-NAME
```

Replace PI-NAME with the name of the Raspberry Pi. After this is done, reboot the machine. Keep in mind that without ”eth0” open in Wireshark, the libiec61850 implementation does not work.

VNC Viewer is software that can be used to control the Raspberry Pi from another PC. This means that the Raspberry Pi does not need to be connected to a keyboard, mouse, or monitor. A great guide is given in https://www.youtube.com/watch?v=08ZwV9xofWw&list=PLySgMiWoycp08Jvd5pnmlz-fNoSzbqwFx&index=3.

For the IEC61850 implementation to be able to read ICD files, we need Java, which is installed through the following command:

```
sudo apt install openjdk-11-jre
```

B.6.4 Installing libiec61850

Libiec61850 is an open-source library for IEC61850 protocols. In this project, it is used to capture IEC61850 SV and to transmit IEC61850 GOOSE. A simple way to download it is to navigate to https://github.com/mz-automation/libiec61850, then under the ”code” button, download the ZIP file on the Raspberry Pi and extract its content where you want to. Then, in the command window, navigate to where it is installed, for example:

```
cd /home/PI-NAME/libiec61850-1.5
```

Run the two commands:

```
make
make examples
```

Now the whole library is compiled. When doing modifications to the existing examples, you need to enter ”make examples” to compile the changes. Furthermore, when creating new programs using libiec61850, the Makefile has to be modified to reflect this.

To run a .c program, navigate to the folder of the program, for example:

```
cd /home/karlv1/libiec61850-1.5/examples/server_example_goose/
```

Then run the sudo command in combination with the program name:

```
sudo ./server_example_goose
```

B.6.5 Modifying ICD Files

For the Raspberry Pi to receive IEC61850-SV, the ICD file used to transmit SV in the OPAL-RT does not need to be shared with the Raspberry Pi, but then the user is in charge of interpreting the packets. However, to transmit GOOSE messages, both the Raspberry Pi and OPAL-RT need to share the same ICD file.

After the ICD file is created, we need to make libiec61850 capable of understanding it. In libiec61850, one way to do this is by compiling the ICD file into a .c and .h file. To do this, place the .icd file in the $libiec61850 - 1.5/tools/model\_generator$ folder. Using the .icd filename, run the following command in the model_generator folder (replace icdFileName with the actual name):

```
java -jar genmodel.jar icdFileName.icd
```

This will generate a .c and .h file in the model_generator folder, which is advised to be moved to the folder where you have your program. In the .c program where you are implementing the communication, use ”#include static_model.h” to include the file.

B.7 Grid

This is a copy of the grid figure so that the reader can quickly look it up.

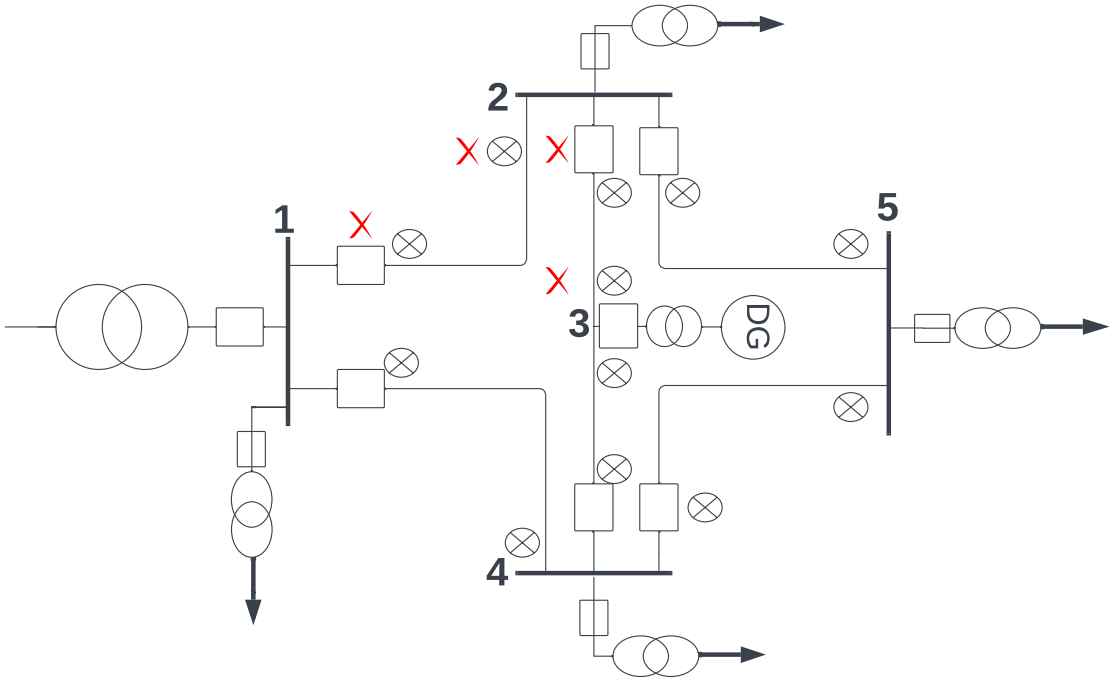
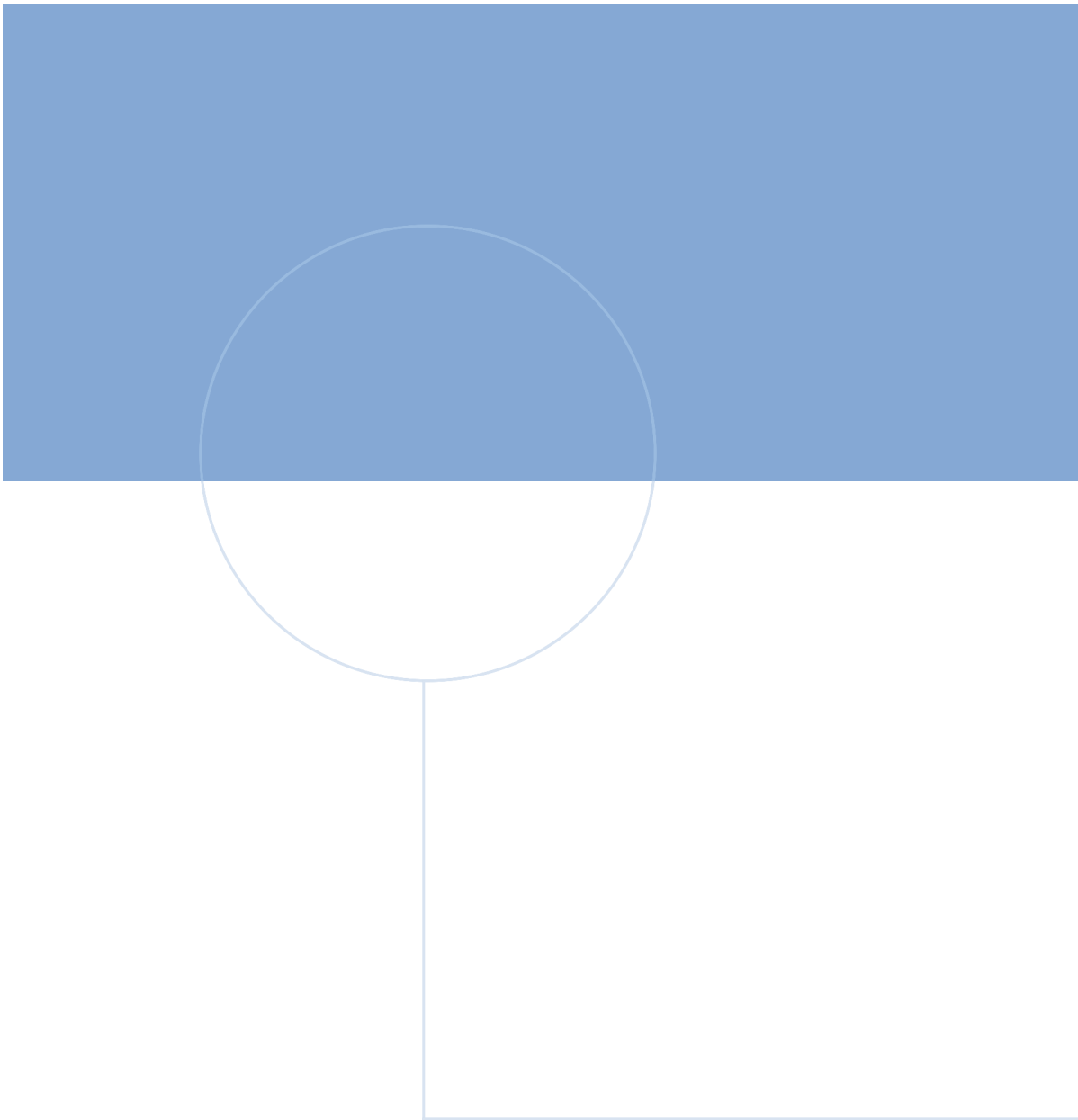


Figure B.9: 22 kV DN implemented in Simulink



NTNU
Norwegian University of
Science and Technology

SINTEF