Graduate thesis

NTNU
Norwegian University of Science and Technology
Faculty of Information Technology and Electrical Engineering
Department of Electronic Systems

Mathias Olsen

Design of a 2.4 GHz, 30 dBm Power Amplifier Utilizing Drain Modulation for Enhanced Efficiency

Graduate thesis in Electronics Systems Design and Innovation
Supervisor: Associate Professor Morten Olavsbråten
Co-supervisor: Associate Professor Carsten Wulff
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Abstract

This thesis presents a study on the design and performance analysis of power amplifiers (PAs) utilizing envelope tracking (ET), or drain modulation, techniques to enhance their efficiency. The focus of this research is centered on two separate 2.4 GHz PAs, each capable of delivering a 30 dBm peak output power, as well as the design of a dual-band PA intended to operate at both 2.4 GHz and 5.2 GHz, delivering a 30 dBm output power as well. In addition to this, a fourth, previously designed PA, is produced and measured. The specifications of these amplifiers are based on performance demands from the nrF7002 WiFi companion integrated circuit (IC).

The very first part of the study investigates the performance of the chosen transistor to be used, through measurements of both the transistor by itself and as part of the previously designed PA. After this, the focus shifts to the design of a single-band PA operating in class A at a down-shifted frequency of 2.3 GHz, optimized for a 300 mA drain current. Through the design process, the amplifier achieves a maximum output power above 30 dBm, gain as high as 12.37 dB with static drain voltage, and with drain modulation employed an average power added efficiency (PAE) of up to 19.90 % while maintaining high linearity.

The second single-band PA operates at the same frequency but sits in class AB with a 65 mA drain current, even though initially designed for a 50 mA. This design iteration shows a maximum output power just above 30 dBm, gain as high as 11.46 dB with static drain voltage, and with drain modulation employed an average PAE of up to 41.87 % while maintaining similar linearity to the 300 mA version.

In an effort to improve system flexibility, better suiting the demands of the nRF7002, the thesis explores the design of a dual-band PA capable of amplifying both 2.4 GHz and 5.2 GHz signals. The amplifier achieves an output power of approx. 30 dBm at the again down-shifted frequency of 2.3 GHz. At this frequency, the highest gain achieved is 12.17 dB with static drain voltage, and with drain modulation employed, an average PAE of up to 10.95 % while maintaining relatively high linearity.

For the higher frequency of the dual-band device, down-shifted from 5.2 to 5.15 GHz, the discrepancy between simulated and measured values is significant and the gain is practically limited, reaching a maximum value of just above 1 dB, not making it relevant to look further into efficiency metrics. However, a maximum output power of not too far below 30 dBm is reached.

A 16QAM is used for the measurements providing the performance metrics, while a test with 64QAM as well is performed with the lower frequency of the dual-band PA.

Abbreviations

Abbreviation	Definition
AC	Alternating current
ACPR	Adjacent channel power ratio
AM	Amplitude modulation
ADS	Advanced Design System
DC	Direct current
ET	Envelope tracking
EVM	Error vector magnitude
FOM	Figure-of-merit
HFET	Heterojunction field-effect transistor
IC	Integrated circuit
ISI	Intersymbol interference
OFDM	Orthogonal frequency-division multiplexing
OFDMA	Orthogonal frequency-division multiple access
PA	Power amplifier
PAE	Power-added efficiency
Peak-to-average power ratio	PAPR
PEP	Peak-envelope power
PET	Power envelope tracking
PM	Phase modulation
PSK	Phase shift keying
QAM	Quadrature amplitude modulation
QPSK	Quadrature phase shift keying
RF	Radio frequency
SMA	SubMiniature version A
STDR	Signal to total distortion ratio
SWR	Standing wave ratio
TEM	Transversal electromagnetic
U-NII	Unlicensed National Information Infrastructure
WTG	Wavelengths toward generator

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1 Introduction

Within wireless communication systems, different demands, among them reduced power consumption and increased efficiency, encourage advancements in radio frequency (RF) PA design. PAs play a critical role in amplifying and transmitting signals with sufficient power levels to enable efficient and reliable wireless communication, [1]. However, battery life in mobile devices and Internet of Things (IoT) applications is a continuously ongoing challenge within the field, [2].

To address this challenge, different variants of ET have emerged as promising solutions to enhance the efficiency of PAs, [3]. ET is a power management technique that adjusts the supply voltage of the PA in real time based on the amplitude variations of the input signal. By dynamically optimizing the supply voltage, ET enables the PA to operate close to its peak efficiency, even when handling signals with high peak-to-average power ratios (PAPRs), [4, p. 511-512].

1.1 Objective of the Work

This master's thesis focuses on the design, implementation, and optimization of a 2.4 GHz PA with a target peak output power of 30 dBm, as well as a 2.4 and 5.2 GHz dual-band PA with the same target output power, specifically tailored for amplifying signals from the Nordic Semiconductor nRF7002 Wi-Fi companion IoT chip. The nRF7002 is a state-of-the-art wireless chip that enables seamless integration of Wi-Fi functionality into various IoT devices, providing connectivity and communication capabilities in the ever-expanding IoT ecosystem, [5].

The primary objectives of this thesis are to create a well-functioning PA, and investigate and demonstrate the feasibility of utilizing ET techniques to enhance the PA's efficiency, thus reducing the power consumption. Through a systematic design approach, various parameters such as linearity, PAE, and gain will be optimized to achieve the desired performance metrics.

To accomplish this goal, a thorough understanding of the underlying theoretical foundations and practical considerations related to PA design and ET is essential. The thesis will cover topics including RF circuit design, device modeling, ET techniques, and impedance matching. In addition, simulation tools and measurements will be employed to optimize and validate the proposed design and evaluate its performance in real-world-like scenarios.

Ultimately, the contributions of this research will provide valuable insights into the application of ET in IoT devices, paving the way for more efficient and sustainable wireless communication systems.

1.2 Structure of the Thesis

The content of this thesis includes the following sections. In Section 2, a solid foundation is laid by providing background information essential for undertaking the work presented in this study. This includes an overview of diverse amplifier classes, the underlying theoretical concepts of amplifier networks, and the sequential steps involved in their creation. Furthermore, this section covers the measures employed to characterize amplifiers, techniques for enhancing their efficiency, and an overview of signals to be amplified.

Section 3 clarifies the methodological approach employed in this thesis, outlining the systematic steps undertaken to fulfill the study's objectives. Specifically, it shows the design approach adopted for the amplifier devices, accompanied by a thorough description of the measurement techniques

employed to evaluate their performance.

Building upon the methodological foundation, Section 4 showcases the achieved outcomes resulting from the application of the aforementioned steps. This section moves into the exploration and analysis of various parameters that characterize different parts of amplifier performance, providing valuable insights into the effectiveness of the design.

In Section 5, in-depth analysis and interpretation of the obtained performance results follow, shedding light on the implications and significance of the findings. This analysis serves as a gateway to Section 6, where potential avenues for further development and exploration are proposed.

Ultimately, Section 7 serves as the culminating segment of this thesis, synthesizing the key findings. It also offers guidance on potential areas for future investigation.

2 Theoretical Background

When following a design process it is always convenient to have a theoretical understanding of the different steps performed and why certain goals are set to be achieved. The background section explores the theoretical foundation of technical tools, devices, and transmission methods/techniques used for this thesis.

First, we look at relevant PAs, of differing classes. Then the useful Smith chart is briefly explained. The chart is highly convenient for designing PA networks based on transmission line theory, discussed after it. Outlining the scattering parameters and the following power amplifier metrics is essential for knowing what characteristics to look for in a PA. Efficiency enhancement techniques via two architectures are explained, and one of them will later be used later in the thesis. Lastly, QAM and orthogonal frequency-division multiplexing (OFDM) are dealt with to give some insight into how the nRF7002 transmits its signals.

2.1 Power Amplifiers

A PA is a device used to amplify an AC input signal in order for the signal to have sufficient energy to be used in a desired way, e.g., an RF signal to be transmitted wirelessly through an antenna, an audio signal to be converted through a loud speaker, etc. There are several different ways of designing a PA. One much-used basic design is the common source layout found in Figure 2.1.1, [6, p. 751-752].

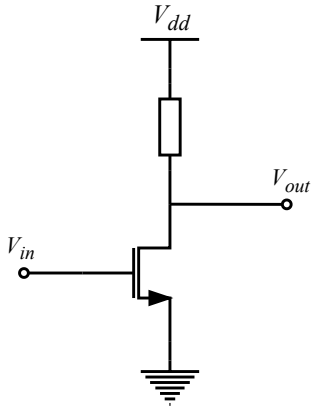


Figure 2.1.1: Common source amplifier, [6, p. 752].

The common source amplifier in Figure 2.1.1 creates a signal amplification due to the voltage drop over the resistor increasing when the current through the transistor increases. In a circuit where efficiency is a priority, we want to avoid using resistors because they introduce additional losses. Thus, the resistor will in practice be presented by the bias network, sometimes also referred to as an RF choke (RFC), connected to the drain of the transistor, as there will be losses here when the transistor is conducting. The transistor source will be coupled directly to ground, [4, p. 94-95].

2.1.1 Power Amplifier Classes

Class A The Class A amplifier is characterized by a conduction angle of 360°, which implies that the amplifying transistor conducts during the entire duration of the input signal to be amplified, as exemplified in Figure 2.1.2, [7, p. 24].

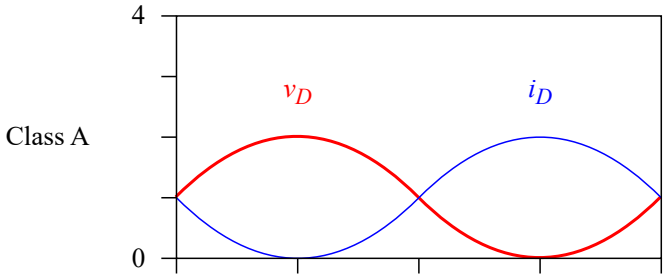


Figure 2.1.2: The class A amplifier is designed such that the gate of the transistor is biased in a manner to maintain a linear operating region, and the drain current remains inversely proportional to the drain voltage throughout the entire signal period, [7, p. 24].

This amplifier design provides certain advantages such as high gain and linearity, but suffers from low efficiency. At the point of Peak Envelope Power (PEP), where the output signal power reaches its maximum, the efficiency of the Class A amplifier attains its theoretical limit of 50 %, [7, p. 24].

Class B The class B amplifier has a conduction angle of 180°. Thus, the amplifier will amplify only half the period of the input signal, while in the other half-period the output signal is zero. This is illustrated in Figure 2.1.3, [7, p. 24].

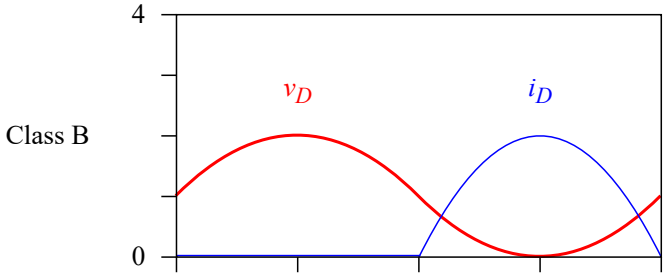


Figure 2.1.3: In a class B amplifier the transistor gate is biased at the conduction threshold, which makes the drain current inversely-proportional to the drain voltage during one half of the signal period, [7, p. 24].

As illustrated in Figure 2.1.3, the linearity of the class B amplifier is good for the half-period where the transistor is conducting and when using two class B amplifiers in a push-pull configuration[1] to be able to amplify both half-periods. In the crossing between the two half-periods the linearity

[1] In a class B push-pull configuration two PAs have their outputs coupled together and their respective inputs set 180° out of phase from each other, in order to create a combined output signal where the entire period of the input signal is amplified, [8].

will usually be degraded. Efficiency-wise the class B PA has a theoretical maximum efficiency of $\frac{\pi}{4}$ ($\approx 78.5\%$) at PEP, which is significantly higher than that of the class A amplifier, [7, p. 24].

Class C The class C amplifier has a conduction angle of less than 180°. So in this case, less than half of the signal period will be amplified and found at the output. The illustration of this is found in Figure 2.1.4, [7, p. 24].

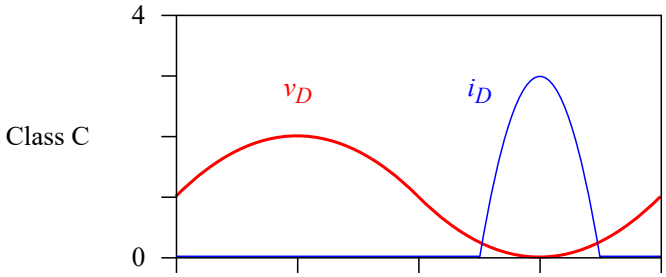


Figure 2.1.4: In a class C amplifier the transistor gate is biased at a voltage below the conduction threshold. This makes the transistor conduct during less than half the period of the signal present at the input, [7, p. 24].

The linearity of the class C amplifier is poorer than the linearities of both the class A and B amplifiers. The efficiency is though better and theoretically it could increase towards 100 % at PEP but this would imply a conduction angle closing in on 0°, which again would demand an output power that is moving towards zero and a drive power moving towards infinite, [7, p. 24-26].

2.2 The Smith Chart

The Smith chart is a graphical tool helping to give designers an intuitive understanding of transmission lines and impedance-matching, [9, p. 63]. It was developed by Phillip Hagar Smith at Bell Telephone Laboratories in 1939, [10]. What the chart represents is a plot of the voltage reflection coefficient, Γ,

$$\Gamma = \frac{V_0^-}{V_0^+} = \frac{Z_L - Z_0}{Z_L + Z_0}, \tag{2.2.1}$$

[9, p. 57], in polar coordinates,

$$\Gamma = |\Gamma| e^{j\theta}, \tag{2.2.2}$$

[9, p. 63]. Thus, the plot's radius from the center of the chart represents $|\Gamma|$ ($|\Gamma| \leq 1$), and when measuring the angle counter-clockwise from the horizontal diameter's right-hand side, θ (-180°$\leq \theta \leq$ 180°) is found, [9, p. 63-64].

The impedance values in the Smith chart, z, are normalized to the characteristic impedance of the transmission line that is used, Z_0, giving

$$z = \frac{Z}{Z_0}, \tag{2.2.3}$$

for an impedance Z, [9, p. 64].

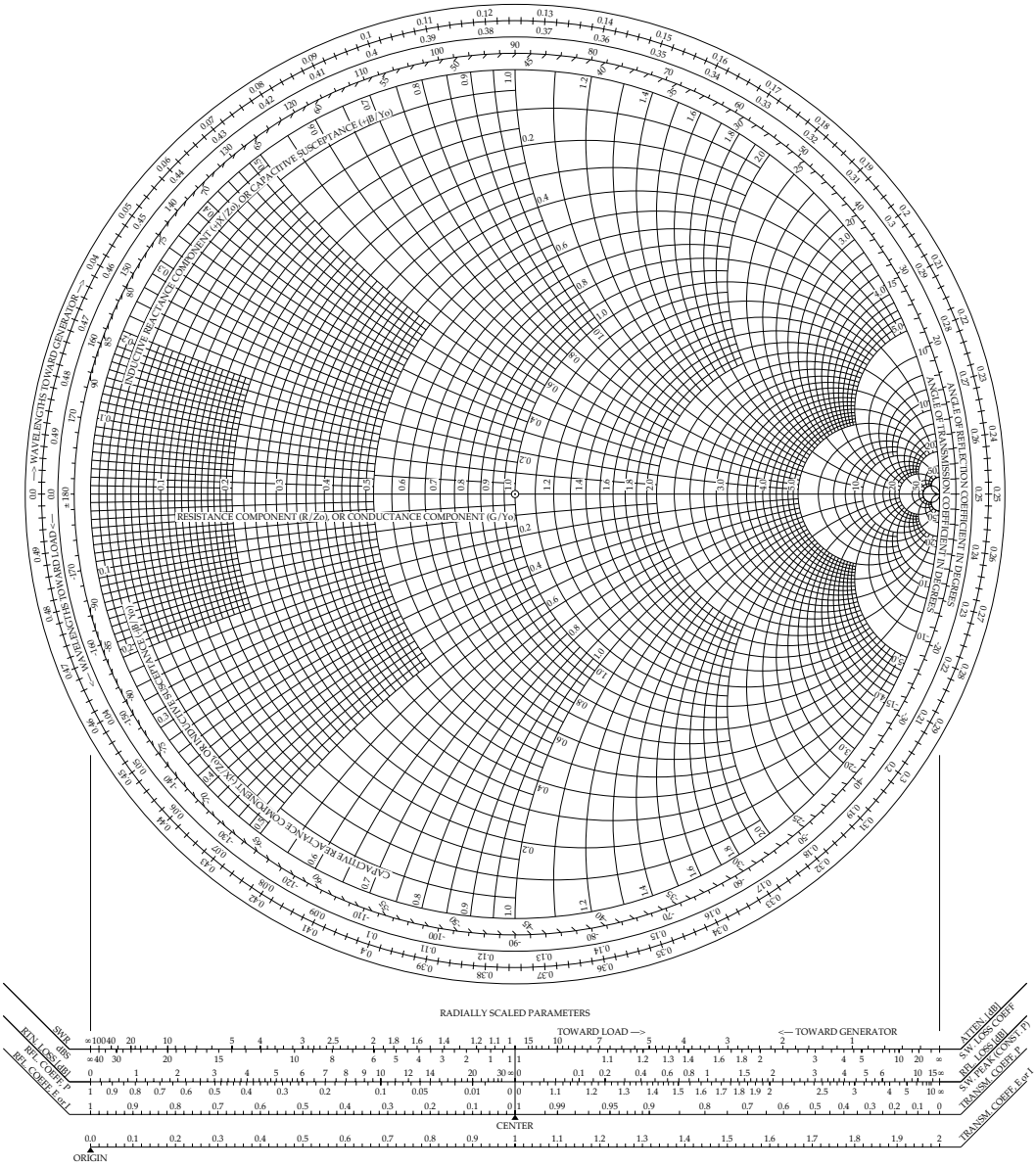


Figure 2.2.1: The Smith chart, provided by IEEE Microwave Theory and Technology Society, [11].

2.3 Power Amplifier Networks

When entering higher frequency spectres, conductors, assumed to behave as short circuits at DC or lower frequencies, will start to introduce losses due to resistive, inductive and capacitive components. Thus, there will be a move from regular circuit theory to transmission line theory and a need to include the, once just conductors, now transmission lines, together with the lumped components, in the analysis of the circuit, [9, p. 48].

2.3.1 Transmission Lines

The transmission line is a network where the parameters are distributed over it and as a consequence, currents and voltages may vary over its length, both in phase and magnitude. When looking at a transmission line model there are two wires. This is a result of there always being two conductors when looking at the propagation of transversal electromagnetic (TEM) waves, [9, p. 48].

Figure 2.3.1 shows a model of a transmission line with the distributed parameters approximated as lumped elements.

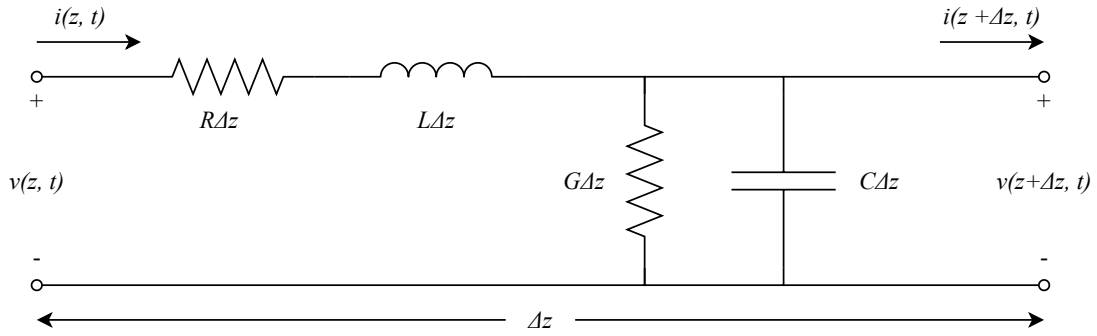


Figure 2.3.1: The transmission line circuit model using lumped elements, [9, p. 49].

The different quantities in the model are as defined by Pozar:

- The series resistance for both conductors, per unit length, R, [Ω/m].
- The series inductance for both conductors, per unit length, L, [H/m].
- The shunt conductance, per unit length, G, [S/m].
- The shunt capacitance, per unit length, C, [F/m].

Hence, there will be losses when including lengths of transmission line in a network [9, p. 48-49].

It is however sometimes useful to look at special cases with lossless, terminated transmission lines to understand some both important and convenient concepts. Figure 2.3.2 shows a transmission line which terminates in a short-circuit, [9, p. 59].

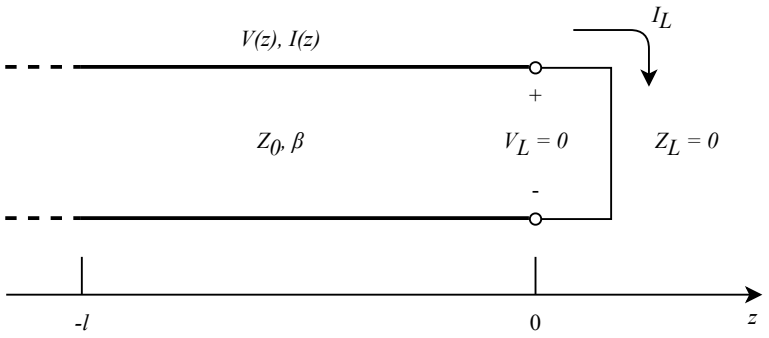


Figure 2.3.2: A short-circuit terminated transmission line, [9, p. 59].

In Figure 2.3.2 most of the variables are already known. The exception is β, the propagation constant in a lossless media, given by

$$\beta = \omega\sqrt{LC}, \tag{2.3.1}$$

[9, p. 56].

Using (2.2.1) on the circuit in Figure 2.3.2 gives a reflection coefficient, $\Gamma = -1$. This indicates a standing wave ratio (SWR),

$$\text{SWR} = \frac{V_{max}}{V_{min}} = \frac{1 + |\Gamma|}{1 - |\Gamma|}, \tag{2.3.2}$$

towards infinity, [9, p. 58-59].

For an open circuit termination, $Z_L = \infty$, (2.2.1) shows that the reflection coefficient would be $\Gamma = 1$ and thus, from (2.3.2), result in a SWR moving towards infinity again, [9, p. 60].

Another useful expression for Z_{in} is

$$Z_{in} = Z_0 \frac{Z_L + jZ_0 \tan \beta l}{Z_0 + jZ_L \tan \beta l}, \tag{2.3.3}$$

which for $Z_L = 0$ reduces to

$$Z_{in} = jZ_0 \tan \beta l, \tag{2.3.4}$$

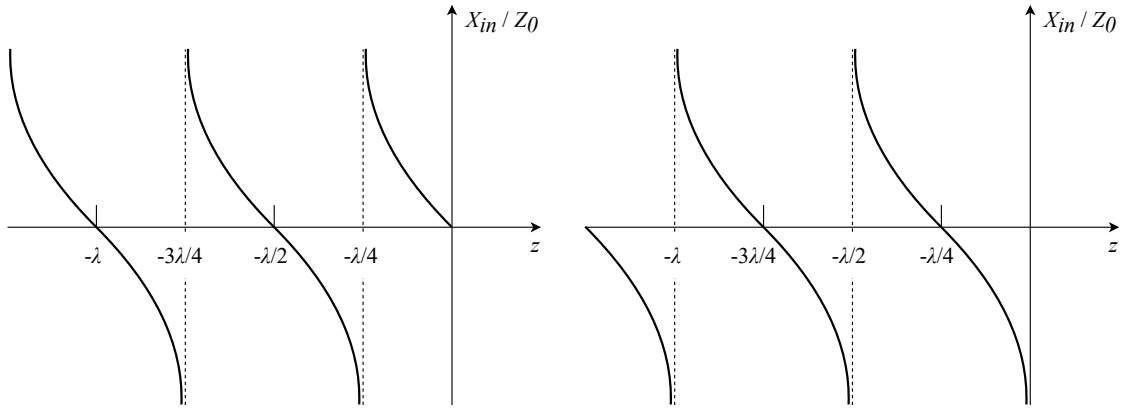
[9, p. 59].

And for $Z_L = \infty$ reduces to

$$Z_{in} = -jZ_0 \cot \beta l, \tag{2.3.5}$$

[9, p. 61].

The input impedances in both (2.3.4) and (2.3.5) are purely imaginary for all lengths l. These observations lead to some interesting phenomenons, as shown in Figure 2.3.3, [9, p. 59-61].



(a) Development of the impedance along a transmission line terminated in a short circuit, [9, p. 60].

(b) Development of the impedance along a transmission line terminated in an open end, [9, p. 61].

Figure 2.3.3: Development of the impedance along transmission lines with different terminations.

In Figure 2.3.3a the impedance, Z_{in}, at the connection point of the transmission line, $z = 0$, is 0, and this is repeated every $\frac{\lambda}{2}$ we move down the line in z-direction. Figure 2.3.3b has an infinite impedance at $z = 0$. This is also repeated every $\frac{\lambda}{2}$ when moving down the line. As a result it is possible to say that adding n transmission lines, each with an exact length $l = \frac{\lambda}{2}$, will not change the impedance of the load. So from this observation combined with (2.3.3) we have

$$Z_{in} = Z_L, \tag{2.3.6}$$

when $l = n\frac{\lambda}{2}$, and $n = 1, 2, 3...$, [9, p. 61].

On the other hand, when moving $\frac{\lambda}{4}$ down the transmission line, the impedance changes from 0 to infinite in Figure 2.3.3a and from infinite to 0 in Figure 2.3.3b. As a matter of fact, when looking at any point on the negative x-axis in both Figure 2.3.3a and 2.3.3b, it is shown that moving $\frac{\lambda}{4}$ will invert the impedance seen at that point. Thus, from (2.3.3) the input impedance can be expressed as

$$Z_{in} = \frac{Z_0^2}{Z_L}, \tag{2.3.7}$$

when $l = \frac{\lambda}{4} + n\frac{\lambda}{2}$, and $n = 1, 2, 3....$ This behavior is a very useful attribute and leads to the transmission line with $l = \frac{\lambda}{4}$ being called a *quarter-wave transformer*, [9, p. 61].

2.3.2 Bias Network

The purpose of incorporating a bias network in RF amplifier design is to maintain a stable bias voltage in the presence of an input signal, and subsequently an output signal. This objective is achieved by constructing a network that offers high impedance between the biasing point and the voltage source within the frequency spectrum under consideration, [9].

2.3.3 Matching Networks

To obtain an optimal power transfer from the source to the PA and from the PA to the load, it is of great importance to create a good impedance match between the source and the PA input, and between the PA output and the load. In the case of the two connecting parts not being matched, the solution is to create some sort of matching network between the two, as demonstrated in Figure 2.3.4, [9, p. 228].

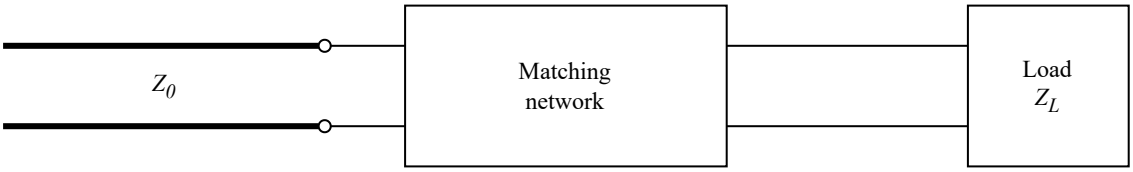


Figure 2.3.4: A matching network matching a load, Z_L, to a transmission line, Z_0, [9, p. 229].

When imagining the matching network in Figure 2.3.4 is just a short between Z_0 and Z_L, the transmission line equation tells what the input impedance, looking into Z_L from Z_0 will be:

$$Z_{in} = Z_0 \frac{Z_L + jZ_0 \tan \beta l}{Z_0 + jZ_L \tan \beta l}, \tag{2.3.8}$$

[9, p. 59]. In other words, if $Z_L = Z_0$ it is also the case that $Z_{in} = Z_0$. If this isn't the case, the mission of the matching network is to transform the impedance seen, when looking from Z_0 towards Z_L, in such a way that it is matched to Z_0, [9, p. 228].

The creation of a matching network can be done in different ways. Examples are using lumped elements, being resistors, capacitors and inductors, using transmission line stubs, or using quarter-wave transformers, [9, p. 229-249]. Figure 2.3.5 shows a practical principle of a matching network using a transmission line stub.

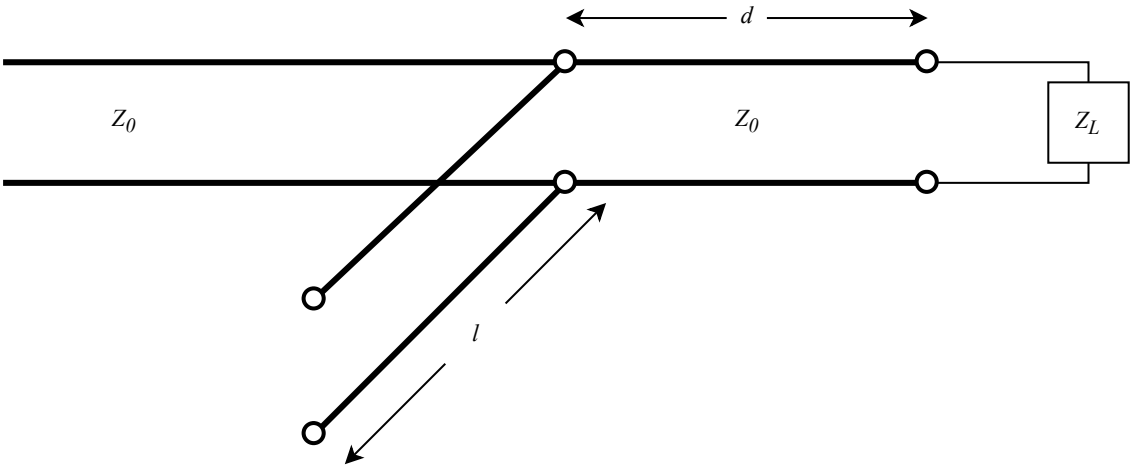


Figure 2.3.5: Open-ended single-stub shunt tuning circuit, [9, p. 235].

The objective is to match the load impedance Z_L to the transmission line Z_0 by adjusting the distance between the connection point of the stub and the load, d, and the length of the stub, l. When knowing the impedances, the following steps are taken to find d and l:

- Z_L is normalized in regard to Z_0 and we get the normalized load impedance z_L, [9, p. 64, 235].
- Then the SWR circle in the Smith chart is created by having the circle's center in the middle of the chart, in the point where the normalized impedance is purely resistive and equal to 1, and letting z_L be a point at the edge of the circle, [9, p. 64, 235–236].
- Convert the normalized load impedance, z_L, to the normalized load admittance, y_L, by moving 180°around the circle, [9, p. 235-236].
- Let the the Smith chart be considered an admittance chart instead of an impedance chart, [9, p. 236].
- Identify the two points where there is an intersection between the SWR circle and the $1 + jB$ circle (the circle where real part of the normalized admittance is 1 and the imaginary part varies). These points are marked as y_1 and y_2 in the graphical presentation of the process in the Smith chart in Figure 2.3.6, [9, p. 236].
- The two different solutions for distance d, in number of wavelengths, are found by drawing lines from from the center of the chart, through the points y_1, y_2, and y_L, to the very edge of the chart and reading the wavelengths toward generator (WTG) scale. This gives three numbers, where the number belonging to y_L is subtracted from each of the numbers belonging to y_1 and y_2. The two resulting differences give the two possible solutions to d, d_1 and d_2, expressed in wavelengths, [9, p. 236].
- The stub length, l, is decided by the susceptance (imaginary part of the admittance) in points y_1 and y_2. By following the pertaining susceptance line to the edge of the Smith chart, the points giving the length are found. These points are marked as l_1 and l_2 in Figure 2.3.6, [9, p. 236-237].
- The values of the points, if using a short-circuited stub, are then found by starting at $y = \infty$ (as the Smith chart now is used as an admittance chart), moving clockwise, and counting the number of wavelengths from the short-circuit to the points l_1 and l_2, [9, p. 237].
- In Pozar's example this results in $l_1 = 0.095\lambda$ and $l_1 = 0.405\lambda$, as we are creating the complex conjugates of the normalized admittances, [9, p. 237].

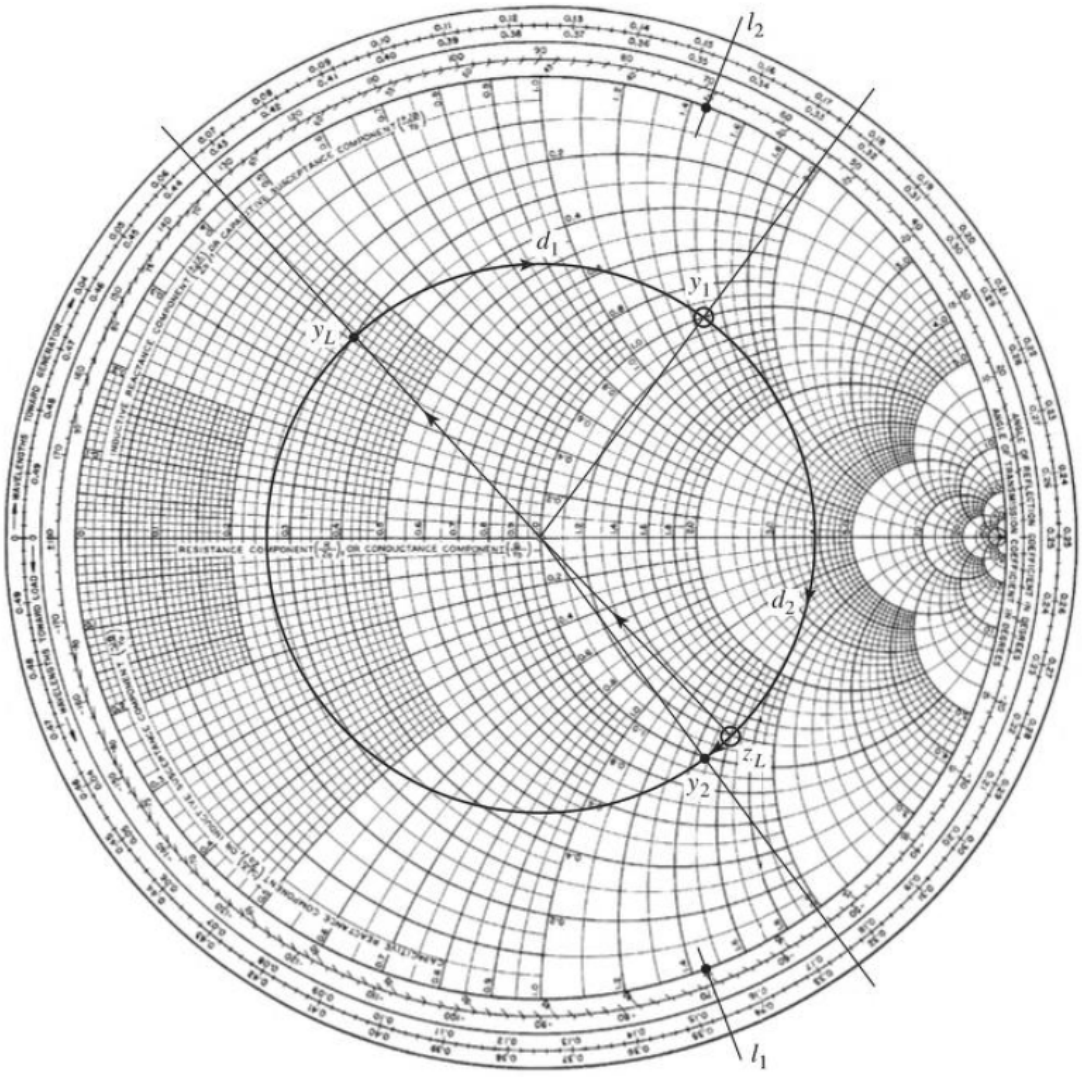


Figure 2.3.6: Smith chart containing Pozar's graphical explanation of finding d and l in the single-stub shunt matching network, [9, p. 236].

2.4 Scattering Parameters

Scattering parameters, or S-parameters for short, are coefficients describing either reflection, when looking into a port in an n-port network, or the transmission between ports in the same network. In many practical cases, e.g., in the case of an amplifier circuit, it will be a two-port network, with one input port and one output port. Such a network will have a 2-by-2 scattering matrix containing its S-parameters,

$$\begin{bmatrix} V_1^- \\ V_2^- \end{bmatrix} = \begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} \begin{bmatrix} V_1^+ \\ V_2^+ \end{bmatrix}, \tag{2.4.1}$$

where V_1^+ and V_2^+ are the amplitudes of the incident voltage waves on ports 1 and 2, respectively, and V_1^- and V_2^- are the amplitudes of the voltage waves reflected from the same ports. Thus, the

scattering matrix with the S-parameters describe the relationship between these voltages. Each parameter is a coefficient for either transmission or reflection. S_{11} is for the reflection when looking into port 1, S_{22} is for the reflection when looking into port 2, S_{21} is for the transmission from port 1 to port 2, and S_{12} is for the transmission from port 2 to port 1, [9, p. 178].

In practice, knowing the S-parameters of the circuit is very helpful when characterising the small-signal gain of the PA. If a condition is met where S_{12} is low enough, i.e., that the reverse transmission of the PA is negligible, S_{11} will represent the input reflection coefficient, Γ_{in}, of the PA and S_{22} will represent the output reflection, Γ_{out}, coefficient of the PA. Thus, S_{11} will be a number telling how well the input is matched to the signal source and S_{22} will be a number telling how well the output is matched to the load. If [9, p. 563].

2.5 Power Amplifier Metrics

2.5.1 Stability

The stability of an amplifier tells if the device is prone to oscillations or not. To find out if the device is stable, input and output reflection coefficients, $|\Gamma_{in}|$ and $|\Gamma_{out}|$, are looked at. A scenario where both values are < 1 indicates that neither the input nor the output impedance has a negative real part. If this is the case for all passive source and load impedances, it is *unconditionally* stable. If this is the case only for a specific range of passive source and load impedances, it is *conditionally* stable (or potentially unstable), [9, p. 564].

Another factor to consider regarding the stability is that the reflection coefficients also change with frequency. This is something to be aware of, as it might be the case that the amplifier is stable at the frequency it is designed to operate at but at the same time unstable within other frequency spectrums, [9, p. 564].

One way to check unconditional stability of an amplifier is to use the K - Δ test, which looks at two different conditions. *Rollet's condition*,

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{21}S_{12}|} > 1, \tag{2.5.1}$$

and an auxiliary condition,

$$|\Delta| = |S_{11}S_{22} - S_{21}S_{12}| < 1. \tag{2.5.2}$$

If both are satisfied, the device is unconditionally stable, [9, p. 567].

In addition to this test, there exists a single parameter, μ, able to tell if a two-port device is unconditionally stable,

$$\mu = \frac{1 - |S_{11}|^2}{|S_{22} - \Delta S_{11}^*| + |S_{21}S_{12}|} > 1, \tag{2.5.3}$$

where it is also the case that greater stability is indicated by a larger μ value, [9, p. 567], [12].

If the device is only conditionally stable, stability circles in the Smith chart can be used to determine which impedances imply stability. For output stability circles, when having $Z_L = Z_0$, $|S_{11}|$ being less than or greater than 1 decides whether stability is found inside or outside the circle. If $|S_{11}| < 1$,

stability is found outside the stability circle but within the Smith chart. If $|S_{11}| > 1$, the stable area is found inside both the stability circle and the Smith chart. In the case where the the circuit is unconditionally stable, the whole stability circle is either placed completely outside the Smith chart or it completely encloses the entire Smith chart, [9, p. 566].

2.5.2 Gain

There exist various definitions for different types of gain in the domain of PAs. Among the most commonly considered types are the three known as *Power Gain*, denoted as G, *Available Power Gain*, denoted as G_A, and *Transducer Power Gain*, denoted as G_T. The similarity among these gain types is contingent upon the degree of matching between the source and load impedances with respect to the amplifier. In the case of a conjugate match between both the source impedance and the amplifier, as well as the load impedance and the amplifier, the relationship among the gains can be expressed as $G = G_A = G_T$, [9, p. 559].

Power Gain, represented by G, is quantified as follows:

$$G = \frac{P_L}{P_{in}}, \tag{2.5.4}$$

where P_L corresponds to the power delivered to the load, and P_{in} denotes the power actually supplied to the input of the power amplifier. The measurement of P_{in} is conducted after the input matching network, hence its value varies depending on the extent of matching achieved between the power amplifier and the source, [9, p. 559].

Available Power Gain, denoted as G_A, is defined as:

$$G_A = \frac{P_{avn}}{P_{avs}}, \tag{2.5.5}$$

where P_{avn} signifies the power available from the power amplifier's output, measured prior to the output matching network. Consequently, P_{avn} remains unaffected by the degree of matching between the power amplifier's output and the load. P_{avs} represents the power available at the output of the signal source, [9, p. 559].

Lastly, Transducer Power Gain, denoted as G_T, is expressed as:

$$G_T = \frac{P_L}{P_{avs}}, \tag{2.5.6}$$

Here, P_L, as in the case of G, denotes the power effectively delivered to the load, whereas P_{avs}, similar to the case of G_A, indicates the power available from the source, [9, p. 559].

The transducer power gain is the gain that will be focused on later, as the power available from the source is what will be amplified and the power delivered to the load is what actually matters in a practical use case. P_{avs} does not change due to the design of the matching networks matching networks, while P_L does depend on both the input and output matching network. Thus, this is the gain telling something about the total matching, and the actual power gain from the source to the output at the load, [9, p. 562].

2.5.3 Linearity

The linearity of a PA plays a role when amplifying modulated signals. There are different effects resulting from non-linearities in a PA. A few of them will be covered briefly here. Which type of effect from non-linearities to focus on depends on the modulation scheme, [6, p. 756].

AM/PM Conversion AM/PM conversion (APC) is a phenomenon where the phase changes as the amplitude changes. Thus, if having a signal which is modulated in amplitude, there may be contamination from the amplitude modulation of the input signal in the phase of the output signal. Analytically, an input signal

$$V_{in}(t) = V_1 \cos \omega_1 t, \tag{2.5.7}$$

[6, p. 33], with amplitude V_1 and frequency ω_1, will in presence of APC result in an output signal

$$V_{out}(t) = V_2 \cos \left[\omega_1 t + \phi(V_1)\right], \tag{2.5.8}$$

with amplitude V_2, the same frequency ω_1, and now also a phase shift dependant on the amplitude, V_1, of the input signal, [6, p. 33].

Gain Compression As the amplitude of the signal input to a PA increases, the gain may change. And in most cases the gain drops. One result of this is that the actual behavior of the amplifier will begin to differ from the model describing the small-signal gain of the device. Therefore, a model describing the large-signal behavior of the PA is necessary to find the point where the compression begins and also for performing reliable simulations when moving into the region where the gain is compressed, [6, p. 16-17].

Regarding the impact on modulated signal, quadrature amplitude modulation (QAM) is an example of a type of modulation modulating the signal's amplitude and thus may be affected negatively by gain compression, [6, p. 756].

To quantify where the linear region of the amplifier ends, the *1-dB compression point*, P_{1dB}, is used. This defines the input power, IP_{1dB}, or output power, OP_{1dB}, where the gain drops 1 dB compared to the ideal operation with linear gain, as shown in Figure 2.5.1, [9, p. 512-513].

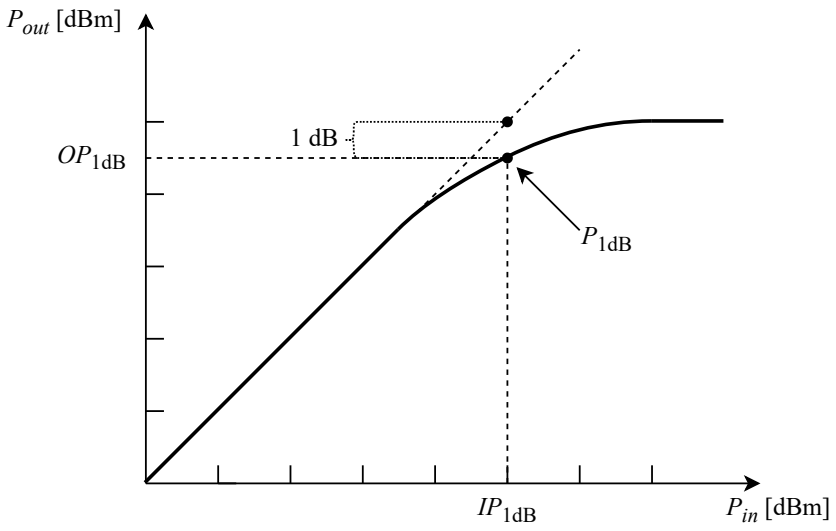


Figure 2.5.1: The 1-dB compression point, $P_{1\text{dB}}$, illustrated together with the corresponding input power, $IP_{1\text{dB}}$, and output power, $OP_{1\text{dB}}$, [9, p. 513].

Spectral Regrowth The phenomenon of spectral regrowth appears when a variable-envelope signal is handled by a system that is non-linear. As a result of spectral regrowth, there may be changes in the adjacent channel power ratio (ACPR). This means that the spectrum of the carrier channel increases and as a result increases the power in the adjacent channels. The result of this is an increased ACPR, which is undesired, [6, p. 118-119].

A way to investigate the ACPR is to perform a two-tone intermodulation test. This is done by applying two unmodulated tones with a power giving each of the two tones an output power 6 dB below the PA's maximum output power level, adding up to the maximum voltage amplitude swing during in-phase output, [6, p. 756-757].

Error Vector Magnitude The error vector magnitude (EVM) is a measure describing the distance between, affected by both amplitude and phase, between a measured and an ideal signal in a constellation diagram representing a signal modulation scheme, e.g., an order of quadrature amplitude modulation (QAM), [13]. The principle is shown in Figure 2.5.2.

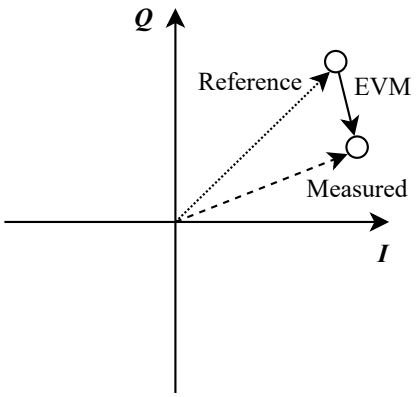


Figure 2.5.2: Error vector magnitude, [13].

Signal to Total Distortion Ratio Signal-to-total distortion ratio (STDR) is a figure-of-merit (FOM) developed to describe the total distortion of a PA, including distortion both "inside and outside of the signal bandwidth", as well as "memoryless non-linear distortion and distortion caused by memory effects," in the presence of such, [14].

2.5.4 Efficiency

The efficiency of a PA can be defined in different ways. One measure is the drain efficiency, η, defined as

$$\eta = \frac{P_{out}}{P_{DC}}, \tag{2.5.9}$$

where P_{out} is the signal output power and P_{DC} is the supply power of the PA. The power added efficiency (PAE) is defined as

$$\text{PAE} = \frac{P_{out} - P_{in}}{P_{DC}} = (1 - \frac{1}{G})\frac{P_{out}}{P_{DC}}, \tag{2.5.10}$$

where again P_{out} is the output power from the PA, P_{in} is the power of the input signal, P_{DC} is the supply power of the PA, and G is the PA's gain. Combining (2.5.9) and (2.5.10) gives

$$\text{PAE} = (1 - \frac{1}{G}) \cdot \eta. \tag{2.5.11}$$

The PAE is the main number, regarding efficiency, we are going to look at later when designing the values of different PA configurations. It is noteworthy that for an equal output power level, P_{out}, a higher gain, G, gives a higher PAE. Thus, it is intuitively desired to have a high gain to achieve a good PAE value. On the other hand, as mentioned in 2.1.1, amplifiers of class A has high gain but at the same time lower efficiency, and subsequently a lower PAE. In short, the focal point of a PA is to amplify an input signal, which requires a certain gain. Then the goal is to do this in a way that is as efficient as possible. Especially when using the PA in an IoT setting, where battery lifetime usually is of great importance, [9, p. 597].

2.6 Efficiency Enhancement Techniques

2.6.1 Doherty PA

The Doherty amplifier is an amplifier architecture used to enhance efficiency, where two PAs are coupled together and biased in a way where one PA amplifies the signal in one power region and the other PA does most of the amplification in the other power region. A principal schematic of how this is done is shown in Figure 2.6.1, [15, p. 290-291].

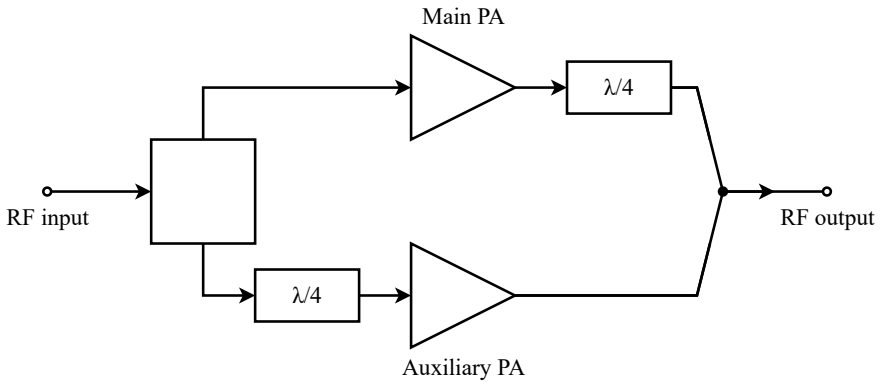


Figure 2.6.1: Doherty PA architecture. The $\frac{\lambda}{4}$-transmission line at the output of the main PA is there to invert the impedance visible to the main PA, present at the RF output. The $\frac{\lambda}{4}$-transmission line at the input of the auxiliary PA is there to compensate for the delay created by the already mentioned $\frac{\lambda}{4}$-transmission line at the output of the main PA, [15, p. 292-293].

By applying the Doherty architecture, the two PAs are able to operate closer to PEP. In other words, the PAs will be operating closer to or in saturation for a greater part of the power region, compared to what would've been the case if they were operating as stand-alone components. By having a look at (2.5.9), this will increase the efficiency, as operation closer to PEP indicates a higher P_{out} compared to the available P_{DC}. Figure 2.6.2 shows the development of both the individual output power from each PA and the combined output power, in relation to input power, [15, p. 291-292].

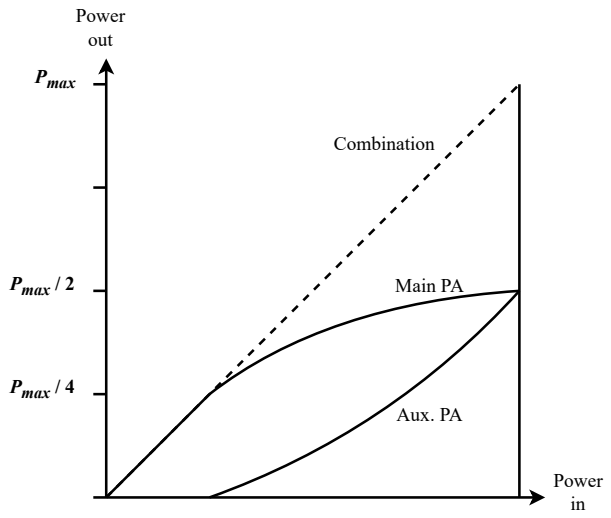


Figure 2.6.2: Output powers in a Doherty amplifier. Each PA has an individual PEP of $P_{max}/2$ (3 dB backoff from P_{max}) and in combination they reach P_{max}, [15, p. 292].

Up until the point where the development of the output power from the main PA starts becoming non-linear in relation to the input power, the output power from the auxiliary PA is zero. This can be done by biasing the gate input of the auxiliary PA transistor with a voltage further away from the threshold than the input of the main PA. When the input power reaches the level where the output power of the main PA is around $P_{max}/4$ (6 dB backoff from P_{max}), the auxiliary PA starts conducting and amplifying. Then both PAs increase their output power as the input power increases up until maximum input power is reached and both the main and the auxiliary PA individually has an output power of $P_{max}/2$, which combined gives a total output power of P_{max}. The maximum efficiency of the Doherty amplifier will be the same as the maximum efficiency of the individual PAs operated as standalone components. Thus, the maximum efficiency won't be increased by using a Doherty architecture but the idea is to be able to operate closer to this maximum efficiency for a greater part of the power spectrum. Figure 2.6.3 illustrates the efficiency of a Doherty amplifier in relation to its output power, [15, p. 291-292].

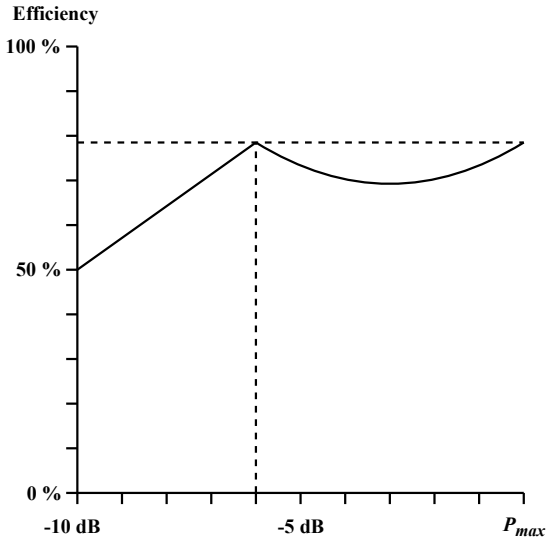


Figure 2.6.3: The efficiency of a Doherty amplifier in relation to the input power, when assuming both PAs operate as ideal class B PAs, [15, p. 298].

Maximum efficiency ($\frac{\pi}{4} \approx 78.5\,\%$) is reached already at 6 dB backoff ($P_{max}/4$), when the main PA is reaching saturation. Then the efficiency drops as the auxiliary PA is activated and increases again when the auxiliary PA gets closer to saturation as well. The alternative of just using a single PA operating as an ideal class B would result in an efficiency of about 25 % at 10 dB backoff and then increasing steadily to 78.5 % at P_{max}, [15, p. 298-300].

2.6.2 Envelope Tracking

Envelope Tracking Envelope tracking, or in more general terms also referred to as supply modulation, drain tracking, or drain modulation, is another technique used to increase the efficiency of a PA. While the Doherty architecture implemented a way to have when looking at (2.5.9), P_{out} operating closer to P_{DC} for a larger part of the signal power spectrum, envelope tracking instead introduce a variation to P_{DC}. This makes it possible to lower P_{DC} when P_{out} decreases, by keeping the DC supply voltage closer to the peak voltage, or envelope, of the AC signal. Thus, making it especially interesting for situations with high PAPRs. The principle is illustrated in Figure 2.6.4 and should lead to increased efficiency, [4, p. 511-512].

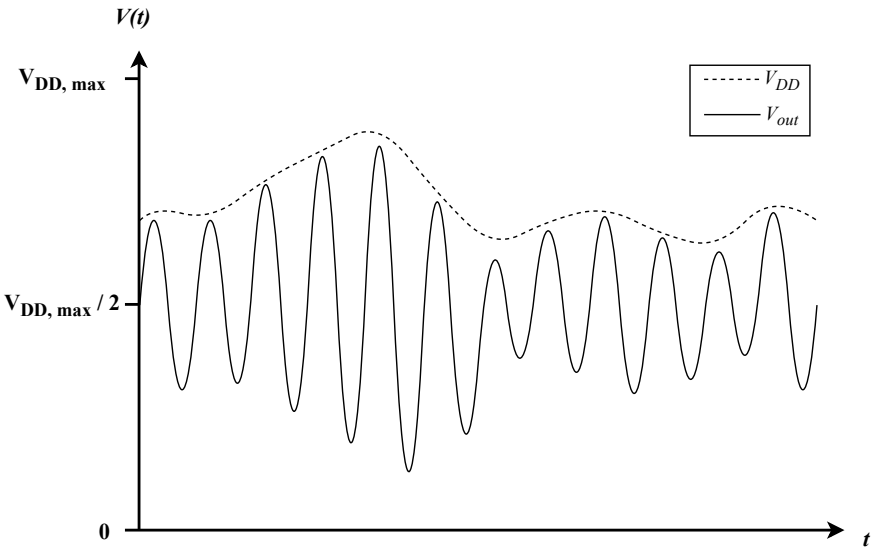


Figure 2.6.4: The DC supply voltage, V_{DD}, depicted by the dotted line, tracks the envelope of the AC signal voltage, V_{out}, illustrated by the solid line, [3].

The implementation of an envelope tracking amplifier is done by using two PAs, where one, the RF PA, is used to amplify the RF signal, and the other one, the envelope PA, is used to provide the supply voltage to the RF PA. This is done by using an envelope detector to detect the envelope of the input signal and feeding this as an input to the envelope PA. The envelope is then amplified and provided as supply voltage. A principle schematic is found in Figure 2.6.5, [4, p. 511].

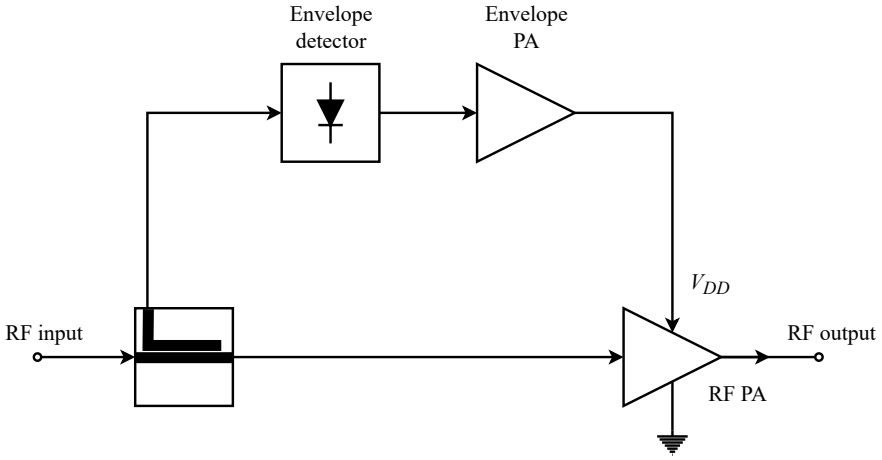


Figure 2.6.5: An envelope tracking PA, where the RF input is amplified by the RF PA and the supply voltage, V_{DD}, is modulated and provided by the envelope PA, fed by an envelope detector, [4, p. 511].

Power Envelope Tracking Performing drain modulation requires a certain bandwidth. Theoretically, this will be infinite, given the following:

$$v_s(t) = v_I(t) + j \cdot v_Q(t) \rightarrow \underline{W = \frac{B_{RF}}{2}}, \tag{2.6.1}$$

$v_s(t)$ being the complex baseband signal with a real part $v_I(t)$, and an imaginary part $v_Q(t)$. B_{RF} is the bandwidth of the transmitted RF signal and W the bandwidth of its baseband signal. The bandwidth of the drain modulation, or tracking, signal, proportional to the signal's envelope will then be

$$v_{d,env}(t) \propto v_{s,env}(t) = |v_s(t)| = \sqrt{v_I^2(t) + v_Q^2(t)} \rightarrow \underline{W = \infty}. \tag{2.6.2}$$

Using the power of the baseband signal, rather than the voltage envelope, what is known as power envelope tracking (PET), reduces the bandwidth of the tracking signal as following

$$p_{env}(t) = v_s(t) \cdot v_s^*(t) = v_{s,env}^2(t) \rightarrow \underline{W = B_{RF}}, \tag{2.6.3}$$

providing the modulated drain voltage

$$v_d(t) = a_0 + a_2 \cdot v_{s,env}^2(t) = \underline{a_0 + a_2 \cdot p_{env}(t)}, \tag{2.6.4}$$

where a_0 and a_2 are coefficients. To maintain better efficiency enhancement, closer to the one of the regular drain modulation, it is possible to increase the order of the PET,

$$v_d(t) = \underline{a_0 + a_2 \cdot p_{env}(t) + a_4 \cdot p_{env}^2(t)}. \tag{2.6.5}$$

This doubles the bandwidth of the tracking signal,

$$v_d(t) = a_0 + a_2 \cdot v_{env}^2(t) + a_4 \cdot p_{env}^4(t) \rightarrow \underline{W = 2 \cdot B_{RF}}. \tag{2.6.6}$$

But still keeping the bandwidth much smaller than what would have been the case with regular drain modulation, [3].

2.7 Quadrature Amplitude Modulation

QAM is a modulation method where both the amplitude and phase of the signal are modulated in order to express symbols. This makes it possible to express more symbols without increasing the bandwidth, as compared to only modulating the phase, like in phase shift keying (PSK) or quadrature PSK (QPSK), or only modulating the amplitude, amplitude modulation (AM), [6, p. 114].

The different symbols are represented by dots in a cartesian coordinate system with the signal's in-phase component, I, on the x-axis and quadrature component, Q, on the y-axis. The distance from origo to the dot defines the amplitude of the signal corresponding to the symbol and the angle between the positive side of the x-axis and the dot represents the symbol's corresponding phase. Figure 2.7.1 shows a 16-QAM constellation map, where 16 different Gray[2] encoded values are represented by different amplitudes and phases, [16].

[2]Gray code is a coding type where neighboring values only differ by one bit, [16].

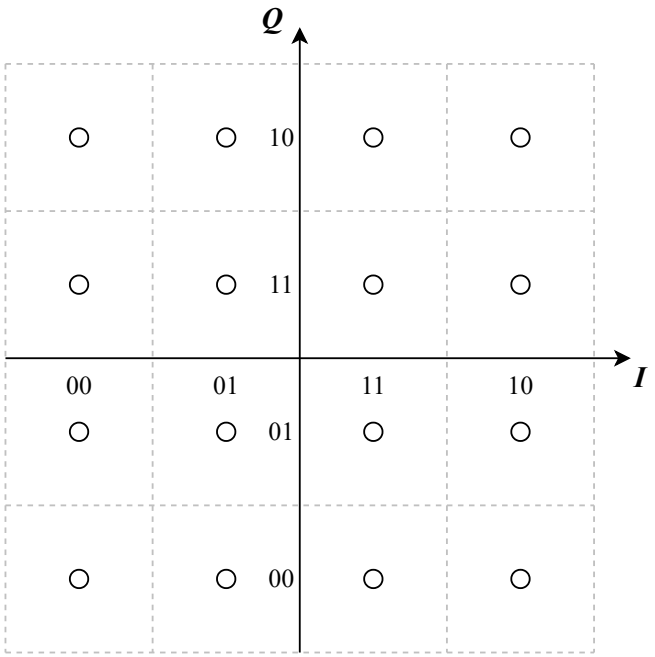


Figure 2.7.1: 16-QAM constellation using Gray encoding, [16].

Among the mentionable technologies, the nRF7002 chip communicates using 64QAM, [5].

2.8 Orthogonal Frequency-Division Multiplexing

OFDM is a method used to avoid information loss due to multipath effects during wireless transmission at higher data rates. When a signal is sent wirelessly it may take several different paths to reach the receiving antenna. E.g., the direct straight route from the transmitter to the receiver, or it may take a path where it reflects off a close-by wall. These paths will have different lengths and because of this there will be a spread in delay between the arrivals of the signals, which may lead to intersymbol interference (ISI), [6, p. 115].

When transmitting high data rates using only one single carrier frequency, a large bandwidth is required and the transmission will be sensitive to ISI caused by multipath effects. OFDM demultiplexes the data to several different data streams that are transmitted on different carrier frequencies. Thus, the total data rate is maintained but the data rate on each single carrier is reduced, leading to lower multipath sensitivity, [6, p. 115-117].

Another type of OFDM is orthogonal frequency-division multiple access (OFDMA), where the bandwidth is divided into separate sub-carriers dedicated to each client. Thus, several users can be connected to the same transceiver and they all are connected to a separate orthogonal frequency sub-carrier, [17]

3 Method

This part will describe the design process used for designing the different PAs and later doing measurements on them to evaluate their performance. The design of a PA requires several steps to ensure the fulfillment of set performance targets such as achieved output power, gain, and efficiency, leading to the working method illustrated by Figure 3.0.1.

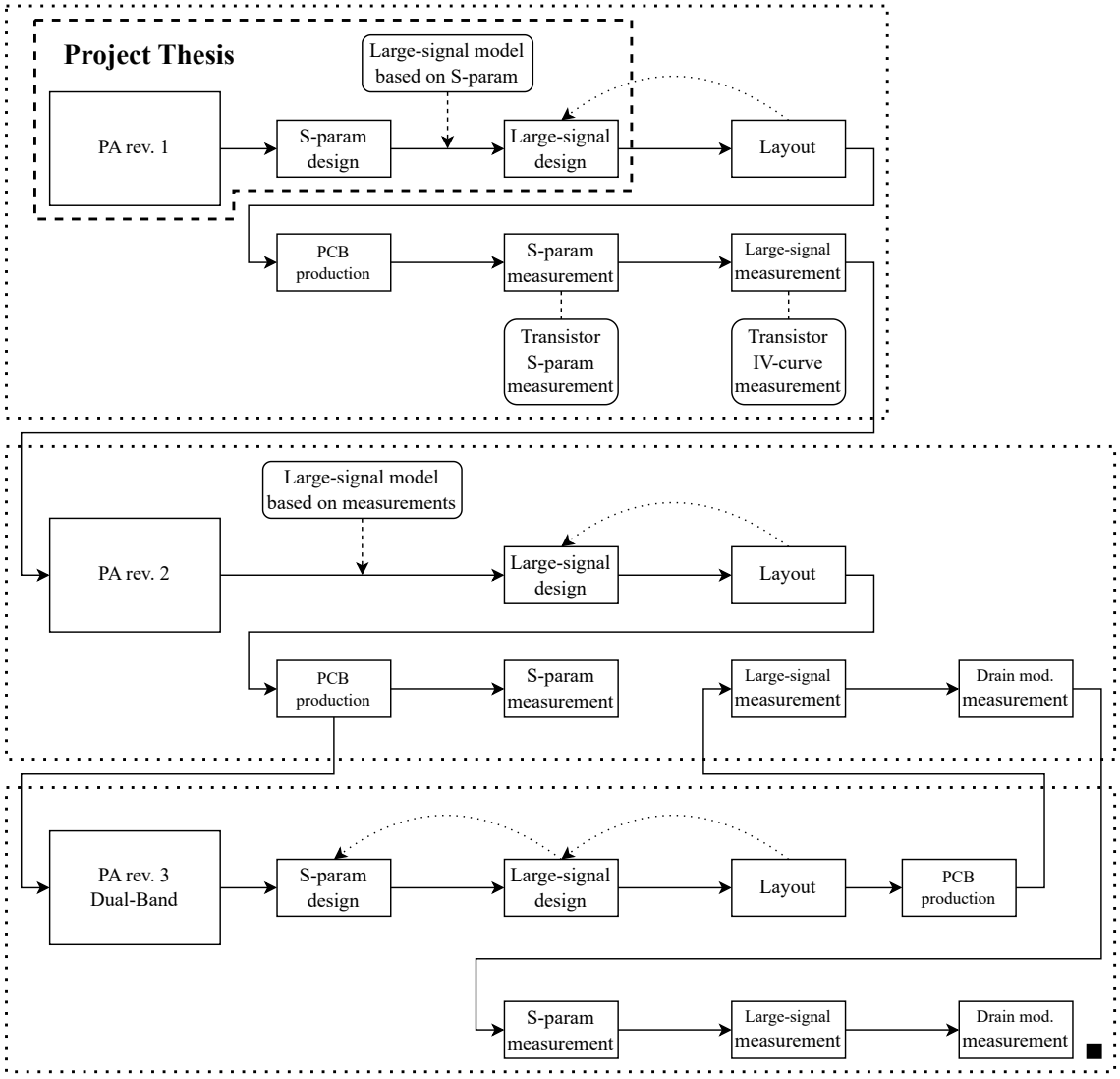


Figure 3.0.1: The workflow used when working on the different designs.

The dashed rectangle-like shape indicates what was part of the project thesis pre-work completed in advance. The dotted rectangles indicate what is part of the same PA revision. The dashed arrows indicate the introduction of a new transistor model. The dotted arrows indicate an iterative process between two or more tasks. Thus, the design of the first PA was slightly altered after finishing the project thesis work, as changes had to be done in the layout process. Notice that the work on the third revision PA was started while waiting to receive the second revision PA from production.

3.1 Advanced Design System

Advanced Design System (ADS) is an RF design program provided by Keysight Technologies and was the program used for the entire design process of all three PAs. The design process in ADS included creating schematics, optimizing and tuning the parameters in these schematics, and finally creating layouts and generating production files for these.

3.2 Transistor Model

3.2.1 XF1001-SC

In the case of the transistor chosen in our design, the MACOM XF1001-SC GaAs Heterojunction Field-Effect Transistor (HFET), S-parameters were provided but not any model describing large-signal behavior. As the PA we are designing at times will be operating in the area where the gain is non-linear, it is necessary to know how its S-parameters change in this region to be able to perform realistic simulations. One way of determining the large-signal behavior is to perform measurements of the device's gain and output power while the source and load impedances change and then use these measurements to create a model for the transistor's large-signal operation, [9, p. 598].

To be able to create a prototype PA before receiving the physical transistor, Morten Olavsbråten created a large-signal model based on the S-parameters delivered by MACOM technologies. This model was used for the design of the initial single PA. Then real-world measurements of the transistor were taken and used in a modified model to enhance the trustworthiness of the simulations done in ADS. This new model was then used when designing the second revision, and later the third revision, of the PA.

3.2.2 Measurements

S-Parameters For the XF1001-SC transistor, MACOM provides S-parameter files that can be used in simulations. However, it is not always certain if this model lines up with reality. To do measurements of, and create a new model from, the S-parameters will help us decide if the model is a good one, or if it is not, it will provide us with a usable model. One factor that may play a role in the correctness of the model is whether the model uses the same points as input and output as you do when measuring. Using different points as a reference will have an impact on the length of the transmission lines into and out from the device, which again will affect input and output networks and the performance of the device. In addition to this, the S-parameters provided by MACOM were only valid for certain drain voltages and a specific drain current. Thus, doing measurements at different drain voltages and currents will give us the possibility of creating a more general model. When doing measurements an Aim-TTi MX100CP Quad Output Multi-Range DC Power Supply, and an Agilent Technologies E8364B 10 MHz - 50 GHz PNA Series Network Analyzer was used, as illustrated in Figure 3.2.1. Before using this to perform measurements, it was necessary to do a calibration. This was done by using a Hewlett Packard 85052D calibration kit and following the onboard calibration program on the network analyzer. To be able to connect to the transistor, Morten Olavsbråten created a test board with 50Ω-transmission lines from the transistor connection pads out to the connectors. The transistor was attached to the board using a 3D-printed clamp. To avoid a potentially too high output power attenuators were used. Two attenuators, each with a 3 dB loss, where the one mounted closest to the test board's RF output had the highest power rating (colored dark). In between the board and the attenuators was a Hewlett Packard 11590B

bias network connected to provide the drain bias voltage. This bias network had a maximum insertion loss of 0.8 dB, [18].

To be able to measure the transistor directly at its pins, the test board also had connections for its onboard *short*, *open*, and *load*, to be able to re-calibrate with the characteristics of the board.

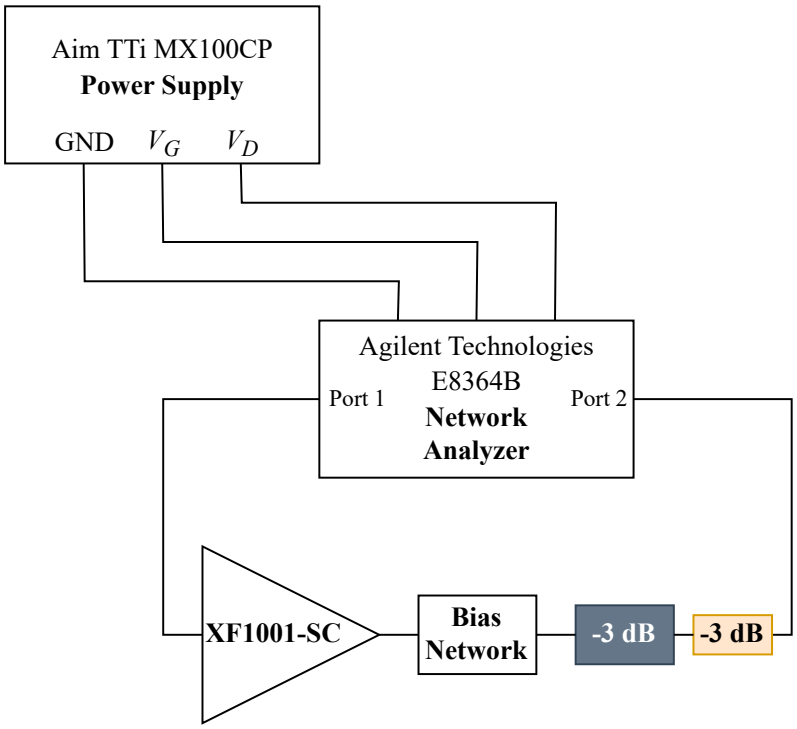


Figure 3.2.1: The setup used for measuring the S-parameters of the transistor.

Here the bias network was attached externally to the test board and is therefore included as a separate component in the setup overview. This will not be the case for the PAs tested later. The attenuators are also included in the overview here, as it is the first time they are used. Attenuators will in later measurements be included in the physical setup as separate components but will not be mentioned in the figures giving an overview of the setup. What the transistor S-parameter measurement setup actually looked like can be seen in Figure 3.2.2.

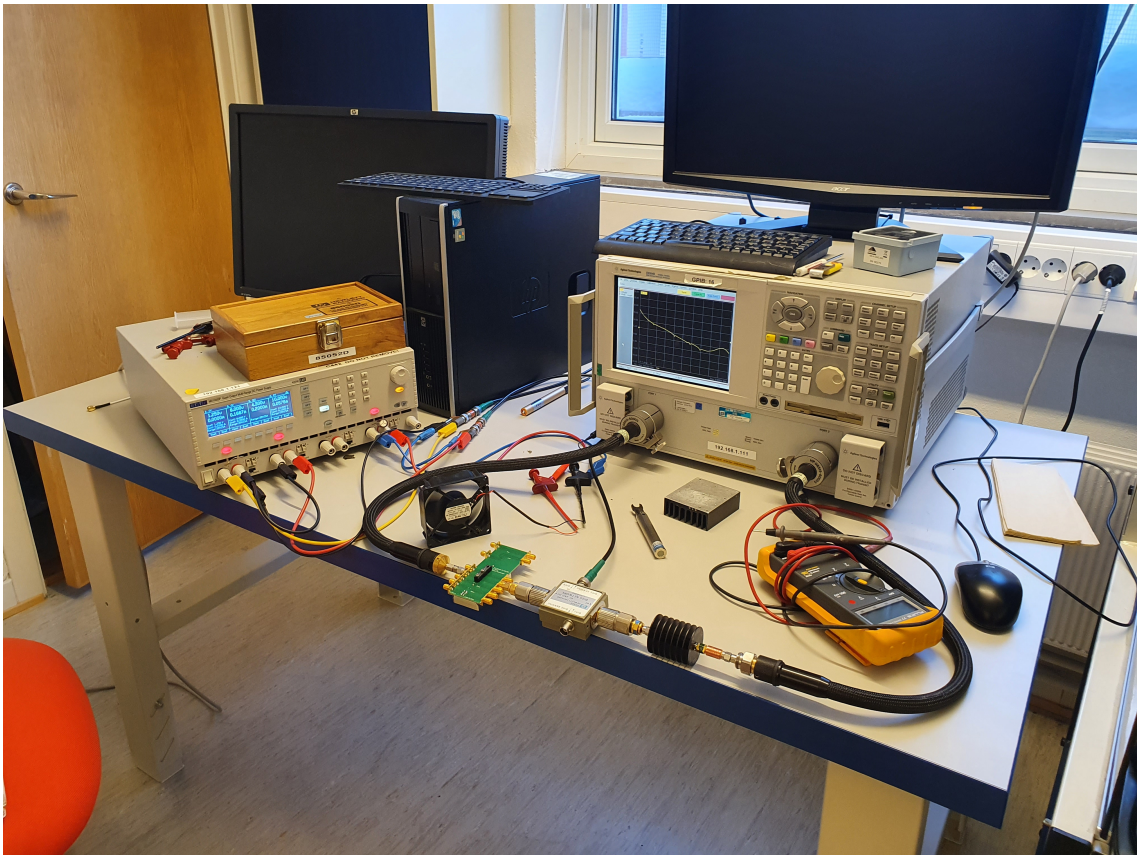


Figure 3.2.2: Picture of the setup used for measuring the S-parameters of the transistor.

When doing the measurements, different gate and drain voltages were applied to the transistor, resulting in different drain currents. The transistor has a gate voltage absolute maximum range of $-2.5\,\mathrm{V} < V_G < 0$. At the moment of performing the measurements, we had only received two transistors from the supplier. Thus, a decision was made to only perform measurements well within this range.

As shown in Table 3.2.1, the gate voltage, V_G, had a minimum value of -2.000 V and a maximum value of -0.727 V when a positive drain voltage, V_D, was applied. When doing *cold capacitor* measurements of the transistor, where the drain voltage is set to zero, 0.500 V steps between -2.000 V and 0.000 V were used. Setting V_G and V_D to certain values results in the conduction of a drain current, I_D.

The procedure of performing the measurements started by measuring the transistor in a completely passive state, where both V_G and V_D were set to zero and no drain current is present. Then the cold capacitor measurements were done, before applying V_D in order for the transistor to start conducting. V_G was set to the lowest value of -2.000 V and V_D was increased from zero to 2.000 V, to 5.000 V, and lastly to 8.000 V. These values were chosen, as the S-parameters provided by MACOM were said to be valid for drain voltages of either 5 V or 8 V and a drain current of 300 mA. In addition to this, it is convenient to have a model valid for a lower drain voltage, as the transistor is supposed to be used in, among other things, an envelope tracking configuration.

The onward procedure consisted of setting V_D to 5 V and then increasing V_G until I_D reached a

certain value. Afterward, V_G was held at the same value and V_D was first lowered to 2.000 V and then increased to 8.000 V. At each of the points with different values for V_G and V_D, I_D was noted and S-parameters were saved.

Table 3.2.1: Gate voltage, V_G, drain voltage, V_D, and drain current, I_D, used when measuring S-parameters of the XF1001-SC transistor.

V_G	V_D	I_D
-2.000 V	0.000 V	0 mA
-1.500 V	0.000 V	0 mA
-1.000 V	0.000 V	0 mA
-0.500 V	0.000 V	0 mA
0.000 V	0.000 V	0 mA
-2.000 V	2.000 V	0 mA
-2.000 V	5.000 V	2 mA
-2.000 V	8.000 V	8 mA
-1.650 V	2.000 V	15 mA
-1.650 V	5.000 V	50 mA
-1.650 V	8.000 V	71 mA
-1.250 V	2.000 V	108 mA
-1.250 V	5.000 V	150 mA
-1.250 V	8.000 V	167 mA
-0.727 V	2.000 V	282 mA
-0.727 V	5.000 V	300 mA
-0.727 V	8.000 V	302 mA

Large-Signal As earlier mentioned, MACOM does not provide files describing the large-signal behavior of the transistor. This makes it necessary to perform measurements in order to create a usable model. Large-signal measurements were done in collaboration with Morten Olavsbråten, using a setup where a program written in Matlab controls two power supplies. One power supply stepping the gate voltage and the other one sweeps the drain voltage from 0 to 8 V at each step of the gate voltage. Plotting the drain current when doing this gives the IV-curves shown in Figure 3.2.3.

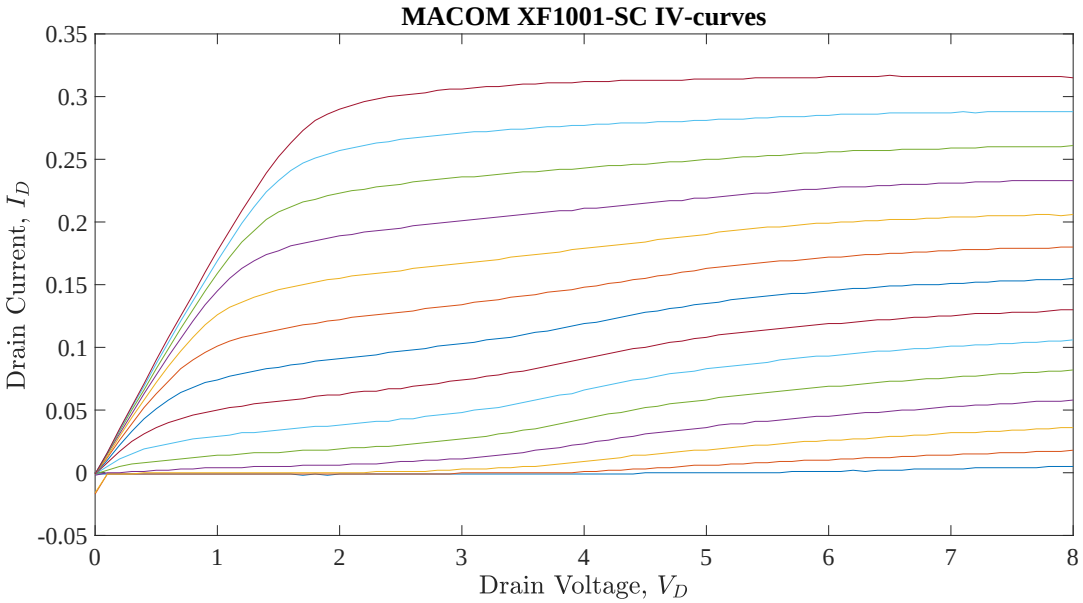


Figure 3.2.3: IV-curves of the MACOM XF1001-SC transistor. The different curves represent different gate voltages, V_G, the x-axis shows the drain voltage, V_D, and the y-axis shows the drain current, V_D.

The data represented by the curves in Figure 3.2.3 were then used by Morten Olavsbråten to describe the transistor by using the Angelov model[3].

3.3 Power Amplifier, vol. 1

Designing the single PA consists of choosing a suitable transistor, which in previous work was done by Morten Olavsbråten, and designing the networks around this transistor. The networks are a bias network, an input-matching network, and an output-matching network. The input-matching network will be the connection between the input of the PA and the gate of the transistor, while the output-matching network will be the connection between the drain of the transistor and the output of the PA. Two identical bias networks will be used as the connection between the lower DC voltage supply and the transistor gate and as the connection between the higher DC voltage supply and the transistor drain.

[3]A transistor model created by Iltcho Angelov at Chalmers University, [19]

3.3.1 Schematic

The creation of the schematics for this first revision of the PA was described in detail in the project thesis written as a pre-study to this thesis and will therefore not be covered here.

3.3.2 Simulations

As with section 3.3.1, this was covered in detail in the project thesis. However, some numbers are included here in Table 3.3.2 and 3.3.3 to compare with the measured results and with the simulated results of the later revisions of the PA.

Table 3.3.1 shows the variables of the PCB substrate used for revision 1.

Table 3.3.1: Substrate details of the FR4 substrate used in the PCB. H is substrate thickness, ε_r is relative dielectric constant, Mur is relative permeability, $Cond$ is conductor conductivity, Hu is cover height, T is conductor thickness, $TanD$ is dielectric loss tangent, and $Rough$ is conductor surface roughness protrusion height.

Variable	**Value**
H	1.52 mm
ε_r	4.4
Mur	1
$Cond$	$5.96 \cdot 10^7$ S/m
Hu	$1 \cdot 10^{33}$ mm
T	35 μm
$TanD$	0.02
$Rough$	0 mm

Table 3.3.2: S-parameter simulation results at 2.4 GHz of vol. 1 of the prototype PA.

S_{21}**, 2.4 GHz**	S_{11}**, 2.4 GHz**	S_{22}**, 2.4 GHz**
9.416 dB	-14.22 dB	-5.787 dB

Table 3.3.3 shows the simulated performance of the PA at 2.4 GHz frequency, with a drain current of 300 mA, and an output power of 30.01 dBm.

Table 3.3.3: Power gain simulation results of vol. 1 of the prototype PA.

$P_{O,fund.}$	G_T	**Gain Comp.**	**PAE**	V_G	V_D	I_D
30.01 dBm	8.46 dB	0.96 dB	29.13 %	-0.533 V	8 V	300 mA

3.3.3 Layout

The layout of the PCB pertaining to the PA is seen in Figure 3.3.1.

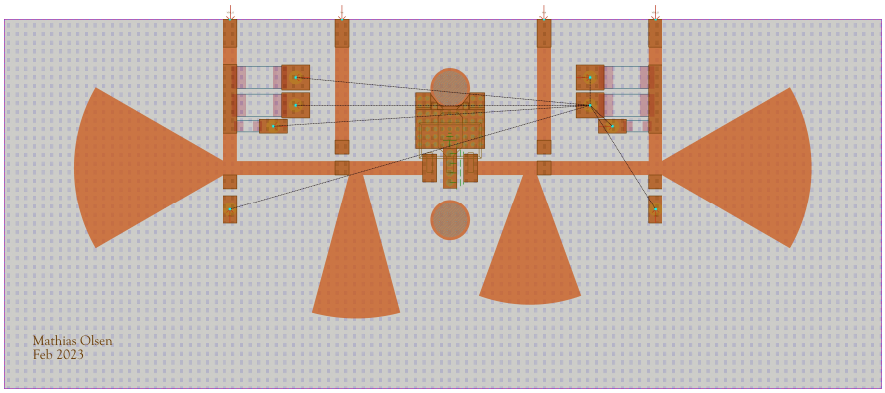


Figure 3.3.1: The PCB layout of the PA. The black lines symbolically connect the points representing the ground net.

For simplicity, in this first design, all line widths were fixed to 1 mm in this design and the same goes for the width of the connection points of the matching stubs. The four lines ending at the top edge of the PCB have different connectors connected to them. The outer lines have DC voltages applied to them. The gate DC voltage at the leftmost one and the drain DC voltage at the rightmost one. The two lines in the middle are where the RF connectors are found. The RF input to the left and the RF output to the right, respectively. To have all connectors at the same side was done because of a relatively compact design in combination with the need for spacing between the fan-formed matching stubs and other transmission lines, soldering pads, and holes.

3.3.4 Physical Printed Circuit Board

The physical PCB for revision one is displayed in Figure 3.3.2.

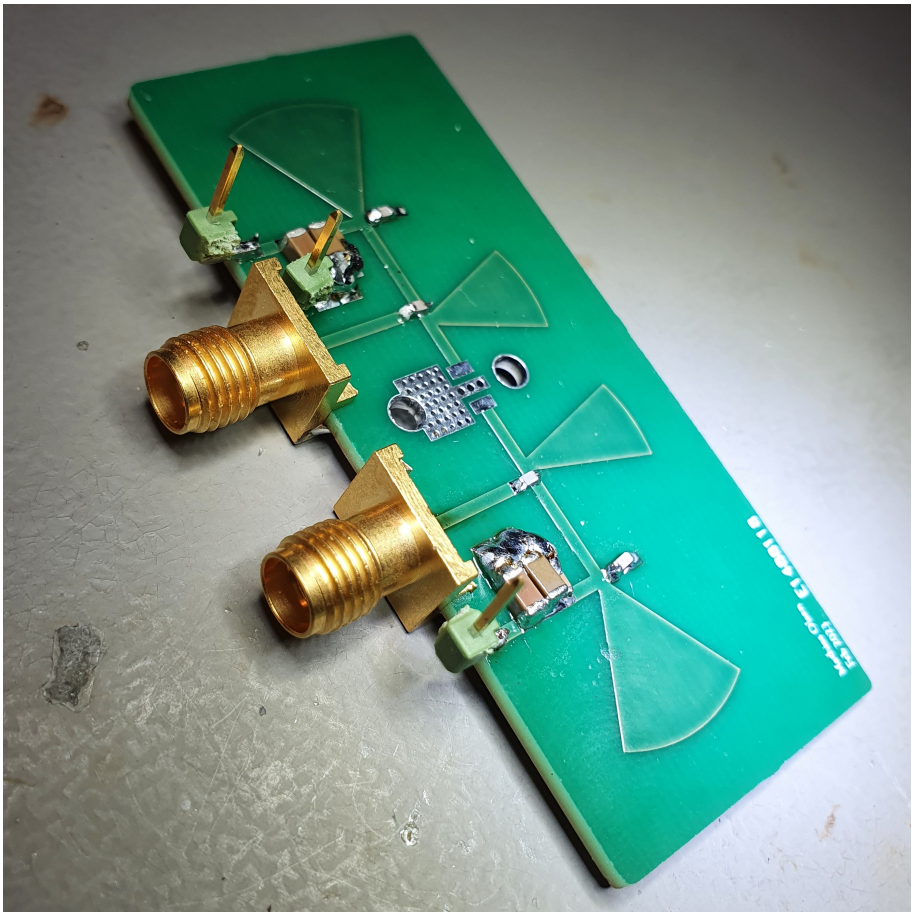


Figure 3.3.2: The physical PCB with the earth plane, to later be covered by the transistor, exposed. The transistor is later attached to the PCB with a 3D-printed plastic clamp and two screws.

When soldering the PCB it was discovered that the footprints of the capacitors used between the DC entry points and the ground planes resulted in a too large distance for the capacitors to cover, which is the reason for the large amounts of solder used at the mentioned ground planes. Thus, for the next revision, gaps with a shorter distance will be used instead of the footprints provided for the capacitors.

All three of DC connection points, gate bias, drain bias, and ground, have simple pin connectors. The RF input and output connections have 3.5 mm SMA connectors connected to them.

3.3.5 Measurements

S-Parameters The S-parameters of the PA were measured using the same method as in section 3.2.2, with the setup illustrated in Figure 3.3.3, using an Aim-TTi MX100CP Quad Output Multi-Range DC Power Supply, and an Agilent Technologies E8364B 10 MHz - 50 GHz PNA Series Network Analyzer. Before the measurements were performed, the setup had to be calibrated. This was done using the network analyzer's onboard calibrating routine and the Hewlett Packard 85052D calibration kit.

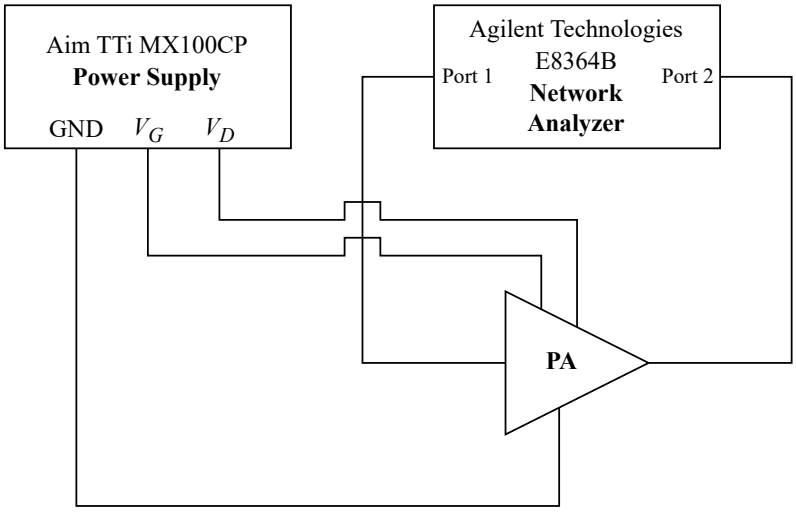


Figure 3.3.3: The setup used for measuring the S-parameters of the rev. 1 PA.

Now only two different points of drain current were measured, as shown in Table 3.3.4. Such few points, compared to what was the case with the transistor alone, were measured because these measurements are not done to create a model of the PA to be used in further simulations but rather just to observe how the PA performs at certain levels of drain current.

Table 3.3.4: Drain voltage, V_D, drain current, I_D, and gate voltage, V_G, used when measuring S-parameters of vol. 1 of the prototype PA.

V_D	I_D	V_G
8.000 V	150 mA	-1.315 V
8.000 V	300 mA	-0.721 V

Large-Signal When measuring the large-signal performance of the PA, a setup equal to the one described for measuring the large-signal behavior of the transistor in section 3.2.2 was used.

An overview of the setup is found in Figure 3.3.4.

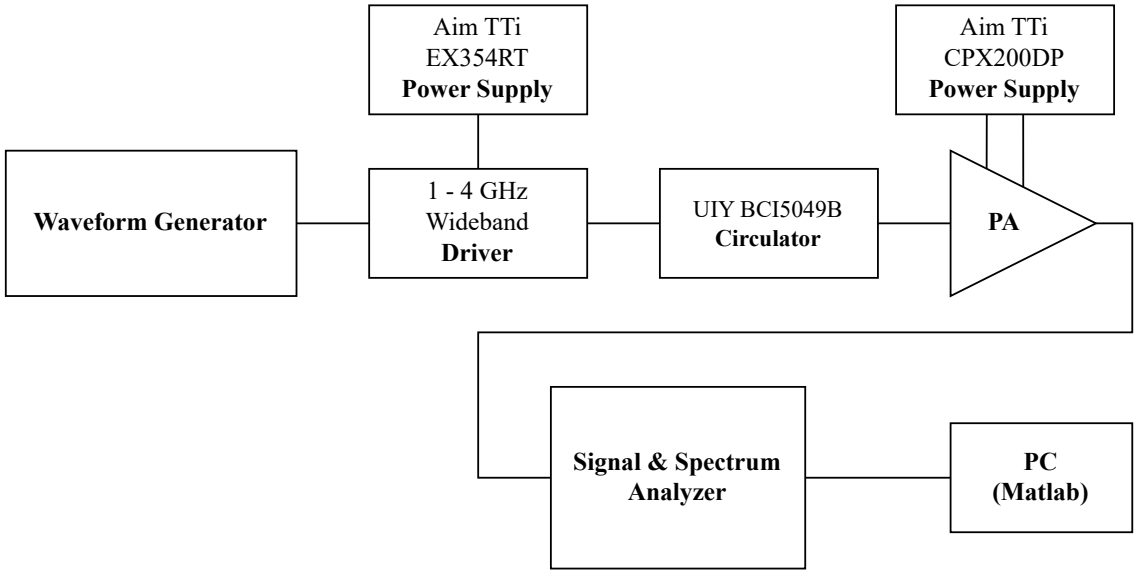


Figure 3.3.4: The setup used for measuring the large-signal behavior of the rev. 1 PA.

In addition to the components in the figure, attenuators were used on the output of the PA to avoid too high output power transmitting from the PA into the spectrum analyzer.

3.4 Power Amplifier, vol. 2

For the second revision of the PA, the following improvements from the first revision are in focus:

- Increase the gain to achieve $G_T \geq 10$ dB for $P_{out} = 30$ dBm.
- Increase the PAE.
- Change placement of input connector, output connector, and bias voltage connectors, for easier connection.

Having more exact parameters for both the substrate used in the PCB and the large-signal behavior of the transistor are major reasons for revision 2 of the PA to perform better than revision 1. For this second revision there will be created two separate PAs, where one is optimized for a drain current of 300 mA, operating as a class A amplifier, and the other is optimized for a drain current of 50 mA, operating as a class AB amplifier. Thus, the 300 mA PA is expected to have a higher gain and linearity than the 50 mA PA at the same output power, while the 50 mA PA is expected to have a higher efficiency, [7, p. 24].

When designing the second revision, rev. 1 of the PA is used as a starting point. Then the transistor model is changed and the substrate parameters are altered to match the new substrate that will be used. After this, the different parameters in the networks surrounding the transistor are adjusted.

The transmission line widths were changed to a width corresponding to a characteristic impedance of 50 Ω, in order to decrease losses, [9, p.148]. This was done by using a tool in ADS called

LineCalc. The new substrate parameters, seen in Table 3.4.1, are entered together with the frequency of interest, 2.4 GHz, and the desired line impedance, 50 Ω.

Table 3.4.1: Substrate details of the IS400 substrate used in the PCB. H is substrate thickness, $varepsilon_r$ is relative dielectric constant, Mur is relative permeability, $Cond$ is conductor conductivity, Hu is cover height, T is conductor thickness, $TanD$ is dielectric loss tangent, and $Rough$ is conductor surface roughness protrusion height.

Variable	**Value**
H	1.473 mm
ε_r	4.46
Mur	1
$Cond$	$5.8 \cdot 10^7$ S/m
Hu	$1 \cdot 10^{33}$ mm
T	35 μm
$TanD$	0.019
$Rough$	0 mm

These substrate parameters result in a line width of 2.76915 mm, summarized in Table 3.4.2.

Table 3.4.2: Characteristic line impedance, Z_0, at a frequency f, for a transmission line with width W.

Z_0	f	W
50 Ω	2.4 GHz	2.76915 mm

The process of transitioning from the first to the second revision PA was in essence to use the optimize tool in ADS and increase the number of variables to be optimized within certain limits, instead of just using the tuning function. During the optimization process the all the networks were optimized simultaneously for most of the time. When using the optimization tool, some goals are set that the optimizer works towards. The goals were altered a bit through the process, as it seemed more important to focus on one parameter than another. In the simulation method that was used, the one named *HB1TonePAE_Pswp*, the frequency is set to a fixed value and then the input power is swept. Goals were set for:

- Minimum gain (Expression: "Gain_Transducer")
- Minimum delivered output power (Expression: "Pdel_dBm")
- PAE (Expression: "PAE")

The minimum gain goal contained three limits. One with a limit equal to the minimum acceptable gain of 10 dB. This limit was weighted high, e.g., 1000, to get a high priority. In addition to this an even higher gain limit, e.g., 14 dB, was set in order to achieve a higher gain if the other goals were already met. For this goal to have a lower priority it was weighted low, e.g., 1. Lastly, a goal with a high priority, limited to a specific region in the higher part of the power spectrum, e.g., 29.9 to 30.1 dBm, to ensure sufficient gain up to 30 dBm output power, was applied. This goal also had a 10 dB gain as a limit, and a high priority, and provided an extra contribution to the optimization calculations.

The minimum delivered output power goal had a limit of a minimum of 30 dBm and was set to be valid when the input power was 20 dBm or above. This implied a gain of 10 dB at 20 dBm input power. The goal was not set to be valid below this input power level, as it had a high priority and would produce unrealistic demands for the lower input powers.

The PAE goal was set to an unrealistically high value, e.g., 80 %, with a low priority, in order for it to be considered, but not be the most important factor, in the calculations.

Mainly the gradient optimization type was used, which calculates gradients to get closer to an optimal configuration. The thing to be alert of when using this optimization type is to settle with local instead of global optimums. To challenge this some values were "kickstarted" when seemingly getting stuck at their minimum or maximum allowed value. This was done by entering the tuning mode in the optimization console and pulling the variable value to the opposite extreme and letting the optimization start working again. Another way of avoiding the problem with local optimums is to use the random function. However, when optimizing for a high number of variables this requires calculations for a higher number of points than what may be possible with the available computing power. So in this process mainly the gradient mode was used.

The approach described above was used in the design process for both the 300 mA drain current and the 50 mA drain current PA. The 300 mA version was designed first and then later this design was re-optimized with the gate voltage changed to a value giving a 50 mA instead of a 300 mA drain current.

3.4.1 Schematic

Optimized for 300 mA Schematics for the PA designed for a 300 mA drain current follow.

Figure 3.4.1 shows the circuit providing the bias voltage for the gate of the transistor. In order to provide a bias point that is as stable as possible, the idea is that when TL_3 is shorted, the output reflection S_{22} of the network will act as a short-circuit for the center-frequency of 2.4 GHz and ideally for the second-harmonic 4.8 GHz as well. The transmission line TL_3 is added with its length being equal to the quarter of a wavelength for a frequency of 2.4 GHz. Thus, at 2.4 GHz, the impedance will be inverted and the short-circuit will instead appear as an open end, prohibiting the 2.4 GHz signal from escaping into the bias network. For the second harmonic of 4.8 GHz on the other hand, the length of the transmission line will correspond to half a wavelength, or in other words two quarter-wavelengths. Thus, the impedance observed in S_{22} will first be converted from a short-circuit to an open end and then back to a short-circuit again, assisting in suppressing the undesired effects of the second-harmonic frequency, [9].

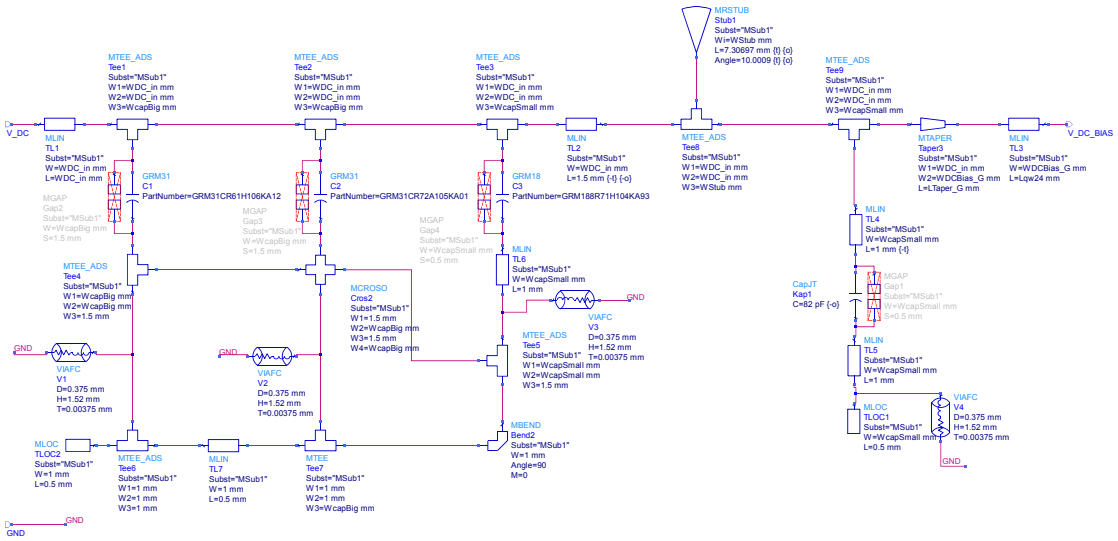


Figure 3.4.1: The bias network for the input of the second revision PA, optimized for 300 mA drain current. The length from the bottom of $Stub_1$ to TL_3, consisting of W_3 of Tee_9 and L of $Taper_3$, adds up to 2.27 mm.

The part to the right of the schematic is where we find the part realizing the behavior described above. Table 3.4.3 summarizes the values of these components. A taper is used to create a smoother transition between lines with different widths and to be able to include the transition's behavior in the simulations. A rule of thumb is that the angle of the taper should not exceed 45° and as a result, the different lengths of most of the tapers in this thesis is decided by a formula, $l_{Taper} = \frac{\text{abs}(w_1 - w_2)}{2}$, where w_1 is is the width of the taper's input line and w_2 is the width of the taper's output line. This makes sure that an angle of 45° is always maintained and as well that the tapers are not longer than what is necessary.

Table 3.4.3: Values for components used in the input bias network of the second version of the PA.

(a) Capacitance and manufacturer of capacitor.

Variable name	Value	Manuf.
C	82 pF	Johanson

(b) Length, width, and angle of transmission lines and stub.

Device name	Length	Width	Angle
$Stub_1$	7.31 mm	0.50 mm	10.0°
TL_3	15.00 mm	0.50 mm	N/A

It can also be observed that next to every capacitor there is a crossed out gap. This is because the capacitor models are used when simulating but for the layout a gap with a certain length is used instead. This was done because of problems with the footprints being too long discovered on the PCB of the first revision PA. The components below the connections to ground, are there only to create a soldering pad for easier soldering of the capacitors and ground connectors. This was done to avoid having to add extra copper for every update of the layout during the process and to

have a continuous visual impression of what the soldering pad would look like as part of the whole design.

One change from the first to the second revision was that instead of having identical bias networks for the input and output, they got individual ones. The main idea for the output bias network was the same as for the input version but letting them be optimized independently should give a more optimal solution. Figure 3.4.2 shows that the basis of the schematic is the same as for the input bias network but with different values for the optimized variables.

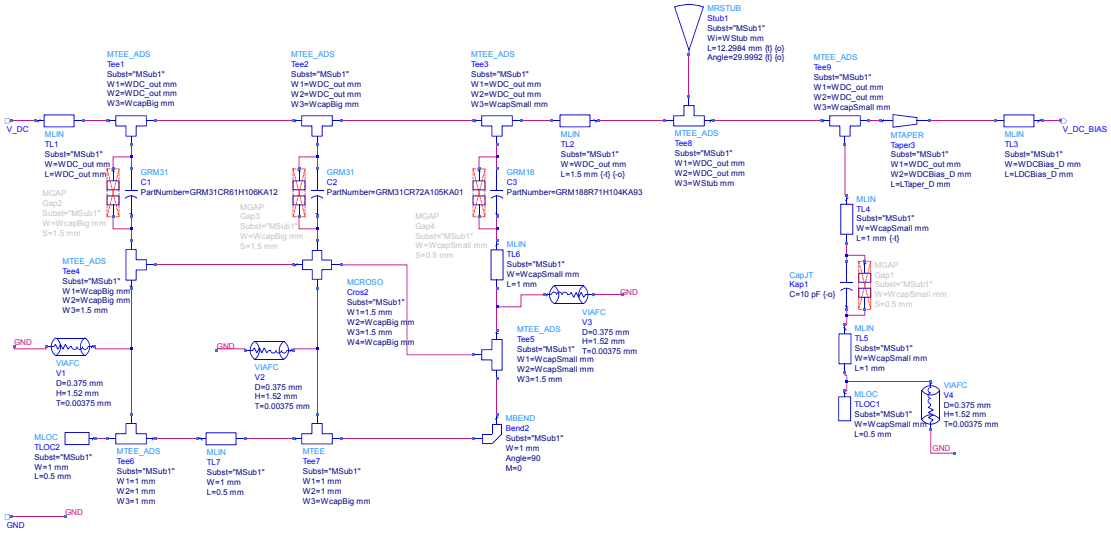


Figure 3.4.2: The bias network for the output of the second revision PA, optimized for 300 mA drain current. The length from the bottom of $Stub_1$ to TL_3, consisting of W_3 of Tee_9 and L of $Taper_3$, adds up to 1.30 mm.

Again the most essential values are summarized in Table 3.4.4.

Table 3.4.4: Values for components used in the output bias network of the second version of the PA.

(a) Capacitance and manufacturer of capacitor.

Variable name	Value	Manuf.
C	10 pF	Johanson

(b) Length, width, and angle of transmission lines and stub.

Device name	Length	Width	Angle
$Stub_1$	14.39 mm	2.14 mm	10.0°
TL_3	12.40 mm	1.41 mm	N/A

The input matching network, depicted in Figure 3.4.3, uses a single stub configuration, similar to what was described in the theory part, but is here open-ended instead of short circuited, which was the case for the bias network as well. Again, the design from the first revision was used as a

starting point and then optimized by ADS. The stub and the transmission lines to the right of it are the essential part of the input match. The bias voltage is connected as close as possible to the transistor gate. The taper between the bias input and the connection point to the transistor has fixed length to ensure spacing between line from the bias network and the ground pad underneath the transistor.

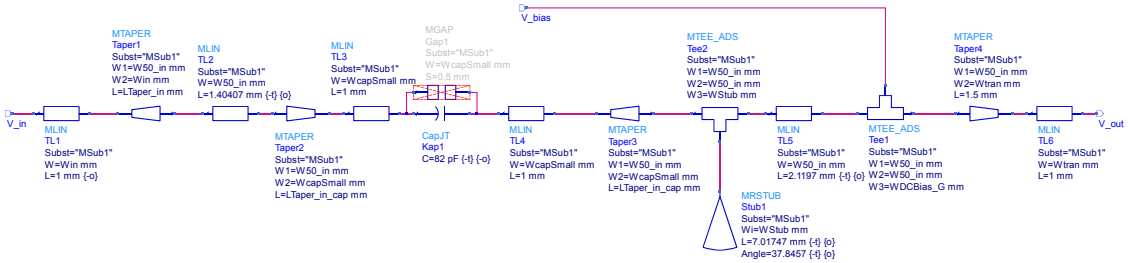


Figure 3.4.3: The input matching network of the second revision PA, optimized for 300 mA drain current.

The most important parameter values are summarized in Table 3.4.5.

Table 3.4.5: Values for components used in the input matching network of the second version of the PA.

(a) Capacitance and manufacturer of capacitor.

Variable name	Value	Manuf.
C	82 pF	Johanson

(b) Length, width, and angle of transmission lines and stub.

Device name	Length	Width	Angle
$Stub_1$	7.02 mm	3.00 mm	37.8°
TL_5	2.12 mm	2.77 mm	N/A

The output matching network, found in Figure 3.4.4, has a design that is in many ways equal to the design of the input matching network but with one added factor. This was that the line between the output from the transistor and the connection point of the bias network should suppress the second-harmonic. The principle used for this was that, as already explained for the bias network, the second-harmonic sees a short circuit to ground from the bias networks connection point. By then adding a quarter-wave transformer this short circuit would be converted to an open end, suppressing the second-harmonic. The quarter-wavelength of the second-harmonic, 4.8 GHz, was

found by the LineCalc tool to be 8.467690 mm. Then the stub and the line between the stub and the capacitor should help create a match that is as good as possible for the fundamental frequency. This was used as a starting point and then the optimizer worked on it to reach the goals mentioned earlier.

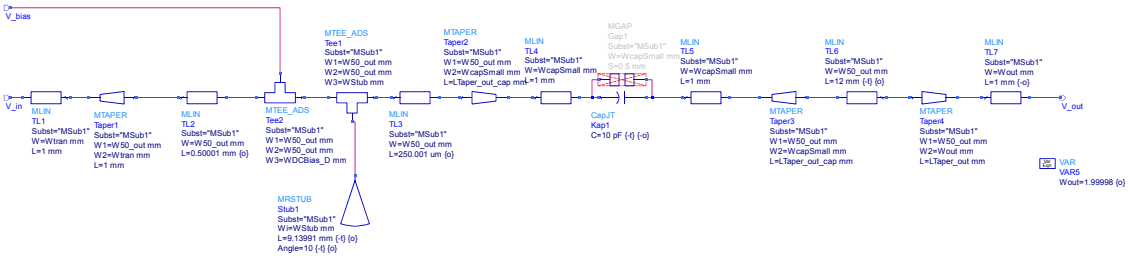


Figure 3.4.4: The output matching network of the second revision PA, optimized for 300 mA drain current.

The values of the most essential parameters are found in Table 3.4.6. As we see, the final value of TL_2 ended up quite a bit shorter, even when adding the line and taper it is connected, than the quarter-wavelength calculated for the second harmonic.

Table 3.4.6: Values for components used in the output matching network of the second version of the PA.

(a) Capacitance and manufacturer of capacitor.

Variable name	Value	Manuf.
C	10 pF	Johanson

(b) Length, width, and angle of transmission lines and stub.

Device name	Length	Width	Angle
TL_2	500 μm	2.77 mm	N/A
$Stub_1$	9.14 mm	3.00 mm	10.0°
TL_3	250 μm	2.77 mm	N/A

Optimized for 50 mA As mentioned the PA designed for a 50 mA drain current, was created by performing a re-optimization of the one designed for a 300 mA drain current. Therefore, this will just be a summary of the what the schematics ended up looking like.

The input bias network is depicted in Figure 3.4.5 and its key parameter values are summarized

in Table 3.4.7.

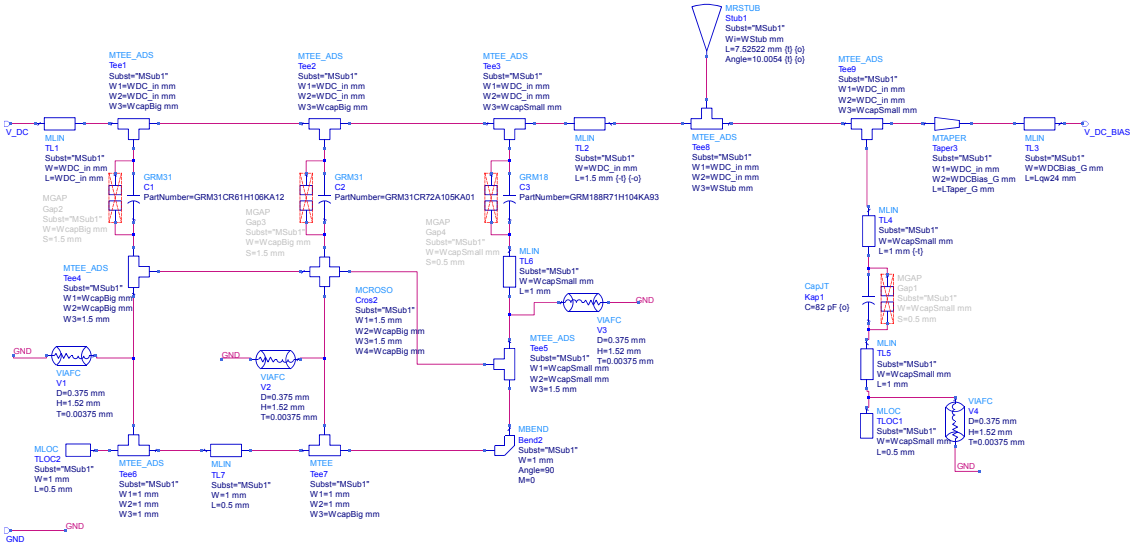


Figure 3.4.5: The bias network for the input of the second revision PA, optimized for 50 mA drain current.

Table 3.4.7: Values for components used in the input bias network of the 50 mA version of the second revision PA.

(a) Capacitance and manufacturer of capacitor.

Variable name	Value	Manuf.
C	82 pF	Johanson

(b) Length, width, and angle of transmission lines and stub.

Device name	Length	Width	Angle
$Stub_1$	7.53 mm	0.50 mm	10.0°
TL_3	15.00 mm	0.50 mm	N/A

The output bias network is depicted in Figure 3.4.6 and its key parameter values are summarized in Table 3.4.8.

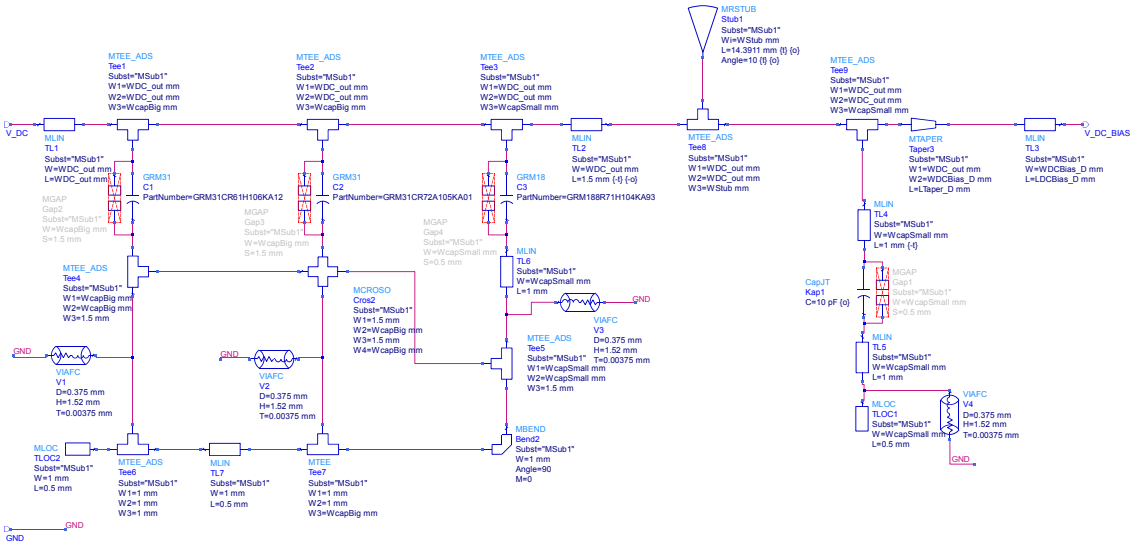


Figure 3.4.6: The bias network for the output of the second revision PA, optimized for 50 mA drain current.

Table 3.4.8: Values for components used in the output bias network of the 50 mA version of the second revision PA.

(a) Capacitance and manufacturer of capacitor.

Variable name	Value	Manuf.
C	10 pF	Johanson

(b) Length, width, and angle of transmission lines and stub.

Device name	Length	Width	Angle
$Stub_1$	14.39 mm	1.99 mm	10.00°
TL_3	10.00 mm	1.59 mm	N/A

The input matching network is depicted in Figure 3.4.7 and its key parameter values are summarized in Table 3.4.9.

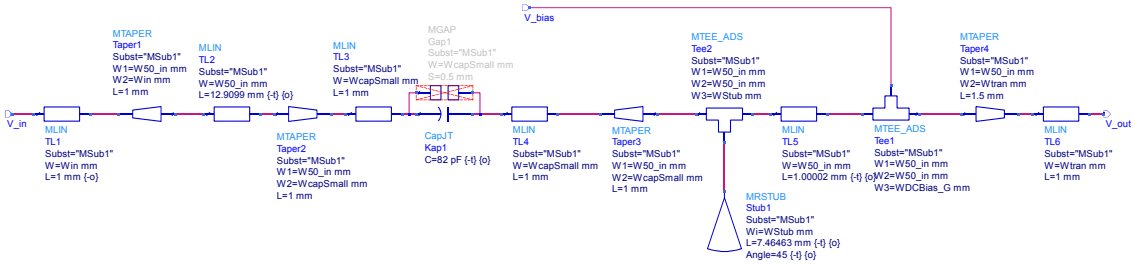


Figure 3.4.7: The input matching network of the second revision PA, optimized for 50 mA drain current.

Table 3.4.9: Values for components used in the input matching network of the 50 mA version of the second revision PA.

(a) Capacitance and manufacturer of capacitor.

Variable name	**Value**	**Manuf.**
C	82 pF	Johanson

(b) Length, width, and angle of transmission lines and stub.

Device name	**Length**	**Width**	**Angle**
$Stub_1$	7.46 mm	3.00 mm	45°
TL_5	1.00 mm	2.77 mm	N/A

The output matching network is depicted in Figure 3.4.8 and its key parameter values are summarized in Table 3.4.10.

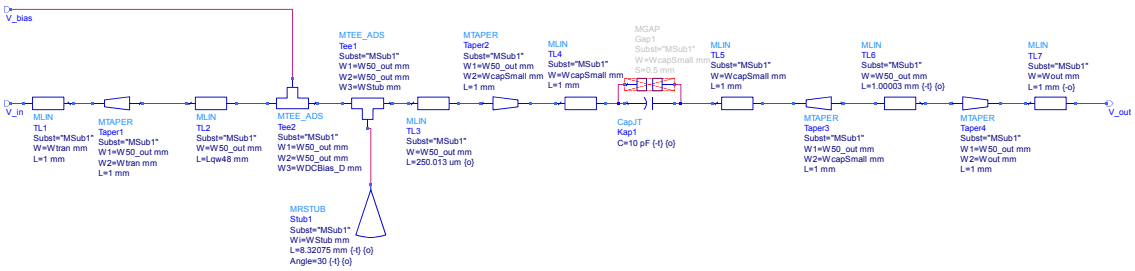


Figure 3.4.8: The output matching network of the second revision PA, optimized for 50 mA drain current.

Table 3.4.10: Values for components used in the output matching network of the 50 mA version of the second revision PA.

(a) Capacitance and manufacturer of capacitor.

Variable name	Value	Manuf.
C	10 pF	Johanson

(b) Length, width, and angle of transmission lines and stub.

Device name	Length	Width	Angle
TL_2	736 μm	2.77 mm	N/A
$Stub_1$	8.32 mm	3.00 mm	30°
TL_3	250 μm	2.77 mm	N/A

3.4.2 Simulations

When optimizing and simulating the circuits of this second revision PA, the large-signal simulations were in focus. The S-parameter simulations were only performed as a quality check after the large-signal processes were finished.

Large-Signal During the large-signal simulations the predefined HB1-tone power sweep simulation setup in ADS was used. The setup is shown in Figure 3.4.9.

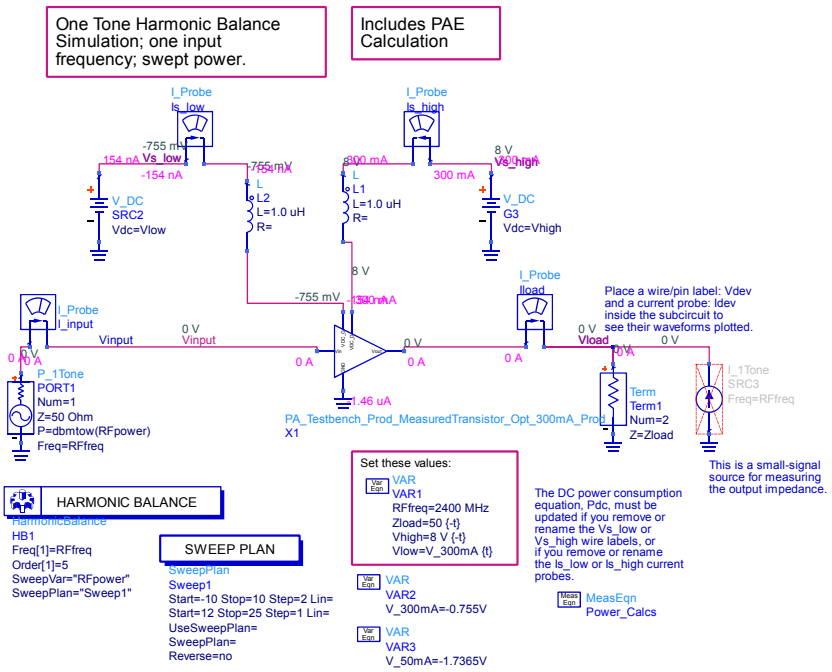


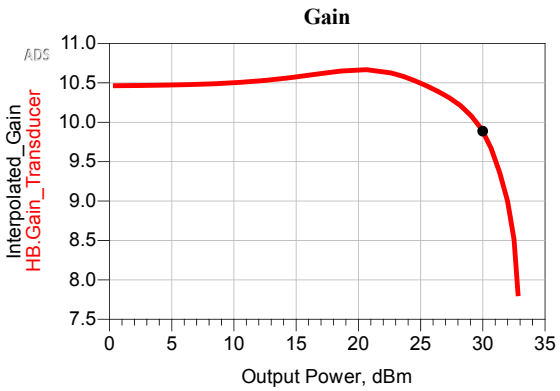
Figure 3.4.9: Simulation setup used in ADS for large-signal analysis of the second revision PA. Here the 300 mA PA is the one being measured.

The small-signal current source used for measuring the output impedance was disabled when performing the measurements, because it created problems when running the optimization function. Table 3.4.11 contains variables that was used in the setup for simulation. $RFfreq$ was the RF frequency used, $Zload$ was the load impedance used, $Vhigh$ set the drain bias voltage, and $Vlow$ set the gate bias voltage. V_300mA and V_50mA contained the gate voltages giving drain currents of 300 and 50 mA, respectively.

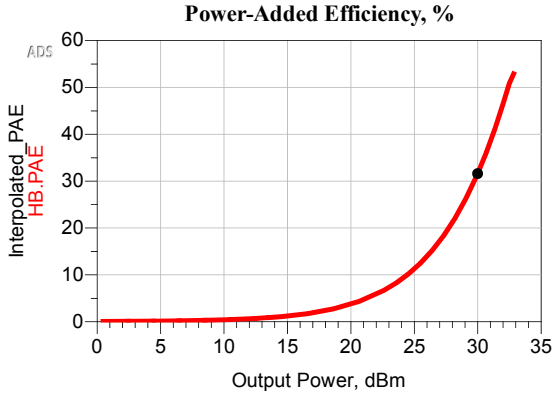
Table 3.4.11: Variables in the simulation setup.

Variable	**Value**
$RFfreq$	2400 MHz
$Zload$	50 Ω
$Vhigh$	8 V
$Vlow$	V_300mA or V_50mA
V_300mA	-0.755 V
V_50mA	-1.7365 V

The large-signal simulation results, being transducer power gain, G_T, vs. output power, P_{out}, and PAE vs. output power, for the 300 mA version are found in Figure 3.4.10.



(a) Simulated gain vs. output power.



(b) Simulated PAE vs. output power.

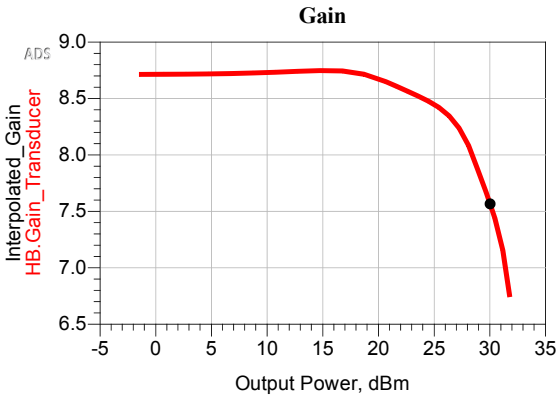
Figure 3.4.10: Large-signal simulation results of the 300 mA version.

We can see that the simulations show gain above 10 dB almost all the way up to 30 dBm output power and a peak PAE above 50 %. The results at approx. 30 dBm output power are summarized in Table 3.4.12.

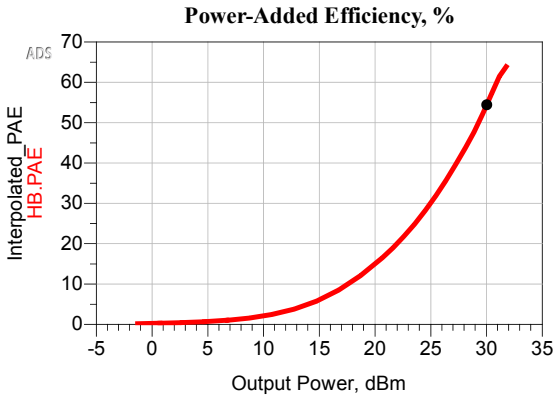
Table 3.4.12: Simulation results of vol. 2 of the prototype PA with a drain current of 300 mA.

P_{out}	G_T	**Gain Comp.**	**PAE**	$\mathbf{V_D}$	$\mathbf{I_D}$
29.99 dBm	9.89 dB	0.780 dB	31.60 %	8 V	300 mA

The large-signal simulation results for the 50 mA version are shown in Figure 3.4.11.



(a) Simulated gain vs. output power.



(b) Simulated PAE vs. output power.

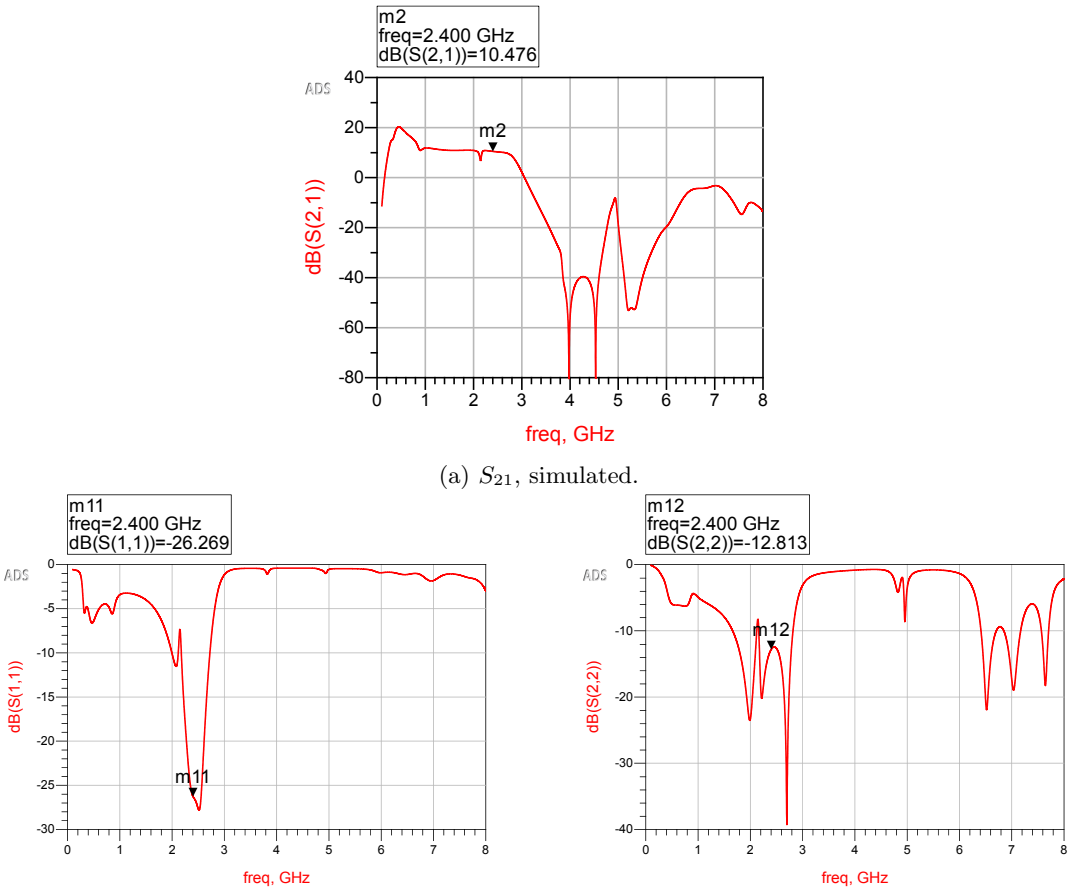
Figure 3.4.11: Large-signal simulation results of the 50 mA version.

For the 50 mA simulations, the gain in the lower, small-signal power region stays between 8.5 and 9 dB. It has dropped about 1 dB at 30 dBm output power. The peak PAE stops above 60 %. The results at approx. 30 dBm output power are summarized in Table 3.4.13.

Table 3.4.13: Simulation results of vol. 2 of the prototype PA with a drain current of 50 mA.

P_{out}	G_T	**Gain Comp.**	**PAE**	$\mathbf{V_D}$	$\mathbf{I_D}$
30.02 dBm	7.57 dB	1.18 dB	54.43 %	8 V	50 mA

S-Parameters The S-parameters were not focused on in the design of the rev. 2 PA. Instead the device was optimized using the HB1-tone power sweep simulation setup to get the best gain possible at output powers up to 30 dBm. However, to investigate if it looks like the input and output are matched to the source and the load, a simulation is performed and the results regarding S_{21}, S_{11} and S_{22} for the 300 mA PA are plotted in Figure 3.4.12.



(a) S_{21}, simulated.

(b) S_{11}, simulated.

(c) S_{22}, simulated.

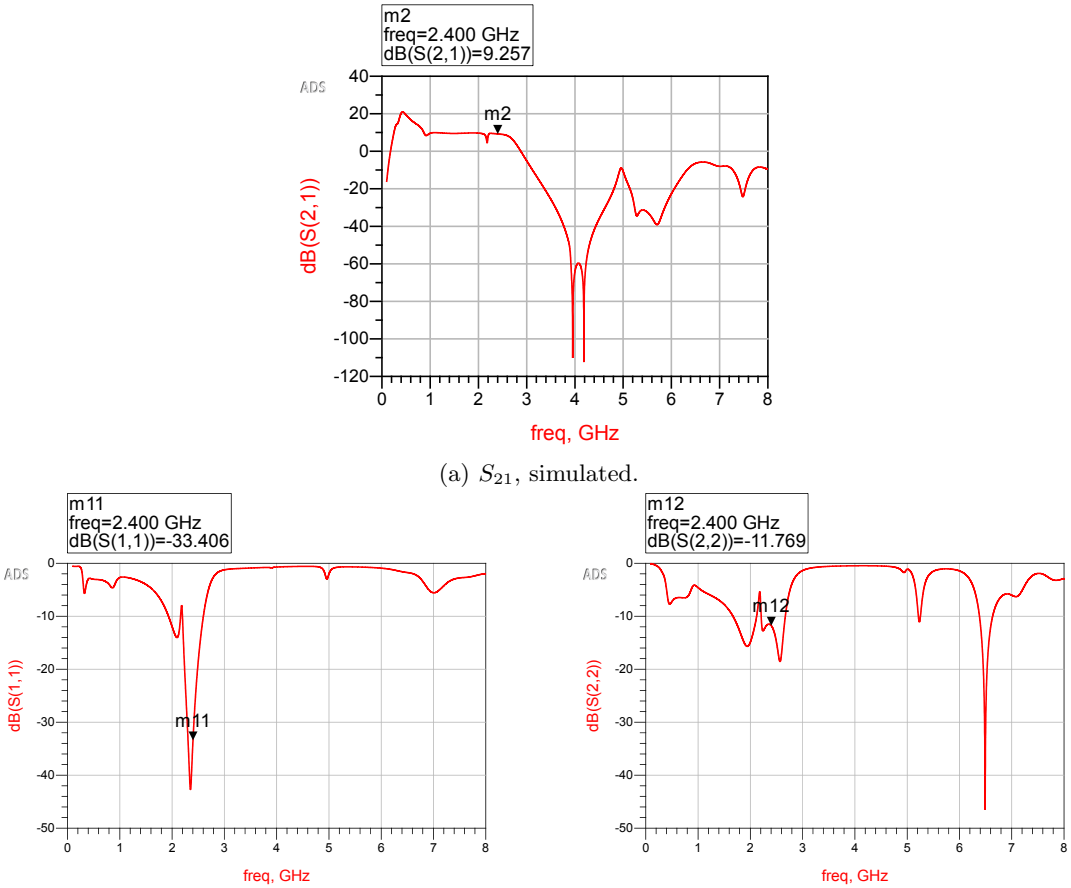
Figure 3.4.12: Simulated S-parameters of the 300 mA version.

And summarized in Table 3.4.14.

Table 3.4.14: S-parameter simulation results at 2.4 GHz of the 300 mA drain current version of the second revision PA.

S_{21}, **2.4 GHz**	S_{11}, **2.4 GHz**	S_{22}, **2.4 GHz**
10.48 dB	-26.27 dB	-12.81 dB

Results from the simulation of S_{21}, S_{11} and S_{22} for the 50 mA PA are plotted in Figure 3.4.13.



(a) S_{21}, simulated.

(b) S_{11}, simulated.

(c) S_{22}, simulated.

Figure 3.4.13: Simulated S-parameters of the 50 mA version.

And summarized in Table 3.4.15.

Table 3.4.15: S-parameter simulation results at 2.4 GHz of the 50 mA drain current version of the second revision PA.

S_{21}, **2.4 GHz**	S_{11}, **2.4 GHz**	S_{22}, **2.4 GHz**
9.257 dB	-33.41 dB	-11.77 dB

3.4.3 Layout

As opposed to revision number one, where all the input ports were at the same side of the PCB, the four different input ports are here placed on the four different edges. This is done for easier connection to the lab equipment and for a better overview of the board in general. Another noticeable update from the first edition of the PA, which was mentioned earlier, is the width of the lines. In revision one, the widths of all the lines were fixed at 1 mm. Now the lines between the input connection and the transistor gate, and the transistor drain and the output connection, are

designed to have an impedance of 50 Ω, while the width of the 1 mm of transmission line closest to the input and output connection points, as well as the lines in the biasing networks, have varying widths due to them representing additional degrees of freedom in the optimization process.

Optimized for 300 mA The layout of the PA optimized for 300 mA is depicted in Figure 3.4.14.

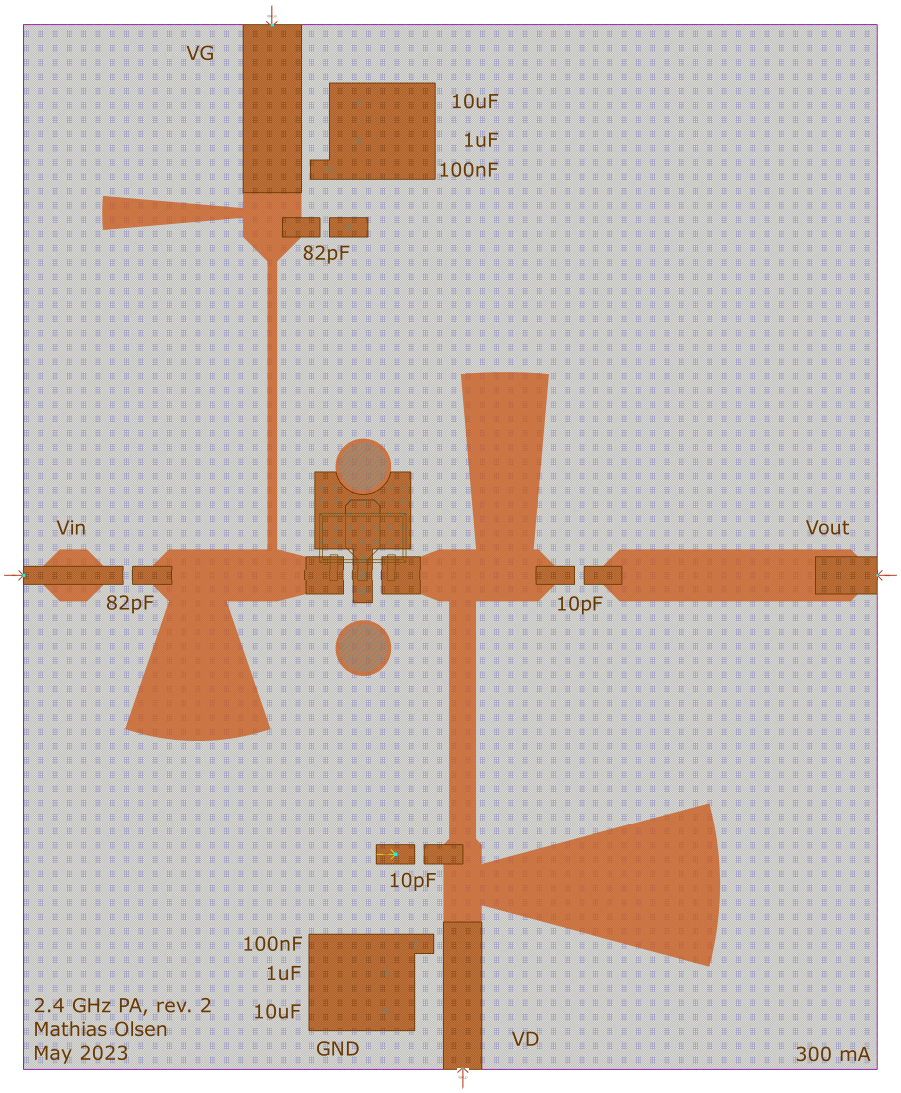


Figure 3.4.14: The PCB layout of the second revision PA, optimized for 300 mA.

The RF input is found on the left side of the layout, while the RF output is found on the right side. The gate bias voltage connection is placed at the top side and the drain bias voltage connection is placed at the bottom side. The transistor solder pads are placed in the middle, between the screw holes for the clamp keeping the transistor in place.

Optimized for 50 mA The layout of the PA optimized for 50 mA is depicted in Figure 3.4.15.

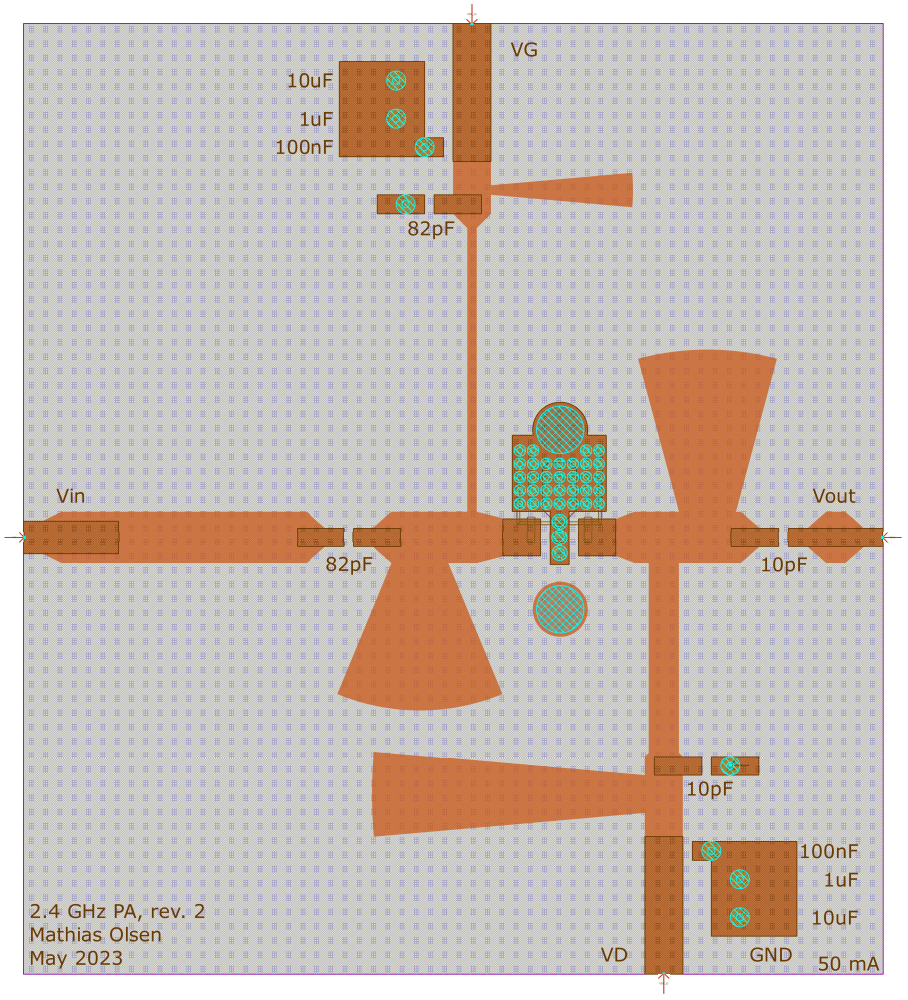


Figure 3.4.15: The PCB layout of the second revision PA optimized for 50 mA. The green circles are highlighting the drill holes. Such drill holes are present in all the layouts created in this thesis but this is the only one where they are highlighted in such a way.

Again, the RF input is found on the left side of the layout, and the RF output is on the right side. The gate bias voltage connection is at the top side and the drain bias voltage connection is at the bottom side, with transistor solder pads in the middle.

3.4.4 Physical Printed Circuit Board

Optimized for 300 mA A picture of the physical PCB is found in Figure 3.4.16.

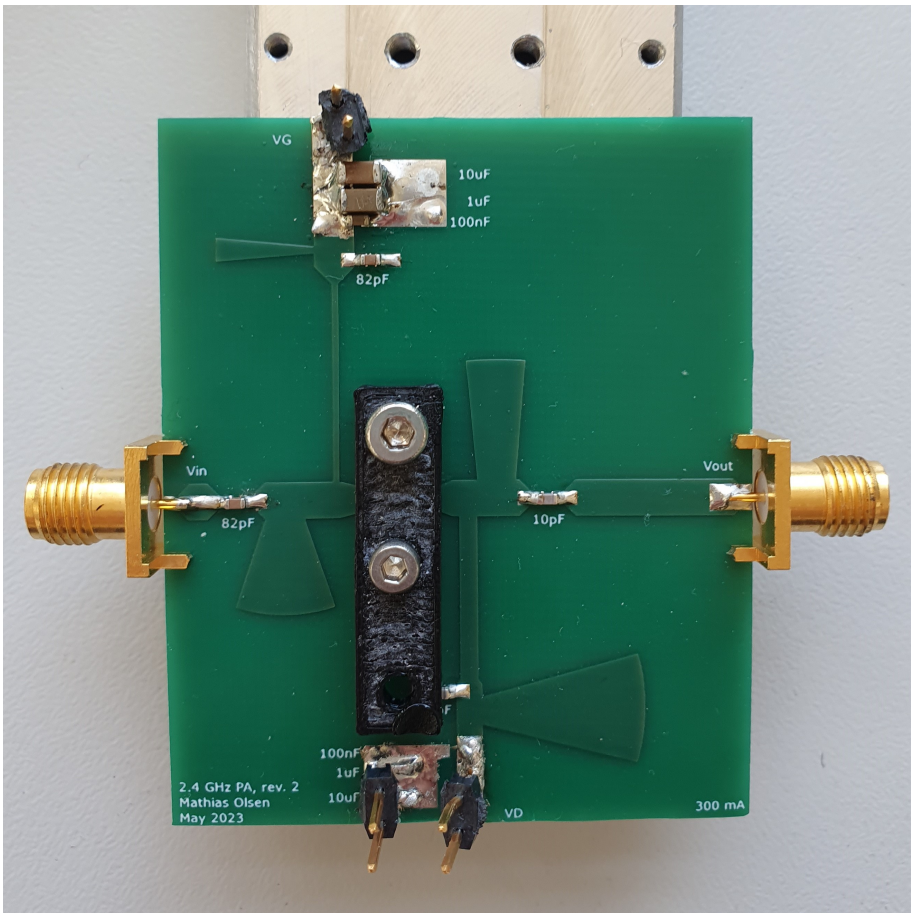


Figure 3.4.16: The final rev. 2, 300 mA PCB.

The transistor is hidden under the plastic clamp. The large capacitors in the drain bias network are not present anymore, because they were removed before performing drain modulation tests and the picture was taken after this. The PCB is firmly attached with screws to a cooling plate to prevent overheating.

Optimized for 50 mA A picture of the physical PCB is found in Figure 3.4.17.

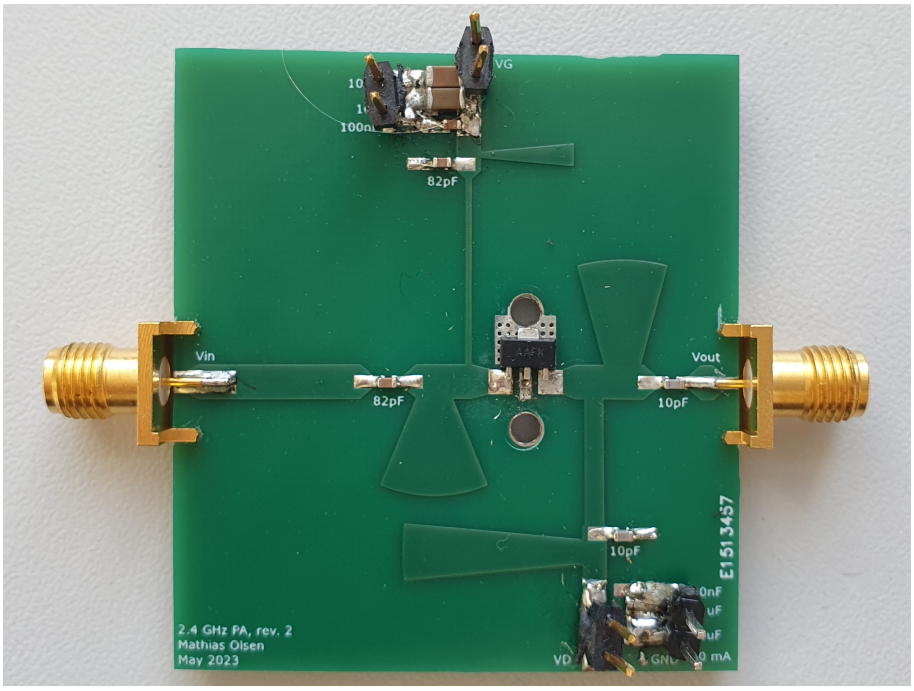


Figure 3.4.17: The final rev. 2, 50 mA PCB.

Here the transistor is visible, as the plastic clamp has been removed. In this case, as well, the large capacitors in the drain bias network are not present anymore, because they were removed before performing drain modulation tests and the picture was taken after this.

3.4.5 Measurements

S-Parameters The S-parameters were measured using an Aim TTi EL302RT power supply and a PicoVNA108 network analyzer, as shown in Figure 3.4.18.

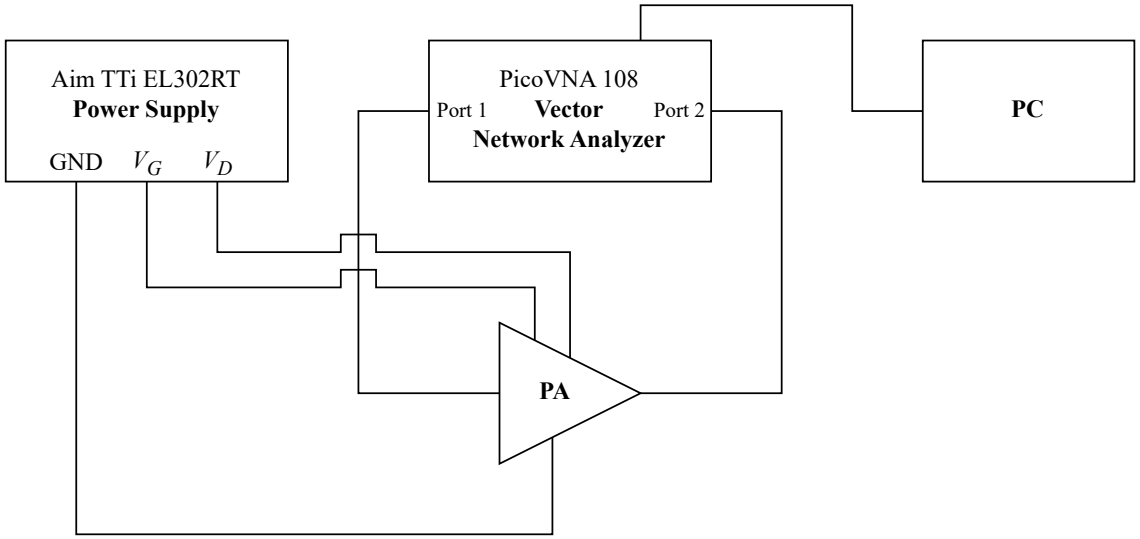


Figure 3.4.18: The setup for measuring the S-parameters of the rev. 2 PA.

When measuring the S-parameters attenuators were used at the output port of the PA to avoid too high output power. Three attenuators were used. Two with 3 dB dampening, and one with 6 dB dampening. Closest to the PA was the 3 dB attenuator with the highest power rating, then came the second 3 dB attenuator, and lastly the 6 dB attenuator. They were attached in this order to avoid any of them having to attenuate too much power.

Before performing the actual measurements, the PicoVNA had to be calibrated with a calibration kit belonging to it. This was done following an onboard calibration guide. The measurements were done by first setting the drain voltage to 8 V and setting the gate voltage to a value giving the desired drain current. The *touchstone* file for this state was saved, before lowering only the drain voltage by 1 V and saving the file for this state. This procedure was then repeated down to a drain voltage of 2 V. The gate voltage was kept the same for all the different drain voltages.

For the 300 mA version, the measurements were done for 300 and 150 mA. For the 50 mA version, they were done for 50 mA and 100 mA.

Figure 3.4.19 shows a picture of the actual setup.

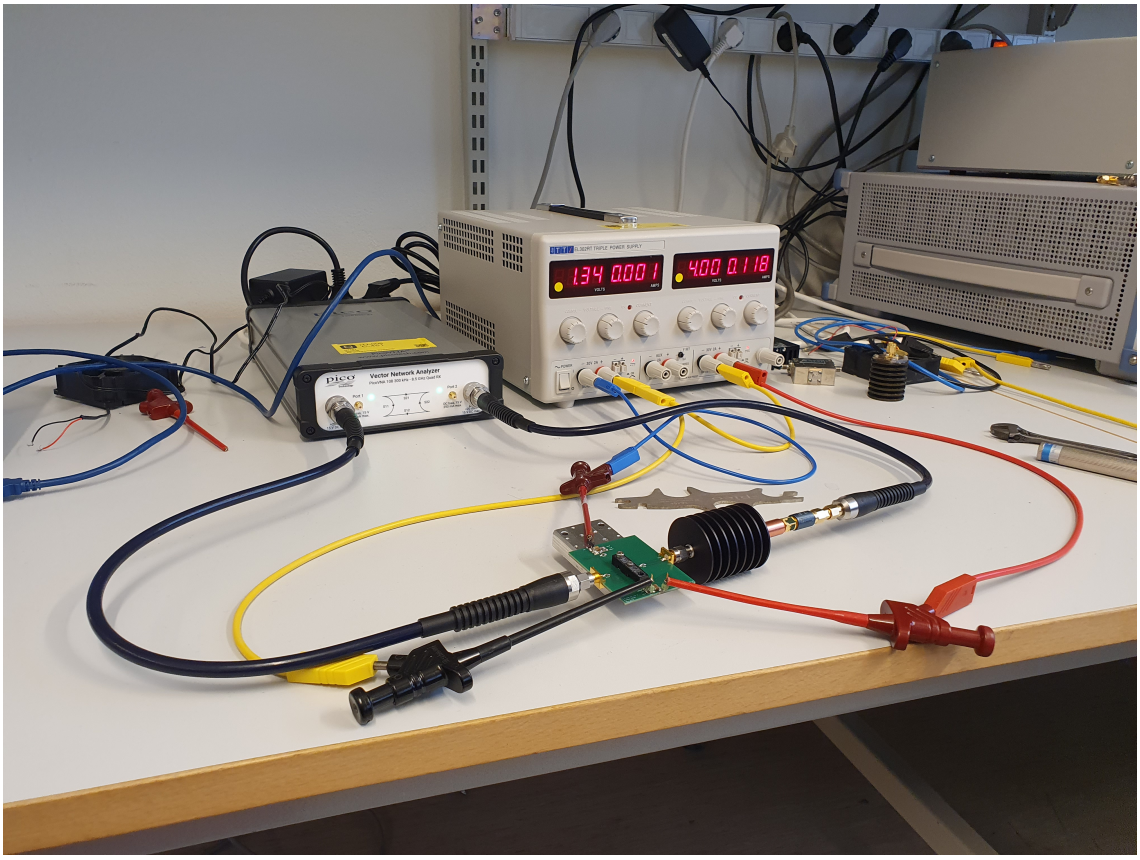


Figure 3.4.19: Picture of the setup for measuring the S-parameters of the rev. 2 PA. The equipment is connected to a laptop outside the picture through the blue USB cable coming from the PicoVNA.

Large-Signal The PA's large-signal behavior was measured using the setup illustrated in Figure 3.4.20. As will later be described in the results, the best gain was found at 2.3 GHz, so this ended up being the frequency used for the RF signal when performing the measurements.

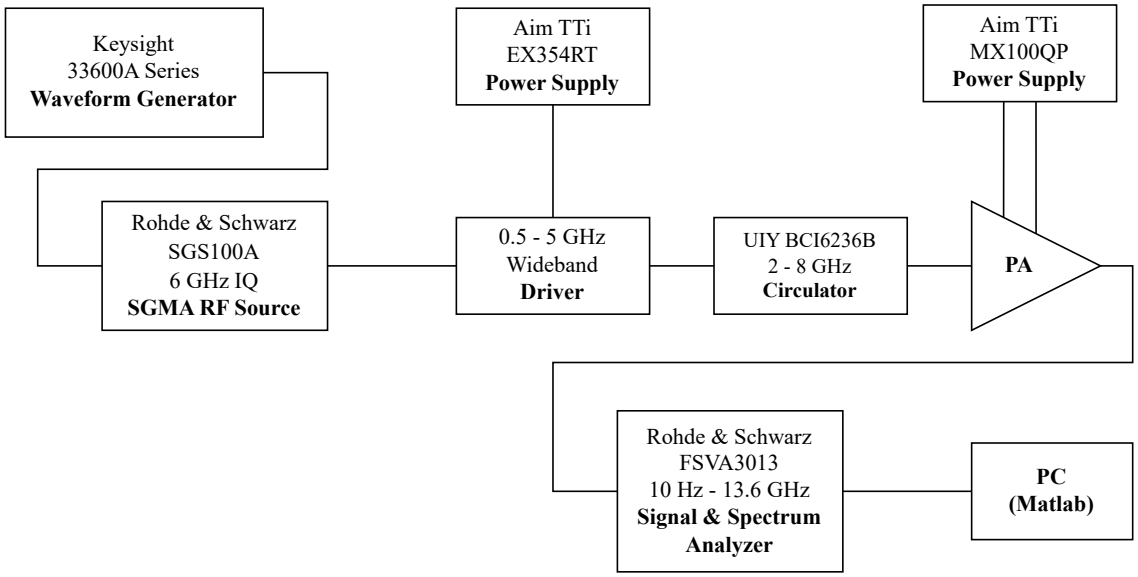


Figure 3.4.20: The setup for measuring the large-signal behavior of the rev. 2 PA.

The RF signal comes from the waveform generator through the SGMA RF source. Then the signal is passed on to the driver (wideband amplifier), where it is amplified to reach the desired input power at the PA input. The wideband driver is supplied by the EX354RT power supply. The purpose of the circulator is to isolate and remove reflections from the input of the PA back to the output of the driver.

The MX100QP power supplies both the gate and the drain bias voltages of the PA, from two of individual outputs. The output of the PA is connected to a signal & spectrum analyzer, through an attenuator and a coupler. The spectrum analyzer reads the output from the PA. This is then again connected to a PC, which is used to further analyze and perform calculations regarding the amplification process. The whole testing process is remotely controlled by the PC.

Before connecting the PA to the system, it was necessary to perform a calibration by finding the losses and gains in the different components between the RF source and the spectrum analyzer. This was done in a procedure where first the cable between the RF source and driver was measured by itself to find its internal loss. Then the driver and the circulator were connected and the gain of these two together was measured. The measured gains and losses used in the calibration are found in Table 3.4.16.

Table 3.4.16: Values used in the calibration of the tracking setup.

Component	**Gain**
Cable from RF source to driver	-2.78 dB
Driver and circulator	22 dB
Attenuator	-6 dB
Coupler	-20 dB
Cables between PA and analyzer	-1.34 dB
Total	**-8.12 dB**

A picture of the entire setup is found in Figure 3.4.21.

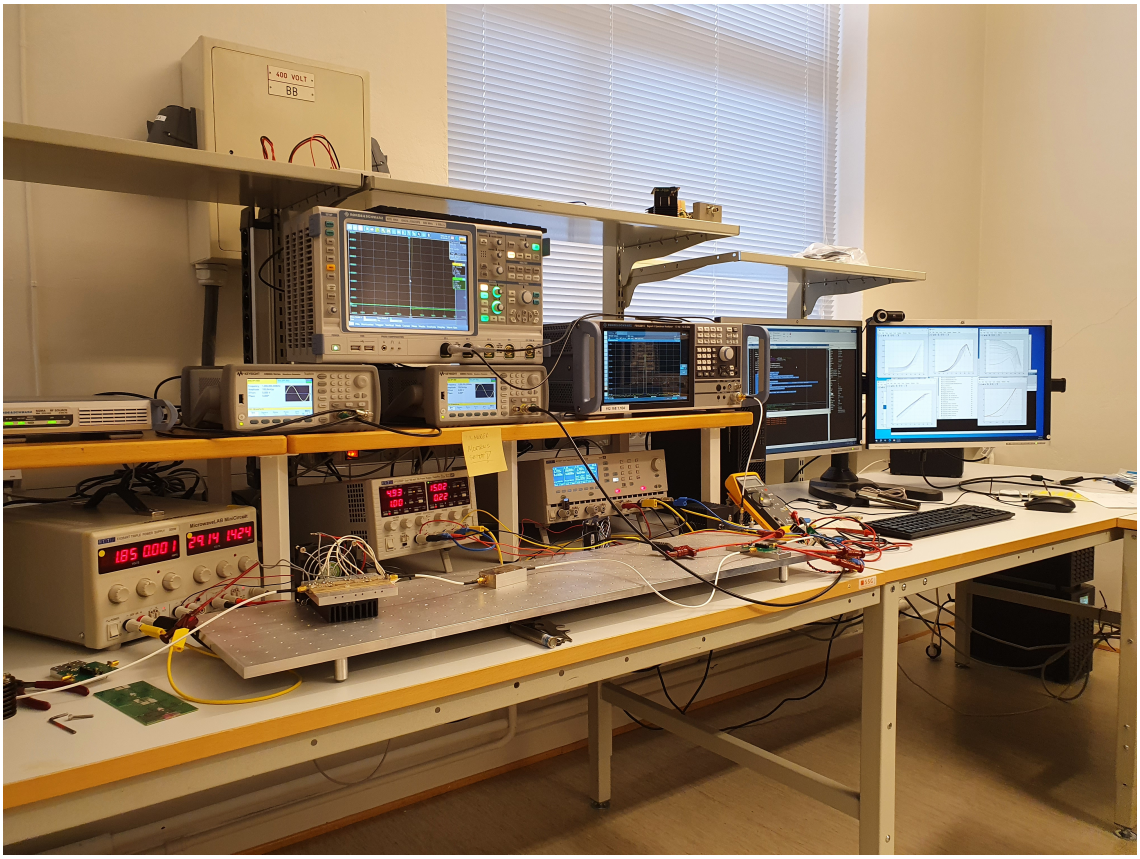


Figure 3.4.21: Picture of the setup for measuring the large-signal behavior of the rev. 2 PA.

The measurements were first performed for a fixed drain voltage value of 8 V, where the power of the input RF signal was swept, measuring gain, output power, PAE, and drain current, vs. input power. Then the procedure was repeated but in addition, the drain voltage was stepped down after each sweep of the input power, to provide the same curves for different levels of drain voltage. This was done for drain bias voltages from 8 down to 2.5 V for the 300 mA version, and from 8 down to 3 V for the 50 mA version, using 0.5 V steps for both of them.

3.5 Power Amplifier, vol. 3, Dual-Band

The third revision of the PA will be a dual-band amplifier, where in addition to the amplification of 2.4 GHz signals, it should be able to amplify signals in the Unlicensed National Information Infrastructure band number 1 (U-NII-1). The frequency range of this band is 5.150 GHz - 5.250 GHz. Thus, the center frequency of the PA's second amplification band will be 5.200 GHz, [20].

Again, the previous revision PA was used as a starting point. Then, a second stub was added to the input and output matching to increase the degrees of freedom. An attempt of just adding goals for 5.2 GHz and re-optimizing the vol. 2 PA was done but it seemed to work better with a second stub in the matching networks. Using a fixed length between the two stubs is a known method for matching one frequency with a shorter transmission line than what is the case with the single stub but the idea here was to provide a better possibility of matching two frequencies, [9].

As it was discovered for revision 2 that it also had significant amplification for frequencies in the lower spectrum, this was worked on for the dual-band PA. Because this may lead to oscillations, due to possible resonance that can occur in the cable loop between the output and the input. One basic action that was taken was to decrease the capacitance of the RF capacitors in the networks on both the input and output.

To be able to have a greater impact on the PA's performance in a greater part of the frequency band, S-parameter optimization was also performed as part of the design process. This was done by setting goals for S_{21}, S_{11}, and S_{22}, in the frequency regions of interest, 2.4 GHz $\pm$ 10 MHz and 5.2 GHz $\pm$ 10 MHz. In addition to this goals were set to suppress S_{21} in the frequency region below 1 GHz. Both by setting a maximum goal for S_{21} and minimum goals for S_{11} and S_{22}. To minimize the simulation times, a sweep plan was used to sweep only the frequencies from 100 MHz to 1.2 GHz, from 2.3 to 2.5 GHz, and from 5.1 to 5.3 GHz.

Regarding the large-signal simulations, one change from the work on PA vol. 2 was that it was necessary to sweep for several frequencies. To sweep only 2.4 GHz and 5.2 GHz, the sweep plan contained these two frequencies as start and stop frequencies and the difference between them as step size. When including a lower frequency, e.g., 900 MHz, to suppress the gain here, the lower frequency was set as the starting point, 5.2 GHz was set as the stopping point, and then the step size was set to hit 2.4 GHz at one of the steps. The goals were set as described in the method section of PA vol.2 but they were specified for each frequency. The goals earlier used were set for 2.4 and 5.2 GHz, while goals for maximum gain and output power were set for the lower frequency. These maximum goals, suppressing the lower frequency, were weighted lower than the gain and output power goals for 2.4 and 5.2 GHz, as the goals for these two frequencies still were the main focuses.

3.5.1 Schematic

The input bias network, in Figure 3.5.1, followed the same principles as for the rev. 2 PA but was re-optimized and the line leading from the stub to the input matching network was created with the intention of being a quarter-wavelength transformer for the 5.2 GHz rather than the 2.4 GHz, as it ended up being a greater challenge optimizing for 5.2 than 2.4 GHz.

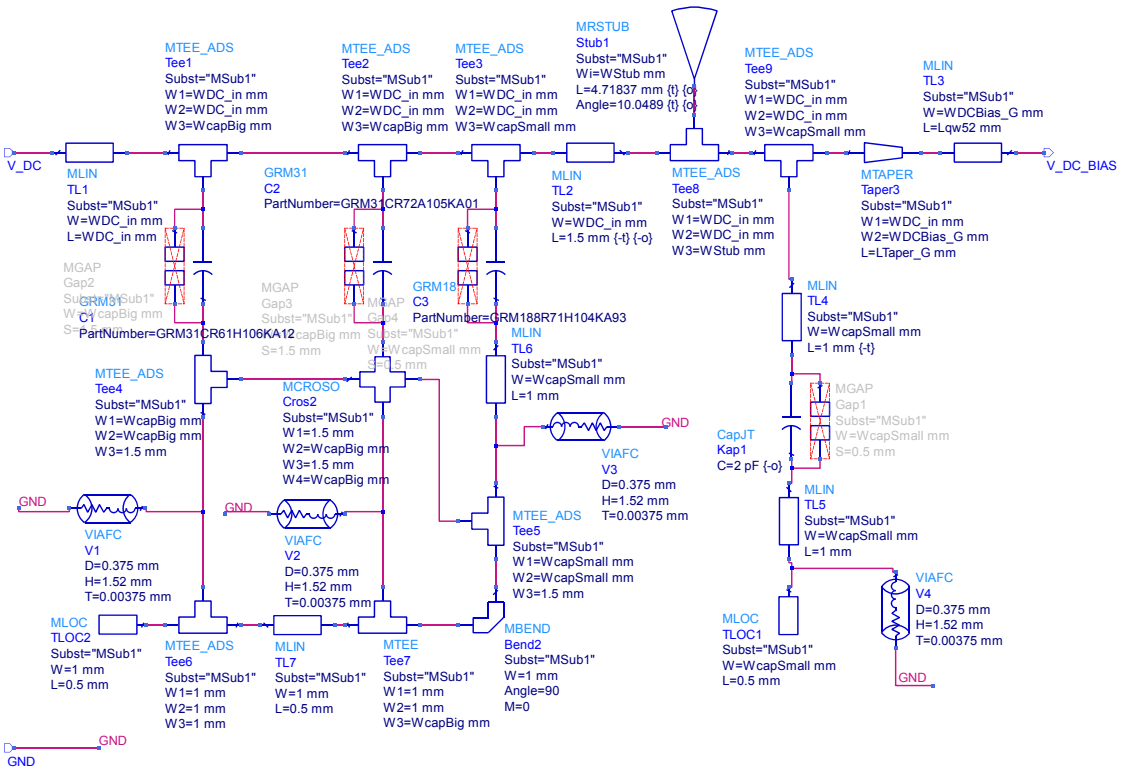


Figure 3.5.1: The bias network for the input of the third revision PA. The length from the bottom of $Stub_1$ to TL_3, consisting of W_3 of Tee_9 and L of $Taper_3$, add up to 3.75 mm.

The values of the most important variables are included in Table 3.5.1.

Table 3.5.1: Values for components used in the input bias network of the dual-band PA.

(a) Capacitance and manufacturer of capacitor.

Variable name	Value	Manuf.
C	2 pF	Johanson

(b) Length, width, and angle of transmission lines and stub.

Device name	Length	Width	Angle
$Stub_1$	4.72 mm	2.39 mm	10.0°
TL_3	8.82 mm	0.50 mm	N/A

In the output bias network, the line designed to be a 5.2 GHz quarter-wavelength in the input bias network was allowed to be optimized for a broader range of values.

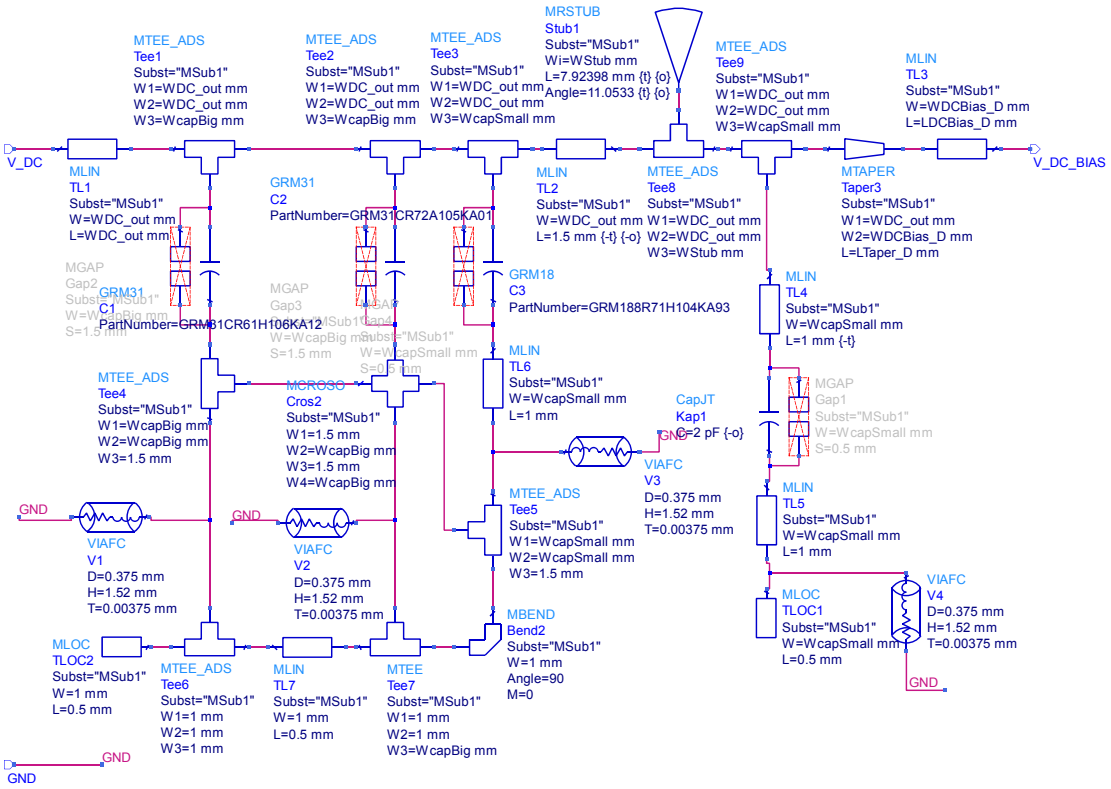


Figure 3.5.2: The bias network for the output of the third revision PA. The length from the bottom of $Stub_1$ to TL_3, consisting of W_3 of Tee_9 and L of $Taper_3$, add up to 3.57 mm.

The values of the most important variables are included in Table 3.5.2.

Table 3.5.2: Values for components used in the output bias network of the dual-band PA.

(a) Capacitance and manufacturer of capacitor.

Variable name	Value	Manuf.
C	2 pF	Johanson

(b) Length, width, and angle of transmission lines and stub.

Device name	Length	Width	Angle
$Stub_1$	11.05 mm	3.00 mm	11.1°
TL_3	8.82 mm	18.00 mm	N/A

The input matching network now includes two stubs, instead of only one in the previous revisions. Both the stub lengths, angles, connection point widths, and distance between, were allowed to be optimized by the optimization tool.

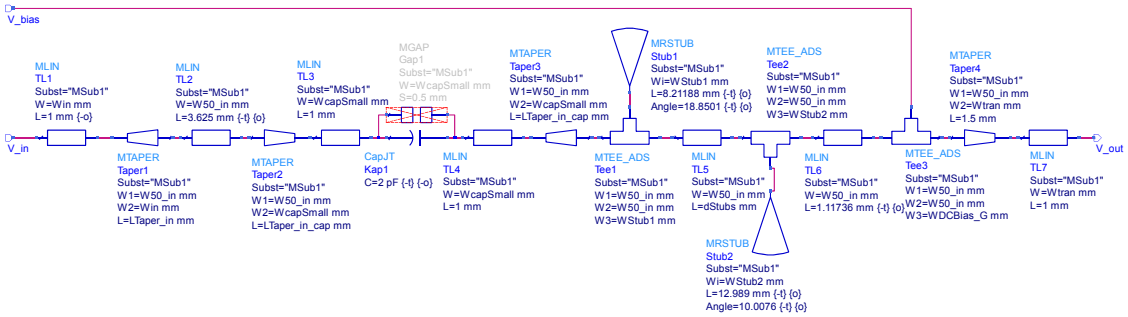


Figure 3.5.3: The input matching network of the dual-band PA.

The most important parameter values are summarized in Table 3.5.3.

Table 3.5.3: Values for components used in the input matching network of the second version of the PA.

(a) Capacitance and manufacturer of capacitor.

Variable name	**Value**	**Manuf.**
C	2 pF	Johanson

(b) Length, width, and angle of transmission lines and stub.

Device name	**Length**	**Width**	**Angle**
$Stub_1$	8.21 mm	3.00 mm	18.9°
TL_5	7.01 mm	2.70 mm	N/A
$Stub_2$	12.99 mm	1.27 mm	10.01°
TL_6	1.12 mm	2.70 mm	N/A

The output matching also had the same stub configuration as the input matching network. In addition to this a transmission line intended to work as a quarter-wave transformer, blocking the second harmonic of 5.2 GHz, was added between the transistor connection point and the bias network connection point.

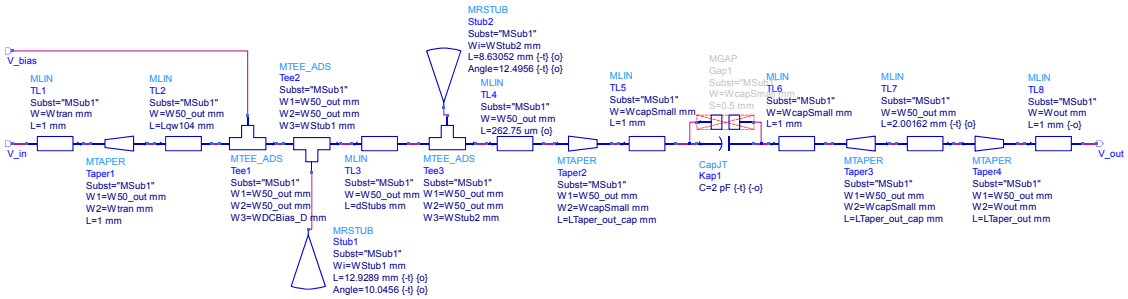


Figure 3.5.4: The output matching network of the dual-band PA.

The values of the most essential parameters are found in Table 3.5.4.

Table 3.5.4: Values for components used in the output matching network of the second version of the PA.

(a) Capacitance and manufacturer of capacitor.

Variable name	Value	Manuf.
C	2 pF	Johanson

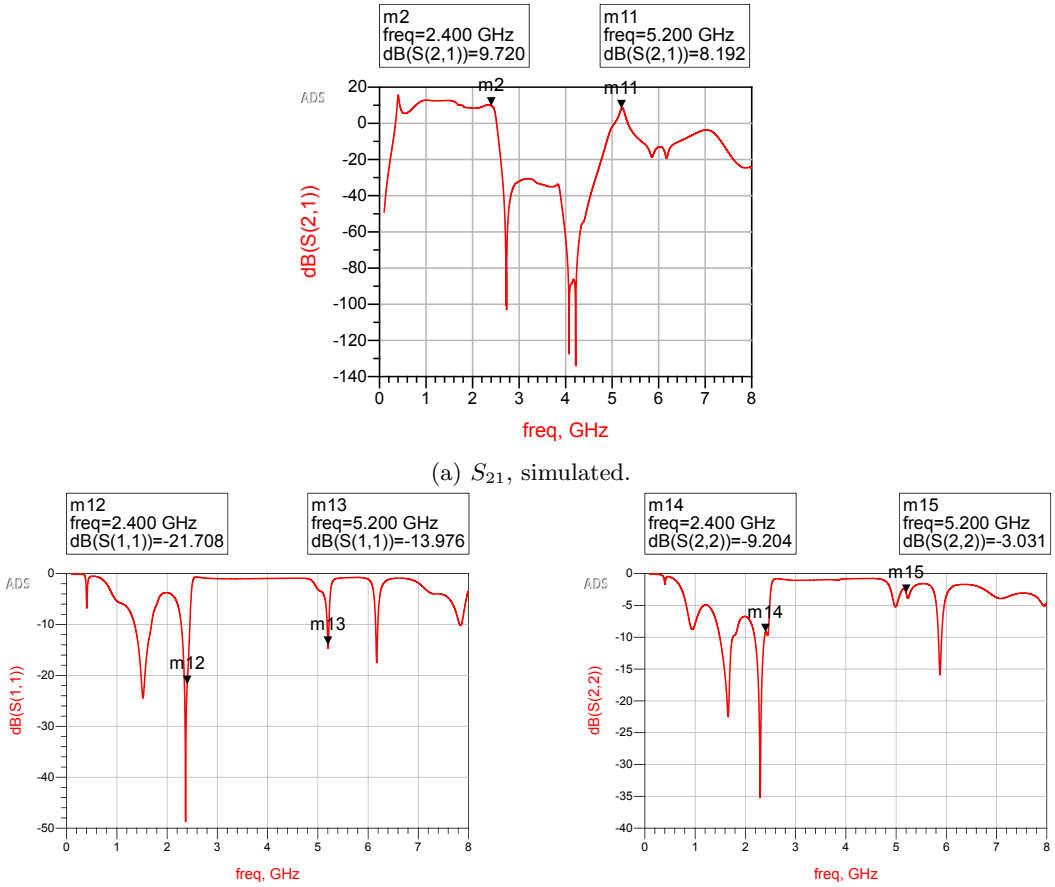
(b) Length, width, and angle of transmission lines and stub.

Device name	Length	Width	Angle
TL_2	1.00 mm	2.90 mm	N/A
$Stub_1$	12.93 mm	0.90 mm	10.0°
TL_3	8.21 mm	2.90 mm	N/A
$Stub_2$	8.63 mm	2.49 mm	12.5°
TL_4	263 μm	2.90 mm	N/A

3.5.2 Simulations

A challenge when working on the dual-band PA was that an optimization of the S-parameters led to lower large-signal performance, especially regarding gain in the higher output power. Thus, optimization back and forth was necessary. The last round of optimization was done with the large-signal simulator to make sure the PA was able to deliver gain at higher output powers as well.

S-Parameters Simulations of S_{21}, S_{11} and S_{22} of the final design are found in Figure 3.5.5 and summarized in Table 3.5.5.



(a) S_{21}, simulated.

(b) S_{11}, simulated.

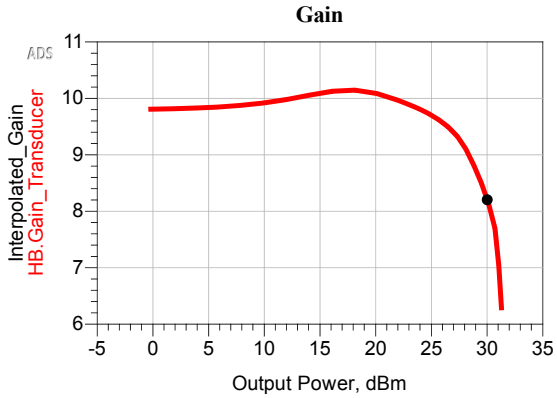
(c) S_{22}, simulated.

Figure 3.5.5: Simulated S-parameters of the dual-band PA.

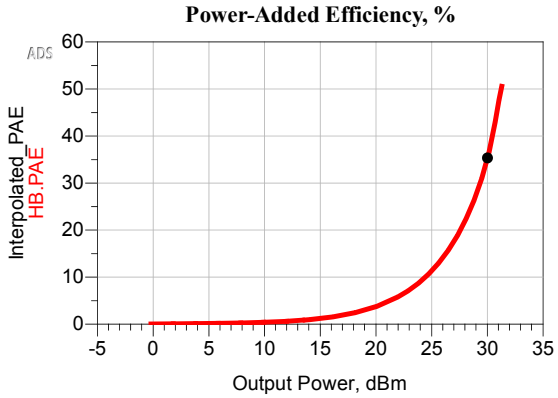
Table 3.5.5: Summary of simulated and measured S-parameters for the dual-band PA.

S-param.	**Sim., 2.4 GHz**	**Sim., 5.2 GHz**
S_{21}	9.72 dB	8.19 dB
S_{11}	-21.7 dB	-14.0 dB
S_{22}	-9.20 dB	-3.03 dB

Large-Signal The large-signal simulation results at 2.4 GHz are found in Figure 3.5.6.



(a) Simulated gain vs. output power.



(b) Simulated PAE vs. output power.

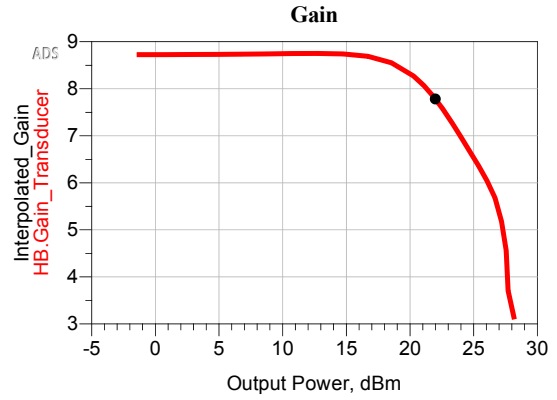
Figure 3.5.6: Large-signal simulation results at 2.4 GHz.

The small-signal gain is close to 10 dB but compresses earlier than what was the case for the rev. 2 PA. The results at 30 dBm output power are summarized in Table 3.5.6.

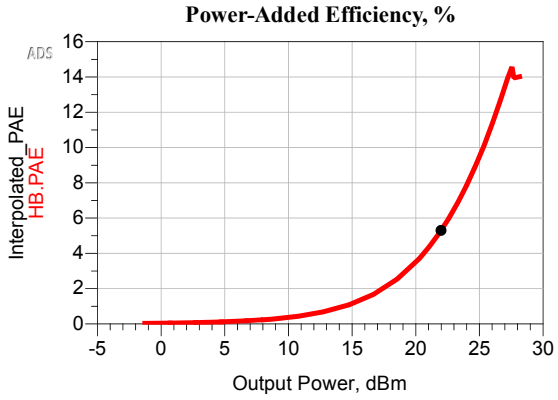
Table 3.5.6: Simulation results of the dual-band PA at 2.4 GHz.

P_{out}	G_T	**Gain Comp.**	**PAE**	$\mathbf{V_D}$	$\mathbf{I_D}$
30.01 dBm	8.21 dB	1.94 dB	35.34 %	8 V	300 mA

The large-signal simulation results at 5.2 GHz are found in Figure 3.5.7.



(a) Simulated gain vs. output power.



(b) Simulated PAE vs. output power.

Figure 3.5.7: Large-signal simulation results at 5.2 GHz.

As we can see, the PA is not able to deliver 30 dBm output power but it has a small-signal gain of almost 9 dB at 5.2 GHz. The results at 22 dBm output power are summarized in Table 3.5.7.

Table 3.5.7: Simulation results of the dual-band PA at 5.2 GHz.

P_{out}	G_T	**Gain Comp.**	**PAE**	$\mathbf{V_D}$	$\mathbf{I_D}$
21.98 dBm	7.78 dB	0.967 dB	5.30 %	8 V	300 mA

3.5.3 Layout

The final layout of the dual-band PA is found in Figure 3.5.8.

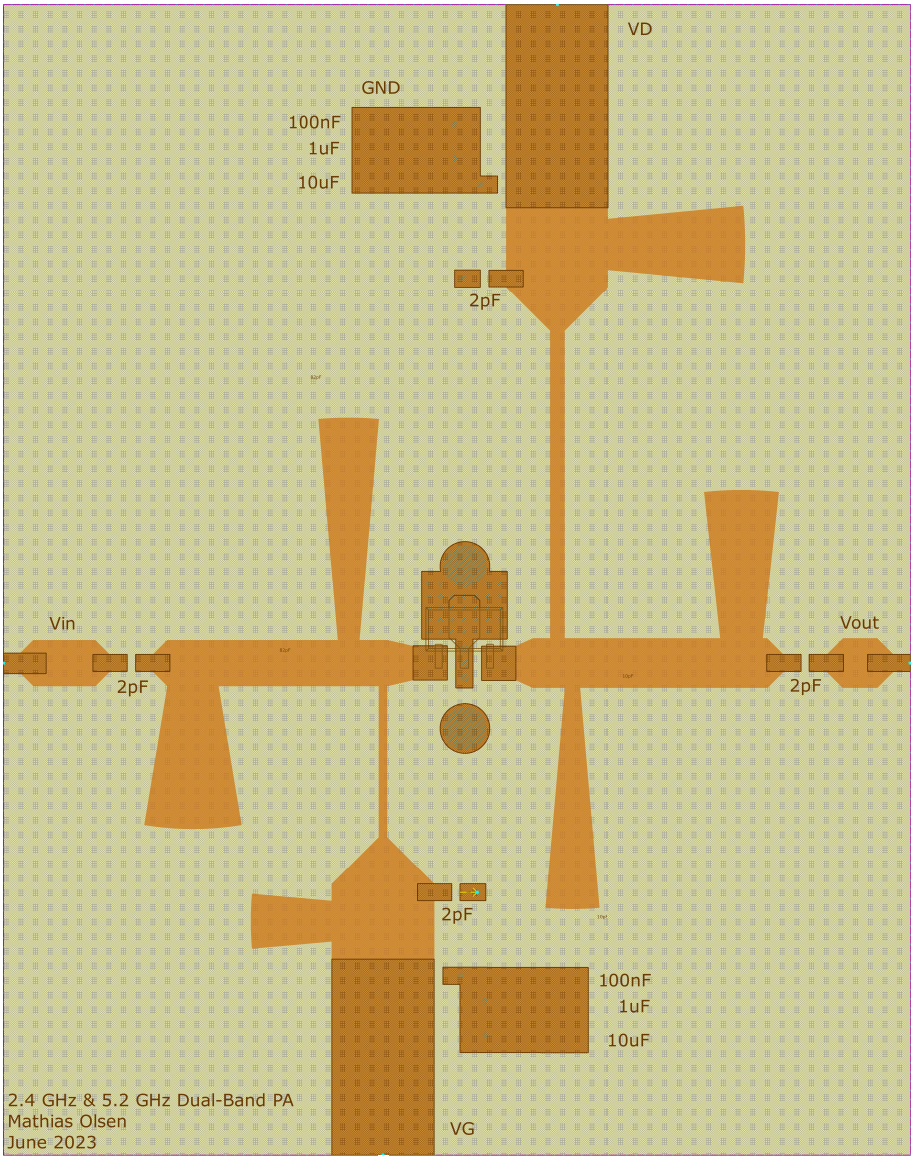


Figure 3.5.8: The PCB layout of the third revision PA.

The RF input is placed to the left, the RF output to the right, the gate bias voltage at the bottom, and the drain bias voltage at the top.

3.5.4 Physical Printed Circuit Board

A picture of the physical PCB is found in Figure 3.5.9.

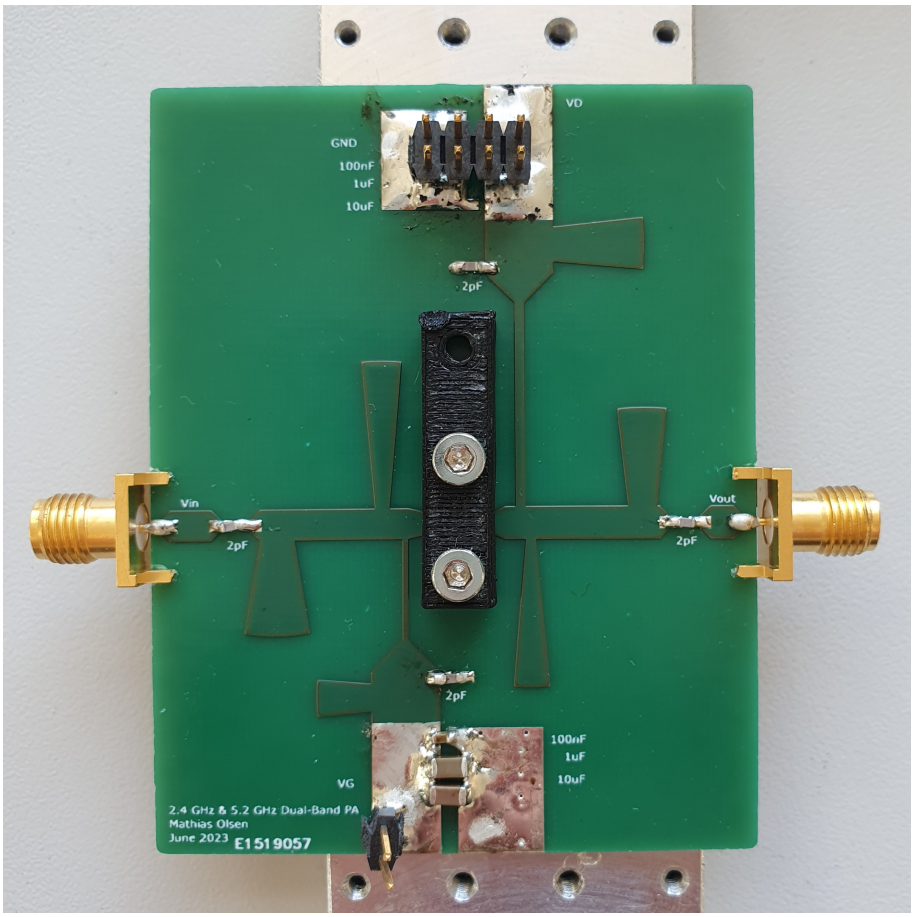


Figure 3.5.9: The final dual-band PCB.

As for the pictures of the rev. 2 PCB, the transistor is hidden under the plastic clamp and the large capacitors in the drain bias network are not present anymore, because they were removed before performing drain modulation tests. The PCB is attached to a cooling plate to prevent overheating. When delivered from production, the PCB came without copper or solder as the bottom layer. This led to copper tape being attached on the backside to connect the grounded areas of the layout and provide a ground layer for the transmission lines.

3.5.5 Measurements

S-Parameters The S-parameters were measured using the same setup as for the second revision of the PA, illustrated in Figure 3.4.18.

Large-Signal The large-signal behavior was measured using the same setup as for the second revision of the PA, illustrated in Figure 3.4.20. The difference in the procedure this time was that

the behavior had to be done twice, as there were two different frequencies to do measurements at. Thus, the calibrating had to be redone for 5.15 GHz after the 2.3 GHz measurements were finished. Increasing the frequency led to an increase in losses in the cables and a decrease in gain in the driver and the circulator.

3.6 Drain Modulation

3.6.1 Setup

Figure 3.6.1 shows the setup used when performing the drain modulation tests of the PA.

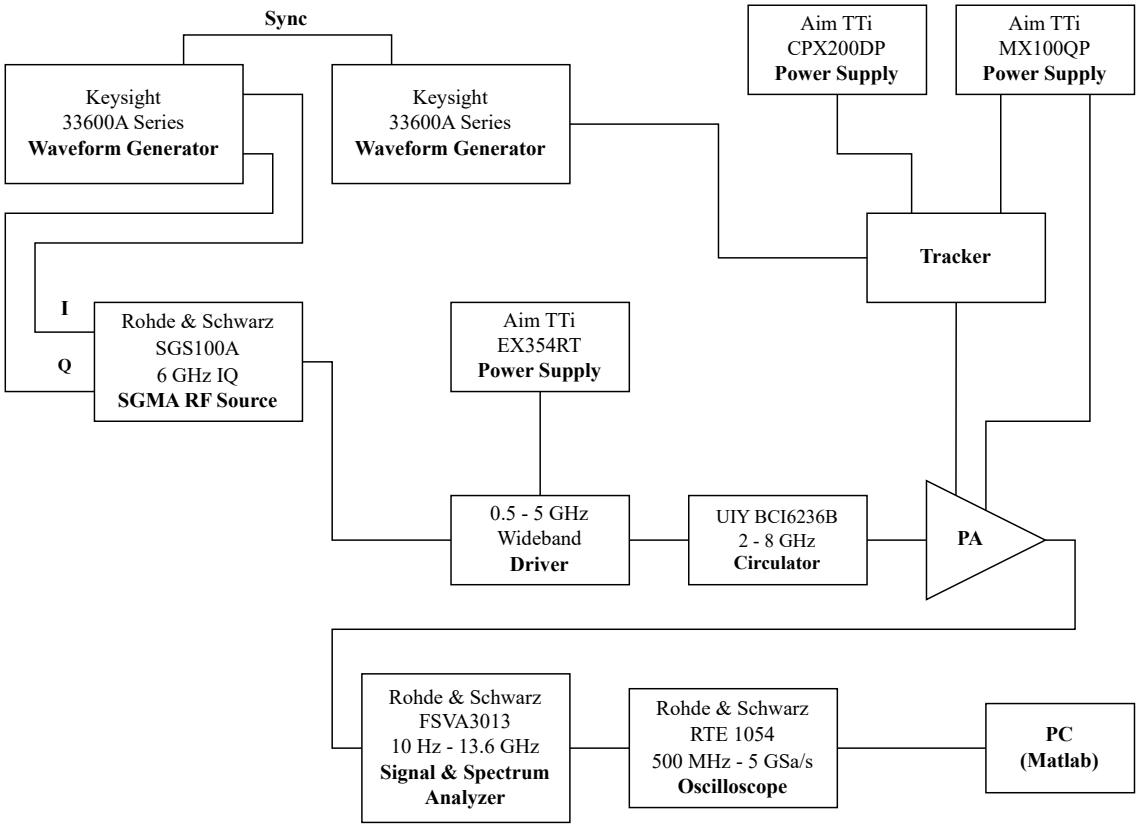


Figure 3.6.1: The setup for performing drain modulation tests.

Two waveform generators in sync are used, where the one to the left generates the waveforms that will be the QAM signal. The signal is sent through an I- and a Q-channel to the SGMA RF source, where they are modulated onto a carrier wave together as a QAM signal. The signal is then passed on to the driver (wideband amplifier), where it is amplified to reach the desired input power at the PA input. The wideband driver is supplied by the EX354RT power supply. The purpose of the circulator is to isolate and remove reflections from the input of the PA back to the output of the driver.

The waveform generator to the right generates the "modulated DC" tracking signal for the tracker. The tracker is built around an LT1210 current feedback amplifier and uses an additional op-amp

as the voltage amplifier. It has -5 V and +15 V supplied from the CPX200DP power supply and +32 V supplied from the MX100QP power supply. The MX100QP power supply also supplies the gate bias voltage of the PA.

The output of the PA is connected to a signal & spectrum analyzer, through an attenuator and a coupler. The spectrum analyzer reads the output from the PA. This is then again connected to a PC, which is used to further analyze and perform calculations regarding the amplification process. The oscilloscope connected between the spectrum analyzer and the PC is a part of the physical setup but is not used in this configuration.

The whole testing process is remotely controlled by the PC.

Except for the inclusion of the tracker, a picture of the setup was seen in 3.4.21.

3.6.2 Measurements

The measurements were performed by running either simulations with static drain voltage or with the tracking functions created from the measurements done earlier. PA revisions 2 and 3 were the ones that were measured with the tracker. Modulated signals were amplified by the PA and either plotted or numeric results were provided for linearity, gain and efficiency.

4 Results

This section will cover the results of the measurements performed on the different revisions of the PA. Each revision will have its own subsection, which covers both small- and large-signal behavior. For revisions 2 and 3, this also includes results of drain modulation when transmitting a modulated signal. The goal is still to be able to deliver a peak output power of 30 dBm with a gain of 10 dBm, and PAE as high as possible.

Both versions of the second revision PA, and the revision when operating in its lower frequency band, achieve the output power target. Regarding gain, the same three cases deliver gain of 10 dB or higher, while only the 300 mA version does at 30 dBm output power. When applying different drain modulation techniques, PAEs in the span between 10.95 % and 41.87 % are shown, varying between the different PAs. In the higher frequency band of the third revision, the gain is measured to be only 1 dB. Thus, effectively eliminating the PA's usefulness in this frequency band.

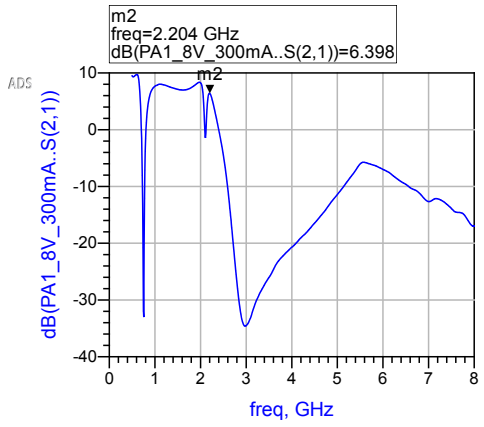
When "gain" is written in this section, it can be interpreted as available power gain, G_A, defined in (2.5.5). However, the load used in the measurements is known to be 50 Ω, which also makes $G_A = G_T$.

4.1 Power Amplifier, vol. 1

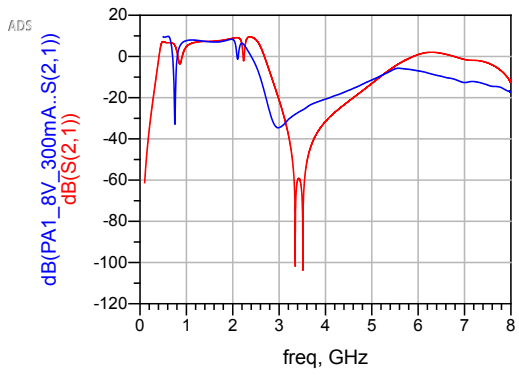
4.1.1 S-parameters

There are four different S-parameters that usually are measured in a two-port network. However, due to attenuators on the output of the PA, the measurements of S_{12} will be highly affected by noise and therefore not included in the plots for any of the PAs.

The measured small-signal gain, S_{21}, for the first PA, is found in Figure 4.1.1a and compared with the simulated S_{21} in Figure 4.1.1b.



(a) S_{21}, measured.

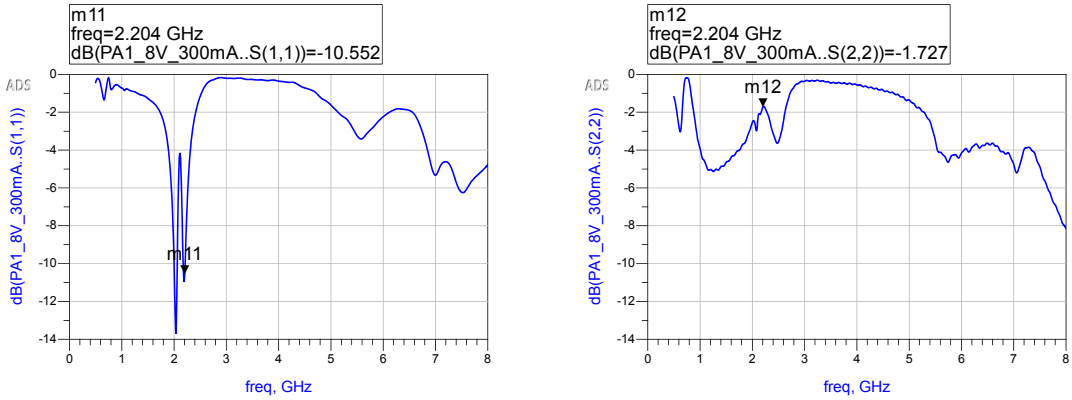


(b) S_{21}, simulated (red) and measured (blue).

Figure 4.1.1: S_{21} of the first revision of the PA, with a marker at 2.2 GHz in the measured only plot.

The peak of S_{21}, earlier found at 2.4 GHz, has now shifted down to 2.2 GHz, in addition to having decreased in value. As a result, S_{21} at the end of the relatively flat region between 1 and 2 GHz

now is greater than at 2.2 GHz as well. The measured input reflection, S_{11}, and output reflection, S_{22}, are found in Figure 4.1.2.



(a) S_{11}, measured.

(b) S_{22}, measured.

Figure 4.1.2: S_{11} and S_{22} of the first revision of the PA, with markers at 2.2 GHz.

Both S_{11} and S_{22} have increased in value. S_{11} is still below -10 dB, while S_{22} is now above -2 dB. In Table 4.1.1 the simulated and measured S-parameter values of interest are summarized. Measured values at 2.0 GHz are also included, due to the measured small-signal gain being higher here than at 2.2 GHz.

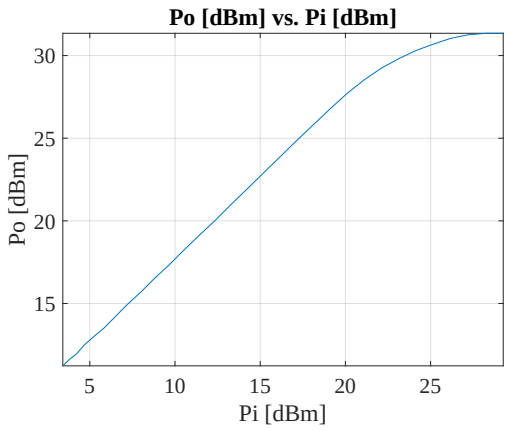
Table 4.1.1: Summary of simulated and measured S-parameters for the rev. 1 PA.

S-param.	**Sim., 2.4 GHz**	**Meas., 2.2 GHz**	**Meas., 2.0 GHz**
S_{21}	9.42 dB	6.40 dB	8.24 dB
S_{11}	-14.22 dB	-10.6 dB	-10.5 dB
S_{22}	-5.79 dB	-1.73 dB	-2.51 dB

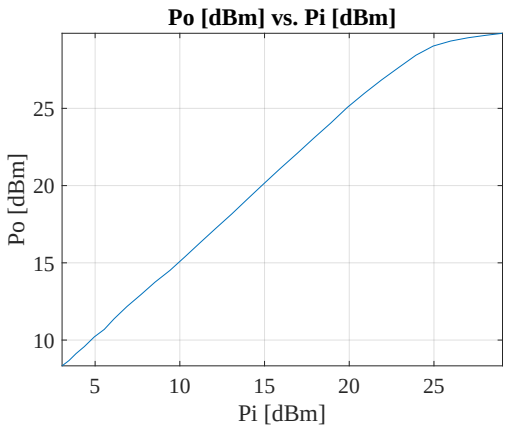
4.1.2 Large-Signal

The PA has to satisfy several performance metrics. One of these is the ability of providing an output power greater than 30 dBm at the desired central frequency. As seen from the S-parameter measurements, the PA had the highest gain at frequencies 2.0 GHz and 2.2 GHz instead of the desired frequency of 2.4 GHz. Reasons for this can be inaccuracy in the provided transistor model, as well as incorrect values used for the substrate in simulations compared to the properties of the real substrate. Because of this we will be looking at the PA's performance at 2.0 and 2.2 GHz, instead of 2.4 GHz, in this paragraph.

Figures 4.1.3a and 4.1.3b show the development of the output power vs. the input power at the above-mentioned frequencies 2.0 and 2.2 GHz.



(a) Output power as a function of input power at 2.0 GHz.

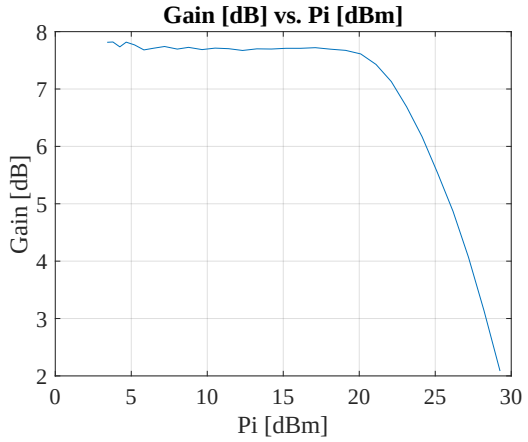


(b) Output power as a function of input power at 2.2 GHz.

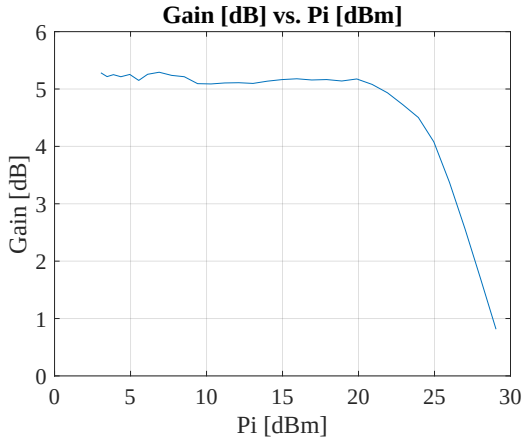
Figure 4.1.3: Output power as a function of input power for the two frequencies where the PA has its best performance.

At 2.0 GHz the PA satisfies the demand of being able to provide an output power above 30 dBm, as can be seen in Figure 4.1.3a. This is not the case at 2.2 GHz, where the output power saturates and tops out right below 30 dBm. The positive to take from this result is the fact that we now have evidence of the MACOM XF1001-SC transistor being able to provide an output signal above the 30 dBm level.

The PA should as well be able to provide a certain gain over a range of input power. Figure 4.1.4 shows the gain as a function of input power.



(a) Gain as a function of input power at 2.0 GHz.

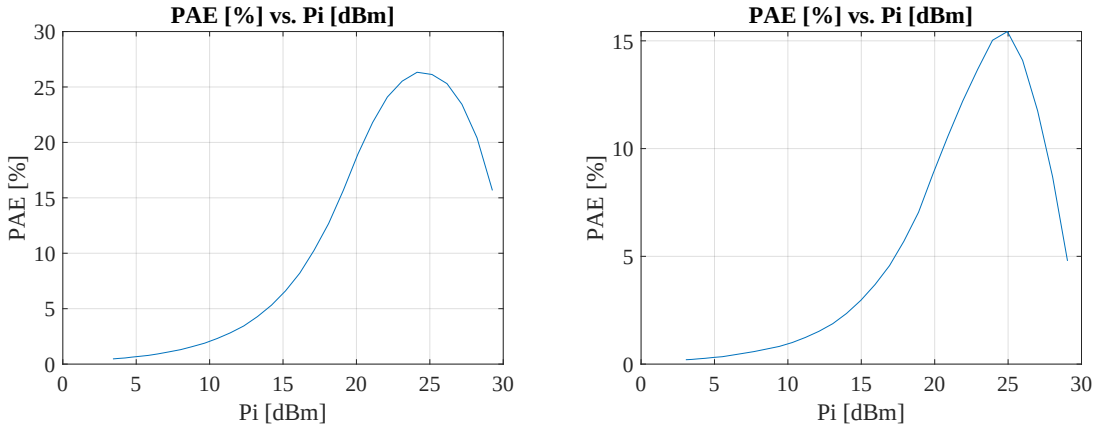


(b) Gain as a function of input power at 2.2 GHz.

Figure 4.1.4: Gain as a function of input power for the two frequencies where the PA is matched the best.

With the frequency set to 2.0 GHz the small-signal gain stays right below 8 dB up until approx. 20 dBm input power, where it begins to enter compression. At 2.2 GHz it stays right above 5 dB

before it again starts to compress around 20 dBm input power.



(a) PAE as a function of input power at 2.0 GHz. (b) PAE as a function of input power at 2.2 GHz.

Figure 4.1.5: PAE as a function of input power for the two frequencies where the PA is matched the best.

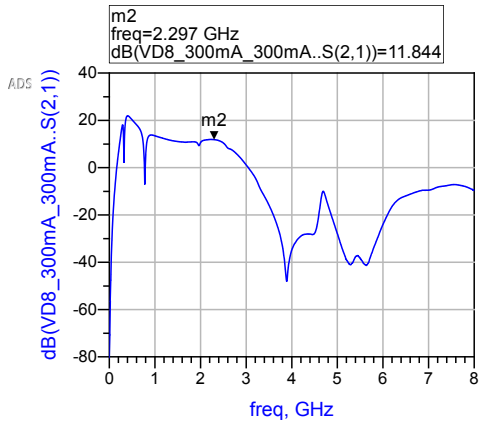
The maximum PAE reached when operating at 2.0 GHz is a little bit above 25 %, while at 2.2 GHz it peaks at about 15 %.

4.2 Power Amplifier, vol. 2

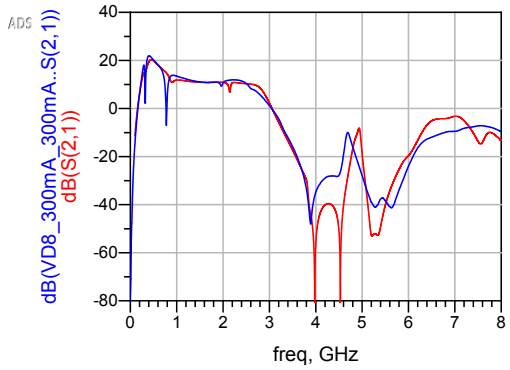
For the second revision of the PA, two separate designs were created. One optimized for a drain current of 300 mA and on optimized for a drain current of 50 mA. Therefore, each subsection is here divided into two paragraphs. One for each design. Different from the first revision PA, this second revision was also tested with power sweeps with stepped drain voltages, modulated signals, and drain modulation as well.

4.2.1 S-Parameters

300 mA Design The S-parameters for the 300 mA drain current design will be presented first. The measured small-signal gain vs. frequency, S_{21}, both alone and compared to the simulated one, is found in Figure 4.2.1.



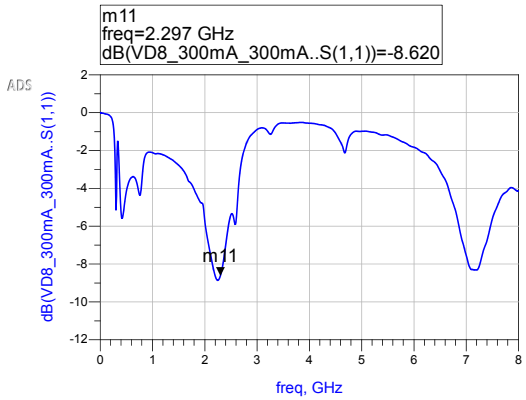
(a) S_{21}, measured.



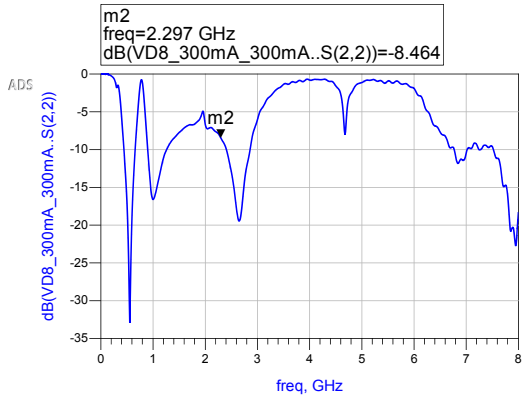
(b) S_{21}, simulated (red) and measured (blue).

Figure 4.2.1: S_{21} of the 300 mA version.

The peak of S_{21} in the frequency region of interest has again shifted a bit down in frequency. This time to about 2.3 GHz. The value of it has increased from 10.5 dB to 11.8 dB. The measured S_{11} and S_{22} are found in Figure 4.2.2.



(a) S_{11}, measured.



(b) S_{22}, measured.

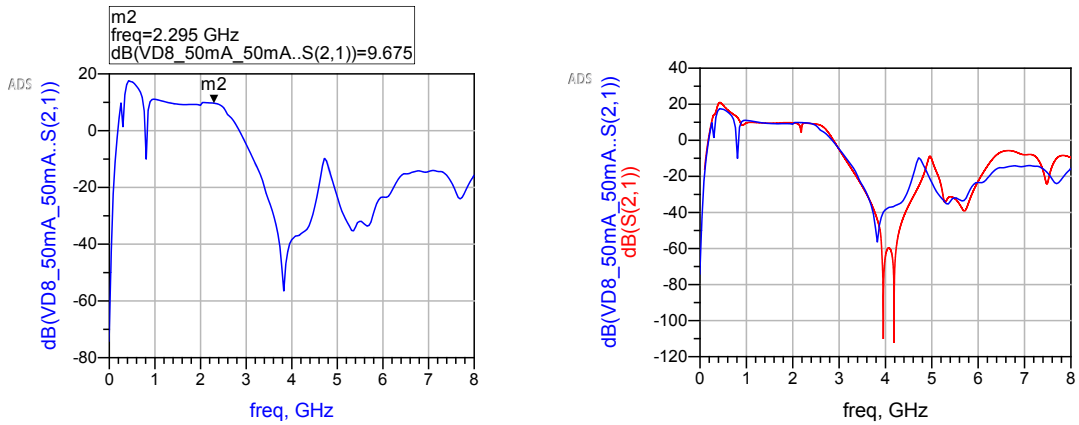
Figure 4.2.2: S_{11} and S_{22} of the 300 mA version.

When comparing these values to the simulated ones, the reflection has increased on both the input and the output. Even though S_{21} had increased. A summary of the values, both simulated and measured, is found in Table 4.2.1.

Table 4.2.1: Summary of simulated and measured S-parameters for the rev. 2 PA designed for 300 mA drain current.

S-param.	**Sim., 2.4 GHz**	**Meas., 2.3 GHz**
S_{21}	10.5 dB	11.8 dB
S_{11}	-26.3 dB	-8.62 dB
S_{22}	-12.8 dB	-8.46 dB

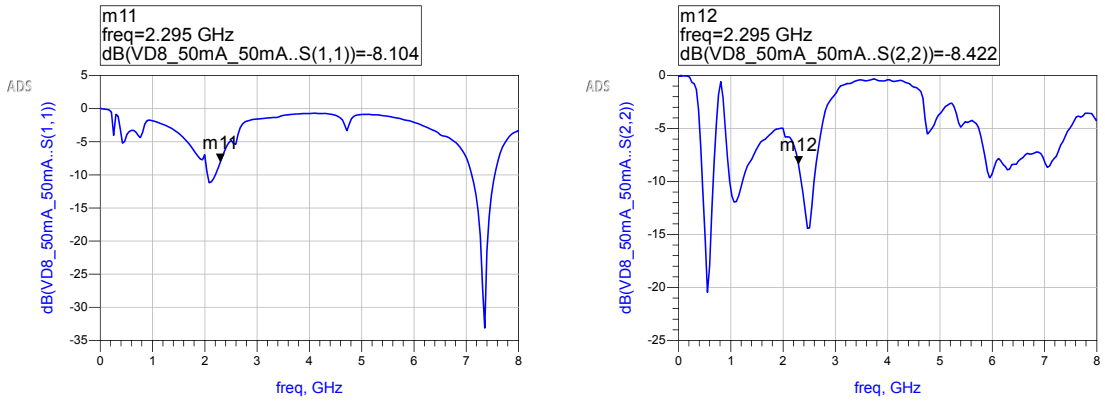
50 mA Design The second design of the second revision is optimized with a 50 mA drain current. Figure 4.2.3 shows its S_{21}-parameter. Both the measured and the measured compared to the simulated.



(a) S_{21}, measured. (b) S_{21}, simulated (red) and measured (blue).

Figure 4.2.3: S_{21} for the 50 mA version.

As with the 300 mA version, the frequency for the optimum gain has shifted down to 2.3 GHz. In addition to this its value has increased slightly compared to what was simulated. Figure 4.2.4 shows the measured S_{11} and S_{22}.



(a) S_{11}, measured. (b) S_{22}, measured.

Figure 4.2.4: S_{11} and S_{22} of the 50 mA version.

Just as with the 300 mA version, both the input and the output reflection have increased. But despite this S_{21} has increased, although just slightly. The numbers for the simulated and measured parameters at the frequencies of interest are found in Table 4.2.2.

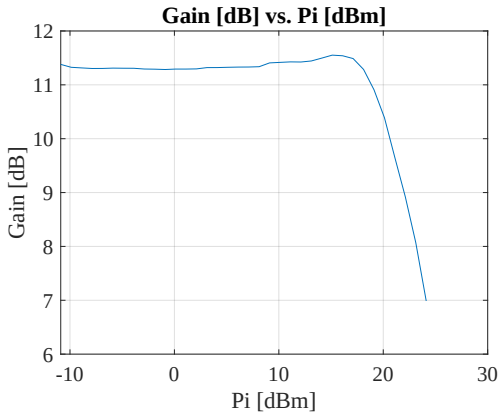
Table 4.2.2: Summary of simulated and measured S-parameters for the rev. 2 PA designed for 50 mA drain current.

S-param.	Sim., 2.4 GHz	Meas., 2.3 GHz
S_{21}	9.26 dB	9.68 dB
S_{11}	-33.4 dB	-8.10 dB
S_{22}	-11.8 dB	-8.42 dB

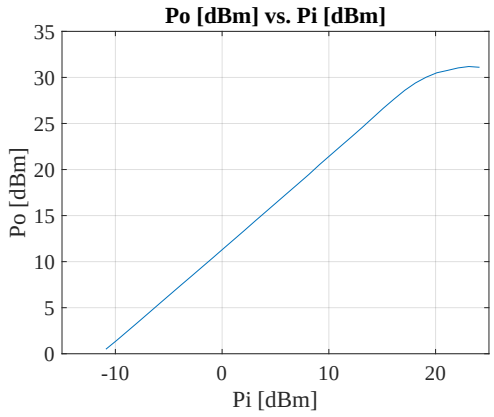
4.2.2 Large-Signal

As mentioned earlier, the large-signal results for this PA revision will also include results from power sweeps with stepped drain voltages, transmission of modulated signals, and drain modulation.

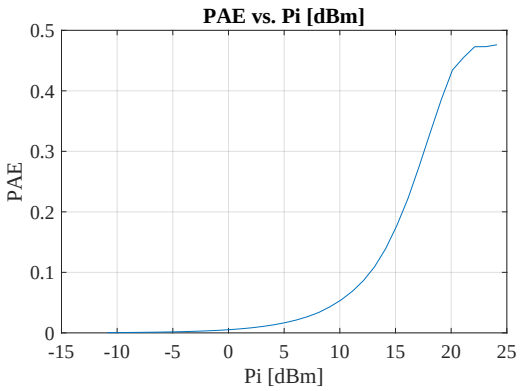
300 mA Design The PA is designed to operate at 2.4 GHz but as the S-parameter measurements showed, the optimal gain frequency has shifted down to 2.3 GHz. As a result of this, the following measurements are performed with a 2.3 GHz RF signal. Figure 4.2.5 shows the results of a power sweep with a fixed drain voltage, $V_D = 8$ V.



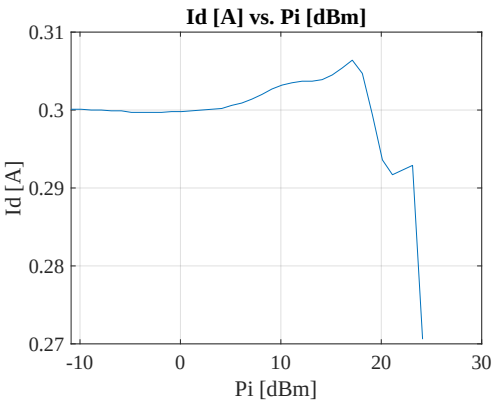
(a) Gain vs. input power.



(b) Output power vs. input power.



(c) PAE vs. input power.

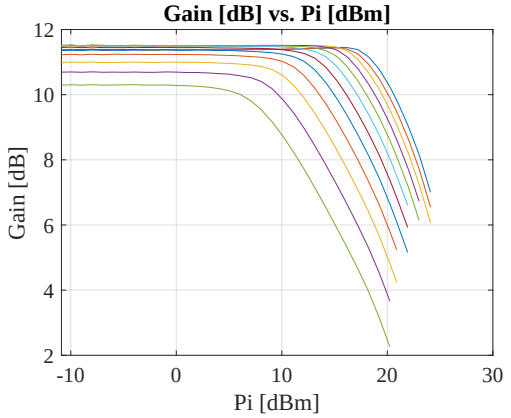


(d) Drain current vs. input power.

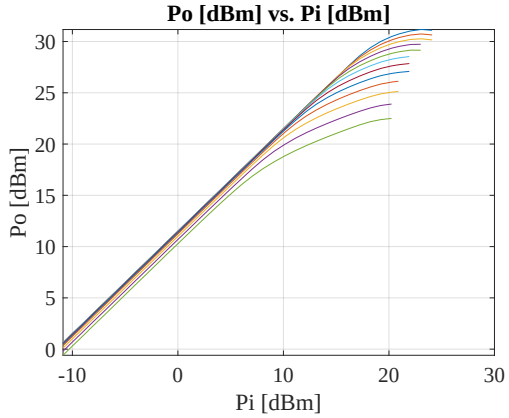
Figure 4.2.5: Results of sweeping the input power with the initial drain current set to 300 mA and the frequency set to 2.3 GHz.

The power sweep in 4.2.5a shows that the gain stays over 11 dB until the input power reaches about 18 dBm and it is still above 10 dB when it reaches 20 dBm. Thus, the PA still has a gain greater than 10 dB when the output power reaches 30 dBm. This is confirmed by the output vs. input power plot in 4.2.5b. The PAE in 4.2.5c reaches a value of more than 45 % in the region where the PA saturates and the output power approaches its limit. The drain current in 4.2.5d at first stays stable at approx. 300 mA before it increases to about 307-308 mA, and then falls rapidly when entering saturation.

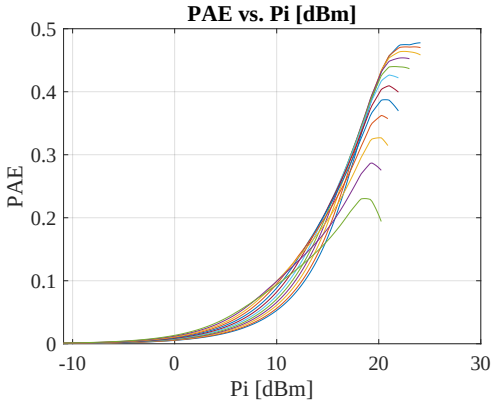
After the power sweep with one single, fixed drain voltage was finished, a new series of power sweeps with different drain voltages was performed. The results from these measurements are found in Figure 4.2.6.



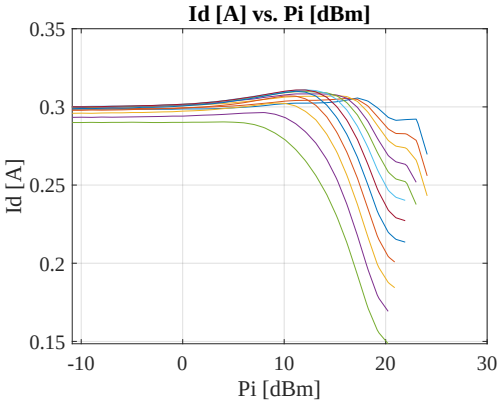
(a) Gain vs. input power.



(b) Output power vs. input power.



(c) PAE vs. input power.



(d) Drain current vs. input power.

Figure 4.2.6: Results of sweeping the input power with the initial drain current set to 300 mA, the frequency set to 2.3 GHz, and stepping the drain voltage from 8 V to 2.5 V in 0.5 V steps. If looking at the highest input powers, the curve with the highest value on the y-axis has the highest drain voltage, $V_D = 8$ V (blue curve). The one with the lowest value has the lowest drain voltage, $V_D = 2.5$ V (green curve).

The plots in 4.2.6a indicate that the PA can provide a gain above 10 dB with all the drain voltages if the input power is low enough. Thus, this is a good indication that it, e.g., should be possible to perform tracking with a flat gain of 10 dB as a goal. 4.2.6b shows that the lower drain voltage

levels saturate at lower input and output power levels, as expected. The PAE plots in 4.2.6c show that the lower drain voltages have higher PAE at lower input power levels. This is no surprise, as a lower drain voltage will make the PA operate closer to saturation at these lower input power levels, but is anyhow a nice observation to make regarding the reason for performing drain modulation. The drain currents for the different drain voltages are plotted in 4.2.6d, where we see that the currents begin in the region around 300 mA for all the drain voltages before most of them increase a few mA and then they all eventually begin to move downwards when saturating.

The measurements in Figure 4.2.6 are used to create different tracking functions for use in both regular drain modulation and PET. The points used to calculate the functions, and the resulting tracking functions, are found in Figure 4.2.7.

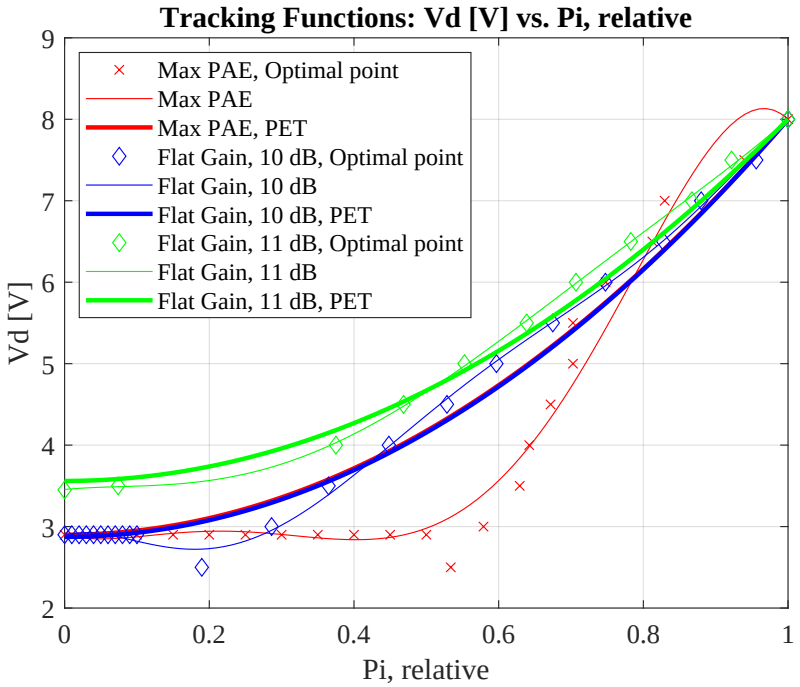
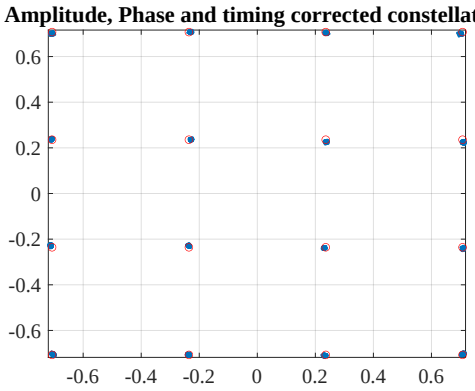


Figure 4.2.7: Tracking functions. The order of the max. PAE function was lowered from 7 to 5, in order to not move too far above $V_d = 8$ V when being right below the maximum input power.

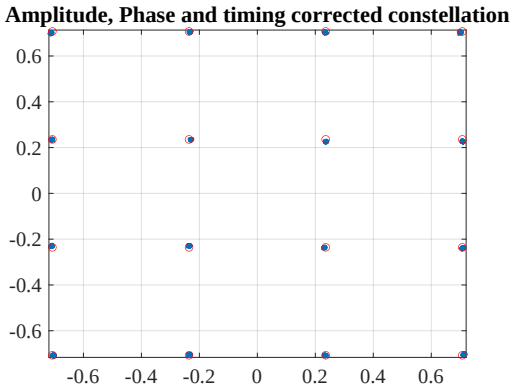
The points that are plotted tightly together in the lowest region of the max. PAE and the 10 dB flat gain plots are there to ensure that the pertaining functions do not move much below this drain voltage level, due to limitations of the tracker used when later performing the tracking[4]. It is possible to observe that for the max. PAE functions, they deviate quite a bit from each other and from the points. For the 11 dB flat gain curves, the regular drain modulation function and the PET function stay quite close to each other. These curves also have a higher lowest drain voltage level of $V_d \approx 3.5$ V.

When performing the tests where linearity is looked at, both when the PA is operating with a static drain voltage and with drain modulation, a 16-QAM signal is used. Figure 4.2.8 shows constellation diagrams for when the PA is operated in two different static modes.

[4]When moving below voltages of 2.8-2.9 V, the voltage from the tracker dropped suddenly and would therefore not provide the necessary reliability to be used in the tracking measurements.



(a) Constellation diagram for static operation with target $P_{out} = 24.9$ dBm.

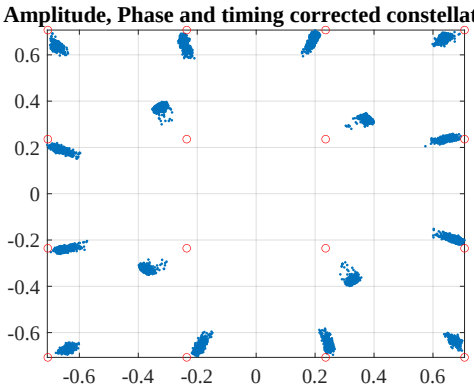


(b) Constellation diagram for static operation with target $P_{out} = 23.1$ dBm.

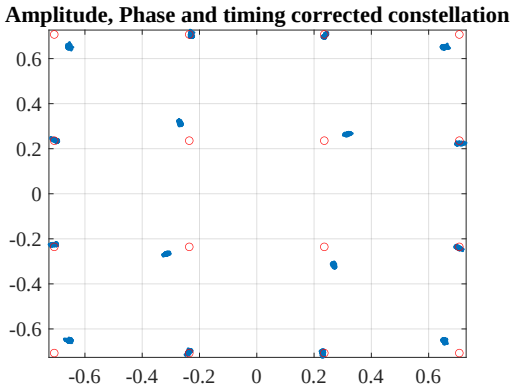
Figure 4.2.8: Constellation diagrams of 16QAM signal, when the PA is biased with a drain current of 300 mA and operated in static mode.

In both diagrams the points are plotted within or very close to the area, marked by a red circle, of the symbol they belong to.

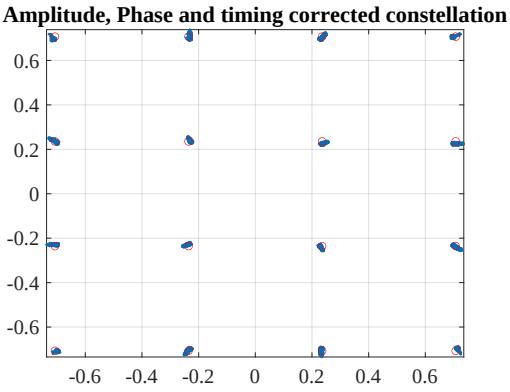
Figure 4.2.9 shows diagrams for when the different tracking modes are used. Seeing all of them next to each other will give an idea of what the different linearity numbers, among other metrics summarized in Tables 4.2.3 and 4.2.4, actually look like in such a diagram. In the later subsections for the other PA versions, only selected constellation diagrams will be shown.



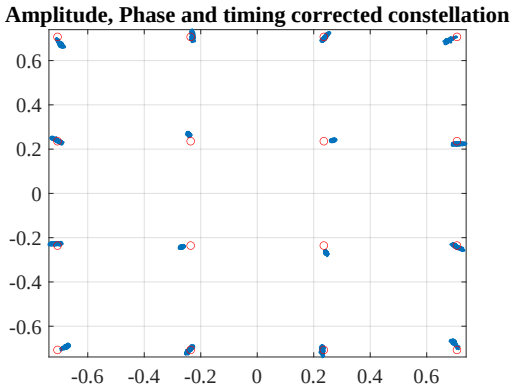
(a) Constellation diagram for classic drain modulation with max. PAE as the goal.



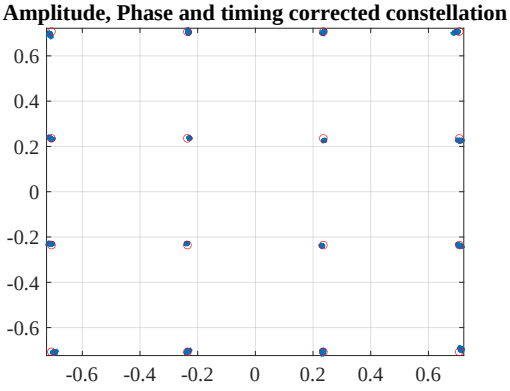
(b) Constellation diagram for operation with PET for max. PAE.



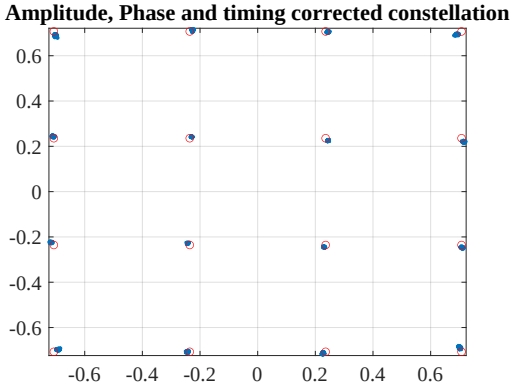
(c) Constellation diagram for classic drain modulation with a flat gain of 10 dB as the goal.



(d) Constellation diagram for operation with PET for a flat gain of 10 dB as the goal.



(e) Constellation diagram for classic drain modulation with a flat gain of 11 dB as the goal.



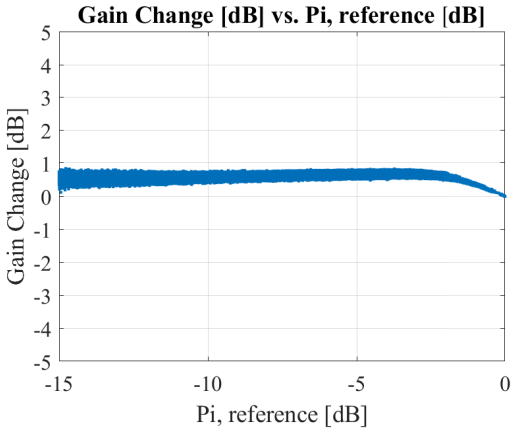
(f) Constellation diagram for operation with PET for a flat gain of 11 dB as the goal.

Figure 4.2.9: Constellation diagrams of 16QAM signal, when the PA is biased with a drain current of 300 mA and the drain voltage is modulated.

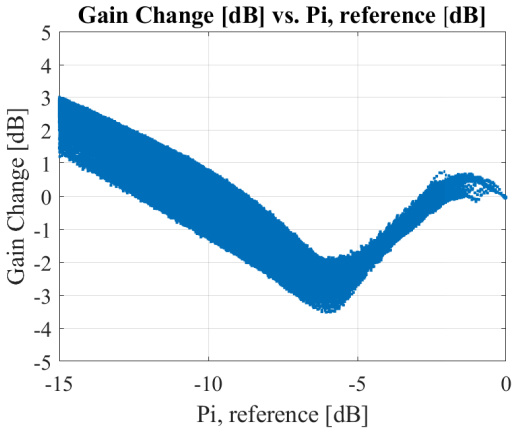
The constellation diagrams show behavior as expected, where the symbols from the static modes or the tracking modes with higher gain and linearity fit better within the ideal symbol positions. Especially Figure 4.2.9a shows what it looks like when the linearity is lower. The points are both

missing the area they are supposed to be placed within and they are not very concentrated. As well the plotted points in 4.2.9b are placed somewhat away from where they ideally should have been but they are not as spread out.

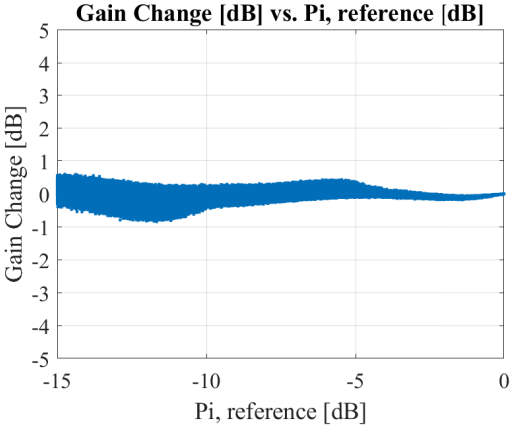
As QAM consists of modulation of both amplitude and phase, it can be interesting to look at how the gain and the phase from the PA change with input power. When comparing with the constellation diagram, variances in gain should result in a spread in distance from the center, or vector length, within points belonging to the same symbol. Variance in phase should result in a spread in angle between the x-axis and the points belonging to the same symbol. Figure 4.2.10 shows how the gain changes with the input power for four different modes, one static and the three classic drain modulation configurations.



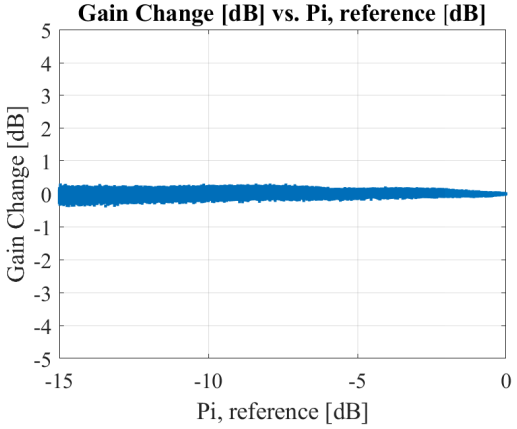
(a) Gain change for static operation with target $P_{out} = 23.1$ dBm.



(b) Gain change for classic drain modulation with max. PAE as the goal.



(c) Gain change for classic drain modulation with a flat gain of 10 dB as the goal.



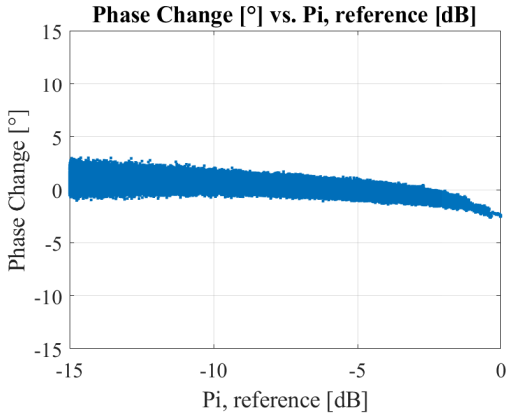
(d) Gain change for classic drain modulation with a flat gain of 11 dB as the goal.

Figure 4.2.10: Gain changes for different modes, when the PA is biased with a drain current of 300 mA.

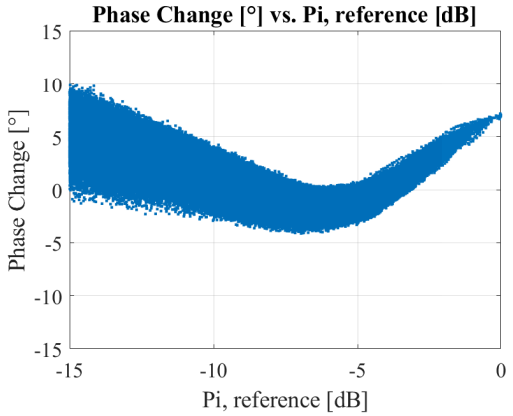
The big variance in gain shown by the plot belonging to the regular drain modulation max. PAE function in Figure 4.2.10b confirms what we saw in the constellation diagram in Figure 4.2.9a. Greater variance in gain leads to a greater variance in distance from the center in the constellation

diagram. The other plots show a relatively flat gain throughout the entire input power region. Especially the 11 dB flat gain plot in 4.2.10d.

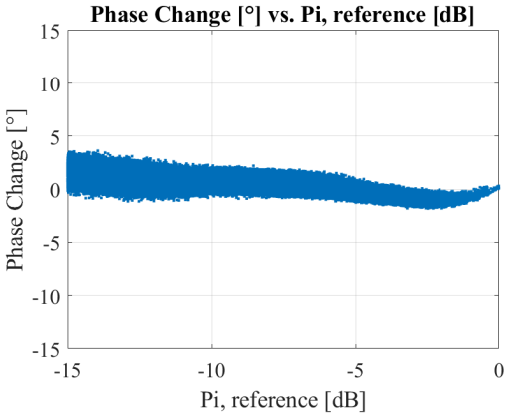
Figure 4.2.11 shows how the phase changes individually with input power for the same four modes.



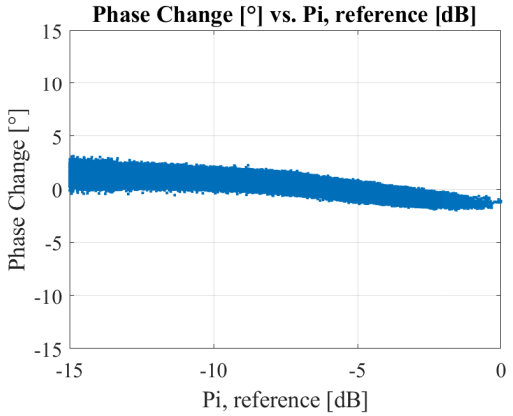
(a) Phase change for static operation with target $P_{out} = 23.1$ dBm.



(b) Phase change for classic drain modulation with max. PAE as the goal.



(c) Phase change for classic drain modulation with a flat gain of 10 dB as the goal.



(d) Phase change for classic drain modulation with a flat gain of 11 dB as the goal.

Figure 4.2.11: Phase changes for different modes, when the PA is biased with a drain current of 300 mA.

Here we can see that the by far biggest variation in phase change vs. input power again is found in the max. PAE plot in Figure 4.2.11b. Confirming that this plot in the constellation diagram, Figure 4.2.9a, has the biggest variation in angle between plotted points belonging to the same symbol. Compared to the max. PAE, the three other plots have a relatively low change in phase as the input power changes.

To get an overview, key performance numbers found when testing the PA biased with a 300 mA drain current and with different tracking functions are found in Table 4.2.3. When operating in static mode, a drain voltage, $V_D = 8$ V, is used.

Table 4.2.3: Measured average performances of PA with 300 mA drain DC current in different operational modes, tested with a 16QAM modulated signal. Here the ACPR corresponds to the highest value of either the lower frequency ACPR, ACPRl, or the higher frequency ACPR, ACPRh.

Mode	$\mathbf{P_{out,\ avg.}}$ **[dBm]**	$\mathbf{G_A}$ **[dB]**	$\mathbf{PAE_{avg.}}$ **[%]**	**STDR [dB]**	**ACPR [dBc]**	**EVM [%]**
Static, $P_{out,\text{Target=24.9 dBm}}$	24.81	12.07	12.11	**34.52**	**-44.30**	**1.09**
Static, $P_{out,\text{Target=23.1 dBm}}$	23.09	12.37	8.18	**38.69**	**-49.01**	**0.945**
Max. PAE	23.15	6.36	**25.41**	16.84	-24.16	13.54
Max. PAE, PET	24.95	8.16	**29.24**	21.74	-30.19	7.77
Flat Gain (10 dB)	23.61	10.41	**19.90**	**34.98**	**-41.28**	**1.58**
Flat Gain (10 dB), PET	23.45	10.24	**19.17**	28.63	-36.96	3.54
Flat Gain (11 dB)	22.95	11.56	14.52	**37.55**	**-46.13**	**1.20**
Flat Gain (11 dB), PET	22.93	11.54	14.16	**33.98**	**-43.67**	**1.43**

The results show that the PA shows very good linearity in both of the two static modes and also three of the tracking modes. The regular drain modulated mode aiming for a 10 dB gain, and both of the two modes aiming for an 11 dB gain have STDR values well above 30, ACPR values below -40 dBc, and EVM values below 2 %. When looking at PAE, both the max. PAE modes have increased this value by about 2-3 times when looking at the static mode with comparable output power. However, the linearity suffers in these modes. The 10 dB flat gain modes, on the other hand, have both approx. doubled the PAE compared to the 23.1 dBm output power, static mode, while still maintaining linearity. Especially the regular drain modulated mode.

The different ACPR values, where both the lower and the higher are included, are found in Table 4.2.4.

Table 4.2.4: Lower and higher frequency ACPR, ACPRl and ACPRh, for PA with 300 mA drain DC current in different operational modes.

Mode	**ACPRl [dBc]**	**ACPRh [dBc]**
Static, $P_{out,\text{Target=24.9 dBm}}$	**-44.30**	**-44.34**
Static, $P_{out,\text{Target=23.1 dBm}}$	**-49.01**	**-49.36**
Max. PAE	-24.27	-24.16
Max. PAE, PET	-30.68	-30.19
Flat Gain (10 dB)	**-46.67**	**-41.28**
Flat Gain (10 dB), PET	-38.15	-36.96
Flat Gain (11 dB)	**-50.83**	**-46.13**
Flat Gain (11 dB), PET	**-44.59**	**-43.67**

When looking at the numbers in Table 4.2.4 it is noticeable how the device has a slightly lower (better), but almost equal, ACPRh compared to ACPRl for the tests without drain modulation. For the tests where drain modulation is used, however, ACPRl consistently has a lower value.

Lastly, it may be interesting to have a look at a bandwidth comparison between regular drain modulation and PET.

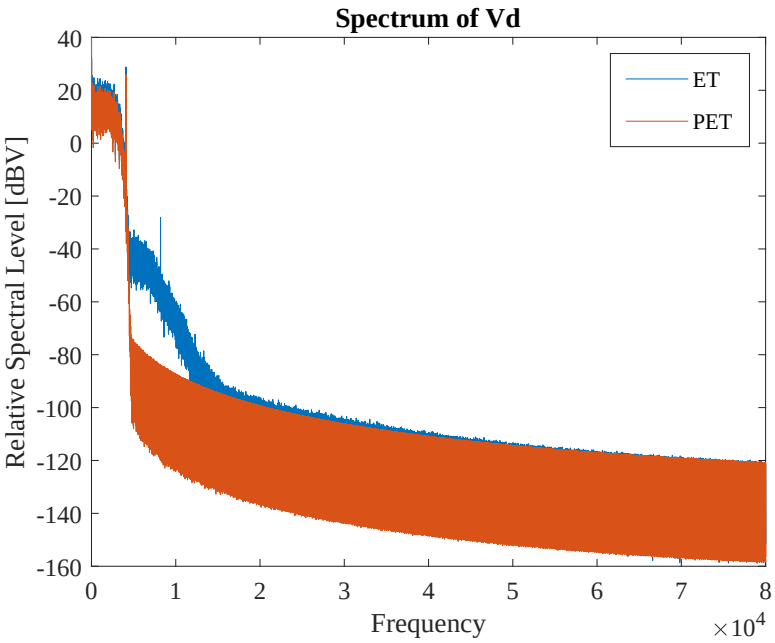
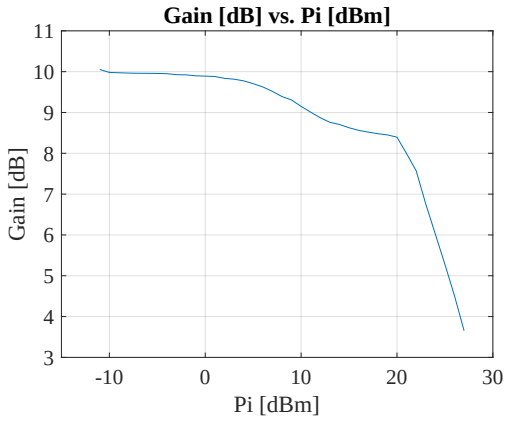


Figure 4.2.12: Bandwidth comparison of the 11 dB flat gain tracking signals.

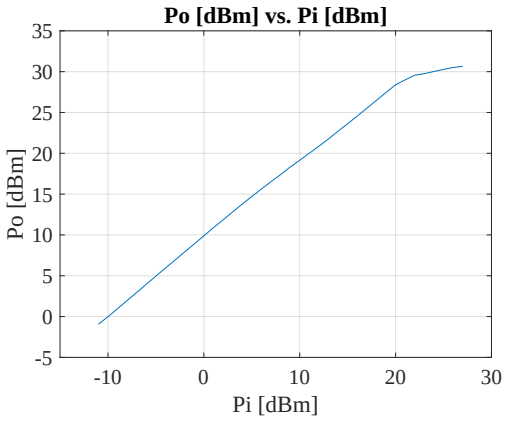
Quite clearly the PET signal shows a narrower bandwidth than the regular drain modulation signal.

50 mA Design For this design as well, the measurements are performed with an RF signal frequency of 2.3 GHz.

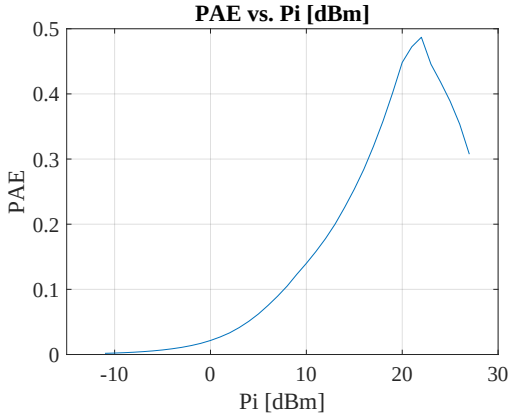
Figure 4.2.13 shows the plotted results from sweeping the input power and maintaining the drain bias voltage fixed at $V_D = 8$ V.



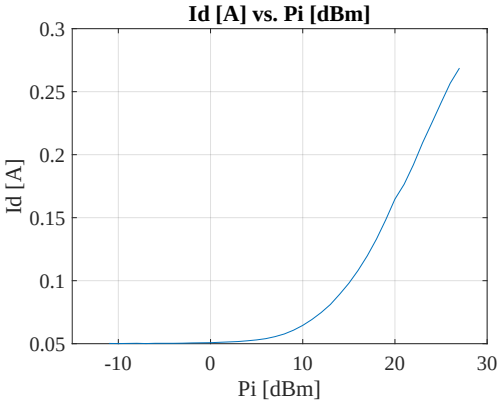
(a) Gain vs. input power.



(b) Output power vs. input power.



(c) PAE vs. input power.

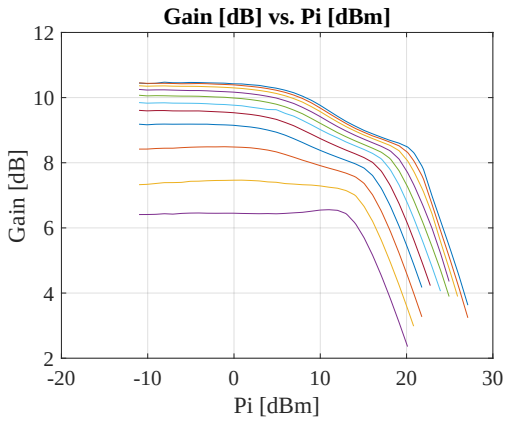


(d) Drain current vs. input power.

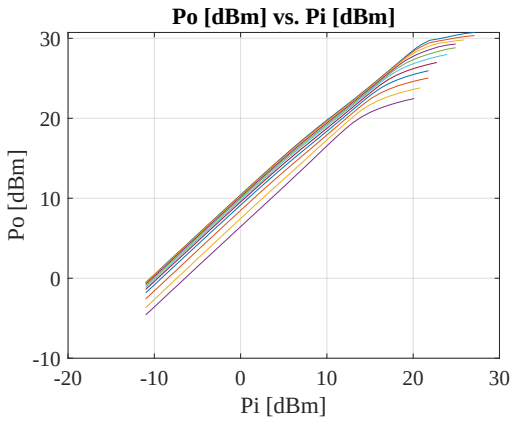
Figure 4.2.13: Results of sweeping the input power with the initial drain current set to 50 mA and the frequency set to 2.3 GHz.

We can see that the gain starts at about 10 dB before it has dropped to approx. 8.5 dB when the compression begins. The PA is just able to deliver 30 dBm output power in the higher input power range. Considering the PAE, it isn't able to reach a higher peak value than what the 300 mA design managed to do but it has a higher value at lower input power levels. E.g., PAE $\approx 15\,\%$ at 10 dBm input power for the design biased with a 50 mA drain current, vs. PAE $\approx 5\,\%$ at the same input power for the design biased with a 300 mA drain current. The plot of the drain current shows that it starts at 50 mA before it increases through the entire power spectrum.

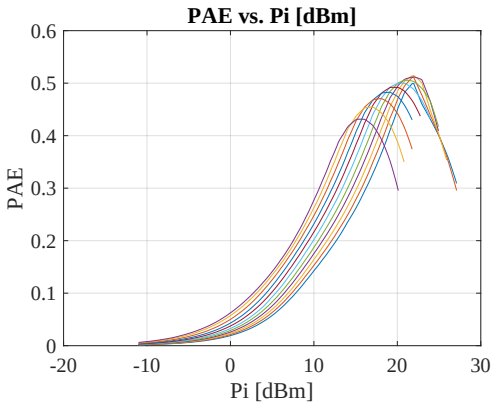
Figure 4.2.14 shows the plotted results of power sweeps with the drain biased with a series of different voltages. To increase the possible range of the drain tracking, the drain current at $V_D = 8$ V is increased to 65 mA.



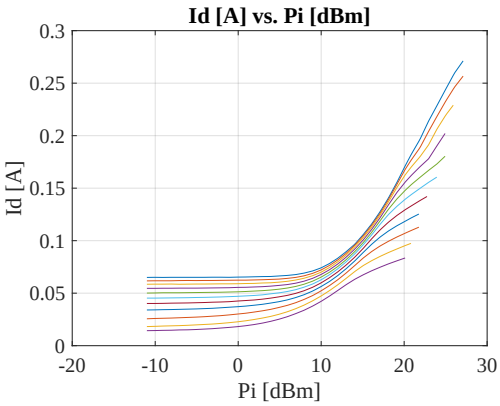
(a) Gain vs. input power.



(b) Output power vs. input power.



(c) PAE vs. input power.



(d) Drain current vs. input power.

Figure 4.2.14: Results of sweeping the input power with the initial drain current set to 65 mA, the frequency set to 2.3 GHz, and stepping the drain voltage from 8 V to 3 V in 0.5 V steps.

The first thing to notice in the plot is that, as mentioned above, the gate bias voltage was altered in order to have a drain current of 65 mA, shown in 4.2.14d, when applying a drain bias voltage $V_D = 8$ V. As the gate voltage now is closer to the threshold than what was the case in the 300 mA design, the relative change in drain current is bigger with the steps in drain voltage. The plots of gain vs. input power also show that the change in gain is bigger with the drain voltage steps. With about a 4 dB difference in small-signal gain, compared to about 1.5 dB in the case of the 300 mA design. In addition to this, the gain is a bit lower, to begin with. Just above 10 dB. The PAE plots confirm some things of what the plot with a single drain voltage showed. If we again use the 10 dBm input power to compare, the 300 mA PA's highest PAE is approx. 10 %, while the highest PAE at 10 dBm input power of this version almost reaches 30 %. As well it is worth noticing that the PAE peaks out just above 50 % now after increasing the drain current starting point to 65 mA and introducing lower drain voltages.

Figure 4.2.15 shows the resulting tracking functions, and the points used to calculate them, from the measurements done previously.

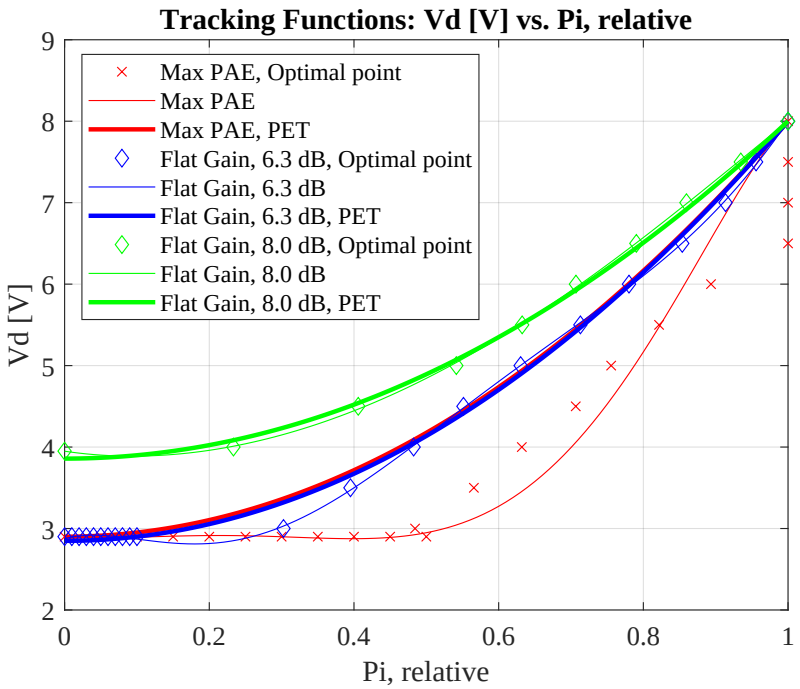
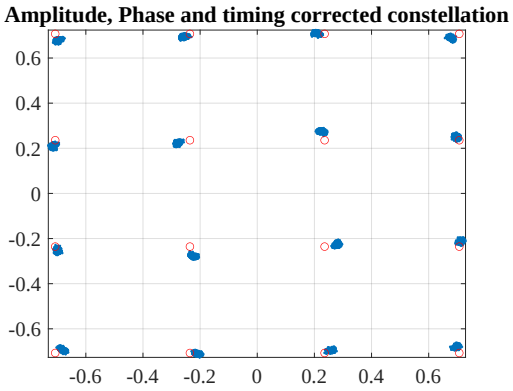


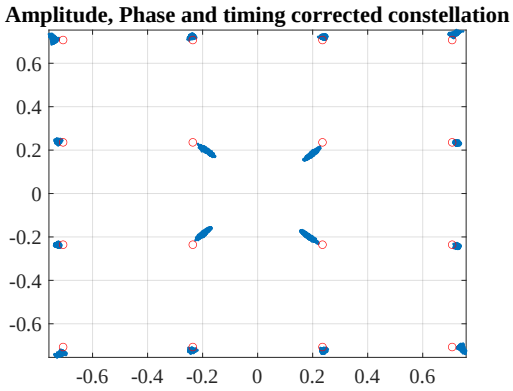
Figure 4.2.15: Tracking functions.

Again the points plotted tightly together in the lowest region of the max. PAE, and this time around the 6.3 dB flat gain plots, are there to ensure that the pertaining functions do not move much below this drain voltage level, due to limitations of the tracker used when later performing the tracking. Also now it is possible to observe that the max. PAE functions deviate quite a bit from each other and from the points. And as for the 11 dB flat gain curves earlier, now 8.0 dB flat gain, the regular drain modulation function, and the PET function stay quite close to each other. These curves again have a higher lowest drain voltage level. Now of almost 4 V.

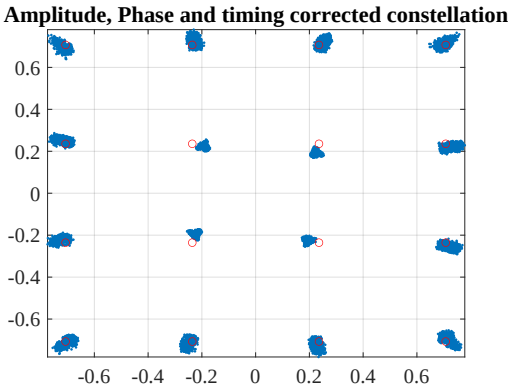
The next step is again to run a modulated signal through the PA. Both by running it with a static drain voltage and with a dynamic drain voltage, using the functions above. Figure 4.2.16 shows the plotted constellation diagrams for one of the static modes and for the three modes using PET.



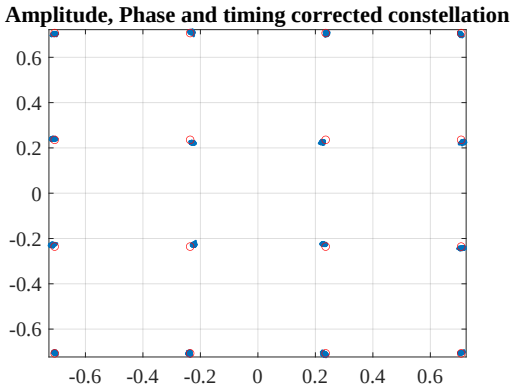
(a) Constellation diagram for static operation with target $P_{out} = 23.1$ dBm.



(b) Constellation diagram for operation with PET for max. PAE.



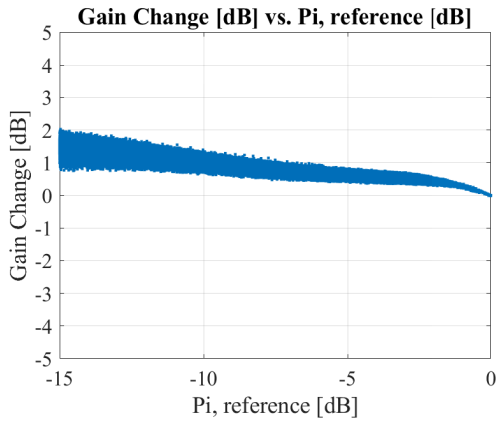
(c) Constellation diagram for operation with PET with a flat gain of 6.3 dB as the goal.



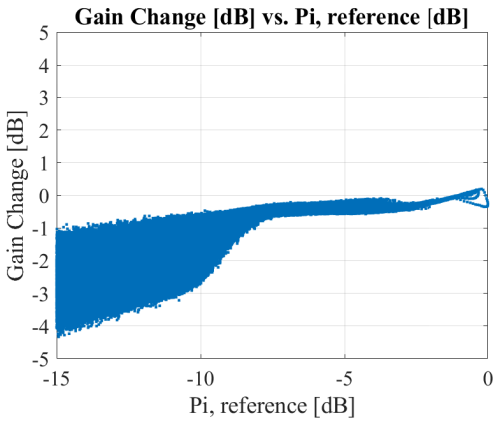
(d) Constellation diagram for operation with PET with a flat gain of 8.0 dB as the goal.

Figure 4.2.16: Constellation diagrams of 16QAM signal, when the PA is biased with a drain current of 65 mA.

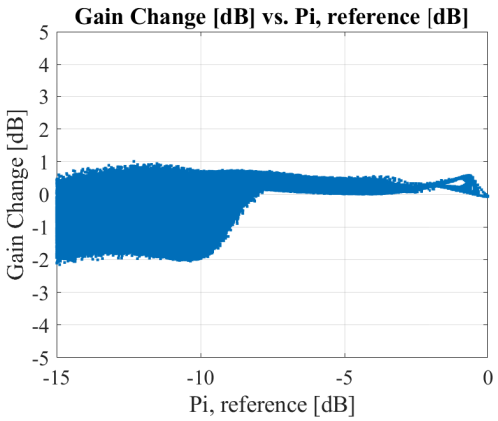
There are some differences between the plots, where it seems like the PET aimed at a flat gain of 8.0 dB has the least spread in the transmitted signals within the same symbol. This is also reflected in the gain variation plotted in Figure 4.2.17.



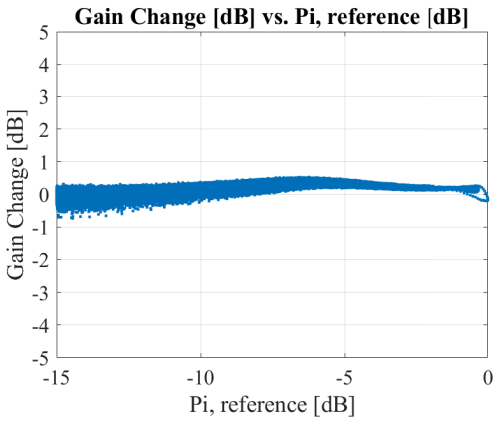
(a) Gain change for static operation with target $P_{out} = 23.1$ dBm.



(b) Gain change for operation with PET for max. PAE.



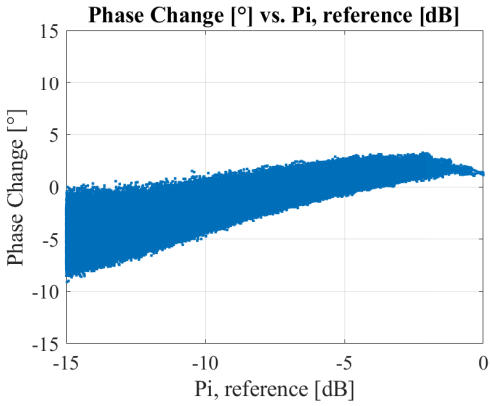
(c) Gain change for operation with PET with a flat gain of 6.3 dB as goal.



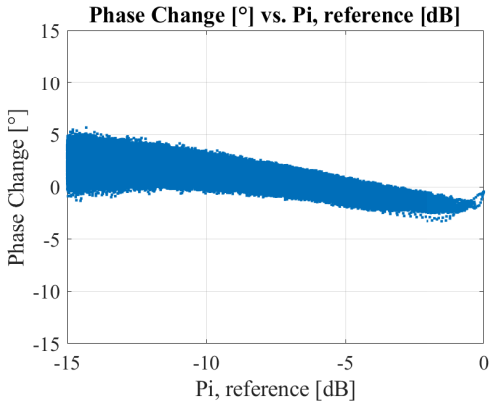
(d) Gain change for operation with PET with a flat gain of 8.0 dB as goal.

Figure 4.2.17: Gain changes for different modes, when the PA optimized for 50 mA drain current is biased with a drain current of 65 mA.

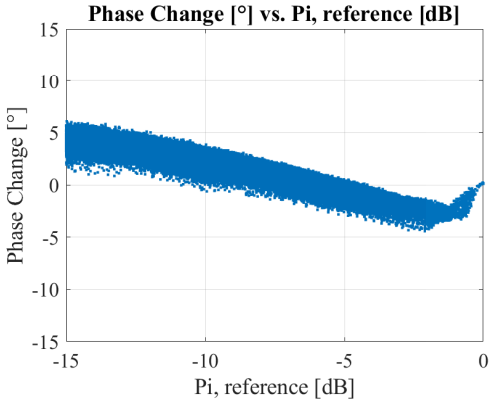
The PET mode with an aimed gain of 8.0 dB stays within ±1 dB deviation from the gain at 0 dB back-off. The PET for max. PAE on the other hand, deviates between -1 and -4 dB in the lower input power spectrum. And the PET aimed at a flat gain of 6.3 dB between +1 and -2 dB. For the static operation plot, both the deviation and variance shrink as the input power increases. The phase changes in correlation to input power for the same four operational modes are found in Figure 4.2.18.



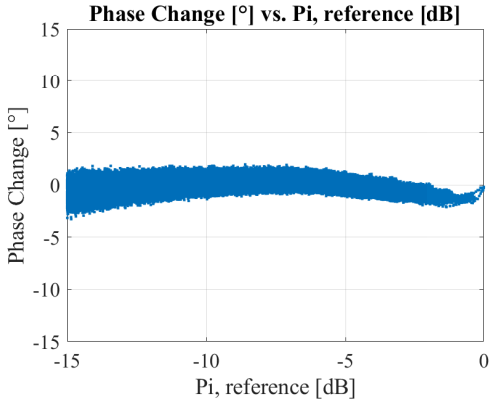
(a) Phase change for static operation with target $P_{out} = 23.1$ dBm.



(b) Phase change for operation with PET for max. PAE.



(c) Phase change for operation with PET with a flat gain of 6.3 dB as the goal.



(d) Phase change for operation with PET with a flat gain of 8.0 dB as the goal.

Figure 4.2.18: Phase changes for different modes, when the PA optimized for 50 mA drain current is biased with a drain current of 65 mA.

Again the PET aimed at 8.0 dB flat gain shows the least deviation and variance, while the biggest deviation and variance actually are found within the static operation mode. At least for the lower input power levels. Summarized performance metrics of the PA are found in Table 4.2.5.

Table 4.2.5: Measured average performances of PA with 65 mA drain DC current in different operational modes. Here the ACPR corresponds to the highest value of either ACPRl or ACPRh. The number in parenthesis behind "Flat Gain" indicates the gain that was set as the goal in the tracking function.

Mode	$\mathbf{P_{out,\ avg.}}$ **[dBm]**	$\mathbf{G_A}$ **[dB]**	$\mathbf{PAE_{avg.}}$ **[%]**	**STDR [dB]**	**ACPR [dBc]**	**EVM [%]**
Static, $P_{out,\text{Target=18.9 dBm}}$	18.89	11.46	10.52	29.22	-39.70	3.67
Static, $P_{out,\text{Target=23.1 dBm}}$	23.08	10.47	21.97	28.19	-37.99	4.55
Max. PAE	18.8	4.43	29.57	16.46	-24.22	8.52
Max. PAE, PET	22.50	8.08	**47.40**	25.44	-32.54	5.41
Flat Gain (6.3 dB)	23.25	6.81	**50.69**	23.99	-31.38	5.14
Flat Gain (6.3 dB), PET	23.34	6.90	**50.32**	27.21	-34.20	3.98
Flat Gain (8.0 dB)	23.20	9.07	**41.87**	**33.64**	**-42.62**	**1.83**
Flat Gain (8.0 dB), PET	23.19	9.06	**41.50**	**35.97**	**-44.53**	**1.43**

The numbers in the table confirm what was found in the previous figures. That operation in the 8.0 dB flat gain PET mode provides the best linearity. The actual gain in this mode is found to be 9.06 dB. 1.41 dB less than the static mode with comparable average output but also with a 19.53 % increase in PAE. The highest PAE is found at right above 50 % in the two 6.3 dB flat gain modes. Table 4.2.6 provides the two different ACPR values for each mode.

Table 4.2.6: Lower and higher ACPR for PA with 65 mA drain DC current in different operational modes.

Mode	**ACPRl [dBc]**	**ACPRh [dBc]**
Static, $P_{out,\text{Target=18.9 dBm}}$	-39.94	-39.70
Static, $P_{out,\text{Target=23.1 dBm}}$	-37.99	-38.03
Max. PAE	-24.22	-24.97
Max. PAE, PET	-33.62	-32.54
Flat Gain (6.3 dB)	-31.75	-31.38
Flat Gain (6.3 dB), PET	-36.26	-34.20
Flat Gain (8.0 dB)	**-42.87**	**-42.62**
Flat Gain (8.0 dB), PET	**-44.86**	**-44.53**

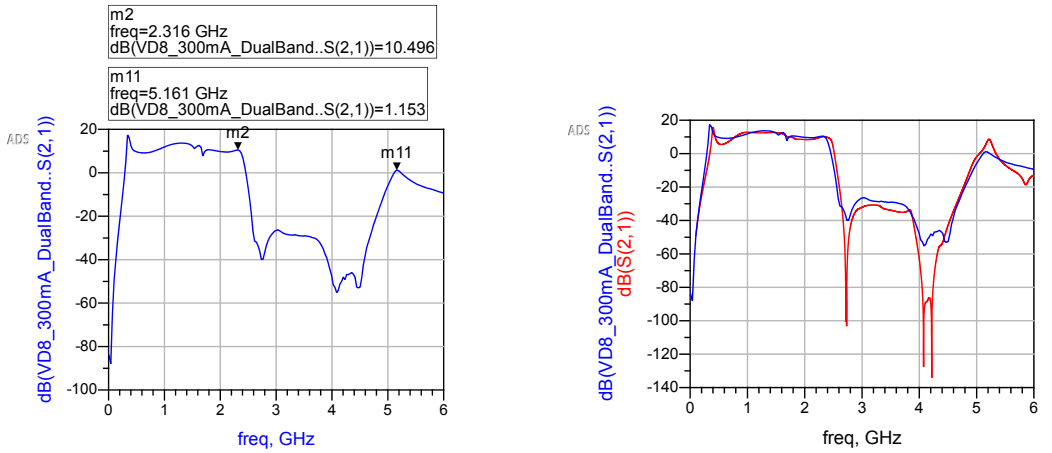
Again the ACPRl values seem to be the lowest for most of the tracked modes, except for the regular drain modulated max. PAE.

4.3 Power Amplifier, vol. 3, Dual-Band

The third and final revision of the PA is not split into two different designs, as rev. 2 was, but designed two operate at two different frequencies. Therefore, the S-parameter results will be presented together, as here the frequency is the variable to be swept. The large-signal results on the other hand, will be presented in two separate paragraphs, as they are measured and analyzed separately.

4.3.1 S-Parameters

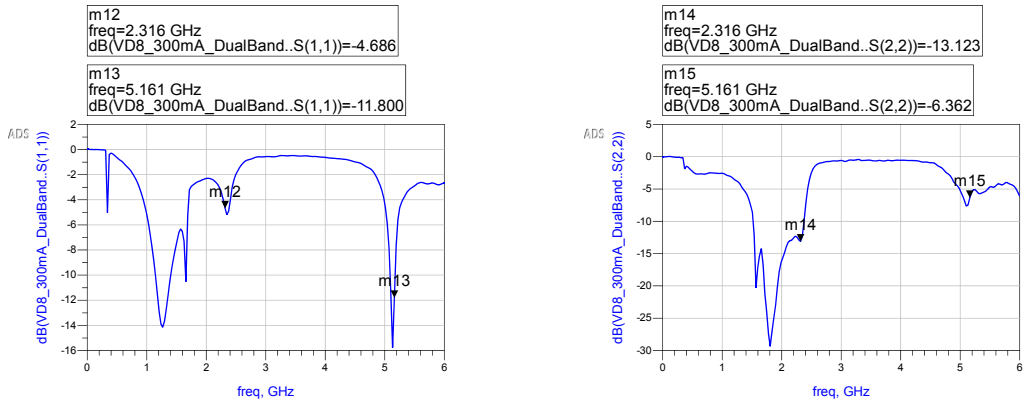
The small-signal measurements of the dual-band PA reveals that it operates close to what was expected for the lower frequency band but not for the higher frequency band, as shown by the comparison of simulated and measured S_{21} in Figure 4.3.1b. The measured S_{21} alone is found in Figure 4.3.1a.



(a) S_{21}, measured. (b) S_{21}, simulated (red) and measured (blue).

Figure 4.3.1: S_{21} of the dual-band PA.

One thing to notice is that again the optimal frequencies gain-wise have shifted a bit down. From 2.4 GHz to about 2.3 GHz for the lower band and from 5.2 GHz to about 5.15 GHz for the higher band. This can be acceptable for a prototype, where some simulation parameters are not exact and as well the PCB arrived without any copper or solder layer on the underside, which led to copper tape being used to minimize the effect this. However, the most important thing to notice is the drop in gain from simulated to measured for the higher frequency band. Measured S_{11} and S_{22} are plotted in Figure 4.3.2.



(a) S_{11}, measured. (b) S_{22}, measured.

Figure 4.3.2: S_{11} and S_{22} of the dual-band PA.

Table 4.3.1 summarizes the simulated and measured S-parameters. As with the previous small-signal results, S_{12} is not included because of the use of attenuators leading to noise and unreliable results for this parameter.

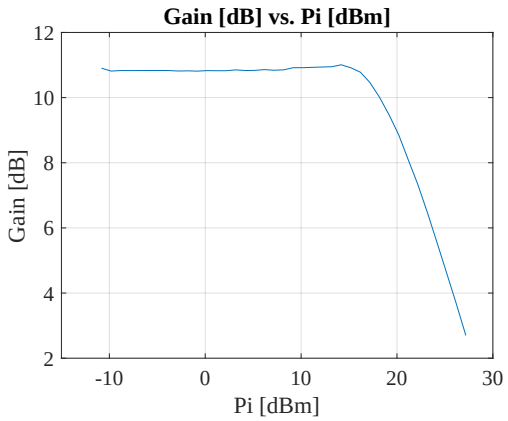
Table 4.3.1: Summary of simulated and measured S-parameters for the dual-band PA.

S-param.	**Sim., 2.4 GHz**	**Meas., 2.3 GHz**	**Sim., 5.2 GHz**	**Meas., 5.15 GHz**
S_{21}	9.72 dB	10.5 dB	8.19 dB	1.15 dB
S_{11}	-21.7 dB	-4.69 dB	-14.0 dB	-11.8 dB
S_{22}	-9.20 dB	-13.1 dB	-3.03 dB	-6.36 dB

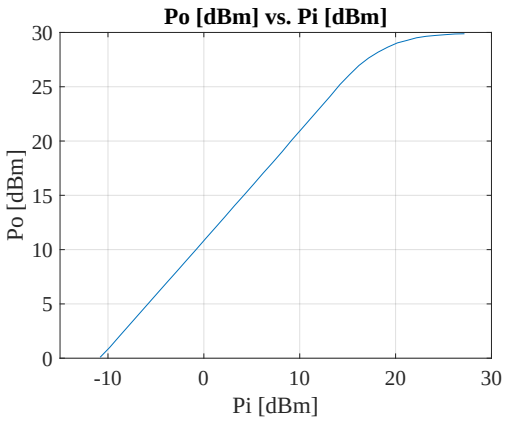
It can be observed, when looking at S_{11}, that the input reflection has increased according to the measurements, compared to the simulation. A bit for the higher band but especially for the lower. The output reflection, S_{22}, has decreased, compared to the simulated values, for both bands. Regarding S_{21}, it has actually increased for the measured value compared to the simulated value, for the lower frequency band. But the most noteworthy observation is, as already mentioned, the decrease in S_{21} for the higher band. From 8.19 dB down to only 1.15 dB.

4.3.2 Large-Signal

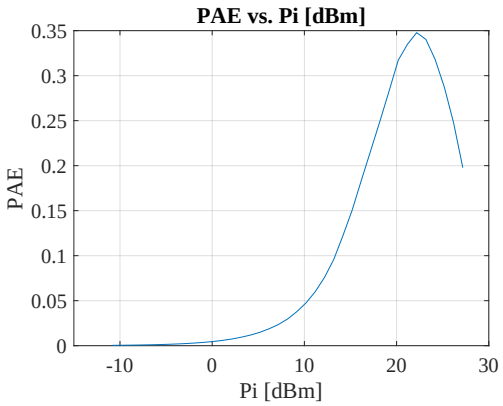
2.3 GHz Like the rev. 2 PA, the lower frequency band of the dual-band amplifier had shifted down to have a better match at 2.3 GHz and will therefore be measured at this frequency for the lower band. Figure 4.3.3 summarizes the results of an input power sweep in the lower frequency band with a fixed drain voltage, $V_D = 8$ V.



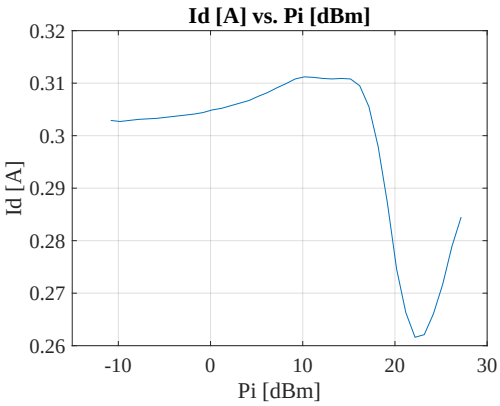
(a) Gain vs. input power.



(b) Output power vs. input power.



(c) PAE vs. input power.

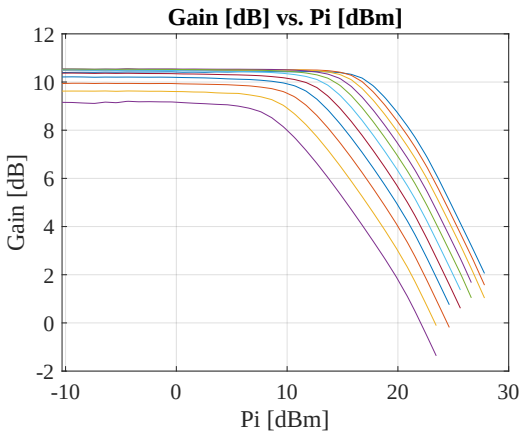


(d) Drain current vs. input power.

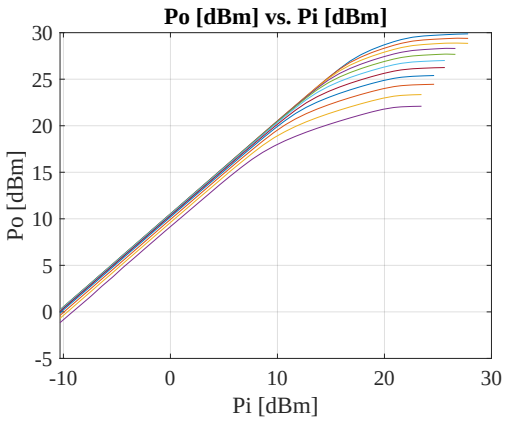
Figure 4.3.3: Results of sweeping the input power with the frequency set to 2.3 GHz.

Some points to notice are that the gain stays quite flat up to an input power of about 16-17 dB, where it starts to drop, seen in Figure 4.3.3a. The PA is just able to deliver an output power of 30 dB, observed in Figure 4.3.3b. The PAE now reaches a maximum of approx. 35 % in Figure 4.3.3c, and the drain current increases to about 310 mA before it starts dropping around where the gain compression begins, see Figure 4.3.3d.

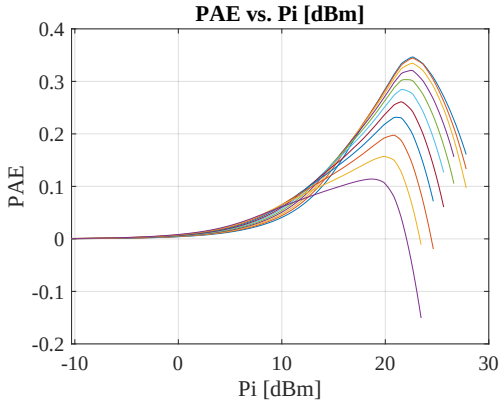
The next figure, Figure 4.3.4, shows the same measurements but now with curves for several different drain voltages.



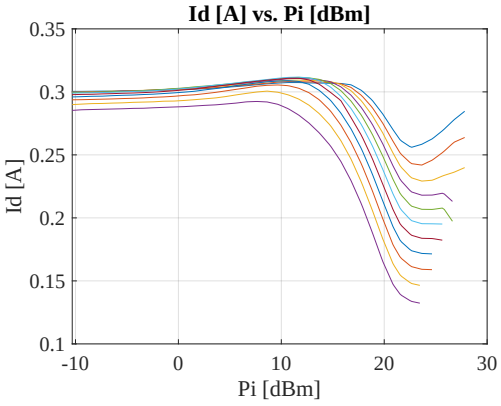
(a) Gain vs. input power.



(b) Output power vs. input power.



(c) PAE vs. input power.



(d) Drain current vs. input power.

Figure 4.3.4: Results of sweeping the input power with the initial drain current set to 300 mA, the frequency set to 2.3 GHz, and stepping the drain voltage from 8 V to 3 V in 0.5 V steps.

The drain voltage was stepped in intervals of 0.5 V. The highest value, $V_D = 8$ V, is represented by the upper curve in each plot (blue), while the lowest value, $V_D = 3$ V, is represented by the lower curve in each plot (purple). The gain curves in Figure 4.3.4a shows possibilities of tracking a flat gain at, e.g., 9.5 dB for the whole drain voltage range and 10.4 dB for a bit higher up in the drain voltage range. The measurements resulted in the tracking functions found in Figure 4.3.5.

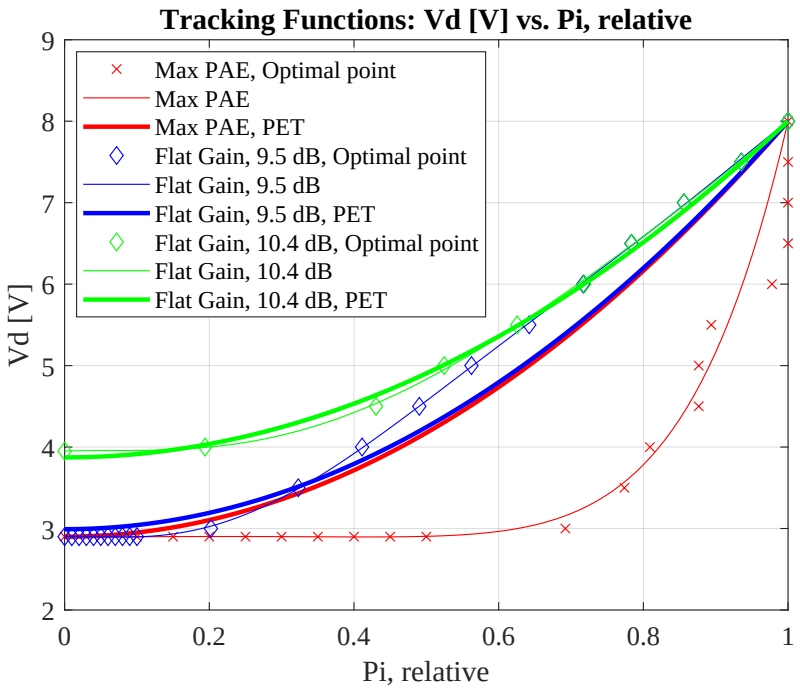
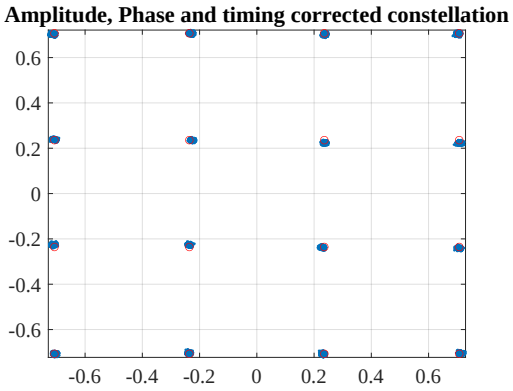


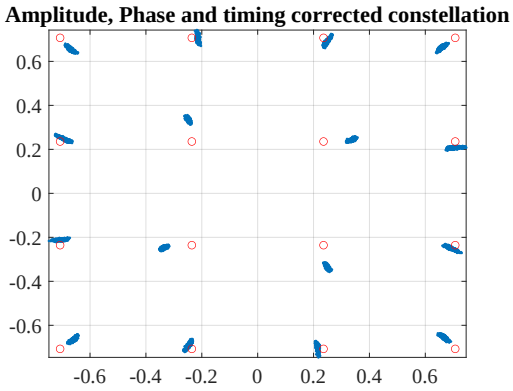
Figure 4.3.5: Tracking functions.

The tracking functions for the 9.5 dB flat gain and the max. PAE all go down to the lowest possible drain voltage value. This lowest value is fixed to 2.9 V, due to limitations of the tracker. The functions for 10.4 dB flat gain go down to a drain voltage of 4 V, as this was the lowest value where such a gain was still achievable.

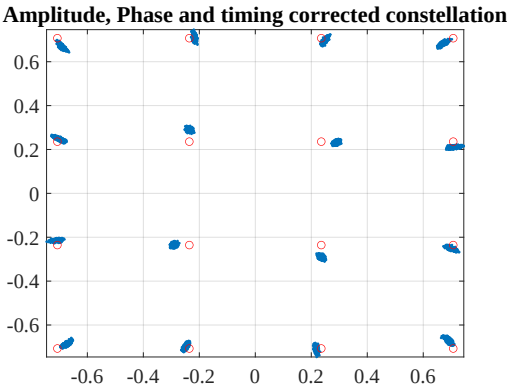
Both amplification without any form of tracking and amplification with the different tracking functions applied was tested with a 16QAM modulated signal. Some of the resulting constellation diagrams are found in Figure 4.3.6.



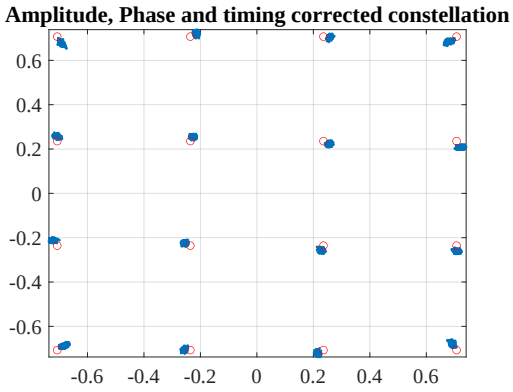
(a) Constellation diagram for static operation with target $P_{out} = 21.8$ dBm.



(b) Constellation diagram for operation with PET for max. PAE.



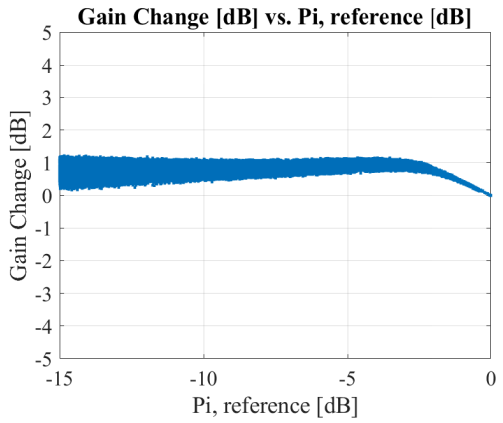
(c) Constellation diagram for use of PET with a flat gain of 9.5 dB as goal.



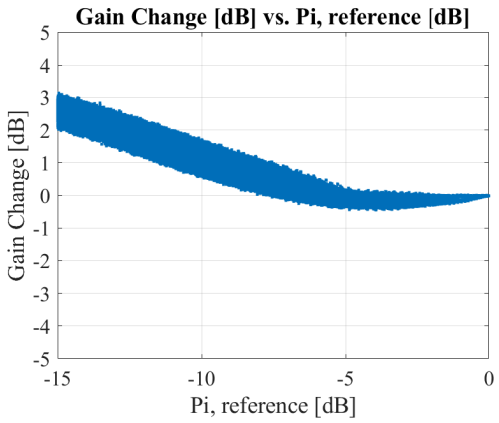
(d) Constellation diagram for use of PET with a flat gain of 10.4 dB as goal.

Figure 4.3.6: Constellation diagrams of 16QAM signal, when the PA is biased with a drain current of 300 mA and the RF signal has a carrier frequency of 2.3 GHz.

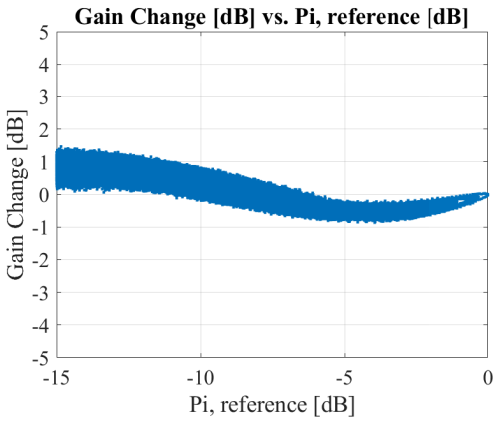
The constellation diagram of the PET for max. PAE seems to be the most distorted of the four, as seen in Figure 4.3.6b. Then comes 4.3.6c. In the two other diagrams the plotted points are found in more focused areas, closer to the region of the symbol they belong to. This should, as for the second revision PA, be reflected in the change of gain through the input power range, seen in Figure 4.3.7.



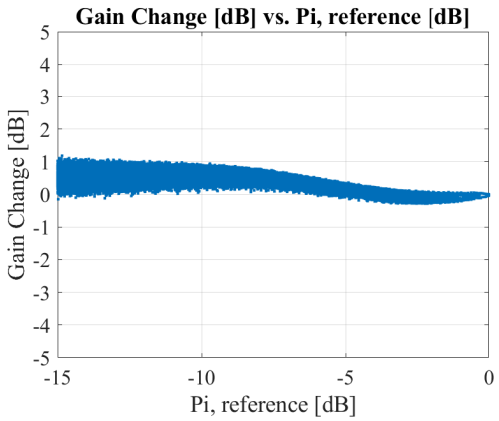
(a) Gain change for static operation with target $P_{out} = 21.8$ dBm.



(b) Gain change for operation with PET for max. PAE.



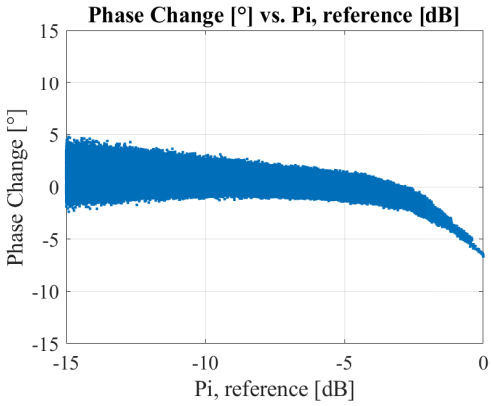
(c) Gain change for operation with PET with a flat gain of 9.5 dB as goal.



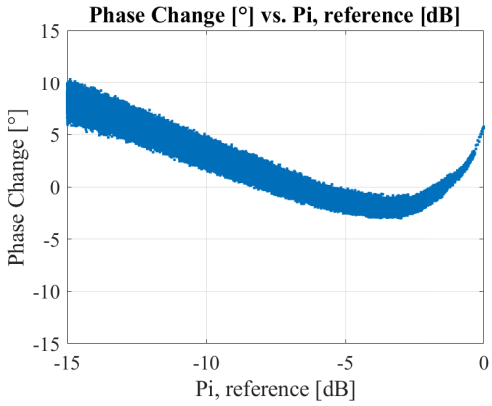
(d) Gain change for operation with PET with a flat gain of 10.4 dB as goal.

Figure 4.3.7: Gain changes for different modes, when the PA is biased with a drain current of 300 mA and the RF signal has a carrier frequency of 2.3 GHz.

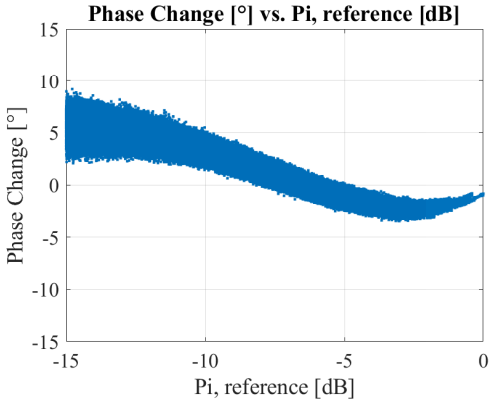
And also in the phase change through the input power range, seen in Figure 4.3.8.



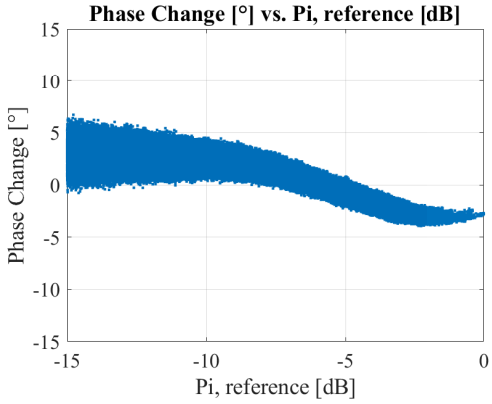
(a) Phase change for static operation with target $P_{out} = 21.8$ dBm.



(b) Phase change for operation with PET for max. PAE.



(c) Phase change for operation with PET with a flat gain of 9.5 dB as goal.



(d) Phase change for operation with PET with a flat gain of 10.4 dB as goal.

Figure 4.3.8: Phase changes for different modes, when the PA is biased with a drain current of 300 mA and the RF signal has a carrier frequency of 2.3 GHz.

Table 4.3.2 summarizes the performance of the PA when transmitting the 16QAM signal.

Table 4.3.2: Measured performances of the PA at 2.3 GHz with 300 mA drain DC current in different operational modes, when transmitting a 16QAM signal. Here the ACPR corresponds to the highest value of either ACPRl or ACPRh.

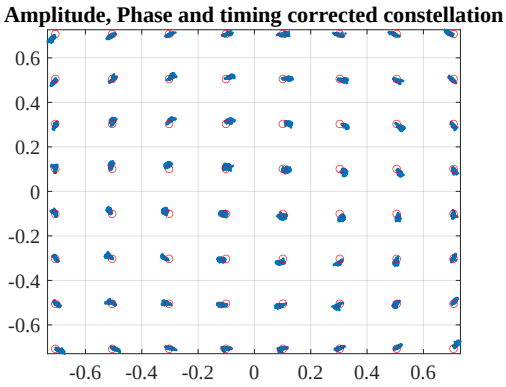
Mode	**$P_{out,\ avg.}$ [dBm]**	**G_A [dB]**	**$PAE_{avg.}$ [%]**	**STDR [dB]**	**ACPR [dBc]**	**EVM [%]**
Static, $P_{out,\text{Target=22.3 dBm}}$	22.35	12.17	5.65	**33.84**	**-43.61**	**1.33**
Static, $P_{out,\text{Target=21.8 dBm}}$	21.84	12.16	5.01	**34.37**	**-45.06**	**1.46**
Max. PAE	20.40	5.04	9.14	14.16	-22.33	18.73
Max. PAE, PET	22.90	7.54	**13.71**	21.39	-29.32	8.54
Flat Gain (9.5 dB)	22.24	9.96	**10.95**	**30.79**	**-38.30**	**2.58**
Flat Gain (9.5 dB), PET	21.85	9.57	**10.24**	25.08	-33.42	5.22
Flat Gain (10.4 dB)	21.73	11.39	8.48	**29.43**	**-38.96**	**3.20**
Flat Gain (10.4 dB), PET	21.77	11.43	8.44	**28.00**	**-37.99**	**3.79**

A summary of both the lower and the higher ACPR is found in Table 4.3.3.

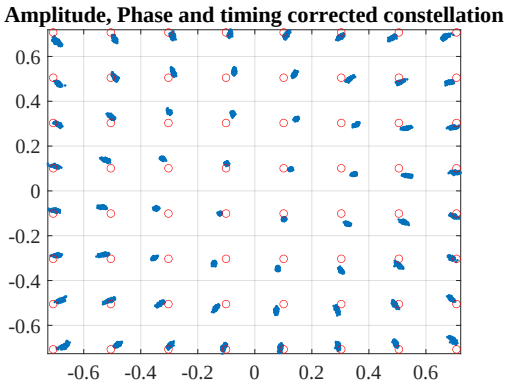
Table 4.3.3: Lower and higher ACPR for PA with 300 mA drain DC current in different operational modes.

Mode	**ACPRl [dBc]**	**ACPRh [dBc]**
Static, $P_{out,\text{Target=22.3 dBm}}$	-43.61	**-44.27**
Static, $P_{out,\text{Target=21.8 dBm}}$	-45.06	**-45.84**
Max. PAE	-22.64	-22.33
Max. PAE, PET	-30.03	-29.32
Flat Gain (9.5 dB)	**-41.71**	**-38.30**
Flat Gain (9.5 dB), PET	-34.06	-33.42
Flat Gain (10.4 dB)	**-39.13**	**-38.96**
Flat Gain (10.4 dB), PET	**-37.99**	**-38.00**

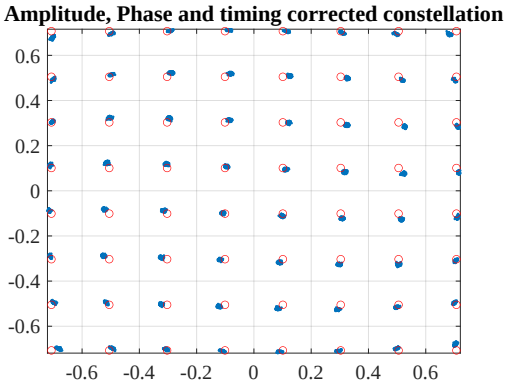
As the nRF7002 chip is able to communicate with a modulation of 64QAM, it is also of interest to see how the PA performs for such a modulated signal, [5]. Figure 4.3.9 shows constellation diagrams for the four different flat gain tracking modes when amplifying a 64QAM modulated signal.



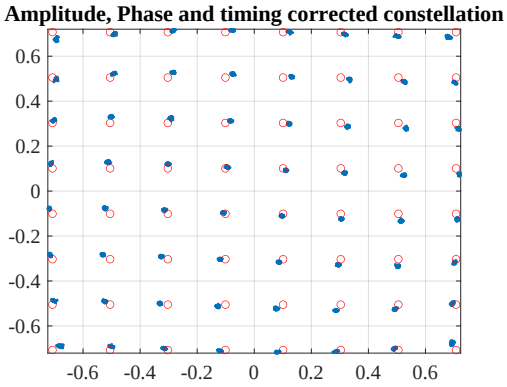
(a) Flat gain function with classic drain modulation and target of 9.5 dB gain.



(b) Flat gain function with PET and target of 9.5 dB gain.



(c) Flat gain function with classic drain modulation and target of 10.4 dB gain.

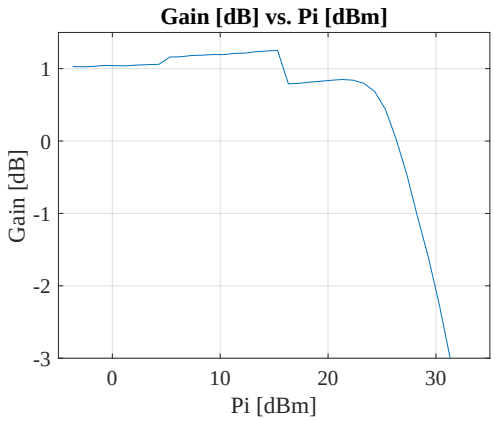


(d) Flat gain function with PET and target of 10.4 dB gain.

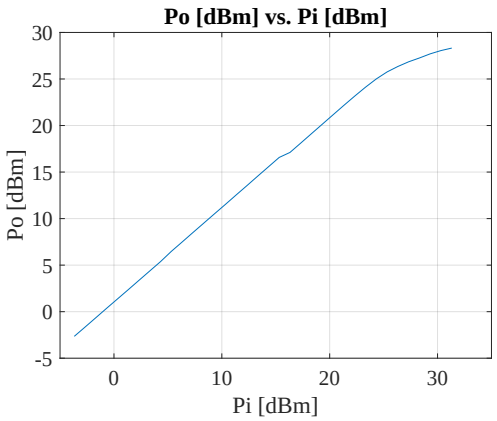
Figure 4.3.9: Constellation diagram for 64QAM signal.

Some distortion can be clearly seen in the 9.5 dB flat gain PET plot in 4.3.9b. The other three seem to be hitting the ideal symbol constellations quite well, even though the linearity numbers (STDR, ACPR, EVM) in Table 4.3.2 were not equally good as the ones in Table 4.2.3 for the 300 mA version of the vol. 2 PA.

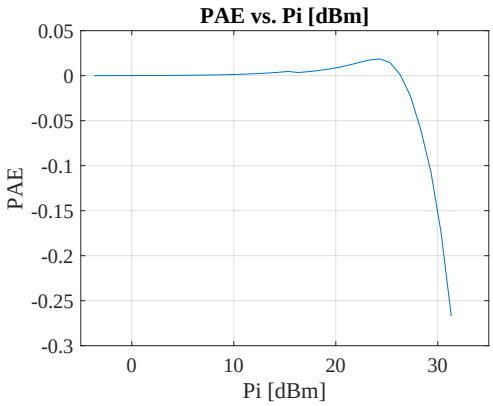
5.15 GHz The best match of the higher band was found at 5.15 GHz. Figure 4.3.10 shows key points of the PA's large-signal behavior at this frequency.



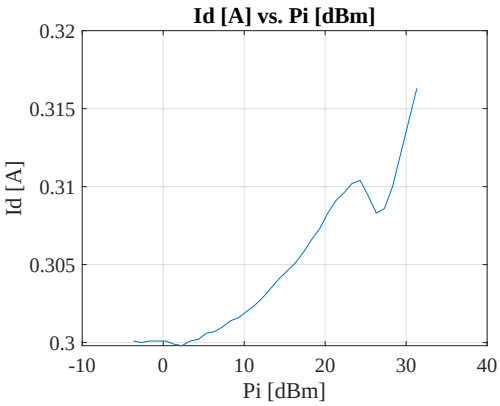
(a) Gain vs. input power.



(b) Output power vs. input power.



(c) PAE vs. input power.



(d) Drain current vs. input power.

Figure 4.3.10: Results of sweeping the input power with the frequency set to 5.15 GHz.

When looking at the results in Figure 4.3.10 it is clear that the amplifier performs much worse at 5.15 GHz compared to what it did at 2.3 GHz. Figure 4.3.10a shows that the gain is only 1 dB up until the input power reaches about 23-24 dB, where it starts to drop and eventually goes negative, dB-wise. Figure 4.3.10b indicates that the output power is almost equal to the input power up to a certain level, as expected from the gain curve. Figure 4.3.10c tells about a PAE close to zero.

With the results above from the input power sweep, it was decided to be unnecessary to move on with further tests of the PA at 5.15 GHz.

5 Discussion

In the previous section, the results of the performed measurements were presented. In this section, these results will be interpreted and discussed.

The Vol. 1 PA did not fulfill the specifications proposed and measures were taken to better this in the second revision. In this revision, the performance improved in all metrics and the device worked well when being both regularly drain modulated and run with PET as well. The next step was then to further develop the design by making it able to amplify two specified frequencies. This worked somehow in simulations but when later testing the physical device, the higher frequency band showed practically no gain. The lower band, however, showed gain and linearity close to the specifications.

The results showed that it is possible to use the chosen transistor in a one-stage PA configuration with single-stub matching networks to amplify 2.3 GHz QAM signals. This should also be the case for 2.4 GHz, if including knowledge about the frequency shift in the design process. It was confirmed that both regular drain modulation and PET as efficiency-enhancing techniques do work for a GaAs-centered device with lower gain and output power than what usually is in, e.g., technologies using GaN, and that they can maintain, or in some cases even improve the linearity measures.

The dual-band PA seemed to be without a problem amplifying 64QAM signals and thus, this should be no problem for the second revision device either. As this showed even better performance in all measures focused on. There were also performed tests, not included in this thesis, with the dual-band PA amplifying even higher-order QAM signals, which seemed promising. So especially if sticking to the 2.4 GHz band, the transistor proposes interesting behavior for use in an efficiency-focused system amplifying modulated signals.

The results are in line with the existing theory regarding the effects of the efficiency-enhancing techniques used and also how operating the PAs in different classes impacts their performance both gain- and efficiency-wise. What is worth considering to review might be the chosen transistor's performance at higher frequencies, above 5 GHz. According to its datasheet, it should be able to deliver 10 dB all the way up to 6 GHz and the simulations also showed considerable gain. With the measurements being significantly different from both these observations, a review of the model or using a different transistor might be of interest.

5.1 Power Amplifier, vol. 1

The first version of the PA showed performance quite far away from what was desired. It was able to deliver 30 dBm peak output power but delivered neither sufficient gain nor PAE numbers close to what should be possible. One of the reasons for this was likely that too narrow transmission lines were used for the signal paths between the input port and the transistor and between the transistor and the output port. Instead of using the calculated with for a 50 Ω transmission line as a starting point and then letting this be an optimizable variable with relatively tight limits together with the other parameters. Thus, it is believable that the characteristic impedance of the transmission lines was greater than it should have been and as a result introduced unwanted losses. Another possible reason for the PA not performing as desired was the transistor model used. During the design process, only S-parameters for two different bias configurations were available, and no large-signal model. It was not until the design was finished that the transistor became available for measurements and Morten Olavsbråten was available to create a new, improved model based on these.

5.2 Power Amplifier, vol. 2

5.2.1 300 mA Version

The performance of the second revision of the PA improved significantly from the first revision. Reasons for this might be the factors mentioned above about why the first revision did not perform very well. Having a large-signal model made it possible to perform more reliable large-signal simulations and subsequently optimizations, including gain up to certain power levels, the achieved output power, and the achieved PAE.

Gain-wise, both the S-parameter and the power sweep measurements showed gains above 11 dB. The dynamic measurements using the tracker showed a gain above 12 dB in the static mode and, depending on the tracking function used, somewhat lower for the other modes. The reason for the gain to increase when using the tracker might have been that the dynamic drain voltage led to a more dynamic drain current, resulting in a lower temperature of the device. It might also have had an impact that the larger capacitors in the drain bias network were removed upon attaching the connection pins for the tracker.

The gains of both measurement configurations were higher than what was simulated, suggesting the model was a bit conservative. The achieved numbers were within the specified demands of at least 10 dB gain up to 30 dBm output power and showed very flat gains of $\sim$10.3 dB and $\sim$11.5 dB were achieved through the entire power region when testing both regular drain modulation and PET for flat gain. This was done over an input power region spanning 15 dB with an average output power of $\sim$23.5 dBm and $\sim$22.9 dBm, respectively. Other linearity metrics, in addition to the flatness of the gain, showed good performances. The total change in phase was close to or below 5° throughout the entire tested power region for all four of the abovementioned configurations tracking for flat gain. Three out of the four had EVM values below 2 %, ACPR below -40 dBc, and STDR above 30 dB, when tested with a 16QAM signal. Thus, showing good promise of being able to handle higher-order modulation schemes. Regarding the ACPR values, ACPRh often had a higher value than ACPRl, which may have been caused by memory effects in the tracker. Thus, it might be that even better linearity could have been achieved if eliminating these.

Considering the PAE, one reason for the increase in the static power sweep measurements, compared to the first revision, was believably lower losses due to a more suitable transmission line width being used for the input and output paths. In addition to this, a more precise model would naturally lead to abilities to create better bias and matching networks. As well, the already mentioned higher gain will also contribute to a higher PAE if the drain efficiency is maintained, as shown in (2.5.11). When comparing the PAE numbers of the two revisions, the first revision achieved a peak PAE of just above 25 % at 2.0 GHz, and the second revision a peak PAE of almost 50 % at 2.3 GHz, which is a big improvement. Tracking the drain voltage made it possible to achieve average PAEs of 25 and 29 % when tracking for max. PAE but in these cases the linearity was compromised. Average PAEs of 19-20 % and 14-15 % were achieved with the linearity very much intact. Still a significant improvement from the 8 % achieved with similar output power and slightly higher gain in static operation.

One factor not mentioned in the results is stability. No oscillations were experienced but the high gain in the lower frequency spectrum, shown both in simulations and measurements, suggests that there is a possibility of oscillations if a 180° loop is created through the cables and the other equipment.

5.2.2 50 mA Version

For the 50 mA version, it was decided to increase the drain current at $V_D = 8$ V from 50 to 65 mA. This was due to limitations of the tracker, where its output voltage became unstable, dropping quickly when moving below the region of 2.8-2.9 V. Even though the increase in drain current was not huge, it may be that the performance would have improved if either the PA design was done with an aim of 65 mA drain current instead of 50 mA or if the tests were performed with a tracker being able to stably move even lower in output voltage.

Lowering the gate bias voltage closer to the threshold confirmed that moving the amplifier from operating in class A into operating more as a deep class AB variant, increased the efficiency significantly. From a PAE of 19-20 % at ∼23.5 dBm average output power with just above 10 dB gain when operating in class A, to a PAE of 41-42 % at ∼23.2 dBm output power with 9 dB gain. Including both the regular drain modulation and the PET configuration. That is more than double the PAE at comparable output power and gain levels, which leads to about half the DC power needed to perform the transmission. This was done with the same 16QAM signal, while still maintaining EVM values below 2 %, ACPR below -40 dBc, and STDR above 30 dB. It is also worth mentioning that these linearity numbers show an increase in performance compared to the numbers achieved with the PA operating in static mode, at the same time as the average PAE was increased from 22 % to 41-42 %. Tracking for a lower flat gain showed an even better PAE of 50 % but here the gain was below 7 dB and with impairment of the linearity. Thus, showing a lesser overall performance.

5.3 Power Amplifier, vol. 3, Dual-Band

One thing to notice is that again the optimal frequencies gain-wise have shifted a bit down. From 2.4 GHz to about 2.3 GHz for the lower band and from 5.2 GHz to about 5.15 GHz for the higher band. This can be acceptable for a prototype, where some simulation parameters are not exact, and as well the PCB arrived without any copper or solder layer on the underside, which led to the copper tape being used to minimize the effect of this. However, the most important thing to notice is the drop in gain from the simulated to the measured values for the higher frequency band. From a simulated S_{21} of 8.19 dB to a measured S_{21} of 1.15 dB. The same behavior was reflected in the large-signal simulations and measurements. A question to look at regarding this is whether the model described the device correctly in this higher-frequency region. If it did, a different transistor will be needed to realize the dual-band PA operating at 2.4 and 5.2 GHz. If a change to the model is the solution, the transistor might still be a good alternative. It might also be a solution to first create a single-band PA working in the higher frequency band to investigate the transistor's performance here.

At 2.3 GHz the dual-band PA showed some reduced performance compared to the second revision PA. One reason for this is the inclusion of another frequency to amplify making it more complicated to create a good match. Another one is the intent of suppressing the gain at lower frequencies to increase stability, as this might introduce additional losses, making it harder to achieve higher gain and efficiency at higher frequencies as well. One solution that maybe could have been better here is to only have reduced the capacitances of the RF transistors, instead of both doing this and including optimization goals for the avoidance of matching, low gain, and low output power at lower frequencies.

However, the PA still showed a satisfying gain at 2.3 GHz and very good linearity when no tracking was applied. The PAE was significantly lower than what was the case for the second revision operating in the same amplifier class. Applying tracking to the drain voltage resulted in increased

PAE but lower linearity. Still, the linearity was good enough to seemingly be able to transmit a 64QAM when using the tracking functions showing EVM values below 4 %, ACPR below -37 dBc, and STDR of 28 dB or above. This also confirms that the second revision should have no problem amplifying modulations of a higher order than 16QAM, as both the 300 and the 50 mA version showed even better linearity than the numbers highlighted here in the dual-band PA case.

6 Future Work

In a further development, the natural first step is to identify whether it was the transistor model or the limitations of the transistor itself causing the discrepancy between the simulated and measured performance at 5.2 GHz. If it is the model, a new model, more precise at this frequency, is needed. If measurements further of the transistor show that it is not able to provide sufficient gain at these frequencies, a different transistor will be the solution.

To maintain better performance it might be an idea to not include the restrictive goals for the lower frequencies but rather just use RF capacitors with lower capacitance to achieve stability. The second revision did not show any tendencies of oscillation, so this might be a good compromise between stability and performance.

When designing the new dual-band networks, an idea will be to first find load-pull contours for both frequencies, in order to identify the impedance region where the PA is able to provide sufficient output power in both frequency bands. And then use this as a starting point for further optimization. This can be done for both single- and double-stub networks. It is also an idea to investigate more complex network structures. As the final goal is to be able to use the PA with an IoT device it should be looked at solutions using capacitors and inductors as well, considering area constrictions.

Using different matching techniques can also be an opportunity for further development of the second revision, which worked well, but has the possibility of fitting in a more compact design. This would be useful to explore if it is desired to place the PA in a device transmitting signals with up to 30 dBm output power.

An increase in stability, while still maintaining the same performance, is also an area possible to explore for the second revision. Where an idea for the first step, as mentioned for the dual-band PA above, is to just replace the RF capacitors with smaller ones and do a slight readjustment of the networks to fit with these.

Further on, it should be explored for the second revision how far up the QAM scheme orders it is able to perform, considering the linearity shown in the 16QAM measurements.

Then, for both the 2.4 GHz only and the dual-band version, it is of interest to actually test together with the nRF7002 chip to see how the system as a whole will perform and to identify the performance compared to existing solutions used with the chip.

7 Conclusion

This thesis has investigated the efficiency-enhancing technique of drain modulation, both in the form of regular drain modulation and in the form of PET, on a PA amplifying RF signals with a frequency of 2.4 GHz. In addition to this, it was looked at a dual-band solution intended to amplify both 2.4 and 5.2 GHz signals, as the nRF7002 chip communicates in these two bands.

A PA has been created in three revisions, using the built-in tools of ADS, where the first revision was a final realization of the thesis' already completed pre-work, the second revision was designed as two versions individually optimized for drain currents of 300 and 50 mA, and the third revision was designed as dual-band PA, suitable for amplifying both the above-mentioned frequencies. For the second revision and the lower band of the third revision, the amplified frequency skewed down to 2.3 GHz. The higher band of the third revision moved to 5.15 GHz.

Measurements were performed, indicating that both the devices from the second revision are suitable to amplify QAM signals of order 16 and even higher. Their response to drain modulation and PET showed promising results for the technique to be used for efficiency-enhancing when amplifying modulated signals, with PAE numbers approx. doubling or more from 8 % to 14-15 % or 19-20 %, depending on the tracking function, for the 300 mA version, and from 22 % to 41-42 % for the 50 mA version. In both cases with relatively comparable gains and output powers between the static and the tracked configurations.

The dual-band showed performances not as good as the ones of the single-band versions in the second revision. Where it, in the lower frequency band, provided a quite similar gain but lower PAE and less linearity. Both when operating in a static configuration and when its drain voltage was tracked. In the higher frequency band, it showed more or less no gain. Thus, eliminating the reason to perform any tracking, and for looking at PAE and linearity values, in this frequency band.

The results suggest it is worth looking further into the use of drain modulation as an efficiency-enhancing technique for signals with the frequencies and power explored here. A new revision of the dual-band PA should be created to be able to test the technique at both frequencies of interest.

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