Bjørn Kristian Eid

Two-Stage Power Amplifier With Interstage Mismatch and Envelope Tracking for Improved Linearity and Efficiency

Master's thesis in Electronic Systems Design
Supervisor: Morten Olavsbråten
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Abstract

The foundation for this thesis is to explore the use of a driver amplifier in series with a power amplifier. Where mismatching the interstage matching network and envelope tracking the power amplifier is used to improve linearity and efficiency, by achieving flat gain and phase. Using envelope tracking to accomplish flat gain at the cost of large phase variation, is a well-established technique. However, mismatching an interstage network to reduce phase variation is not well-established.

The proposed two-stage power amplifier is a discrete implementation simulated in Keysight Advanced Design System (ADS) to confirm wanted behavior, a layout is then created such that the amplifier can be produced on a printed circuit board (PCB), the produced circuit board is then measured at NTNU's RF-laboratory. The two-stage power amplifier uses gallium nitride (GaN) high-electron-mobility transistors (HEMT) from Wolfspeed as active devices. The driver amplifier uses the 10 W CG2H40010 transistor, while the power amplifier uses the 25 W CG2H40025 transistor.

The two-stage power amplifier, with a slight mismatch and envelope tracked for a flat gain of 14.1 dB, achieves an average output power of 37.2 dBm with a peak-to-average power ratio of 7.2 dB, giving a peak output power of 44.4 dBm. The average power-added efficiency is 33.1 %, while the gain ripple is less than 0.5 dB, and total phase variation is less than 2.8°. The 15.5 dB flat gain tracking achieves an average power-added efficiency of 30.1 %, and a gain ripple of less than 0.5 dB while the total phase variation is less than 3.4°.

Sammendrag

Utgangspunktet for avhandlingen er å utforske bruken av en driver-forsterker i serie med en effektforsterker. Hvor mismatch i matchenettverket mellom forsterkertrinnene, og envelope tracking av effektforsterkeren er brukt til å forbedre linearitet og effektivitet, slik at flat forsterkning og fase er oppnådd. Det å bruke envelope tracking for å oppnå flat forsterkning på bekostning av stor fasevariasjon er en svært etablert teknikk. Derimot, mismatch av matchenettverket mellom forsterkerne for å redusere fasevariasjon er ikke svært etablert.

Den foreslåtte to-trinns effektforsterkeren er en diskre implementasjon som er simulert i Keysight Advanced Design System (ADS) for å bekrefte ønsket oppførsel, et layout er deretter lagd slik at forsterkeren kan bli produsert på et kretskort. Det produserte kretskortet er deretter målt ved NTNU's RF-laboratorium. To-trinns effektforsterkeren bruker gallium-nitrid (GaN) high-electron-mobility transistorene (HEMT) fra Wolfspeed som aktive enheter. Driver-forsterkeren bruker en 10 W CG2H40010 transistor, mens effektforsterkeren bruker en 25 W CG2H40025 transistor.

Når to-trinns effektforsterkeren har litt mismatch, og er envelope tracked for en flat forsterkning på 14.1 dB, så oppnår forsterkeren en gjennomsnittlig utgangseffekt på 37.2 dBm med en peak-to-average power ratio (PAPR) på 7.2 dB. Dette gir en utgangseffekt som er 44.4 dBm ved toppen. Den gjennomsnittlige power-added efficiency (PAE) er 33.1 %, mens variasjonen i forsterkning er mindre enn 0.5 dB, og fasevariasjonen er mindre enn 2.8°. Trackingen for flat forsterkning på 15.5 dB gir en gjennomsnittlig PAE på 30.1 %, og en variasjon i forsterkningen som er mindre enn 0.5 dB, mens fasevariasjonen er mindre enn 3.4°.

Preface

The foundation for this thesis was set in the autumn semester of 2022, as a semester project that explored simulations of an ideal two-stage monolithic microwave integrated circuit (MMIC) amplifier architecture [1]. The work in this thesis was conducted in the spring semester of 2023, and is my last requirement before finishing my Master of Science degree at Norwegian University of Science and Technology (NTNU). The semester project and the Master thesis were both carried out at the Department of Electronic Systems, and supervised by Associate Professor Morten Olavsbråten.

I would like to thank Morten Olavsbråten for noticing and coming up with the idea that mismatching a driver amplifier could be used to improve the phase of a two-stage envelope tracked amplifier. Furthermore, I would like to thank him for the solid guidance throughout the whole process, from design to measurements at the laboratory. I would further like to extend my appreciation to fellow Master student Magnar Lundberg for productive conversations and discussions.

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Acronyms and explanations

ADS - Advanced Design System
ACPR - Adjacent channel power ratio
DUT - Device under test
ET - Envelope tracking
EVM - Error vector magnitude
FET - Field-effect transistor
HEMT - High electron mobility transistor
MESFET - Metal-semiconductor field-effect transistor
MMIC - Monolithic microwave integrated circuit
PA - Power amplifier
PAE - Power-added efficiency
PAPR - Peak to average power ratio
PCB - Printed circuit board
PET - Power envelope tracking
RF - Radio frequency
STDR - Signal to total distortion ratio
VNA - Vector network analyzer

1   Introduction

1.1   Background and motivation

An undesirable effect from using envelope tracking (ET) to achieve flat gain and enhanced efficiency, is that one ends up having a large phase variation. This phase variation and other nonlinearities can be adjusted for by using some digital linearization techniques. Based on work done in [1], it was shown that by mismatching the interstage matching network, one could achieve a phase that can counteract the undesired effect envelope tracking has on the phase. Therefore, by creating a discrete two-stage amplifier with a driver amplifier as the 1st stage, and a power amplifier as the 2nd stage, with a mismatched interstage matching network, one can achieve improved linearity. This possibly removes the need for digital linearization as linearity can be achieved solely through smart analog amplifier design.

A highly linear amplifier with a flat gain and phase is beneficial for use in systems that employ modulation techniques such as quadratic amplitude modulation (QAM). This is because of how binary data is modulated onto the signal. QAM modulates the signal with amplitude shift keying and phase shift keying, which makes constant gain and phase to be advantageous, since it would cause amplitude and phase variations to be minimal.

In this thesis a two-stage power amplifier will be designed, produced, and measured. The amplifier in the 2nd stage will employ techniques to enhance the efficiency, and introduce mismatch in the interstage matching network to improve linearity. The mismatch in the interstage network will be able to be adjusted to further determine the impact on linearity.

1.2   Scope of thesis

The thesis will only consider the tracking methods, envelope tracking and power envelope tracking. However, other methods have been included in the theory for completeness. The two specific transistors used in this thesis are Wolfspeed's CG2H40010 and CG2H40025, which are gallium nitride (GaN) High- Electron-Mobility Transistors (HEMT).

1.3   Structure of thesis

Section 2 presents necessary background information in the form of theory. It presents information regarding the transistors and materials. It provides some information surrounding important parts and parameters of power amplifiers. The section also explains different amplifier classes, while also presenting concepts of efficiency enhancement techniques. Most of the theory section is taken from the semester project [1], with some changes and additions.

Section 3 covers the design procedure of the two stages of the two-stage amplifier, which involves deciding operating point, and design of the bias networks, stability networks, and matching networks. The measurement setups in the laboratory are also explained in the end of this section.

Section 4 presents all the results obtained from the measurements and simulations. These results are presented in the form of graphs.

Section 5 discusses the results presented in Section 4, by comparing and commenting on what is seen in the figures. This includes comments on performance and how it compares to the requirements that have been set. Future work is also presented at the end of the discussion section.

Section 6 concludes the thesis with the important parts of what has been done, and essential results are summarized.

2 Theory

2.1 Field-effect transistors

Field-Effect Transistors (FETs) are considered monopolar, because they only have one carrier type (holes or electrons), that provide current flow through the device [2]. An n-channel FET will provide current flow by using electrons, while a p-channel FET provides current flow by using holes. FET devices are considered voltage controlled, because of their output current being controlled by the input voltage. [2]

There are different types of FETs, two of them are, Metal-Semiconductor FET (MESFET), and High Electron Mobility Transistor (HEMT). Gallium arsenide (GaAs) MESFETs can be used at frequencies up to 60 GHz, and is therefore commonly used in microwave circuits [2]. GaAs MESFETs and HEMTs are particularly beneficial for low-noise amplifiers, as they have a lower noise figure than other devices. Another recent development is the gallium nitride (GaN) HEMTs, which are preferable for high power RF amplifiers [2].

2.1.1 GaN HEMT

HEMTs are considered heterojunction FETs, because they are constructed with several layers of different semiconductor materials, instead of a single semiconductor material. By being constructed in such a manner, results in a higher carrier mobility compared to regular MESFETs [2]. GaN can achieve higher frequencies and higher power density than Si and GaAs, this is because of GaN having a wider bandgap and higher saturation velocity [3]. The isolation between the gate and the channel is usually created with aluminium gallium nitride (AlGaN). Such a construction allows for a larger current to flow from the source to the drain [3].

2.2 Power amplifiers

Power amplifiers are commonly found in radar and radio transmitters, as they are necessary to amplify the power to be radiated. They achieve this by converting the DC input power to some amount of RF output power. Output powers tend to vary from 1 mW for short-range wireless systems, up to 1 MW for long-range broadcasting transmitters. While other systems such as mobile communication may range from 100 to 500 mW. [2][4]

2.2.1 Matching networks

Power amplifiers experience power losses because of reflections caused by improper matching. The purpose of matching is to match one impedance to another, in order to avoid unnecessary loss of power. Proper matching can make sure that maximum power is delivered to the load. Matching networks can be made using either lumped components or transmission lines. [2] Matching networks can also be tuned and optimized such that the amplifier has the highest possible gain, or highest possible power-added efficiency.

When matching for maximum power transfer, the power theorem is employed, which states that maximum power occurs when the load resistance is equal to the source resistance [5]. This is quite simple for DC circuits, however, for AC circuits it is required that the load impedance, Z_L, equals the complex conjugate of the source impedance, Z_S. This can be seen in the circuit diagram in Figure 1. The circuit diagram shows a source impedance with a reactive component $+jX_S$ in series with a capacitive component $-jX_L$, which causes them to cancel each other. This leaves only the source and load resistances, which are equal by definition. [5] An impedance transformation as such, can also be done by using transmission lines.
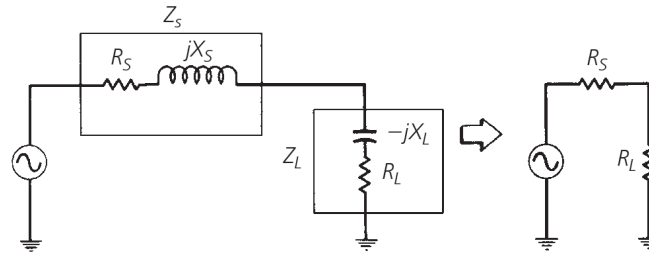
Figure 1: Circuit diagram showing complex conjugate matching and the resulting equivalent circuit. [5]

2.2.2 Bias networks

The purpose of bias networks is to make sure there is no leakage of RF power into the DC supply, and that there is no DC power affecting the RF inputs. This is because it would cause some interference, and may affect the performance of the amplifier. The building blocks to fulfill this requirement are known as DC blocks and DC feeds. Where the DC block is placed in series on the RF signal path, and the DC feed is located in series with the DC power supply.

The simplest of the two would be the DC block, as it would just be a capacitor. Because of the large frequencies used in microwave circuits, the capacitor will generally not affect the performance of the amplifier. It is however important to note that parasitic capacitances will affect the amplifier at certain frequencies. This is because as the frequency increases, the behavior of the capacitor can be affected.

The more complex building block is the DC feed. This one is more complex because it must block RF power from entering the DC supply, while also passing DC power to the gate and drain of the amplifier. This can be done according to the circuit seen in Figure 2. The circuit implements two $\lambda/4$ transmission lines, with the DC supply connected in between them, and the RF connected to the lower transmission line. The capacitors, C_L and C_S, are large and small respectively. This is beneficial as it will have improved attenuation of a broader range of frequencies. For the fundamental frequency, the transmission lines behave as an open circuit such that RF is unable to leak into the DC supply. Meanwhile, the DC supply connected in between the transmission lines will see a short circuit.
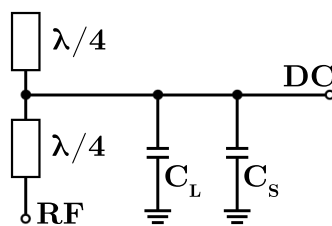
Figure 2: Circuit diagram of the DC feed network.

2.2.3 Efficiency

Efficiency is considered a critical factor when designing PAs. However, there are three common definitions of efficiency. Drain efficiency would be one of them, which is the ratio of RF output power to the DC input power. [4]

$$\eta = \frac{P_{out}}{P_{DC}} \tag{1}$$

Main drawback for this definition is that it does not consider the RF power that is delivered to the input of the PA. Added that most PAs have relatively low gains, then this definition might give higher efficiency than the actual efficiency. Therefore, a second definition which is called power-added efficiency might prove useful, as it includes the effect of the input power. This definition can also provide information on the gain, G. [2]

$$\eta_{PAE} = \frac{P_{out} - P_{in}}{P_{DC}} = \left(1 - \frac{1}{G}\right)\frac{P_{out}}{P_{DC}} = \left(1 - \frac{1}{G}\right)\eta \tag{2}$$

Another definition is by looking at the average efficiency, which is the ratio of the average output power to the average DC input power. This is useful since signals with time-varying amplitudes will have time-varying efficiencies. [4]

$$\eta_{AVG} = \frac{P_{out\_AVG}}{P_{DC\_AVG}} \tag{3}$$

2.2.4 Stability

For amplifiers, it is required that they are stable, in order to avoid oscillations. Oscillations can occur when $|\Gamma_{in}| > 1$ or $|\Gamma_{out}| > 1$. This is because the input and output reflection coefficients depend on Γ_S and Γ_L, which in turn depend on the load and source matching networks. There are two definitions of stability, unconditional and conditional stability. Unconditional stability is achieved when $|\Gamma_{in}| < 1$ and $|\Gamma_{out}| < 1$ for all load and source impedances. While conditional stability is achieved when $|\Gamma_{in}| < 1$ and $|\Gamma_{out}| < 1$ for a certain load and source impedances. [2]

The stability of a system can be checked by observing the μ-factor. The system is unconditionally stable if $\mu > 1$ for all frequencies, and larger values of μ implies a more stable system [2]. The definition of μ can be seen in Equation 4.

$$\mu = \frac{1 - |S_{11}|^2}{|S_{22} - \Delta S_{11}^*| + |S_{12}S_{21}|} > 1 \ , \qquad \Delta = S_{11}S_{22} - S_{12}S_{22} \tag{4}$$

2.2.5 Linearity

A perfectly linear amplifier would have a transfer characteristic, gain, that is completely linear, such that the output power is the input power multiplied by the gain [6]. However, in reality, as the input signal power increases the output signal power will start saturating because of gain compression. This effect will distort the signal, and cause a nonlinear amplification.

Some measures of linearity that are commonly used when analyzing modulated signals are, Adjacent Channel Power Ratio (ACPR), and Error Vector Magnitude (EVM). Another measure that has been proposed by D. Gecan, et al. is Signal to Total Distortion Ratio (STDR), which is a figure of merit for linearity evaluation [7]. These will be described below.

Adjacent channel power ratio
Adjacent channel power ratio is a measure of linearity that shows how much of the signal that spreads into adjacent channels [6]. The definition of ACPR is the ratio of the power within the adjacent channel, and the power within the main channel. As shown by Equation 5, and visualized in Figure 3. [3]

$$ACPR = \frac{P_{adjacent}}{P_{main}} \tag{5}$$
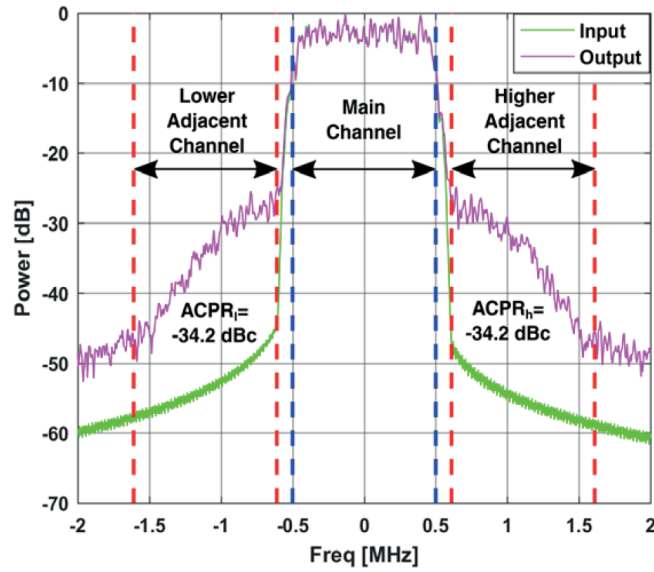
Figure 3: Adjacent channel power ratio for the neighboring channels of the distorted output 1 MHz 16-QAM signal. [3]

Error vector magnitude

Error Vector Magnitude (EVM) is a useful parameter when analyzing signals using quadrature amplitude modulation (QAM) as its modulation scheme. This is because EVM evaluates the error in the amplitude and phase of the signal, by creating an error vector as seen in Figure 4. [3] The formula to calculate the EVM for a kth symbol in a signal sequence of N symbols can be seen in Equation 6. Where I_k is the in-phase value of the kth symbol, and Q_k is the quadrature phase value of the kth symbol [3].

$$EVM_k = \sqrt{\frac{e_k}{\frac{1}{N} \sum_{k=1}^{N} \left(I_k^{ref2} + Q_k^{ref2} \right)}} \cdot 100 \tag{6}$$

$$e_k = (I_k^{ref} - I_k^{meas})^2 + (Q_k^{ref} - Q_k^{meas})^2 \tag{7}$$
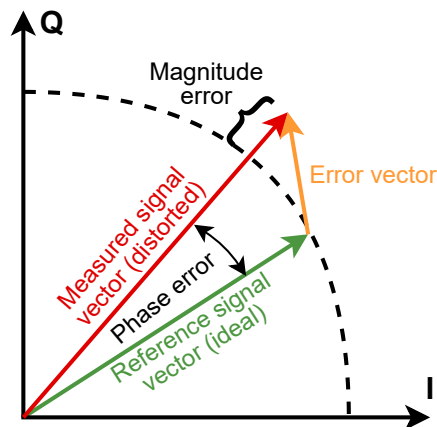
Figure 4: Error vector magnitude (EVM) illustration. [3]

Signal to total distortion ratio
STDR is a figure of merit proposed by Gecan et al. which can be used for linearity evaluation. The formula can be seen in Equation 8, where I_a, I_b, and I_x are integrals. The average input power is given by I_a, the average total output power is I_b, and I_x is twice the power of the baseband signal [7]. A maximized STDR will happen when the nonlinear power is minimized and the linear power is maximized. Where a minimized nonlinear power will assure a linear power amplifier, and a maximized linear power will assure high output power. How the figure of merit is derived and verified is explained thoroughly in [3] and [7].

$$STDR = 10log\left(\frac{I_a I_b}{I_a I_b - |I_x|^2}\right) [dB] \tag{8}$$

2.3   Amplifier classes

When creating power amplifiers it is important to know the different amplifier classes and their bias points, such that one can implement the class that is adequate for a specific use case. The current-voltage characteristics (IV-curves) of the CG2H40010 GaN HEMT can be seen in Figure 5, and is fundamental when deciding the class of operation.
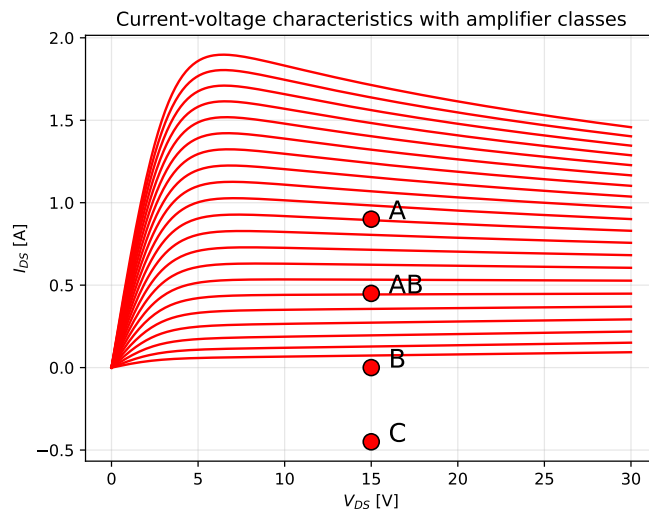

Figure 5: Current-voltage characteristics with embedded bias points for different amplifier classes.

2.3.1   Classes A, AB, B and C

Classes A, AB, B and C are inherently similar, where the main difference between the classes is the conduction angle, α. The class A amplifier is biased in the middle of the IV-curves, which can be seen in Figure 5. This causes the conduction angle to be $\alpha = 2\pi$, which represents a full period of the signal. Since it is conducting during a whole period, the theoretical maximum drain efficiency becomes $\eta = 50\%$ [6].

As one move downwards on the IV-curves, the conduction angle becomes smaller. The class B amplifier is biased at the bottom of the IV-curves, meaning that it only conducts during one half of the signal period, causing the conduction angle to be $\alpha = \pi$. Meanwhile, the theoretical maximum drain efficiency is $\eta = \pi/4 = 78.5\%$ [6].

The area between class A and B is where a class AB amplifier is biased. Which leads to the

conduction angle being $\pi < \alpha < 2\pi$, and the drain efficiency is $50\% < \eta < 78.5\%$. Class AB amplifiers are considered a compromise between class A and B, as it will have less distortion than a class B, but higher than class A [6]. As seen from the drain efficiency, class AB will be less efficient than class B, but more efficient than class A.

From Figure 5 it can be seen that a class C amplifier is biased below the IV-curves. Therefore, class C amplifiers are biased below the threshold for conducting current, which results in a conduction angle that is less than half a period, $\alpha < \pi$. As the conduction angle decreases toward zero, the theoretical efficiency increases toward 100%. However, this decreases the output power, while the drive power increases toward infinity. The point in the figure is only for visualization, and does not mean that the amplifier has a negative current. [4]

2.3.2   Classes D, E and F

Compared to the analog amplifier classes A, B and C, the classes D and E deviate from being purely analog and can be considered as a more digital approach since they behave as switches. A class D amplifier that has a perfectly ideal switch would have an efficiency of 100%, because of no losses in the switching [6]. It uses two or more transistors such that a square wave drain voltage can be generated. On the output there is a series resonance filter such that only the fundamental frequency component is delivered to the load. [4]

The class E amplifier is similar to D, but E has a shunt capacitor placed in parallel with the transistor. A class E achieves an output voltage based on the sum of the DC and RF currents that charge the shunt capacitor. In an optimal class E amplifier, the output voltage is zero just as the transistor is turned on, resulting in an ideal efficiency of 100%. [4]

A more complex amplifier is the class F, as it implements harmonic resonators at its output to harmonically tune the amplifier. Such an amplifier can be made using the classes A through C, however, AB and B are commonly used. The added odd harmonics cause the output voltage to approximate a square wave, while the even harmonics approximates a half sine wave current. The harmonic resonators can be replaced by a $\lambda/4$ transmission line. This causes a short circuit for all even harmonics, and an open circuit for all odd harmonics. [4][6]

2.4   Smith chart

The Smith chart is a central tool when working with RF and power amplifiers, as matching is important to reduce losses and maintain performance of PAs. A Smith chart can represent the impedance as seen from a source at a specific frequency. The impedances on a Smith chart are normalized with a normalization constant that is usually the characteristic impedance [2]. Furthermore, complex impedances can be displayed, where the x-axis is the real component, and y-axis is the complex component. The upper half is positive complex values, and the lower half is negative complex values, which would be considered capacitive and inductive respectively. The Smith chart can be used to create matching networks as one can move along the lines in a manner that represents some specific transmission line or lumped component.
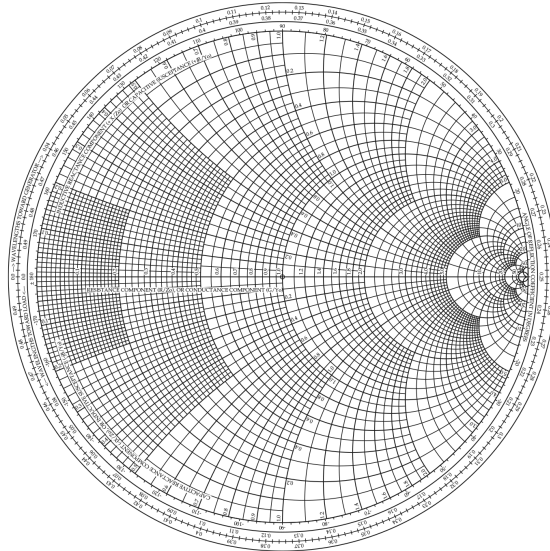
Figure 6: The Smith chart. [2]

2.5   S-parameters

S-parameters are necessary when analysing performance of microwave circuits, as they provide information on reflections and power transfer. For microwave circuits there can be created a scattering matrix with S-parameters that describe the incident and reflected waves on the ports. The scattering matrix that describes the two-port network in Figure 7, can be seen from Equation 9.

$$\begin{bmatrix} b_1 \\ b_2 \end{bmatrix} = \begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} \begin{bmatrix} a_1 \\ a_2 \end{bmatrix} \tag{9}$$

The equations for b_1 and b_2 can be derived from the scattering matrix in Equation 9, or through signal flow graph analysis based on the signal flow graph seen in Figure 7b. The derived equations can be seen in Equation 10.

$$b_1 = S_{11} \ a_1 + S_{12} \ a_2$$
$$b_2 = S_{21} \ a_1 + S_{22} \ a_2 \tag{10}$$

Further analysis can be done such that an expression can be derived for the input reflection coefficient, Γ_{in}, and the output reflection coefficient, Γ_{out} [2].

$$\Gamma_{in} = \frac{b_1}{a_1} = S_{11} + \frac{S_{12}S_{21}\Gamma_L}{1 - S_{22}\Gamma_L}$$

$$\tag{11}$$

$$\Gamma_{out} = \frac{b_2}{a_2} = S_{22} + \frac{S_{12}S_{21}\Gamma_S}{1 - S_{11}\Gamma_S}$$

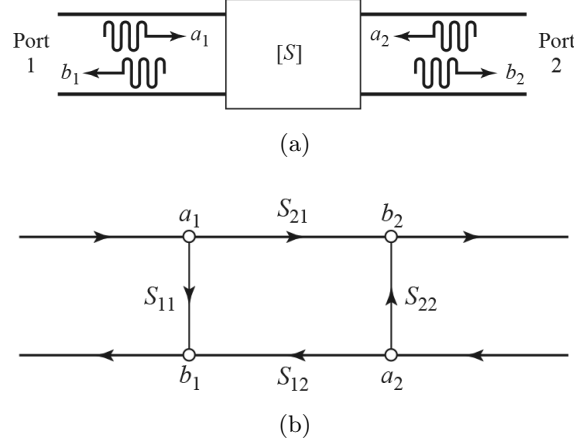Figure 7: A two-port network showing the dependence between the ports and the S-parameters. (a) Definition of incident and reflected waves. (b) Signal flow graph. [2]

2.6 Efficiency enhancement techniques

2.6.1 Envelope tracking

Envelope tracking (ET) uses the envelope of the signal to control the drain voltage of the amplifier. This is done in such a way that the drain voltage of the amplifier is reduced when the envelope of the input signal is small. By having the drain voltage follow the envelope, reduces the power consumption when the envelope is small, which results in an enhanced average efficiency. This is because it allows the amplifier to operate close to saturation for all input signals. The RF amplifier used in such a system can be either class A, AB or B. [6]

An important factor to consider when using ET, is the bandwidth of the input signal that is to be tracked. If the input signal has a bandwidth, B_{RF}, and a baseband signal, $v_s(t)$, that is a complex modulated time varying signal with a baseband bandwidth as given by Equation 12. [8]

$$v_s(t) = v_I(t) + j \cdot v_Q(t) \;\; \rightarrow \;\; W_{BB} = \frac{B_{RF}}{2} \tag{12}$$

While the drain voltage being shaped as a function of the envelope signal in Equation 13, results in a bandwidth that is theoretically infinite, which is because of the square root function. [8]

$$v_{d,env}(t) \propto v_{s,env}(t) = |v_s(t)| = \sqrt{v_I^2(t) + v_Q^2(t)} \;\; \rightarrow \;\; W = \infty \tag{13}$$

2.6.2 Power envelope tracking

A further development of the envelope tracking technique is the power envelope tracking (PET) technique, which was proposed by Olavsbråten et al. in [8]. The main reason for this technique is to reduce the required drain voltage bandwidth of an envelope tracked amplifier. This is done by creating a tracking function that follows the power of the envelope, which can be realized by assuming that the bandwidth of the input signal is $B_{RF} = 2W_{BB}$. With this as a basis, the drain voltage can be shaped from the power of the envelope, and is shown in Equation 14. [8]

$$p_{env}(t) = v_s(t) \cdot v_s^*(t) = v_{s,env}^2(t) \;\; \rightarrow \;\; W = B_{RF}$$
$$\Rightarrow v_d(t) = a_0 + a_2 \cdot v_{s,env}^2(t) = a_0 + a_2 \cdot p_{env}(t) \tag{14}$$

The PET technique will not perfectly follow the envelope of the signal, which will result in a slightly lower efficiency than perfect ET. However, the loss in efficiency can be mitigated by using power of higher orders, such that the function follows the envelope more. In Equation 15 one can see a 2nd order PET, which will have a bandwidth twice as large. However, the efficiency will be increased compared to a 1st order PET. [8]

$$
\begin{aligned}
v_d(t) &= a_0 + a_2 \cdot v^2_{env}(t) + a_4 \cdot v^4_{env}(t) \;\rightarrow\; W = 2 \cdot B_{RF} \\
v_d(t) &= a_0 + a_2 \cdot p_{env}(t) + a_4 \cdot p^2_{env}(t)
\end{aligned}
\tag{15}
$$

2.6.3   Doherty

Another efficiency enhancement technique is the Doherty technique, which is considered as an active load-pull technique. The principle of doherty architecture is to split the signal, and feed the signal into two amplifiers in parallel. The architecture functions such that both amplifiers contribute to the output, until the power is 6 dB less than the maximum power. At this point, the auxiliary amplifier is shut down and no longer contributes to the output. One important concept is that when the auxiliary amplifier is conducting, the load impedance of the main amplifier will be affected. This behavior has to be counteracted by inserting a $\lambda/4$ transmission line at the output of the main amplifier, such that it experiences active load modulation. This transmission line will cause a time delay, therefore, another $\lambda/4$ transmission line must be inserted in front of the auxiliary amplifier to compensate for the added time delay. Such a configuration can be seen in the circuit diagram in Figure 8. [6][9]
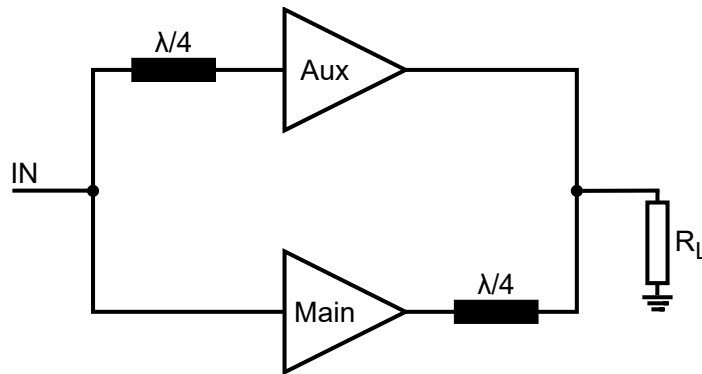
Figure 8: Doherty amplifier circuit diagram.

2.6.4   Chireix outphasing

The Chireix outphasing enhancement technique uses two similar power amplifiers, that both operate at the same fixed power level. These two power amplifiers can be nonlinear, which differentiates it from the Doherty technique which requires linear amplifiers. The outphasing technique can be easily explained by a trigonometric identity: [9]

$$
cos(A) + cos(B) = 2cos\left(\frac{A+B}{2}\right) \cdot cos\left(\frac{A-B}{2}\right)
\tag{16}
$$

By using a phase modulator on an amplitude modulated signal $S_{in}(t)$, it is possible to create two equal signals that have a fixed amplitude, $S_1(t)$ and $S_2(t)$, such that if

$$
S_{in}(t) = A(t) \cdot cos(\omega t)
\tag{17}
$$

then

$$S_1(t) = cos\Big(\omega t + cos^{-1}\big(A(t)\big)\Big)$$
$$S_2(t) = cos\Big(\omega t - cos^{-1}\big(A(t)\big)\Big)$$

(18)

The combined output, if the amplifiers have a gain of G, becomes

$$S_{out}(t) = G \cdot \big(S_1(t) + S_2(t)\big)$$
$$= 2 \cdot G \cdot A(t) \cdot cos(\omega t)$$

(19)

This explaines that the main purpose of an outphasing power amplifier is to create two constant amplitude input signals which have the information of the amplitude modulation embedded as a differential phase shift [9]. This causes the two signals to be able to be amplified by a nonlinear amplifier, and the amplitude modulation can be retrieved by a summing operation. [9]

3   Method

In this chapter it is explained how the driver and the power amplifier were designed by the use of the design, simulation, and layout program, Keysight Advanced Design System (ADS). The two amplifiers are both designed with a FR-4 type substrate in mind, specifically the IS400 substrate. The characteristics of the IS400 substrate can be seen in Table 1. The design methodology is similar to what was done in the semester project [1]. However, it is designed with regards to a discrete architecture instead of MMIC.

Table 1: Characteristics of the IS400 substrate

Parameter	Value
H	1.473 mm
ϵ_r	4.46
Cond	$5.8 \cdot 10^7$ S/m
Hu	$1 \cdot 10^{36}$ mm
T	35 μm
TanD	0.019

Table 2: Requirements for the driver and power amplifier

Parameter	Value
Fundamental frequency	3.9 GHz
Bandwidth	> 10 %
Gain	$> 10\ dB$
Output power	$> 43\ dBm$
Efficiency	As large as possible

The requirements that were set for both the driver and power amplifier can be seen in Table 2, above. These requirements will be the foundation for the design choices being made. A simple circuit diagram showing the proposed two-stage amplifier architecture can be seen in Figure 9. The figure shows a smaller driver amplifier in series with a larger power amplifier, these are 10 W and 25 W respectively. The power amplifier will have a drain tracker such that envelope tracking and power envelope tracking can be employed.
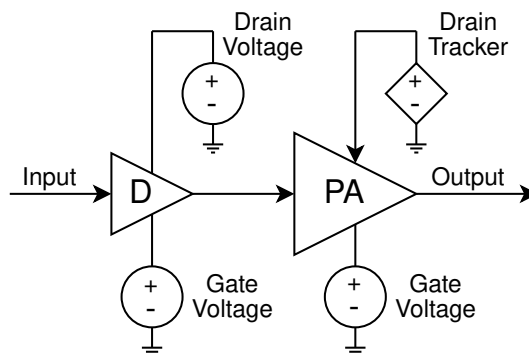

Figure 9: Proposed two-stage amplifier architecture. [1]

3.1   Design of the 10 W driver amplifier

The design process for the 10 W driver amplifier will be described in this section. This will include choice of biasing, design of the stability network, bias network, and matching networks. The driver amplifier uses a 10 W GaN HEMT transistor from Cree, specifically the CG2H40010 transistor.

3.1.1   Class of operation

First of is to decide the class of operation for the amplifier, which involves deciding the operating point of the amplifier. The datasheet for the transistor gives typical operating points for both the gate voltage and the drain voltage. The gate voltage is typically between -3.6 V and -2.4 V, and the drain voltage is 28 V. It is important to check the current-voltage characteristics (IV-curves) of the transistor, to gain insight into the biasing current at different operating points. This can be done by simulating the transistor, and sweeping both the gate and drain voltages. The IV-curves of the CG2H40010 transistor can be seen in Figure 10.
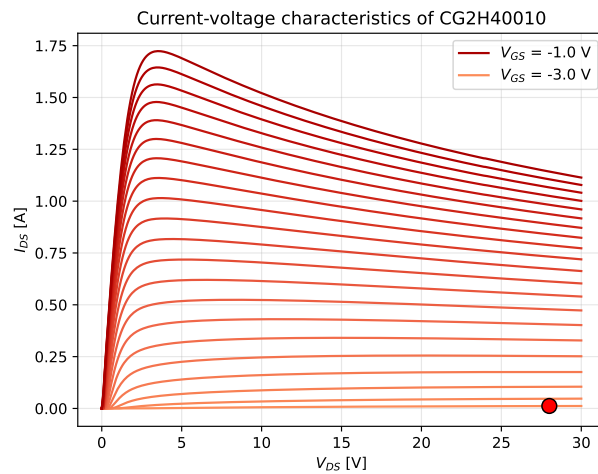

Figure 10: Current-voltage characteristics of the 10 W, CG2H40010, transistor.

Since efficiency, linearity and output power are important parameters, it is decided to bias the amplifier such that it operates as a class-AB amplifier. From the semester project [1], it was discovered that biasing the driver amplifier deep into class-AB, almost B, was beneficial for a phase that has a declining slope. Therefore, $V_{GS} = -3.0\ V$ and $V_{DS} = 28\ V$ is chosen as the desired operating point, which results in a biasing current, I_{DS}, of 12.1 mA.

3.1.2   Stability network

After the class of operation and operating point have been decided, it is imperative that the amplifier is stable for all frequencies. If the amplifier is not stable for all frequencies, it is possible that it will oscillate at specific frequencies. As stated in Section 2.2.4, one can inspect the μ-factor, and see whether it is larger than 1. If it is larger than 1 for all frequencies, then the amplifier can be considered unconditionally stable. From Figure 11 one can see that both μ_{source} and μ_{load} are less than 1 for the lower half of the frequency range, thus the amplifier is conditionally stable.
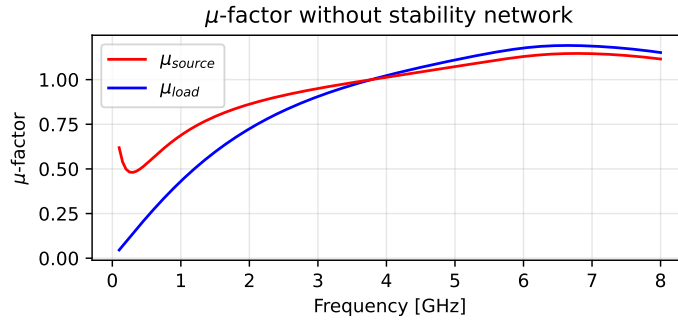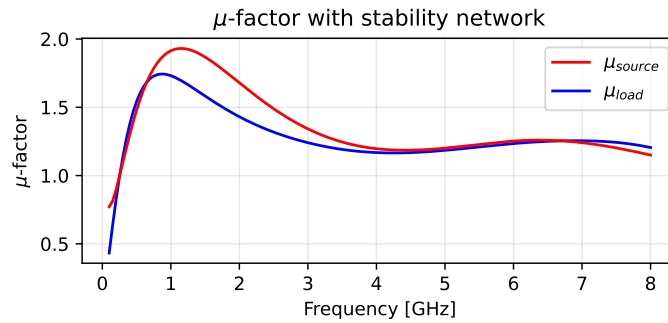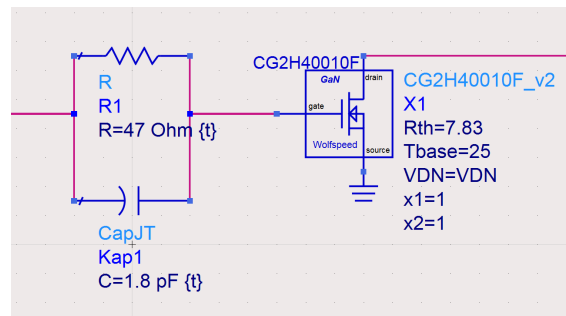
Figure 11: μ-factors for the driver amplifier without stability network.

A way to improve the stability is to add a stability network at the gate of the amplifier. As the μ-factors need to be increased in the lower half of the frequency range, adding a resistor and capacitor in parallel, as seen in Figure 12b, will ensure that. These two components are then tuned such that $\mu > 1$ for as low frequency as possible, and rounded off to the closest standardized value in the E12 series. This results in a capacitor and resistor value of 1.8 pF and 47 Ω respectively. The μ-factors after having added the stability network can be seen in Figure 12a, and it shows that the amplifier is unconditionally stable for frequencies larger than approximately 300 MHz.

(a) μ-factors.

(b) Schematic.

Figure 12: μ-factors and schematic for the driver amplifier with stability network.

3.1.3   Bias network

In Section 2.2.2 it was explained that a bias network requires two $\lambda/4$-transmission lines to transform the impedance the RF signal observes, such that no power leaks into the power supply. An ideal version of this network can be seen in the schematic in Figure 13a. The ideal network is created using two ideal transmission lines which have the fundamental frequency, characteristic

impedance, and the electrical length as parameters. The electrical length is given in degrees related to the wavelength, such that an electrical length of $90°$ is equal to $\lambda/4$. The S-parameter terminations are where the RF and DC supply is connected, for which the DC supply is connected between the two transmission lines.

The S-parameter S11 can be seen plotted in Figure 13b. S_{11} shows that at 3.9 GHz, $S_{11} = 1\angle 0°$ on the right side of the smith chart, meaning that there is a total reflection. The impedance for the RF signal at 3.9 GHz is $Z = \infty$, which theoretically shows that there will be no leakage of RF power towards the DC supply. This effect is only for the fundamental frequency of 3.9 GHz, at any other frequency, the impedance will be different. This is confirmed by the second harmonic at 7.8 GHz being in the center of the smith chart. This is because the transmission lines will have a length of $\lambda/2$ which results in an impedance of $Z = 50$ Ω.

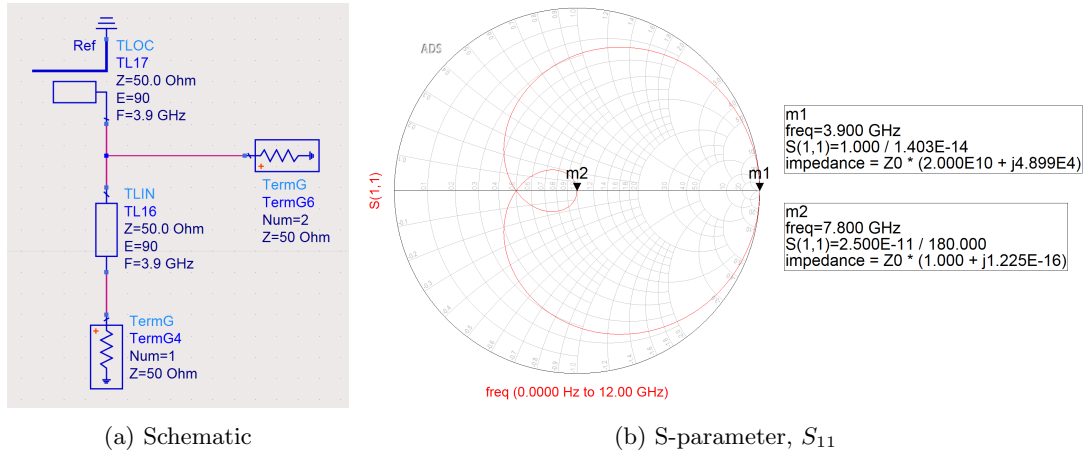(a) Schematic   (b) S-parameter, S_{11}

Figure 13: The schematic and S_{11} of an ideal bias network.

When converting from ideal transmission lines to real lines, the characteristic impedance and electrical length has to be realized with physical lengths. This can be done manually through the use of formulas, or the Linecalc tool included in ADS can do the calculations. The Linecalc tool requires the substrate characteristics, fundamental frequency, and the ideal line parameters. The Linecalc tool produced a line length, $l = 11.2$ mm, for a $\lambda/4$ line with a characteristic impedance of 100 Ω. As $\lambda/4$ lines are inherently narrow band, means that small deviations in the frequency will affect the performance. Therefore, a characteristic impedance of 100 Ω was chosen, as it showed a slightly improved performance when the frequency deviated. The $\lambda/4$ line length was fine-tuned to $l = 10.95$ mm, such that the RF signal sees an open circuit at 3.9 GHz. The resulting S-parameter, S_{11}, can be seen in Figure 14.

The bias network is further expanded by including the capacitors C_L and C_S, as depicted in Figure 2 from Section 2.2.2. These capacitors are added such that other frequency components do not leak into the DC supply. The two large capacitors are both from Murata, and are 10 μF and 100 nF respectively. Another capacitor of 12 pF from Johanson Technology is added to the left side, as seen in Figure 15.
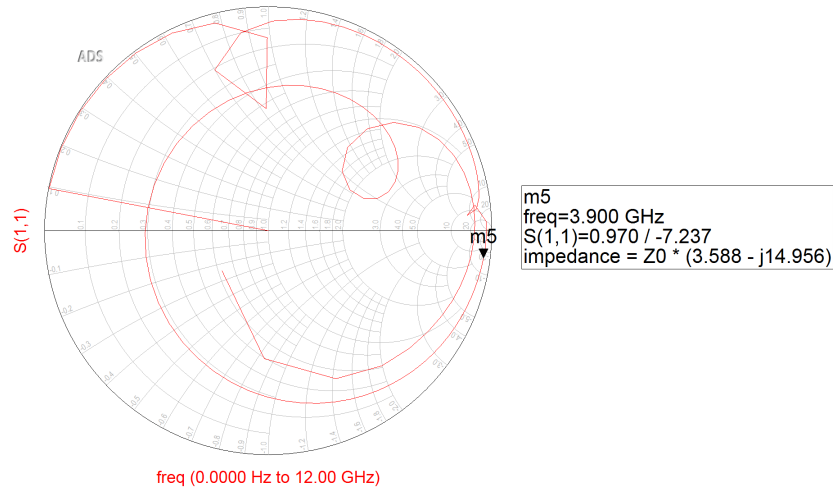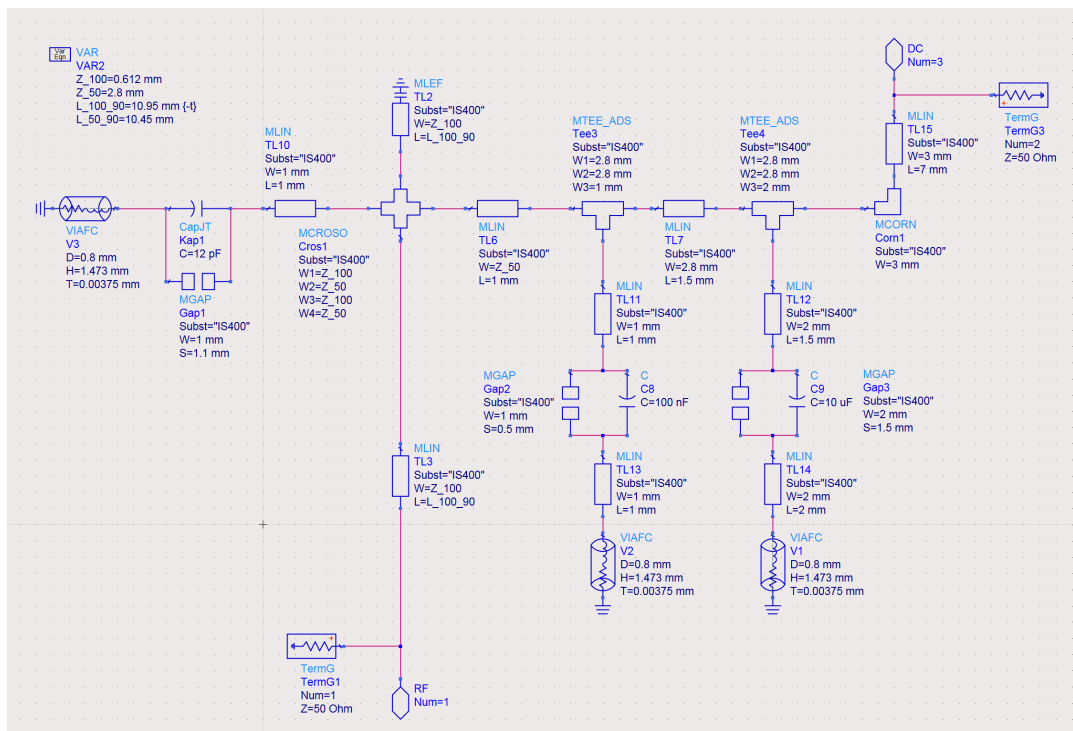
Figure 14: S-parameter, S_{11}, of the real bias network.

Figure 15: Schematic of the real bias network.

3.1.4 Matching networks

The driver amplifier is designed for maximum power transfer, which was described in Section 2.2.1. To assist with the design of the networks, some source-pull and load-pull building blocks are used, both of which are created by Associate Professor Olavsbråten. The benefit with these blocks is that the reflection coefficients, Γ_S and Γ_L, can be set directly. The two blocks allow for setting the fundamental frequency, magnitude and phase of Γ. This makes it possible to use the magnitude and phase variables when tuning and optimizing. The building blocks can be seen in Figure 16.

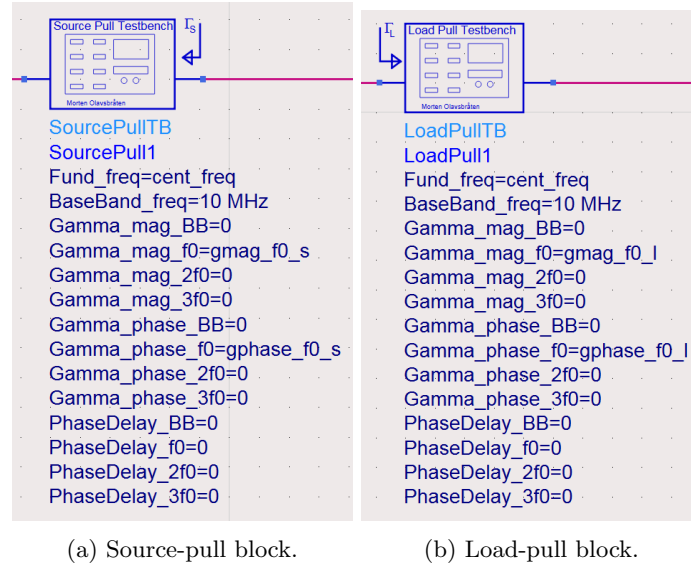(a) Source-pull block.   (b) Load-pull block.

Figure 16: The source- and load-pull blocks used as matching networks. [1]

As the output network of the driver amplifier is to be combined with the input network of the power amplifier, it is designed with the use of the load-pull block. This output network can be seen in Figure 17. By using the the load-pull block, and using the magnitude and phase of the reflection coefficient as optimization variables, it is optimized to achieve a maximum power transfer match. The magnitude is optimized between 0 and 1, and the phase between -180° and 180°. This optimization and tuning resulted in $\Gamma_L = 0.79\angle -131.5°$. Which will be further used when designing the interstage matching network.
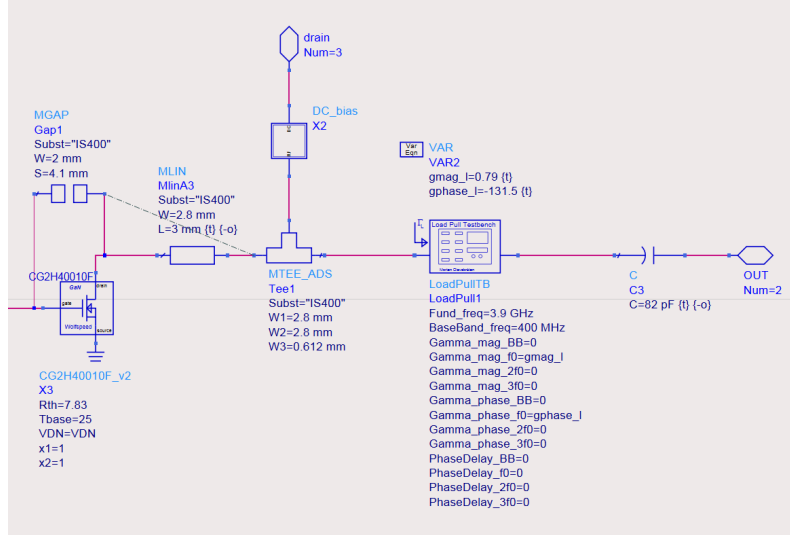

Figure 17: Schematic of the output network, with the load-pull block, for the driver amplifier.

The input matching network was designed such that it primarily used a singular transmission line and an open-ended stub to realize an appropriate match. However, when converting to layout this is further extended to include tapers and extra length required for soldering components, and fitting it to a cooling plate. First off the optimization only used the length of the lines as optimization and tuning variables, but a fixed width made it difficult to achieve the bandwidth requirement while at the same time staying above 10 dB small-signal gain. However, when the

widths are included as variables, the bandwidth and gain requirements are achieved. The resulting network is seen in Figure 18.
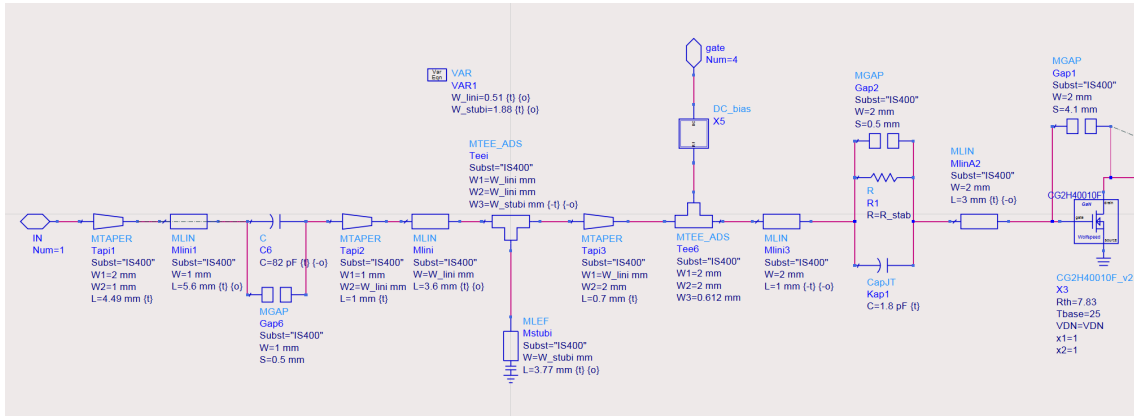

Figure 18: Schematic of the input network for the driver amplifier.

3.2   Design of the 25 W power amplifier

The 25 W power amplifier uses the same transistor technology as the 10 W driver amplifier. The transistor that is used is the CG2H40025, which is in the same series as the CG2H40010 transistor used in the driver amplifier. The design of the power amplifier is similar to that of the driver amplifier, however, there are some differences that will be pointed out in the next sections.

3.2.1   Class of operation

From the datasheet for the CG2H40025 transistor, the typical operating points for the gate voltage is between -3.8 V and -2.3 V, and the drain voltage is typically 28 V. By simulating the transistor the same way as in Section 3.1.1, the resulting IV-curves is seen in Figure 19. The same requirements of efficiency, linearity and output power is also wanted from the power amplifier. Therefore, a gate voltage of -2.8 V and a drain voltage of 28 V is chosen such that a class-AB amplifier is realized. This operating point gives a biasing current of 226 mA.
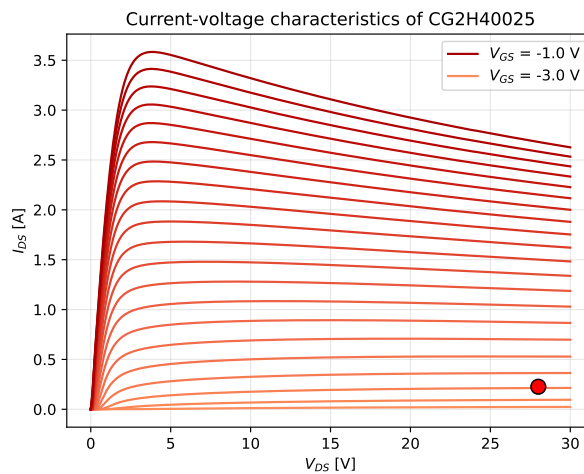

Figure 19: Current-voltage characteristics of the 25 W, CG2H40025, transistor.

3.2.2   Stability network

The stability network of the power amplifier is designed with the same principle as for the driver amplifier. From Figure 20, one can see that the μ-factors are less than 1 for frequencies below approximately 2.3 GHz, thus is only conditionally stable.
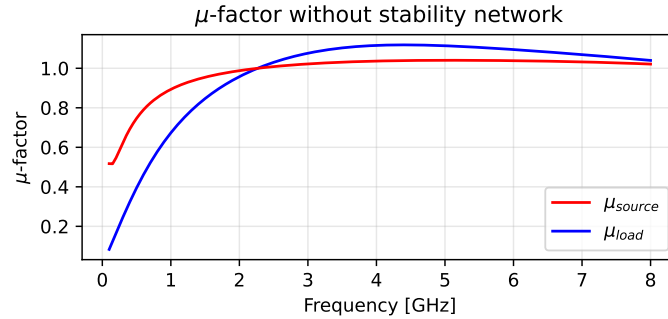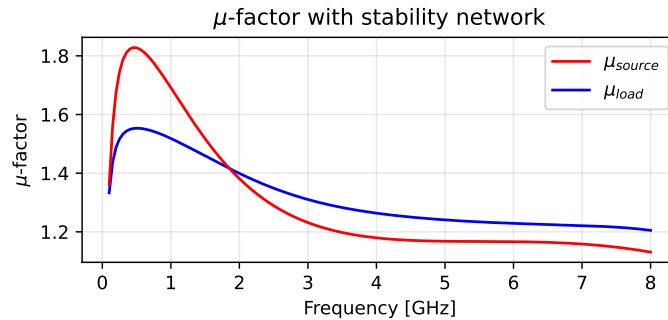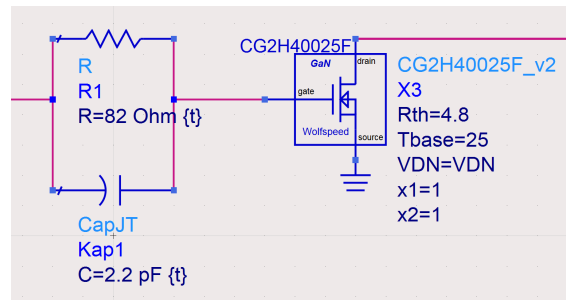

Figure 20: μ-factors for the power amplifier without stability network.

A stability network, as described in Section 3.1.2, consisting of a resistor and a capacitor in parallel is added at the gate of the power amplifier. The components are tuned the same way as for the driver amplifier, which results in a capacitor and resistor value of 2.2 pF and 82 Ω respectively. The resulting μ-factors can be seen in Figure 21a, and the schematic in Figure 21b. The μ-factors are larger than 1 for all frequencies, thus the amplifier is unconditionally stable.

(a) μ-factors.

(b) Schematic.

Figure 21: μ-factors and schematic for the power amplifier with stability network.

3.2.3 Bias network

The bias network design for the power amplifier is almost exactly the same as for the driver. The only thing that differs is the network for the gate biasing. For the power amplifier, a small resistor of 12 Ω is added in series with the $\lambda/4$ transmission line. This is for some added stability since the power amplifier is going to be envelope tracked. Such a change requires that the length of the $\lambda/4$ transmission lines are slightly adjusted to $l = 7.75$ mm, because of the added length from the taper lines on either side of the resistor.

3.2.4 Matching networks

The power amplifier is also designed for maximum power transfer to begin with, then the output network is further tuned to achieve maximum output power and power-added efficiency. The input network is designed in a similar manner to that of the output network for the driver amplifier. Where the input network employs the source-pull block to optimize and tune the magnitude and phase of the reflection coefficient. This resulted in $\Gamma_S = 0.61\angle - 66.6°$, which will be used in the design of the interstage network. The input network of the power amplifier can be seen in Figure 22.
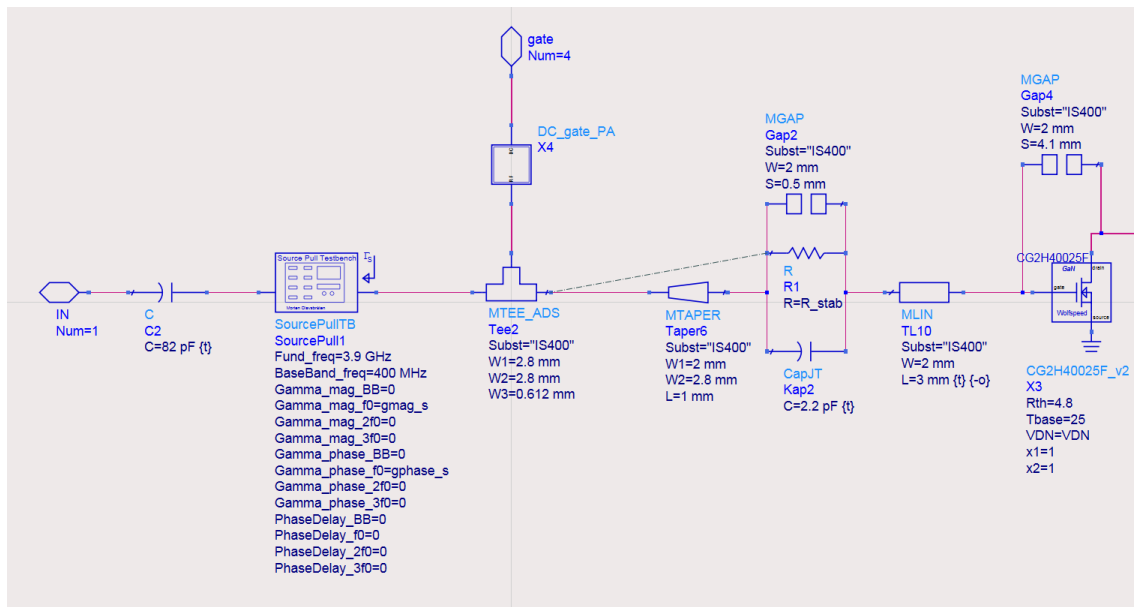

Figure 22: Schematic of the input network, with the source-pull block, for the power amplifier.

The output network is designed similarly to the input network of the driver amplifier. The output network can be seen in Figure 23. The main difference is that the output network of the power amplifier does not require the widths to be optimized and tuned, as the bandwidth and gain requirement is easier to fulfill because of gain overhead as the power amplifer is not biased as deep as the driver amplifier. This made it possible to design the network with only a transmission line and an open-ended stub. The lengths of the tapers and other lines are also tuned.
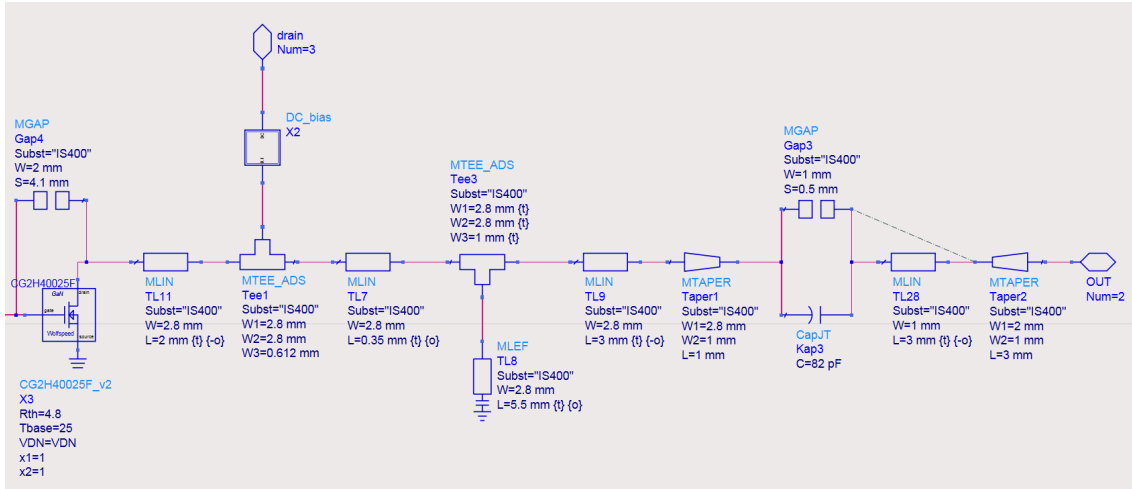
Figure 23: Schematic of the output network for the power amplifier.

3.3   Design of the interstage matching network

The purpose of the interstage matching network is to combine the output match of the driver amplifier, and the input match of the power amplifier. These two networks are represented by their respective load and source reflection coefficients. While designing the network, the small-signal gain of the two-stage amplifier is observed, such that it is as large as it can get, and centered on the fundamental frequency of 3.9 GHz. The design is also compared to an ideal combination of the two networks, which incorporates an isolator. Both of these are considered when finalizing the design, such that it behaves similarly. The interstage network and highlighted tuning stub can be seen in Figure 24. All of the components that are seen in the figure, is used when optimizing and tuning, which means that the lengths of the tapers, and the capacitance of the capacitor is also tuned.

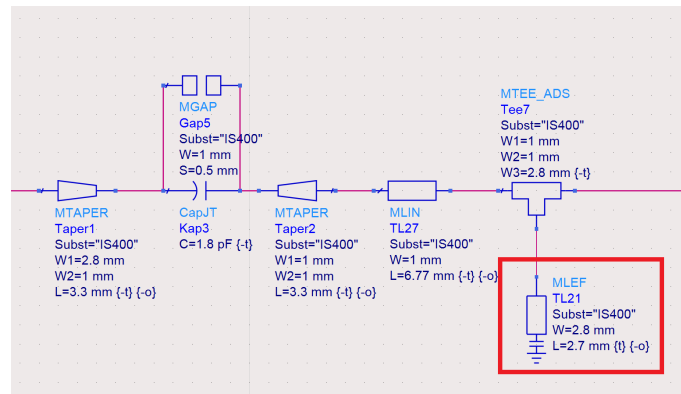Figure 24: Schematic of the interstage matching network.

3.4   Layout of the two-stage amplifier

The two-stage amplifier is designed such that it can be produced on a PCB, and be measured in the laboratory. The output network of the two-stage amplifier is separated from the rest since it would be the only part that would not change if other designs of the driver amplifier was to be produced.

The layout for the whole design is created such that it can be mounted onto a cooling plate with the dimensions 62.5 x 62.5 mm. This means that the input and output networks are adjusted such that they have a 5 mm overhang, for mounting of the female SMA connectors. A diagram showing the drilled hole layout of the cooling plate can be seen in Figure 25. The holes are primarily used to fasten the transistors, and the PCB to the cooling plate, for adequate cooling. These holes ended up setting some restrictions to the design of the different networks, since the transistors can only be mounted with these holes. Each mounting hole has 9.5 mm of distance from center to center. This means that the distance between the two transistors must be in intervals of 9.5 mm, which affects the interstage network as it has to be designed with regards to this as well.

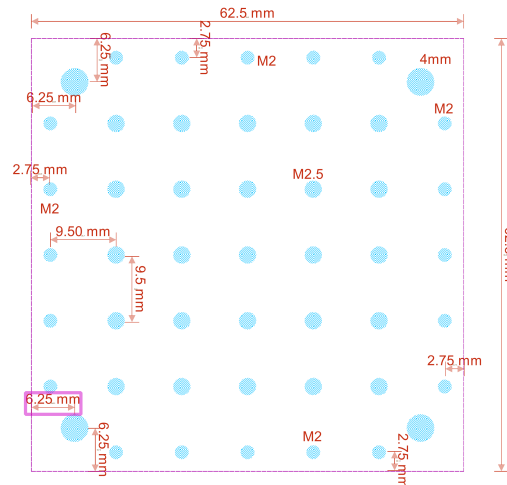Figure 25: Layout of the drilling holes required for mounting on the cooling plate.

Keysight ADS is not primarily a layout tool, but it does have the capability to produce the necessary gerber files for layout creation. The complete layout can be seen in Figure 26, while the PCB mounted on the cooling plate can be seen in Figure 27.
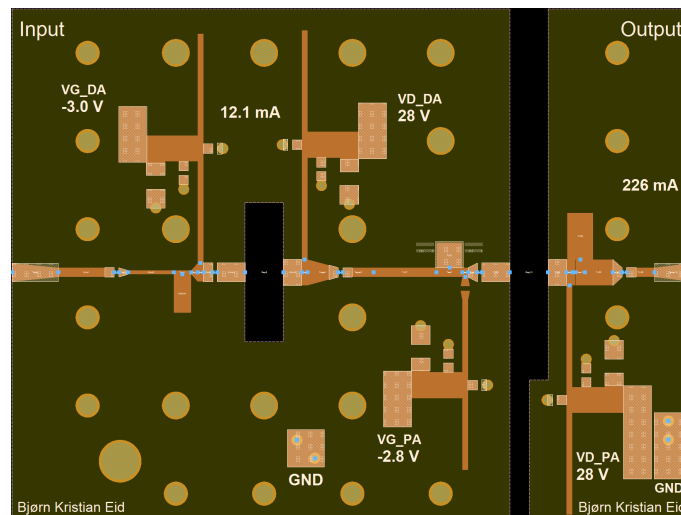

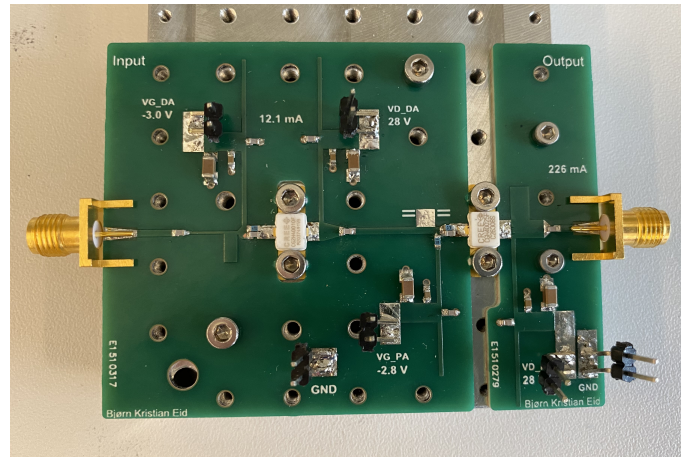Figure 26: Layout of the two-stage amplifier as seen in the layout editor.

Figure 27: The PCB of the two-stage amplifier, mounted on a cooling block.

3.5   Laboratory measurements

This section will go over the measurement setups for small-signal and large-signal with envelope tracking. All of the measurements are performed at NTNU's RF-laboratory.

3.5.1   Small-signal setup

The small-signal measurements are perfomed with a Vector Network Analyzer (VNA) from Pico Technology. A VNA can measure the S-parameters of the amplifier across a specified frequency range. The VNA used is a PicoVNA with a frequency range of 300 kHz to 8.5 GHz. This specific VNA can handle a maximum of 20 dBm of power into its ports. Because of this, a directional coupler is added between the output of the amplifier, and port 2 of the VNA, such that the output signal is attenuated with approximately 20 dBm. An attenuator of approximately 9 dB is added between port 1 of the VNA, and the input of the amplifier. This attenuator is for extra protection in case the amplifier oscillates. A diagram that depicts the measurement setup can be seen in Figure 28.
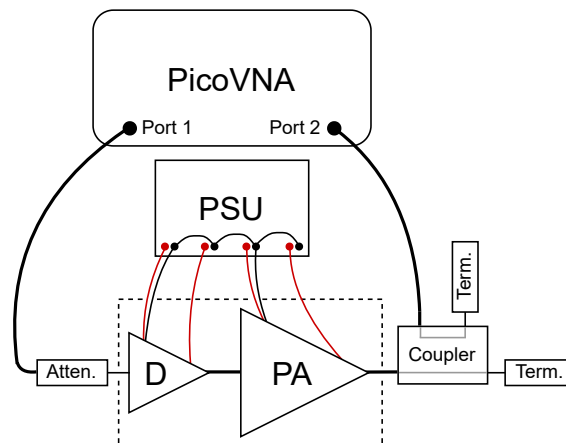

Figure 28: Small-signal measurement setup.

Before any measurements are done, the VNA has to be calibrated such that losses in the cables, attenuator, and the coupler is corrected for. This creates a new reference plane which is at the

input and output of the amplifier. This calibration is done with a Short-Open-load-Through (SOLT) calibration kit, which is also created by Pico Technology.

Since the two-stage amplifier has two gates and two drains that has to be supplied with power, a quad port power supply was used. This allows the whole two-stage amplifier to be supplied by the same power supply. The ground reference for all the ports were connected together to ensure a common ground for the whole amplifier. The most important parameter to have correct is the drain current, therefore, each of the gate voltages are fine tuned such that the driver and power amplifier have the correct drain currents.

3.5.2 Large-signal and envelope tracking setup

The large-signal and envelope tracking setup can be seen in Figure 29. This setup is inherently more complex than the small-signal setup, since the RF input power has to be swept. The RF source is used for supplying the amplifier with the RF signal, and is also capable of sweeping the RF input power. This signal goes through a wideband power amplifier before it is transferred to the device-under-test (DUT) which is the two-stage power amplifier in this thesis. Between the wideband PA and the DUT is a circulator that will make sure that the wideband PA does not affect the DUT. The wideband PA is required for making sure that the DUT is driven into saturation. The tracking function is supplied to the tracker through one of the waveform generators. Meanwhile, the other waveform generator supplies the RF source with the I/Q signal when modulation measurements are being done. The power measurements are done at the output of DUT with a signal and spectrum analyzer, there is a directional coupler between the DUT's output and the input of the spectrum analyzer. The list of known equipment can be seen below Figure 29.

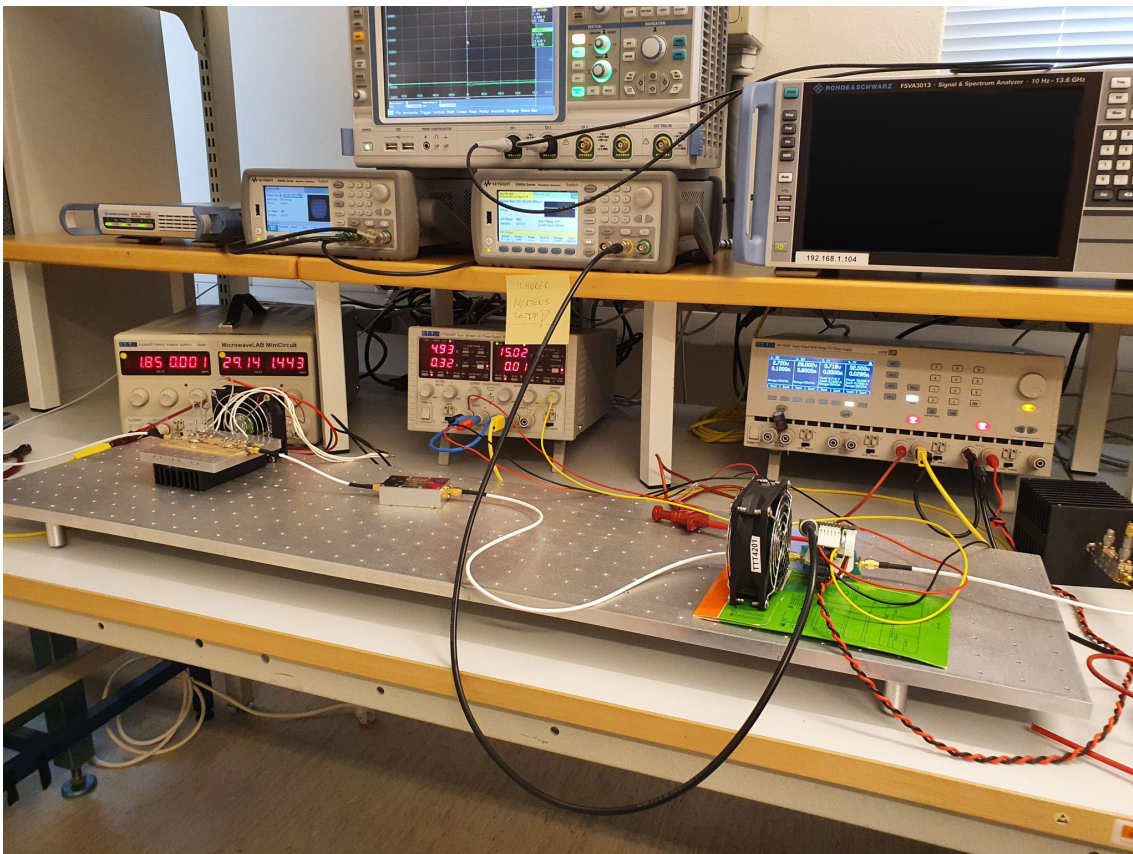Figure 29: Large-signal and envelope tracking measurement setup. Picture provided by Mathias Olsen.

- Olavsbråten Wideband PA, 2 to 5 GHz

- 2x, Keysight K33600A Trueform Waveform Generator

- Rohde & Schwarz SGS100A, SGMA RF source

- Rohde & Schwarz FSVA3013, Signal & Spectrum Analyzer

- Aim-TTi CPX200DP, 180 W DC Power Supply

- Aim-TTi EX354RT, 300 W DC Power Supply

- Aim-TTi MX100QP, 420 W DC Power Supply

4   Results

In this section the results from the small- and large-signal simulations and measurements will be presented. For the small-signal analysis, only simulation results are included for the driver and power amplifier, as they were simulated separately, and then combined onto a singular PCB, making them unable to be measured separately. However, there will be simulation and measured results for the two-stage amplifier, in both small- and large-signal. The large-signal simulations and measurements will use a skewed fundamental frequency of 3.85 GHz since the fundamental frequency shifted a bit between simulations and measurements.

The measured results use a 16-QAM signal with a symbol rate of 3.84 MHz. The signal is created in Matlab, and has a sequence of 10,000 symbols. The signal is then filtered by a raised-cosine filter that has a roll-off factor, $\alpha = 0.22$, and the signal has an oversampling factor of 64. Every measurement should have a Peak-to-Average Power Ratio (PAPR) that is approximately 7.2 dB, besides one of the static measurements and the maximum PAE tracking, which have a larger PAPR of approximately 10 dB. All of the measurements use the same 16-QAM signal.

4.1   Small-signal analysis

4.1.1   Driver and power amplifier
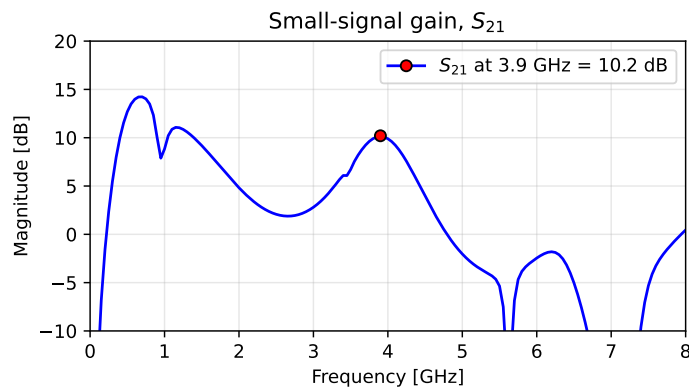
(a) Driver amplifier.
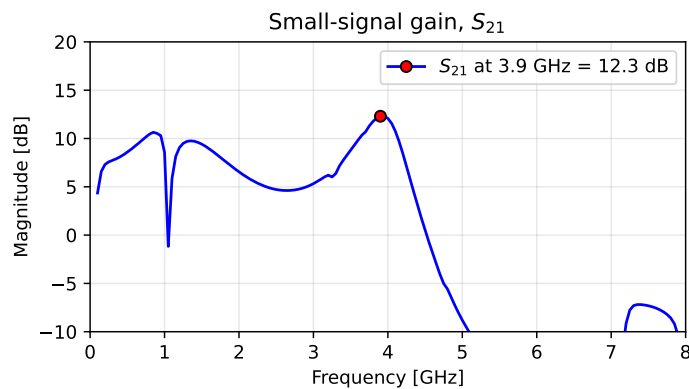
(b) Power amplifier.

Figure 30: Simulated small-signal gain, S_{21}, for the driver and power amplifier.
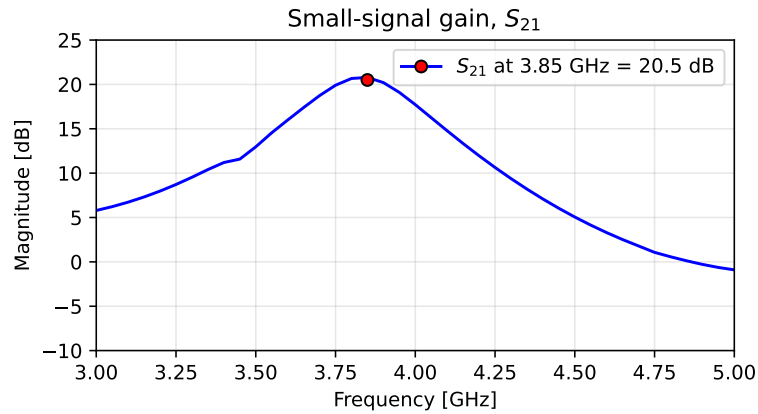
4.1.2   Two-stage amplifier

Figure 31: Simulated small-signal gain, S_{21}, for the two-stage amplifier.
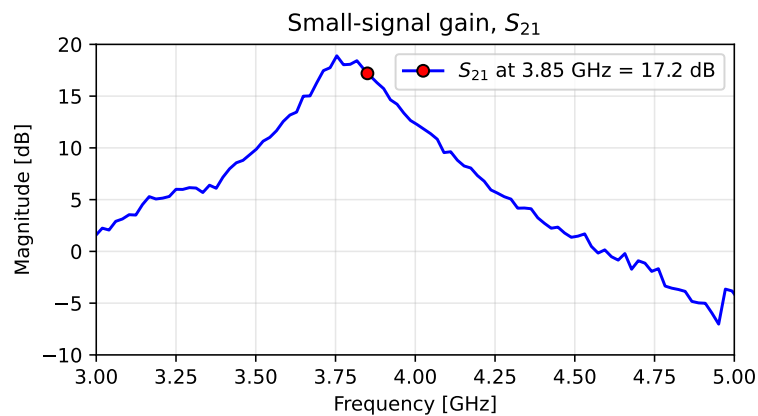

Figure 32: Measured small-signal gain, S_{21}, for the two-stage amplifier.

4.2   Large-signal analysis

The large-signal analysis will consist of the simulated and measured results of the two-stage amplifier. The simulations were done with one-tone tests at the skewed fundamental frequency of 3.85 GHz. The RF input power was swept from -10 to 30 dBm in the simulations and in the measurements. The drain voltage was also swept from 10 to 30 V with a step of 2 V for both. A mismatch is created for the simulations and the measurements by shortening the stub in the interstage matching network. This is done by physically cutting the line. The simulations from ADS is plotted with dashed lines and with a blue hue, meanwhile the measurements are plotted with solid lines and a red to orange hue.

4.2.1   Transducer gain for the two-stage amplifier

Figure 33: Measured and simulated transducer gain, uncut.
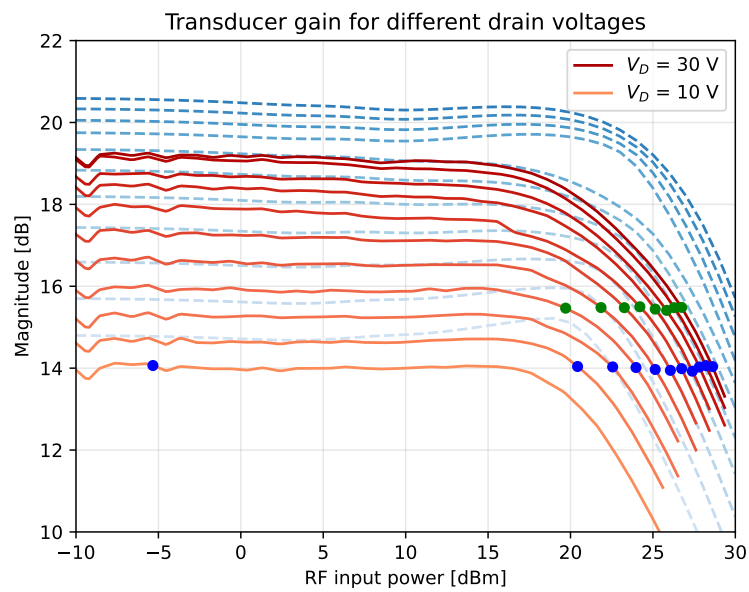
Figure 34: Measured and simulated transducer gain, after one cut.
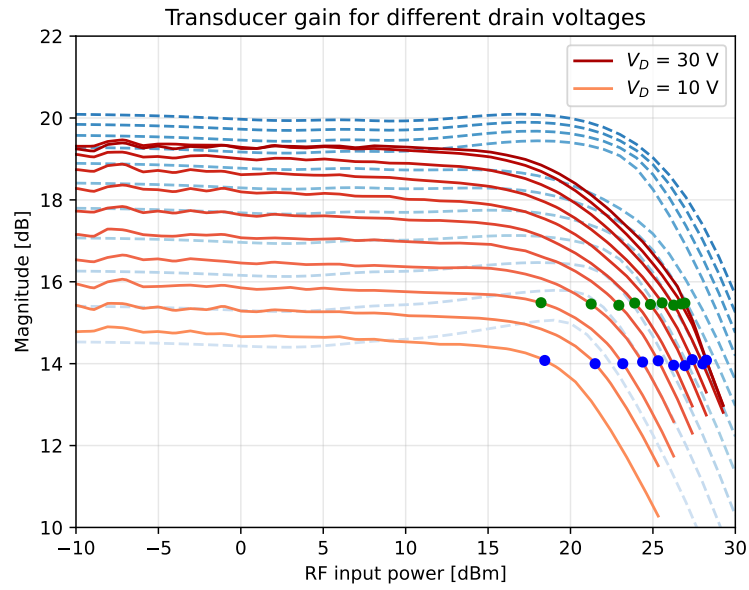
Figure 35: Measured and simulated transducer gain, after two cuts.

4.2.2 Output power for the two-stage amplifier
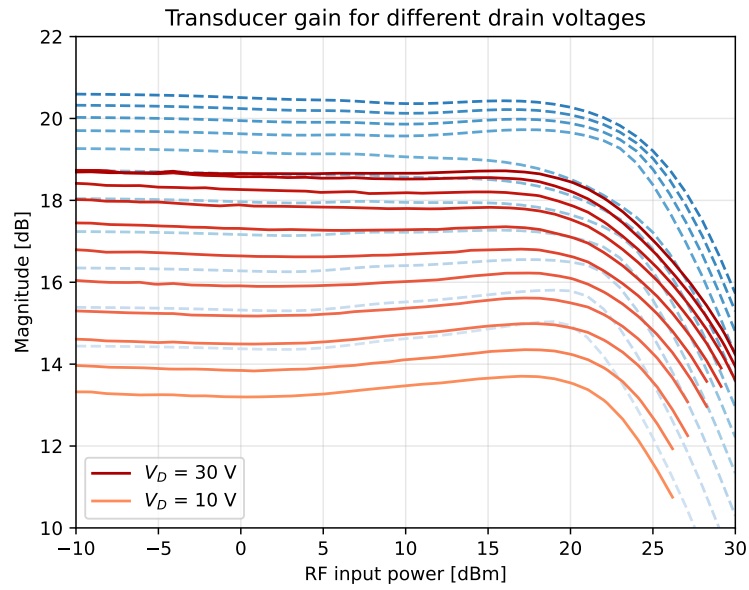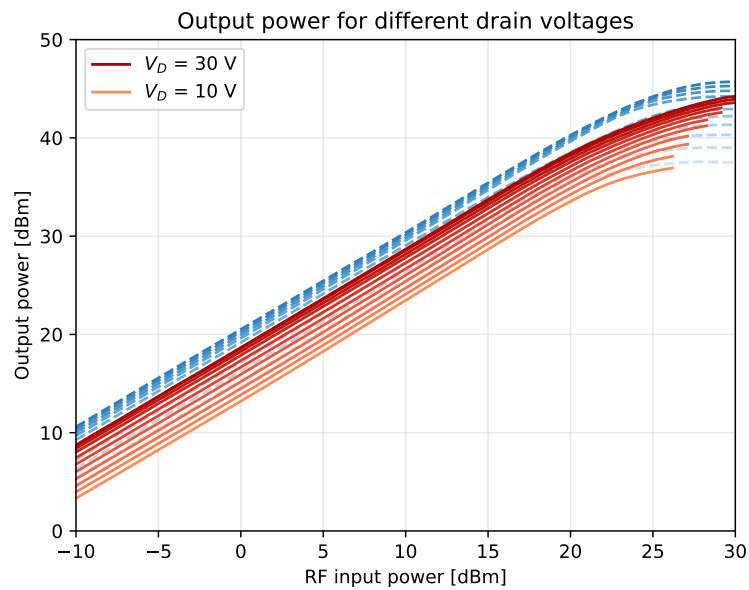

Figure 36: Measured and simulated output power, uncut.
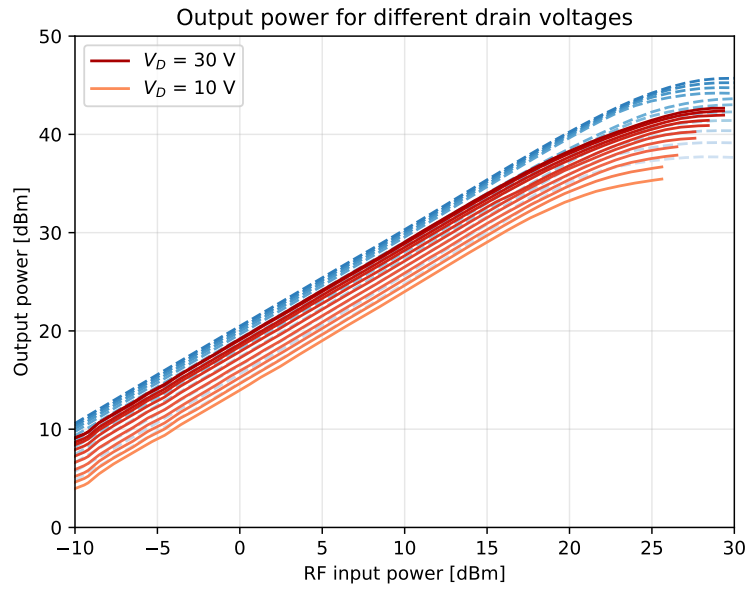
Figure 37: Measured and simulated output power, after one cut.
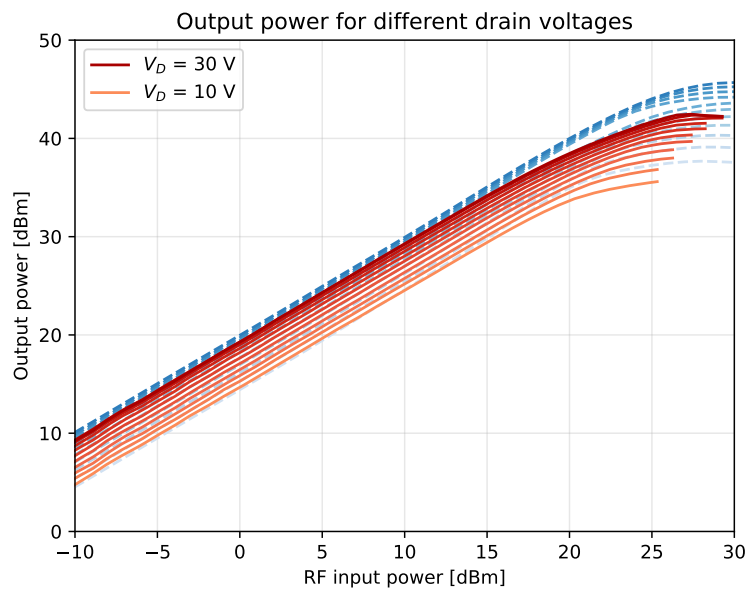
Figure 38: Measured and simulated output power, after two cuts.

4.2.3 Power-added efficiency for the two-stage amplifier
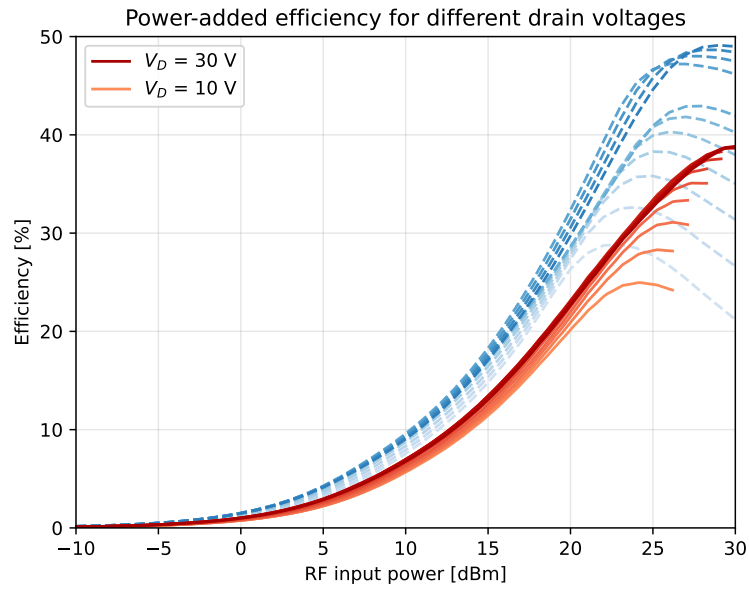
Figure 39: Measured and simulated power-added efficiency, uncut.
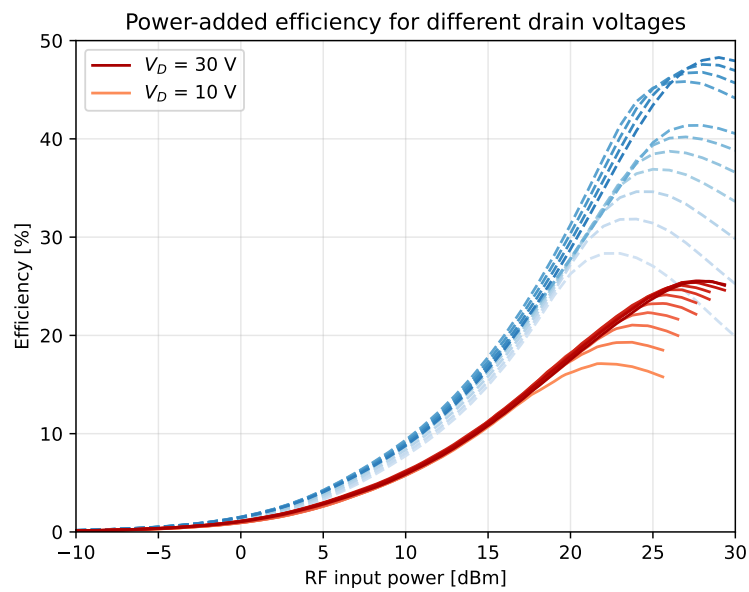
Figure 40: Measured and simulated power-added efficiency, after one cut.
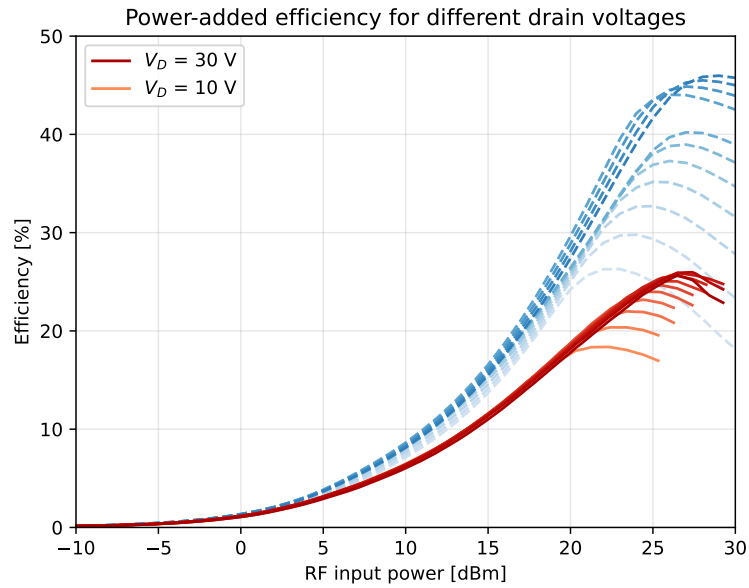
Figure 41: Measured and simulated power-added efficiency, after two cuts.

4.2.4   Modulation and envelope tracking

All the figures that represent gain and phase ripple have a normalized x-axis, which is normalized to the peak of the output power at 0 dB. The plotted lines are approximated to best fit the 10,000 measured symbols from the QAM signal. Each figure also includes a line that is a static measurement at $V_d = 28$ V, and the same average output power.
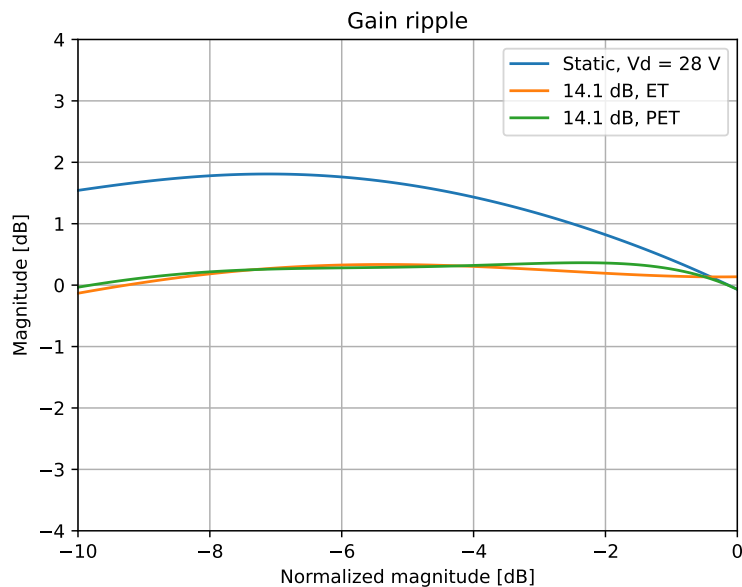
Figure 42: Measured gain ripple for the 14.1 dB flat gain tracking, after one cut.
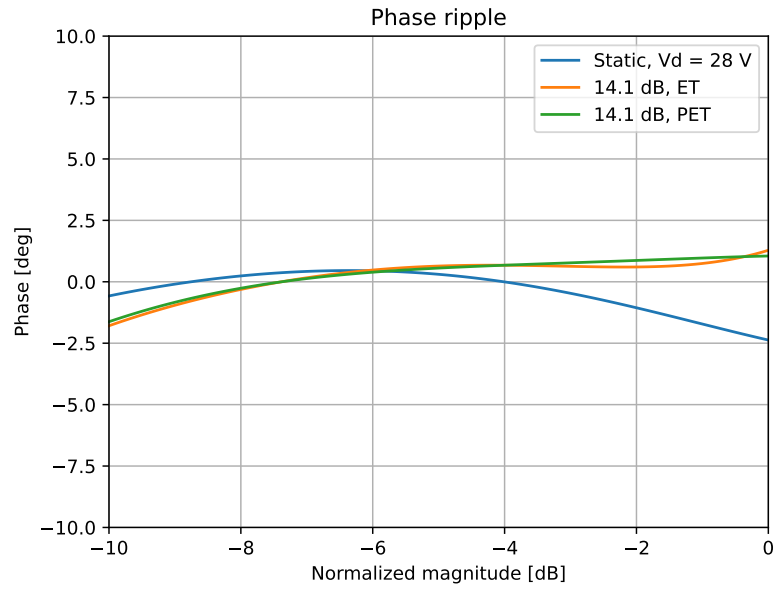
Figure 43: Measured phase ripple for the 14.1 dB flat gain tracking, after one cut.
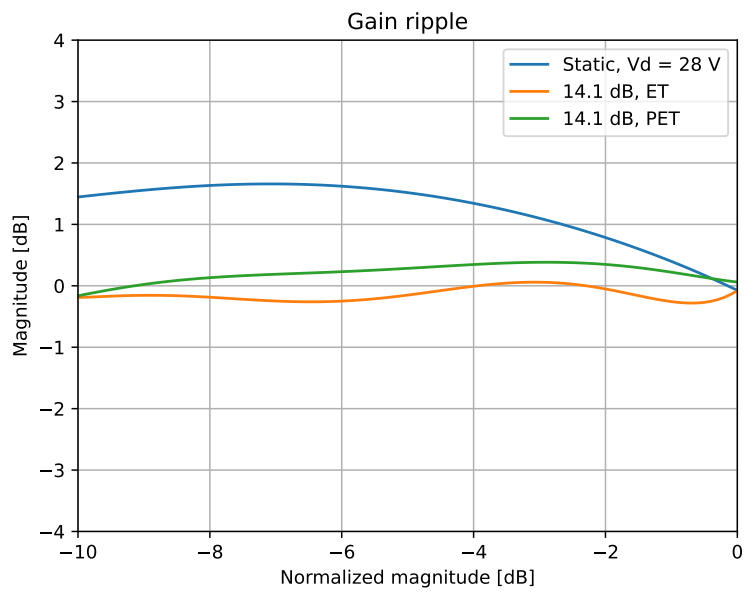
Figure 44: Measured gain ripple for the 14.1 dB flat gain tracking, after two cuts.
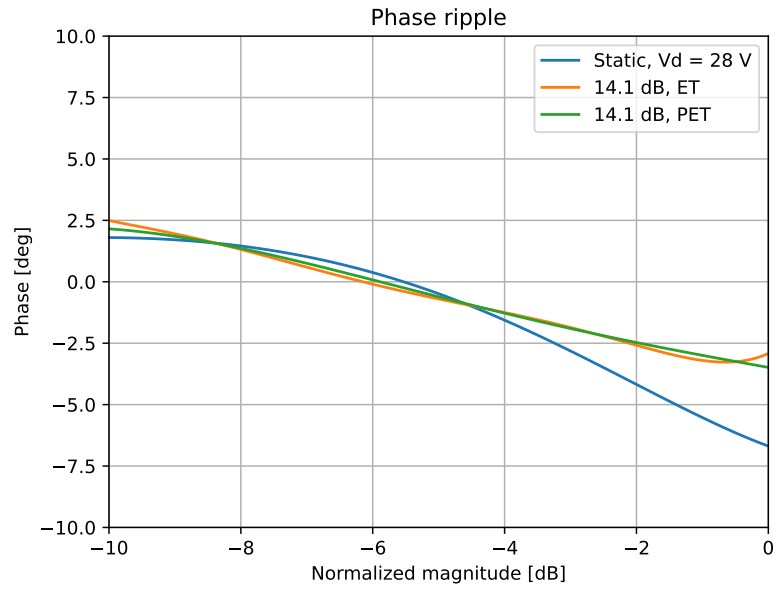
Figure 45: Measured phase ripple for the 14.1 dB flat gain tracking, after two cuts.
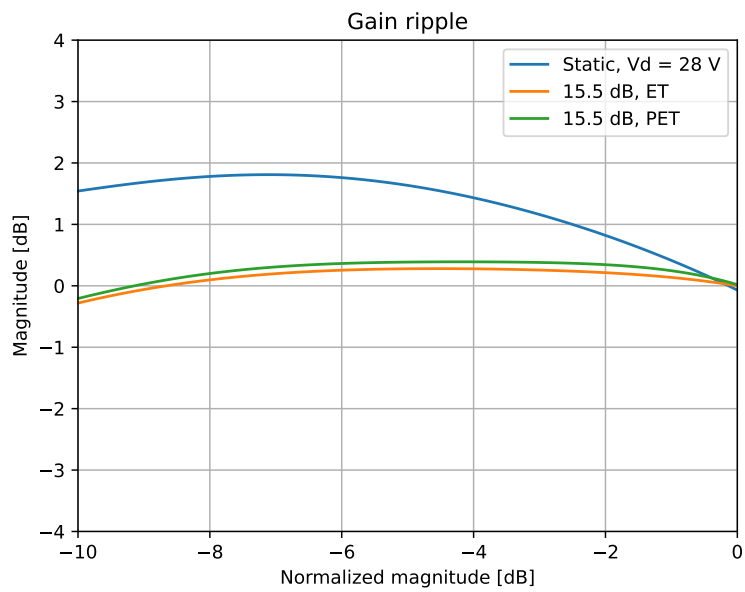
Figure 46: Measured gain ripple for the 15.5 dB flat gain tracking, after one cut.
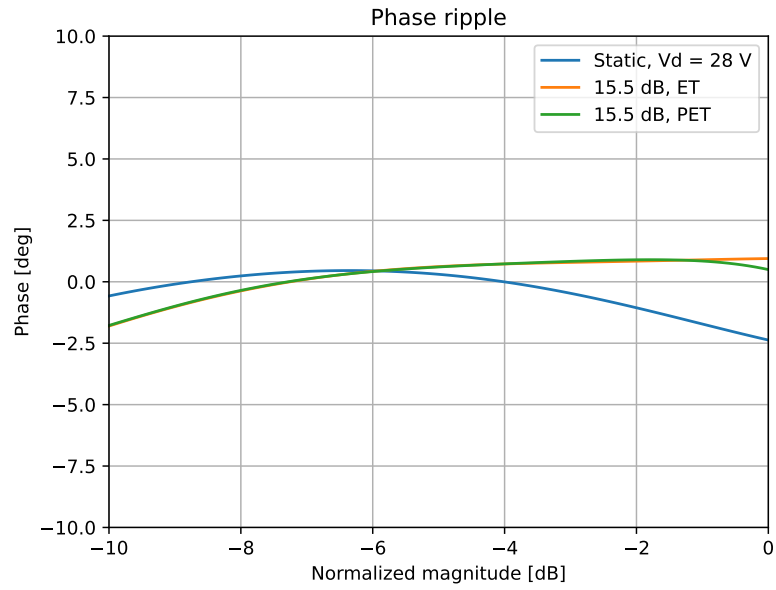
Figure 47: Measured phase ripple for the 15.5 dB flat gain tracking, after one cut.
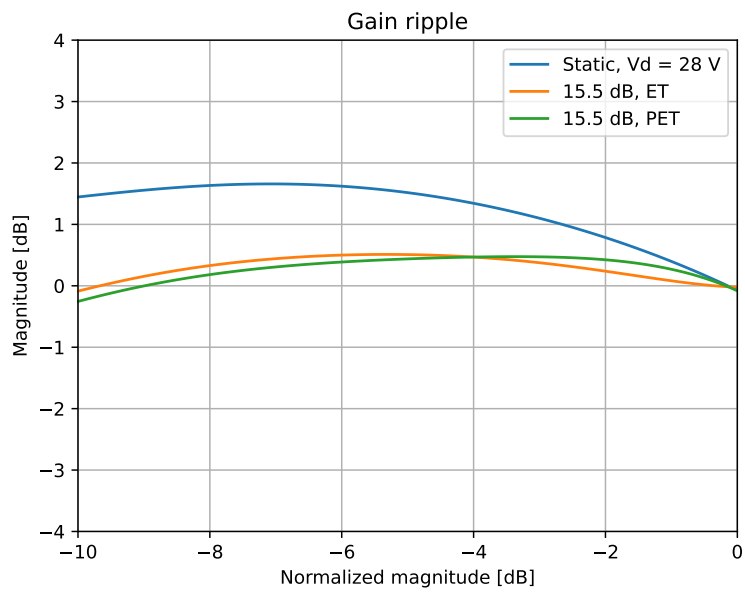
Figure 48: Measured gain ripple for the 15.5 dB flat gain tracking, after two cuts.
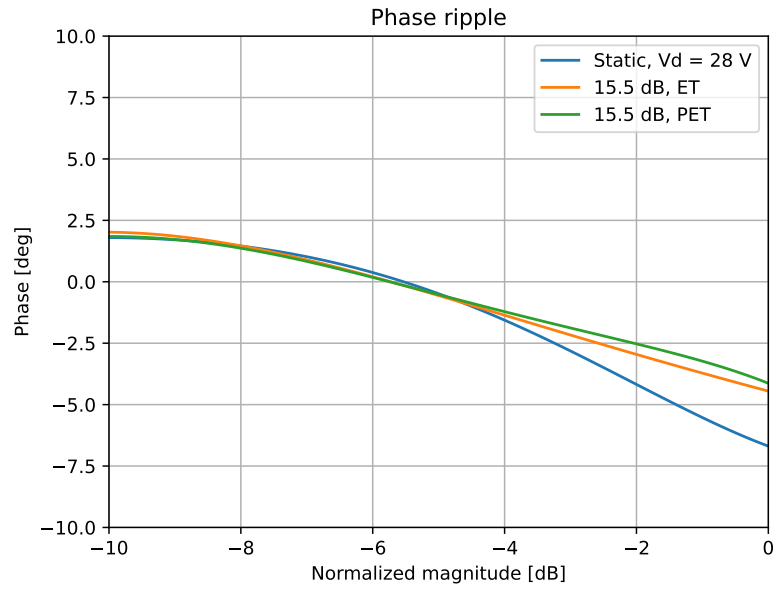
Figure 49: Measured phase ripple for the 15.5 dB flat gain tracking, after two cuts.
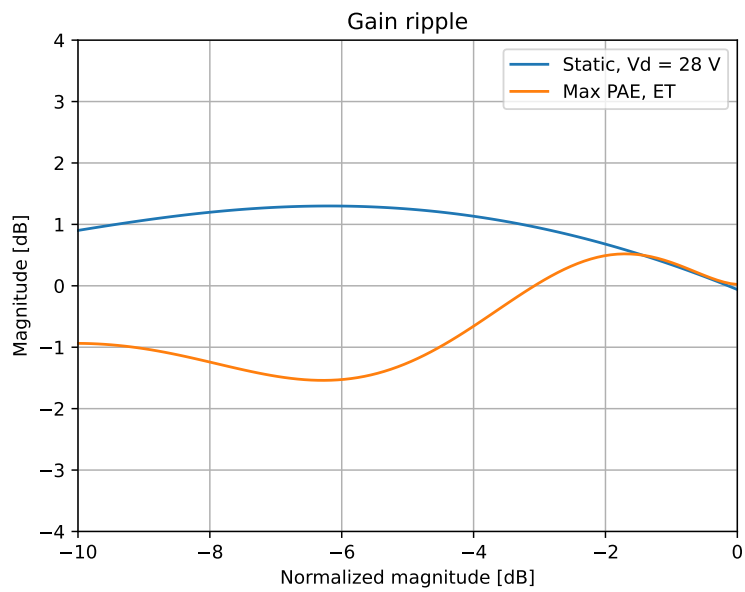
Figure 50: Measured gain ripple for the max PAE tracking, after one cut.
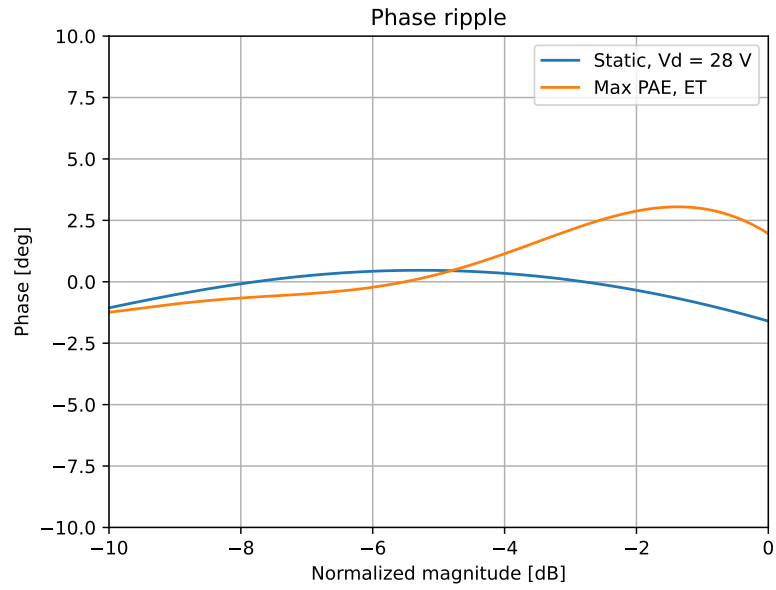
Figure 51: Measured phase ripple for the max PAE tracking, after one cut.
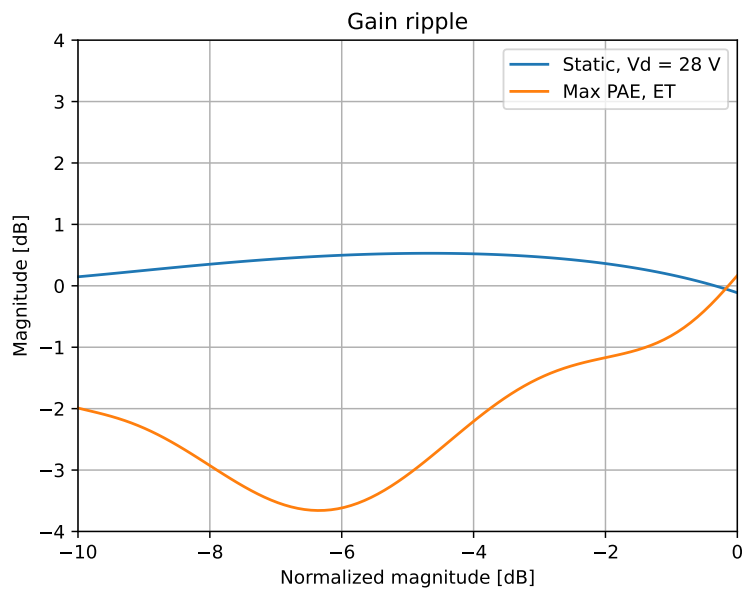
Figure 52: Measured gain ripple for the max PAE tracking, after two cuts.
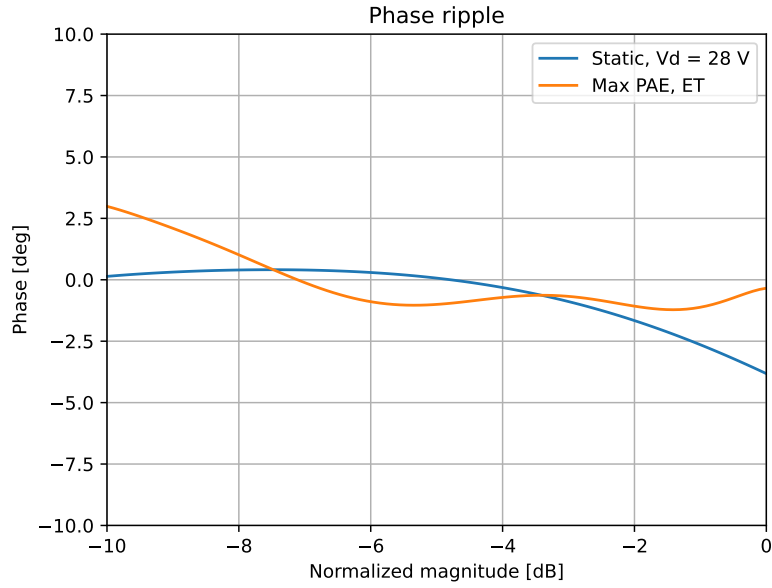
Figure 53: Measured phase ripple for the max PAE tracking, after two cuts.

Table 3: Measured results for different tracking scenarios, after one cut.

|	$P_{out,avg}$ [dBm]	$Gain_{avg}$ [dB]	PAE_{avg} [%]	$STDR$ [dB]	$ACPR$ [dB]	EVM [%]
Static, Vd = 28 V	36.1	21.4	15.9	28.2	-35.9	3.8
Static, Vd = 28 V	37.2	21.2	18.0	27.4	-35.4	3.7
Max PAE, ET	36.1	16.1	30.3	22.9	-31.7	4.4
Flat gain, 14.1 dB, ET	37.3	17.1	33.1	25.3	-33.1	5.2
Flat gain, 14.1 dB, PET	37.4	17.2	33.4	25.4	-33.1	5.4
Flat gain, 15.5 dB, ET	37.1	18.4	30.1	24.9	-32.6	6.1
Flat gain, 15.5 dB, PET	37.2	18.6	30.3	24.4	-32.1	6.0

Table 4: Measured results for different tracking scenarios, after two cuts.

	$P_{out,avg}$ [dBm]	$Gain_{avg}$ [dB]	PAE_{avg} [%]	$STDR$ [dB]	$ACPR$ [dB]	EVM [%]
Static, Vd = 28 V	34.2	22.1	12.5	32.2	-40.6	2.2
Static, Vd = 28 V	37.2	21.6	17.8	27.5	-35.7	3.7
Max PAE, ET	34.2	15.4	26.3	21.0	-28.5	4.5
Flat gain, 14.1 dB, ET	37.0	17.0	33.0	26.9	-35.6	3.6
Flat gain, 14.1 dB, PET	37.2	17.2	34.5	25.0	-33.5	5.1
Flat gain, 15.5 dB, ET	37.4	18.5	32.5	24.8	-32.7	5.5
Flat gain, 15.5 dB, PET	37.4	18.5	32.5	24.4	-32.5	5.6

5   Discussion

In this section, the results from Section 4 will be compared and commented.

5.1   Small-signal analysis

The simulations done for the driver and power amplifier focused on making sure that each of them could fulfill the gain and bandwidth requirement of at least 10 dB, and 10 % respectively. Being able to fulfill the 10 dB gain requirement for the driver amplifier, proved to be complicated. Mainly caused because of the bandwidth requirement, the gain dropping as the frequency increases, and the deep class-AB biasing required for the driver characteristics presented in [1].

The small-signal gain S_{21}, for the driver amplifier can be seen in Figure 30a. The driver achieves a small-signal gain of 10.2 dB at the fundamental frequency of 3.9 GHz. It is more difficult to see from the figure what the bandwidth is, but the simulations show that the 1 dB bandwidth is from 3.7 GHz to 4.1 GHz. This bandwidth fulfills the requirement of at least 390 MHz (10 %).

For the power amplifier, the small-signal gain can be seen in Figure 30b. From this figure one can see that the power amplifier achieves a gain of 12.3 dB. Meanwhile, the 1 dB bandwidth of the power amplifier is from 3.7 GHz to 4.1 GHz, same as the driver.

Based on the small-signal gains of the driver and power amplifier it is expected that the small-signal gain of the two-stage amplifier should ideally be 22.5 dB if the interstage match is a perfect combination of the output network of the driver, and the input network of the power amplifier. The simulated small-signal gain of the two-stage amplifier can be seen in Figure 31. From the figure it is apparent that the interstage match is not perfect, and has 2 dB of loss, since the peak is at 20.5 dB. However, this is with a slight mismatch as the tuning stub is made to be 0.35 mm longer than what is nominal. It is also expected that the bandwidth is halved for the two-stage because of the 1 dB bandwidth for the driver and power amplifier being from 3.7 GHz to 4.1 GHz, with the limits being at 9.2 dB and 11.3 dB respectively. This causes the combined gain to be 20.5 dB at the limits, and the 1 dB bandwidth is now approximately from 3.8 GHz to 4.0 GHz. Because of the 50 MHz shift, the bandwidth becomes 3.75 GHz to 3.95 GHz.

The measured small-signal gain can be seen in Figure 32. The figure shows that the peak is shifted slightly further than 50 MHz, however, it is important to bear in mind that a slight shift is expected because of the tuning stub being longer than nominal. Some of the shift will also be caused by slight changes in the permittivity and loss tangent of the substrate, as changes in both will affect the performance drastically.

5.2   Large-signal analysis

A specific thing to note is that every measurement that was done for the two-stage amplifier with an uncut tuning stub is measured directly without the use of the drain tracker connected to the drain of the 2nd stage. This has an impact on the measured performance which is prominent in the power-added efficiency figures. Each cut of the tuning stub is approximately 0.35 mm, such that an uncut stub is 2.70 mm long, then first cut makes it around 2.35 mm, and the second cut makes it around 2.00 mm. All these lengths are approximate as it is difficult to make precise cuts of 0.35 mm with a hobby knife.

The simulated and measured transducer gain for an uncut tuning stub can be seen in Figure 33. From the figure one can see that there is an unusual behavior for the simulation, that happens when the drain voltage changes from 22 V to 24 V. This is because of the simulation model of the CG2H40025 transistor is slightly wrong. This fault in the model causes the gain to be larger during simulations when the 2nd stage amplifier has a drain voltage of 24 V or higher. The simulated

transducer gain is approximately 20.5 dB at -10 dBm input power, which is as expected since the gain at a small input power is the same as the small-signal gain. The measured transducer gain at -10 dBm is approximately 18.8 dB, which is larger than the small-signal gain of 17.2 dB. It is possible to see that the two-stage amplifier begins to saturate between 15 and 20 dBm of input power.

The transducer gain for the two-stage amplifier after the tuning stub was cut once, is shown in Figure 34. The simulated transducer gain changed with less than 0.2 dB because the fundamental frequency of 3.85 GHz is located at the small-signal peak, such that shortening the stub did not shift the peak drastically to the right. However, where cutting the tuning stub does impact the results is for the measured gain, which has increased to 19.2 dB at -10 dBm. Such a change confirms the location of the small-signal gain peak of the measurements, since making the stub shorter causes the peak to shift to the right. Thus, it moves the peak towards the fundamental frequency of 3.85 GHz. The measured gain is now closer to the simulation if the fault in the simulation model is accounted for. There are some green and blue dots embedded on Figure 34, these are the points used when creating the tracking functions. The blue dots are placed at a flat gain of 14.1 dB, which works well because it manages to track the whole drain voltage range from 10 to 30 V. The green dots are placed at a flat gain of 15.5 dB, and tracks from 16 to 30 V.

Last up for the transducer gain is after two cuts, which is seen in Figure 35. The gain at -10 dBm input power has increased some more, up to around 19.6 dB. This means that even after one cut, the peak was still not at 3.85 GHz. One can also see a drop of about 0.5 dB in the simulated gain, since after two cuts the small-signal gain peak is past the 3.85 GHz mark, and is dropping. The blue and green dots still represent the 14.1 dB and 15.5 dB tracking points, respectively.

Next up is the output power, which for an uncut stub can be seen in Figure 36. The measured output power is approximately 44.0 dBm at an input power of 30 dBm, this is at a drain voltage of 28 V. For a drain voltage of 30 V, the output power is approximately 44.4 dBm. This is about 1.5 dBm less peak output power than simulated, which is approximately 45.9 dBm and 45.5 dBm for a 30 V and 28 V drain voltage respectively. This is expected as the transducer gain of the amplifier also dropped with approximately 1.5 dB.

After having cut the stub once, the output power is measured to be 42.8 dBm at 30 dBm input power and a drain voltage of 30 V. For a drain voltage of 28 V, the output power is 42.5 dBm. This can be seen in Figure 37. These measured values are a decrease in output power compared to the uncut stub. This means that even though the gain increased, the two-stage amplifier appears to be saturating earlier. The same behavior can be seen after two cuts, which is shown in Figure 38. However, after two cuts the amplifier saturates even earlier, and gets current limited by the supply, hence the flatness at the peak.

The power-added efficiency for the two-stage amplifier with an uncut stub is seen in Figure 39. The two-stage amplifier achieves a peak PAE of around 38 %, meanwhile the simulation achieves a peak PAE of almost 50 %. However, because of the faulty model it is realistically somewhere around 45 %. The efficiency dropped even further with the stub being cut once, where the peak PAE can be seen to be as low as 25 % for the 30 V trace. This can be seen in Figure 40. The efficiency did not drop much further after two cuts, which is seen in Figure 41. However, at the higher input powers the power supply started current limiting, which is what causes the abnormal behavior at said input powers. The drop in efficiency when cutting the stub is explained in the next paragraphs.

Something that is noticeable for the figures where the stub has been cut, is that the performance has changed compared to when the stub was uncut. Figure 33 has a gain that resemble the simulations, while the measurements when the stub has been cut diverge from the simulations. Such a divergence can also be seen for the output power and most noticeably the power-added efficiency figures. This could possibly be caused by the stub being shortened, which could have little impact on the simulations, but a larger impact on measurements. However, it is reasonable to suspect that the inconsistency is caused by the added drain tracker, and an improper compensation

of its increased current draw and other behavior that can affect the two-stage amplifier. This suspicion is further strengthened because of the PAE, as the formula for PAE is the difference of output power and input power, divided by the DC power. Which means that if the drain tracker draws more current than what is compensated for, the DC power will be larger, thus reducing the power-added efficiency.

The maximum drain current of the 2nd stage amplifier is 1.74 A measured directly from the supply. With the drain tracker attached, the maximum drain current is 1.87 A and getting current limited by the supply. The drain current of 1.87 A is already compensated by a static 29 mA, making the actual drain current 1.899 A which is the set current limit of the supply. What this shows is that a static compensation of 29 mA is not enough at larger current draws, because the drain tracker uses more current when the amplifier draws more current. Based on the current values, the tracker uses up to 140 mA more than what is compensated for, which is a current increase of approximately 9 %. This could possibly be even higher as the supply got current limited.

The gain and phase ripple for the two-stage amplifier with a modulated input signal, envelope tracked 2nd stage, and tuning stub cut once, can be seen in Figure 42 and Figure 43 respectively. The figures show two different tracking functions, one for envelope tracking (ET), and one for power envelope tracking (PET), both of which are tracking for a flat gain of 14.1 dB. One can see that a static drain voltage has a gain ripple of almost 2 dB at most. Meanwhile, the gain ripple is less than 0.5 dB for ET and PET. The phase ripple for a static drain voltage is within $\pm 2.5°$, which is to be expected as the phase does not change much when the drain voltage is static. For both ET and PET, the phase ripple is approximately $+1.0°$ at the peak, and changes to $-1.7°$ at 10 dB back-off, resulting in a difference of $2.7°$. PET performs similar to ET, but has the benefit of having a reduced bandwidth requirement for the drain supply.

Figure 44 and Figure 45, shows the gain and phase ripple, respectively, for the 14.1 dB flat gain tracking with a tuning stub that has been cut twice. The gain ripple for the static drain voltage measurement shows a similar behavior to that of the stub being cut once, since the gain does not change much when going from one cut to two. The tracking functions changed slightly, hence the observable change in the gain ripple for ET and PET. Both ET and PET maintains a gain ripple that is less than 0.5 dB from the peak to the 10 dB back-off. The phase however, changes a considerable amount after two cuts. This is because of the declining phase slope which was shown in [1], meaning that after two cuts, the downwards slope is steeper than the upwards slope created by tracking. This is also seen for the static drain voltage measurement, as the phase ripple changes from $+2°$ at -10 dB, to $-6.7°$ at 0 dB. Which is further proven by the traces for ET and PET, which both have a downwards trend from $+2.5°$ to $-3.0°$. All of this shows that the 2nd cut is shortening the stub too much, and the optimal length would be somewhere between 2.00 and 2.35 mm. However, because of the imprecision in the cuts, it cannot be said for certain what the optimal length is. This also means that the design of the interstage match is important and should be done precisely, or with means to precisely edit it after production.

The gain and phase ripple for the 15.5 dB flat gain tracking, and tuning stub cut once, can be seen in Figure 46 and Figure 47. The gain ripple for ET appears to be slightly better on average than the PET for the 15.5 dB tracking. However, both of them appear to be less than 0.5 dB total, since the lowest is -0.2 dB and highest is approximately $+0.3$ dB. When it comes to the phase ripple, ET and PET are almost exactly the same, with only a minor difference at the peak of 0 dB. The phase ripple is $+1.3°$ at the peak, and $-2.0°$ at 10 dB back-off. The gain and phase ripple after two cuts can be seen in Figure 48 and Figure 49 respectively. The gain ripple for ET is less than 0.5 dB throughout the whole range. PET however, appears to reach $+0.5$ dB at 4 dB back-off, and -0.2 dB at 10 dB back-off, which gives a total difference of 0.7 dB. The phase ripple has a total variation of approximately $6.4°$.

There was also done ET for maximum PAE instead of flat gain. Figure 50 and Figure 51 shows the gain and phase ripple with the tuning stub cut once. From the gain ripple figure one can see that if the amplifier is not tracked for flat gain, the gain ripple becomes quite large, with the largest difference being from -1.5 dB to $+0.5$ dB. The static drain voltage has also a smaller difference

since this tracking operates the amplifier at a lesser average output power, and a larger PAPR. This becomes prominent in the phase ripple figure, where the phase ripple for the static drain voltage is smaller than for the other tracking scenarios. The phase ripple for the max PAE tracking has a difference of approximately 4.5°. For a tuning stub cut twice, the gain and phase ripple can be seen in Figure 52 and Figure 53. The gain ripple figure shows that the specific tracking function used for max PAE tracking after two cuts, gives a large gain ripple of 3.7 dB. Meanwhile, the phase ripple difference is approximately 4.0°.

Table 3 shows the measured results for the different tracking scenarios, with the tuning stub being cut once. All the flat gain tracking scenarios attempted to achieve an average output power of 37.2 dBm with a PAPR of 7.2 dB, such that they can easily be compared to each other. From the table it becomes clear that one can achieve a good linearity without envelope tracking the amplifier, which can be seen from the static drain voltage rows. However, the average efficiency is worse. It is immediately noticeable that the average gain for the flat gain tracking scenarios are larger than what the functions were created for. The average power-added efficiency is also larger for every tracking scenario, compared to that of the static drain voltage scenarios. Both ET and PET perform similar because of the tracking functions being similar.

The measured results for different tracking scenarios after two cuts can be seen in Table 4. The goal for average output power is maintained for both cut scenarios. A highly linear amplifier is achieved with the first row with a static drain voltage, however, it has a smaller average output power, and the average PAE has dropped further. It is important to note that almost every tracking scenario shows an improved EVM and ACPR, which could have been better if the stub was cut slightly less. The 14.1 dB flat gain ET is better in every linearity measure than the other tracking scenarios.

5.3   Future work

An idea for this thesis was to be able to change everything besides the 2nd stage output, such that different versions of the 1st stage and the interstage match could be tested. Therefore, creating a different version of the interstage match is something that can be done. This changed interstage matching network should include ways to more precisely tune it such that it can be tuned while being measured to get the exact behavior that is wanted. This could also improve some different parameters like the gain and power-added efficiency.

6 Conclusion

The thesis realizes a linear and efficient two-stage power amplifier, by the use of envelope tracking and power envelope tracking for flat gain and efficiency, while linearity is improved through a tuneable mismatch in the interstage matching network. The thesis also conveys the importance of precisely designing the interstage matching network, as small changes in the mismatch can affect the linearity of the two-stage amplifier.

The design program ADS is used throughout the whole design process of the two-stage power amplifier. A deep class-AB driver amplifier and a class-AB power amplifier is designed and combined into a two-stage amplifier by a interstage matching network. These two discrete amplifiers employ GaN HEMT transistors from Wolfspeed as active devices, where the driver amplifier uses the 10 W CG2H40010, and the power amplifier uses the 25 W CG2H40025 transistor. The two-stage power amplifier is to be produced on a PCB, therefore, layout design is required. The two-stage power amplifier is measured at the RF-laboratory of NTNU, where small-signal and large-signal is measured and performance is presented.

The two-stage power amplifier is envelope tracked for a flat gain of 14.1 and 15.5 dB. An average output power of 37.2 dBm, with a PAPR of 7.2 dB is achieved. When the 2nd stage is tracked, an average PAE of larger than 30 % can be seen. The efficiency enhancement techniques ET and PET, perform similarly, but the PET has an advantage of the drain power supply requiring less bandwidth. When further mismatch is introduced, the measures of linearity improves across the board. However, the linearity can be improved further as the extra introduced mismatch is larger than necessary because of imprecision in the tuning.

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