Master's thesis

NTNU
Norwegian University of Science and Technology
Faculty of Information Technology and Electrical Engineering
Department of Electronic Systems

Magnar Fossbakken Lundberg

Efficiency and Linearity Improvement on a Two-Stage Power Amplifier using Drain- and Gate Modulation with Power Envelope Tracking

Master's thesis in Electronic Systems Design
Supervisor: Morten Olavsbråten
June 2023

NTNU
Norwegian University of
Science and Technology

Magnar Fossbakken Lundberg

Efficiency and Linearity Improvement on a Two-Stage Power Amplifier using Drain- and Gate Modulation with Power Envelope Tracking

Master's thesis in Electronic Systems Design
Supervisor: Morten Olavsbråten
June 2023

Norwegian University of Science and Technology
Faculty of Information Technology and Electrical Engineering
Department of Electronic Systems

NTNU
Norwegian University of
Science and Technology

Executive summary

This report is a master thesis written by Magnar Fossbakken Lundberg, at the Norwegian University of Science and Technology in Trondheim. The master is written at the Department of Electronic Systems, with Associate Professor Morten Olavsbråten as supervisor. The main subject of this thesis is Power Envelope Tracking performed on a two-stage power amplifier. The Power Envelope Tracking is used to modulate the drain voltage and the gate voltage in the transistors to increase the efficiency of the power amplifier without decreasing the linearity.

The power amplifier is designed during the project and is a two-stage amplifier with harmonic tuning in the output matching circuit in both the stages. The design and simulation were performed using the software Advanced Design System from Keysight. The power amplifier has a center frequency of 2GHz, with a transducer power gain of 31dB, power added efficiency of 63%, a peak output power of 43dBm and a small-signal gain of 28.2dB.

The Power Envelope Tracking is firstly tested in simulation and optimized to get high efficiency and linearity. Later a model of the power amplifier is used to amplify a 16-QAM signal. The distortion caused by the model, and the efficiency is calculated. In the simulation three different Power Envelope Tracking formulas will be tested. One for high efficiency, another for flat gain and one for flat gain and flat phase. The first two will only use drain voltage modulation and the third will use drain voltage modulation combined with gate voltage modulation. With flat gain and flat phase the linearity increased, and the efficiency stayed the same compered with drain modulation to get flat gain.

During the tracking measurements a 5MHz 16-QAM signal was generated using a Matlab script. This signal was amplified using the power amplifier and the distortion is then calculated. Due to the time constraints caused by issues with the setup used in the tracking measurements only drain voltage modulation was tested during the tracking measurements. With only drain voltage modulation to get flat gain one can see the linearity increases. Drain voltage modulation for flat gain gave a higher efficiency compered with drain voltage modulation for high efficiency. The results from the simulation and the tracking measurements shows that the efficiency and linearity of a PA can be increased using drain voltage modulation combined with gate voltage modulation.

Sammendrag

Denne rapporten er en masteroppgave skrevet av Magnar Fossbakken Lundberg, ved Norges teknisk-naturvitenskapelige universitet i Trondheim. Masteren er skrevet ved Institutt for elektroniske systemer, med Førsteamanuensis Morten Olavsbråten som veileder. Hovedtemaet for oppgaven er "Power Envelope Tracking" utført på en totrinns effektforsterker. Power Envelope Trackingen er brukt for å modulere drain-spenningen og gate-spenningen på transistorene for å øke effektiviteten i effektforsterken uten at lineariteten blir redusert.

Effektforsterkeren er laget for dette prosjektet og er en totrinns forsterker med harmonisk tuning i utgangsnettverkene i begge trinnene. Effektforsterkeren har en senterfrekvens på 2GHz, "transducer power gain" på 31dB, "power added efficiency" på 63%, maks utgangseffekt på 43dBm og småsignal forsterkning på 28.2dB.

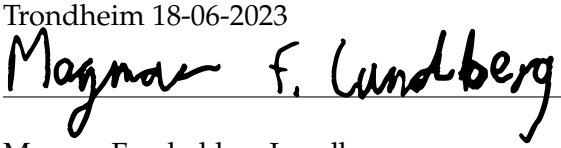
Power Envelope Tracking er først testet i simulering og optimalisert for å gi høy effektivitet og linearitet. Deretter lages det en modell av effektforserkeren som brukes til å forsterke et 16-QAM signal. Forvregningen forårsaket av modellen og effektiviteten er beregnet. I simuleringen vil tre ulike Power Envelope Tracking-formler bli testet. Den ene skal gi høy effektivitet, den andre skal gi flat forsterkning og den tredje skal gi flat forsterkning og flat fase. De to første skal kun bruke modulasjon av drain-spenningen og den tredje skal bruke modulasjon av drain-spenningen kombinert med modulasjon av gate-spenningen. Med flat forsterkning og flat fase forblir effektiviteten lik som den var med kun modulasjon av drain-spenningen for kun å oppnå flat forsterkning.

Under målingene av tracking ble et 5MHz 16-QAM generert av et script i Matlab. Dette signalet ble forsterket av effektforsterkeren og forvregningen ble beregnet. På grunn av tidsbegrensninger som følge av noen problemer i oppsettet av utstyret brukt i testing av tracking, er kun modulasjon av drain-spenning testet. Med kun modulasjon av drain-spenning kan man se at lineariteten økte. Modulasjon av drain-spenningen for å få flat forsterkning ga en høyere effektivitet sammenlignet med modulasjon av drain-spenning for å få høy effektivitet. Resultatene fra simuleringene og målingene av tracking viser at effektiviteten og lineariteten i en effektforsterker kan forbedres ved å bruk av modulasjon av drain-spenningen gate-spenningen.

Preface

This master thesis was worked on and written by Magnar Fossbakken Lundberg during the spring of 2023. The supervisor during the project was Associate Professor Morten Olavsbråten. The topic of the thesis was given by Associate Professor Morten Olavsbråten at the Department of Electronic Systems at the Norwegian University of Science and Technology in Trondheim.

Trondheim 18-06-2023

Student: 

Magnar Fossbakken Lundberg

Acknowledgements

I would like to thank my supervisor Associate Professor Morten Olavsbråten for his guidance and valuable advice and for giving me the the topic for my thesis. Olavsbråten's engagement and interesting discussions have help further sparking my interest regarding the topic of radio frequency design. I would also like to thank Associate Professor Morten Olavsbråten and Dragan Gecan for their discovery of Power envelope tracking and for laying the foundation that this thesis is based on.

Further I would like to thank my brother Torbjørn Lundberg for proofreading this thesis. I want to thank Steffen Kirknes for being an inspiration and a great teacher the last year. Finally, a special thanks goes to both of my parents Trond Lundberg and Magni Fossbakken for immense support both in regards to my studies and in life in general.

Contents

1 Introduction

Higher efficiency is an important subject in electronics. Higher efficiency will give the device a longer battery life, longer life span or one can expand the system by adding more components. In this thesis the efficiency enhancing technique power envelope tracking will be tested. It will also be used to improve the linearity of a power amplifier by gate voltage modulation. This technique was presented by Morten Olavsbråten and Dragan Gecan. This is the first time power envelope tracking on the gate voltage and drain voltage is used on a two-stage power amplifier to improve its linearity and efficiency, as far as the author knows.

1.1 Background and motivation

In most modern wireless transmitters, the Power Amplifier (PA) consumes most of the power. The PA amplifies the power of a signal before it is transmitted. A PA with low efficiency drains the battery in mobile, transmitting devices faster. In stationary base stations, used by telecommunication companies a PA with low efficiency will increase the power consumption, which increases the companies electricity bill. As a result the consumers telephone bill can increase. A PA with low efficiency will have a high heat build up, which in turn requires active cooling, which further increases the power consumption.

A number of efficiency enhancing techniques exist today, including Doherty, Envelope Elimination and Restoration (EER), Outphasing and Envelope Tracking (ET). Each having its advantages and disadvantages. Most of today's wireless communication uses some sort of amplitude and phase modulation, as in Quadrature Amplitude Modulation (QAM). This requires a PA with high linearity in regards to phase and gain, as a function of output power. Linearity enhancing techniques include Feedback, Feed Forward, Pre-Distortion and gate voltage modulation or gate tracking [1].

ET consists of tracking the envelope of the baseband signal and modulating the supply voltage to follow this envelope. This increases the efficiency drastically, as the PA is mainly operating close to compression regardless of the input power level. ET requires a tracker with a large bandwidth and high efficiency[1]. Morten Olavsbråten and Dragan Gecan introduced in 2017 a technique based on ET. This technique is called Power Envelope Tracking (PET) and reduces the needed bandwidth of the tracker. This is because one tracks the power of the envelope instead of the voltage, requiring two times the baseband signals bandwidth with 1st order PET and four

times the baseband bandwidth with 2nd order PET [2]. Using the power of the envelope one can use the same technique on the gate voltage, called gate voltage modulation or gate tracking. Modulating both the gate voltage and the drain voltage in a PA one can potentially achieve both high linearity and high efficiency [1].

1.2 Description of project

The use of PET gives a substantial increase in a PA's efficiency, which comes at a cost of the linearity. The main topic of this project is to design and measure a two-stage PA. PET will be performed on both the drain voltage and gate voltage in both stages to linearize the PA and increase the efficiency. The task of the project will be to:

- Design and simulate a two-stage PA in ADS, optimized for efficiency.
- Learn about harmonic tuning to increase efficiency in a PA.
- Optimize the coefficients in the tracking formulas for high linearity and efficiency.
- Design layout and produce PA.
- Measure and characterize the produced PA.
- Test PET on the produced PA.

The following specification requirements are given for the PA:

- $Z_0 = 50\Omega$.
- Center frequency f_c should be 2GHz.
- 1dB bandwidth of 100MHz.
- Small signal gain S_{21} > 26dB.
- Peak output power > 43dBm.
- S_{11} < -10dB.
- Efficiency should be as high as possible.

1.3 Related work

In the paper "Bandwidth Reduction for Supply Modulated RF PAs Using Power Envelope Tracking" Morten Olavsbråten and Dragan Gecan presented a version of envelope tracking that required less bandwidth [3]. This method has later been used to linearize the phase and gain by modulating the gate voltage in the PA in "Investiogation of linearity improvement with dynamic gate bias technique for flat gain or phase of an 10 W GaN HEMT power amplifier"[4]. Dragan Gecan investigated the use of gate voltage modulation in combination with drain voltage modulation with PET in his PhD thesis "Techniques for Linearity and Efficiency Improvement by Biasing Gate and/or Drain as Functions of Envelope Power and Introduction of a Novel FOM for Linearity, Applied on GaN PA's" [2]. This was used to linearize and increase the efficiency in a PA.

1.4 Scope of the project and overview

Chapter 2 is a theoretical background needed for this project. In this chapter the basics of PAs will be explained, as well as the building blocks, gain, efficiency and stability. Scattering parameters, the efficiency improving techniques ET, PET and Doherty will also be explained, including the theory behind gate voltage modulation for linearization. **Chapter 3** will explain the PA's design, with each part of the PA and the reasoning behind the design. This chapter will also explain how the PET formulas was designed and the setup needed for small-signal analysis, large-signal analysis and tracking measurements. **Chapter 4** will show the results from the simulations and the testing of the power amplifier. This chapter will end with a discussion of the results from the testing. **Chapter 5** will show the result from tracking simulations and the measurements from the testing, ending with a discussion of the results. **Chapter 6** will give a conclusion of the results from the testing of the power amplifier and the tracking, ending with some recommendations for further work.

1.5 Limitations of the project

This thesis will only study one linearization technique and one efficiency enhancing technique. The linearization technique is gate voltage modulation and the efficiency enhancing technique is drain voltage modulation. These two techniques will be tested together. Only a few different modulation formulas and combinations will be used. The complexity of these for-

mulas will be kept low due to some time constraints. Due to the time constraints caused by issues with the setup used in the tracking measurements only drain voltage modulation was performed during measurements. Gate voltage modulation was only tested during simulations.

2 Theory

2.1 Power Amplifier

A PA amplifies the amplitude of the power of an input signal. Previous PA designs relied on tubes to amplify the input signal. Due to the improvement in solid state technologies in the last 50 years most PAs now a days are made with transistor devices. There are several devices that can be used, including Si BJT, GaAs MESFET or in this thesis GaN HEMT. Transistors can operate at a wide range of power, are more compact, got a wide bandwidth and has low noise figure [5].

In Fig.1 a block diagram of a PA is shown. The three main building blocks in a PA are the input matching circuit, the output matching circuit and the transistor. The input matching should match the impedance presented to the signal source as close to the reference impedance as possible, which is usually 50Ω. This reduces the reflection back to the source and increases the small-signal gain of the PA. The output matching circuit should match the impedance seen by the output of the transistor close to the optimal load impedance. This gives the PA high output power as well as efficiency. Components for the matching circuits is usually made with microstrip lines or discrete components [5].

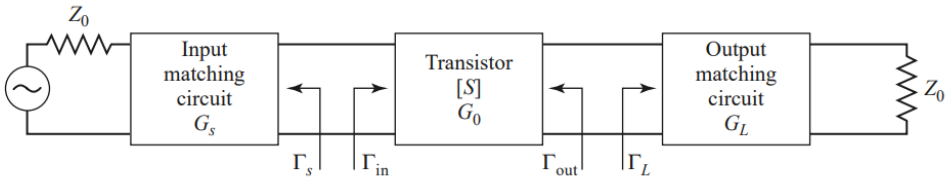


Figure 1: Block diagram of a PA, from [5].

2.2 Scattering parameters

Scattering parameters (S-parameters) are used to describe how a system with N-ports responds to an input signal at one of the ports. S-parameters are usually displayed in a matrix, with the number of cells in the matrix being 2^N [6].

In Fig.2 a two port system is depicted. The S-parameters can be divided into two groups, the reflection coefficients and the transmission coefficients. S_{11} and S_{22} are a complex number that usually represent the normalized

impedance of port one or port two. A normalized impedance is referred to the reference impedance Z_0, which is usually 50Ω. S_{11} and S_{22} can be plotted in a Smith-chart and the distance from the center and the phase, will be the reflection coefficient at the port. The magnitude of the reflection coefficient shows the ratio of the input signal that will be reflected and the phase shows the phase shift of the reflection. S_{12} and S_{21} are the transmission coefficients of a two-port system. The transmission coefficients show the ratio of the input signal that is transmitted to the other port and the phase shift of the signal transmitted. S_{ij} is the general form for a transmission coefficient, where i is the output port and j is the input port [6].

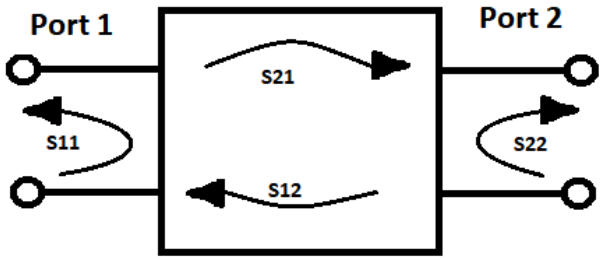


Figure 2: Two port system showing the reflection and transmission.

S-parameters are useful when designing an RF system, as they can help describing the gain, loss, stability and reflection of the system.

2.3 PA classes

The PA classes are generally divided into two groups, biased based classes and switching amplifiers. The biased based classes include class A, B, AB and C, while the switching amplifiers are class D, E and F. The biasing influences the current conduction angle of the PA, which in turn influences the PAs linearity, gain and efficiency. A higher conduction angle will result in a higher gain and linearity, at the cost of efficiency. Table1 shows how the conduction angle and efficiency correspond with the different biasing classes. Fig.3 illustrates this further [7].

Table 1: PA classes biasing

Class	Conduction angle	Maximum Efficiency
Class A	360°	50%
Class B	180°	78.5%
Class AB	180° to 360°	50% to 78.5%
Class C	less than 180°	more than 78.5%

Switching PAs class D and E will not be used in this project and will not be covered any further.

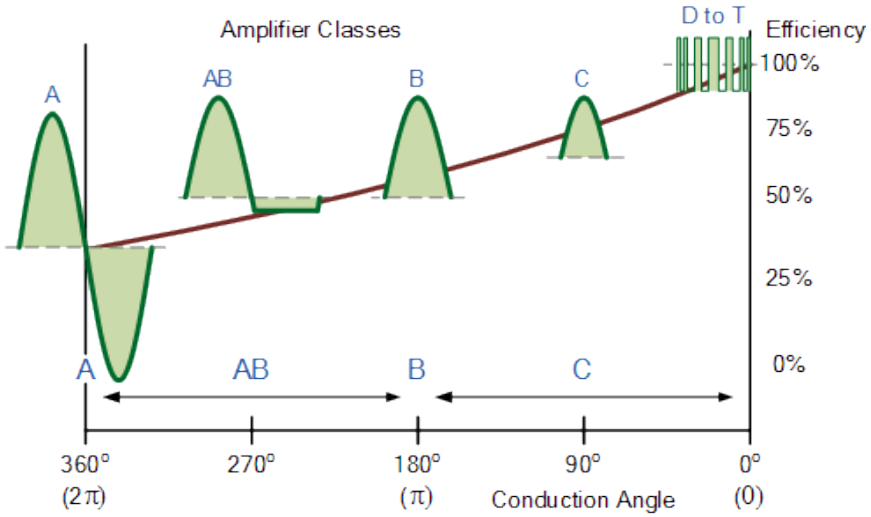


Figure 3: The biasing classes with the conduction angle and efficiency, from [8].

Class F PAs utilize harmonic resonators at the output network. The harmonics produced by the non-linear nature of the PA is used to shape the drain-source voltage. As the transistor conducts current when the drain source voltage is flat or low, a sharper slope on the drain-source voltage will reduce the DC power consumption. Increasing the number of harmonic resonators will cause the drain-source voltage to take on a square shape. With a fully square shape, the efficiency will be 100%. A class F PA is usually biased in the class AB or class B range. A block diagram of a class F amplifier is shown in Fig.4 [7].

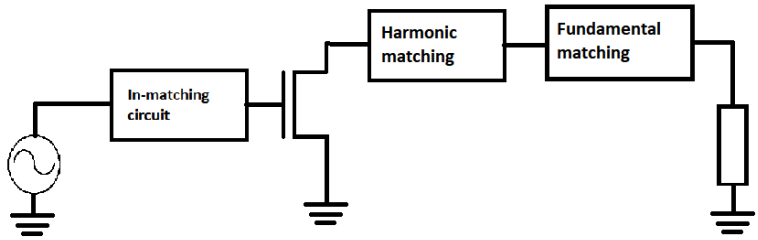


Figure 4: Block diagram of a class F PA.

2.4 Gallium Nitride RF transistors

GaN transistors appeared in the 1990s and offers a higher bandwidth and power at higher frequencies. Currently GaN components are grown on either silicon or silicon carbine. The bandgap of GaN being 3.49eV is much higher than 1.42eV in gallium arsenide and 1.1eV in silicon. This gives GaN a much higher breakdown voltage, making GaN transistors suitable for high power applications. GaN transistors also has a high saturation velocity, allowing a high current density. These two factors gives GaN transistors high power density. With a high power density GaN transistors can deliver high power with a small surface area. A small surface area will give the transistors less parasitics, allowing the GaN transistors to work in wide bandwidth applications [2].

2.5 Stability

To avoid unwanted oscillations at certain frequencies, it is important to keep the PA stable. If the reflection coefficient seen by the source $|\Gamma_{in}|$ or the load $|\Gamma_{out}|$ is greater than 1, the PA is unstable. The PA can either be unstable, conditionally stable or unconditionally stable. With unconditional stability the PA will not oscillate at any frequencies independent of the source and load impedance. Eq.[1] and Eq.[2] shows how these reflection coefficients are calculated. In Fig.1 one can see the reflection coefficients in a PA [9].

$$\Gamma_{in} = S_{11} + \frac{S_{12}S_{21}\Gamma_L}{1 - S_{22}\Gamma_L} \tag{1}$$

$$\Gamma_{out} = S_{22} + \frac{S_{12}S_{21}\Gamma_S}{1 - S_{11}\Gamma_S} \tag{2}$$

$$\Gamma_S = \frac{Z_S - Z_0}{Z_S + Z_0} \tag{3}$$

$$\Gamma_L = \frac{Z_L - Z_0}{Z_L + Z_0} \tag{4}$$

The stability in a PA is sorted into two categories. These are conditionally stability and unconditionally stability. Whether the PA is conditionally or unconditionally stable can be determined by looking at the μ factor and Rollets k factor [9].

Conditional stability is when $|\Gamma_{in}| > 1$ and $|\Gamma_{out}| > 1$ only for certain source and load impedance [9].

Unconditional stability is when $|\Gamma_{in}| > 1$ and $|\Gamma_{out}| > 1$ for all passive source and load impedance [9].

Rollets stability, or k factor shows whether a PA is stable or unstable and at which frequencies. The formula for the k factor is shown in Eq.[5] [9].

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{12}S_{21}|} \tag{5}$$

$$|\Delta| = |S_{11}S_{22} - S_{12}S_{21}| \tag{6}$$

μ **factor** and μ_{prime}, similarly to the k factor, shows whether a PA is stable and at which frequencies. The formulas for μ and μ_{prime} are shown in Eq.[7] and Eq.[8]. μ shows the distance from the center of the Smith chart to the closest input- and output stability circle. μ_{prime} gives the distance to the closest unstable input- and output stability circle. Both μ and μ_{prime} must be > 1 for the PA to be unconditionally stable [9].

$$\mu = \frac{1 - |S_{11}|^2}{|S_{22} - \Delta S_{11}^*| + |S_{12}S_{21}|} \tag{7}$$

$$\mu_{prime} = \frac{1 - |S_{22}|^2}{|S_{11} - \Delta S_{22}^*| + |S_{12}S_{21}|} \tag{8}$$

2.6 Gain and efficiency

Gain in a PA generally tells how much the input signal is amplified. The input signal can have its current, voltage or power amplified. In PAs the amplification of the power is of interest. The gain is an important parameter in PAs, as it determines how much input power the PA needs to reach a certain output power. Higher gain also gives a high Power-Added-Efficiency (PAE), which is also an important parameter. Power Gain, Available Power Gain and Transducer Power Gain are the three different types of gain in a PA[5].

Power Gain is given by the ratio between the output RF power at the load and the input RF power from the source. The power gain is independent of Z_s. Eq.[9] shows how the power gain is calculated [5].

$$G = \frac{P_L}{P_{in}} \tag{9}$$

Available Power Gain is given by the ratio between the power available from the two-port PA and the power available from the source. Eq.[10] shows how the available power gain is calculated [5].

$$G_A = \frac{P_{avn}}{P_{avs}} \tag{10}$$

Transducer Power Gain is given by the ratio between the power delivered to the load and the power available from the source. Eq.[11] shows how the transducer power gain is calculated [5].

$$G_T = \frac{P_L}{P_{avs}} \tag{11}$$

As the output power approaches the peak output level, the gain will start to decrease. This is called gain compression. The point where the curve of the actual delivered power is 1dB lower than the ideal curve, is called the 1dB compression point[10]. This is shown in Fig.5

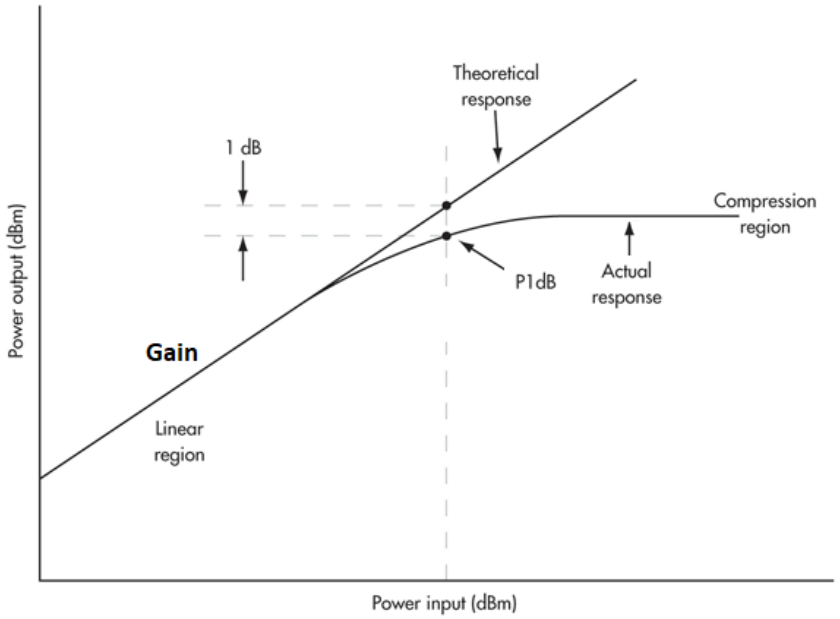


Figure 5: 1dB compression point, from [10].

The efficiency in a PA shows how efficiently the PA uses the DC power to amplify the power of an input signal. Efficiency in PAs are generally divided into three types, Drain Efficiency, Power Added Efficiency and Overall Efficiency[2].

Drain Efficiency, η describes the ratio between the output RF power and the DC supply power. Drain efficiency does not take the input RF power into consideration and can therefore be misleading, as a PA with high drain efficiency can have low gain[11]. Drain efficiency is calculated using Eq.[12].

$$\eta = \frac{P_{out}}{P_{DC}} \tag{12}$$

Power Added Efficiency (PAE), η_{PAE} is preferred by engineers as it uses the effective output RF power. This means that the input power is subtracted from the output power before dividing by the DC supply power. This results in gain being added into the formula and will be important to get a high PAE[11]. PAE is calculated using Eq.[13].

$$\eta_{PAE} = \frac{P_{out} - P_{in}}{P_{DC}} \tag{13}$$

Overall Efficiency, $\eta_{overall}$ is the ratio between the output power and the DC power added to the input power. This shows how well the PA amplifies the input RF power in relation to the DC- and input RF power [2]. Overall efficiency is calculated using Eq.[14].

$$\eta_{overall} = \frac{P_{out}}{P_{DC} + P_{in}} \tag{14}$$

2.7 Efficiency and linearity improvement techniques

Most of modern wireless transmission use some sort of amplitude and phase modulation, an example is QAM. Modulation of the amplitude causes the transmitted signals to have a high Peak-to-Average-Power-Ratio (PAPR). Multi carrier transmission further increases the PAPR[12]. PAPR refers to the ratio between the peak power and the average power in a signal, expressed in dB. High PAPR reduces the efficiency in the amplifier stage in a transmitter, as the efficiency in a PA is highly dependent on the output power [13]. Low efficiency in PAs decreases the battery life in mobile equipment and introduces problems with thermal management [7]. Signals with high PAPR will drive the PA into compression which introduces non-linearities. Transmitting data using amplitude modulation and phase modulation introduces requirements in the linearity of the PA to decrease the error in the transmitted data. In this section some efficiency- and linearity enhancing techniques will be presented.

Linearizing techniques that will not be described in this thesis include digital predistortion, negative feedback and feed forward.

2.7.1 Envelope tracking

Fig.6 shows the main issue with using a fixed supply voltage in a PA. With a low output voltage swing, most of the power will be dissipated as heat. As the voltage swing increases, the PA goes into compression and more power is transmitted and less dissipated. By modulating the supply voltage as a function of the envelope of the baseband signal, one can keep the PA running close to compression. This is called envelope tracking or ET and increases the efficiency over a large range of input power, compared with a PA with a fixed supply voltage [7].

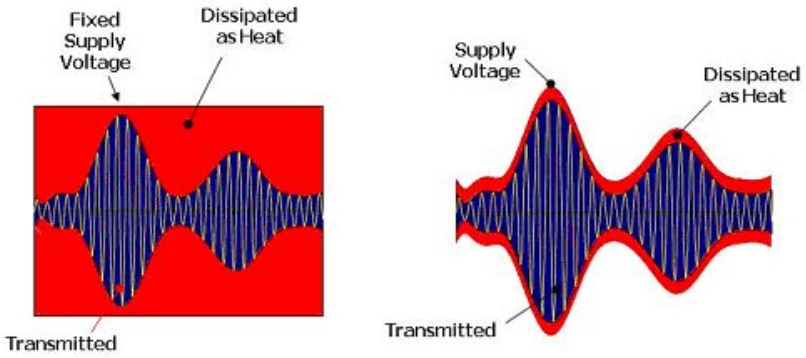


Figure 6: Power dissipation in a PA, from [14].

Fig.7 shows the block diagram of an envelope tracking PA. The input signal is split into two paths. One path leads into an envelope detector followed by a supply modulator or envelope tracker. The output of the envelope tracker will be used as the supply voltage in the PA. The other path leads into a delay followed by the input of the PA.

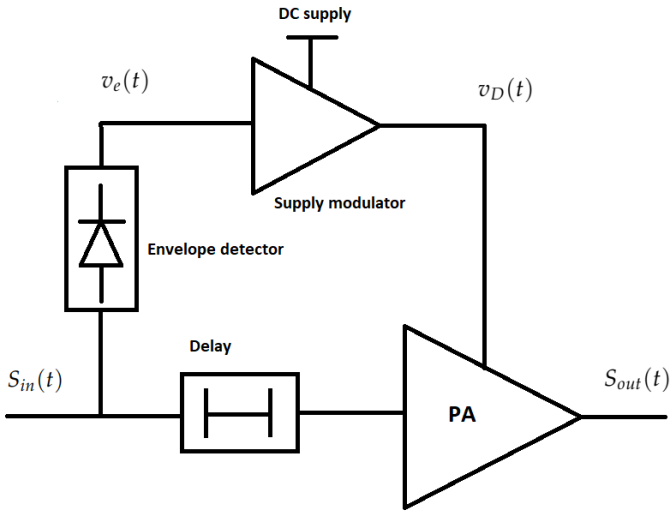


Figure 7: Block diagram of an envelope tracking PA.

A complex time varying baseband signal can be described by Eq.[15]. The envelope of this signal, $v_e(t)$ is the absolute value of $v(t)$ can be described by Eq.[16].

$$v(t) = v_I(t) + j * v_Q(t) \tag{15}$$

$$v_e(t) = |v(t)| = \sqrt{v_I(t)^2 + v_Q(t)^2} \tag{16}$$

2.7.2 Power envelope tracking

One limiting factor of ET is the bandwidth required by the tracker to track the envelope. This problem can be demonstrated using Eq.[16]. A square root can be represented as an infinite power series, shown in Eq.[17]. This causes the theoretical bandwidth of the envelope to approach infinite, $B \rightarrow \infty$ [2].

$$\sqrt{x+1} = 1 + \frac{1}{2}x + \frac{1}{8}x^2 + \frac{1}{16}x^3 + ... \tag{17}$$

Thus the tracker is required to have an infinite bandwidth to track the envelope fully, which is impossible. Usually a compromise is made between bandwidth and practicality, and a bandwidth of $6 * B_{BB}$ is used for the tracker, with B_{BB} being the bandwidth of the baseband signal. The bandwidth of the supply voltage is shown in Fig.8 [2].

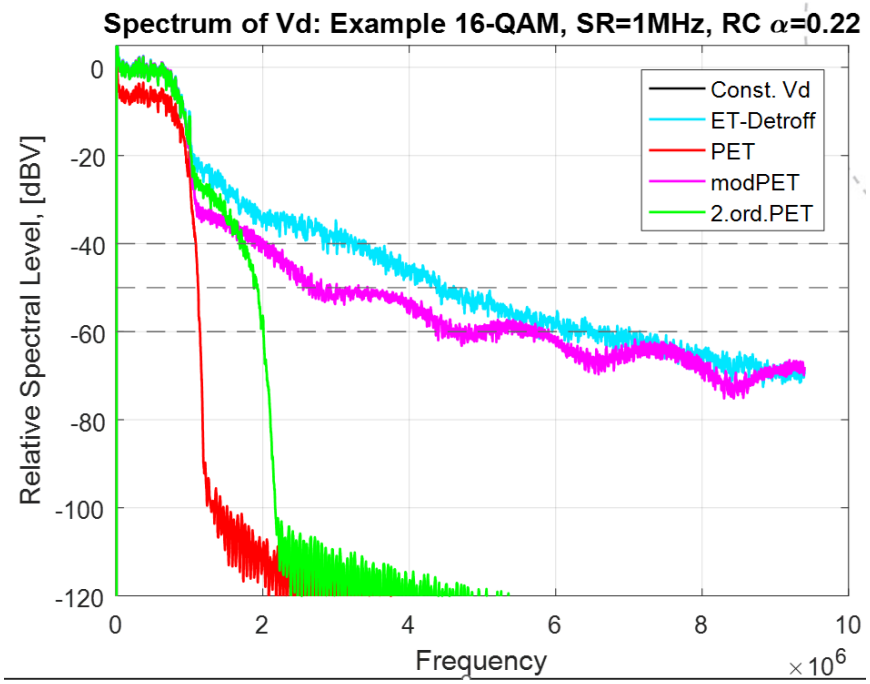


Figure 8: Bandwidth of the drain voltage for ET, PET and constant V_D, from [15].

A possible solution to this problem was presented by Morten Olavsbråten and Dragan Gecan in 2017. By tracking the power of the input signal instead of the voltage one can remove the square root, as shown in Eq.[18]. This drastically reduces the bandwidth to $2 * B_{BB}$ [3].

$$p_e(t) = |v_e(t)|^2 = v_I(t)^2 + v_Q(t)^2 \tag{18}$$

This method is called power envelope tracking (PET). It is shown that a 2nd order PET can give an improvement in efficiency close to ET. As the envelope tracker does not track the voltage but the power, the efficiency will not be as good as with ET. Eq.[19] and Eq.[20] show the tracking functions of a 1st order and 2nd order PET [3].

$$v_D(t) = a_0 + a_1 * p(t) \tag{19}$$

$$v_D(t) = a_0 + a_1 * p(t) + a_2 * p(t)^2 \tag{20}$$

2.7.3 Doherty amplifier

The main components in a Doherty amplifier are the main PA and the auxiliary PA, and two $\lambda/4$ lines. The main PA is usually biased in class AB and is designed to be most efficient at the lower and average power levels and will clip the signal at higher input power levels. The auxiliary PA is usually biased in class C and only conducts current when the input signal reaches a certain power level. This technique makes both PAs operate in their most efficient region and thus increasing the over all efficiency and linearity [7].

2.7.4 Envelope elimination and restoration

An amplitude modulated and phase modulated signal can be represented using Eq.[21]. Envelope elimination and restoration (EER) involves separating these two parts of the signal before the amplifying stage, to increase the linearity and efficiency of the PA. The separation is done using an envelope detector for the AM part and a limiter for the PM part. The voltage can be represented with Eq.[22] for the AM signal and Eq.[23] for the PM signal. Proceeding the envelope detector the AM signal $v_m(t)$ is amplified using a low frequency (LF) PA with a voltage gain of A_v producing a modulating voltage $A_v * v_m(t)$. The PM signal is usually amplified by a high efficiency switch mode PA. A switch mode PA will have an output amplitude that is directly proportional to the supply voltage. Using the modulating voltage $A_v * v_m(t)$ as the switch mode PA's supply voltage, the resulting amplified output signal can be represented as $v_o(t) = A_v * v_m(t) * v_{PM}(t)$. [7].

$$v_i(t) = V(t) * cos(\omega_c * t + \theta(t)) \tag{21}$$

$$v_m(t) = V(t) \tag{22}$$

$$v_{PM}(t) = V_c * cos(\omega_c * t + \theta(t)) \tag{23}$$

2.7.5 Outphasing amplifier

An outphasing amplifier is made with two identical non-linear PAs, with high efficiency. The input signal is separated into two constant amplitude and variable phase signals, that will summarize into the input signal. Each

signal is amplified by the two amplifiers and added together, using a power combiner. The sum of these two signals will be an amplified version of the input signal [1].

2.7.6 Gate tracking

Using PET on the drain voltage can cause the phase shift through the PA to change as a function of the input power. The phase shift through a PA based on a GaN transistor can also be changed by modulating the transistors gate voltage. This is demonstrated in Fig.9. The gate voltage in a GaN transistor in a PA is increased and one can observe that the phase decreases as the gate voltage increases.

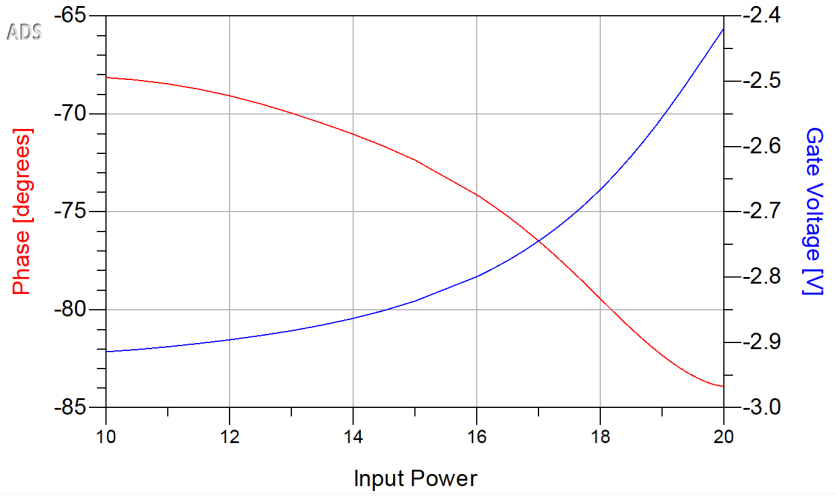


Figure 9: Gate voltage in blue and phase in red.

By tracking the power envelope of the baseband signal the gate voltage can be modulated the same way as the drain voltage. A combination of gate and drain modulation can give a highly linear PA, in regards to both phase and gain [2]. A higher order formula can be used with the gate tracker. When designing a tracker one usually have to make a compromise between bandwidth, output power and efficiency. The power delivered by the gate tracker is much lower than the drain tracker, so the bandwidth can be increased. As a result of this the order of the gate tracking function should be as high as the bandwidth supported by the tracker. A 4th order tracking function is shown in Eq.[24].

$$v_G(t) = b_0 + b_1 * p(t) + b_2 * p(t)^2 + b_3 * p(t)^3 + b_4 * p(t)^4 \quad (24)$$

2.8 Methods for measuring linearity

To judge the linearity of a PA three methods will be used in this thesis. Error Vector Magnitude (EVM) measures the accuracy of the transmitted symbols within its constellation. Adjacent Channel Power Ratio (ACPR) shows how much of the transmitted signal that leaks into the adjacent channels. Signal to Total Distortion Ratio (STDR) shows the distortion happening both inside and outside of the baseband.

2.8.1 AM-AM and AM-PM distortion

The relation between the amplitude of the output signal and the amplitude of the input signal is called AM-AM distortion. The relation between the phase of the output signal and the amplitude of the input signal is called AM-PM distortion [2].

2.8.2 Memory Effect

Memory Effects in a PA are additional sources of non-linearity usually not included in PA models. These sources of non-linearity are deviations from the static characteristics of the PA and make it hard to predict the response of the PA to a modulated signal. The Memory Effects are caused by three phenomenons, dynamic thermal effects, unintentional supply rail modulation and semiconductor trapping effects[16]. One can measure the memory effects using dynamic amplitude distortion (AM/AM) and phase distortion (AM/PM), as well as swept two-tone measurements[17].

2.8.3 EVM

The symbols transmitted from a non-ideal transmitter will not align with their ideal position in the constellation diagram. This error is caused by distortion inside the signals bandwidth. This error is caused by the AM-AM and AM-PM distortion, that causes error in the phase and the amplitude of the output signal [2]. This is depicted in Fig.10, with the measured signal vector having an error in its magnitude and phase compared with the

reference signal vector. The EVM can be expressed either in dB or as a percentage. A transmitted signals EVM is calculated using Eq.[25] or Eq.[26] [18].

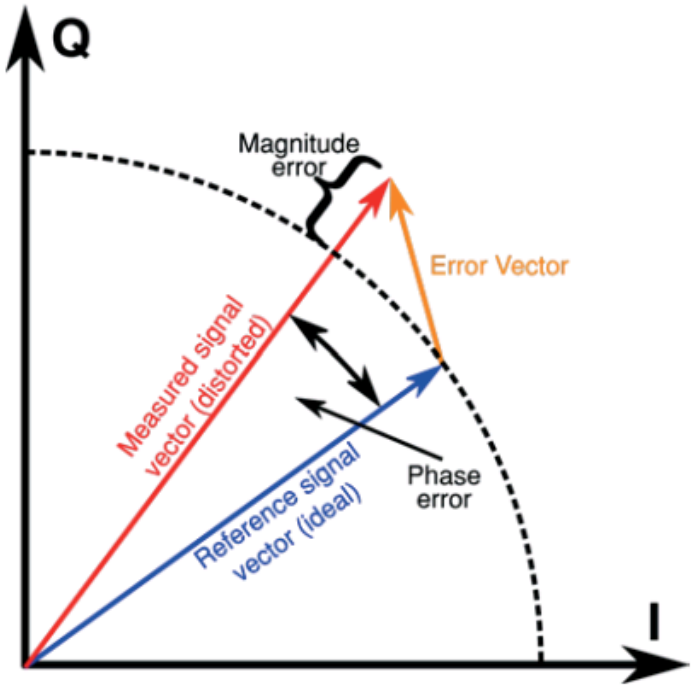


Figure 10: EVM distortion demonstrated in a constellation diagram, from [2].

$$EVM_{dB} = 10log_{10}(\frac{P_{Error}}{P_{Ideal}}) \tag{25}$$

$$EVM_{\%} = \sqrt{\frac{P_{Error}}{P_{Ideal}}} * 100\% \tag{26}$$

2.8.4 ACPR

ACPR measures how much the signal power spreads into neighbouring channels, which is the distortion outside the baseband signals bandwidth. ACPR is measured in dBc, which means in relation to the carrier. The ACPR

is calculated by dividing the power of the signal in the neighbouring channels by the power inside the bandwidth of the signal, shown in Eq.[27][2].

$$ACPR = \frac{P_{Adjacent}}{P_{Main}} \tag{27}$$

2.8.5 STDR

STDR was presented by Morten Olavsbråten and Dragan Gecan and measures the distortion happening to the transmitted signal inside and outside the bandwidth of the signal. It includes both the distortion happening due to non-linear distortion and the Memory Effects, both inside and outside the bandwidth of the baseband signal [2].

The STDR is presented as the inverse of the Nonlinear Linear Power Ratio (NLPR) and is calculated using Eq.[28]. With I_a being the average input power and I_b being the average output power. I_x is the mixing product of the input and output signal [2].

$$STDR = 10log(\frac{I_a I_b}{I_a I_b - |I_x|^2}) \tag{28}$$

3 Method

3.1 Power Amplifier

Design, simulation and layout is done using Advanced Design System (ADS), by Keysight. The PA is designed on a two layer stack using FR4 as the substrate. The stack's parameters are shown in Table2. The PA is using two amplifying stages using two GaN, High-Electron-Mobility-Transistors (HEMT) from Cree. The 1st stage uses the 10W CG2H40010 transistor, while the 2nd stage uses the 25W CG2H40025 transistor. The PA's general specification requirements are shown in the introduction.

Table 2: Parameters of substrate stack

Parameter	**Value**	**Unit**
H	1.473	mm
ϵ_r	4.46	
Mur	1	
Cond	5.8e7	
Hu	1e36	μm
T	0.035	mm
TanD	0.019	

A PA used with PET will have some additional requirements compared to a PA with fixed supply voltage. The PA must be stable regardless of the supply voltage in the two stages. This is because the voltage at the drain and the gate will be fluctuating when they are modulated by the tracker. Additionally the shunt capacitors in the DC feed must be kept small to keep the charge-up time short during the modulation. A larger capacitance will help with the stability as they provide a low impedance path to ground.

The PA is a two-stage class F amplifier and it is made with six main parts, the DC feeding circuit, the input match, the 1st amplifying stage, the combined matching circuit with harmonic tuning, the 2nd amplifying stage and the output matching with harmonic tuning. Each part will be described further in this chapter. The final layout is shown in Fig.11. Using a two-stage PA gives a higher degree of freedom when it comes to tracking. In comparison a PA with one stage can have the gate voltage and drain the voltage modulated, while a two-stage PA can potentially have the voltage at both gates and both drains modulated. This should increase the performance. A two-stage PA will also give a higher gain than a PA with one stage, as the signal gets amplified twice.

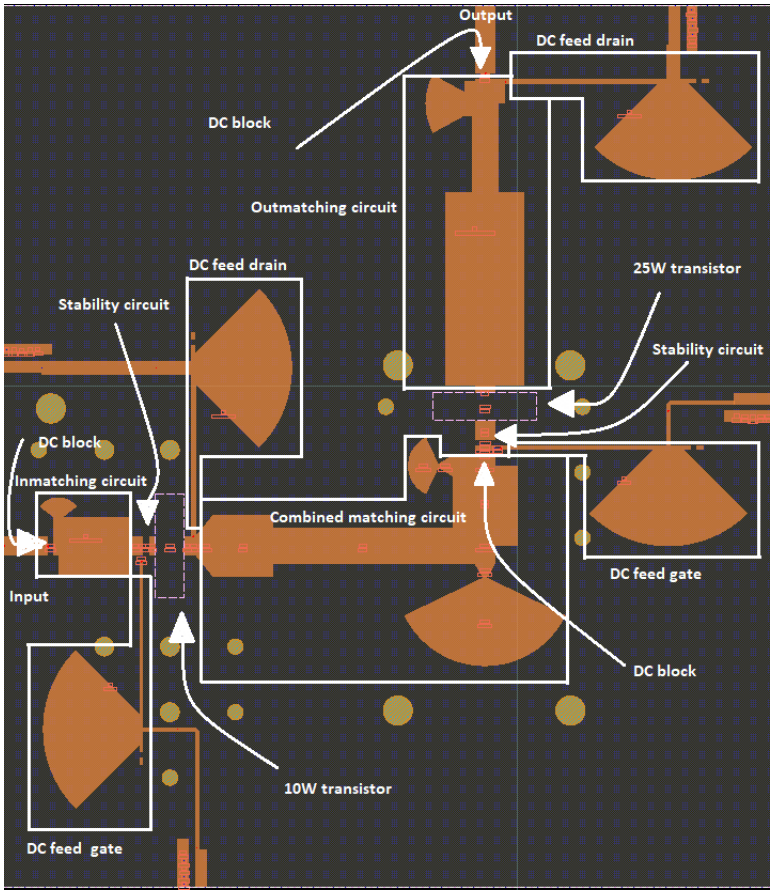


Figure 11: Final layout of the PA.

3.1.1 Bias point

Both amplifying stages are biased in class AB due to the compromise between gain, linearity and efficiency in this class. Due to the non ideal harmonic tuning in the matching circuits, the bias point will have a significant influence on the efficiency. The 1st stage is biased slightly closer to class B with $V_G = -2.85V$ giving $I_D = 70mA$, than the 2nd stage with $V_G = -2.8V$ giving $I_D = 200mA$.

3.1.2 DC feed or RF choke

As the DC source is a short circuit for RF signals, a DC feed or RF choke is needed. The DC feed is made using an open $\lambda/4$ line which is seen as a

short circuit at f_c. Transforming this short circuit with a $\lambda/4$ line in series creates an open circuit. This configuration is shown in Fig.12 and presents a high impedance from the transistor to the DC source at 2GHz. S_{11} plotted in a Smith chart is shown in Fig.13, showing a high impedance and close to full reflection.

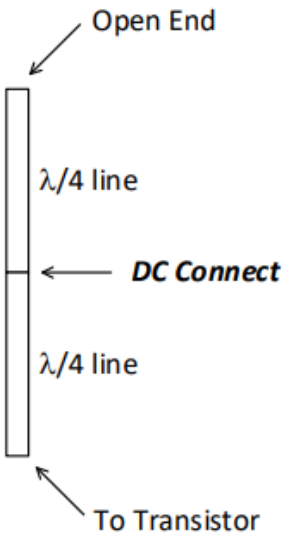


Figure 12: [19]

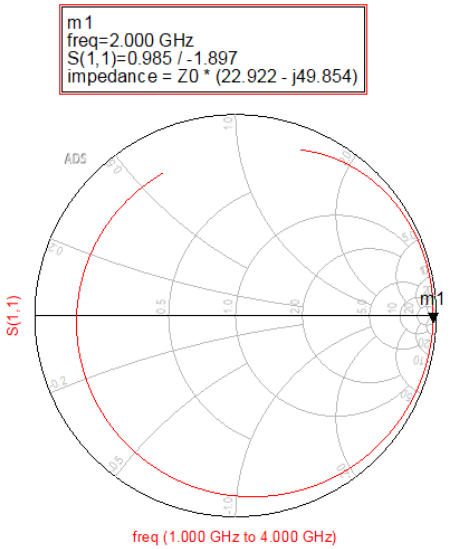


Figure 13: S_{11} plotted in a Smith chart

The width of the DC feed at the drain of the transistor influences the efficiency and the peak output power of the PA. A wider line will have less resistance and therefore the DC power loss over this line will be lower thus resulting in higher efficiency. The transformation from short circuit to open circuit will be worse with a wider line, due to the lower impedance in the line. This will result in higher RF leakage. A compromise between efficiency and peak output power is made and a line width of 0.7mm is used. The DC current in the DC feed at the gate will be low and only due to gate leakage in the transistor. Therefore the line width in the DC feed at the gate is thin to avoid RF leakage. RF leakage at the gate will negatively influence the gain. A line width of 0.6mm is used.

As the PA will be used in supply voltage modulation the shunt capacitors at the DC connection needs to be low to decrease the charge time. The capacitance is tuned to keep the PA unconditionally stable while keeping the capacitance low. A 5.9pF capacitor is used in both the DC feed at the gate and at the drain. A 150Ω resistor is added in series to the DC feed at the gate to help with the stability. The schematic of the DC feed is shown in Fig.14.

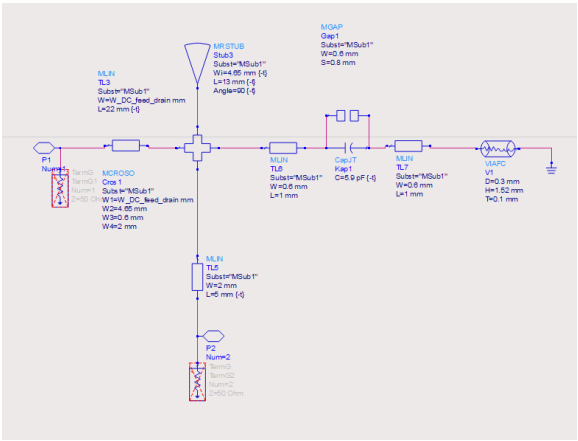


Figure 14: Schematic of the DC feed

3.1.3 Stability circuit

The PA is kept stable by introducing loss at the input of the two transistors. This loss is made by an RC circuit that will give more loss at lower frequencies. This circuit affects both the small signal gain, peak output power and efficiency. A larger resistance and capacitance in the RC circuit will give more output power and higher efficiency, but decreases f_c. Both stages uses a 47Ω resistor and a 4.7pF capacitor, making the PA unconditionally

stable regardless of the supply voltage and inductance in the supply cable.

3.1.4 Matching circuits

The input matching circuit will present the input of the 1st stage with a complex conjugate of the input impedance of the 1st stage transistor in series with the stability circuit without any matching. This can be achieved with an open microstrip line and a microstrip line in series. The input matching circuit is optimized to get high small signal gain with a 1dB bandwidth of >0.1GHz, stability and a reflection <-10dB.

The output matching circuit of the 2nd stage will present resonators to the harmonics giving the voltage curve a square shape. This will result in a high efficiency. The total length of the circuit will give more conduction loss in the lines, causing the number and size of the microstrip structures to be kept at a minimum. This circuit is optimized to give high peak output power and PAE. This circuit is composed of two microstrip lines in series with different width, an open stub and a line in series.

The combined matching circuit needs to be close to a complex conjugate of the input impedance of the transistor in the 2nd stage in series with the stability circuit without any input matching. In addition a harmonic tuned output match for the 1st stage. This circuit is optimized to give flat gain from 1.9GHz up to 2.1GHz and high PAE. This circuit is designed using two open microstrip stubs and three microstrip lines in series.

The connection point between the lines in series and the stubs is a T-junction. T-junctions have a model in ADS that has a range of usage to make the model work properly. One rule is that the width of the largest connected line can not be more than five times the width of the smallest line [20]. If this rule is not followed in the matching circuits a tapered line will be placed between the line and the connection of the T-junction. This is shown in Fig.15.

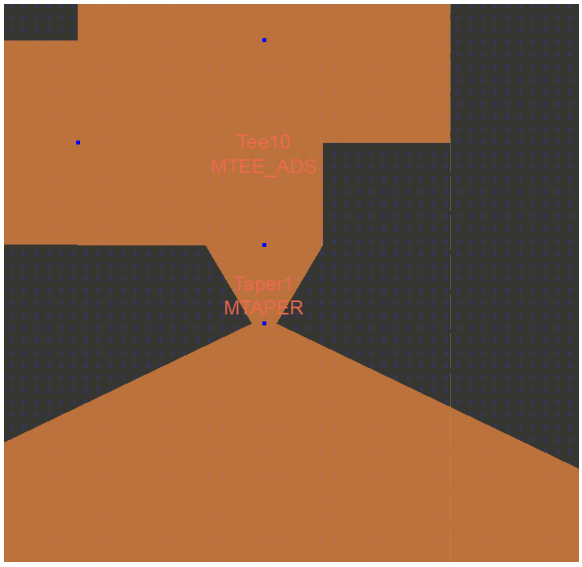


Figure 15: Taper component in ADS.

3.2 Tracking formula

The coefficients needed in the tracking formulas will firstly be determined and tested using simulation in ADS. In simulation three tracking formulas will be tested and compared. The combinations of PET formulas used in simulations are shown in Table3.These combinations will also be tested on the physical PA and can be compered with the simulations.

Table 3: Tracking formulas

V_G **1st stage**	V_D **1st stage**	V_G **2nd stage**	V_D **2nd stage**	**Goal**
Fixed	1st order PET	Fixed	1st order PET	High PAE
Fixed	Fixed	Fixed	1st order PET	Flat gain
4th order PET	Fixed	Fixed	1st order PET	Flat gain, flat phase

3.3 Testing

The PA's small-signal and large-signal parameters will be determined and later compered to the simulated values. After determining the small-signal and large-signal parameters, the coefficients of the different PET functions must be found.

Before any measurements can be performed the PA needs to be powered

on gradually to check for oscillations. In case of oscillations a $1\mu F$ shunt capacitor can be added in the DC feed circuits. The two stages will be powered on separately with a drain voltage of 8V. The gate voltage giving close to the desired current must be found, as the threshold voltage tolerance in GaN is high. Later the correct gate voltage giving 70mA in the 1st stage at a drain voltage of 20V and 200mA in the 2nd stage at a drain voltage of 28V must be found. The needed equipment for both the small-signal analysis, the large-signal analysis and during tracking measurements is shown in Table4.

Table 4: Testing equipment

Equipment	**Name**
Vector Network Analyzer	Pico Technology, PicoVNA 108
VNA cables	
Calibration kit (SOLT)	Pico Technology, SOLT-STD-F
20dB attenuator	
Power supply	AimTTi CPX200DP
Vector signal generator	Rohde and Schwarz, SMU200A
Signal analyzer	Rohde and Schwarz, FSQ40
Circulator	Uiy
Tracker	Designed by Morten Olavsbråten

3.3.1 Small-signal analysis

The small-signal analysis will be performed in order to characterise the reflection coming from the input of the PA S_{11} and the small-signal gain S_{21}. The reflection from the output S_{22} and the isolation S_{12} will also be characterised, but due to the lack of requirements regarding these two S-parameters they will not be shown or discussed.

In Fig.16 the setup needed to perform the small-signal analysis is shown. A two port Vector Network Analyzer (VNA) will measure the S-parameters of the PA. The two ports of the VNA will be connected to the input and the output of the PA. If the PA oscillates, the output power will increase and exceed the max input power of the VNA port and this can damage the VNA. To prevent the output power to exceed this limit, an attenuator will be placed between the output of the PA and the 2nd port of the VNA.

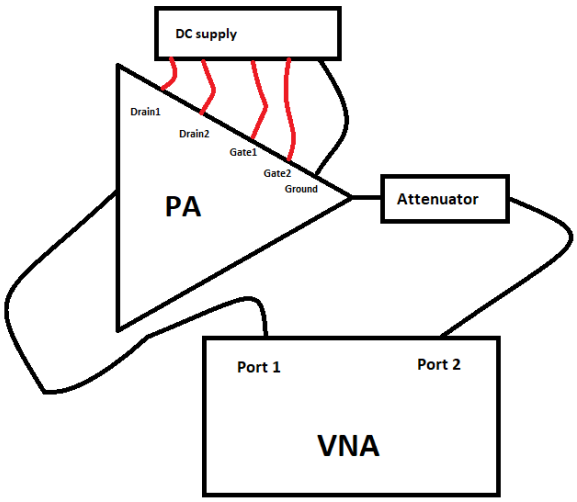


Figure 16: Block diagram showing the setup of small-signal analysis.

In order to only measure the parameters of the PA and not the loss and phase delay in the cables and the attenuator, a calibration is performed. This calibration is a Short-Open-Load-Through (SOLT) calibration and is performed at the placement of the PA. After the SOLT calibration is performed the VNA will only display the S-parameters of the PA.

3.3.2 Large-signal analysis

Performing a large-signal analysis will characterise the transducer power gain, peak output power and the PAE as a function of the input power. Fig.17. shows the setup needed to perform this analysis.

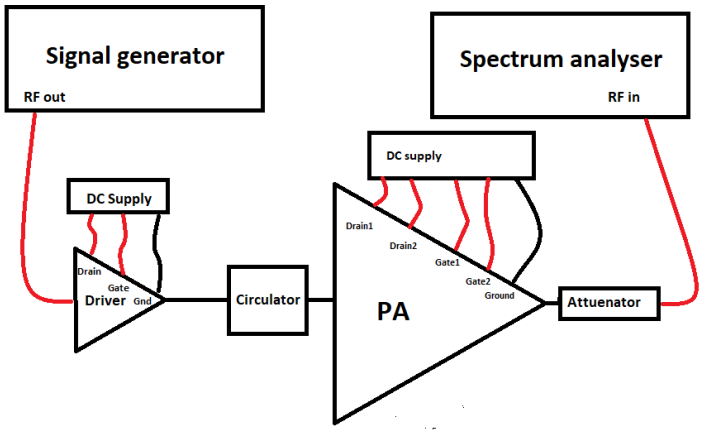


Figure 17: Block diagram showing the setup of large-signal analysis.

A signal generator is used to generate a 2GHz signal. This signal generator is not able to generate a clean output power high enough to drive the PA into compression. Therefore a driver is placed between the signal generator and the PA, that amplifies the output signal from the signal generator. A circulator is also added between the driver and the PA to terminate any reflection from the PA to the driver, it will also present 50Ω to the input of the PA. Following the PA an attenuator is added to prevent the output power of the PA to exceed the maximum rated input power of the spectrum analyser. All loss added by the cables, attenuator, circulator and the gain in the driver is removed by calibration. The test and the calibration is controlled using a Matlab script.

3.3.3 Envelope tracking

Before the tracking of the PA is performed, the coefficients used in the tracking formulas needs to be determined. As the testing will include both V_D modulation separately and in combination with V_G modulation, two different procedures will be used to find the coefficients. The coefficients used when only modulating the V_D will be determined by sweeping V_D from 6V up to 30V. Then one can find the different values for V_D giving flat gain or high PAE. This can be done at one amplifying stage or both amplifying stages. Only 1st order PET and ET will be tested during measurements.

Finding the coefficients used with modulation of V_G in the 1st stage and V_D

in the 2nd stage is slightly more complicated. For simplicity the formula for V_G modulation will only use a constant and either a 1st order or 2nd order coefficient. This is shown in Eq.[29] and Eq.[30]. The goal of the V_G formula is to compensate for the non-linear phase shift in the PA and the coefficients can be modified to better the linearity. After the coefficients in the V_G modulation formula is determined, one can sweep V_D from 8V up to 30V and pick the the different values for V_D giving flat gain and as high PAE as possible.

$$v_G(t) = a_0 + a_1 * p(t) \tag{29}$$

$$v_G(t) = a_0 + a_2 * p(t)^2 \tag{30}$$

A Matlab script is used to generate a 5MHz 16QAM signal that is used to modulate a 2GHz signal. This modulated signal is amplified by a driver in order to get the correct input power for the PA. A circulator is placed in between the driver and the PA to terminate reflections from the PA and present 50Ω to the input. The envelope of the generated 16QAM signal is used to calculate the envelope of the signal which is used to generate a voltage that is fed to the envelope trackers. A block diagram of the setup used during the tracking is shown in Fig.18. The difference in delay between the tracker and the input if the PA is compensated for in the Matlab script.

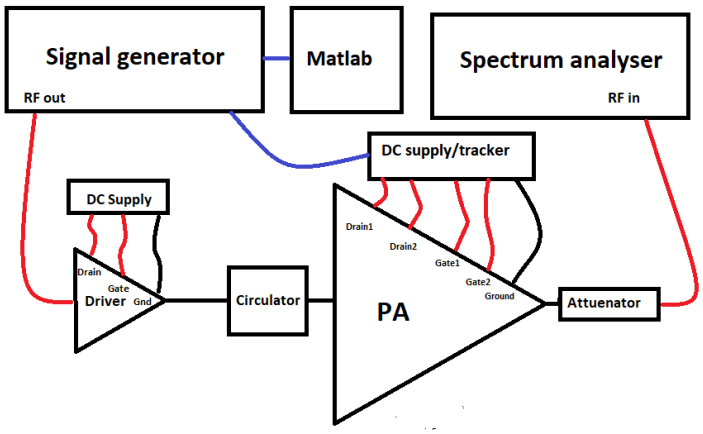


Figure 18: Block diagram showing the setup of the tracking.

4 Power Amplifier results

4.1 Simulated Small-signal parameters

The small-signal gain S_{21} and reflection S_{11} will be determined using an S-parameter analysis. The S-parameters can be used to calculate the μ for the source and the load of the PA, as well as the k factor. This is shown in Chapter2. As the PA will be powered by an external power supply with a cable, the cable inductance needs to be added in the test bench. This inductance can worsen the stability. The cable inductance in the test bench should be varied to check for instability at any inductance. The test bench in shown in Fig.19.

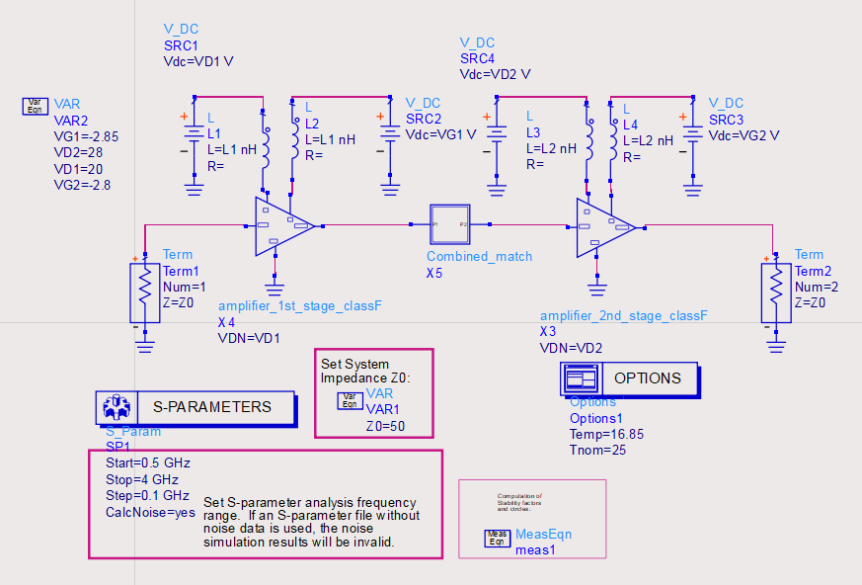
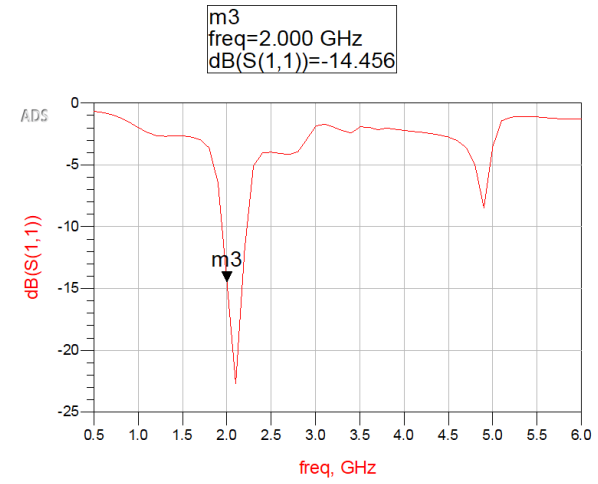


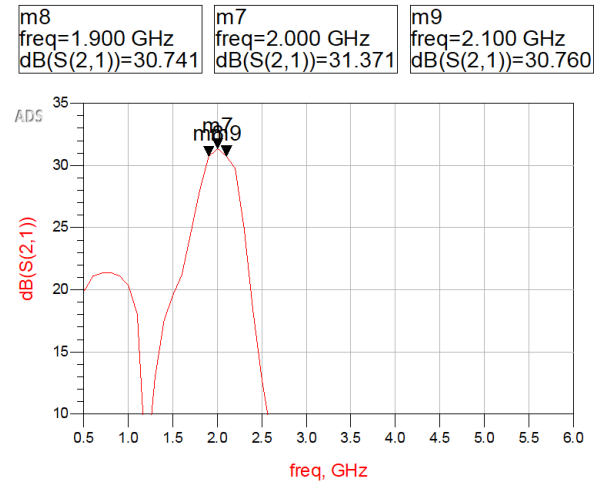
Figure 19: Test bench for the Small-Signal analysis

An S-parameter analysis is performed with $V_D = 20V$ and $V_G = -2.85V$ for the 1st stage and $V_D = 28V$ and $V_G = -2.8V$ for the 2nd stage, with a cable inductance of 100nH at the gate and drain in both the stages. A frequency range of 0.5GHz to 6GHz is used to secure the stability. The results from the analysis is shown in Fig.20. Fig.20a shows S_{11} to be -14dB at 2GHz. Fig.20b shows the small-signal gain S_{21} in dB to be 31dB at 2GHz and the 1dB bandwidth is > 100MHz. Fig.20c shows the μ factor for the source and the load as well as the k factor, which are > 1 for the whole frequency range. A parameter sweep of V_D from 6V to 30V, V_G from -3V to -2.4V and cable inductance ranging from 10nH to 100nH shows that the

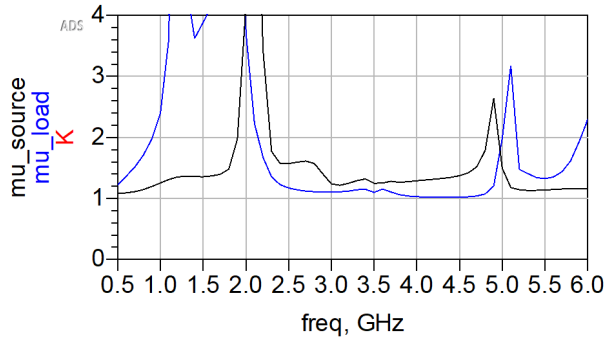
unconditional stability still holds true.



(a) S_{11}



(b) S_{21}



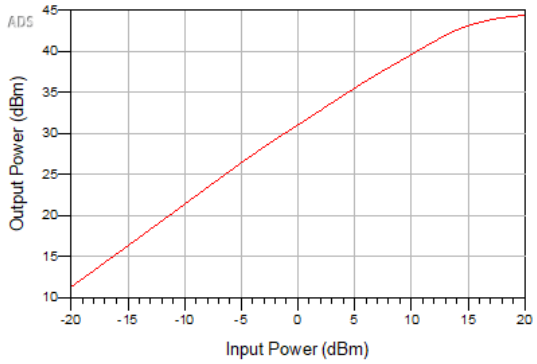
(c) μ source, μ load and Rollets k factor

Figure 20: Simulated S-parameters and μ source, μ load and Rollets k factor at V_D and V_G being 20V and -2.85V at 1st stage and 28V and -2.8V at the 2nd stage.

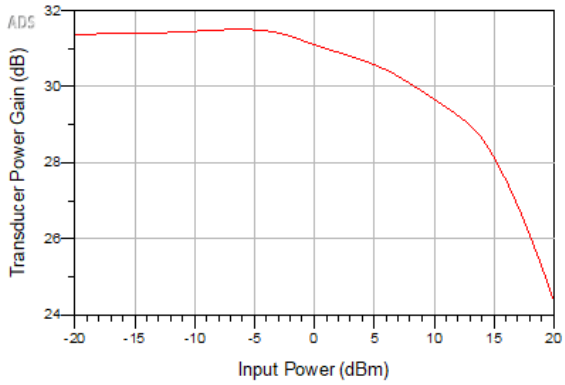
4.2 Simulated Large-signal parameters

The large-signal analysis will determine the peak output power, the transducer power gain and the PAE. The analysis will be carried out with $V_D = 20V$ and $V_G = -2.85V$ for the 1st stage and $V_D = 28V$ and $V_G = -2.8V$ for the 2nd stage. With a high V_D on the 2nd stage, the peak output power will be higher and the peak PAE will be higher for a high V_D in both stages.

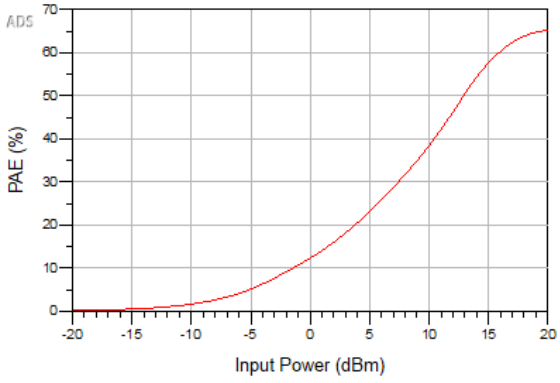
Fig.21 shows the results from the large-signal analysis as a function of the input power. Fig.21a shows the output power delivered by the PA. The 1dB compression point is reached at an input power of about 5dBm and the peak output power is 44.3dBm or 27W. Fig.21b shows the transducer power gain and it peaks at 31.4dB. The PAE is plotted in Fig.21c and is 65%.



(a) Output Power delivered by the PA.



(b) Transducer Power Gain.



(c) PAE.

Figure 21: Simulated output power, transducer power gain and PAE at V_D and V_G being 20V and -2.85V at 1st stage and 28V and -2.8V at the 2nd stage.

4.3 Measurements

When measuring the parameters with a fixed voltage at the drain and gate, a 1μF capacitor was added in the DC feeding circuit to insure unconditional stability. This capacitor will be removed during testing of PET. The gate voltage giving 70mA at the 1st stage is -2.37V and the gate voltage giving 200mA at the 2nd stage is -2.46V. Fig.22 shows the setup used for the small-signal analysis and Fig.23 shows the setup used for the large-signal analysis.

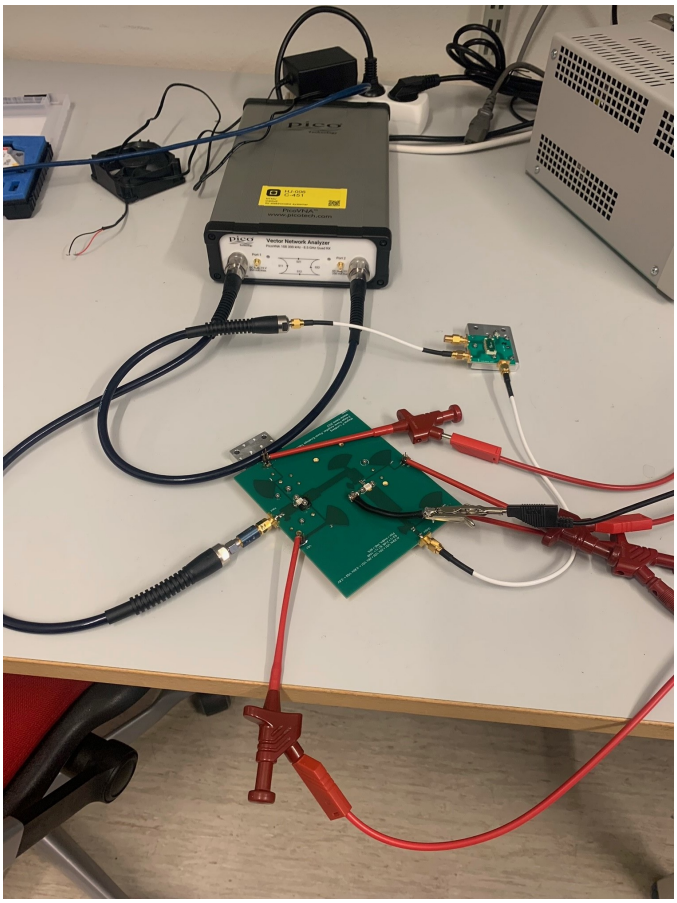


Figure 22: Setup used for small-signal measurements.

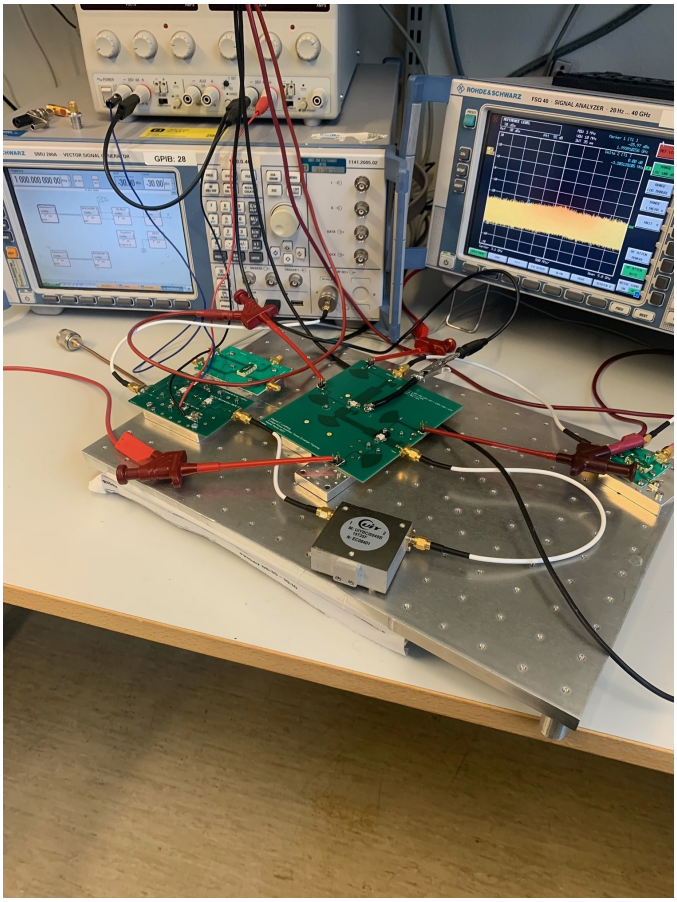
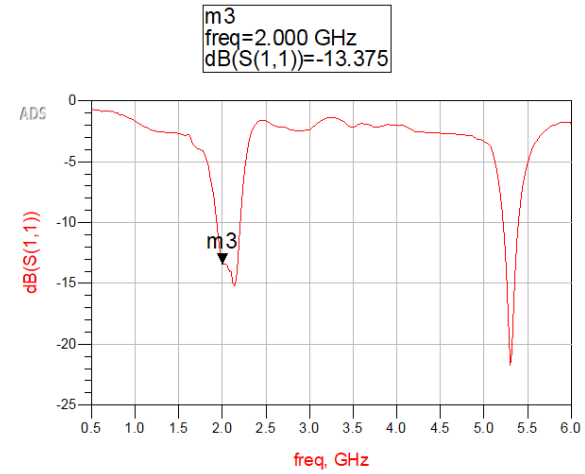


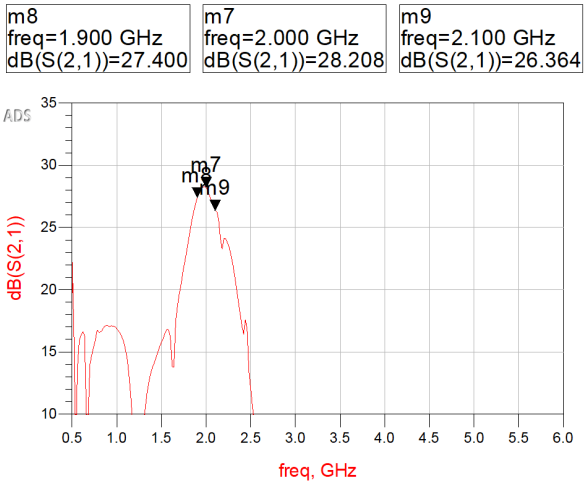
Figure 23: Setup used for large-signal measurements.

4.3.1 Measured Small-signal parameters

The PA is powered using an external power supply with $V_D = 20V$ and a drain current of 70mA at the 1st stage and $V_D = 28V$ and a drain current of 200mA at the 2nd stage. The measured S-parameters from the VNA is shown in Fig.24. S_{11} is shown in Fig.24a and is equal to -13dB at 2GHz, at 5.2GHz S_{11} is lower than -20dB. The small-signal gain S_{21} is shown in Fig.24b and is equal to 28.2dB and the center frequency is 2GHz. The 1dB bandwidth is 100MHz when the frequency is reduced, but not when it is increased.



(a) S_{11}.

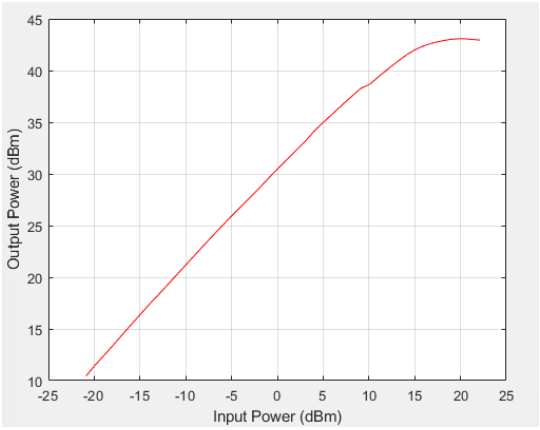


(b) S_{21}.

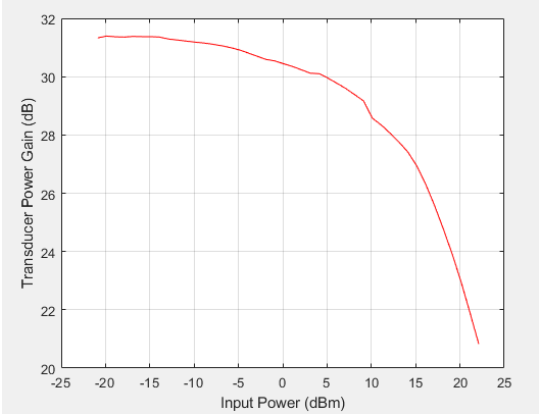
Figure 24: Measured S-parameters with V_D and drain current being 20V and 70mA at 1st stage and 28V and 200mA at the 2nd stage.

4.3.2 Measured Large-signal parameters

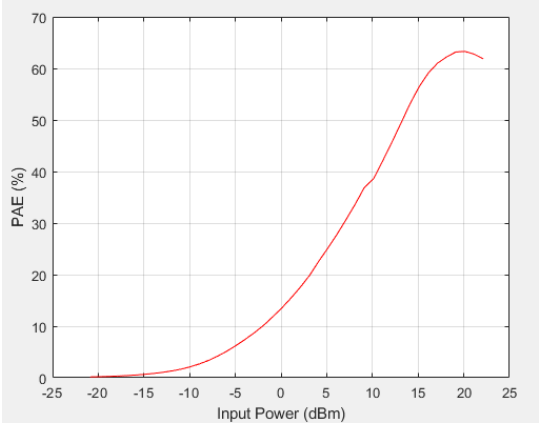
Fig.25 shows the measured large-signal parameters. These are measured with V_D being 20V and with a drain current of 70mA at the 1st stage and with V_D being 28V and with a drain current of 200mA at the 2nd stage. Fig.25a shows the output power delivered by the PA. The 1dB compression point is reached at a input power of about 0dBm and the peak output power is 43.1dBm or 20.4W. Fig.25b shows the measured transducer power gain which peaks at 31.4dB. The PAE is plotted in Fig.25c and is 63%.



(a) Measured Output Power delivered by the PA.



(b) Measured Transducer Power Gain.



(c) Measured PAE.

Figure 25: Measured output power, transducer power gain and PAE with V_D and drain current being 20V and 70mA at 1st stage and 28V and 200mA at the 2nd stage.

4.4 Discussion

The threshold voltage of both the transistors where higher than in the model. This caused the transistors to conduct the desired current at -2.37V and -2.46V in the 1st and 2nd stage respectively.

Table5 shows the simulated and the measured values compared with the specifications. The specifications of both the small-signal and the large-signal parameters are met in the simulations. All the measured values varied from the simulated ones. The measured small-signal gain is 3dB lower than what was simulated. The reflection coefficient S_{11} is 0.7dB lower in the results from the measurements at the center frequency. At 2.1GHz the simulated S_{11} is 7dB lower than the measured. This can be the explanation on why the small-signal gain drops off when the frequency is increased. The measured bandwidth does not meet the specification.

The large-signal simulation shows similar values to the simulated ones. The measured delivered power is 1.2dB lower in the measured results compared with the simulated. The transducer power gain is the same in the measured large-signal analysis and the PAE dropped with 2%. Both the simulated and the measured large-signal results are within the specifications.

Table 5: Simulated and measured Parameters

Parameter	**Simulated value**	**Measured value**	**Specification**	**Reached**
f_c	2GHz	2GHz	2GHz	Yes
BW	>100MHz	<100MHz	>100MHz	No
S_{21}	31.37dB	28.2dB	26dB	Yes
S_{11}	-14dB	-13.3dB	-10dB	Yes
P_{out}	44.3dBm	43.1 dBm	43dBm	Yes
G_T	31dB	31dB	>26dB	Yes
PAE	65.2%	63%	As high as possible	Yes

Variations between the simulated and the measured results can be caused by a number of reasons. All produced transistors will have some variations from the model used in simulation. These variations will influence the input- and output impedance of the device, the threshold voltage, efficiency and gain. Variations in other components like the capacitors and resistors will also influence the impedance in the PA. An other reason behind the variations can be an error in the simulations. The microstrip lines in the matching networks did not include the component called MSTEP. This component will take the reactive field caused by changes in the line

widths into consideration. An EM simulation on the layout could have showed this error. The circuit board did also get some small damages during the mounting of components, which could influence the impedance on the damaged lines. By designing the PA with a 1dB bandwidth with some margin above the specification, the measured bandwidth could have satisfied the specification.

5 Tracking

5.1 Power Envelope Tracking

In this section some different combinations of PET formulas will be tested. The results will be compared to a PA with fixed supply voltage. The comparison will be done in regards to gain and phase variation as a function of input power, as well as distortion of a generated 16-QAM signal. EVM, ACPR and STDR will be used to measure the distortion. The average PAE can be compared between the different modulation formulas.

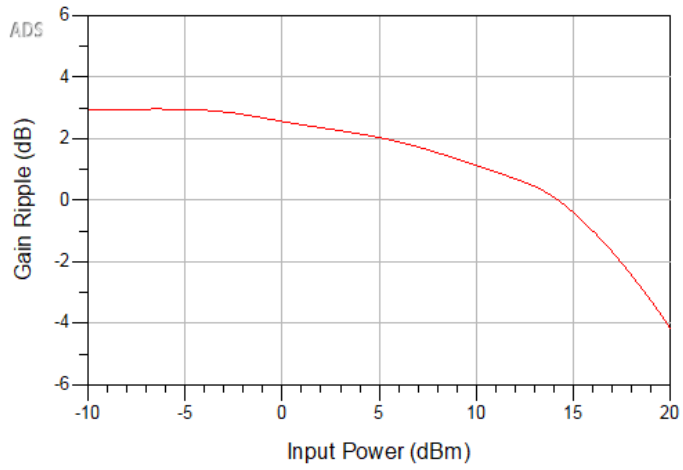
5.1.1 Modulation formulas

During the simulation three tracking formula combinations will be tested. These formulas will have different goals, but can be compared. The first combination will be will be 1st order PET on V_D at both the 1st and 2nd stage, with fixed V_G at both stages. The coefficients will be optimized to give as high PAE as possible. The second combination will be 1st order PET on V_D at 2nd stage, with fixed V_G at both stages. The coefficients will be optimized to give a flat gain and a high PAE. The third combination will be fixed V_D in the 1st stage and 1st order PET at V_D in the 2nd stage, with 4th order PET at V_G in the 1st stage and fixed V_G at the 2nd stage. The coefficients will be optimized to give flat gain, flat phase and high PAE.

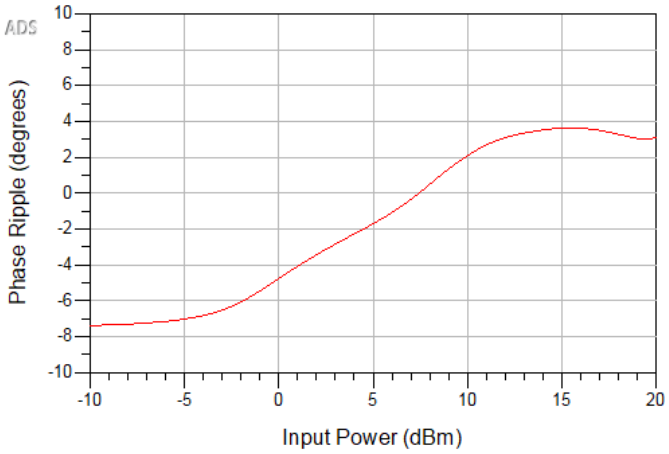
5.1.2 Gain- and Phase ripple

In the upcoming plots one can see an error in the model used in the simulations. This error causes the phase and the gain to rapidly increase or decrease at an input power of 18dBm. The real phase and gain in a physical device will most likely have a smoother graph.

Fig.26 shows the ripple in both gain and phase as a function of the input power with no modulation at either V_G or V_D. One can observe the nonlinearity in regards to both the gain and the phase. The gain drops with 7dB and the phase increases as the PA starts compressing the signal. The phase increases with about 11° over a -10dBm to 20dBm input power sweep.



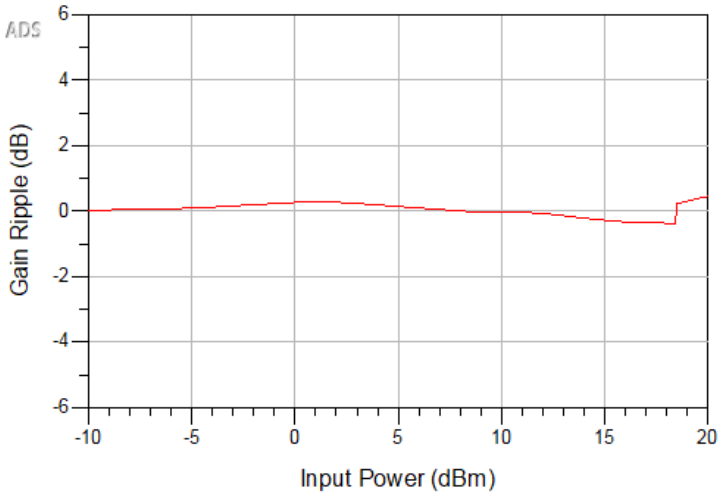
(a) The Gain ripple.



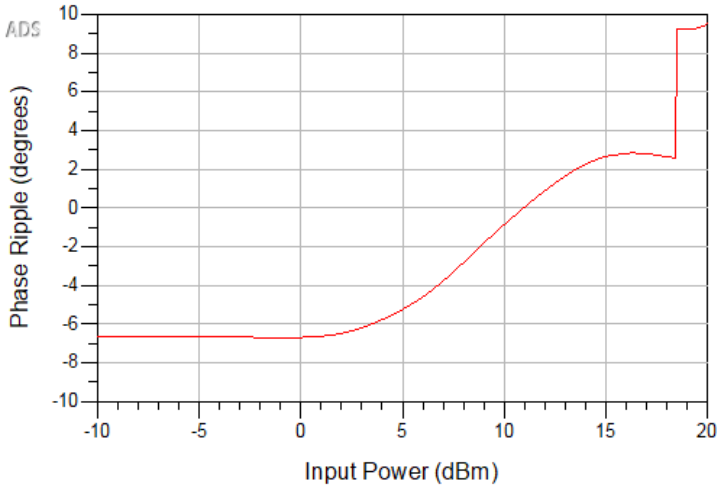
(b) The Phase ripple.

Figure 26: The Gain and Phase ripple of the PA without PET.

In Fig.27 the V_D at the 2nd stage is modulated using a 1st order PET for flat gain. This results in a gain ripple lower than 1dB over the whole input power range. As V_D is modulated the phase increases, and the phase ripple changes with 15° over the whole input power range.



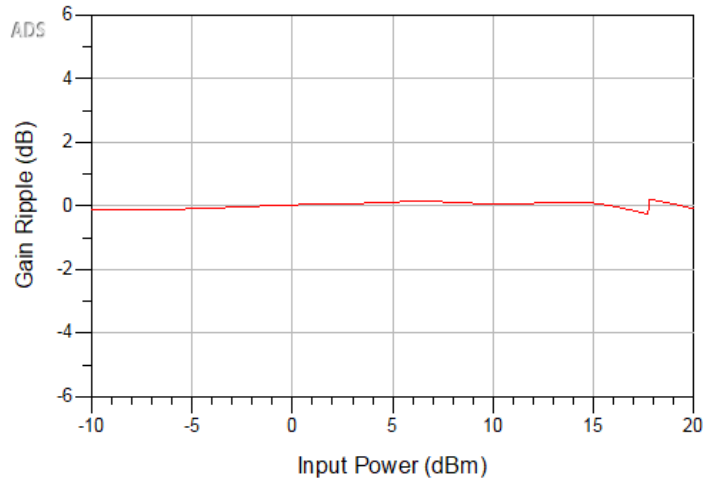
(a) The Gain ripple.



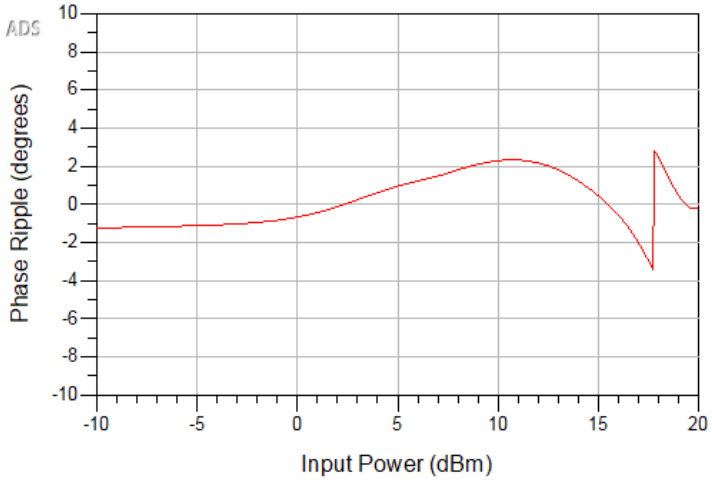
(b) The Phase ripple.

Figure 27: The Gain and Phase ripple of the PA with PET for flat gain.

Fig.28 shows the gain and phase ripple with 1st order PET at the 2nd stage drain and 4th order PET at the 1st stage gate. The 1st stage drain and 2nd stage gate is fixed. With the 1st stage gate voltage compensating the change in phase, the phase ripple is kept low. The gain ripple is still lower than 1dB and the phase ripple is 4°.



(a) The Gain ripple.



(b) The Phase ripple.

Figure 28: The Gain and Phase ripple of the PA with PET for flat gain and phase.

5.1.3 Simulated PET

By using the simulated gain and phase from ADS a Matlab script can make a model of the PA. This PA model will have the complex gain as a function of the input power from ADS, shown in Eq.[31]. By amplifying a 16QAM sequence, the distortion caused by the PA can be calculated. Average PAE, average Power delivered, EVM, ACPR and STDR will be calculated by the

Matlab script. As the gain in the different tracking formulas are different and the input signal is fixed, the average output power will be different.

$$G_{complex}(Pi) = G(Pi) * e^{-j*\phi(Pi)} \tag{31}$$

Table6 shows the results from the different PET formulas. The results from each formula combination is compared with the PA with fixed V_D and V_G with a similar output power. A graphical presentation of the simulated results are shown in Fig.29, Fig.30, Fig.31, Fig.32 and Fig.33.

Table 6: Distortion of a 16QAM signal by simulated PA

Formula	PAE_{avg}	P_{avg}	**EVM**	**ACPRl**	**ACPRr**	**STDR**
PET, max PAE	49.3%	40dBm	9.2%	-28.5dBc	-28.3dBc	19.6dB
Fixed V_D and V_G	41.6%	40dBm	6.5%	-31.1dBc	-30.9dBc	21.9dB
PET, flat gain	33.7%	36.5dBm	3.3%	-37.2dBc	-37.1dBc	29.2dB
Fixed V_D and V_G	19.1%	36.5dBm	5.3%	-33.4dBc	-33.6dBc	24.8dB
PET, flat gain and phase	33.4%	37.6dBm	3.9%	-39.7dBc	-39.6dBc	31.1dB
Fixed V_D and V_G	24.7%	37.6dBm	5.4%	-33.3dBc	-33.1dBc	24.3dB

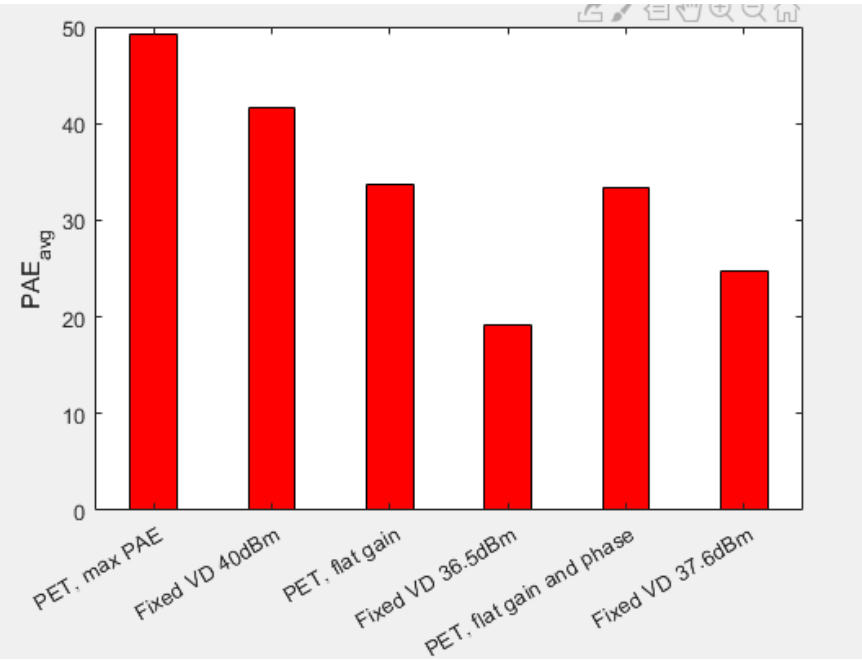


Figure 29: Average PAE of the simulated modulation formulas.

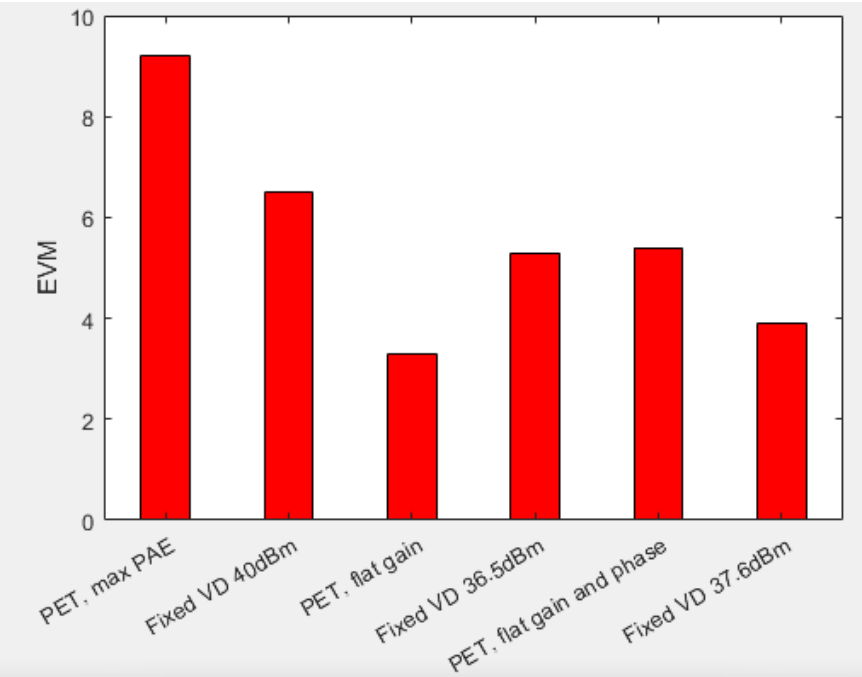


Figure 30: EVM of the simulated modulation formulas.

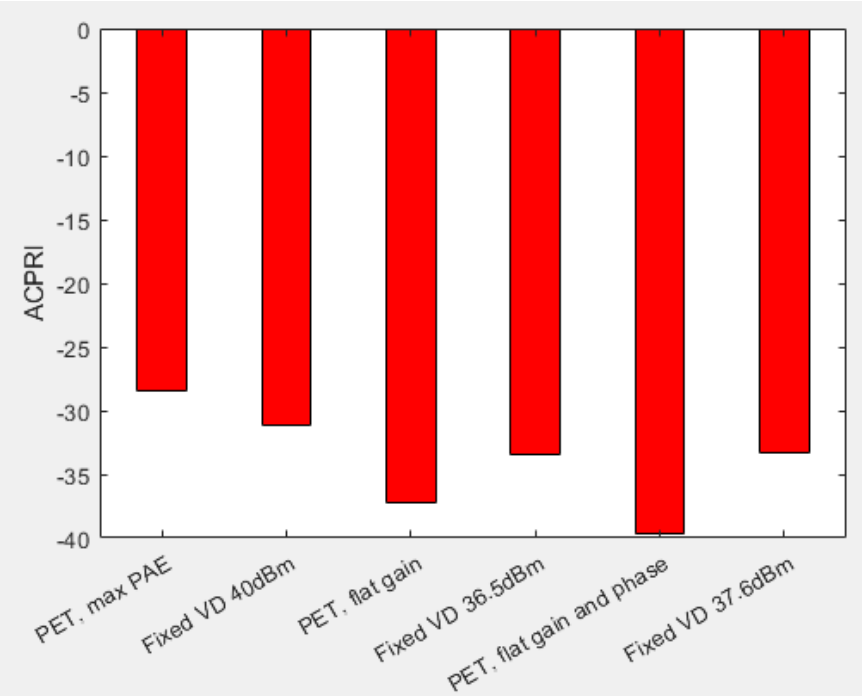


Figure 31: ACPR left of the simulated modulation formulas.

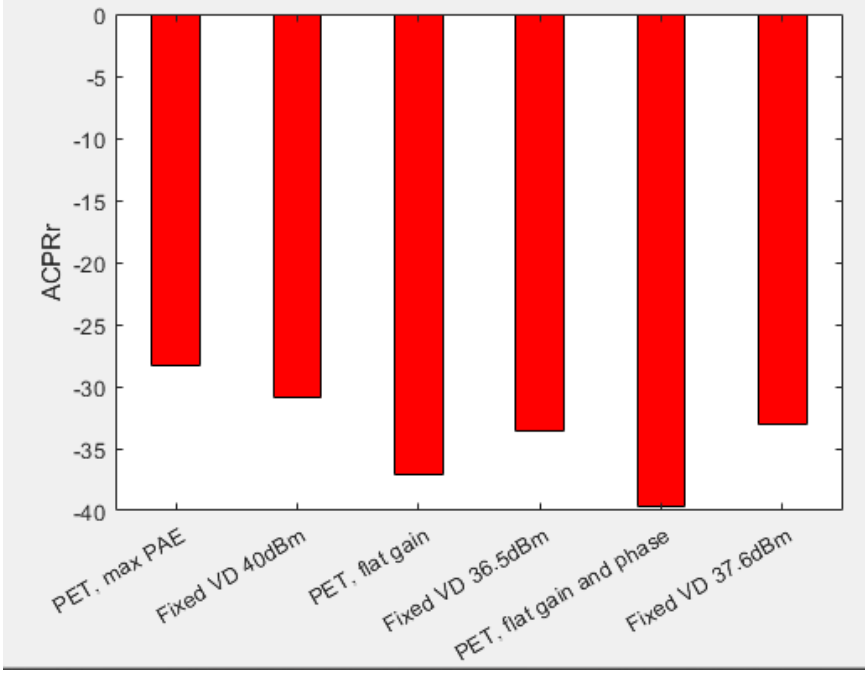


Figure 32: ACPR right of the simulated modulation formulas.

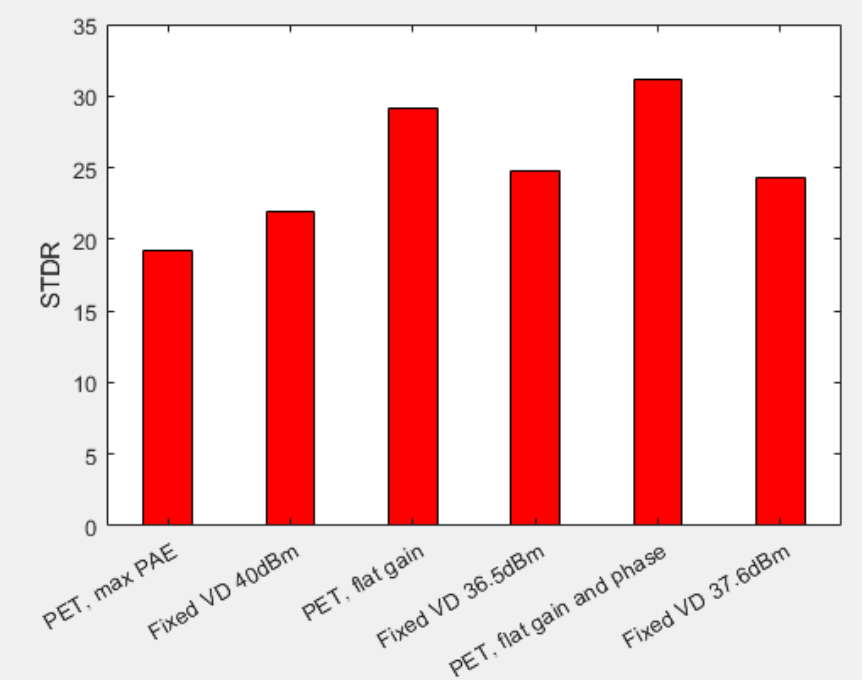


Figure 33: STDR of the simulated modulation formulas.

5.1.4 Measured PET

As V_G in the 1st stage and V_D is the 2nd stage would be modulated, the 1μF capacitors added to the DC feeding circuits where removed. A Matlab script is used to sweep the 2nd stage V_D from 6V to 30V, the 2nd stage V_D is kept at 20V. Later the script calculated coefficients used in ET and PET for flat gain 24dB and 25dB, as well a max PAE. The V_D curves of the different modulation formulas are shown in Fig.34, Fig.35 and Fig.36. The V_D is shown as a function of the normalized input voltage.

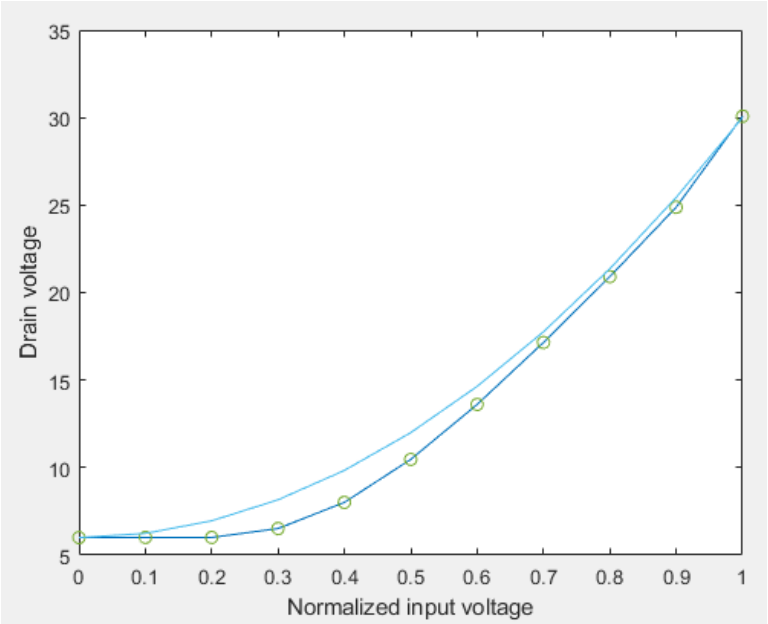


Figure 34: Drain voltage giving max PAE, dotted line is 6th order ET and solid line is 1st order PET.

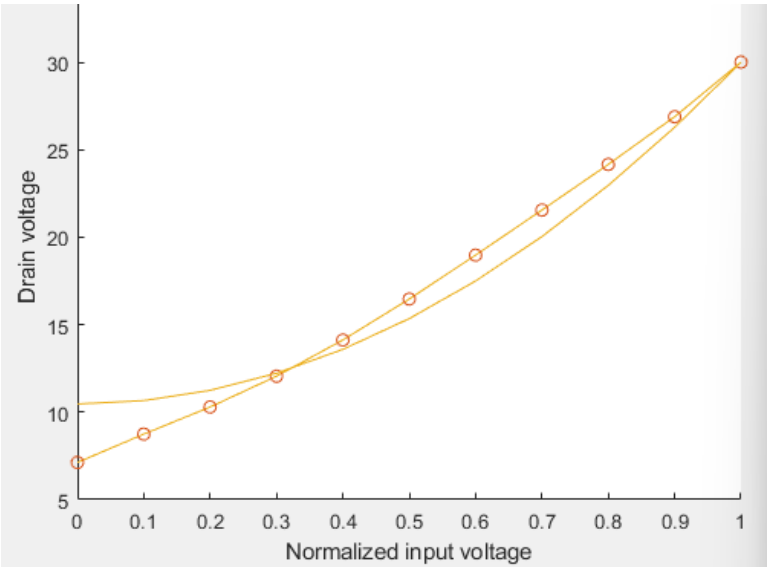


Figure 35: Drain voltage giving flat gain at 24dB, dotted line is 6th order ET and solid line is 1st order PET.

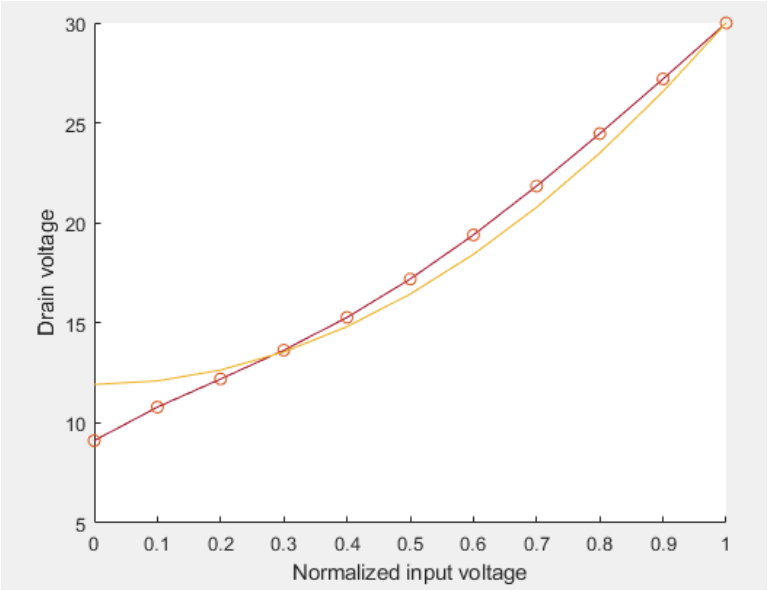


Figure 36: Drain voltage giving flat gain 25dB, dotted line is 6th order ET and solid line is 1st order PET.

Table7 shows the results from the different PET formulas. The results from each formula combination is compared with the PA with fixed V_D and V_G with a similar output power. A graphical presentation of the measured

results is shown in Fig.[37], Fig.[38], Fig.[39], Fig.[40] and Fig.[41].

Table 7: Distortion of a 16QAM signal by measured PA

Formula	PAE_{avg}	P_{avg}	**EVM**	**ACPRl**	**ACPRr**	**STDR**
Max PAE ET	54%	34dBm	7.3%	-29.6dBc	-29.8dBc	20.5dB
Max PAE PET	50.6%	34dBm	3.2%	-35.6dBc	-35.9dBc	26.5dB
Fixed VD	18.4%	34dBm	3.5%	-38.8dBc	-40.3dBc	30.2dB
Flat gain 24dB ET	60.3%	36dBm	2.3%	-39.7dBc	-39.0dBc	31.7dB
Flat gain 24dB PET	57.6%	36dBm	3.5%	-35.7dBc	-36.2dBc	27.9dB
Flat gain 25dB ET	57.6%	36dBm	2.8%	-38.6dBc	-38.1dBc	30.4dB
Flat gain 25dB PET	57.9%	36dBm	3.1%	-38.1dBc	-38.3dBc	29.6dB
Fixed VD	25.2%	36dBm	4.0%	-35.3dBc	-36.9dBc	26.8dB

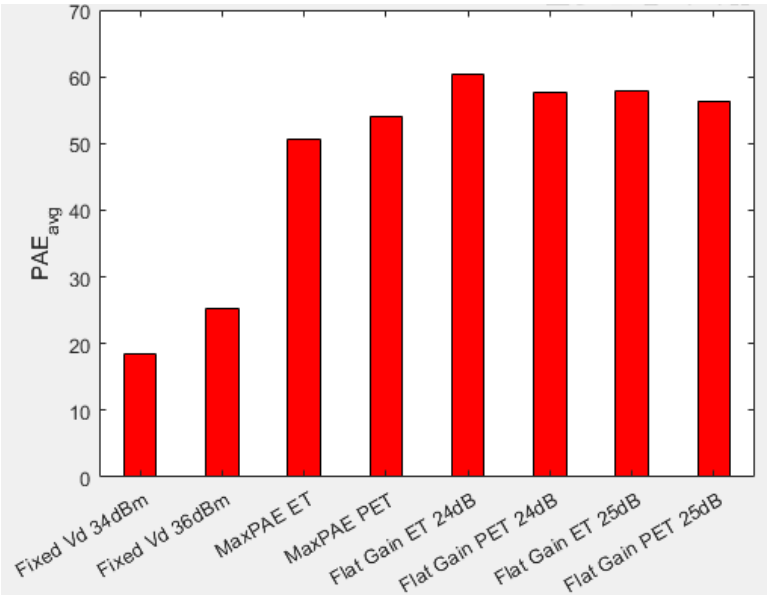


Figure 37: PAE of the measured modulation formulas.

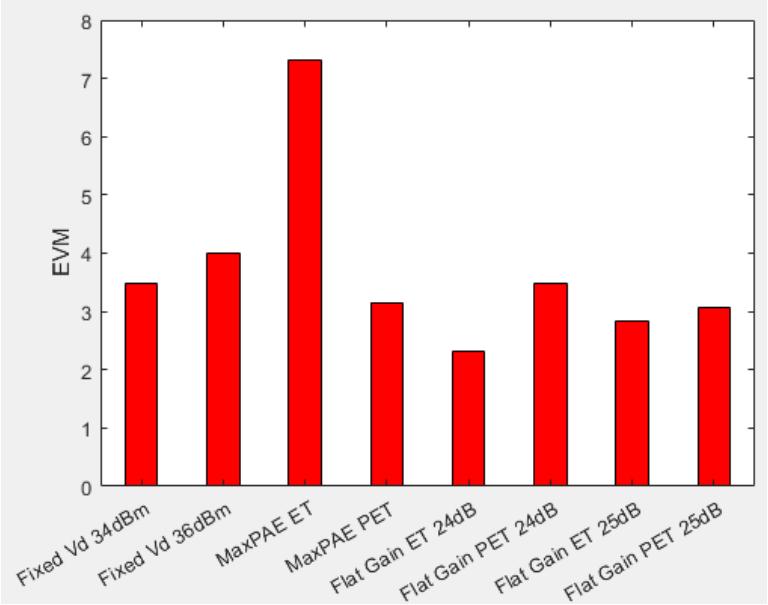


Figure 38: EVM of the measured modulation formulas.

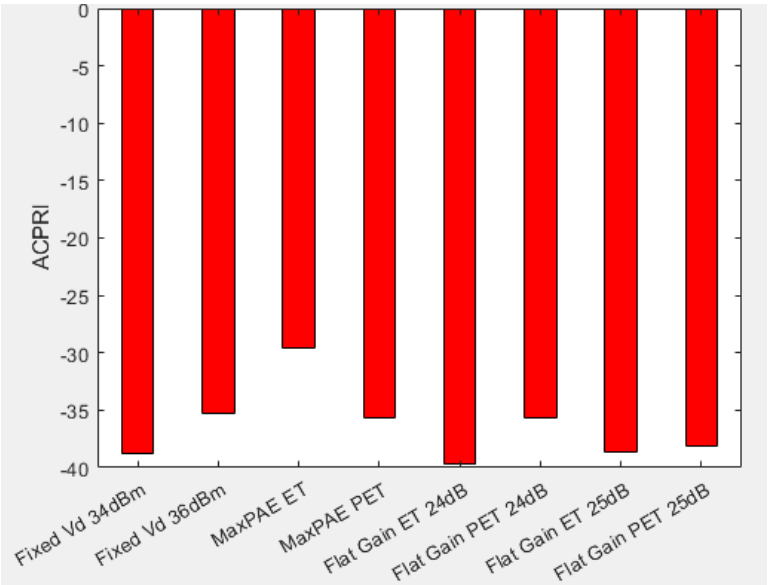


Figure 39: ACPR left of the measured modulation formulas.

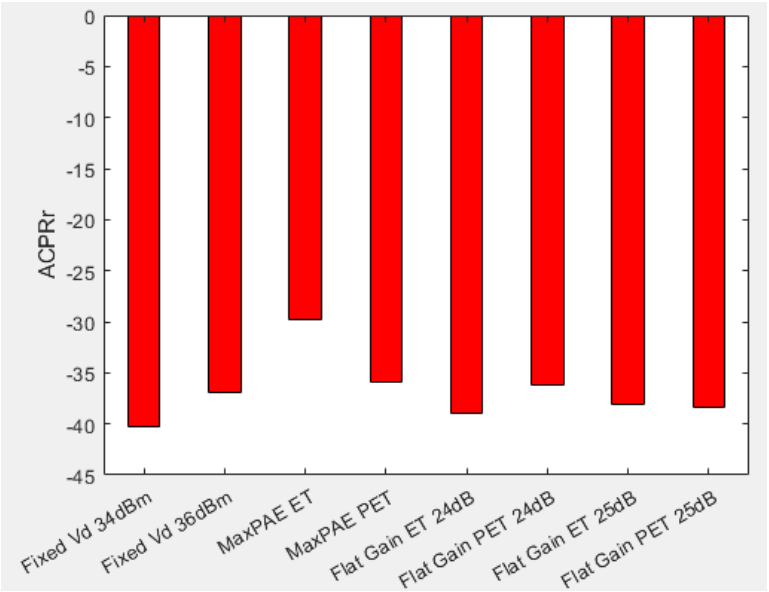


Figure 40: ACPR right of the measured modulation formulas.

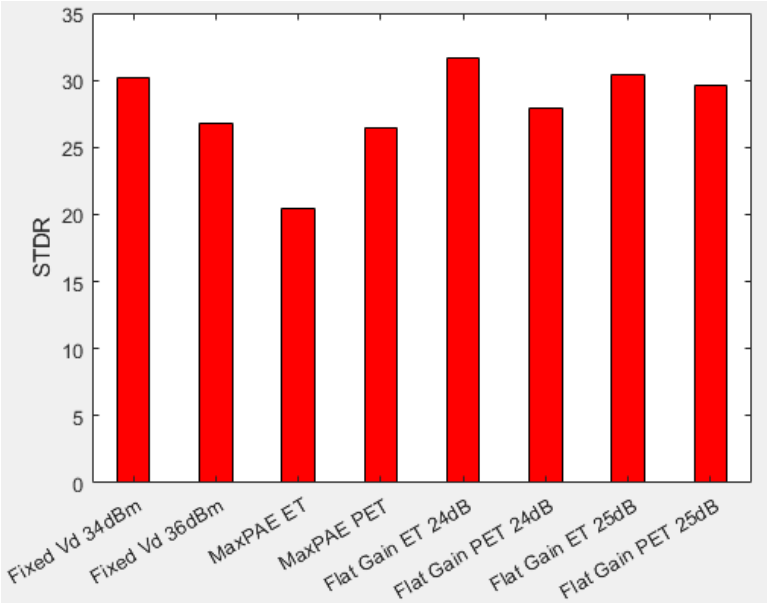


Figure 41: STDR of the measured modulation formulas.

5.2 Discussion

5.2.1 PAE_{avg}

The PAE in the simulation is highest when the modulation formulas are optimized for PAE. This is because the optimizer increased the drain voltage to get as high gain as possible and operating close to compression over the whole input power range. This can be seen when looking at EVM, ACPR and STDR. Fixed V_D and V_G with the same average output power also had high PAE due to the compression of the signal. The two flat gain formulas had the same PAE, showing that including V_G modulation does not degrade the efficiency in a PA.

The PAE from the measurements shows that the PAE is highest when the goal is flat gain. The ideal ET giving max PAE is 6% lower than the ideal ET giving flat gain of 24dB. Ideal ET giving flat gain of 25dB is also higher than the ET giving max PAE. This also hold true with PET with the highest PAE is reached by flat gain at 25dB. This is because the average gain and average output power is higher with flat gain. Fixed V_D gives the lowest PAE, with 36dBm as the average output power giving a higher PAE, at the cost of linearity.

5.2.2 Distortion

The distortion is different when compering the simulated and the measured modulation formulas. When modulating V_D to get flat gain in the simulation the EVM is 3.3% and increases to 3.9% when V_G modulation is introduced to flatten the phase. In Fig.27b and Fig.28b one can see the V_G modulation will flatten the phase, changing the phase ripple from 15° with only V_D modulation to 3° with both modulation of V_D and V_G. The gain ripple is less than 0.5dB when modulating V_D with fixed V_G and when modulating both. The EVM does not get better when modulation of V_G is included, however the left and right ACPR drops with 2dB when V_G modulation is used and STDR increases from 29.2dB to 31.1dB. This points to that modulation of the gate voltage in the 1st stage increases the linearity in a PA.

The models used in the simulation seems to have some inaccuracies when the operation point is changed outside of the default. This can be seen in the difference in the phase shift between the simulated and the measured modulation formulas giving flat gain. The phase shift through a PA biased close to class B will have a negative change in phase when the input power

is increased. As the 1st stage PA is biased in deep class AB, this can be the reason why the phase in the flat gain modulation is as flat as it is. This theory is further tested and explained by Bjørn Kristian Eid in his ongoing master thesis. The phase of the complex gain of the flat gain modulation formulas are shown in Fig.42, Fig.42, Fig.42 and Fig.42 for ET 24dB, PET 24dB, ET 25dB and PET 25dB respectively. The phase ripple for all the modulation formulas are lower than 5°, which lowers the phase distortion. One can observe the cloud of points forming the line of the phase. This is caused by noise and memory effects in the PA. The result is minimal distortion when modulating the 2nd stage V_D for flat gain. The best ideal ET modulation in regards to distortion is flat gain at 24dB and the best PET modulation is flat gain at 25dB. This points to that one does not need to modulate V_G in the 1st PA in cases where it is biased sufficiently close to class B and the design of the PA is good.

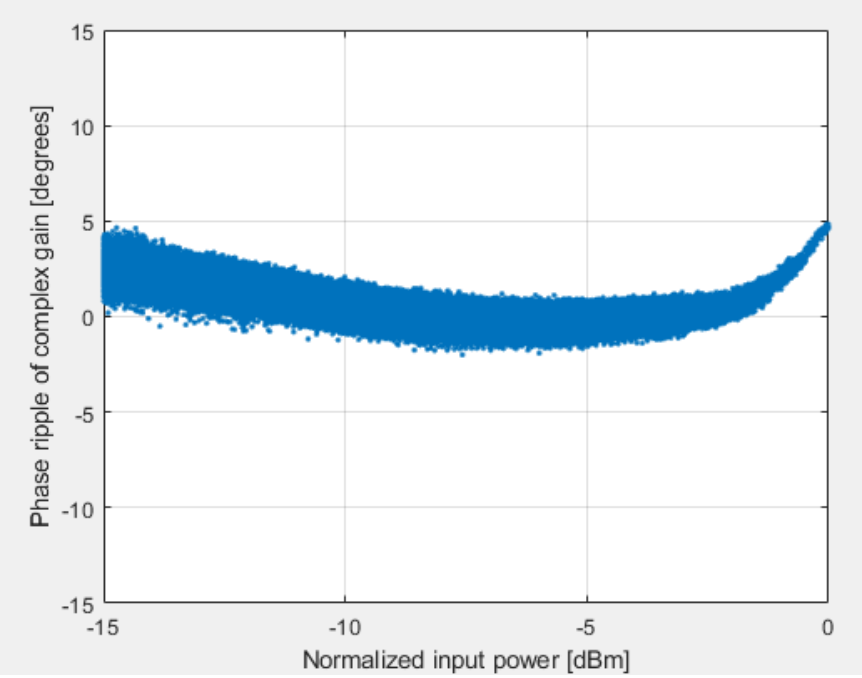


Figure 42: Phase of the complex gain of flat gain of 24dB ET.

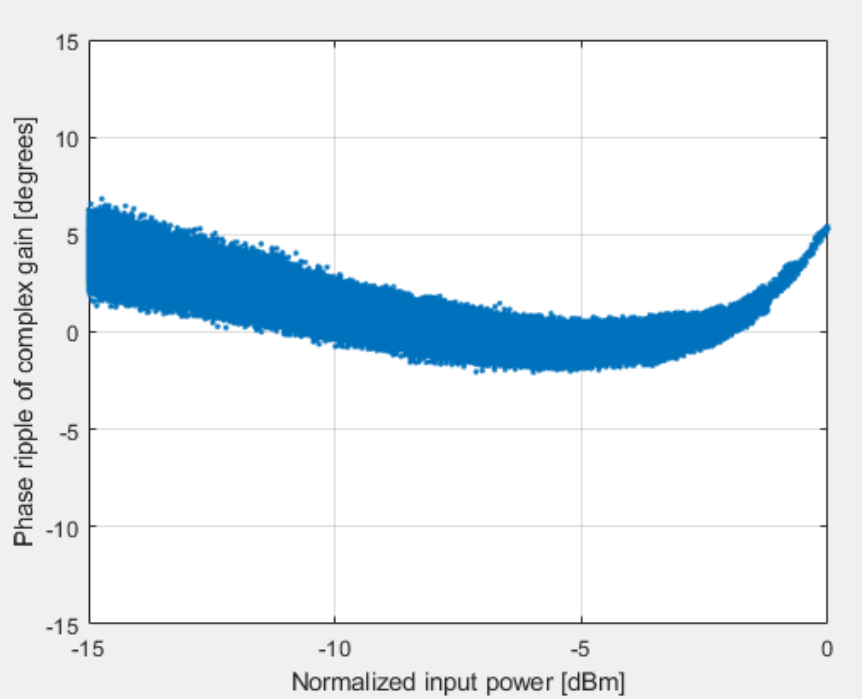


Figure 43: Phase of the complex gain of flat gain of 24dB PET.

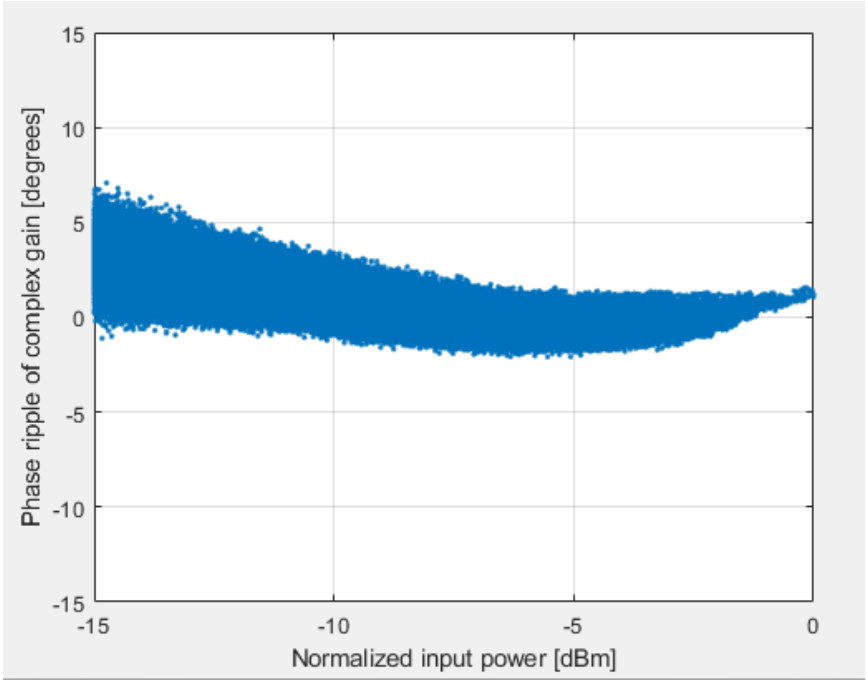


Figure 44: Phase of the complex gain of flat gain of 25dB ET.

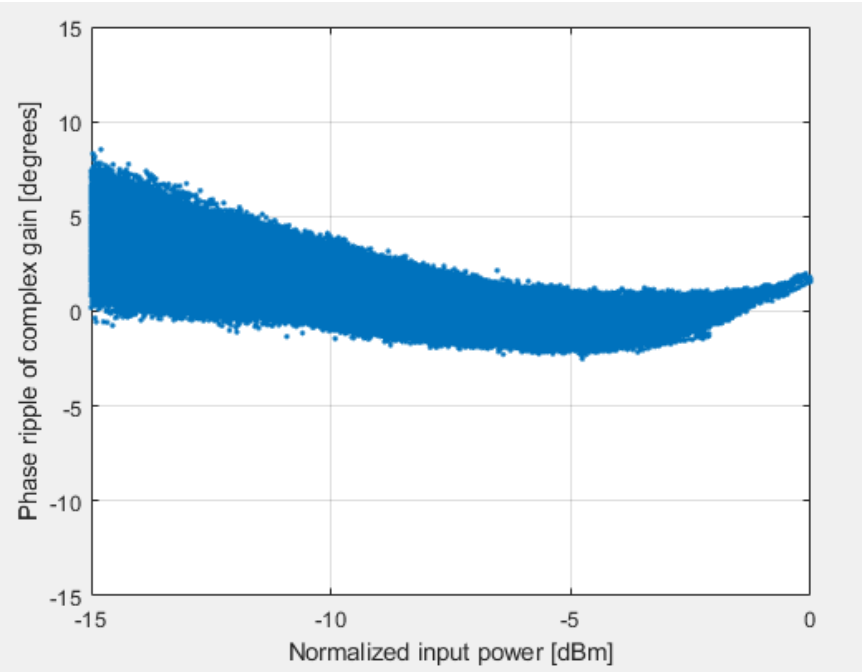


Figure 45: Phase of the complex gain of flat gain of 25dB PET.

5.3 Comparison

As previously stated in Chapter 1, this is the first time modulation of both V_G and V_D is performed on a two stage PA. Therefore the results can not be directly compered with research performed by other students and researchers. Different technology used in the PA when it comes to transistors, PCB substrate and passive components will have a substantial influence over the performance of the PA. Despite this issue a comparison can be done with this fact in mind. This is to show what other researchers have achieved with different techniques. The two techniques used in this compression will be V_G and V_D modulation and digital predistortion.

In the paper "Digital Predistortion for Envelope Tracking Power Amplifiers" [21] the researchers used ET in combination with DPD on a 5MHz at 2.14GHz signal. One of the PAs they used was based on a GaN transistor. They used both memoryless DPD and DPD with memory. They achieved an ACPRl of -53.7dBc and ACPRr of -51.6dBc without memory and an ACPRl of -57.3 dBc and ACPRr of -56.5dBc. Without DPD the PA had an ACPRl of -34.6dBc and an ACPRr of -34.1dBc.

In the paper "Linearity and Efficiency Enhancement of GaN PAs using

Bandwidth Reduced Dynamic Gate and Drain Supply Modulation (PET)" [22] the researchers used both drain and gate voltage modulation to get high efficiency as well as high linearity. The results were EVM of 1.9%, ACPRl of -40.4dBc, ACPRr of -40.1dBc and STDR of 30.5dB with a PAE of 57.4%.

6 Conclusion

6.1 Conclusion of the Power Amplifier

Both the small-signal- and the large-signal analysis was performed with V_D being 20V with drain current of 70mA in the 1st stage and with V_D being 28V with drain current of 200mA in the 2nd stage. The PA reached all the specifications in the description of the project except for the required 1dB bandwidth, which was less than 100MHz when the frequency was increased. Further the small-signal analysis showed that the center frequency was 2GHz, small-signal gain was 28.2dB and reflection was -13.3dB. The large-signal analysis showed that the peak delivered power was 43.1dBm, transducer power gain peaked at 31dB and the highest efficiency was 63%. Most of the measured values was different from the simulated ones. This could be caused by variation in the components used and in the transistors. An other reason could be because the component MSTEP was not used in the simulation.

6.2 Conclusion of tracking

Modulation of V_D for flat gain gave a higher average PAE compered with modulation of V_D for max PAE. This is because the average gain is higher giving a higher average output power. This holds true for both ideal ET and PET and both flat gain of 24dB and flat gain of 25dB. Ideal ET 24dB had the highest average PAE with 60.3%, 2.4% higher than PET for flat gain at 25dB. PET for flat gain of 24dB and ET for flat gain of 25dB gave the same average PAE of 57.6%. Fixed V_D gives an average PAE of 25.2% with the same output power as with flat gain.

Simulations gave a higher change in phase when modulating only V_D at the 2nd stage, compered with the measured results. This results in little overall distortion when V_D is modulated to flatten the gain. This is most likely due to the low biasing in the 1st stage PA which can give a negative change in phase when the input power increases, compensating for the positive change in the 2nd stage. ET for flat gain of 24dB gave the best result with EVM being 2.3%, ACPRl being -39.7dBc, ACPRr being -39.0dBc and STDR being 31.8dB. The best PET formula for drain modulation was flat gain of 25dB with EVM being 3.1%, ACPRl being -38.1dBc, ACPRr being -38.3dBc and STDR being 29.6dB. With fixed V_D one could observe the trade off between the efficiency and linearity with PAs. When the average output power was increased, the efficiency increased, but the linearity decreased.

One can conclude that using a two-stage PA with the 1st stage having a low bias can compensate for the the non-linearities introduced by modulation of V_D in the 2nd stage. This in combination with a well designed PA can get nearly flat phase and flat gain. Simulations show that modulation of V_G will give a negative change in phase. This can still be used if the bias in the 1st stage is higher which will remove the improvement caused by the low bias. A higher bias will give some benefits like a higher gain.

6.3 Further work

In the further work one should increase the bias in the 1st stage PA and observe if the phase ripple is increased when modulating V_D. Modulation of V_G is shown to increase the linearity in PAs with one stage [2] [4]. Higher order PET should also be tested and see if the linearity and PAE is increased. Different combinations of modulation of V_D and V_G should be tested on the two stages to see what gives the best results.

Bibliography

[1] T. J. Rouphael, *Wireless Receiver Architectures and Design Antennas, RF, Synthesizers, Mixed Signal, and Digital Signal Processing*. Elsevier Inc., 2015.

[2] D. Gecan, *Techniques for linearity and efficiency improvement by biasing gate and/or drain as functions of envelope power and introduction of a novel fom for linearity, applied on gan pa's*, Accessed 08. 09. 2022, 2017. [Online]. Available: https://ntnuopen.ntnu.no/ntnu-xmlui/bitstream/handle/11250/2453328/Dragan%5C%20Gecan.pdf?sequence=5.

[3] M. Olavsbråten and D. Gecan, "Bandwidth reduction for supply modulated pf pas using power envelope tracking," 2017, Accessed 08. 09. 2022. [Online]. Available: https://ieeexplore.ieee.org/document/7890479.

[4] M. Olavsbråten, D. Gecan, and K. M. Gjertsen, "Investiogation of linearity improvement with dynamic gate bias technique for flat gain or phase of an 10 w gan hemt power amplifier," 2016, Accessed 15. 06. 2023. [Online]. Available: https://ieeexplore.ieee.org/document/7465391.

[5] D. M. Pozar, *Microwave engineering, 4th edition*. 111 River Street, Hoboken, New Jersey: John Wiley & Sons, Inc, 2012.

[6] microwaves101, *S-parameters*, [Accessed 15.03.2023], 2012. [Online]. Available: https://www.microwaves101.com/encyclopedias/s-parameters.

[7] M. K. Kazimierczuk, *RF Power Amplifiers, 2nd edition*. John Wiley & Sons, Ltd, 2015.

[8] Electronics tutorials, *Amplifier classes*, [Accessed 19-November-2022], 2022. [Online]. Available: https://www.electronics-tutorials.ws/amplifier/amplifier-classes.html.

[9] M. Olavsbråten, *Gain, stability and cad simulations*, Radio System Design and RF/Microwave Techniques TTT4201 [Lecture slides], Norwegian University of Science and Technology, delivered 2021-09-16, Sep. 2021.

[10] EverythingRF, *What is p1db?* [Accessed 20-May-2023], 2018. [Online]. Available: https://www.everythingrf.com/community/what-is-p1db.

[11] Cadence, *Drain efficiency vs. power-added efficiency pae and the efficiency assessment of rf devices*, [Accessed 15-November-2022], 2022. [Online]. Available: https://resources.pcb.cadence.com/blog/2019-drain-efficiency-vs-power-added-efficiency-pae-and-the-efficiency-assessment-of-rf-devices.

[12] Kouassi, Kouakou and Andrieux, Guillaume and Diouris, Jean-François, *Papr distribution for single carrier m-qam modulations*, [Accessed 20.03.2023], 2018. [Online]. Available: https://hal.science/hal-01904878.

[13] EverythingRF, *What is papr (peak to average power ratio), why it matters to power amplifier ?* [Accessed 20.03.2023], 2017. [Online]. Available: https://www.everythingrf.com/community/what-is-peak-to-average-power-ratio.

[14] Wikipedia contributors, *Envelope tracking — Wikipedia, the free encyclopedia*, [Accessed 14-November-2022], 2022. [Online]. Available: https://en.wikipedia.org/wiki/Envelope_tracking.

[15] M. Olavsbråten, *Bandwidth reduction techniques for the supply modulated rfpas (et) usable for wideband- and multicarrier signals.* Radio System Design and RF/Microwave Techniques TTT4201 [Lecture slides], Norwegian University of Science and Technology.

[16] S. C. Cripps, *RF Power Amplifiers for Wireless Communications, Second Edition*. Artech House, 2006.

[17] M. Isaksson, D. Wisell, and D. Rönnow, *A Comparative Analysis of Behavioral Models for RF Power Amplifiers*. IEEE TRANSACTIONS ON MICROWAVE THEORY and TECHNIQUES, 2006.

[18] EverythingRF, *What is evm*, [Accessed 17.04.2023], 2020. [Online]. Available: https://www.everythingrf.com/community/what-is-evm.

[19] M. Olavsbråten, *Real lumped components, transistors, dc-bias, design procedure, stabilisation*, Radio System Design and RF/Microwave Techniques TTT4201 [Lecture slides], Norwegian University of Science and Technology, delivered 2021-09-16, 2021.

[20] Miller, Greg, *Mtee (microstrip t-junction*, [Online; accessed 20-April-2023], 2008. [Online]. Available: https://edadocs.software.keysight.com/pages/viewpage.action?pageId=5912155.

[21] P. J. Draxler, J. J. Yan, D. F. Kimball, and P. Asbeck, *Digital Predistortion for Envelope Tracking Power Amplifiers*. IEEE TRANSACTIONS ON MICROWAVE THEORY and TECHNIQUES, 2012.

[22] M. Olavsbråten and D. Gecan, "Linearity and efficiency enhancement of gan pas using bandwidth reduced dynamic gate and drain supply modulation (pet)," 2018, Accessed 15. 06. 2023. [Online]. Available: https://ieeexplore.ieee.org/document/8363912.

A Appendix

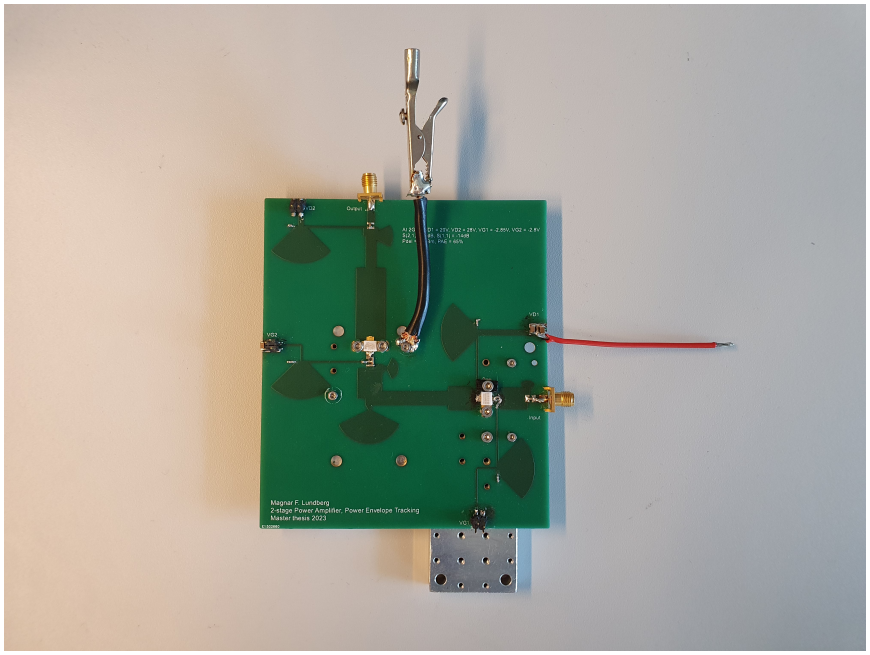


Figure 46: PCB of the two-stage PA.

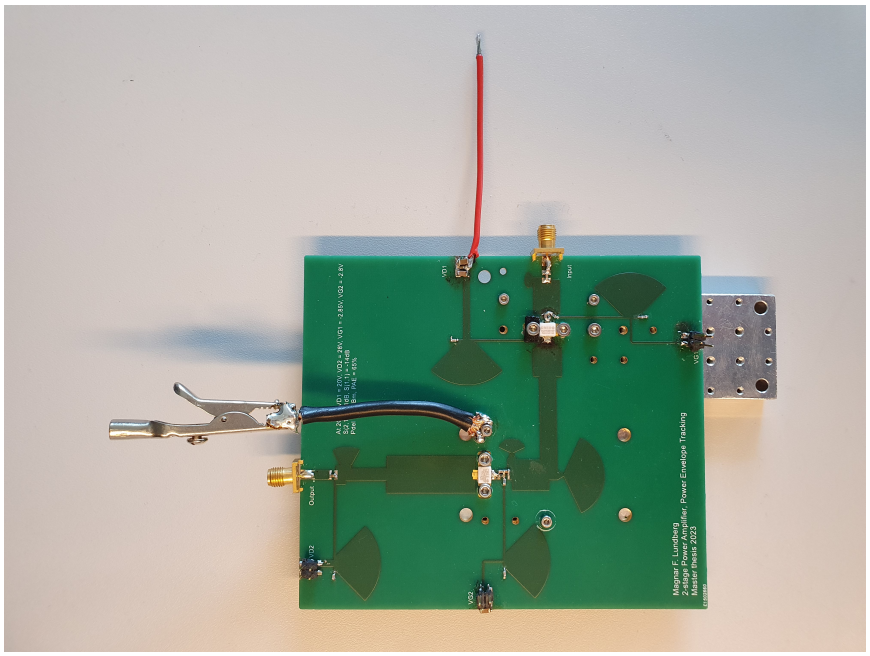


Figure 47: PCB of the two-stage PA.

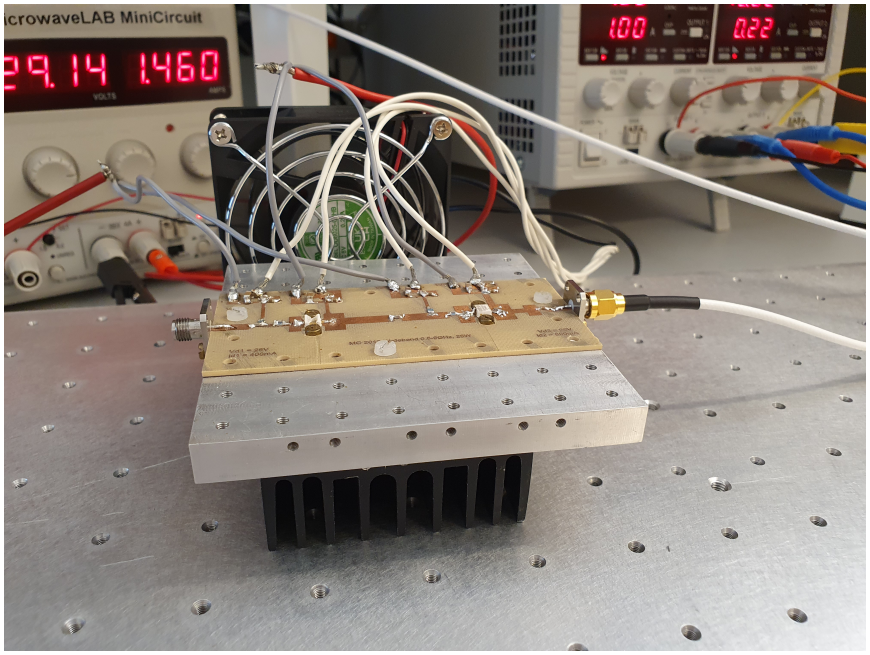


Figure 48: Driver, designed and produced by Morten Olavsbråten.

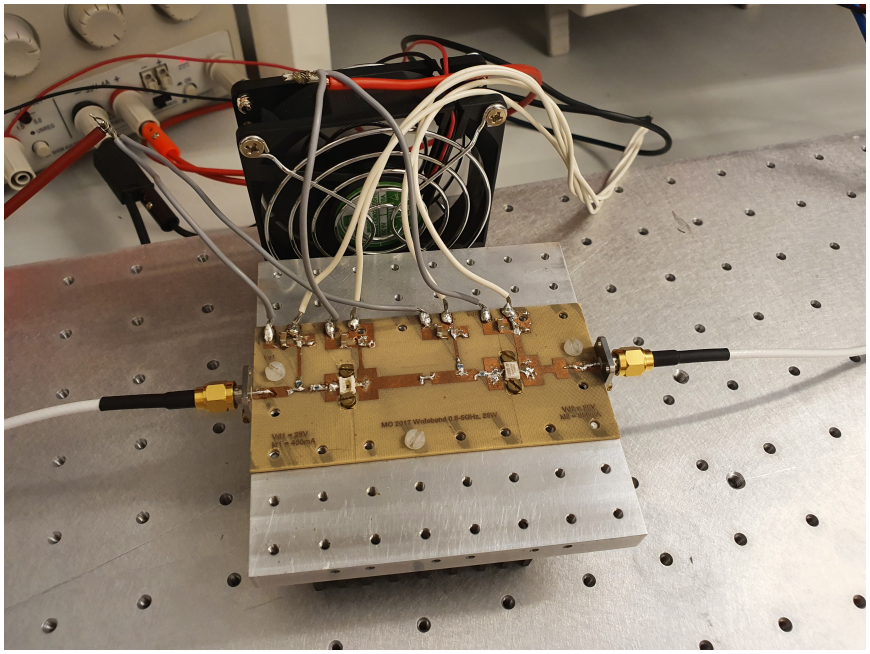


Figure 49: Driver, designed and produced by Morten Olavsbråten.

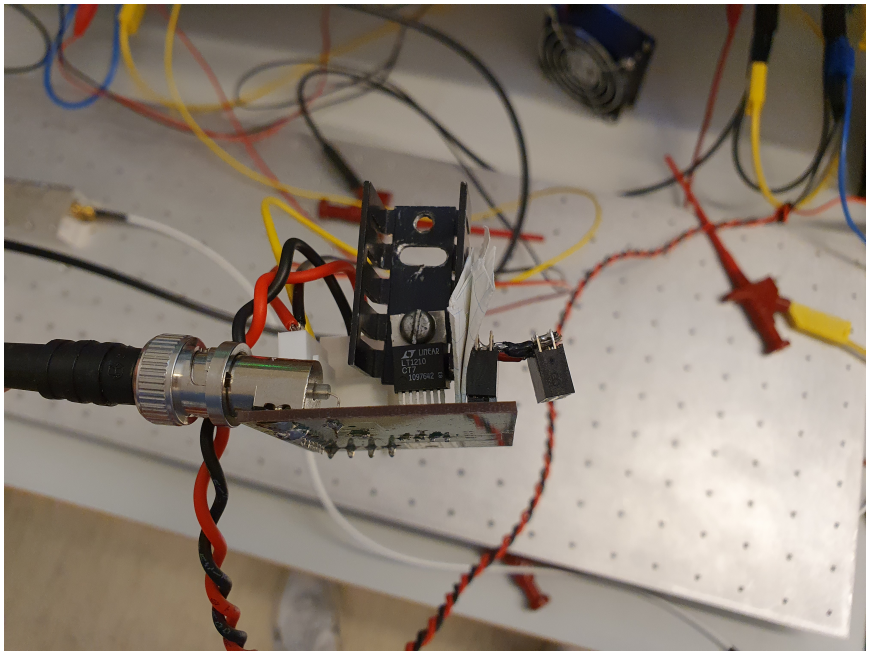


Figure 50: Tracker, designed and produced by Morten Olavsbråten.

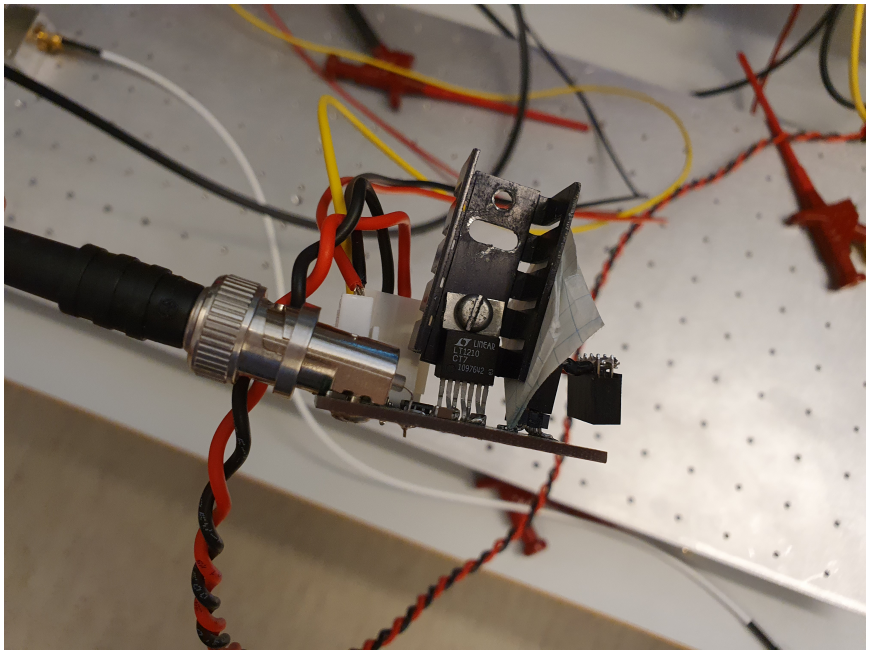


Figure 51: Tracker, designed and produced by Morten Olavsbråten.

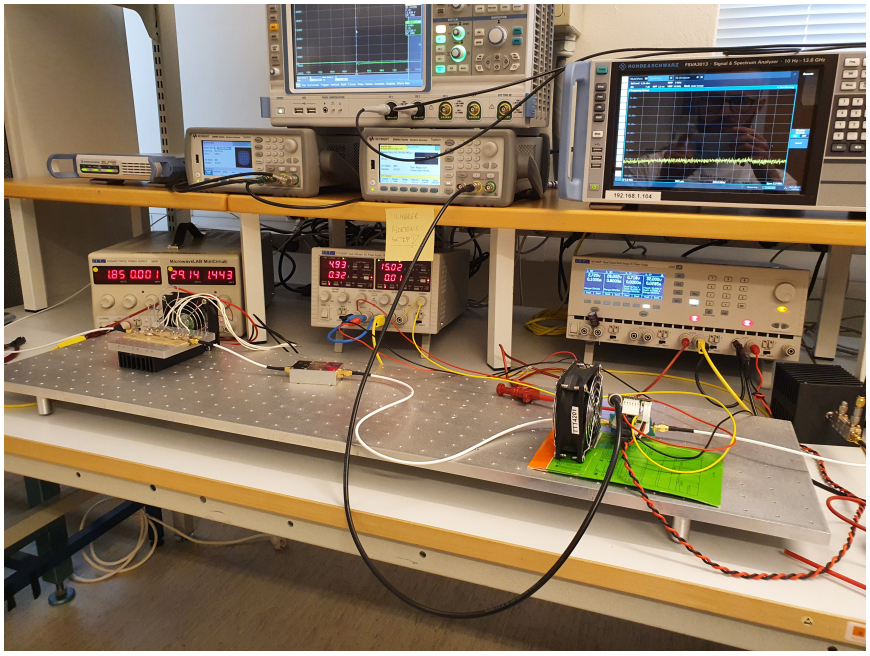
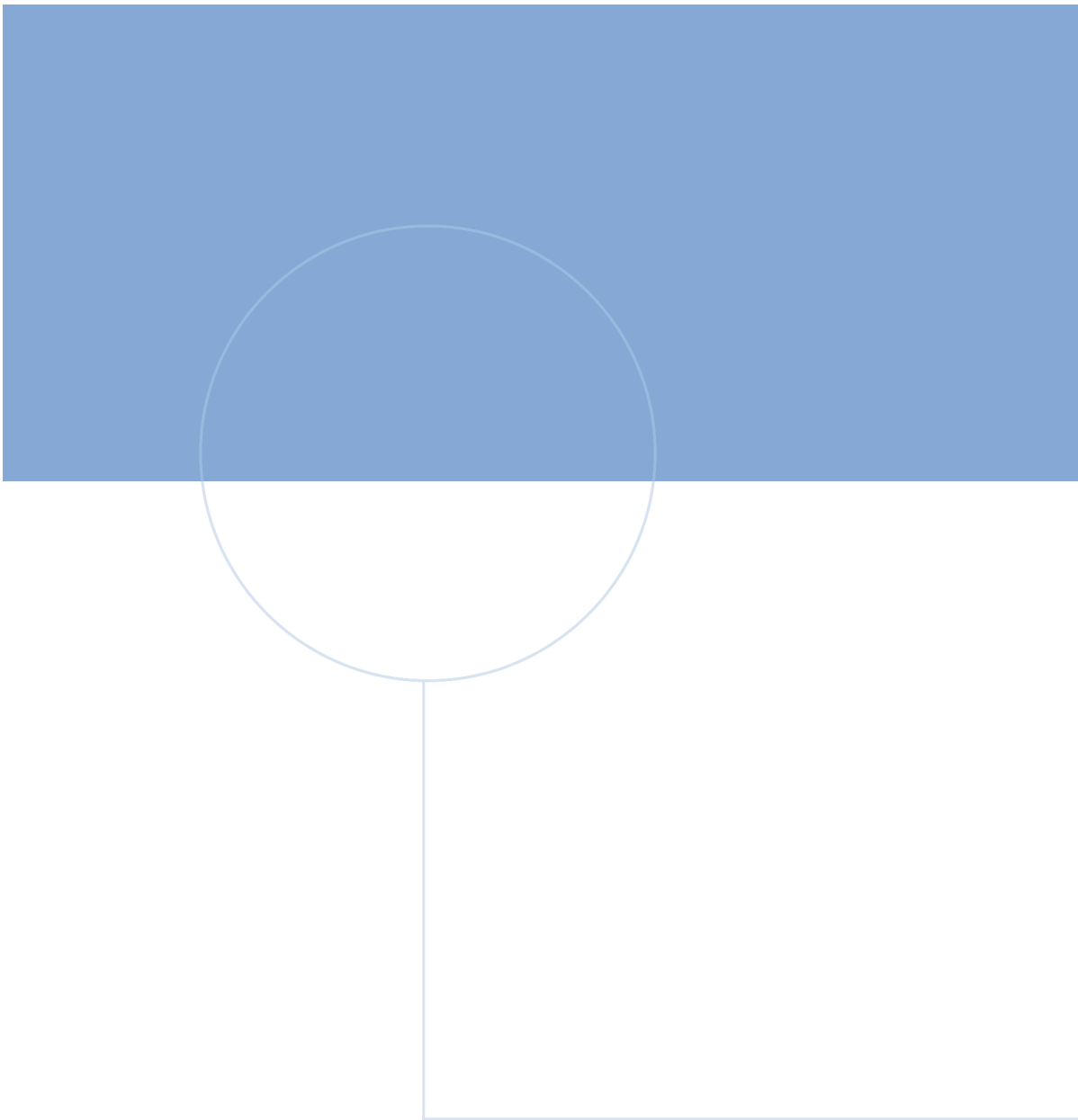


Figure 52: Setup used during the tracking.



NTNU

Norwegian University of
Science and Technology