Master's thesis

NTNU
Norwegian University of Science and Technology
Faculty of Information Technology and Electrical Engineering
Department of Electric Power Engineering

Vegard Yssen Rørstad

Experimental verification of control methods for series connected VSCs applied to a modular HVDC power train for offshore wind

Master's thesis in Energy and environment
Supervisor: Pål Keim Olsen
Co-supervisor: Lorrana Faria da Rocha
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Summary

In this thesis, current control and voltage balancing control of series-connected modular voltage source converters applied to a generator with isolated three-phase segments have been verified experimentally and through simulations. The research done in this thesis is a continuation of previous research done on an HVDC power train concept for offshore wind turbines called ModHVDC. The proposed control method is based on vector field-oriented control in the dq0 plane. The control system has a cascade structure with inner loop current control and outer loop voltage control. Each module has its own module-level controller, which is identical in all modules to uphold the modularity principle.

The objective of this thesis is to verify the feasibility of the proposed DC voltage balancing control algorithm while employing different strategies for saturating the voltage controller output in relation to the system ratings. Simulations on a two-module system have been performed in Simulink. Firstly on a simulation model containing both module(slave)-level control and turbine(master)-level control, in order to verify appropriate interaction between the two control levels. For the experimental verification, a small-scale two-module lab setup was developed. The lab setup emulates the segmented stator windings of the generator through two three-phase transformers, each connected in series with its own grid-connected variable transformer. The VSCs are controlled by a microcontroller-based embedded system. Additionally, simulations of the physical lab setup were conducted in parallel with the development of the lab in order to verify the obtained experimental results.

The results from both simulation and experimental verification showed accurate reference tracking by the inner loop current controller and the outer loop voltage balancing. However, in the lab having a master-level set point voltage reference controller was impossible, therefore, a fixed reference was used instead. This resulted in a small steady-state error which is detrimental over time due to integral windup. The voltage balancing strategies explored were all shown to be feasible in terms of stability and accurate reference tracking, however, more research has to be done in order to ascertain whether the strategies are economically and practically viable in a full-scale system.

Oppsummering

I denne avhandlingen har strømkontroll og spenningsbalanseringskontroll av serie koblede modulære spenningskildeomformere (VSC) blitt testet eksperimentelt og gjennom simuleringer. Forskingen gjort i sammenheng med denne avhandlingen er en fortsettelse av tidligere forskning utført på et HVDC-krafttogs konsept for offshore vindturbiner. Dette konseptet har fått kallenavnet ModHVDC og er basert på en høyspennings generator med isolerte stator segmenter som hver er koblet til en individuell spenningsomformer. Spenningsomformerne er så koblet i serie på DC siden for å skape høy spenning for HVDC transmisjon. Det foreslåtte kontrollsystemet er basert på feltorientert vektorkontroll i dq0 planet, med en kaskade struktur som inneholder en indreløkke med strømkontroll og ytre løkke spennings balanserings kontroll. Hver modul har en modulnivåkontroller, som er identisk i alle moduler for å opprettholde modularitetsprinsippet.

Målet med denne avhandlingen er å verifisere gjennomførbarheten av den foreslåtte DC spenningsbalanseringskontrollalgoritmen, mens man benytter forskjellige strategier for å begrense spenningskontrollerens handlingsrom i forhold til systemets maksimale strømtoleranse. Simuleringer av et to-modul-system er utført i Simulink med en modell som inneholder både modul(slave)-nivå kontroll og turbin(master)-nivå kontroll. For den eksperimentelle verifiseringen av modulnivå kontrollsystemet, ble et småskala to-modul laboratorieoppsett utviklet som en del av arbeidet gjort i denne avhandlingen. Laboratorieoppsettet etterligner de segmenterte statorviklingene til generatoren ved bruk av to trefasetransformatorer. Transformatorene er matet av hver sin nett-tilkoblede variable transformator. De to spenningsomformerne er styrt av et embedded-system som er basert på mikrokontrollere fra Texas Instruments. Simuleringer av laboratorieoppsettet ble utført parallelt med utviklingen av lab oppsettet.

Resultatene fra både simulering og den eksperimentelle verifiseringen demonstrerte nøyaktig referansesporing fra både den indreløkke strømkontrolleren og den ytreløkke spenningsbalanserings kontrolleren. Det var imidlertid umulig å implementere master-nivå-settpunkt spenningsreferansekontroll i laboratoriet. Derfor ble det observert en liten stasjonær feil i DC spenningen relativt til referansen. Dette er kritisk på grunn av integraloppbygging over tid. Alle spenningsbalanseringsstrategiene som ble utforsket viste seg å være gjennomførbare når det gjelder stabilitet og nøyaktig referansesporing. Men det må utføres mer forskning for å fastslå om strategiene er økonomisk og praktisk gjennomførbare i et fullskala system.

Acknowledgements

Finishing this thesis marks the end of five years at NTNU Gløshaugen. It has been some of the most memorable years of my life. I am proud to have completed this degree and am ready for the next chapter.

The last year has been the perfect culmination of what I have learned as a student. Since their introductory courses, control theory, and power electronics have been the topics I find most fascinating. Now, I have been fortunate enough to try my hand at developing a laboratory setup that requires an understanding of both. Implementing what I had previously simulated in a real-life application was a rollercoaster ride, but the highs were higher than the lows. The feeling of having a breakthrough moment after struggling with a problem for a long time is one of the most rewarding experiences, and for me, its a big part of what it means to be an engineer.

Firstly I want to thank my supervisors, Pål Keim Olsen and Lorrana Faria da Rocha. Thank you, Pål, for introducing me to this project and pushing for us to make this lab setup. Thank you also for allowing me to work so freely in the lab and for your counsel along the way. Thank you to Lorrana for all your help in developing the lab and feedback on the thesis. I would also like to thank all the guys in the power electronics lab for their willingness to advise me when I hit a wall with my setup. So thank you to Daniel, Yoga, and Dimos! Also, thank you to Thomas for your advice on the lab configuration. Lastly, a big thanks to Svein Erling and the guys at the service lab for their endless help with setting up the lab, finding equipment, and debugging problems.

Preface and acknowledgements of previous work

Certain sections of this thesis report are restatements of text from the author's specialization project. These sections are marked with an "*", and it is specified in the text which subsections are taken from the specialization project.

The Simulink models and corresponding Matlab scripts developed for this thesis work are included as attachments, and might be made publicly available in a github repository a later time.

Note that although the Simulink models used for lab simulations and for the embedded system were made by the author for this thesis project[1], some methods and variables are inspired by or directly taken from examples provided by Mathworks. The author does not claim to have developed these methods/subsystems or any rights to their design. Most notable are the methods for setting and removing a trip zone bit, and the configuration of the ePWM blocks are largely copied from the following Mathworks examples[2][3].

Also, the model used to simulate the turbine level and module level control system together, called "Complete control system model" is heavily inspired by the model developed by Faraasen in his thesis work [4], as is also stated in the main text. Therefore, the simulation model named "Complete control system model" is largely credited to Faarasen[2]

The overall control system discussed in this thesis is credited to [5], as is stated in the main text.

[1]The model simulation model used for simulating the turbine -and module-level control system ("Complete control system model") was created as a part of the pre-project to the masters [1] and is not considered a part of this thesis work, as is stated in the main text.

[2]The differences between the model developed for the pre-project and Faarasens model lies in the implementation of the mechanical subsystem, tweaks in controller tuning, DC-link impedance, and introduction of the pitch controlled. The core control system is the same and is credited to [5].

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1 Introduction

1.1 Motivation

Offshore wind is predicted to be a key energy source in the shift toward net zero emissions. The International Energy Agency (IEA) reports an increase in installed wind capacity of 113 GW in 2020 worldwide, and in order to reach the net zero scenarios, installed wind capacity must increase by an estimated 18% per year until 2030[6]. "WindEurope" has released a report claiming it is feasible to deploy 450GW of offshore wind power in Europe by 2050. Most of which will be installed in the North Sea[7]. Despite these optimistic predictions for future wind power development, the cost of installing and operating offshore wind parks, in particular, remains high. Recently Equinor postponed the building of their offshore wind park project in the North-sea "Trollvind," claiming that the project was no longer economically feasible.

Reducing installation, operation, and maintenance costs is crucial for the future expansion of offshore wind power. Although costs are expected to reduce due to economies of scale, significant technological developments must take place to make offshore wind profitable enough for the expected increase in commissioned large-scale wind parks [8]. As more offshore wind is being commissioned, the wind parks are moving further away from shore. This makes transmission costs an important factor for the economic feasibility of new offshore projects. Because HVDC is the most cost-effective method of transmission for distances over 150-200km [9], HVDC transmission is expected to become more prominent going forward. Additionally, offshore wind parks sets particular demands for low weight and volume of the offshore side converters and the conversion platform [9]. In short, there is a great demand for AC-to-HVDC conversion technology that reduces installation costs, improves reliability, and is compatible with offshore applications.

1.2 Modular HVDC-generator concept

The research done in this thesis is a continuation of previous research on a power train concept for offshore wind turbines nicknamed ModHVDC. The ModHVDC concept proposes modular AC to HVDC conversion with transmission level voltage after just one conversion stage. The single conversion stage is achieved by series connecting the DC side of N VSCs[4], where the AC side of each converter is connected to an isolated stator segment of the HV generator in the turbine. The sum of the DC potentials of the VSCs creates the DC voltage required for HVDC transmission. The concept is based on modularity and proposes that all modules consist of identical three-phase stator segments and VSCs, with corresponding modularity-based control. This modular power train concept is currently in review at "EU Horizon" for further research funding.

The control synthesis of the turbine level and module level control system for the ModHVDC concept is presented by S.Gjerde in [5]. The control system discussed in this thesis is based on the control system presented by Gjerde, and a continuation by Faraasen in [4].

A concept drawing of the ModHVDC system is presented in Figure 1. This thesis only considers the wind turbine power train denoted as "ModHVDC power train" in the illustration. Therefore, the grid-side converter and DC-link voltage control is not discussed.

1.2.1 Advantages of the ModHVDC system concept

The ModHVDC improves upon the existing state-of-the-art power train in several ways.

1. Removing the need for a step-up transformer in the nacelle. The turbine-level step-up transformer particularly is a driver of increased installation cost due to its weight and subsequent demands it set for the tower construction. [10].

[4]The number of modules is not set. For now, up to 32 modules have been considered for a 20MW generator.

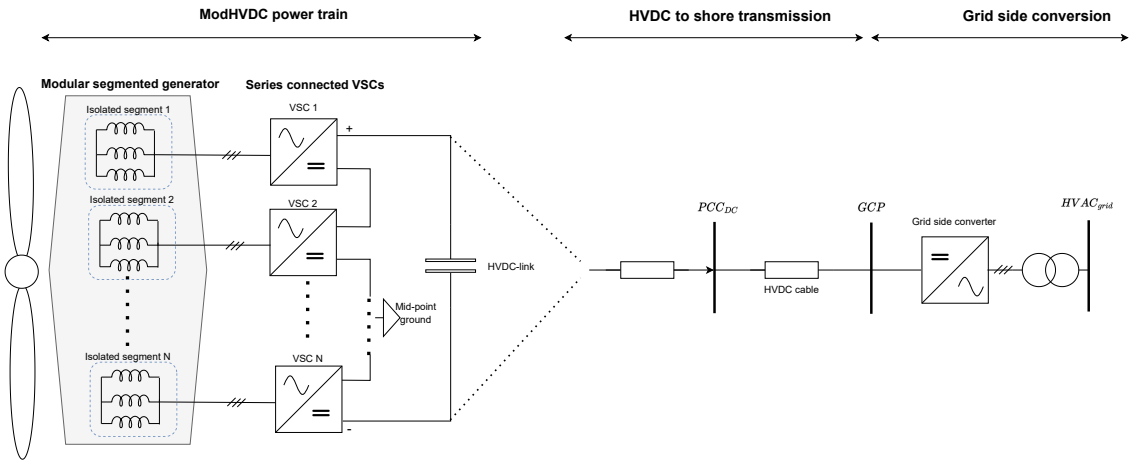


Figure 1: Concept drawing of the ModHVDC system.

2. Reduced isolation thickness on the slots in the generator, which will allow for a high power-to-weight ratio.

3. Improved reliability due to modularity and the resulting possibility of module fault bypass.

1.3 Problem description

One of the main challenges of the ModHVDC concept is handling potential differences in power production between the modules due to imbalances between the stator segments in terms of flux linkage, stator coil resistance, etc. Any difference between the stator segments in terms of power produced will cause unequal voltage levels on the DC bus. Because the DC-link voltage is fixed, a lower DC voltage on one module results in increased DC voltage on the other modules. Above-rated voltage levels can be critical for the system's reliability over time. Therefore, the DC bus voltages have to be effectively balanced. Balancing is achieved by controlling the active power component of the AC current in each module individually to compensate for the initial difference in AC side power between the modules. Because this control method causes the magnitude of the AC current to be unequal from module to module, another issue arises: How can effectively balance the DC bus voltage at nominal power while still respecting the rated limit on the AC -current imposed by the system ratings? An illustration outlining the problem in basic terms is presented in Figure 2.

This thesis investigates through simulations and experimental testing the effectiveness of the DC voltage balancing algorithm in terms of stability and achieving equal DC bus voltages. Additionally, the feasibility, from a control perspective, of three different voltage balancing strategies is investigated. The voltage balancing strategies are simply three different methods for limiting the voltage balancing controllers' output in relation to the AC current rating and the power produced by the system.

1.4 Research objectives

The main research objective of this thesis project is to develop a small-scale laboratory implementation of the ModHVDC power train and test the module-level control system proposed by [5] on the lab system. Then using the lab setup investigate different strategies for balancing the DC-bus voltages of the modules while maintaining nominal power production and maximum possible utilization of the system rating. The underlying research objectives are as follows:

1. Simulate the turbine -and module-level control system for a two-module implementation in Simulink. Two modules are the minimal realization of the modular system.

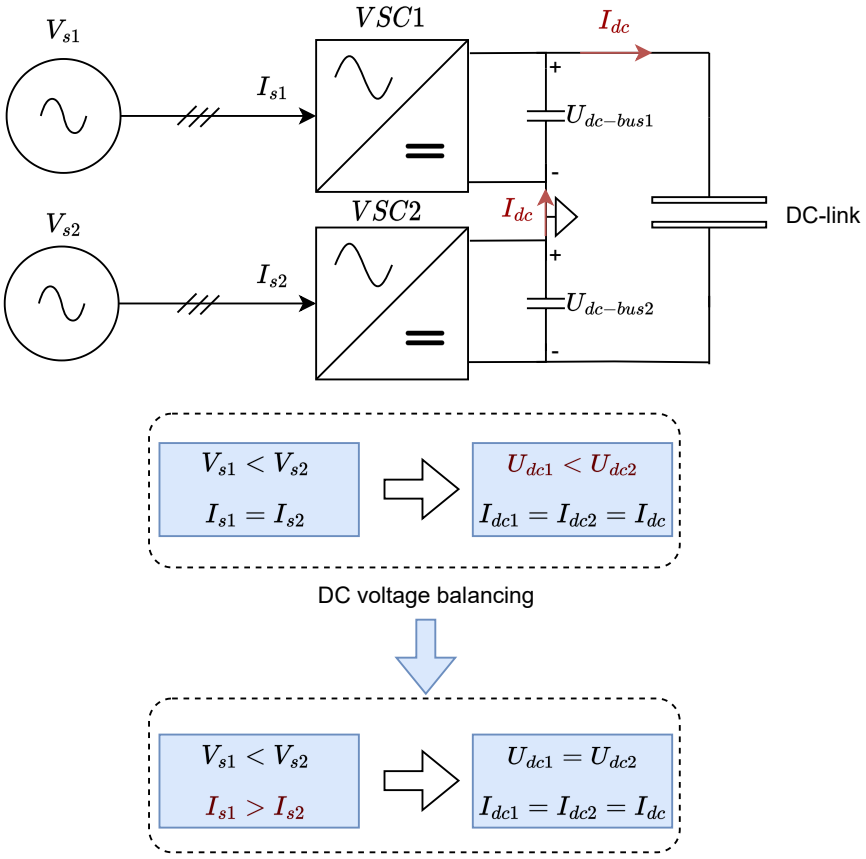


Figure 2: Schematic illustrating in basic terms the challenge introduced by imbalances between the stator segments and the consequence of implementing the proposed DC voltage balancing method.

2. Develop a base case two-module small-scale lab setup with the possibility to expand to more modules.
3. Perform base case system testing of current control and voltage balancing.
4. Investigate the feasibility from a control perspective of different voltage balancing control strategies in the lab.
5. Verify the observed system behavior in the lab by making a simulation model which models the physical lab setup as closely as possible.

1.4.1 Research questions

Based on the research objectives the following research questions were formulated.

Can we create a small-scale lab implementation that emulates the ModHVDC concept at the module level by using separate grid-connected transformers instead of a segmented synchronous machine?

What voltage balancing strategies are feasible from a module-level control perspective, and how do they affect the total system output power?

1.5 Scope

The scope of this thesis is limited to the following aspects of the ModHVDC control system.

- Only a two-module system is implemented and tested both in the lab and the ModHVDC concept simulation model.
- Only two-level voltage source converters are used for the implementation. Multilevel modular converters (MMC) are considered a viable option for the ModHVDC system [4] however, low-power MMC for the lab are harder to find, and MMCs require an additional level of control for internal circulating current, which is considered outside the scope of this thesis.
- For the lab implementation only the module-level control system is considered. I.e. current control and voltage balancing control. Speed control, Maximum power point tracking, and other turbine-related controllers are not attempted to be emulated or considered in the lab setup. Grid-connected transformers, used in the lab setup, operate at the fixed frequency of the grid, therefore, emulating speed control would be challenging with the lab setup developed in this thesis.
- The system is modeled using first-order differential equations. Any nonlinear effects are assumed to be negligible in the simulations.

1.6 Overview of methodology

The methodology employed to investigate the research questions in this thesis consists of three main parts.

1. **Simulation of the turbine level and module level control system in Simulink reduced to a two-module system.**
   This simulation includes inner loop current control, voltage balancing, speed control, and pitch control, with the synchronous generator modeled based on simplified differential equations describing a permanent magnet synchronous generator with a symmetrical rotor.
2. **Laboratory testing of a small-scale two-module system**.
   A small-scale low-power lab setup was designed, constructed, and tested during the course of this master's project. Programmable Texas Instruments microcontrollers and three-phase VSC boards were used for the converter module implementation. The module-level control system was implemented using the Simulink C2000 Microcontroller Blockset, and the isolated stator segments of the generator were emulated using separate three-phase isolation transformers connected to grid-connected variable transformers. The lab setup was developed incrementally, meaning several stages of testing were performed for increasingly complex lab setups were conducted before arriving at the final test setup configuration. As illustrated by Figure 3.
3. **Simulink simulations of the physical laboratory setup.**
   Simulink simulations of the laboratory setup were conducted in parallel with the development of the lab in order to verify the laboratory results and in turn investigate the realism of the simulation models used in this thesis.

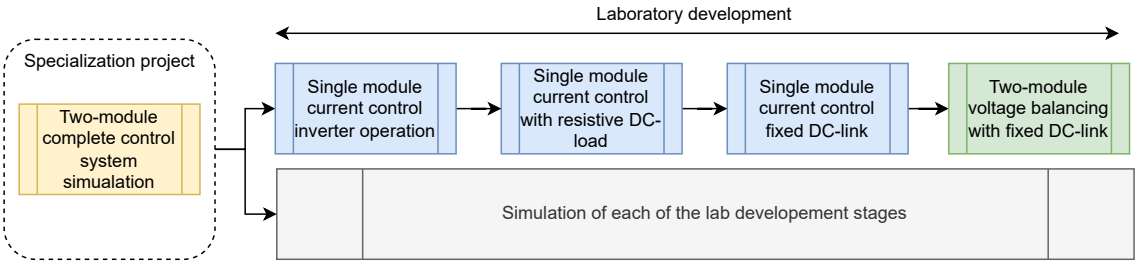


Figure 3: Flow chart showing an overview of this thesis project's methodology.

1.7 Thesis contribution

The main contribution of this thesis work is the development of the laboratory setup and the experimental verification of the voltage balancing control. Therefore, a large part of this thesis report is devoted to the methodology around the lab development. Further research and development will be done on the base case setup developed in this thesis. Previous research on the ModHVDC concept has involved experimental verification[5], however, the lab setup was completely different in design and implementation from the lab developed as a part of this thesis work.

2 Theory

2.1 dq0-transform

The dq0-transform is used to simplify the mathematical representations of three-phase sinusoidal waveforms. By introducing a rotating reference frame that rotates with the same frequency as the waveforms, the waveforms become time-invariant at steady state. This makes computation easier since we can operate with DC quantities rather than oscillating AC quantities.

There exist several variations of the dq0- transform. In this thesis, the amplitude in-variant transform is used. This means that the magnitude of the dq-signals is equal to the peak of the AC signals in the ABC plane, assuming a balanced three-phase. Following the convention in [11], the d-axis of the rotating reference frame is oriented along the A-phase at initialization. The matrix representation of the dq0-transform from ABC coordinates is given in Equation 2.1.

$$T_{dq0} = \frac{2}{3}\begin{bmatrix} cos(\omega t) & cos(\omega t - \frac{2\pi}{3}) & cos(\omega t + \frac{2\pi}{3}) \\ -sin(\omega t) & -sin(\omega t - \frac{2\pi}{3}) & -sin(\omega t + \frac{2\pi}{3}) \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} \tag{2.1}$$

2.2 Modeling of a PMSG

A permanent magnet synchronous generator is proposed for the ModHVDC concept. A mathematical model of the generator is required to design an appropriate control system and formulate a control strategy that determines the generator's operating point based on the desired outcome. In the case of a wind turbine generator, the desired outcome is usually optimizing torque per amp or maximum active power production at the given wind speed.

A simplified mathematical model of the PMSG is used in this thesis. In order to for this mathematical model to be viable the following assumptions have to be made about the physical properties of the PMSG.[12]

1. No magnetic saturation of the stator or rotor iron.
2. No hysteresis effects or eddy currents are present in the generator.
3. The induced emf in the stator coils are balanced three-phase purely sinusoidal waveforms.

The above assumptions result in the following system equations for the PMSG represented in the synchronous reference frame (dq0-plane).[13]

$$v_{ds} = -R_s i_d - L_d \frac{di_d}{dt} + \omega_e L_q i_q \tag{2.2}$$

$$v_{qs} = -R_s i_q - L_d \frac{di_q}{dt} - \omega_e L_d i_d + \omega_e \psi_m \tag{2.3}$$

Where R_s is the stator resistance, L_{ds} and L_{qs} are the d -and q-axis inductance respectively. ω_e is the electrical frequency. ψ_m is the permanent magnet flux linkage. i_d and i_q is the stator current d -and q-axis component. v_{ds} and v_{qs} is the stator terminal voltage d and q-axis components.

The equivalent circuits representing the d and q-axis respectively are displayed in Figure 4. In a symmetrical PMSG with surface-mounted magnets, $L_d = L_q$ is assumed. This assumption is used throughout this thesis, resulting in equal tuning of the d -and q-axis current controllers.

2.2.1 Vector diagram representation of a PMSG

A vector diagram representing a two-pole permanent magnet synchronous machine in steady-state operation is shown in Figure 5. The power angle δ is negative because the emf leads the stator

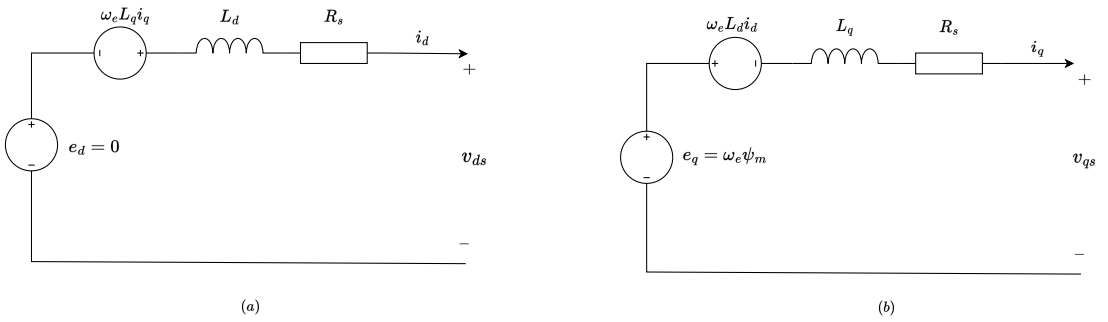


Figure 4: Equivalent circuits of the PMSG mathematical model presented in Equation 2.2 (a) and Equation 2.3 (b).

voltage, which means the machine is operating in generator mode.[14]. The ABC axes indicate the orientation along which the three-phase stator voltage vectors oscillate. The d-and q-axes rotate with a frequency equal to the electrical frequency induced in the stator. θ will therefore be determined by the integral of the rotor rotational speed times the number of pole pairs. In Figure 5 the number of pole pairs is one. Therefore the d-axis will rotate together with the rotor's north pole and θ will describe the rotor position between 0 and 2π.

2.2.2 Electromagnetic torque, active and reactive power PMSG

The electrical torque produced by a PMSG generator is described by Equation 2.4[15].

$$\tau_{em} = \frac{3}{2} P_p(\psi_m * i_{sq} + (L_d - L_q) i_{sd} i_{sq}) \tag{2.4}$$

Given the assumption of equal inductance along the d and q-axis, which is valid in symmetrical PMSM with surface-mounted magnets, the equation simplifies to Equation 2.5

$$\tau_{em} = \frac{3}{2} P_p(\psi_m * i_{sq}) \tag{2.5}$$

Where P_p is the number of pole pairs and psi_m permanent magnet flux linkage.

The active and reactive power transferred from the PMSG produced by a PMSG is described by Equation 2.6 when considering the dq-synchronous reference frame[16].

$$\begin{aligned} p_{gen} &= \frac{3}{2}(v_{sd} \cdot i_{sd} + v_{sq} \cdot i_{sq}) \\ q_{gen} &= \frac{3}{2}(v_{sq} \cdot i_{sd} + v_{sd} \cdot i_{sq}) \end{aligned} \tag{2.6}$$

2.2.3 PMSG current control strategies

With field-oriented current control implemented, a control strategy is needed to determine what reference value should be set for the d -and q-axis component of the stator current in order to reach the desired operation objectives. In the context of an HVDC-connected generator, these objectives are usually to maximize the amount of transmitted power to the DC grid while maintaining the current and voltage levels within the systems rated values. Several control strategies for power and torque in PMSM exist, such as zero d-axis control, unity power factor control, maximum torque per amp, etc.[13] In this thesis, only two will be considered: "Unity power factor" and "maximum torque per amp".

The unity power factor strategy involves controlling the d-axis current in such a manner that the stator current is in phase with the stator terminal voltage. As illustrated in Figure 6a. The

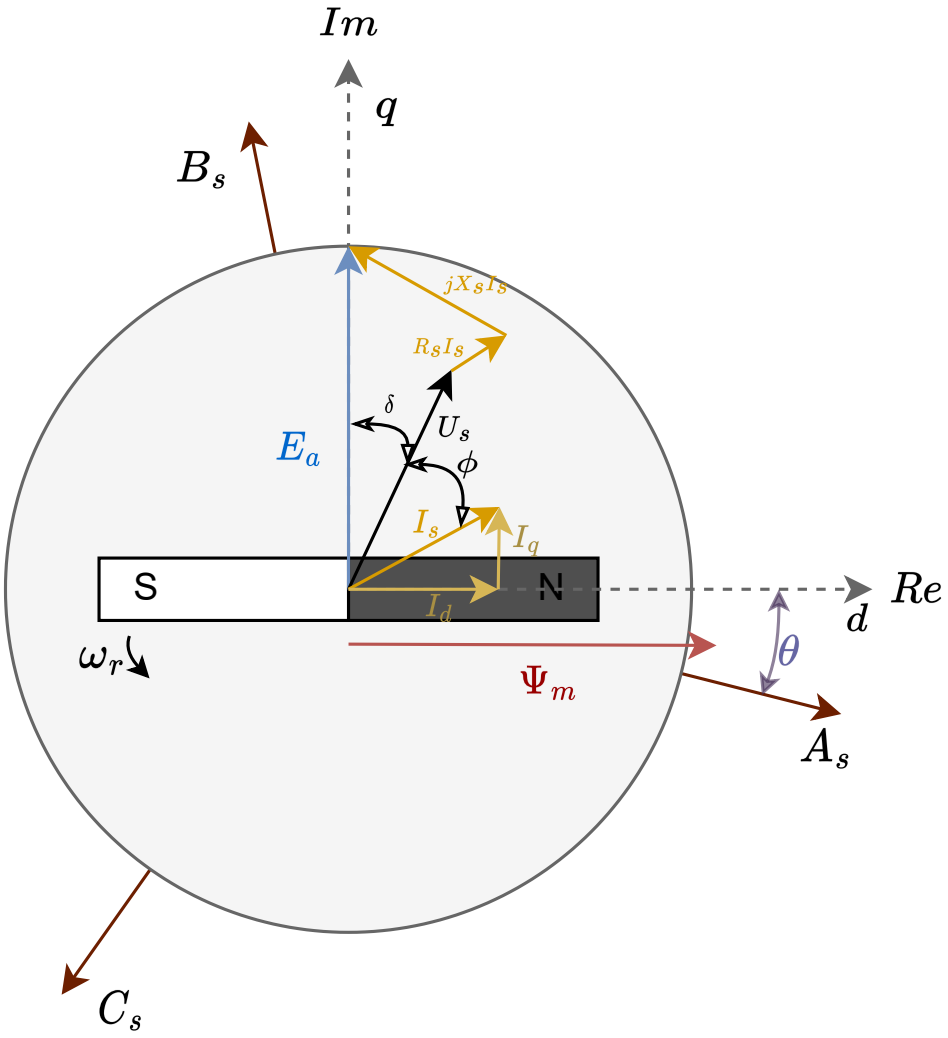
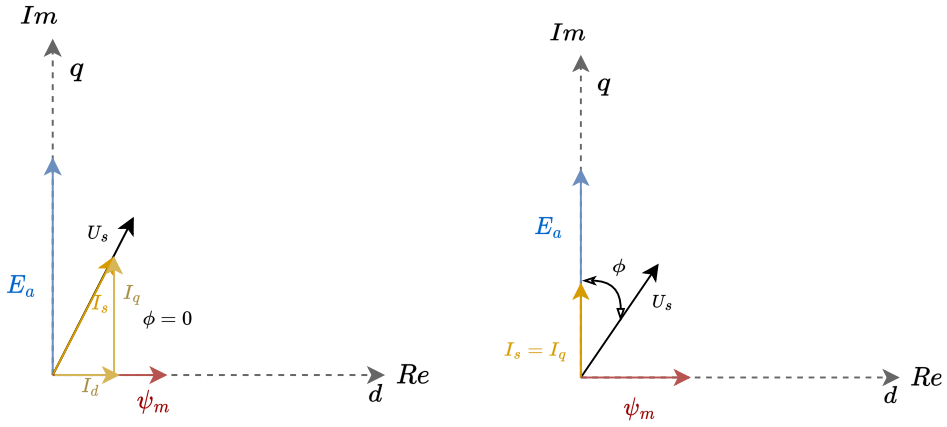


Figure 5: Vector representation of a PMSG during steady state operation. Where δ denotes the power angle, ϕ denotes the phase shift between stator voltage and current, θ denotes the phase angle reference used for the dq0 transformation. This illustration has been inspired by [14] and [12].

advantage of this control strategy is to maximize the utilization of the voltage ampere rating of the VSC.[17].

The maximum torque per ampere strategy is implemented in symmetrical surface-mounted PMSGs[5] by controlling the d-axis current to zero. This ensures that the stator current magnitude correlates directly with the amount of electromagnetic torque produced in the PMSG because the stator current is equal to its q-axis component. Based on Equation 2.4 this gives the maximum amount of torque for the least amount of total stator current.[18] A vector diagram illustrating this technique is presented in Figure 6b.



(a) Unity power factor strategy.

(b) Maximum torque per amp strategy.

Figure 6: Vector diagrams illustrating the relevant current control strategies. This figure is inspired by figures in [18] but are modified to represent generator mode. The relative magnitudes of the vectors are not to scale.

2.3 Grid connected Voltage source converters

Because the lab setup developed in this thesis uses grid-connected VSC, the relevant theory on grid-connected 2L-VSC is presented here.

2.3.1 Two-level voltage source converter

A typical two-level voltage source converter topology is presented in Figure 7. The converter illustrated does not have a split capacitor with access to the neutral point because, in the lab implementation, a split capacitor is not used. However, in the complete control system simulations a split capacitor is used.

2.3.2 Differential equations for grid-connected VSC

A one-line illustration of a grid-connected VSC is shown in Figure 8. The power flow is defined as positive into the converter. Equation 2.7 shows the differential equations describing the grid-to-VSC system displayed in Figure 8.[19]

$$\begin{aligned} v_{d,g} &= Ri_d + L\frac{di_d}{dt} - \omega L i_q + v_{d,c} \\ v_{q,g} &= Ri_q + L\frac{di_q}{dt} + \omega L i_d + v_{q,c} \end{aligned} \tag{2.7}$$

[5]In internal magnet PMSG the assumption of $L_d = L_q$ does not hold true. Therefore reluctance torque must be taken into account. In this case, controlling the d-axis current to zero does not necessarily equate to maximum torque per ampere.

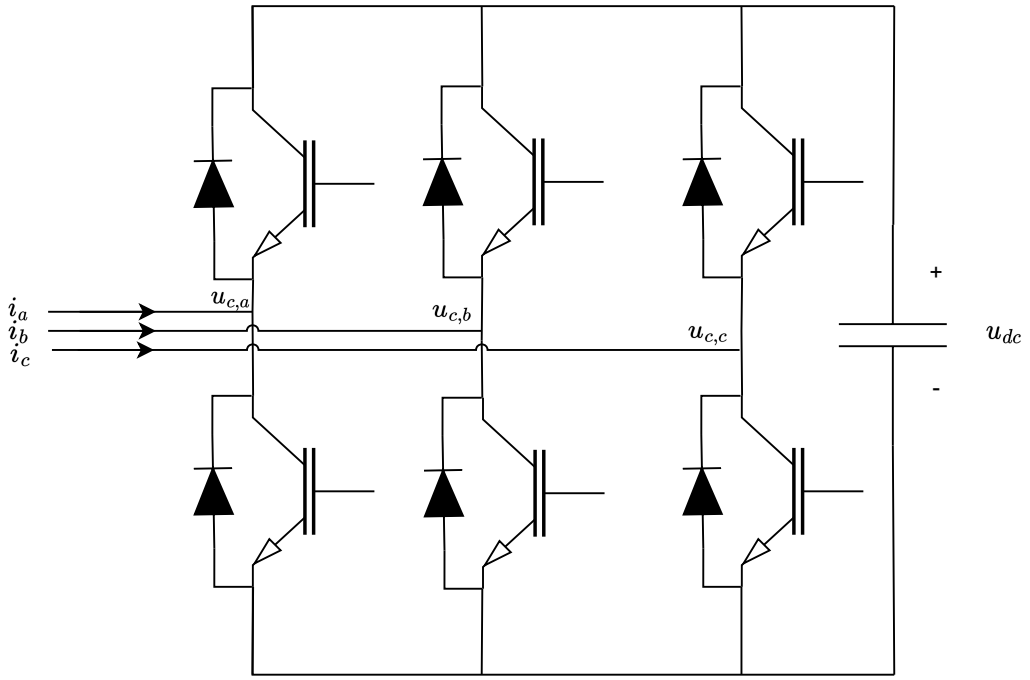


Figure 7: Two-level voltage source converter topology

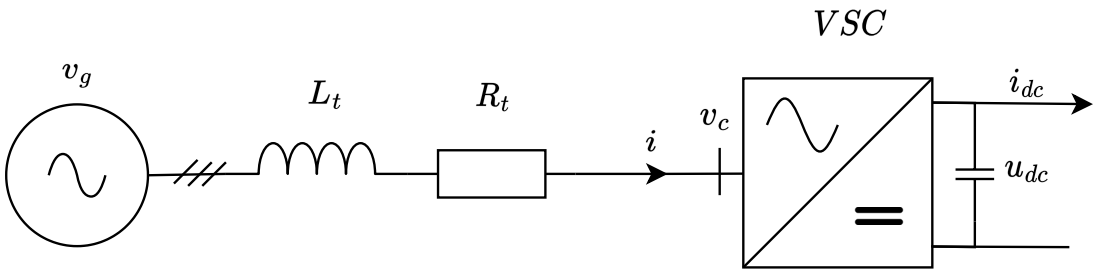


Figure 8: One line schematic of a grid-connected VSC with power flow from AC to DC.

Where v_g is the grid voltage, v_c is the ac terminal voltage. L and R represent the impedance between the grid and converter. This could be the impedance of an L-filter, phase reactor, or as is the case in the lab implementation, three-phase transformers. Hence the use of subscript t in Figure 8.

The equation for active power on the AC side is presented in Equation 2.8.[19]

$$p = \frac{3}{2}(v_d i_d + v_q i_q) \tag{2.8}$$

If the phase angle reference is generated by a phase-locked loop (PLL) which is locked onto the input AC voltage of the VSC converter then the q-axis component of the voltage is zero as long as the PLL is operating effectively. The PLL structure is explained in Section 2.3.3. Assuming $v_q = 0$, the power equations simplify to Equation 2.9[19].

$$\begin{aligned} p &= \frac{3}{2} v_d i_d \\ q &= \frac{3}{2} v_d i_q \end{aligned} \tag{2.9}$$

2.3.3 Phase locked loop (PLL)

In order to perform the dq0 transformation, the phase angle and frequency of the three-phase voltage must be known. In an electrical machine, this information can be estimated based on the rotor position and speed. In grid-connected VSC, a phase-locked loop (PLL) can be used to estimate the phase angle and frequency of the system reference voltage.

The dq-PLL is implemented in three main steps shown in Figure 9. First, the three-phase waveform is transformed into the dq0-plane using the dq0 transform. The voltage phase angle used for dq0-transform is the output phase angle from the PLL itself, creating a feedback loop. Second, the q-axis component is controlled to zero using a PI or PID controller. Due to the initial alignment of the d-axis with phase A in the dq0 transform, as discussed in Section 2.1, zero q-axis voltage corresponds with zero phase shift between the actual phase angle of the ABC-voltage and the phase angle output of the PLL. Lastly, the output of the PID controller is added to the angular velocity of the ABC waveform. This sum is then integrated to obtain the phase angle [20].

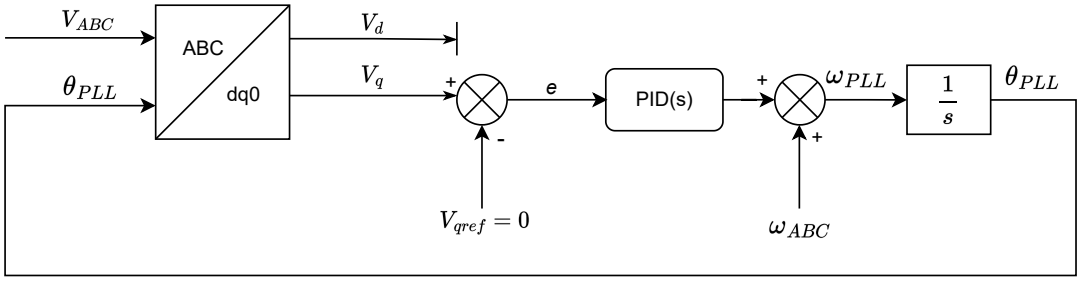


Figure 9: dq-Phase locked loop structure diagram.

2.4 Maxmium power transfer theorem

The maximum power transfer theorem becomes relevant in Section 5.6.3 describing the laboratory implementation of the small-scale system emulating the ModHVDC concept due to the high relative impedance of the AC-side circuit. The maximum power transfer theorem states the following relationships between the power transferred to the load impedance in an AC system relative to the series source impedance.

- "If the load resistance and the load reactance are independently variable, maximum power is transferred to the load when the load impedance is equal to the complex conjugate of the internal impedance of the source."[21]
- "If the load has a variable impedance but a constant power factor, maximum power is transferred to the load when the magnitude of the load impedance is equal to the magnitude of the internal impedance of the source"[21]

2.5 Tuning techniques for PI controllers*

There exist many techniques for tuning PI controllers. In this thesis, the Modulus optimum method is used to tune the inner-loop current controller, and the symmetrical optimum method is used for the outer loop speed and voltage balancing control.

**The following sections on PI-controller tuning are taken from the specialization project report written by the author of this thesis in the Autumn of 2022.[1] Certain changes have been made.*

2.5.1 Modulus optimum

The modulus optimum method is suitable for systems with a single dominant time constant in the plant transfer function. If the dominant time constant is orders of magnitude larger than all other time constants in the control loop, it is an allowable approximation to merge all the remaining smaller time constants into a single time constant (T_{sum}). This assumes only first-order expressions in the open loop transfer function. Then the dominant pole of the system can be effectively canceled by choosing the integral time constant of the PI-controller (T_i) equal to the dominant time constant in the plant.

The modulus optimum method defines K_p such that the closed-loop transfer function has an underdamped response, with a dampening factor $\zeta = 1/\sqrt{(2)}$. In theory, the modulus optimum method should result in a fast unit-step response with a reference overshoot of just 4.7%.

The equations defining the PI controller tuning parameters K_p and T_i are displayed in Equation 2.10.

$$\begin{aligned} T_i &= T_{dominant} \\ K_p &= \frac{T_i}{2K_s T_{sum}} \end{aligned} \tag{2.10}$$

where K_s is the gain of the open loop system, excluding the K_p, and $T_{dominant}$ is the dominant time constant of the plant[22].

2.5.2 Symmetrical optimum

Symmetrical optimum is suitable when the system plant has an integrator in its transfer function. I.e., an open loop pole at the origin. In this case, one cannot cancel the plant pole by choosing the integrator time constant equal to the dominant. If one were to cancel T_{sum} by selecting $T_i = T_{sum}$ the remaining transfer function would have two integrators and a phase margin of 0 deg. This is a marginally stable system, which is unacceptable because the system is operating on the verge of instability, and any discrepancy between the system model and the real-life system could make the real-life system unstable. The symmetrical optimum method is therefore employed. The tuning constants are defined as presented in (2.11)

$$\begin{aligned} T_i &= \alpha T_{sum} \\ K_p &= \frac{T_{plant}}{\sqrt{\alpha} K_s T_{sum}} \end{aligned} \tag{2.11}$$

where α is a tuning constant that is chosen by the designer based on the desired dampening and cross-over frequency of the system [22].[6]

2.6 Turbine operational zones

In this, the operation zones of a wind turbine are divided into four sections. The definition of the operating zones is based on [23][7], and are illustrated in Figure 10. Zone 1 is before the windspeed reaches the cut in speed which is where the turbine begins its operation. Zone 2 the turbine and the windspeed are below their respective nominal values, and the maximum power point tracker decides the turbine's rotational speed. In zone 3 the turbine has reached its nominal speed and is kept constant here, but the windspeed does not yet equate to full loading of the generator. In zone 4 the wind speed has surpassed the nominal wind speed, and the generator is operating at maximum power. In this zone, the pitch controller is responsible to adjust the power coefficient in order to maintain the turbine speed at the nominal level.

[6] The tuning constant in symmetrical optimum is often depicted as β, but since β is used to describe the pitch angle of the turbine blades in this report, α is used instead.

[7] Operational zone 1 is defined slightly differently in [23] than in this thesis. Zone 1 is not discussed further in this thesis and is, therefore simply defined as a zero speed and power zone.

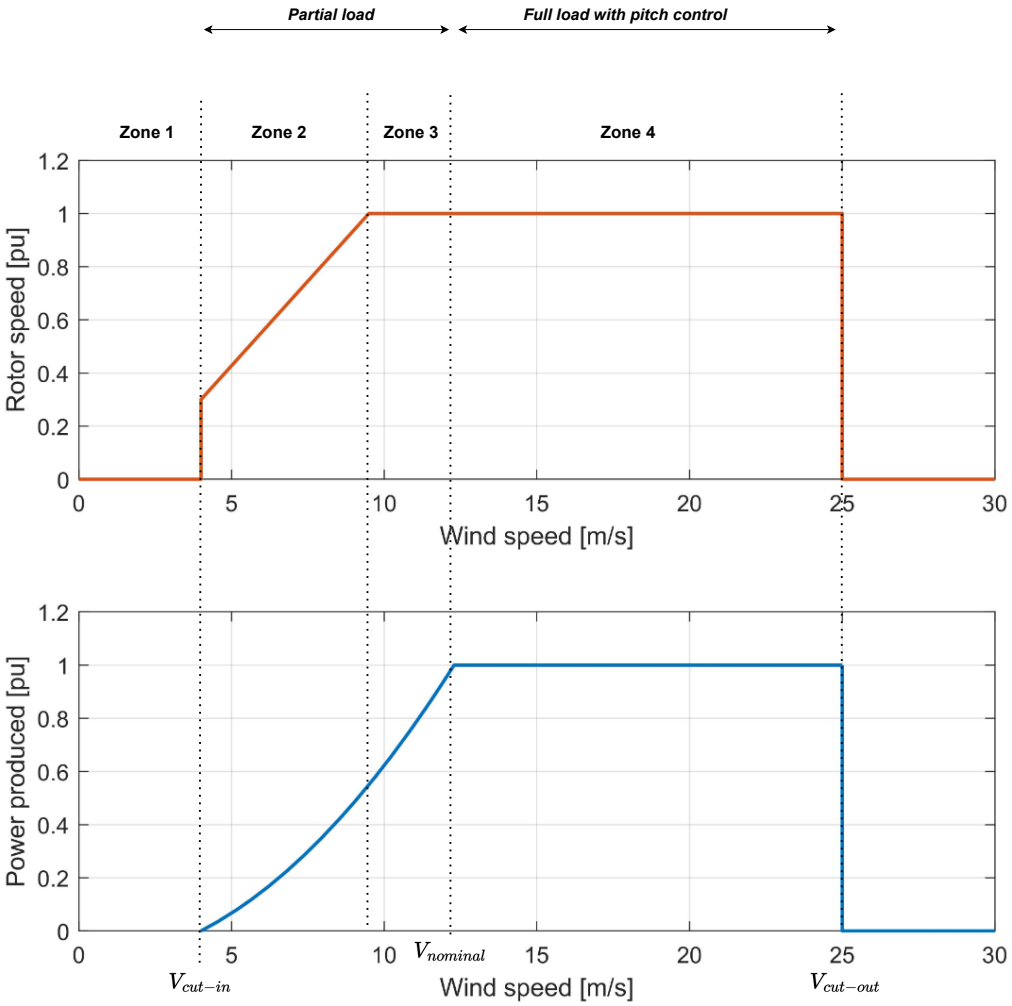


Figure 10: Operational zones of a wind turbine. Inspired by [23] and [24]

3 Control system design and implementation

In this section, the control system of the ModHVDC system is presented. First, the complete control system architecture for the control system used for the ModHVDC system simulation is introduced. The presentation of the architecture does not go into detail on each controller's design and functionality but focuses on the system structure and flow of information, i.e measurements and generated references. The subsequent sections describe each of the controller blocks in detail, starting from inside the nested system structure and working outwards. The development of the control system as a whole is credited to [5], and the direct speed controller design is credited to [4].

3.1 Control system architecture

The total ModHVDC control system discussed in this thesis hereby referred to as the "complete control system", is illustrated in Figure 11. The control system is based on proportional-integral (PI) controllers and has two levels to its structure. The outer level, sometimes referred to as the master level, is the turbine-level control system which includes the Maximum power point tracker (MPPT), pitch controller, DC voltage set point controller, and direct speed controller. The inner level, sometimes referred to as the "servant-level", is the module-level control system which is based on field-oriented vector control and consists of an outer loop voltage-balancing controller and an inner loop current controller. The turbine-level generates the references for the module-level controllers.

Ultimately the complete control system generates only two outputs that affect the physical system. The pitch controller controls the mechanical pitch angle (β) of the turbine blades according to the desired power level extracted from the wind. The current controller outputs dq-axis voltage references which are translated into gate signals for the corresponding VSC. In Figure 11 the module-level control system is illustrated for module i in a two-module system consisting of module i and $i+1$. Every system module has its own instance of the module-level control system. Flux weakening control is not implemented, therefore, the d-axis current is always controlled to zero in accordance with the "maximum torque per ampere" control strategy presented in Section 2.2.3.

Section 3.2 and Section 3.3, can be considered as a restating of paragraphs from the corresponding specialization project [1]. Necessary changes have been made to the text.

3.2 *Current control

This section presents the current controller design, functionality, and tuning. The current controller design and synthesis are again credited to [5].

3.2.1 Controller requirements

The current controller is the core of the complete control system due to the cascade structure. Therefore, the design and tuning of the controller should be such that certain performance requirements are met.

- High controller bandwidth compared to the outer loop.
- Minimal tracking error over a wide range of frequencies.[25]
- Robust control, i.e sufficient suitability margin.

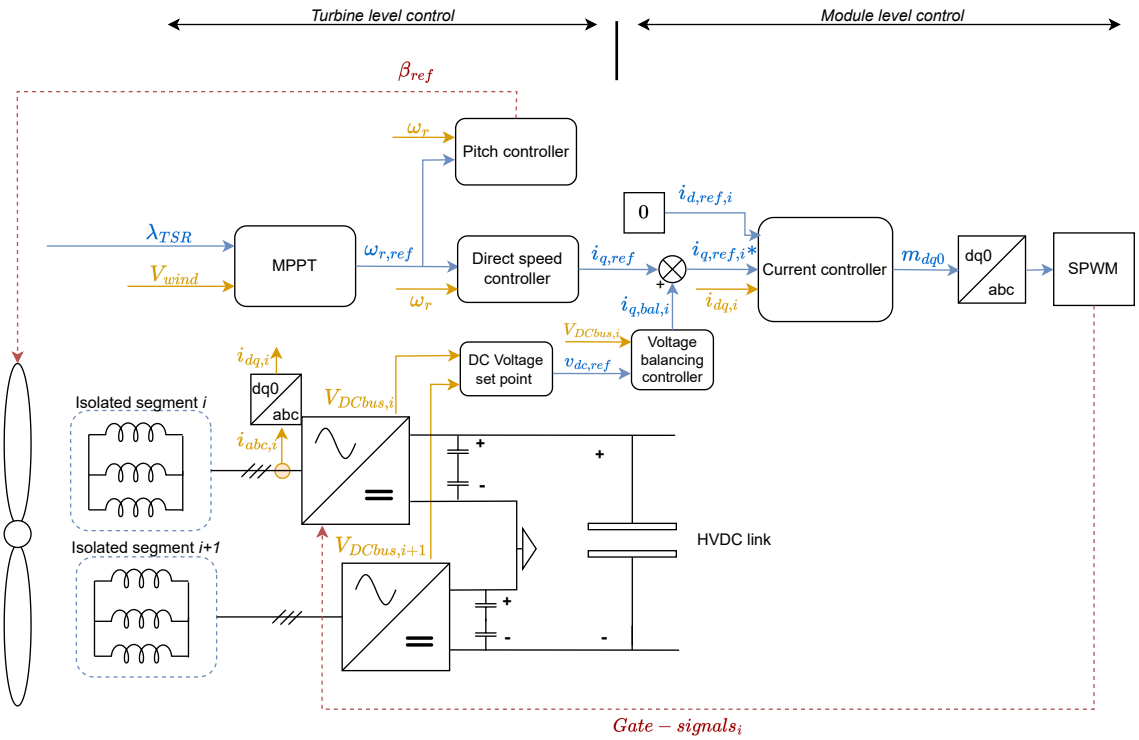


Figure 11: Complete control system architecture in the context of a two-module system physical system. Yellow arrows: measured values, Blue arrows: predetermined/calculated references, Red dotted arrows: control system outputs that actively affect the physical system.

3.2.2 Current controller structure

The current control structure is based on linear feedback control with proportional and integral (PI) controllers. The equations describing the dynamic model of the PMSG are given in (2.2) and (2.3). It is desirable to control the d -and q-axis currents separately. I.e. as two separate single-input-single-output systems (SISO) instead of a single MIMO system.[26] In order to do this, the d-and q-axis needs to be decoupled. Decoupling is achieved via feed-forward of the mutual flux linkage between the d and q axis, represented by the terms u_{qI} and u_{dI} in (3.1) and (3.2) respectively. The remaining terms are controlled by the PI controller [27]. The current control structure is illustrated in Figure 12

The rotor in the PMSG is assumed to be symmetrical $x_q = x_d = x_s$. Therefore x_s is used in this report.

$$\begin{aligned} u_{q,ref} &= -u_{qI} + u_{qII} \\ u_{qI} &= u_{PI} \\ u_{qII} &= -\omega_r x_s i_d + \omega_r \psi_m \end{aligned} \tag{3.1}$$

$$\begin{aligned} u_{d,ref} &= -u_{qI} + u_{qII} \\ u_{dI} &= u_{PI} \\ u_{dII} &= -\omega_r x_s i_q \end{aligned} \tag{3.2}$$

The feedforward terms should equate to the actual electromagnetic dynamics of the PMSG. Feed-forward is an effective control strategy as long as the compensation term models the real dynamics of the system somewhat accurately. If the compensation terms misrepresent the actual coupling between the axes, then the feed-forward compensation terms will worsen the system response and potentially make the system unstable. Small differences between the model dynamics and the real dynamics will be compensated by the PI controller [28],[29].

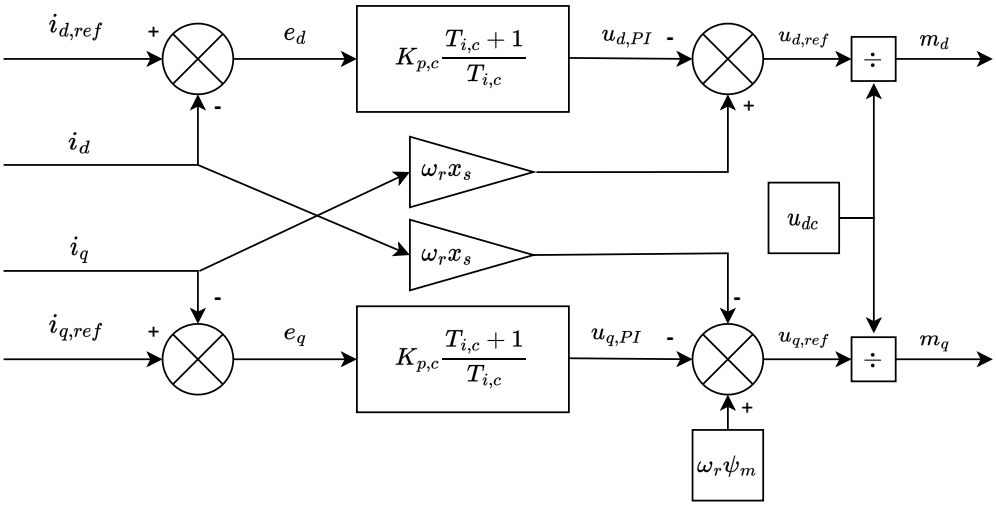


Figure 12: Block diagram of current controller structure in dq frame.

Table 1: Current controller tuning parameters

Parameter	Value
T_ω	0.5 [ms]
$T_{i,f}$	2.0 [ms]
T_i	0.088 [s]
K_p	0.36 [pu]

3.2.3 Current controller tuning

The current controllers are tuned using the modulus optimum method. Because the electrical RL-time constant of the stator windings is much larger than the other time constants in the control loop, it will be a valid approximation to merge the remaining time delays of the loop into one time constant, T_{sum}. Then by choosing the integral time constant equal to the electrical time constant the dominant pole of the system is cancelled. [22].

The resulting open loop transfer functions of the current controller loops are given in (3.3).

$$\begin{aligned} h_{oid} &= \frac{K_{p,d}}{T_{i,d} \cdot s} \cdot \frac{\omega_b \cdot T_d}{x_s(1 + T_{sum} \cdot s)} \\ h_{oiq} &= \frac{K_{p,q}}{T_{i,q} \cdot s} \cdot \frac{\omega_b \cdot T_q}{x_s(1 + T_{sum} \cdot s)} \end{aligned} \tag{3.3}$$

T_{sum} contains the sum of all the significant time delays of the current loop. This includes the current measurement filter and PWM/Converter delay, represented by $T_{i,f}, T_{C,delay}$ respectively. $T_d = T_q = x_s/(w_b \cdot r_s)$

The frequency response and stability margins of the current control loop are presented in Figure 13. The phase margin is approximately 65 degrees. Usually, a stability margin of more than 45 degrees is desirable [29].

The estimated time delay introduced by the VSC and current measurement filter is discussed in Appendix A.1, along with a discussion on the allowable current ripple and subsequent filtering.

3.3 *Voltage balancing

The proposed voltage balancing controller is based on DC bus voltage state feedback with a proportional-integral controller. As described previously, the voltage balancing controller is a

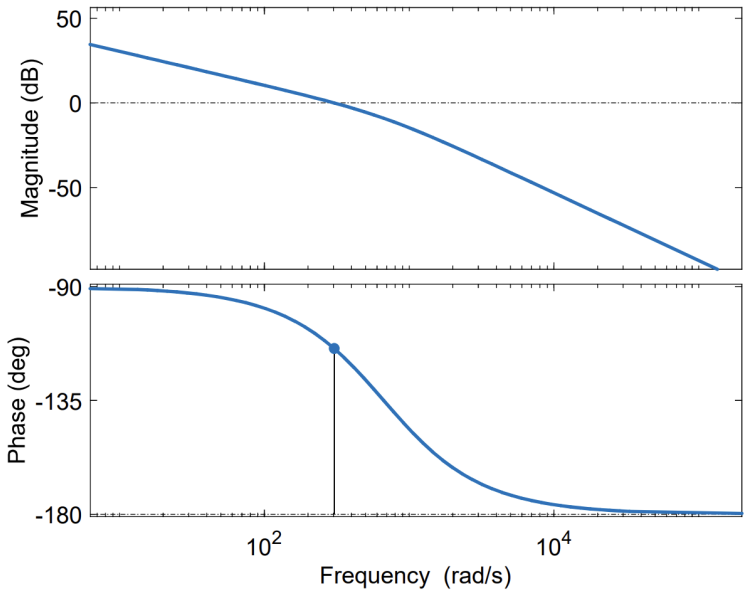


Figure 13: Open loop frequency response current controller. Phase margin indicated.

module-level controller, meaning that each module controls its own DC-bus voltage with identical but individual controllers. The set point voltage reference, on the other hand, is set at the turbine level and is the same for all modules. An illustration of the voltage balancing control algorithm is displayed in Figure 14.

The module voltage balancing controller is placed in the outer loop of the controller cascade. The output of the voltage controller is a balancing current reference $i_{q,bal,i}$. This balancing current is added to the reference from the speed controller $i_{q,torqe,i}$, and fed to the respective module current controller. As shown in Figure 14. Here $u_{dc,f,i}$ illustrates that it is the filtered value being used.

3.3.1 The need for voltage balancing control

The DC link is considered fixed in this thesis. In a full-scale implementation of the ModHVDC system, the DC-link is controlled by the grid side control system common for the entire wind park. Therefore, the assumption of a fixed DC-link is considered valid. A fixed DC link voltage means that the sum of the DC-bus voltages in each turbine always equals the DC-link voltage, as stated by (3.4). Therefore, the voltage balancing controller controls only the relative voltage magnitude between the module DC-bus voltages.

$$u_{DC-link} = \sum_{i=1}^{N} u_{dc,i} \tag{3.4}$$

A voltage balancing controller would be redundant if we assume perfect symmetry between all modules and only allow generator mode operation. This is because the DC-bus voltages are inherently stable in generator mode operation [8], and perfect symmetry between all modules would result in equal power transfer to the DC link from all modules, resulting in equal DC-bus voltages.

However, in a real-life system, there is a possibility of significant deviations in flux linkage, resistance, converter efficiency, or other module parameters between segments. Such imbalances will affect the power produced by the corresponding module and subsequently DC-bus voltage of the

[8] A small signal stability analysis is performed in [5], and stability in generator mode was shown. In this thesis, stability is demonstrated through simulations and experimental verification. The small signal stability analysis showed the DC-bus voltages to be inherently unstable in motor mode operation. Motor mode operation is considered unnecessary and is not analyzed in this thesis.

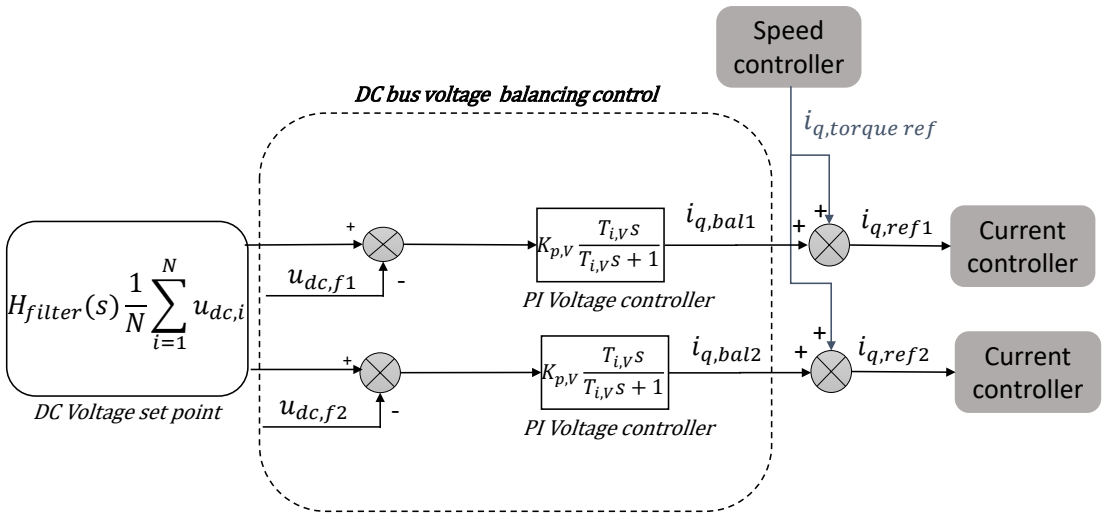


Figure 14: DC-bus voltage controller illustrated in the context of a two-module system.

respective module. The relationship describing the DC bus power is given in (3.5). Because the DC current is common for all modules, the power a module produces is directly proportional to its DC bus voltage. When the DC bus voltage of one module goes down, then the voltage of another module must come up in order to fulfill the condition of constant DC link voltage. Therefore, unbalanced power production between the modules will lead to one or more modules operating at above-rated DC voltage. This puts increased stress on the voltage insulation and converter components and must be avoided over time. Hence the need for control of the voltage balance between modules.

$$p_{dc,i} = u_{dc,i} \cdot i_{dc,i} = u_{q,i} \cdot i_{q,i} \tag{3.5}$$

Where $p_{dc,i}$ is the power on the dc bus of module i.

In the synchronous rotor-oriented reference frame, the d and q-axis currents correspond to the reactive and active power respectively. The DC-side power is described by (3.5). Because the DC current is the same for all modules the DC bus voltage of each module is controlled using the relationship described in (3.5). [5] The voltage balancing controller relies on the positive correlation between the AC-side q-axis current component $i_{q,i}$, and power transmitted to the DC side of the VSC $p_{dc,i}$. In commercial generators, such a positive correlation is usually the case because the system operating range is far away from the point of maximum power transfer to the VSC in order to have high system efficiency. I.e. the stator resistance is usually low relative to the system ratings.

3.3.2 Tuning of DC bus voltage balancing control

The desired characteristic of the DC voltage control is a stable, robust response with minimal overshoot. In order to achieve this, tuning with the symmetrical optimum method as well as filtering of the feedback measurements, have been employed.[22]

The system transfer function is presented in (3.8). The current controller has been reduced to a first-order transfer function (3.6).[26]

$$\begin{aligned} h_{ol,cc}(s) &= \frac{1}{T_{eq,cc}s + 1} \\ T_{eq,cc} &= 2 \cdot T_{sum,cc} \end{aligned} \tag{3.6}$$

The plant transfer function is developed from the relationship between the change in DC capacitor

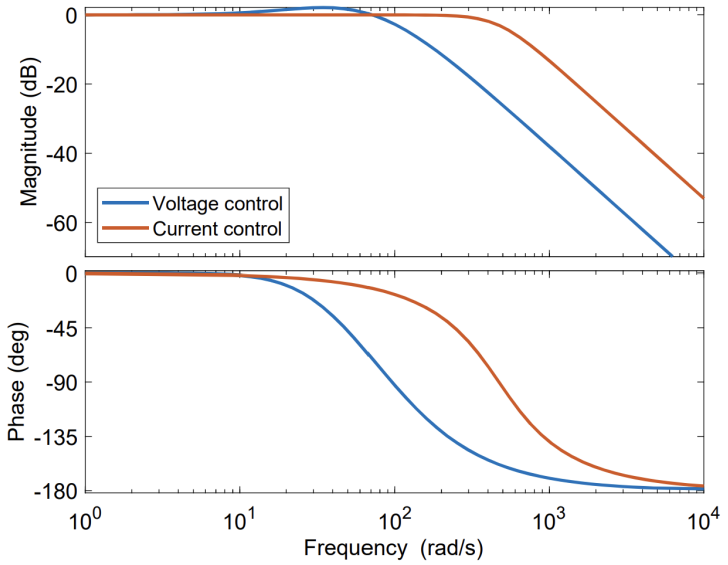


Figure 15: Closed loop response of voltage and current controller.

voltages and the DC-link current. Described by (3.7),[4] chapter 2.4.

$$\frac{c}{\omega_b}\frac{dv_{dc,i}}{dt} = i_{dc,i} - i_{dc-link} \tag{3.7}$$

The PI-controller, first-order approximation, filtering, and the plant gives us the simplified open loop transfer function of the system. Assuming unity modulation index [26][29].

$$\begin{aligned} h_{ol,vc}(s) &= K_p \frac{1+T_i s}{T_i s}\frac{1}{1+T_{sum,vc}\cdot s}\frac{1}{T_c s} \\ T_{sum,vc} &= T_{eq,cc} + T_{f,vc} \end{aligned} \tag{3.8}$$

Because the plant transfer function has an integrator the symmetrical optimum tuning method is employed. resulting in the following tuning constants.

Table 2: Voltage controller tuning. $\alpha = 10$

Parameter	Value
$T_c = \frac{c}{\omega_b}$	34 [ms]
$T_{vc,f}$	2.0 [ms]
$T_{eq,cc}$	3.0 [ms]
$T_{i,vc}$	50 [ms]
K_p, vc	2.16 [pu]

A phase margin of 55°is achieved for the voltage controller open loop transfer function with the tuning shown in Table 2. An α value of 10 is used to ensure a sufficient phase margin. Figure 15 shows the closed loop response of the inner and outer loops of the cascade controller. The bandwidth of the inner current control loop is about five times greater than the outer voltage control loop. Ideally, it should be ten times greater.

3.3.3 Set point voltage reference

The DC-bus voltage reference set point is defined as the filtered average of all N DC-bus voltage measurements. As shown in (3.9). The advantage of using the module measurements themselves

is that all of the modules can always reach the DC bus voltage set point reference. This is not necessarily the case if the voltage set point is equal to $U_{DC-link}/N$. Any error between the measured and the actual DC bus voltage in a module will cause the sum of the measured DC bus voltages to be unequal to $U_{DC-link}$. Consequently, it is impossible for all N modules to stabilize at the reference set point simultaneously. This in turn will lead to the DC-bus voltage controllers fighting each other in order to match the reference, causing a steady state error that is physically impossible for the controllers to remove. This phenomenon can be observed in the lab Section 5.9.3 where the steady state error causes the integral terms of the PI controller to windup in both modules.

The following thought experiment illustrates why any error in any of the module DC bus measurements will cause integral windup in all modules. Imagine a three-module system with 10kV on each DC bus module. The reference set point is 30kV/3 for all modules. Module 1 measures its DC voltage to be 1% lower than its actual voltage, while the remaining two modules have accurate measurements of 10kV each. In order to reach the reference, module 1 increases its balancing current output which increases the module power and subsequently the DC-bus voltage to the reference. However, since the actual voltage of module 1 is now 1% higher than 10kV the voltage on the remaining modules drops by 0.5%. Module 2 and 3 will then increase their respective balancing current output to compensate for this drop in voltage, causing a drop in voltage in module 1. This cycle will continue, and the balancing currents of all modules will continue to increase until the system saturates. In the actual system, the voltage balancing controllers of modules 2 and 3 will respond faster than described in this thought experiment which will cause the measured voltage on module 1 to be stuck below the reference. But the constantly increasing balancing current will be observed in all modules.

$$u_{dc,ref} = H_{filter}(s)\frac{1}{N}\sum_{i=1}^{N} u_{dc,i} \tag{3.9}$$

Where $H_{filter}(s)$ indicates the filtering of the voltage measurements.

3.4 Voltage balancing control strategies

The voltage-balancing controllers' operating region is restricted by the rated current level of the VSC and generator according to Equation 3.10, which assumes accurate reference tracking by the current controller and a d-axis current of zero. When the turbine is operating at a constant speed and maximum electrical torque (zone 4), the q-axis current is equal to the system's rated current value. In this zone of operation, the balancing current output from the voltage balancing controller can not be positive without violating the current limit. If the system is designed to be operated at the rated current during normal operation (i.e $i_{s,rated} = i_{s,nominal} = 1pu$)[9] then the limit imposed by Equation 3.10 must be respected. In this case only the "Weakest link" balancing strategy is feasible for the system, which will result in the derating of the output power for the entire turbine. However, if the AC side of the system has a current rating above the nominal value, then the "Split the difference" and "Lift to nominal power" strategies can be implemented.

$$i_s = i_{q,ref}* = i_q, ref + i_{q,bal} \leq 1pu \tag{3.10}$$

Where i_s is the total stator current, $i_{q,ref}*$ is the reference given to the current controller and $i_{q,ref}$ and $i_{q,bal}$ are the output references from the speed controller and voltage balancing control respectively.

The three voltage balancing strategies outlined below are discussed mainly in the context of parameter deviations that lead to reduced power production relative to the expected. Parameter deviations resulting in above-expected power production in some segments/modules can also occur and are handled equally by the voltage balancing controller. However, it is mainly the upper

[9] In this thesis nominal refers to the voltage, current, power, etc. at which the system is designed to operate. Nominal values are used to form the basis for the per-unit system. Rated refers to the maximum voltage, current, power, etc at which it is safe to operate over time.

limit of the q-axis current which causes challenges in the control strategies, not the lower limit. Therefore the control strategies are mainly discussed in the context of modules underproducing power due to parameter deviations. The first two strategies discussed, namely the "weakest link" and "split the difference" strategies are discussed in [4]. The last strategy was, to the best of the author's knowledge, not considered by [4]

3.4.1 "Weakest link" voltage balancing strategy

The weakest link strategy must be implemented if the maximum allowable AC current (rated current) is equal to the current level during normal operation in zone 4 (nominal current). The strategy is implemented by imposing a saturation limit on $i_{q,bal}$ according to Equation 3.11. The output from the speed controller $i_{q,ref}$ is also limited to 1pu. The voltage balancing controllers now have an upper saturation limit of zero when the speed controller requests maximum electrical torque (zone 4 operation). The consequence of the "weakest link" strategy is that the output DC bus power of all the modules must come down to the level of the weakest module to have equal DC bus voltage on all modules in zone 4. This effectively derates the entire turbine by the same percentage as the difference between the weakest module power output and the nominal power output. The results of voltage balancing with the "weakest link" strategy are presented for the complete control system simulation in Section 4.2.1 and from the experimental verification in Section 5.9.4.

$$i_{q,bal} \leq i_{q,ref} - i_{s,rated} \tag{3.11}$$

The weakest link strategy is effective in balancing the DC bus voltages, however, the derating of the whole turbine would be critical from an economic perspective. In [4] a case study that quantified the total loss in annual energy for an eight-module 10MW wind turbine was performed. An expected loss of 1300MWh was estimated as a consequence of derating the turbine to achieve voltage balancing. Such a loss in produced power would potentially take away the proposed economic benefit of the ModHVDC system. In the case study, the parameter deviations between the modules were estimated based on randomly selecting numbers from a normal distribution of expected parameter deviations. The largest DC-bus voltage deviations were roughly $\pm$ 5%, which the author considered to be conservative[4].

3.4.2 "Split the difference" voltage balancing strategy

The "split the difference" voltage balancing strategy treats the balancing current as a free variable. In other words, no saturation limit is imposed on the voltage balancing output. Since the voltage balancing controller of each module can operate freely, the sum of the balancing current outputs of all module control systems will be zero, assuming identical control responses in all modules. When the sum of all voltage balancing currents is zero, the electrical torque in the generator is maintained according to Equation 2.5. This means the sum of active power produced by the generator segments does not change. In other words, the "split the difference" voltage balancing does not compensate for the lost power production due to negative parameter deviations in certain modules. The strategy only ensures that the modules split the difference in power production between them, ensuring equal power transfer to the DC-bus in all modules. Explained in the context of a three-module system where two of the modules are operating at nominal power and the third module has a power transfer to the DC-bus of -5% relative to the other modules, "split the difference" voltage balancing would result in a negative power adjustment of 1.25% in modules 1 and 2 while the power in module 3 increases by 2.5%.

The "split the difference" strategy will require overrating of the AC side current relative to the normal operating range because the strategy does not limit the balancing current contribution to the q-axis reference. Therefore, modules can be forced to operate continuously at above nominal AC current.

3.4.3 "Lift to nominal power" strategy

The last strategy considered in this thesis is the "lift to nominal power" strategy. This strategy controls the q-axis current of all modules such that every module's power transfer to the DC bus is equal to the highest power-producing module. This strategy is implemented by simply setting the saturation limit on the balancing current according to Equation 3.12. This will prevent any modules from reducing the produced power in order to balance the voltages. Increasing to the highest-producing module can be an issue if some modules have "better" than expected performance. This can then lead to the system producing more than nominal power in zone 4. However, this should be solvable in theory by imposing an upper-level saturation on the speed controller which is equivalent to the measured overproduction in power. However, this has not been tested in this thesis and can be considered future work.

$$0 \leq i_{q,bal,i} \leq 1pu \tag{3.12}$$

3.5 DC-Voltage droop control

In [5] the voltage droop controller is proposed in order to compensate for any nonzero torque contribution from the voltage balancing controllers due to a potential difference in controller response time between the modules. The voltage balancing control system is over-determined. Meaning there are infinite combinations of module balancing currents that yield equal DC bus voltages in all modules. If the response times of the voltage balancing controllers are different, this could result in one or more modules contributing with a greater balancing current than the module's DC bus voltage percentage deviation from the voltage set point. For example in a two-module system with ±5% DC voltage deviation from the set point in the modules, the faster module could end up compensating for 7.5% of the voltage deviation while the slow module only compensates 2.5%. Since the voltage balancing controller reaches a steady state as soon as the DC bus voltages are equal this imbalance in the q-axis balancing current will not change, leading to a nonzero torque contribution from the voltage balancing controller and higher than necessary AC side current in the fast module.

The droop control compensates for this by changing the voltage set point according to the average of the balancing currents from all modules. If the sum of the voltage balancing currents is net positive the voltage set point will be reduced, causing all modules to believe they are operating at too high DC bus voltage and subsequently reduce their balancing current output. When the sum of the balancing currents is zero, the contribution from the droop controller is also zero because it is just a proportional contribution. Zero contribution from the droop control corresponds to steady state. The same happens if the sum of the balancing currents is negative, just in the opposite direction. [5]

The droop controller is illustrated in Figure 16.

The droop controller should not be activated if the "weakest link" or "lift to nominal power" voltage balancing control strategies are employed. Because these strategies allow the sum of the voltage balancing currents to be non-zero. Which is exactly what the droop controller is trying to prevent. In this thesis, a direct speed controller is used for the turbine level control instead of an indirect torque controller like in [5]. Therefore, a nonzero torque contribution from the voltage balancing controller is not a big issue for the system because the speed controller will just reduce its q-axis current reference in response to an increased torque contribution from the balancing controller and, visa versa for a negative contribution.

The tuning of the droop controller is taken directly from [5]. $k_{delta} = 0.05$ and $T_{LPF} = 0.5s$.

**The following subsections on direct speed control, MPPT, and pitch control can be considered a restating of paragraphs from the author's specialization project [1]. Necessary changes to the text have been made.*

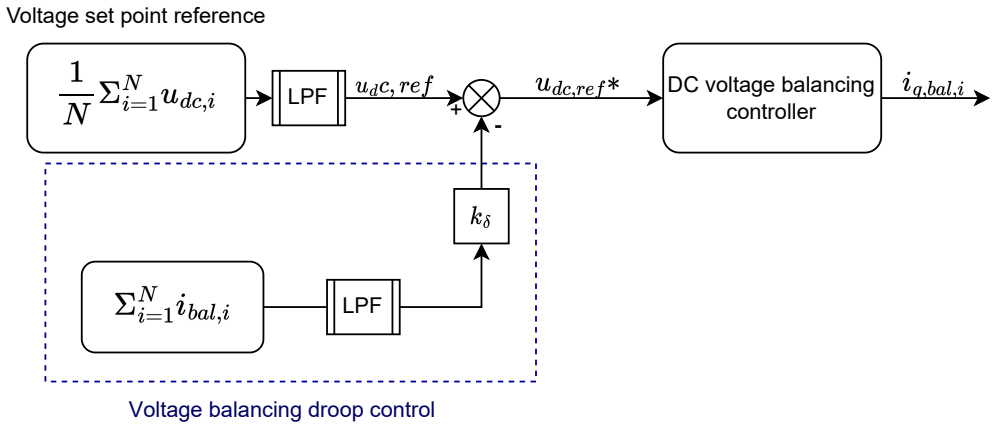


Figure 16: DC-voltage droop controller. LPF: first-order low pass filter

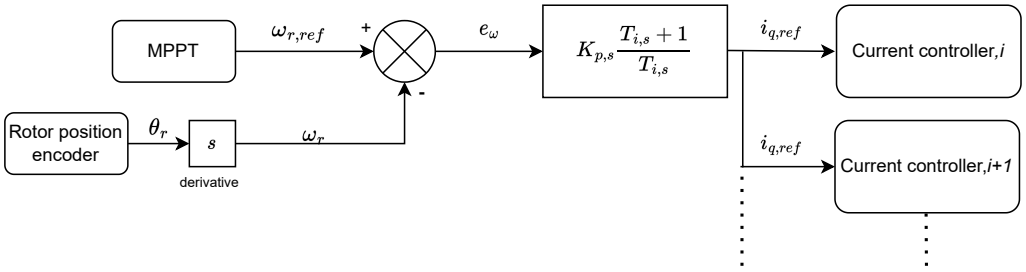


Figure 17: Direct speed controller

3.6 Direct speed control*

The direct speed controller is implemented as illustrated in Figure 17. The q-axis current output is common for all N modules.

A speed reference filter is implemented in the simulation model in order to reduce abrupt changes in the torque (q-axis current) as a consequence of wind gusts. The tuning of the speed controller is done according to the symmetrical optimum criteria.

Because the turbine level control system is not the main focus of this thesis the tuning and frequency response of the speed controller is presented in Appendix A.2.

3.7 Maximum power point tracking*

In operational zone 2 the wind turbine attempts to extract the maximum possible power at below-rated wind speed. The method employed in this proposed system is that of tracking the optimal tip speed ratio at any given moment. Therefore MPPT sets the turbine speed reference based on (3.13).

$$\omega_T^{ref} = \frac{V_w \lambda_{opt}(\beta)}{R} \tag{3.13}$$

In the wind turbine model used for the complete control system simulation model $\beta = 0$ yields the highest power factor from the turbine. Therefore β is set equal to zero and turbine speed is controlled such that the tip speed ratio (λ) is equal to $\lambda_{optimal}$. Because the pitch angle β is constant, $\lambda_{optimal}$ is also constant and equal to 8.1.

3.8 Pitch controller*

A basic pitch controller was implemented as a secondary speed controller. Meaning that when the wind speed rises beyond the nominal wind speed, and the direct speed controller becomes saturated at the rated q-axis current (1pu), the pitch controller is activated and controls the pitch angle of the blade such that the speed of the turbine remains at the nominal speed. It is more conventional to implement the pitch controller as a power controller, which sets the adjusts the pitch according to a power reference[30]. However, because pitch control is not the focus of this thesis the control method that seemed most convenient at the time was selected. The implemented pitch controllers' performance in an actual system would be questionable, but it performs just well enough to illustrate the concept of the control system operation in zone 4 (over nominal wind speed). The pitch controller implementation is presented in Appendix A.3.

4 Simulation of the complete control system for a two-module implementation of the ModHVDC concept*

The following results were obtained in the corresponding specialization project and is therefore not credited to this thesis work. The results are included for comparison with lab results and to provide context to the experimental verification in Section 5.[1].

The complete control system simulation model was developed as a two-module system in Simulink. All the controllers presented in Section 3 are included in the model, and the generator dynamics are modeled by the PMSG differential equations presented in Section 2.2. The simulation model used to obtain the results presented in the following sections is heavily inspired by the simulation model developed by Faraasen in [4].

4.1 System operation in all normal zones of operation.*

In this section, the complete control system is analyzed during normal operation in different wind turbine operational zones. The operational zones are outlined in Section 2.6. The system is operating with turbine-level speed and pitch control as well as module-level voltage, current, and droop control. "Maximum torque per amp" is employed as the current control strategy.

Figure 18 illustrates the system operation from zone 2 (below nominal wind -and turbine speed) to zone 4 operation (above-rated wind speed) and back down to zone 2. In zone 2 the turbine speed is set by the MPPT. As the wind speed reaches the rated wind speed of 12 m/s, the turbine enters zone 3 (rated wind speed, but below-rated load) for a very brief period of time. The electrical torque reference quickly reaches 1pu which is the saturation level. The pitch controller is observed to effectively control the turbine speed back to nominal after the wind speed increases to 14 m/s (Zone 4). It is observed that the "maximum torque per amp" strategy is enforced throughout the full operation of the wind turbine. I.e the d-axis current is effectively controlled to approximately zero pu. The modules are set to be completely identical in the simulation corresponding to Figure 18. Meaning that no voltage balancing was needed and the q-axis current reference was identical for both modules. Hence only the current from one module is presented.

A reference filter on the turbine speed input was included in order to avoid abrupt changes in the q-axis current reference. Sudden changes in electrical torque should generally be avoided in order to reduce stress on the mechanical system.

4.2 Voltage balancing control*

In this section, the results of introducing the DC bus voltage balancing algorithm are presented. The resulting system behavior for all three voltage balancing strategies outlined in Section 3.4 are presented.

Stator segment imbalance is modeled by a 5% reduction in flux linkage in module 1. In the simulations presented in the following subsections, the turbine is operated at nominal speed and power (Zone 4).

4.2.1 Weakest link strategy

Simulation results from this strategy are displayed in Figure 19. By enforcing an absolute q-axis current limit of 1pu, the power of module 2 is forced to comply with the reduced power level of the deviating module 1. This is because in order to maintain effective voltage balancing the limitation must be set on the common q-axis reference from the speed controller. In Figure 19 it is observed that when DC bus voltage balancing is activated the q-axis current and subsequent DC-power of module 2 decreases. The power decreases until it is equal to the power of module 1, resulting in

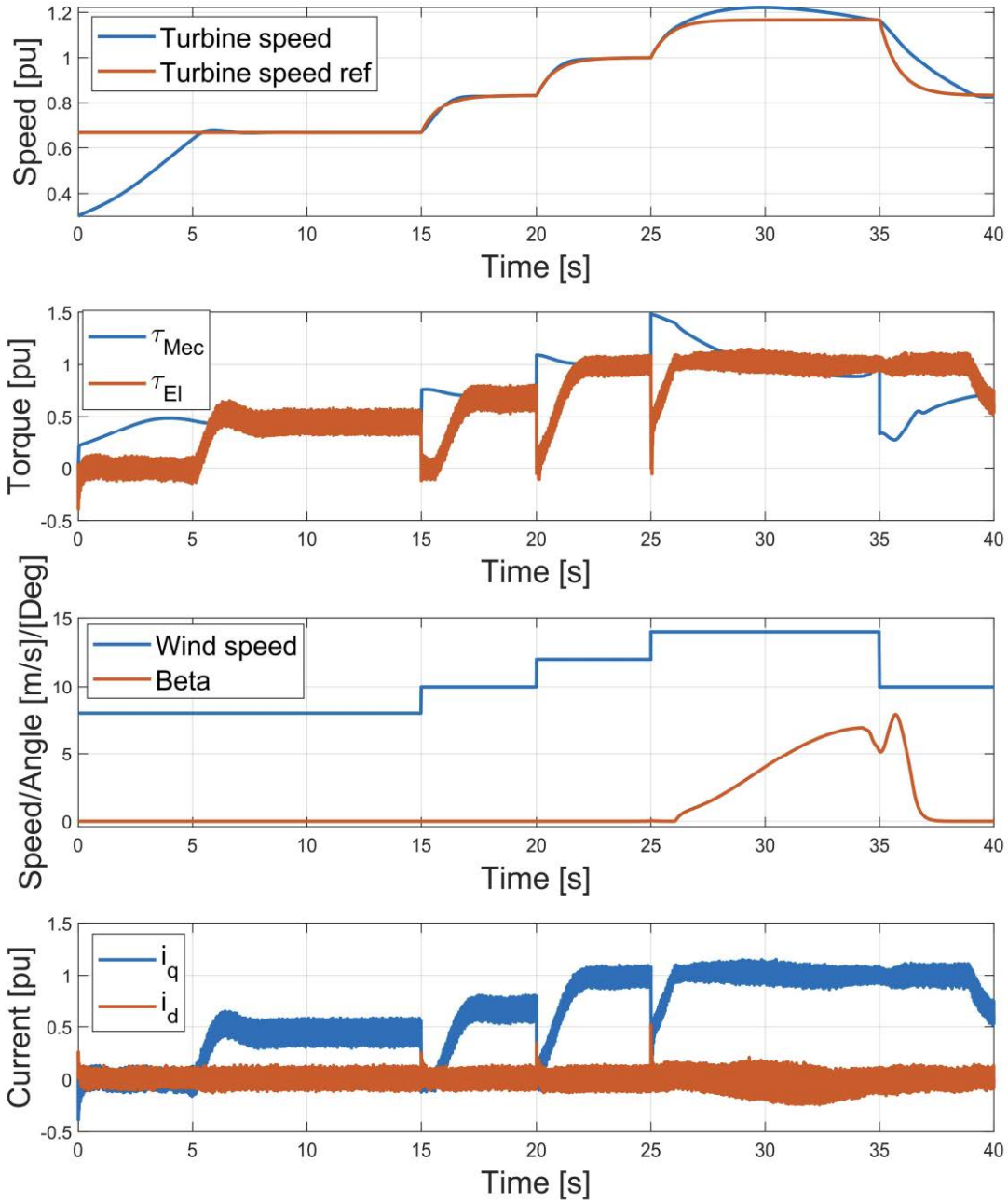


Figure 18: System operation in zone 2, 3 and 4. With speed reference filter

a derating of the total DC link power equal in percentage to the reduction in the single deviating module.

In this case with a reduced flux linkage of 5% in one module, the resulting total power reduction is approximately 110kW for the two-segment system ($\approx$ 5% reduction). A substantial amount that would reduce the profitability of the concept as a whole.

4.2.2 Split the difference strategy

By allowing the balancing current to be controlled freely by the voltage balancing controller the modules will meet in the middle due to an equal control response of the modules. The total DC power will therefore end up being slightly below the nominal level. As shown in Figure 20

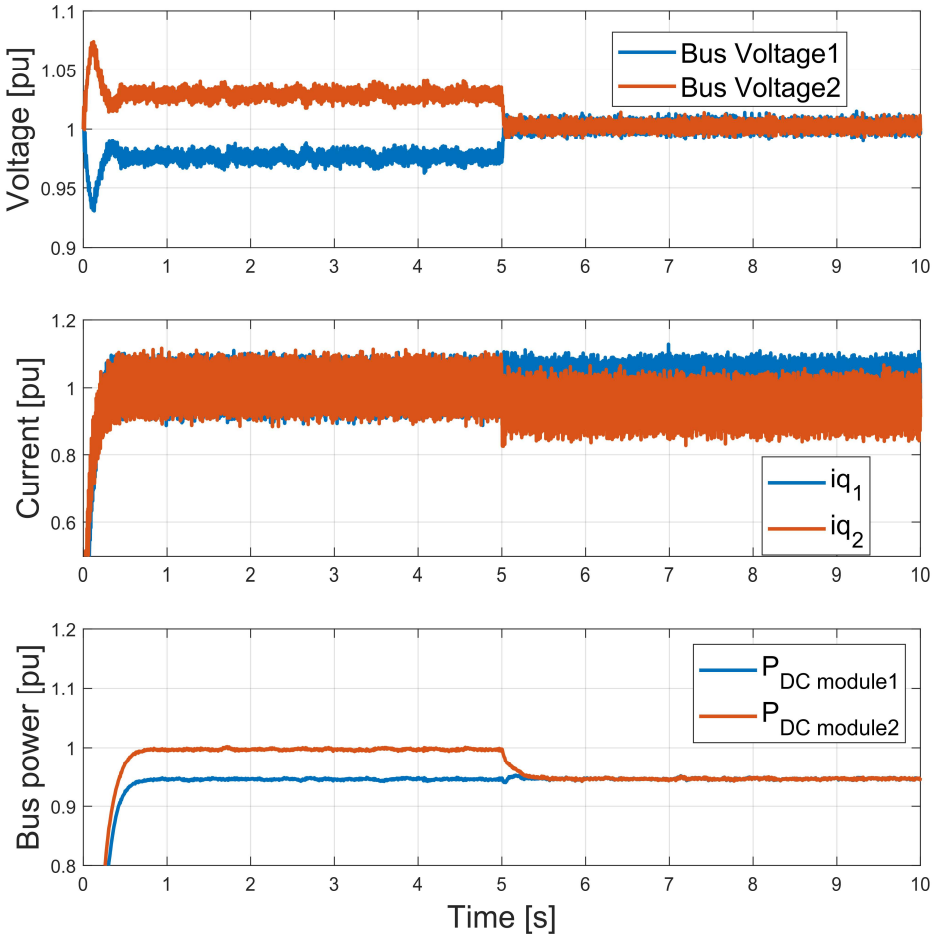


Figure 19: DC voltage balancing, with the "weakest link" strategy employed. Voltage balancing activates at t=5s

4.2.3 Lift to nominal power strategy

The final strategy limits the balancing current output from below such that the balancing current output must be greater or equal to zero. The result is that the module segment with lower than rated power output increases its DC bus power until it equals to the other normal module. As can be seen from Figure 21.

It is clear from the corresponding plots that both the "meet in the middle" and "Lift to nominal" control strategy requires the AC side to be overrated in terms of AC current. Because the current in module 1 has to increase above 1pu in order to meet the reference set by the speed and voltage balancing controllers simultaneously. The "lift to nominal" strategy requires a higher overrating of the system but in return offers the possibility to operate the entire turbine at nominal power even with substantial parameter deviations between the module and/or stator segments.

4.2.4 Brief discussion on the obtained results from the complete control system simulations.

The results presented in this section of the thesis serve the purpose of demonstrating how the turbine-level and module-level control system operates in the context of a system that models both the physical dynamics of a PMSG and a wind turbine. The dynamics of the model are based on the differential equations presented in Section 2.2 and with the circuit parameters presented in Appendix A.4. The system parameters used are based on [5] and the model developed by [4].

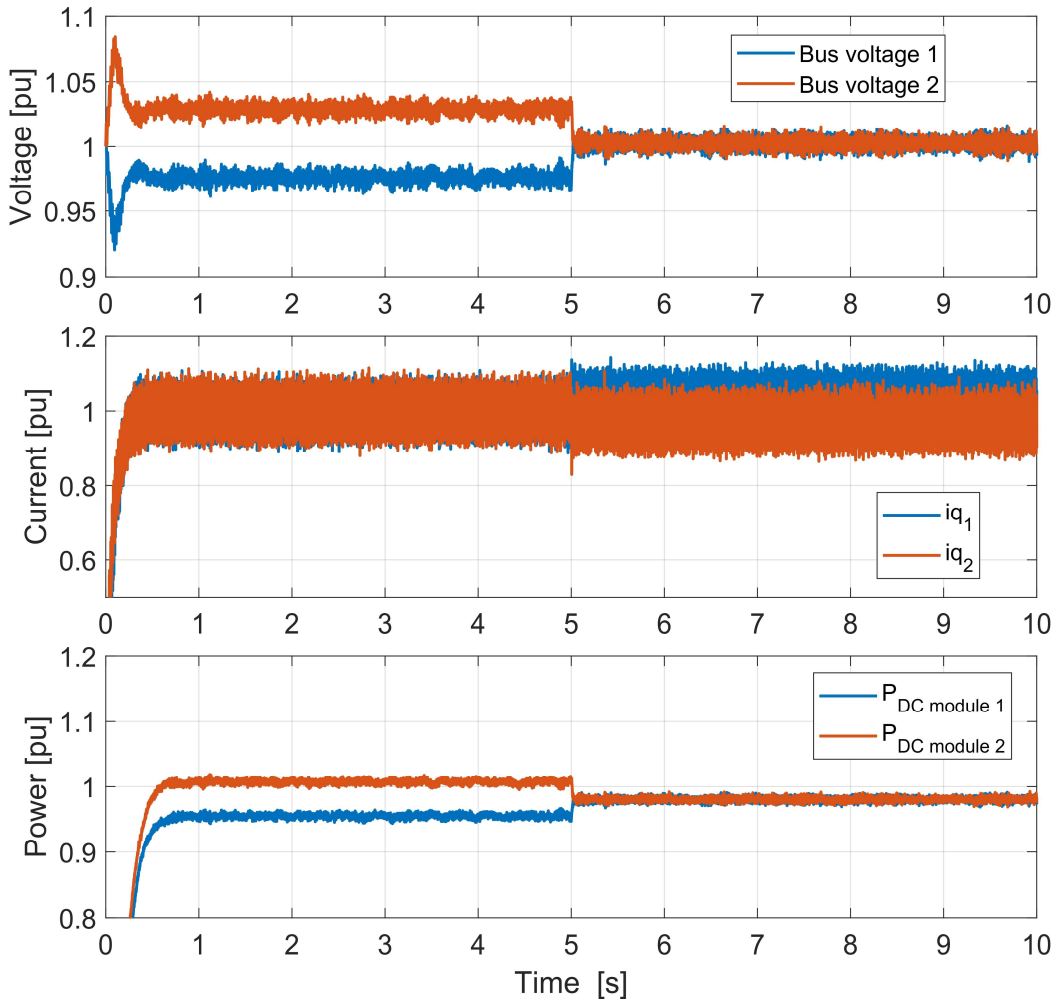


Figure 20: DC voltage balancing, with "split the difference" strategy employed. Voltage balancing activates at t=5s

A considerable amount of noise is visible on the measured AC current and DC voltage. A filter is used before passing the dq0 current to the current controllers to avoid the noise propagating throughout the control system. However, the dq-current and DC voltage waveforms displayed in the plots are unfiltered. The DC power displayed in the plots is filtered with a time constant of 0.1s. This large filtering constant is used to more clearly illustrate the change in mean DC power due to voltage balancing. Generally, the complete control system simulation model is considered to model the actual system well enough to illustrate the dynamics of the voltage balancing and resulting system power. However, further work should be done to ensure the model's realism. The amount of noise on the AC side current appears unrealistically high. The noise primarily results from the PWM converter side voltage being used to calculate the resulting AC side current without any filtering, which might be unrealistic.

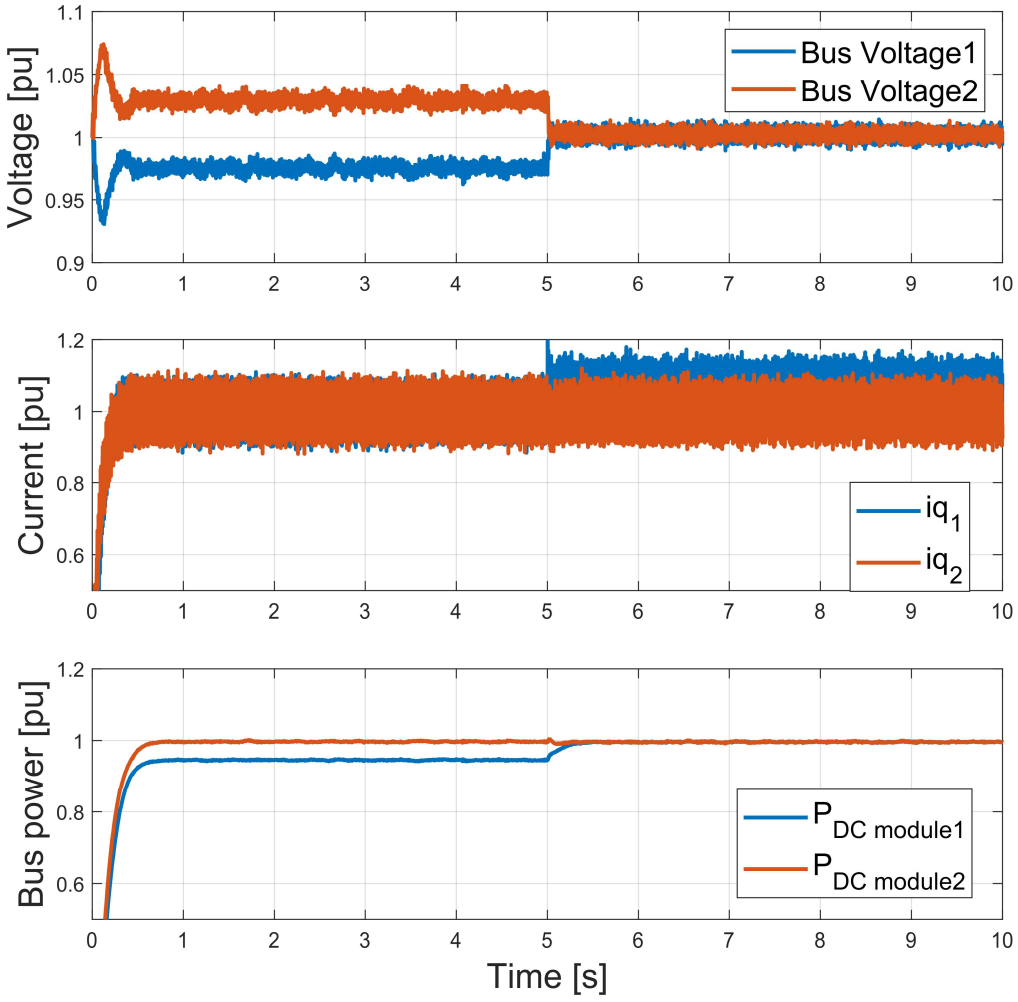


Figure 21: DC voltage balancing, with "lift to nominal power" strategy employed. Voltage balancing activates at t=5s

5 Experimental Verification

5.1 Introduction

The experimental work done in this thesis consists of developing and testing a small-scale low-power implementation of the two-module, which emulates the large-scale ModHVDC system described and simulated in Section 4. The setup has been developed incrementally, meaning that the functionality of the components used and the embedded system executing the control algorithms have been developed and tested in stages before moving on to the final setup[10]. A conceptual drawing of the final setup is displayed in Figure 22. The components of this schematic will be explained in their respective sections.

5.1.1 Experimental testing objectives

The main objectives of the laboratory experimental testing are the following:

- Verify the accurate reference tracking by the current controller and voltage balancing algorithms presented in [5] and simulated in Section 4 on a small-scale physical lab system.
- Verify the feasibility of the proposed voltage balancing strategies outlined in Section 3.2 from a control perspective on a physical system.
- Establish a functioning small-scale laboratory implementation of the ModHVDC concept, which will be expanded upon and serve as a foundation for future research.

5.1.2 Overview of the stages of development

The stages of development have been the following:

1. **Inverter mode**. A single VSC-board operated with current control in inverter mode. Connected to a DC source and a three-phase resistive load.
2. **Rectifier mode -Resistive load**. A single VSC-board operated with current control in rectifier mode. Connected to a three-phase transformer and a resistive load on the DC side.
3. **Rectifier mode - DC link**. A single VSC-board operated with current control in rectifier mode. Connected to a three-phase transformer and a bi-directional DC source serving as a fixed-voltage DC-link.
4. **Rectifier mode - DC link- Two modules**. Two VSC boards operated with current control and voltage balancing in rectifier mode. Connected to two separate three-phase transformers and a bi-directional DC source serving as a fixed-voltage DC-link.

Regarding documentation of preliminary testing stages.
The method description and results for the preliminary testing stages (stage 1-2) are presented concisely. These stages are primarily aimed at validating the anticipated operation of the equipment and control algorithms employed before moving on to the final setup. Documentation of the preliminary testing stages is included for the completeness of the method section and to reinforce the final results. However, the method and results from certain stages, such as "VSC in rectifier mode powering a DC-load," is omitted because it largely overlaps with rectifier operation with a fixed DC-link in terms of results and implementation. Results and implementation of the VSC in inverter mode are included because implementing a back-to-back VSCs configuration is an option

[10]The final laboratory setup used for testing in this thesis does not represent the ultimate stage of the overall laboratory setup. The ambition was to have at least three modules in series with split DC capacitors to access DC neutral points. However, due to time limitations, pursuing this development level in the scope of this thesis work was impossible.

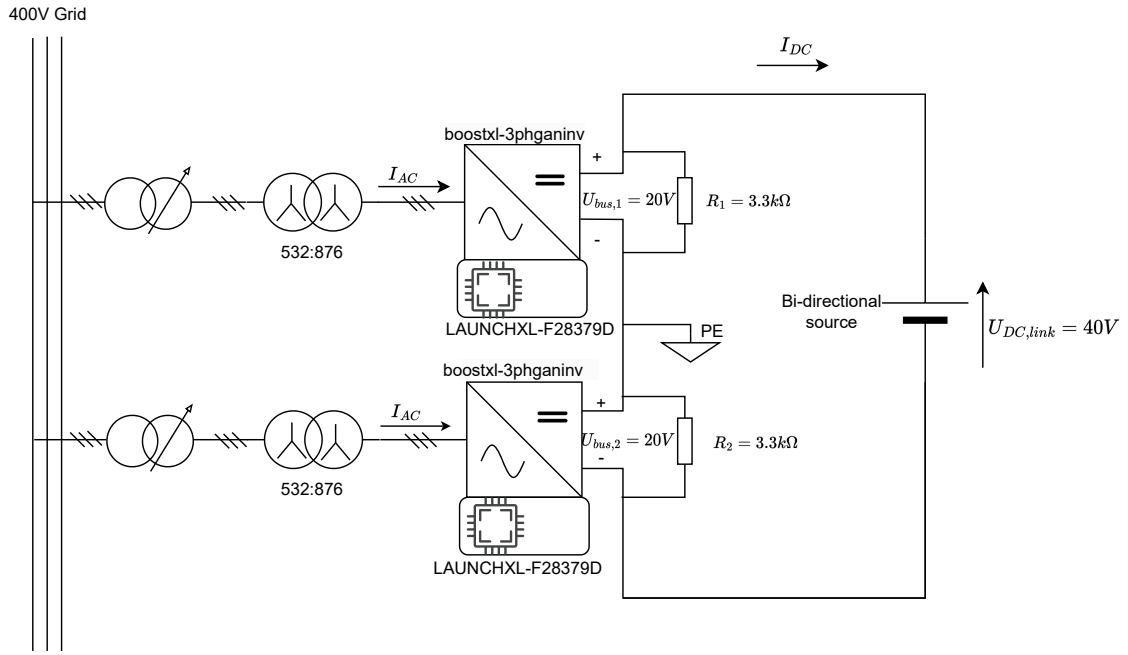


Figure 22: Principle drawing of two-module laboratory setup

for further development beyond this thesis to replace the bi-directional DC source. Hence, verifying inverter mode operation is considered relevant.

For ease of reading, the method and results from each development stage will be presented and discussed together in an individual section before moving on to the next stage of development. Lastly, a comprehensive discussion of the experimental testing as a whole is presented.

5.1.3 Simulation of the laboratory setup

Parallel to the development of the lab, simulations of the lab setup have been conducted in Simulink. The simulation models have been made to replicate the physical lab setup as closely as possible to have comparable results from the simulations and laboratory measurements. Showing good correspondence between the observations made in the lab and the simulation results lends confidence to the lab's implementation and intended function. Which in turn bolsters the simulation models' validity. The simulation results from each stage of development are presented together with the lab results in their respective sections.

5.2 Conceptual comparison laboratory setup and ModHVDC system

The experimental lab setup attempts to emulate the ModHVDC system as closely as possible. However, since this experimental setup is at an early stage of development, notable disparities exist between the laboratory implementation detailed in this thesis and the proposed ModHVDC system. These disparities are outlined in this subsection and are discussed in more detail later in the respective method section.

Figure 23 shows a schematic illustrating a single-module configuration of the lab implementation and, equivalently, one module of the proposed ModHVDC system. As is evident from this illustration, the induced voltage in the generator windings is emulated by the output voltage of the variable AC grid-connected transformer. The isolation transformer's impedance emulates the stator coils' impedance, and a bi-directional DC source emulates the HVDC link.

The main differences that are consequential for the control system implementation are the generation of the phase angle reference θ. And the relation between the magnitude and phase angle of

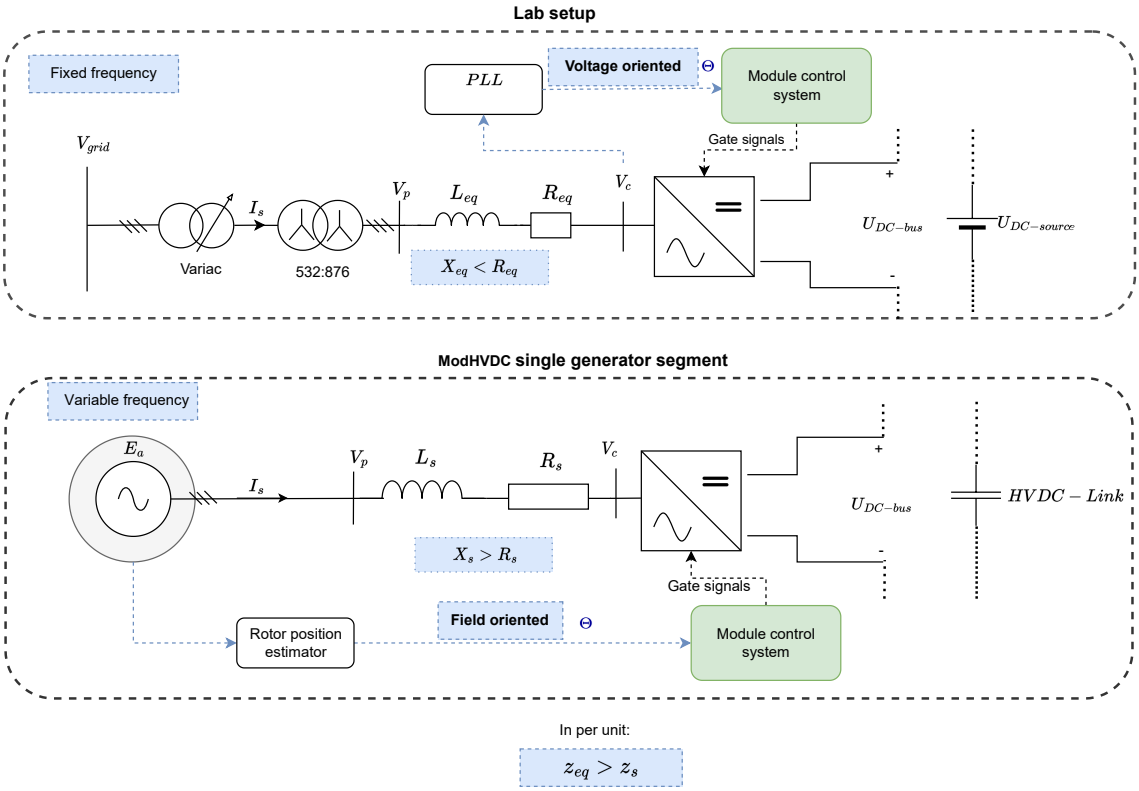


Figure 23: Schematic of a single module in the context of a multi-module system, highlighting (in blue) the two most consequential differences between the lab implementation(top) and the system concept being emulated (bottom). L_{eq} and R_{eq} are the equivalent resistance and inductance of the circuit referred to the secondary side of the isolation transformer. L_s and R_s represent the generator stator impedance.

the impedance in the generator versus the transformers used in the lab.

The phase angle reference is generated based on the rotor field in a convectional FOC drive system. The rotor position is often estimated based on measurements of the flux. A field-oriented phase angle reference means that in the dq0-plane, the q-axis corresponds to active power, and the d-axis to reactive because E_a lags the rotor field by 90 degrees. In the lab implementation, the phase angle reference is generated by a PLL based on the voltage measurements at the converter. Firstly this means that the d-axis corresponds to active power because θ is aligned with phase A of the three-phase voltage. This is, however, of little consequence because d -and q-axis current control is implemented the same way. Therefore, the only difference in the control system implementation is that the d and q axis references must be swapped relative to the implementation presented in Section 3.2. Using the converter voltage V_c for the PLL is, on the other hand, more unconventional and has some implications for the "minimum stator current control" strategy, which was employed in Section 4. This is explained in more detail in section Section 5.6.2 where the implementation of the PLL is outlined. Nevertheless, the current controller itself is not changed because it is the relative magnitude and phase shift between V_c, V_p, and subsequently I_s, which determines the power flow in the circuit. The effectiveness of a PLL with a PWM-voltage input is also discussed in Section 5.5.2.

The second significant difference is the magnitude of the resistance in the transformer, which emulates the generator's stator. In a commercial high-voltage generator, the stator impedance is dominated by the reactance because stator resistance is kept at a minimum to reduce losses. In the simulation model employed in Section 4, the stator resistance constituted about 5% of the total stator impedance. While in the three-phase transformer, which emulates the stator, the

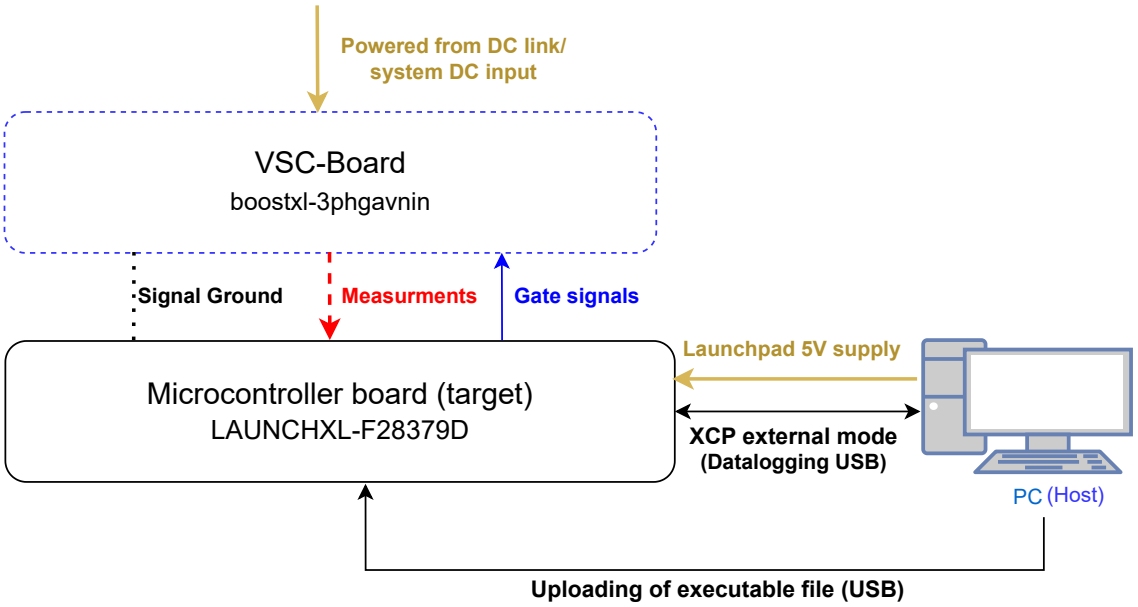


Figure 24: Illustration of the flow of information (data) in the embedded system and the power supply for the microcontroller and VSC -board.

coil resistance is so significant that it dominates impedance. This becomes a problem due to the maximum power transfer theorem. This phenomenon is detailed in Section 5.6. However, as long as the current is kept below a certain threshold, the large transformer resistance does not seem to cause any issues for the control system.

The outlined differences between the physical lab setup and the ModHVDC system are mainly due to limitations in available equipment and time for development. And since the consequences seem to be non-critical in regards to the control system, the discrepancies are not considered to significantly affect the validity of the experimental results for investigating the research objectives. Therefore, meeting the presented goals for the experimental verification section is possible with the proposed laboratory setup.

5.3 Embedded system programming

5.3.1 Embedded real-time system

The laboratory setup consists of an electrical power circuit that is controlled by an embedded system operating in real time[11]. The embedded system is implemented using microcontroller boards from Texas Instruments (Launchxl-F28379D), often referred to as "Launchpads". The microcontrollers are responsible for executing the control algorithms, software triggers, activation logic, etc. This functionality is implemented in the microcontroller through the following sequence of actions. A program specifying the microcontroller's tasks and functionality is made on the host computer. Then this program is compiled to C-code and uploaded as an executable file to the microcontroller's flash memory[12] from the host PC. The microcontroller then runs the executable and performs the programmed tasks in real-time. At its core, the microcontroller's only job is to control the MOSFETS (switches) on the VSC-boards by generating gate signals. The measurements from the VSC board are inputted to the microcontroller and used in the control algorithm through analog-to-digital conversion (ADC). The ADC is also governed by the program uploaded to the microcontroller from the host PC. The data flow in the embedded system, as well as the power supplied to the microcontroller and VSC-board is illustrated in Figure 24

[11]The system does not fulfill the criteria for a hard real-time embedded system

[12]Alternatively, the embedded program can be uploaded to the RAM, but the flash memory was mainly used in this lab implementation.

In this thesis, the programming was done in Simulink. The following Add-ons were used for interfacing with the Texas Instruments C2000 hardware and for implementing PWM, ADC, and software triggers in the Simulink model: "SoC Blockset Support Package for Texas Instruments C2000 Processors", "Motor Control Blockset", "Embedded Coder Support Package for Texas Instruments C2000 Processors", as well as the Matlab - Simulink -and embedded-coder. Once the Simulink program is developed, it is compiled into a Code Composer Studio (CCS) project. From there, it is uploaded and run on the microcontroller. The project files and headers can be viewed and debugged in CCS.

5.3.2 Logging with Simulink external mode

Simulink allows for the embedded system to run in what is called external mode. In external mode, a two-way communication link is established between the microcontroller (target) and the PC (host). The XCP protocol was used in this implementation (XCP on serial). In external mode, values can be uploaded live from the target to the host as data packets at the baud rate specified in the hardware settings in Simulink. The host can also send commands and alter system parameters in real-time [31]. Logging through external mode has been the primary method for logging system data in the lab implementation because any input value or internally generated value can be logged and analyzed. In the early stages of the lab development, the baud rate was set to 5Mbit/s, and too many values were logged simultaneously. This leads to the amount of data being transmitted exceeding the baud rate. Therefore, some data points are dropped in transmission. Resulting in low resolution on the logged signals. In the final lab implementation, the baudrate was set to 12Mbit/s, and fewer signals where logged simultaneously, resulting in higher resolution on the logged data.

5.4 Inverter mode. Single module

In this section the setup, control implementation and results from inverter mode operation testing with the microcontroller and inverter board. This was chosen as a starting point for the preliminary testing

5.4.1 Laboratory test setup

Inverter mode operation of the boostxl-3phgavnin board was implemented and tested using the setup illustrated in Figure 26. In inverter-operation, power is transferred from a DC supply to an AC load. In the case of this setup, a unidirectional DC-voltage supply was used as the power source. Switching pulses for the MOSFETS are generated through PWM, which in turn creates an AC output voltage over the three-phase resistive load. The three-phase load consists of three separate star-connected variable resistances. The gate signals are generated based on the reference voltage set by the current controller.
The neutral point of the star-connected load is floating. However, a large ohmic resistance connects the neutral point to the power ground to reduce low-power noise on the neutral point. The neutral point cannot be grounded directly because the AC voltages over the symmetric load are not perfect three-phase sine waves but rather pulse-width modulated square waves. This results in a pulsed alternating potential on the neutral point as shown in Figure 27. The presence of this neutral point voltage is confirmed through simulations of the lab setup.

5.4.2 Control implementation

Current control was implemented with PI controllers in the dq0-plane. Contrary to rectifier operation, when operating as an inverter AC voltage and AC current are proportional. This is intuitive when considering that the AC current is in this case purely dictated by the AC voltage over the load resistance. The current control is hence implemented as described in Equation 5.1. D and q-axis control is implemented identically. No feedforward terms are included.

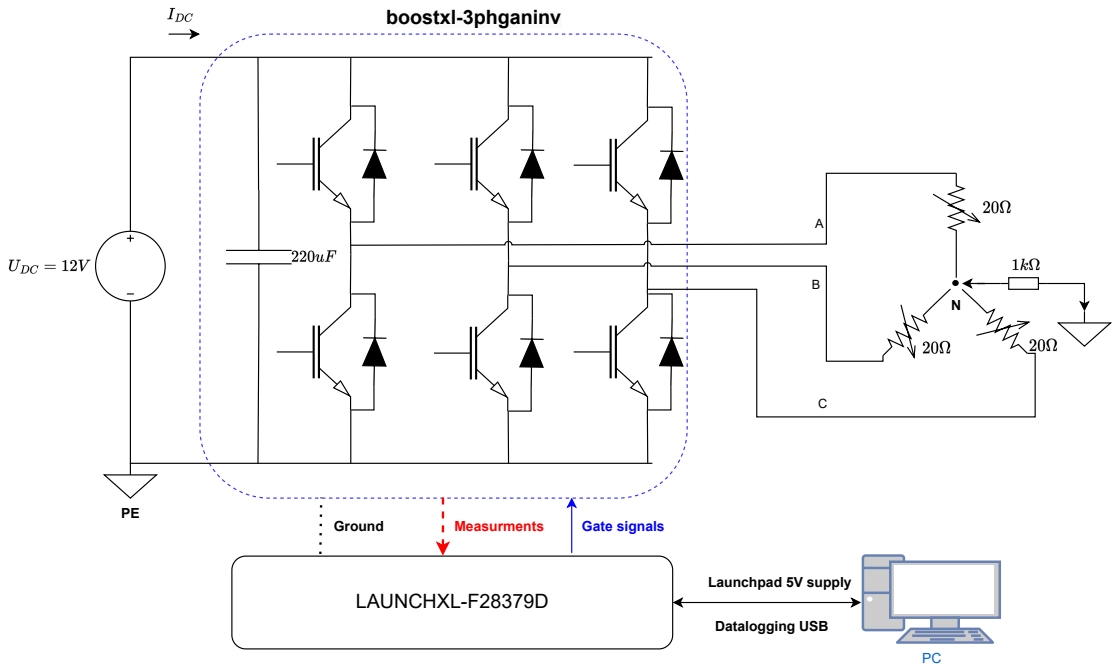


Figure 25: Illustration of three-phase VSC board inverter operation setup.

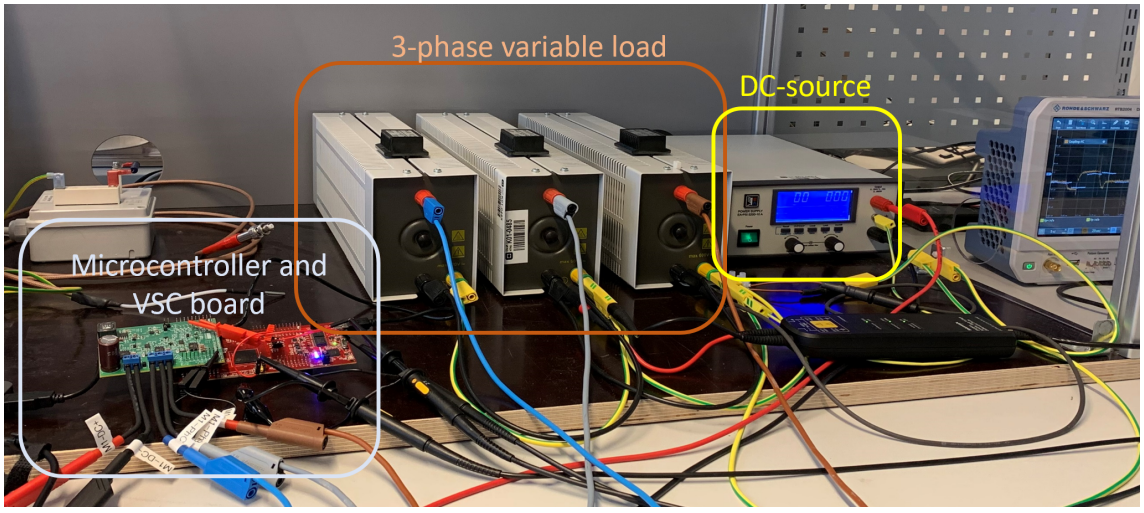


Figure 26: Three-phase VSC board inverter operation setup. Picture from the lab.

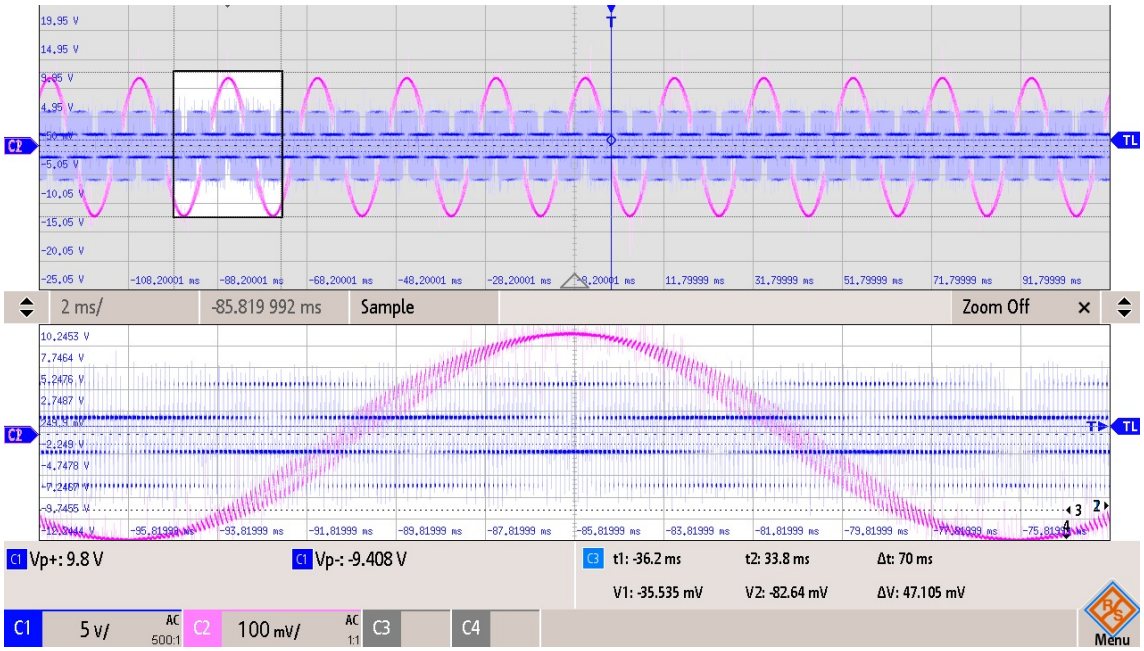


Figure 27: Neutral point to ground voltage -Blue. Filtered A-phase voltage measured from DAC pin on the microcontroller board -Pink.

$$V_{d,ref} = K_p \cdot e_{Id}(t) + K_i \cdot \int_0^t e_{Id}(t)\, dt \tag{5.1}$$

Time domain equation for the PI-controller, where Kp is the proportional gain, Ki is the integral time constant times Kp, and e_{Id} is the d-axis current reference minus the measured d-axis current.

Since there are almost no reactive elements in the system circuit, the dynamics of the system are simple. Therefore no feedforward compensation is included and tuning is selected based on experience and trial and error. The purpose of this testing stage is to verify the VSC-boards and microcontrollers functionality. Hence tuning and performance is not of interest. The controllers' proportional and integral gain is selected as $K_p = 2$ $K_i = 20$.

5.4.3 Dq0 transformation and phase angle reference

Because there is no rotating machine or AC-grid in this setup the reference phase angle can be generated freely. In this implementation, it is generated from a code block that outputs a linearly increasing reference wrapped between 0 and 2π with a period of 20ms (50Hz). This phase angle is used to transform the d-and q-axis voltage references outputted from the current controller into a three-phase sinusoidal reference which in turn generates the gate pulses transferred from the microcontroller to the inverter board.

5.4.4 Initialization

It was considered undesirable to initiate the current controller at zero voltage and current. Therefore a constant three-phase voltage waveform was given as a reference to the PWM at start-up. This ensured a constant AC current and voltage before the current control was initiated at t=20 seconds. At this point, the phase angle reference was initiated to match the exact point at which the constant voltage reference was at the previous time step. This was achieved through a PLL following the constant voltage reference waveform. To avoid a large transient the integral terms of the d -and q-axis current controllers were initiated at values approximately equal to the measured d-and q-axis voltages at the time instants before control activation.

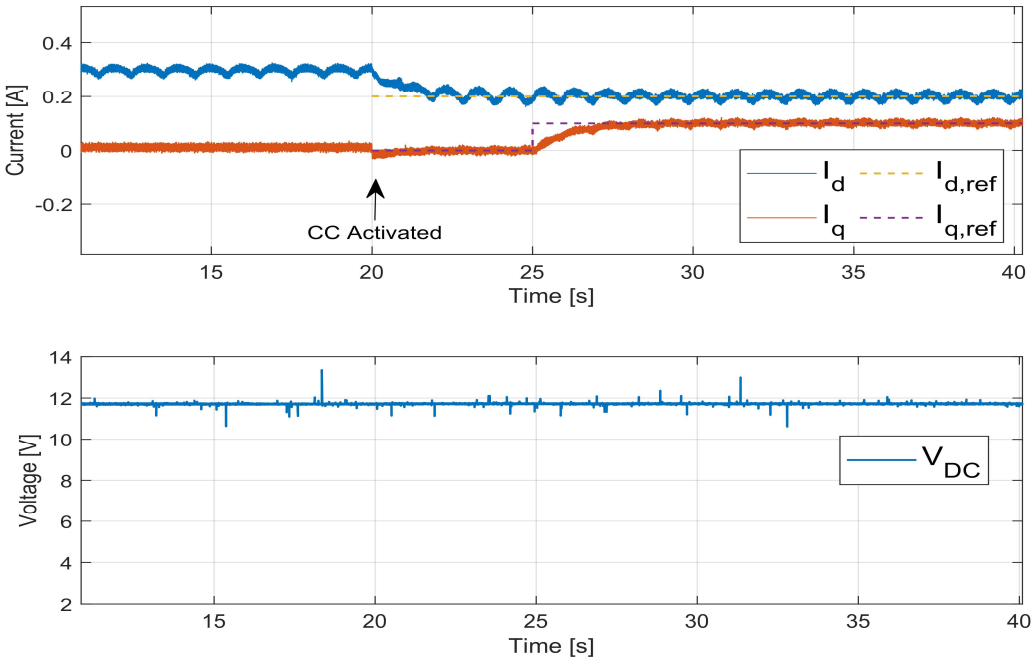


Figure 28: D- and q-axis current being controlled to the predetermined references of 0.2A and 0.1A respectively. DC voltage is supplied from a DC-voltage source and maintains constant throughout.

5.4.5 Results from inverter mode testing

Current control of both d and q-axis current was demonstrated, as shown in Figure 28. Several reference values were tested and the AC current was controllable within the range of what is physically possible with 12V DC and 20Ω per phase resistance.

Phase shift
In the inverter mode implementation, the reference phase angle (Theta) is generated as a constant 50Hz reference, independent of the measured voltage and current. This allows the q-axis component of the current to be controlled regardless of the even though there is negligible reactance in the AC circuit. In order to meet the current reference values the current controller shifts the generated AC voltage and, consequently, the AC current, relative to theta. Mathematically this results in a q-axis component in the dq0 plane. However voltage and current are still in phase with each other. Therefore no additional reactive power is produced even though the q-axis is normally correlated with reactive power in for instance grid-connected VSC. As explained in Section 2.2.2. The shift between voltage, current, and theta as well as a comparison of the lab simulation and actual lab measurements are shown in Figure 29. At the instance the oscillograms were captured in Figure 29 Iq was maintained at a relatively low value compared to Id resulting in a small phase shift between voltage and the reference phase angle (theta).

Compliance with simulation
Verifying correspondence between lab results and the simulations of the lab strengthens the credibility of the lab results and in turn, bolsters the trustworthiness of the simulation model. Comparisons of the simulation results and the logged values from the microcontroller and external measurements showed clear compliance. At this stage in the lab development, the correspondence between simulations is expected since the system consists of a few components and most physical quantities are known with a fair degree of accuracy. Apart from the fact that the simulations are in line with expectations, further results regarding controller performance at this stage hold limited significance to the goals of this thesis. Therefore no further simulation results are presented from this part of the lab development.

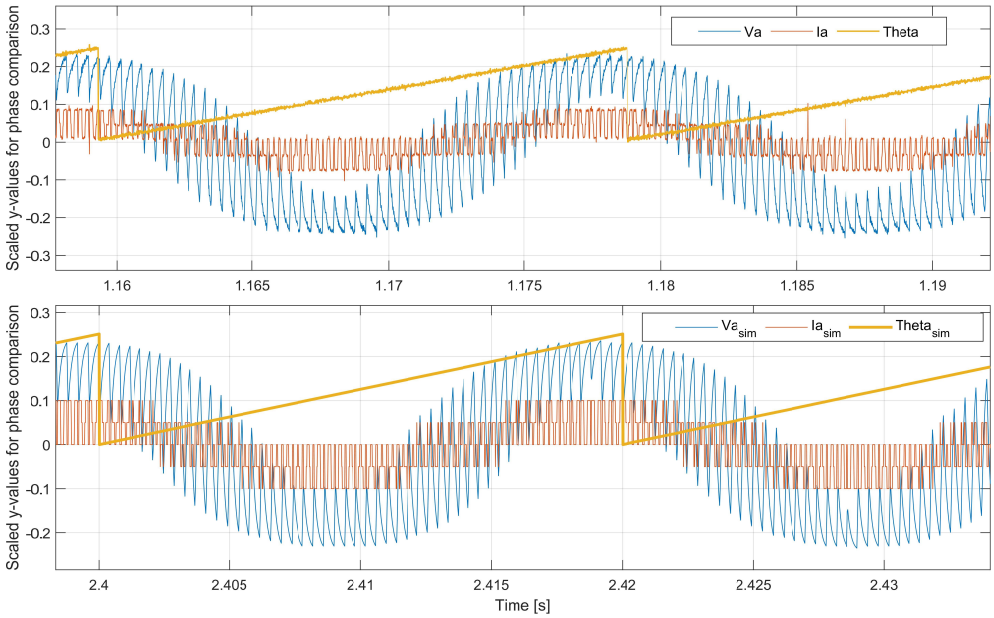


Figure 29: **Top:** Oscillogram recorded to CSV-file and plotted in Matlab. Va and Ia recorded from probing the measurement output pins on the inverter board. Theta was recorded from DAC-pin on Launchpad. **Bottom** Simulation result from simulation of the inverter lab setup. Va was measured through a voltage divider and RC-filter circuit that matches the physical one in the inverter board.

5.5 Single VSC with fixed DC link

In this testing stage, current control in rectifier mode is implemented while a bi-directional DC source keeps the DC link voltage at a fixed level. The general current control system is described in Section 3.2, but some necessary modifications have been made and are described in Section 5.5.3. The single module setup is illustrated in Figure 30 and depicted in Figure 31.

Single-module current control is at the core of the complete multi-modular control system for the ModHVDC concept. Therefore, much emphasis is put on this lab testing stage. The subsections of this chapter are structured as follows. Firstly, the necessary details regarding the lab implementation and corresponding control algorithms and embedded code are presented. Secondly, the relevant results are presented and briefly discussed. The results presented in this section form the basis for the implementation and larger discussion on the two-module final setup.

5.5.1 System impedance estimation

A reasonable estimate of the reactance and resistance in the laboratory setup is helpful for tuning the current controller and developing an accurate simulation model of the system. However, not all system impedances are easy to estimate or given in the respective datasheets of the equipment used. Therefore, some educated guesswork has been employed when setting the impedance values used in the simulations.

The estimated values used in the lab simulation are presented in Table 3. The resistance of the isolation transformer coils was measured with a multimeter. Due to the impedance values not being listed in the datasheet, a short circuit test was performed to determine the transformer reactance. However, it was not possible to make an accurate estimate based on the results from the SC test because the phase shift between the phase voltage and current was smaller than the given range of phase-shift error introduced by the clamp meter used to measure the current waveform. The negligible phase shift observed in the short circuit test is due to the inductance being small relative to the large resistance in the transformer coils. However, it seemed unlikely that a transformer with over 500 turns should have negligible reactance. Therefore, it was concluded that the transformer

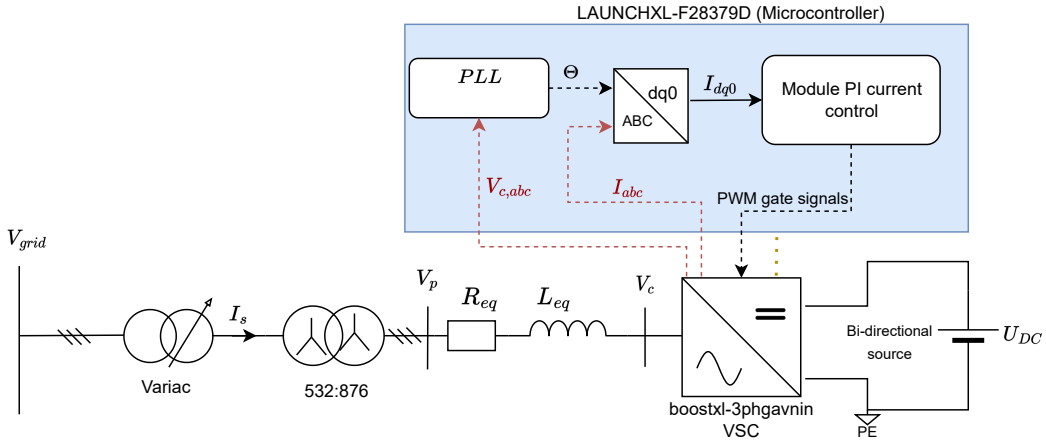
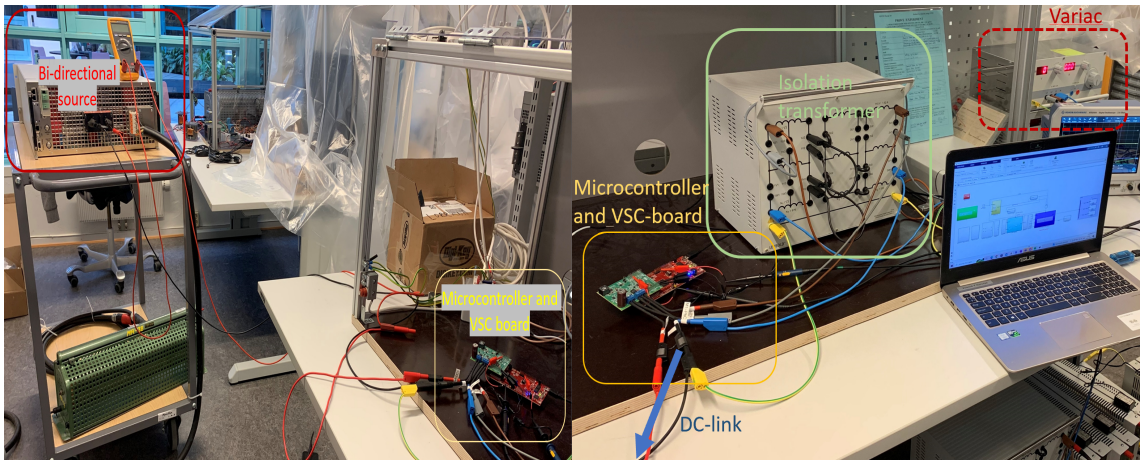


Figure 30: Concept schematic of the "single module with fixed DC voltage" implementation. L_{eq} and R_{eq} represent the equivalent impedance of the circuit including the variac referred to the converter side. V_p is a fictitious voltage that represents the emf from a generator. Red dotted lines illustrate measurements from the VSC board inputted to the embedded control system via ADC.



(a) DC side. (b) AC side.

Figure 31: Pictures of the laboratory setup with a single module operating as a rectifier. The lab setup has power flow from the right to the left and is therefore mirrored in relation to the schematic.

reactance was somewhere in the range of 15% of the resistance at 50Hz. Translating to a per-phase inductance of 3mH on the primary, which is the coil with the most turns, and 2mH on the secondary. Results from the short circuit test is shown in Appendix Section B.2.

The impedance of the variac was not found in any datasheet and is difficult to measure. Therefore, the variac impedance has been set based on reasonable guesses and fair correspondence between simulation results and observations in the lab. The variac has 400 turns on the primary and the secondary is adjusted based on the desired output voltage. The Variac is assumed to have more inductance and less resistance than the isolation transformer.

$R_{t,p}$	3.0 Ohm
$R_{t,s}$	3.7 Ohm
$L_{t,p}$	3.0mH
$L_{t,s}$	2.0mH
$R_{v,p}$	3.0 Ohm
$R_{v,s}$	2.0 Ohm
$L_{v,p}$	40mH
$L_{v,s}$	5.0mH
$R_{eq,c}$	5.5Ohm
$L_{eq,c}$	5.0mH

Table 3: Roughly estimated circuit impedance values. Used for simulation of the single and two-module setup. t denotes transformer, v-variac, p-primary, s-secondary. $R_{eq,c}$ and $L_{eq,c}$ are the total circuit impedance referred to the converter side (secondary of the isolation transformer).

The magnetizing impedance of the transformers is assumed to be large enough to be neglected in the modeling of the system behavior. The grid is assumed to be stiff.

5.5.2 Phase locked loop (PLL)

To transform three-phase signals to the dq0-plane, a phase angle reference (θ) is needed. In the inverter mode implementation, this reference could be generated arbitrarily because the VSC itself generated the AC voltage and did not need to match any existing voltage in terms of phase shift or frequency. In the full-scale ModHVDC concept field oriented control is used. Meaning the phase angle reference is aligned with the rotor magnetic field (d-axis). In this lab implementation, however, the AC generator segments are emulated by grid-connected transformers. Therefore θ has to be generated using a phase-locked loop (PLL) to provide the control system with accurate state variables in the dq0-plane. As well as to ensure the control system output in the abc-plane has the intended magnitude and phase shift relative to the output voltages from the variac.

The algorithm used for the PLL implementation is presented in Section 2.3.3.

PLL tuning
The tuning of the PID in the PLL implementation is taken directly from the default tuning used by Mathworks in their three-phase PLL Simulink block[32], and is presented in Table 4. Reducing the proportional gain was tested to give lower bandwidth and better gain margins however no stability issues were observed with the original tuning, and since a high bandwidth in the PLL is desirable to mitigate any potential coupling effects between the PLL and current control the original tuning was restored and yielded consistent and accurate phase tracking.

K_p	180
K_i	3200
K_d	1
N	100

Table 4: Tuning of the Phase locked loop. Where N is the derivative filter divisor for the derivative branch of the PID controller [33].

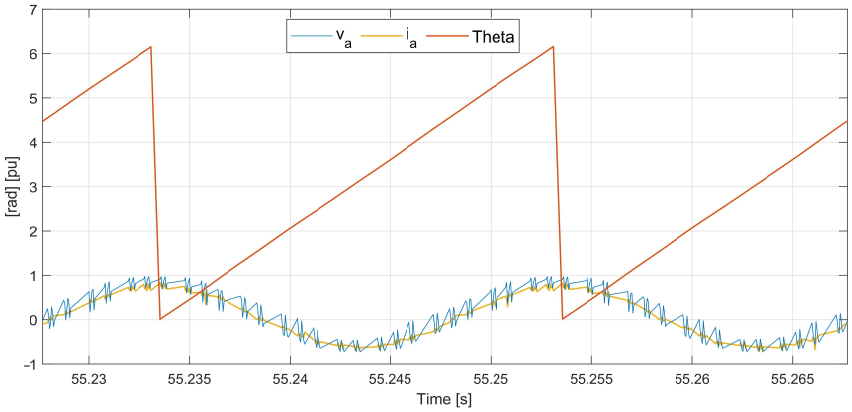


Figure 32: Phase angle output from PLL (Θ) given $V_{abc,c}$ as input, plotted against the measured AC voltage and current in the VSC-board (V_a and I_a) in per unit. i_d and i_q is being controlled to 0.8pu and 0.0pu respectively.

PLL input It is conventional for grid-connected VSCs to have a physical filter between the point of common coupling (PCC) and the VSC. The filter is often an LCL filter or just an L filter which is connected between the grid, or grid-connected transformer, and the VSC[34] [35]. In the lab implementation detailed in this thesis the inductance of the isolation transformer and the variac act as an L-filter between the grid voltage and the VSC.

Unconventionally the PLL generates θ based on the voltage measured at the converter terminals (V_c), as shown in Figure 30 In most implementations of a grid connected PLL-based VSC control, the three-phase measurement input to the PLL is taken from the capacitors on the LCL-filter, as in [5], or at the point of common coupling (PCC), as in [36]. Using V_c for the PLL poses some challenges. Firstly because the voltage is square wave PWM voltage waveforms when the converter is in operation. Which can make it difficult for the PLL to track the fundamental frequency component of the voltage. This issue is handled through filtering. The voltage measurement circuit on the VSC-board is implemented as a voltage divider with a passive low pass RC filter. The cutoff frequency is about 1kHz and the introduced phase shift on a 50Hz signal is calculated to be around 2.4 degrees. Having a phase shift in the voltage measurement provided to the PLL is not ideal, however it is deemed small enough to be acceptable for the intended purposes of this implementation.

Using the voltage V_c as the reference voltage has implications for the implementation of the current control strategies presented in Section 2.2.3. This will be shown and further discussed in the next subchapter.

PLL performance
The PLL successfully tracks the the phase angle of the input three-phase signal accuratly and precisely. No issues were observed in the lab or in simulation regarding the PLL tracking the phase inaccurately or loosing the reference during transients in the input voltage. A plot showing the phase angle output of the PLL against the measurd A-phase voltage and current is shown in Figure 32.

5.5.3 Current control implementation

In essence, the current control is implemented as described in Section 3.2. However, the feedforward compensations terms for the d and q-axis coupling are not included due to several factors. Firstly, the coupling effects in a PMSG and a transformer are not the same. Therefore, using the feed-forward compensation for the PMSG in the physical lab system will not necessarily have the desired effect because the system dynamics are different. Also several quantities are only roughly estimated in the physical laboratory setup, such as the transformer and variac reactance, and a feed forward term has to represent the actual coupling between the d -and q-axis in order to be effective.

Current control tuning
The tuning of the current controller was tuned based on trial and error. The modulus optimum method as used in Section 3.2.3, requires somewhat good estimates of the system impedance and the total delay in the control system loop. Since there are many uncertainties regarding these quantities in the physical lab setup tuning was done experimentally. Empirical tuning methods like Ziegler-Nichols [37] were considered, but pushing the system to the point of instability to find the tuning constants was not desirable.

The tuning constant used in the single and two-module implementation is presented in Table 5.

K_p	2
K_i	20

Table 5: Tuning of the current controller in the lab implementation.

In hindsight, this current controller tuning is quite aggressive in terms of proportional gain. This results in high bandwidth, but the stability margins might be below what is desirable. The tuning is considered aggressive because the estimated total reactance of the lab circuit is low relative to the resistance, which results in a significantly lower circuit time constant (L/R) than the time constant used to model the stator characteristics in the full-scale concept simulation. A smaller time constant means that the current changes faster in response to changes in the voltage which usually translates to a lower proportional gain in the controller. The total delay in the control loop is assumed to be in the same order of magnitude in the lab setup as in the full-scale simulation due to the same filtering time constant (2ms) being used for filtering d and q-axis current. The delay introduced by the converter on the other hand is smaller in the lab setup due to the switching frequency being 5kHz contrary to 1kHz which is used in the full-scale simulation. The sampling rate and ADC sigma-delta filtering also introduce a delay in the embedded system. However, the delay introduced by these is considered negligible in comparison to the larger filter delay.

A lower dominant system time constant and the same order of time delay in the controller loop should constitute a lower proportional gain (K_p) according to the equations describing the modulus optimum criteria outlined in Equation 2.10. However, since the integral time constant is lower the integral branch gain K_i should be greater. This would indicate that $K_p = 2$ is far too large of a proportional gain, but $K_i = 20$ is in the right order of magnitude. This could in theory lead to stability issues. However, no stability issues were observed, so the original tuning of $K_p = 2$ and $K_i = 20$ was used for both the single and two-module setup. Less aggressive tuning was tested as well with varying success. However, the estimated tuning constants based on the modulus optimum method were not tested on the lab system. The system step response with decreased controller proportional gains is presented in the appendix Section B.3.

5.5.4 Initialisation of the lab system for current control test.

In order to control when the current control (CC) algorithm was activated, several activation criteria was implemented in the Simulink embedded model. Unless these criteria were fulfilled all gate signal pins were forced to low. The trip zone functionality in the c2000-ePWM block was used to implement these software triggers. Forcing the gate signals to low opens the MOSFETs and disables operation. The trip zone logic was used to implement over-current and over-voltage triggers which would also disable operation. The activation criteria are set before the operation begins. Usually, the measured AC and DC voltage from the VSC board was used as activation triggers. Therefore, a convenient way to start current control at a given time was to step the voltage from the DC link from just below the threshold to just above. For example from 18V to 20V, with a threshold of 19.5V. This method for activation was also used in the two-module setup because the DC-link voltage is a global value that can trigger both microcontrollers simultaneously.

The initialization/start up procedure for the current control tests with a single module and fixed DC-link followed the following steps.

1. Set the desired current control activation criteria in the Simulink embedded model. All gate

signals are set to low until current control is activated.

2. Build, deploy and start the Simulink embedded model on the microcontroller board with external mode for signal logging.

3. Activate the bidirectional DC-source and charge the DC-side capacitor on the VSC-board to a voltage level below the desired CC activation level. This powers up the VSC board.

4. Adjust the voltage on the converter AC side from zero to the desired value by adjusting the variac, and monitoring $V_{c,AC}$ with the oscilloscope.

5. Step the DC-link voltage to the desired voltage for operation (20V=1pu). This triggers a counter which in turn activates the CC subsystem in the embedded code after a 10-second delay. Normal operation with current control begins.

6. Turn off is achieved by turning down the AC-side voltage to zero. The gate signal pins will again be forced to low when the AC voltage goes below a certain threshold.

5.5.5 Per unit values

The following values have been used as base values for representing the systems measured states in per unit. The base values have been chosen based on the range desired operating range of the variables and does not reflect the rated values of the system components or VSC board. The definition of the per-unit system for voltage source converters presented in Table 6 and Table 7 is from [38].

Quantity	Symbol and Value	Description
Voltage	$V_b = 10V$	Amplitude of the phase voltage
Current	$I_b = 1A$	Amplitude of the line current
Power	$P_b = 15W$	$= \frac{3}{2} V_b I_b$
Impedance	$Z_b = 10Ohm$	$= \frac{V_b}{I_b}$

Table 6: Base Values for a VSC System AC-Side Quantities

Quantity	Symbol and Value	Description
Voltage	$V_{b-dc} = 20V$	Equivalent DC voltage to $V_{b,ac}$ at unity modulation
Current	$I_{b-dc} = 0.75A$	$= \frac{3}{4} I_{b,AC}$
Power	$P_{b-dc} = 15W$	
Impedance	$R_{b-dc} = 26.6Ohm$	$= \frac{8}{3} Z_b$

Table 7: Base Values for a VSC System DC-Side Quantities

5.5.6 Simulation model of the single module laboratory setup in Simulink

A simulation model of the lab setup has been developed in Simulink and tested in parallel with the development of the lab. This model of the physical electrical lab setup should not be confused with the Simulink model used to generate the embedded code for the microcontroller, often referred to in this thesis as the embedded system Simulink model. The simulation model uses "Simscape specialized power systems" to simulate the physics of the electrical lab setup. The control algorithms are implemented as close to identically as possible in the embedded system and the system simulation model. Results from the system simulation model are presented alongside the results from the lab for comparison and verification.

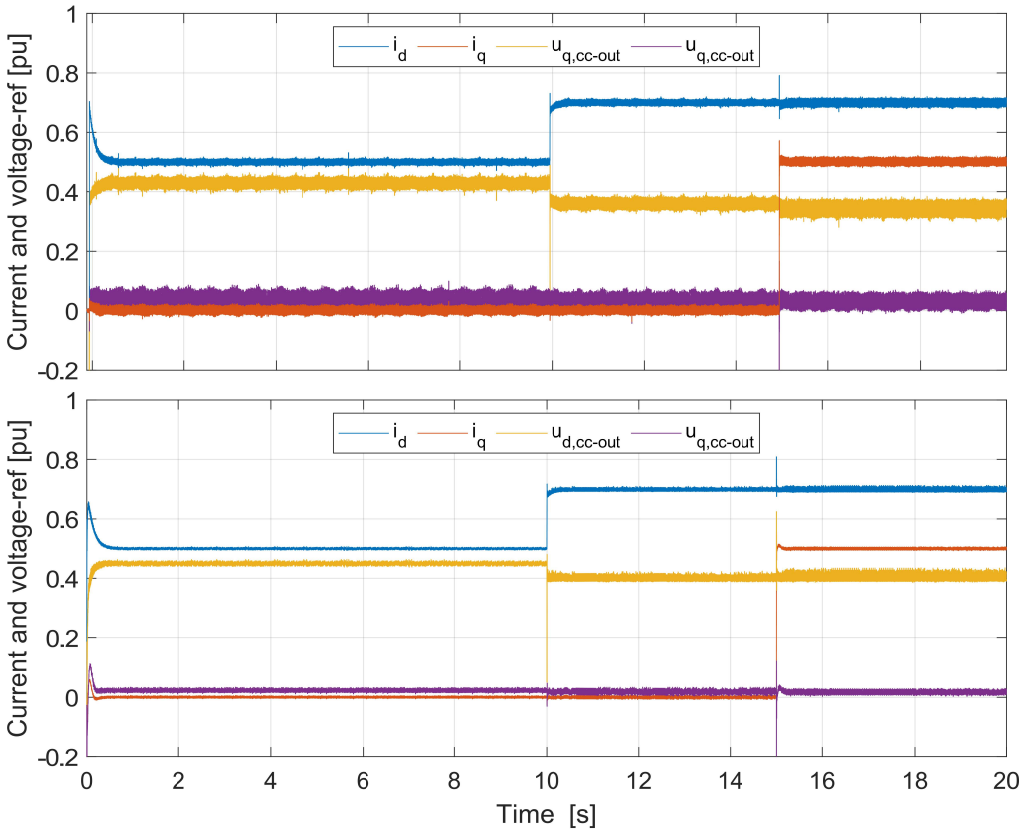


Figure 33: Step response of the current controller from lab (top) and system simulation model (bottom). Showing the measured d and q-axis currents i_d and i_q, and the controller output $ud_{cc,out}$ $uq_{cc,out}$. The CC is initiated at t=0, i_d steps from 0 to 0.5pu. And from 0.5pu to 0.7pu at t=10s. Reference step i_q from 0 to 0.5pu at t=15s.

5.6 Results and discussion of Current Control (CC) single module with fixed DC-link voltage

The main goal of this lab stage is to verify accurate reference tracking and system stability. Other points of interest such as bandwidth, noise filtering, appropriate startup and shutdown procedures, software triggers etc, were also investigated. However, the main objective at this testing stage is to prove the controllability and stability of the system experimentally. Verifying these control objectives lays the foundation for a successful implementation of the two-module voltage balancing in the next testing stage.

All lab tests presented in the following section were conducted with a fixed DC-link voltage of 20V

5.6.1 CC reference tracking and step response

The step response of the current controller was tested by stepping the d -and q-axis current references and observing the system states through logged signals from the microcontroller and waveforms captured on the oscilloscope. Numerous tests with varying reference values were performed with success in terms of stability and accurate reference tracking. Both the d-axis and q-axis current is shown to be controllable.

Correspondence with the simulations
Figure 33 shows the d -and q-axis current response to a predetermined sequence of steps in the reference as well as the voltage reference outputs from the current controllers. The results from the system simulations are also presented in Figure 33. As illustrated correspondence between

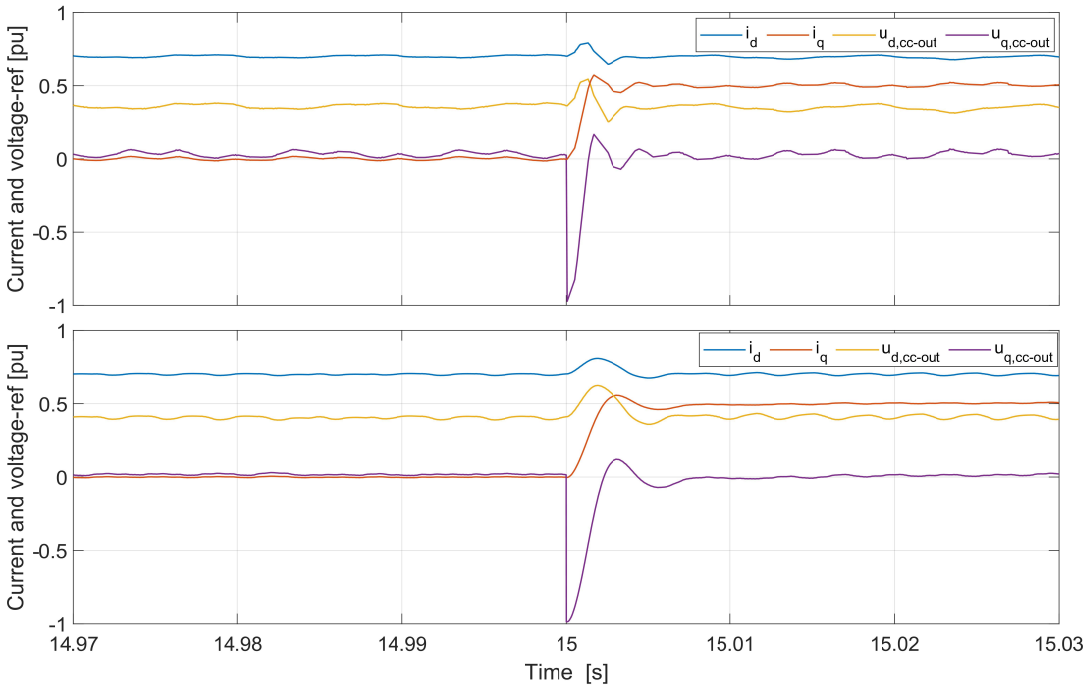


Figure 34: Step response i_q from 0 to 0.5 from lab measurements (top) and system simulation model (bottom). Showing the d -and q-axis current transient, as well as the current control system outputs in the d and q-axis.

the simulation and the lab results indicates that the simulation model replicates the lab setup well enough to be comparable and to aid in the analysis of the system dynamics. Also, the close correspondence with the simulations indicates that modeling the circuit as a linear time-invariant system (LTI) is an acceptable approximation. This means that the real-life circuit does not seem to be significantly affected by non-linear phenomena such as saturation in the transformer core, temperature-dependent impedance etc. In addition, the assumption of a stiff grid and negligible magnetizing current appears to be reasonable. In the simulation, the magnetizing impedance of the transformers is set to be at least 1000 times larger than the other circuit impedances.

Transient performance of the CC

Figure 34 shows the transient response of the q-axis current controller given a reference step input from 0 to 0.5pu at t=15s. Results from the lab are displayed in the top plot and the simulation results are in the bottom plot for comparison. Some significant overshoot is observed both in the lab results and simulations. This is as expected based on the quite aggressive tuning used for the current controller. As discussed in Section 5.5.3. An overshoot of around 10-15% is observed which is substantial but acceptable for the intended purposes. The rise time is less than 3ms and the settling time is around 6ms. This constitutes a fast control response. Without an accurate system transfer function, which requires accurate system impedance and control loop delay estimates, it is difficult to quantify the stability margins of the system. However, phase margin and overshoot are correlated and since the currents converge quickly to the reference with relatively low overshoot one can assume that the system is not close to the instability point.

Verifying logged data from the microcontroller with scope measurements

In order to verify the observations made based on the logged measurements from the microcontroller, external measurements on the system circuit are also made with an oscilloscope. Figure 35 shows two oscillograms captured during the step response testing (illustrated in Figure 33) before and after the step in the q-axis current. By looking at the phase shift of the current and line-to-line voltages[13] before and after the q-axis current step one can verify that the current and voltages do indeed shift relative to each other in the expected manner. Figure 35a shows that the current

[13]The line-to-line voltages on the primary and secondary were measured on the transformer terminals with differential probes.

waveform and the reference phase angle θ are in phase with each other. The A -to-C phase voltage of a three-phase system lags the phase A-to-neutral voltage by 30°. Because the current is purely in the d-axis at this point in time the secondary voltage of the isolation transformer $V_{A-C,s}$ should therefore lag the phase current by 30 degrees. The cursors in the oscillogram show the approximate phase shift between the primary line voltage and the phase current. This is measured to be 1.31ms equating to a phase shift of 23.6°. Since the secondary line voltage lags the primary line voltage by a measured 6.7°, the secondary line voltage lags the current by about 30°as expected. This indicates that the PLL does indeed track the actual phase voltage in the system even though some phase shift is introduced in the filtering on the measuring circuit of the VSC-board.

Figure 35b shows the same waveforms after the q-axis current has been controlled to 0.5pu. The d-axis current is still 0.7pu. Now the current has been shifted to 2.13ms leading in relation to θ, which corresponds to 38.3 degrees phase shift. Since $atan(\frac{0.5}{0.7}) = 35.5°$ is the theoretical phase shift this shows reasonable correspondence with the expected behavior. Since the measurements of the phase shift are quite inaccurate better compliance was not to be expected. Figure 35b also shows how the secondary (converter side) voltage shifts relative to the primary voltage in order to create the desired phase shift in the current.

5.6.2 Current control strategies

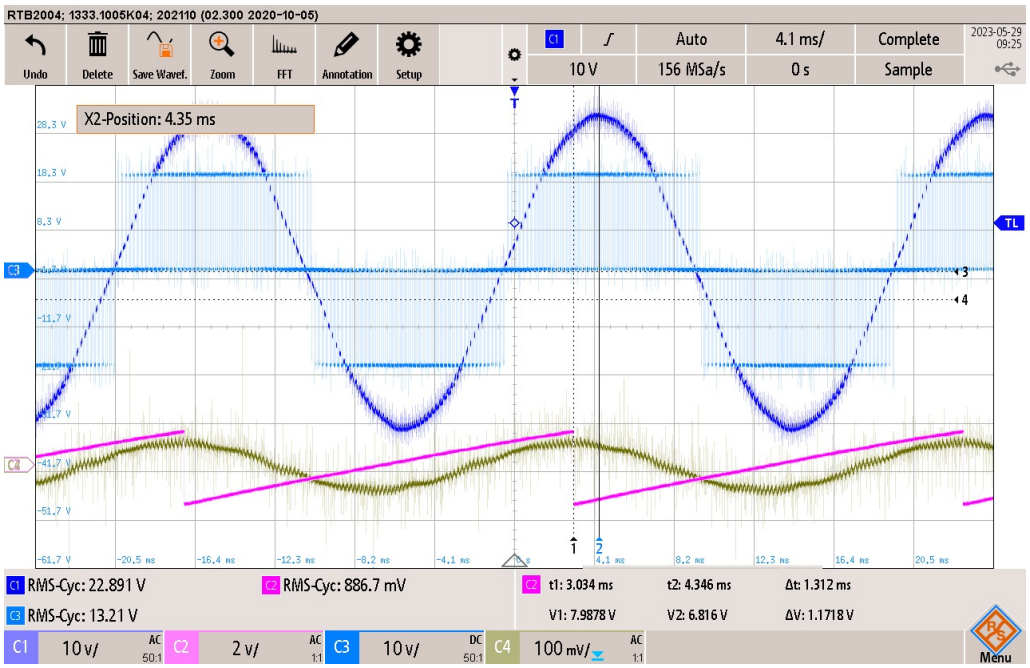
As mentioned previously in Section 5.2 using the converter side voltage as the reference voltage for the phase angle reference has some implications for the control strategies outlined in Section 2.2.3. When one uses a field-oriented phase angle reference for FOC current control of a PMSG, controlling the d-axis current to zero equates to controlling the stator current to be in phase with the induced emf in the stator windings. This gives the maximum amount of torque per amp of current, but the power factor on the stator output terminals/ converter input is not unity. However, in the lab setup detailed in this thesis, the voltage at the converter input is the reference voltage. Therefore, controlling the q-axis current to zero equates to aligning the stator current with the stator output voltage, aka the unity power factor strategy, and not the maximum torque per amp strategy. This does not compromise the validity of the lab results because the "unity power factor" strategy is also a viable strategy for PMSG control. However, it is important to highlight that due to this key difference in implementation between the lab setup and the proposed ModHVDC control system, a seemingly equivalent action such as controlling the reactive component of the current to zero is not equivalent in terms of the power output of the converters.

5.6.3 Maximum power transfer in the lab implementation

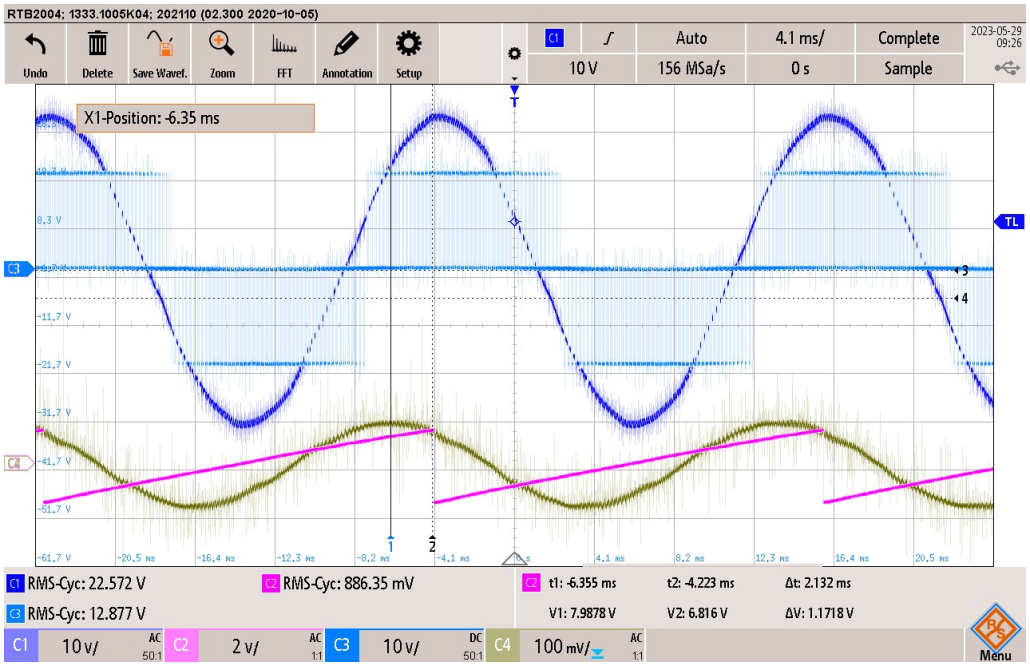
The maximum power transfer theorem becomes relevant when the d-axis current is increased beyond a certain threshold due to the high relative impedance of the AC side circuit. In order to increase the d-axis current the controller decreases the voltage on the converter AC-side terminals. This is because the magnitude of the current is dictated by the voltage difference between the voltage (V_p), and the converter side voltage (V_c) over the equivalent AC-circuit impedance. Figure 36 shows results from the lab and the corresponding simulation model while the d-axis current is being gradually stepped up by 0.2pu every 2 seconds. The point of maximum power transfer can clearly be observed based on the DC-current, which starts to decrease as the d-axis current increases after the d-axis current drops below half. Being aware of this pullout point is critical for the implementation of the voltage balancing control, presented in Section 3.3, Because the voltage balancing algorithm assumes a positive correlation between the d-axis current and power transferred to the dc-bus. Why an inverse correlation is observed after a certain threshold is explained in this subsection.

The VSC and transformer impedances can be simplified to a single-phase circuit with two series impedances and an AC source as shown in Figure 37.

[14]The current into the DC-link was measured using a multimeter because the VSC board does not have a built-in sensor for the DC-side current. The display of the multimeter was video-recorded during the test to log the measurements.



(a) Oscillogram captured at $i_d = 0.7pu$, $i_q = 0.0pu$



(b) Oscillogram captured at $i_d = 0.7pu$, $i_q = 0.5pu$.

Figure 35: Oscillogram showing; Ch1: $V_{A-C,p}$, Ch2: θ_{PLL}, Ch3: $V_{A-C,s}$, Ch4: $I_{a,pin}$. Where $V_{A-C,p}$ is the line voltage between phase A and C on the primary of the isolation transformer. $V_{A-C,s}$ is the line voltage between phase A and C on the secondary. θ_{PLL} is the output from the PLL in the embedded system probed on a DAC pin on the microcontroller. And $i_{a,pin}$ is the measurement of the current in phase A into the VSC board probed at the measurement output pin (range 0-3.3V)

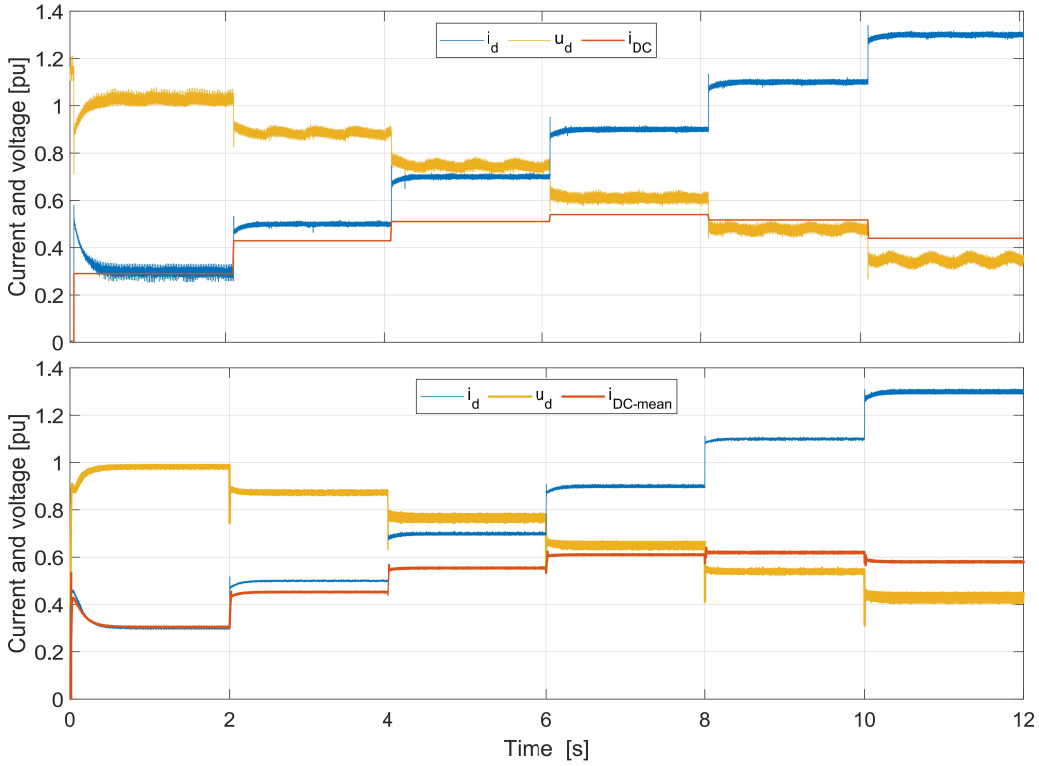


Figure 36: Lab measurements (top) and system simulation model (bottom). Showing the measured d-axis current and voltage, as well as the measured current into the DC-link[14], while the d-axis current reference was stepped up in increments of 0.2pu every 2 seconds from 0.3 to 1.3pu. i_q is controlled to 0pu throughout the test.

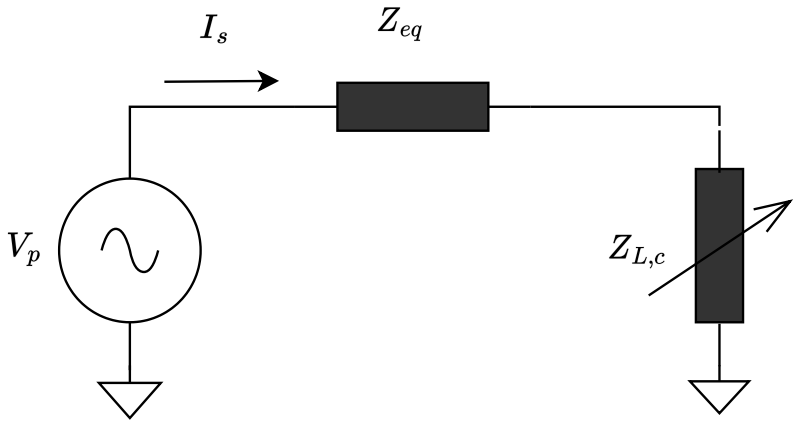


Figure 37: Simplified per phase equivalent circuit of the single module lab setup. V_p represents the fictitious voltage on the AC source side of the equivalent impedance Z_{eq}. $Z_{L,c}$ represents the voltage source converter as a variable load.

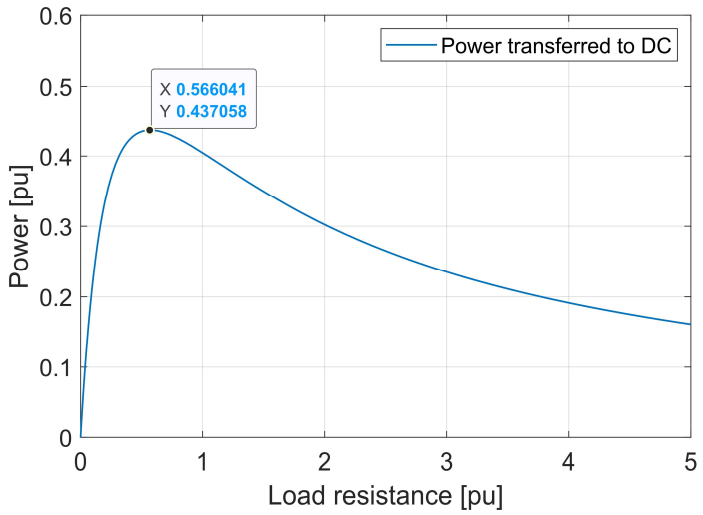


Figure 38: Plot showing the correlation between the magnitude of the load resistance representing the VSC and the active power transferred to the DC bus.

As stated in Section 2.4, the maximum power transfer to the load (DC link) occurs when the load impedance is equal in magnitude to the series connected source impedance (Z_{eq}), provided that the power factor of the load is fixed. A fixed power factor is the case because as explained in the above section unity power factor control strategy is implemented by controlling i_q to zero. If we simplify the circuit further by modeling the converter as a purely resistive load due to the unity power factor, we can plot the active power transferred to the DC side against the load resistance magnitude, as shown in Figure 38.

Figure 38 is plotted based on Equation 5.2, with r_L varying over a range of 0 to 5pu. v_p is set to 1pu, $|z_L|$ is the magnitude of the equivalent impedance in the transformer and variac in the lab setup in per unit. z_L is estimated in Section 5.5.1, and is set to $z_L = 0.57pu$.

$$p_{dc}(r_L) = \frac{|v_p|^2}{(|r_L| + |z_L|)^2} \cdot r_L \tag{5.2}$$

Where p_{dc} is the active power transferred to the DC side of the VSC.

As expected the maximum power transfer is achieved at $r_L = |z_L|$. Which gives an equal voltage drop over the two impedances. This is in compliance with the presented results from the lab and simulations. In a commercial electrical machine, the stator impedance will never be as large relative to the system ratings as in the lab setup proposed in this thesis. Because high stator impedance results in poor efficiency. Therefore commercial machines operate far to the right of the pullout point when considering a power transfer graph like the one presented in Figure 38.

Regarding the compliance between the simulations and lab results in Figure 36, it seems the impedance of the real-life lab circuit is higher than estimated due to the pullout point being reached earlier in the lab results compared to the simulations.

5.7 Potential sources of error

This subsection presents potential sources of error or discrepancies between the expected and presented results from the experimental verification.

Unbalanced AC voltage
Because the variable AC transformer (variac) is not entirely symmetrical in regards to output phase voltage magnitude, a ripple of twice the fundamental frequency (2x50Hz) is introduced in the dq0 current and voltage. This ripple is visible in the measurements from the lab, as shown in

Figure 39. The imbalances in voltage are more easily observed on the primary side of the isolation transformer and are generally in the range of 1-2V.

A more significant imbalance can cause problems for the PLL due to the 100Hz ripple component in the dq0 axis plane. As shown in [39], in which an alternative PLL implementation is presented for successfully mitigating the effect of the double frequency component on the phase angle tracking. However, in the lab related to this thesis, no significant tracking error was observed from the PLL. As shown in Section 5.5.2.

A simple simulation model was made in Simulink to verify that the PLL algorithm and tuning used in this thesis works well with an unbalanced input. To test this the PLL was given an unbalanced three-phase input with a 20% greater magnitude on phase C than A and B, and the PLL was initiated to be out of phase with the three-phase signal. The PLL did not appear to be significantly hindered by the imbalance in the three-phase signal, and the phase angle output stabilized quickly and correctly. The simulation model and results are shown in appendix Section B.1. In conclusion, the imbalanced AC source voltage observed in the lab implementation does not appear significant enough to impact the PLL or the current control system's performance.

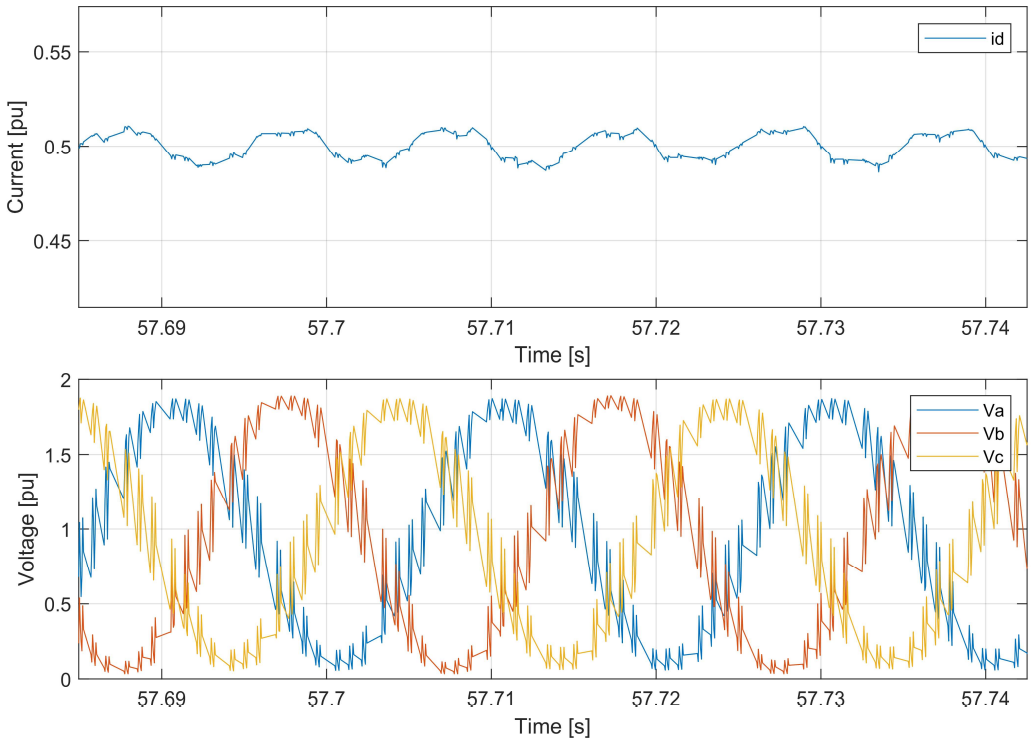


Figure 39: 100Hz ripple on d-axis current (top) due to the slightly unbalanced AC voltage (bottom). The displayed measurements are made by the VSC board and logged via Simulink external mode.

5.8 Two-module setup with fixed DC-link voltage

The final stage of the lab setup development for this thesis work is the two-module setup depicted in Figure 40. Two modules is the minimum realization of the modular system and is sufficient for proving the voltage balancing control algorithm works for series connected voltage source converters with a grounded system midpoint. The voltage balancing algorithm used in the embedded system in the lab setup is the same as presented in Section 3.3 and simulated in Section 4, with the exception of the implementation of the voltage reference set point and the tuning.

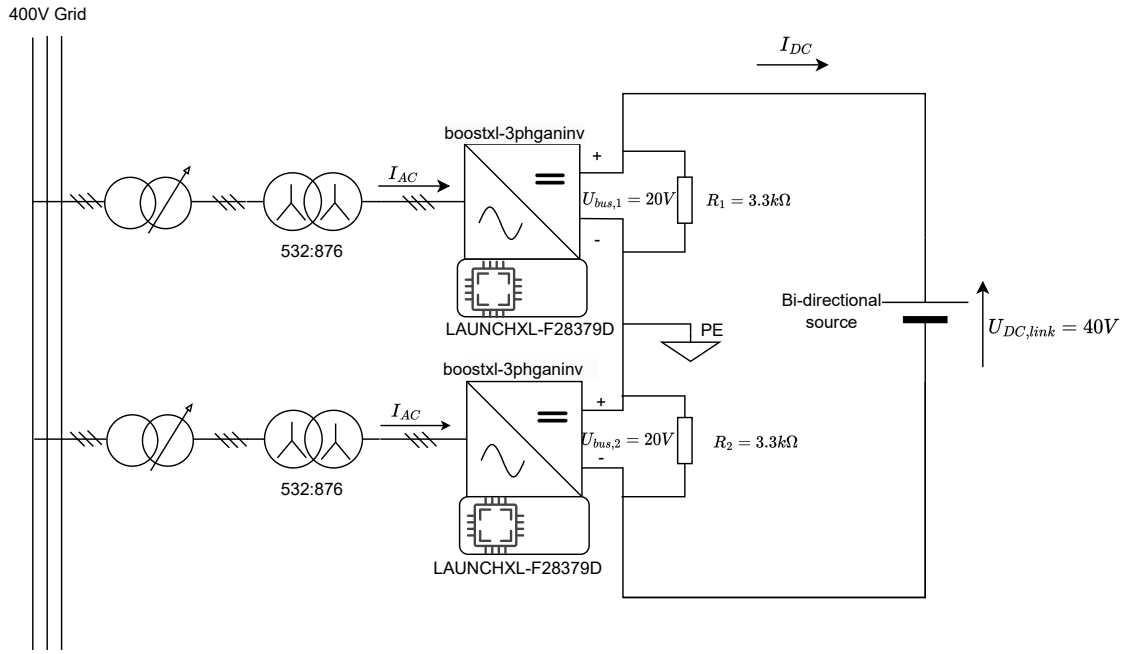


Figure 40: Two module lab setup

The ModHVDC system is based on modular converter units and modular control. This means that the control system is identically implemented in all modules. Therefore, the two-module system consists of identical single-module instances series connected together. The implementation of each is almost exactly the same as outlined in the "single module with a fixed DC-link" section of this thesis. Only now the voltage balancing algorithm is implemented in the embedded code. This section will be structured as follows. Firstly some technical design choices made for this stage of the lab implementation are explained, and the restrictions this places on the implementation are discussed briefly. Secondly, the implementation of the voltage balancing is outlined, and the results from testing the different voltage balancing strategies from Section 3.3 are presented. Lastly, the performance of the voltage balancing method and the laboratory test setup as a whole is discussed in terms of compliance with expectations and how well this proof of concept test-rigg manages to emulate the ModHVDC system concept.

5.8.1 Parallel resistors for even charge distribution between the DC-bus capacitors

The startup procedure used for these tests involves charging the DC-bus capacitors from the bi-directional DC source before the operation of the VSC is initiated. However, it was observed that the charge was not evenly shared between the modules. One of the modules would only reach 6V which appears to be the point at which the VSC-board starts drawing power and turns on, while the other module would receive the rest of the voltage drop ($V_{DC-link} - 6V$). This is a known phenomenon when connecting capacitors in series in real-world applications. A quick passive solution[15] is to connect a high ohmic resistor in parallel across each of the DC capacitors on the VSC boards. This solved the issue by allowing a path for the current to flow in order to

[15]Credit to Professor Dimosthenis Peftitsis for this solution.

even out the charge on the capacitors. The parallel capacitors are depicted in Figure 40. The DC-bus capacitors (220uF) are built into the boostxl-3phganiv (VSC) boards and are not displayed separately in the system schematic drawing.

5.8.2 Floating voltage and signal ground

In the boostxl-3phganiv boards, the signal ground and the power ground are two partitions of the same ground. Meaning the power ground and signal ground are galvanically connected to each other. This connection is not possible to break[16] while maintaining the functionality of the boards therefore the system design had to be altered from the intended layout. Because the signal ground of the VSC board is connected to the signal ground of the microcontroller the whole embedded system in module 2 is operated at a floating voltage equal to the floating voltage on the power ground. Aka, relative to the system ground (PE) the microcontroller is floating at $U_{DC,bus2} = -U_{DC,link}/2$. In order to avoid potential ground loops the microcontrollers were isolated from the host PCs by use of commercial USB isolators[17]. It is also possible to disconnect the 5V and ground in the USB port of the microcontroller by changing the jumper configuration on the board, but since the microcontroller draws a noticeable amount of power relative to the total power flow in the lab circuit powering the microcontroller from the USB was considered preferable. Ultimately, the consequence of the signal ground and power ground being inseparable is that two VSC boards cannot be controlled by the same microcontroller when one of the VSC boards is operating at a floating voltage potential. Therefore each VSC was controlled independently from two galvanically isolated microcontrollers. Also, practically it was impossible to transmit measurements between the two microcontrollers by means of direct wiring. Usually, measurements can be transmitted between the DAC pin on one board and the ADC pin on another through a wire, however this is not possible when there is a voltage potential difference between the two boards. As shown in Figure 41. It could be possible to transmit measurements by means of separate voltage divider circuits and inverting operational amplifiers, but there was not enough time to test and implement such circuits within the scope of this thesis work.

5.8.3 DC-voltage setpoint reference

Using the average of the measured DC-bus voltages as proposed by [5] and described in Section 3.3 was not possible due to the technical challenges described in the above subsection. Because the microcontrollers cannot exchange measurement data live, they are not aware of each other's DC bus voltage. Therefore a fixed voltage reference is used as the set point voltage for the bus voltage balancing controller. This is not ideal because the internal measurement circuits in the VSC are not necessarily accurate nor precise relative to each other or the real-world voltage on the DC-buses.[18] Ultimately the fixed reference voltage was manually set based on the estimated mean of the board measurements over a small interval. The DC-bus voltage setpoint was set to 19.335V for both modules.

5.8.4 Voltage balancing controller tuning and filtering.

The voltage balancing controller tuning constants are set as shown in Table 8. The tuning was done through trial and error since the precise physical quantities of the system and the delay of the inner loop current controller are uncertain. Stability and minimal overshoot were prioritized over high bandwidth. The DC bus voltage measurements were filtered with a first-order low pass filter with a 4ms time constant before they are passed to the voltage balancing controllers.

[16] It was confirmed by Texas Instruments that the signal ground and power ground could not be separated. Physically scraping away the conductive layer in the printed circuit was also tested, however, the board would not power up with this connection removed.

[17] RS PRO Isolated USB separator

[18] The internal DC voltage measurement circuit of VSC boards has an error of about 2% relative to measurements made with a multimeter. The error is however quite consistent and almost identical in both boards. The DC-link voltage provided by the DC source is also not accurate relative to its own setpoint but is consistently 3% lower than the setpoint.

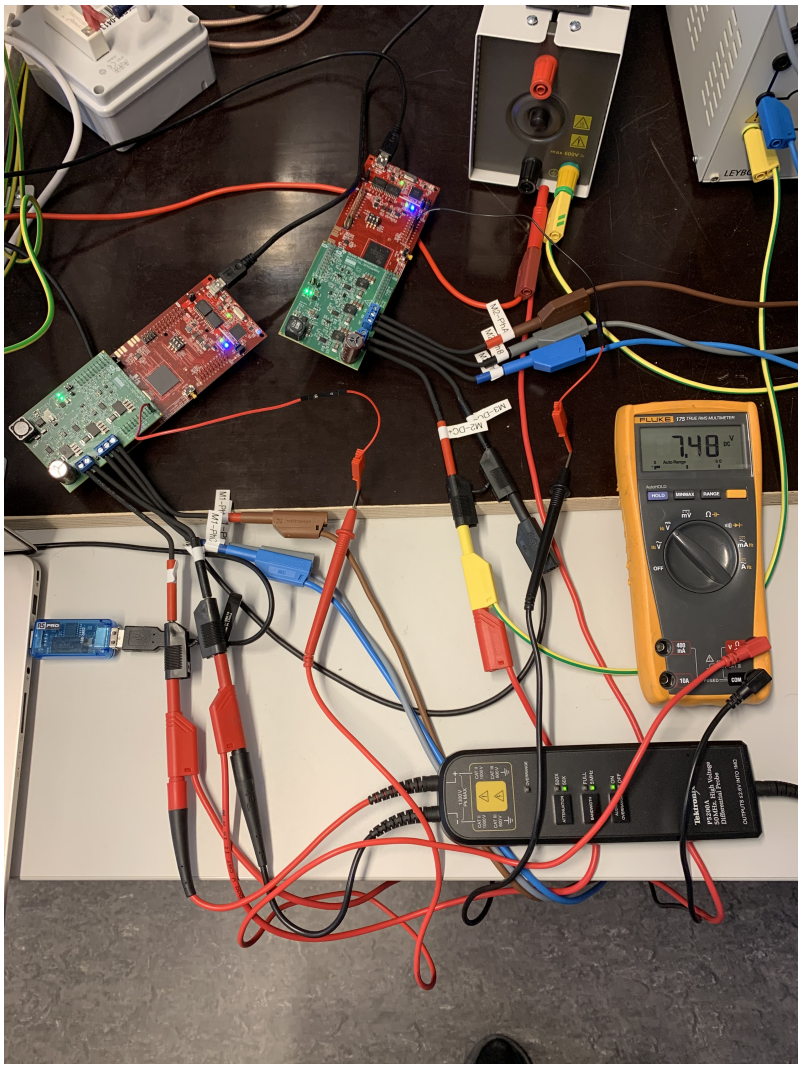


Figure 41: Voltage difference between two arbitrarily chosen pins on the separated microcontrollers used in the lab setup. DC link voltage is set to 20V.

K_p	0.5
K_i	3.0
T_{filter}	4ms

Table 8: Tuning of the voltage balancing controller in the lab implementation.

5.9 Results two-module voltage balancing

In order to test voltage balancing an imbalance in the DC-bus voltages has to be introduced. Uneven power production between the generator segments due to small asymmetries is a potential cause of uneven DC voltage between the modules in the ModHVDC concept[5]. Such asymmetries can easily be emulated in the lab by adjusting the winding ratio in the variable AC transformers (variacs) to be unequal. In practice, the three-phase output of the variacs will not be equal anyway due to imbalances between the phases internally in each variac, as described in Section 5.7. The results presented in the following subsections are from experiments in which the variacs were adjusted to produce an imbalance of around 10-15% between the DC-bus voltages during normal operation without voltage balancing enabled.

5.9.1 Test initialization and startup

The experiments presented below are all performed according to the following procedure.

1. Charge the DC-bus capacitors on the VSC-boards from the DC-link to below the predetermined current control software activation level.
2. Adjust the variac output voltage to the desired voltages (close to 1pu). All switches in the VSC are open until CC is activated.
3. Step the DC-link voltage to the desired level (40V), which activates a 10-second countdown until CC is activated.
4. The current controller (CC) controls the q-axis current to zero and the d-axis current to 0.5pu.
5. 10 seconds after CC is activated the voltage balancing controller is activated.
6. Shutdown is performed by turning down the AC-side voltage. The VSC switches are opened when the ac voltage drops below a certain threshold.

A plot of the voltage balancing operation in which the activation stages are clearly marked is displayed in Appendix Section B.4.

5.9.2 Voltage balancing results -"Split the difference" strategy

Figure 42 shows the effect of activating voltage balancing when the AC-input voltages to the modules are unequal in magnitude. The DC-bus voltages are effectively controlled to the DC-voltage setpoint. The system response is overdamped as a consequence of the passive tuning. No stability issues are observed as a consequence of activating the voltage balancing algorithm.

In the scenario tested in Figure 42 no saturation constraints are implemented on the voltage balancing controller. This is a viable tactic when the wind turbine is operating at below-nominal power because the current level is not close to the system components' rated value. Therefore, increasing the d-axis current on one of the modules is unproblematic.

5.9.3 The consequence of discrepancies between the fixed set point voltage and the voltage measurements on the VSC boards.

Figure 42 only shows the first 15 seconds of operation after the voltage balancing is activated. When the experiment is run over a longer time frame, a detrimental consequence of using a fixed voltage reference set point for the voltage balancing controller becomes evident. Figure 43 shows the same system states as Figure 42 over a longer time frame. Here it becomes clear that the predetermined voltage reference is slightly lower than the mean of the actual voltage measurements in the VSc boards. Meaning there is a slight steady-state error between the reference and the measured system states. This is an error that voltage controllers cannot compensate for because the error is present in both modules. Therefore the modules will be fighting each other by reducing the balancing current equally in both modules. Since the DC-link voltage is externally controlled, neither module sees a decrease in its respective DC-bus voltage because it is only the relative power transfer of the modules compared to each other that determines the distribution of voltage between the modules. The integral term in the voltage balancing controllers will continue to integrate the steady-state error indefinitely because both modules cannot reach the reference simultaneously. A reference that cannot be reached is unacceptable in a PI-based control system. Consequently, three options are considered viable for determining the fixed set point for the voltage balancing controller.

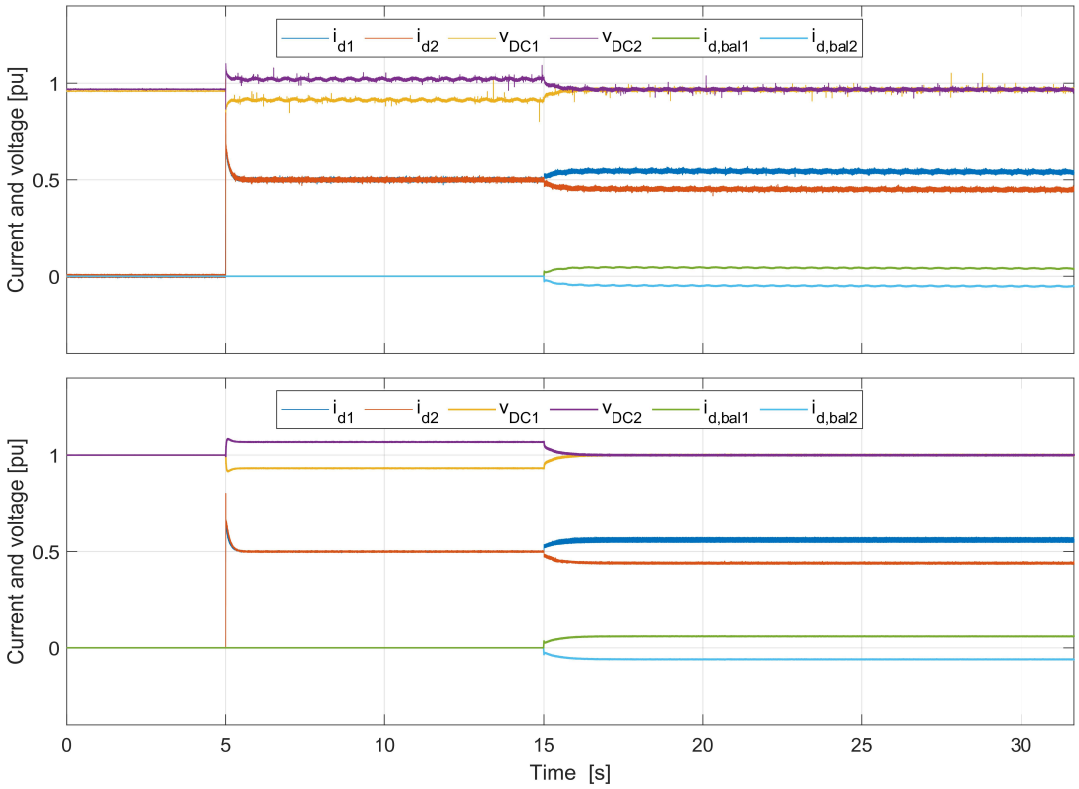


Figure 42: Voltage balancing results from the lab (top) and simulation (bottom). Current control is activated at t=5s and voltage balancing at t=15s. $i_{d,bal}$ represents the balancing current reference outputs from the voltage balancing controllers.

1. Either the reference has to be set based on highly precise measurements of the DC-link voltage divided by the number of modules (N), while also making sure that the measurements of each DC-bus voltage are accurate and precise relative to the DC-link and relative to each other. Differences between the individual module measurements will also cause integral wind up, as explained in [5]. This solution is practically challenging because even slight measurement deviations will accumulate over time due to the integral term in the PI controller. It could be viable to floor the error given to the PI, which allows for some error in the voltage balancing but would remove deviations outside a certain threshold.

2. Setting the reference based on the sum of the DC-bus measurements made by each respective module, as proposed by [5]. This is clearly a superior method, however, it requires live transferring of data between the modules which is not possible in the lab setup detailed in this thesis, as explained in Section 5.8.2.

3. Lastly, this specific phenomenon of both module balancing references drooping in tact with each other can be solved by implementing the torque droop control proposed by [5]. The droop controller is explained in Section 3.5. The purpose of the droop controller is to remove any non-zero torque contribution from the balancing currents. Therefore it will compensate both a positive and negative trend in $i_{d,bal}$, as shown in Figure 44. Because the droop controller also requires intercommunication between the module control systems, the droop controller cannot be implemented in the lab setup detailed in this thesis.

5.9.4 Voltage balancing lab results- ”The weakest link” strategy

When the system is operating at the rated power the voltage balancing control comes into conflict with the limits imposed by the system ratings, as explained Section 3.4. Therefore if the AC

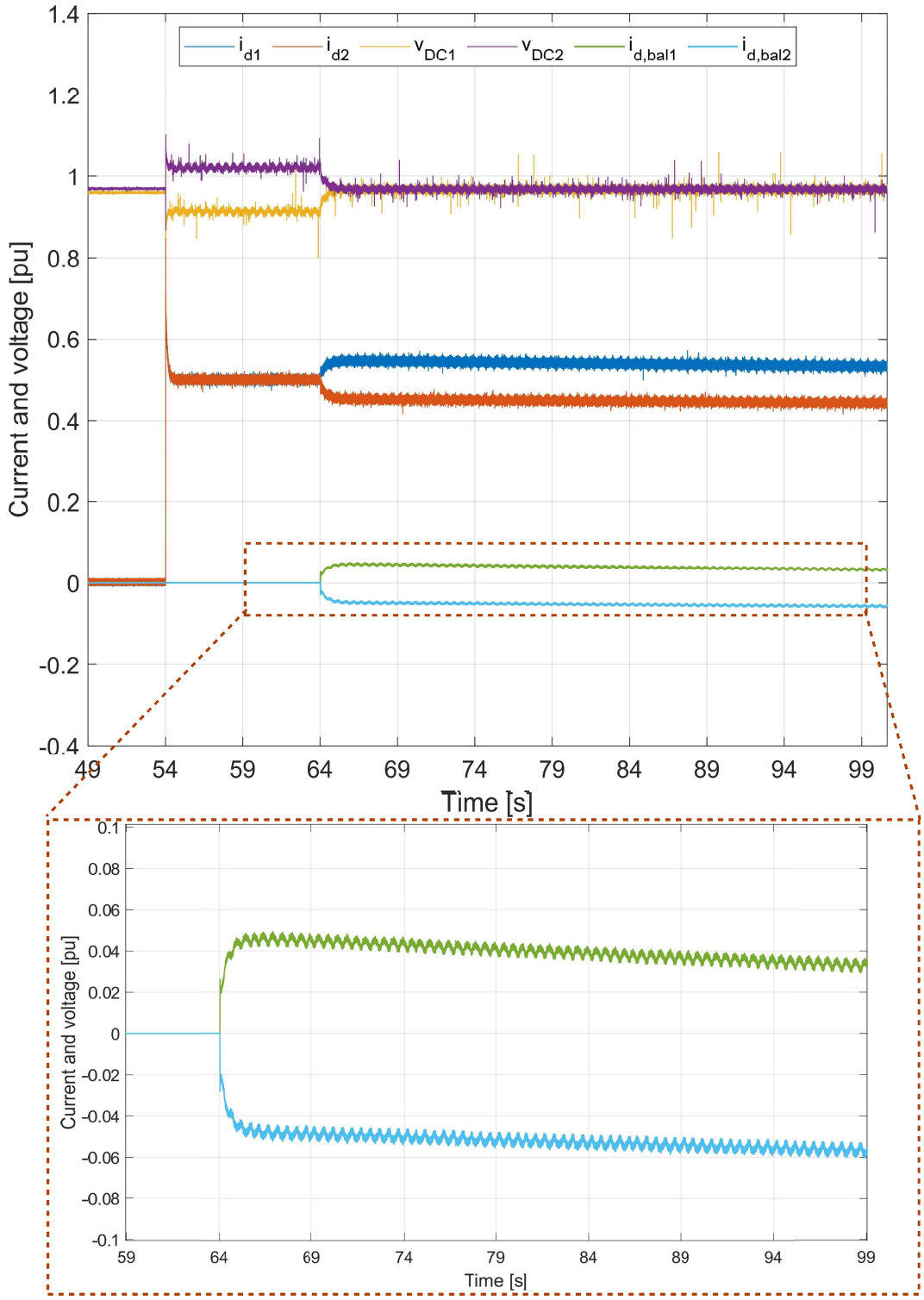


Figure 43: Voltage balancing results from lab experiment with a longer time frame. With zoom on the balancing current reference outputs from the voltage balancing controllers.

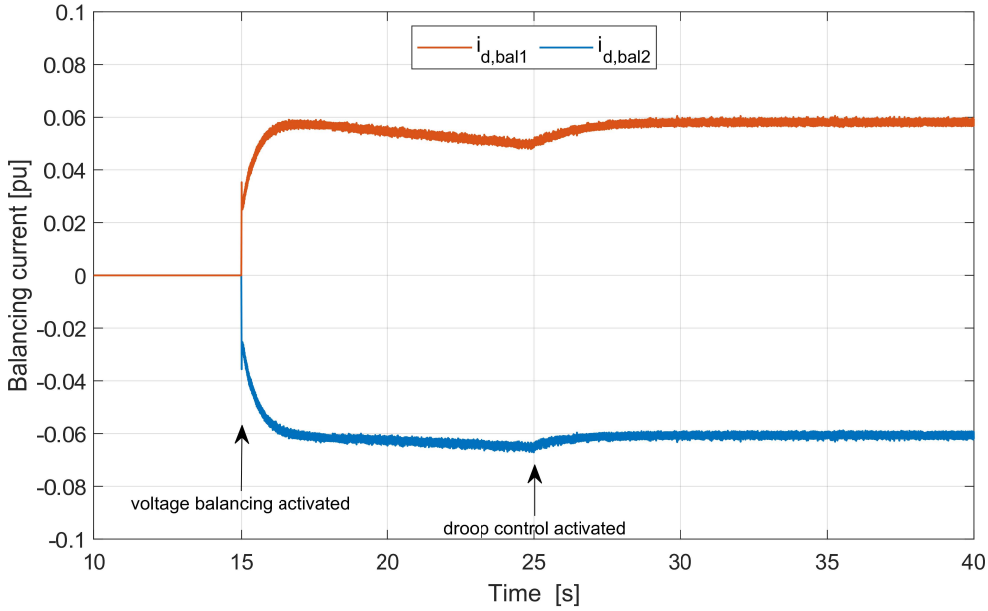


Figure 44: Simulation results showing the effect of introducing voltage balancing droop control when the voltage set point for the balancing controllers is lower than the measured DC bus voltage of both modules.

current rating of the system is considered a hard limit according to Equation 5.3, then voltage balancing will require all modules to come down to the power produced by the weakest module. This strategy is shown in Figure 45. Note that the lab setup is not operating at rated power during this test, however, the balancing logic is the same regardless. The critical aspect is that the modules with the most power transferred to the DC must come down to match the power of the weakest module.

$$i_{d,i} = i_{d,s} + i_{d,bal,i} \leq 1pu \tag{5.3}$$

Where $i_{d,i}$ is the total d-axis stator current of module i, $i_{d,s}$ is the d-axis reference set by the speed controller.$i_{d,bal,i}$ is the balancing current reference set by the voltage balancing controller for module i.

5.9.5 Voltage balancing lab results- "Lift to rated power" strategy

The final strategy discussed in this thesis involves voltage balancing by forcing all modules to produce rated power regardless of the voltage deviations on the AC side. This means that the modules with lower AC voltage than the rated will increase their d-axis balancing current until their DC bus voltage is equal to the rest of the modules. However, the normal modules which are already operating at rated power will not decrease their d-axis current in response to the voltage imbalance. The controller behavior with this strategy implemented is shown in Figure 46. Again the lab system is not actually operating at rated power, but the voltage controller behavior is the same as long as we define the operating point of module 2 as the desired operating point. The "Lift to rated power" is effective in achieving DC link voltage balancing and does not require the system to reduce its power output from the rated, however, the strategy requires the underpowered modules to exceed the AC current limit significantly. Therefore this strategy requires overrating of the AC side of the system in terms of maximum current. All modules must be overrated because it is difficult to know before the operation of the system has begun which module will deviate from the others in terms of flux linkage, stator resistance etc. Overrating all modules increases the initial cost of components and materials. Especially overrating the continuous current rating of the transistors in the VSC can make the ModHVDC concept less attractive due to increased

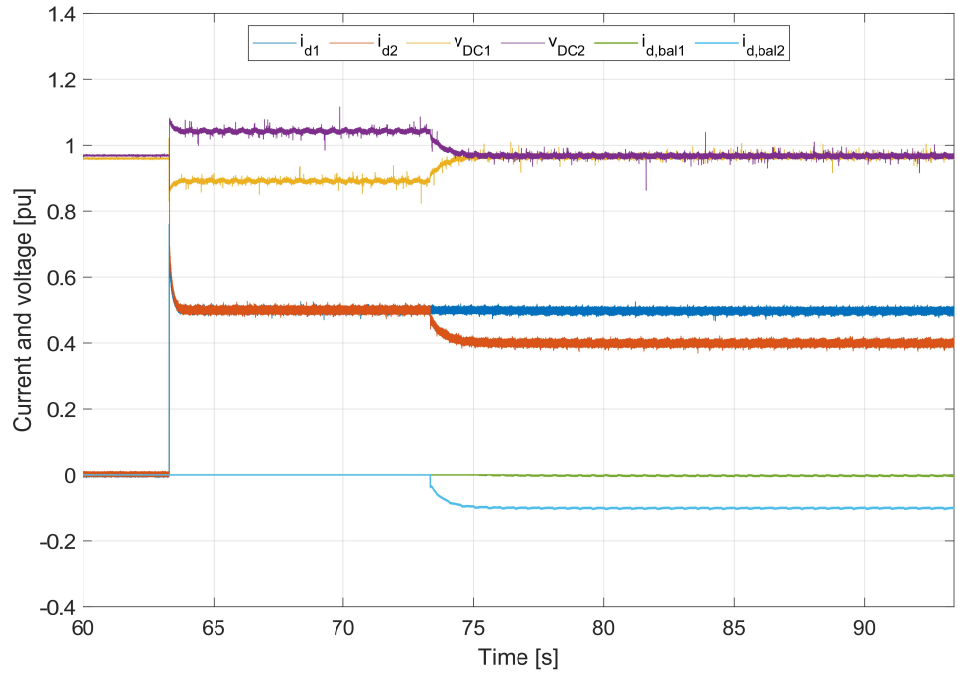


Figure 45: Voltage balancing using the "weakest link" strategy. Lab results. The reference for i_d and i_q are set to 0.5pu and 0.0pu respectively.

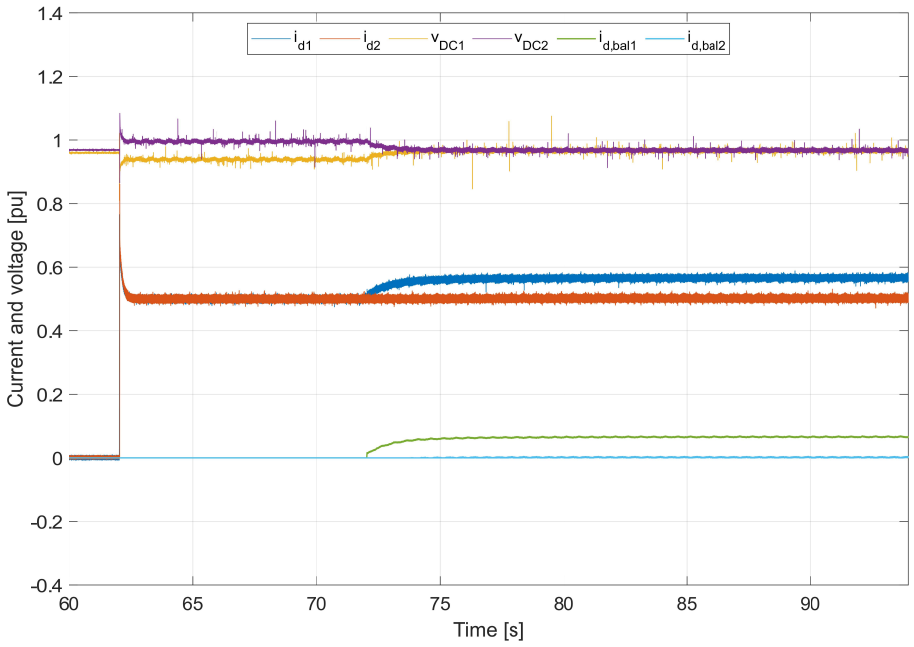


Figure 46: Voltage balancing using the "Lift to rated power" strategy. Lab results. The reference for i_d and i_q are set to 0.5pu and 0.0pu respectively.

upfront costs. Further cost analysis must be performed in order to determine if it is economically viable to implement the "Lift to rated power" strategy.

5.10 Discussion on the overall laboratory setup and results.

Overall the results from the experimental test made on the laboratory setup yielded results that are in line with the simulation results from the ModHVDC concept simulation, presented in Section 4. The main objective of the experimental lab setup is to emulate the concept of ModHVDC as closely as possible while at the same time reducing the complexity of the system enough to enable swift development and testing of the lab. Reducing the need for expensive equipment is also crucial for "proof of concept" experimental verification. In this section, a review of how well the lab setup emulates the ModHVDC concept is presented. As well as a discussion on the viability of the obtained lab results and the possibility for further expansion of the lab setup.

5.10.1 Three phase transformers for emulating the segmented stator of the proposed PMSG

Using a separate grid-connected variable transformer (variac) and separate isolation transformers in order to emulate the segmented stator of the proposed PMSG proved to be viable in terms of providing the VSCs with independently adjustable three-phase AC voltages. No coupling effects were observed between modules on the AC side. Meaning that the voltages measured on the variacs were not affected by changes in AC voltage on the other module. This is as expected. Even though the variacs are connected in parallel at the point of common coupling with the grid, there should be no galvanic or magnetic coupling between the AC branches of the modular system.

The main difference between a variable speed PMSG and the grid connected transformers is the variable frequency of the output voltage. The frequency of the ModHVDC generator will vary according to the speed of the turbine between 0.3 and 1pu, assuming a cut in speed of 0.3pu. Meaning the electrical frequency can vary by 70% during operation in zone 2 and 3. A change in will alter the reactance in the circuit, which could affect the performance of the current controller due to the tuning being based on nominal speed operation. Also estimating the flux and thereby rotor position can be more challenging at low frequency. No such effects are possible to test with grid connected transformers.

5.10.2 Bi-directional DC source for emulating DC-link

The bidirectional DC source used in the lab setup served its purpose well, even though it is rated for much higher power applications than this lab setup. The source is rated for up to 30kW, and the manufacturer's datasheet specifies that the internal measurements of the board are inaccurate when used for low-power applications. This was noticeable but not an issue for the intended purposes. Because although the DC voltage output from the source was not 100% accurate, it was highly precise and consistent. Meaning that although the DC link voltage was approx. 38.6V when 40V was specified, the voltage did not fluctuate during operation, and the error between the set point and actual voltage[19] was the same every time. The internal current measurement and logging functionality were not used due to the low resolution of the current measurement.

5.10.3 Embedded system

The LAUNCHXL-F28379D launchpads from Texas Instruments were able to execute the programmed functionality of the embedded code in real-time. Although the system does not meet the requirements for a hard real-time system, the embedded system output corresponded well with real-world values when measured using an oscilloscope live during tests. If the embedded system were not able to perform its tasks in the allotted time it would be visible from measured variables like the frequency of the PLL output relative to the AC waveforms on the oscilloscope. During Simulink external mode operation, there seems to have been some data drops based on the non-homogeneous time stamps of the logged data. However, this is not considered to be critical in terms of the validity of the obtained results.

[19] Measured with a multimeter

5.10.4 PLL for producing phase angle reference

Using a PLL for the phase angle reference has been shown to be a viable option. However, using the converter side AC voltage is undesirable due to the voltage waveforms at the converter being square waves and the possibility of undesired coupling effects between the PLL and the current controller. Therefore using the voltage on the primary side of the isolation transformer as the input to the PLL might be a superior implementation.

Current control The current controller showed accurate reference tracking and low settling time in response to reference changes. It is therefore acceptable to assume that the inner loop current controller has a sufficiently high bandwidth relative to the outer loop voltage balancing controller. The stability margins based on a qualitative analysis of the current controller overshoot and relative dampening it seems that the stability margins are acceptable as well. It is however possible to make an accurate estimate of the control loop delay and AC side system impedance. When these quantities are known, it is possible to improve the tuning by utilizing the modulus optimum criteria. Implementing feed-forward terms of the cross-coupling effects between the d and q-axes will also improve performance and reduce the coupling effects observed in Section 5.6.1.

Measurements made on the lab circuit with an oscilloscope supported the observations made based on the internal measurements in the VSC. When controlling the q-axis current which corresponds to introducing a phase shift between the converter side voltage and current, the corresponding phase shift was observed on the oscilloscope. Being able to accurately control the q-axis current is important in order to implement different current control strategies and to emulate field weakening control which is not discussed in this thesis but is a functionality that could be desirable to test at a later stage.

5.10.5 Voltage balancing

The voltage-balancing controller was successful in balancing the DC bus voltages of two series connected modules and showed an overdamped response when activated. However, due to the individual module controllers being blind to the voltage and balancing current of the other module, a fixed DC voltage set point had to be used as the reference for the voltage controllers. Small discrepancies between the measured steady-state DC bus voltage of the individual modules and the set point causes infinite integral windup in both modules. Ultimately this will lead to instability in the system as the d-axis current reference approaches negative values. Any such runaway behavior is unacceptable. In general, effects which cause the d-axis current to deviate more than necessary from the reference set by the speed controller are undesirable.

It is shown in Figure 44 that implementing voltage droop control prevents the sum of the balancing currents from drifting to net positive or negative. Implementing the set point voltage reference based on the average of the DC bus voltage measurements would eliminate the problem of constant steady-state error in the voltage balancing controllers and subsequently the drifting balancing current because the set point voltage will then always be an attainable value for all modules. This highlights the need for intercommunication between the control system of the modules because both the voltage droop control and average value set point voltage require measurements from the other N-1 modules to function as intended.

5.10.6 Voltage balancing strategies

The voltage balancing strategies outlined in Section 3.4 showed the expected behavior in terms of voltage balancing current contribution and effective DC bus voltage balancing. The test conducted on the lab setup only emulates the concept of implementing a given limitation on the voltage balancing controller output and which in turn forces a certain behavior in terms of which module must compensate for the discrepancy in DC bus voltages between the voltages. However, a test which demonstrates that the underlying physical relationship between the control system actuator mechanism and the system's response is of value. In the case of this specific lab setup, it was shown how if we go beyond the point of maximum power transfer to the load (VSC) the actuator

mechanism of the voltage balancing controller uses to increase the DC bus voltage (increase the d-axis current reference) has the opposite effect on the bus voltage than intended.

The three strategies present different advantages and drawbacks. The split the difference method in combination with the voltage droop control balances the voltages without a net torque contribution from the balancing currents. The split the difference method is therefore a good option if torque control is used instead of speed control. The split the difference strategy is considered to be the preferable relative to the other two strategies when the turbine is operating at below nominal power (Zone 2 and 3), because it results in the most even loading of the modules in terms of current and torque contribution.

As discussed previously, At nominal power the choice of strategy comes down to what is considered to be most important, maximum power production while in operation or avoiding increased component costs due to overrating. Switching between strategies at nominal operation in order to reduce the continuous loading on the components is also a possibility. As well as allowing DC voltage bus imbalance within a certain margin. As is discussed in [4].

5.10.7 Correspondence with simulations

The physical lab system behavior corresponds well with the simulation model which was made to replicate the physical lab setup. Both the transient controller response and system quantities were shown to comply with the real-world results. This supports the validity of the lab setup because it means that it is unlikely that unknown factors play a large role in the obtained results. Also, it supports the credibility of the Simscape Specialized power systems library in its realism and ability to aid in the further development of this specific lab setup by accurately predicting the lab system behavior.

6 Conclusion

In this thesis, the control system for a two-module realization of the series-connected VSCs from the ModHVDC concept has been investigated through simulations and a laboratory small scale implementation. The lab implementation includes an embedded system carrying out the module-level control algorithms.

The experimental laboratory setup was found to emulate the ModHVDC concept proficiently, and the behavior of the lab system relative to the simulations of the complete control system with a modeled PMSG showed reasonable correspondence. The implemented control algorithms in the lab setup, including the PLL, current control, and voltage balancing, all operated successfully, although with room for improvement. Using the measured AC voltage on the converter terminals was found to be unideal but not detrimental to the system's performance. Using the primary side of the isolation transformer would likely be preferable in terms of emulating a field-oriented generator drive. The floating voltage potential on the lower module propagated to the microcontroller due to the power ground and the signal ground being galvanically connected. Making intercommunication between the modules challenging. Therefore, master-level voltage set point control was not possible to implement, which takes away some of the compliance between the lab and the ModHVDC system. A fixed DC voltage reference was found to cause instability over time unless the voltage reference exactly matches the DC-bus measurements made by each module.

The current control algorithm resulted in accurate reference tracking, and despite aggressive tuning the system step response had acceptable settling time and overshoot percentage.

Each of the voltage balancing strategies discussed in this thesis provides viable alternatives for balancing the bus voltages in the ModHVDC system. Each has specific implications regarding system performance, economic feasibility, and equipment rating requirements and further cost-benefit analysis is necessary to find the optimal strategy for implementing the ModHVDC system. However, it is demonstrated through experimental testing and simulations that all three strategies provide accurate DC voltage matching between the modules and provide a stable system response with the given tuning constants.

Switching between strategies in different operational zones of the turbine could be beneficial. "Split the difference" is considered most optimal in zone 2 and 3 while one of the other to strategies could be chosen in zone 4 in order to either reach nominal power production in all modules or reduce the power production of all modules in order to not surpass the AC current rating of the weakest modules.

7 Further work

Expanding the lab setup to three modules would allow for investigating several essential aspects of the modular system. With three modules, faulty-module-bypass could be implemented and tested on the lab system setup. However, structural changes must be made to the existing module configuration to facilitate three series-connected modules. First, split external capacitors must be connected to the DC buses to access the system midpoint for grounding. Secondly, the signal ground and power ground must be separated, or new VSCs which do not have a connection between the two grounds must be acquired. Separating the grounds is necessary to implement DC voltage set point control and for operating several VSCs from the same microcontroller. Verifying the discussed voltage balancing strategies in a three-module lab implementation is also critical for assessing the feasibility of the strategies for a multimodular system.

In order to better emulate the ModHVDC system, using the output voltage of the variac as the PLL input instead of the converter terminal voltage might be a superior solution. This method might be tested in future work. However, replacing the grid-connected transformers with low-power synchronous machines would allow for better emulation of the system as a whole. Flux-based rotor position estimation can then be used to generate the phase angle reference, and master-level speed control can be implemented.

Lastly, a dedicated study on the economic feasibility of the discussed voltage balancing strategies should be performed. Taking into account both the cost of increasing the AC current-rating of all module converters and the potentially increased cooling needs in the stator segment as a result of increased ohmic losses due to the above-rated current level.

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Appendix

A Complete Control System Synthesis Appendix

The subsections of "complete control system appendix" are a restatement of paragraphs from the author's specialization project [1], and are therefore not a product of this thesis work.

A.1 Current ripple filtering and converter delay, for CC tuning*

Filtering of the current measurement introduces a delay in the control loop which must be accounted for with tuning. In the proposed control system, the dominant source of high-frequency harmonics on the current measurements comes from the voltage source converters. If the ripple in the current measurement is not filtered, it will propagate back through the controller and become noise on the voltage reference output from the PI-current controller. To mitigate this noise a simple first-order low-pass filter is implemented. According to [29] the ripple level in the voltage reference should not exceed 8%. The filter-to-PWM switching time ratio controls the percentage ripple. T_f/T_{sw}. A Ripple of 8 % should be achievable with a ratio of 0.02 for a generic three-phase converter, i.e T_f =200μs for a switching frequency of 1kHz. Because a smaller ripple than 8% is desired, the filtering time constant is set to 1ms.

The delay introduced by the two-level VSC can be simplified as shown in (.1). Where $T_{\omega s}$ is assumed to be equal to $1/(2 \cdot fs)$ [40].

$$e^{-T_\omega s} \approx \frac{1}{T_\omega s + 1} \tag{.1}$$

Modeling the time delay in the converter as shown in (.1) is a simplification of the delay dynamics. In [41] the implications of delay in the control system for a 2L-VSC is discussed. It is found that high-frequency resonance can occur in VSC-HVDC when a critical time delay is surpassed in the control system. Advanced delay modeling is outside the scope of this report but is worth bearing in mind.

A.2 Speed controller tuning and frequency response*

The speed controller is tuned using the same method as for the voltage controller. Only the plant time constant and filtering values are different. Using the symmetrical optimum method the following tuning parameters are proposed for the speed controller.

Table 9: Direct speed controller tuning. $\alpha = 7$

Parameter	Value
T_m	6 [s]
$T_{sc,f}$	60 [ms]
$T_{eq,cc}$	3.0 [ms]
$T_{i,vc}$	0.44 [s]
K_p, vc	36.0 [pu]

These tuning constants yield a phase margin of 48.6 degrees for the direct speed controller. This is within the desired phase margins. The speed controller's bandwidth is about 50 times smaller than the inner loop current controller. Hence the current controller should have no problem keeping up with the speed controller's changes in q-axis current reference.

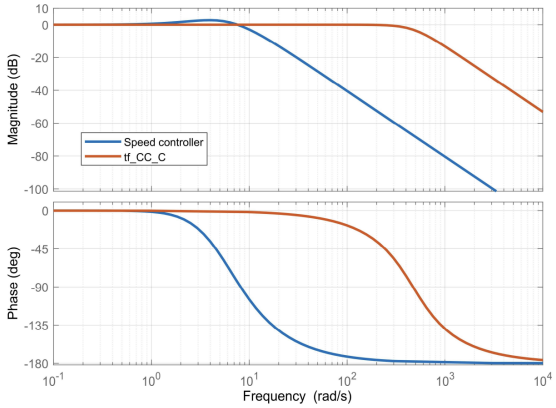


Figure 47: Closed loop frequency response of speed controller and current controller.

A.3 Pitch controller implementation*

The pitch controller developed for the simulation model is based on simple PID control and empiric tuning. Little research was found on the implementation of pitch controllers used for speed control in wind turbines. Therefore, the implementation is only a product of the author. The pitch controller's function is consequently not optimized nor guaranteed to be viable on a real wind turbine. For the purposes of the simulation model, however, it is sufficient.

The pitch controller block diagram is depicted in Figure 48.

The if statement in Figure 48 indicates the activation conditions for the pitch controller. The pitch controller is only supposed to step in when the DSC is saturated in zone 4, due to the rated current and torque limits of the generator.

The hydraulic delay is introduced to impose some realistic delay in the controller. According to [42], large wind turbines often use hydraulic pressure in order to pitch the turbine blade. The delay from the hydraulic system is assumed to have a time constant of 0.25s in [42]. The same is assumed to be true in this report.

The tuning of the pitch controller is presented in Table 10. Because the relationship between pitch and torque is complex and non-linear, the tuning is based only on trial and error and not on the system transfer function. The goal of the tuning is to make the control response slow and overdamped. It is not desirable to have oscillations in the speed or pitch angle of the turbine. Therefore, the derivative term is added in this controller.

Table 10: Pitch controller tuning.

Parameter	Value
K_p, p	50 [pu]
$K_{i,p}$	10 [pu]
$K_{d,p}$	20 [pu]

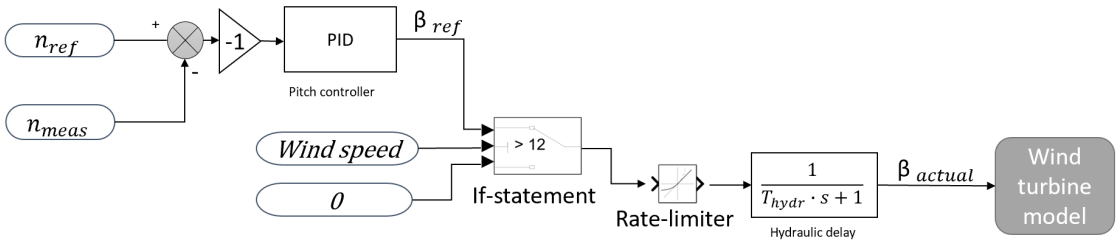


Figure 48: Pitch controller block diagram.

A.4 Complete control system simulation models base values*

Table 11: Base values for VSC and the two-module system.[38]

Parameter	Base Value
Module AC power P_{base}	1.11[MW]
Module peak AC phase voltage U_{base}	$\sqrt{2/3} \cdot 6.43 kV_{rms}$=5.28[kV]
Module peak AC-line current I_{base}	$\sqrt{2} I_n$ =140.3[A]
Impedance Z_{base}	U_{base}/I_{base} =37.6 [Ω]
DC-link power $N \cdot P_{DClinkbase}$	2.22[MW]
DC bus power P_{DCbase}	1.11[MW]
DC bus voltage	$2 \cdot U_{base}$= 10.6 [kV]
DC link voltage	$N \cdot 2U_{base}$= 21.1 [kV]
DC Current	$(3/4) \cdot I_{base}$= 105[A]

B Experimental Verification Appendix

B.1 Simple PLL performance simulation with unbalanced three-phase

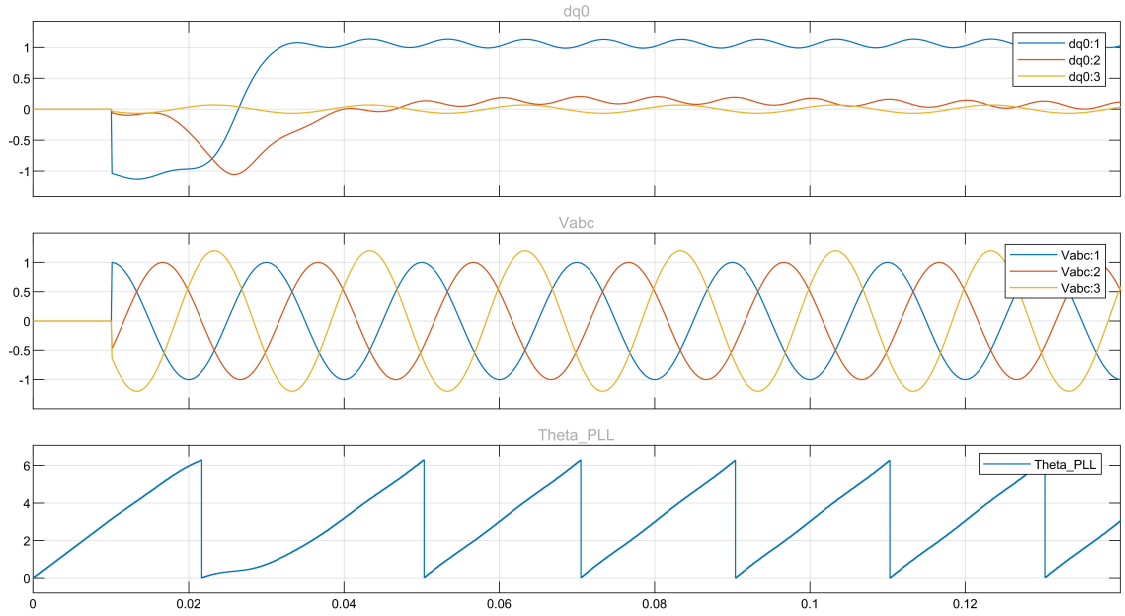


Figure 49: Simulation of the performance of the PLL used in this thesis for unbalanced three-phase input. The three-phase signal is delayed to create an initial phase shift between theta and the A phase. Inputs are all 50Hz.

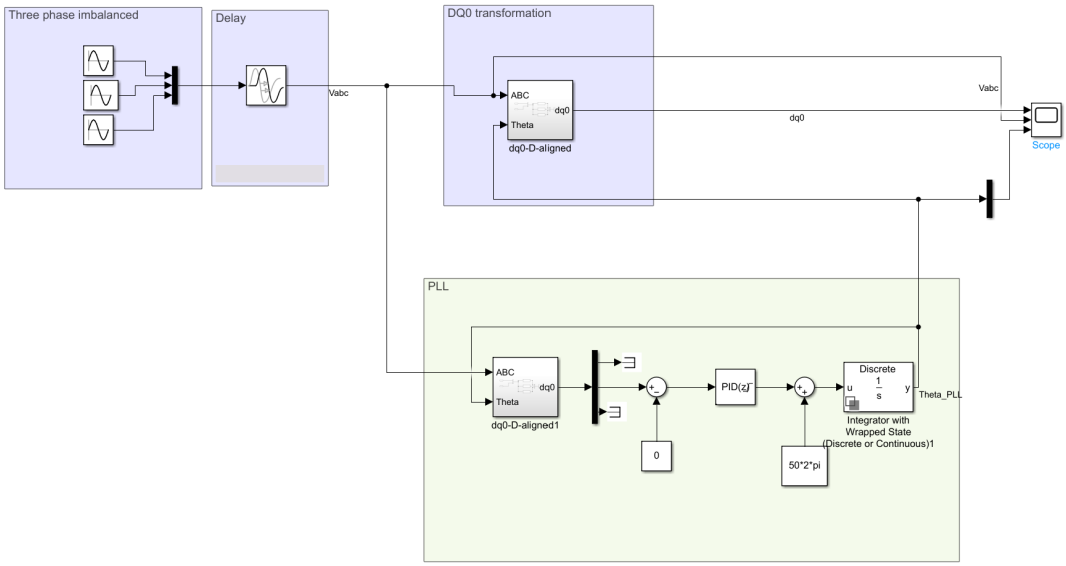


Figure 50: Simulation model for the performance test of the PLL used in this thesis for unbalanced three-phase input. The three-phase signal is delayed to create an initial phase shift between theta and the A phase. Inputs are all 50Hz.

B.2 Short circuit test of isolation transformer

Both measurements were taken on the primary side of the transformer. The configuration was star-star with the secondary short-circuited. The clamp meter used is a i1000s from Fluke and is rated for higher currents than the ones used here. They specify a maximum phase shift of 15° for current from 2-10A so it is fair to assume some significant phase shift is introduced in the 1A range.

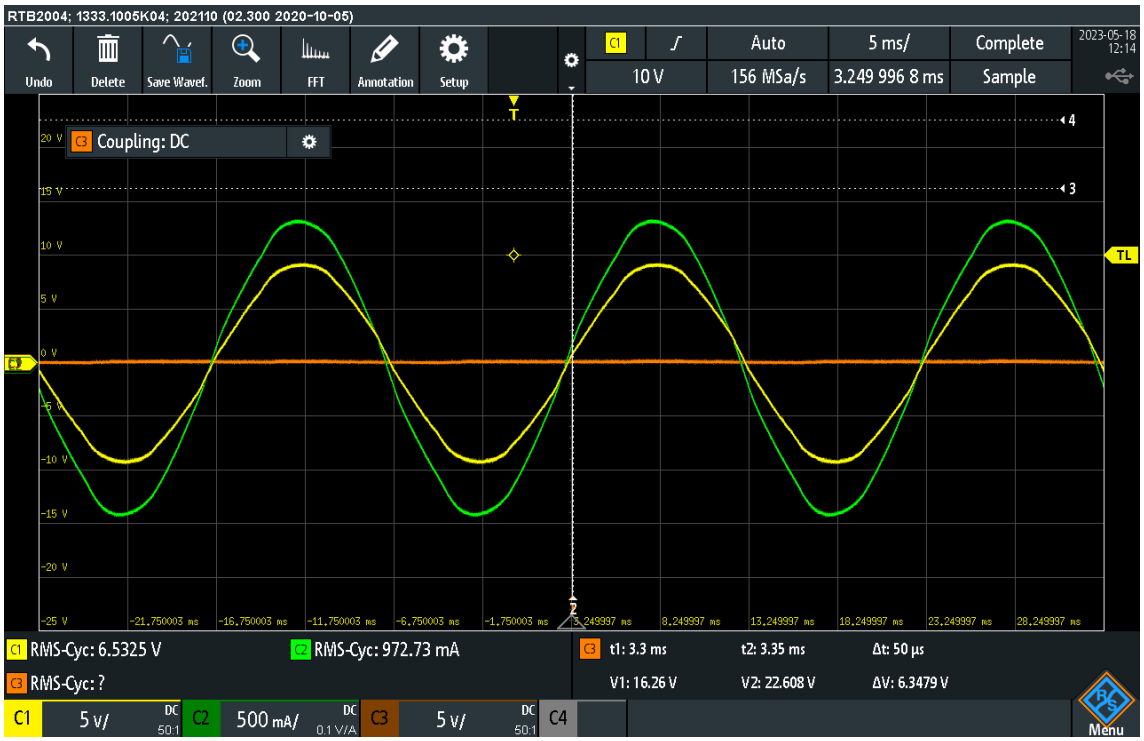


Figure 51: Oscillogram showing phase voltage (yellow) and phase current (green) during a short circuit test of the three phase isolation transformer.

B.3 Lab results with less aggressive tuning of the current controller

The system response when using the tuning constants $K_p = 0.2$ $K_i = 2$, displayed in Figure 53 showed accurate reference tracking with minimal overshoot. The bandwidth of the controller appears to be lower than with the original tuning (see Section 5.5.3), however still a fast enough settling time for the intended purposes. With tuning constants $K_p = 0.02$ $K_i = 0.2$ the system appeared to be marginally stable with oscillations that are neither converging nor diverging on the q-axis current. This is not a desirable system characteristic for our application.

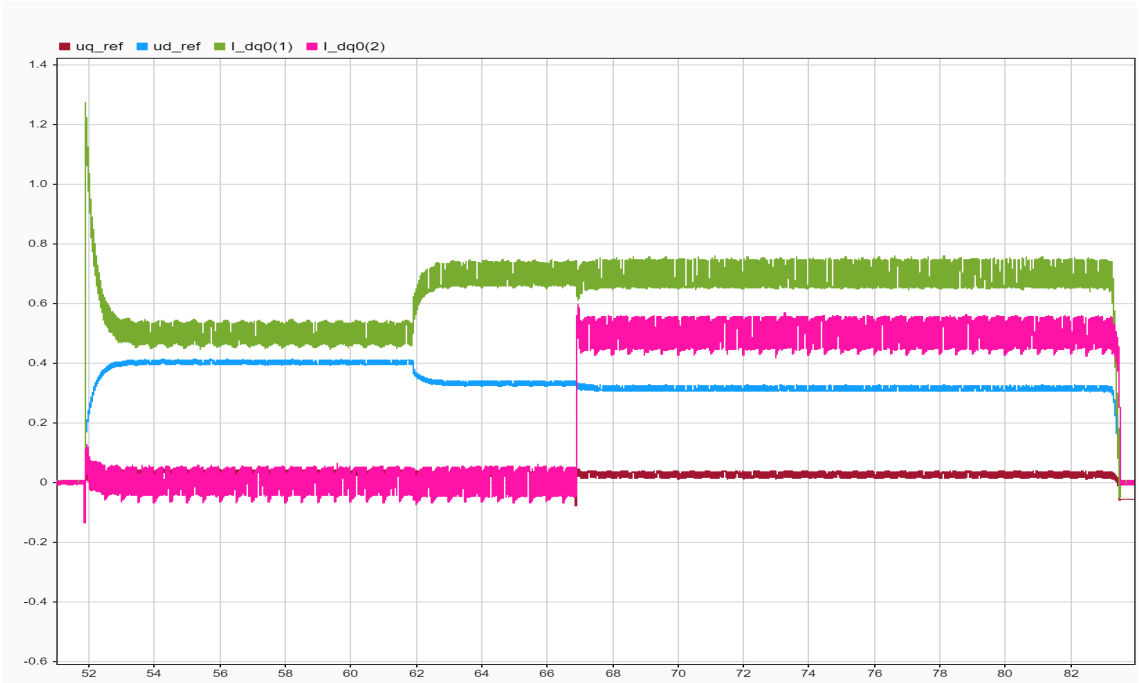


Figure 52: Plot showing d -and q-axis current, $idq(1)$ and $idq(2)$ respectively, being controlled from 0.5 to 0.7 pu and from 0.0 to 0.5 pu respectively. $K_p = 0.2$ $K_i = 2$. $ud - ref$ and $uq - ref$ is the current controller output in the dq0 plane.

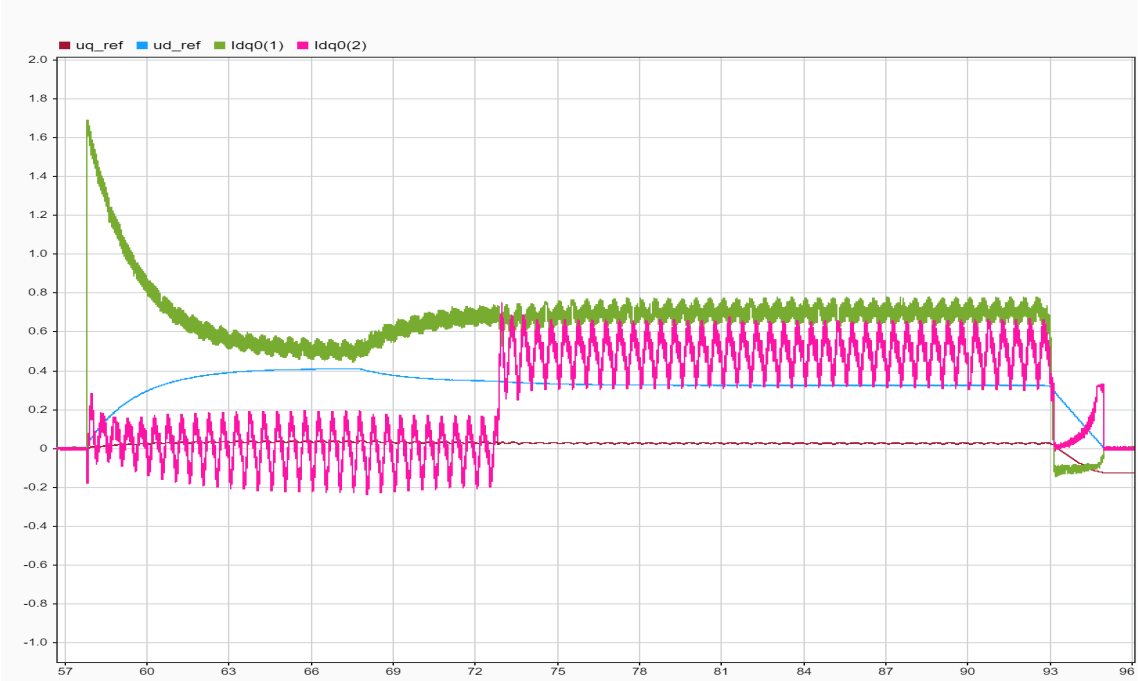


Figure 53: Plot showing d -and q-axis current, $idq0(1)$ and $idq0(2)$ respectively, being controlled from 0.5 to 0.7 pu and from 0.0 to 0.5 pu respectively. $K_p = 0.02$ $K_i = 0.2$. $ud - ref$ and $uq - ref$ is the current controller output in the dq0 plane.

B.4 Activation sequence two-module tests

Figure 54 shows the activation sequence of the voltage balancing operation used in the experiments presented in this thesis.

The step in DC-link voltage is necessary because it is a global signal that can be used to synchronize the isolated microcontroller. Because the microcontrollers can't intercommunicate a global trigger signal was needed.

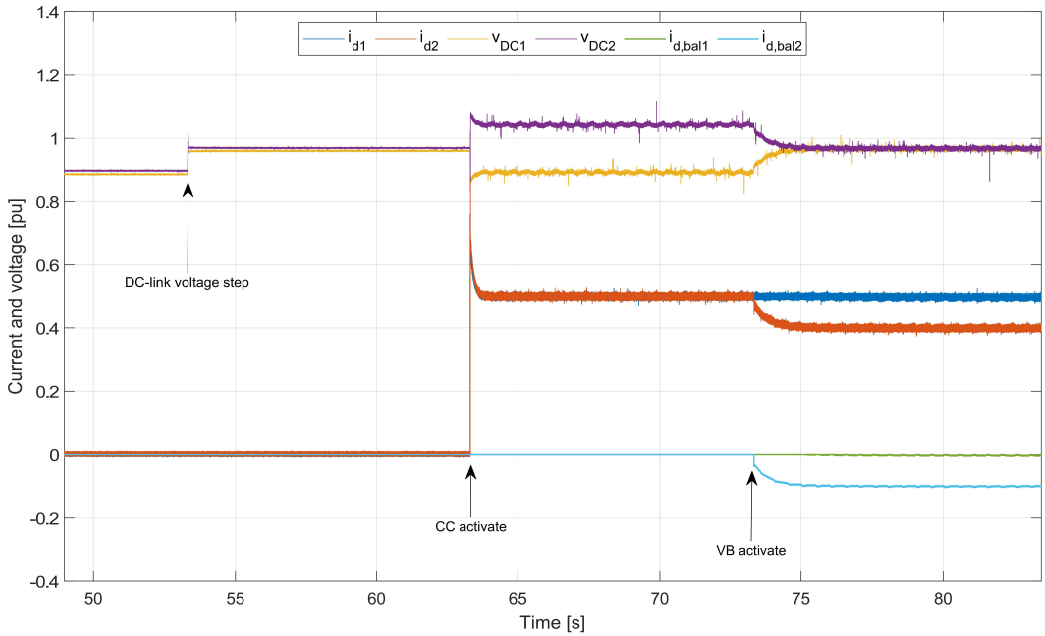
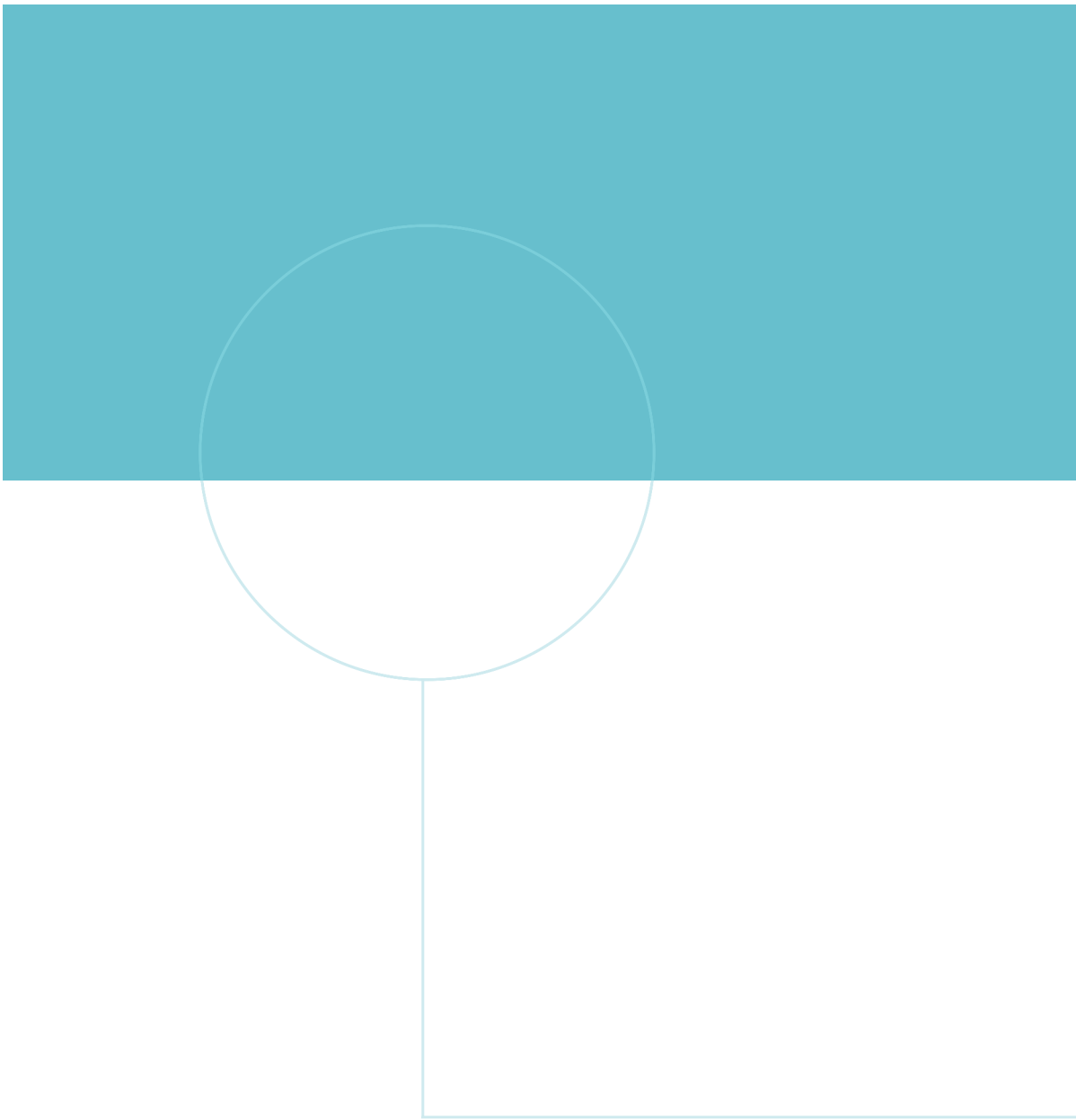


Figure 54: Plot of voltage balancing test results where the activation stages are clearly marked.



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