Master's thesis

NTNU
Norwegian University of Science and Technology
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Department of Electric Power Engineering

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Temperature Dependency and Active Gate Driver enabled Active Temperature Control of SiC Power MOSFETs

Master's thesis in Energy and Environmental Engineering
Supervisor: Dimosthenis Peftitsis
Co-supervisor: Daniel Alexander Philipps
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Preface

This master's thesis concludes the course TET4900 Electric Power and Energy Systems, Master's Thesis. It is written as the final segment of the five-year Master of Science programme Energy and Environmental Engineering, with a specialization in Electrical Energy Engineering and Smart Grids. The course accounts for 30 ECTs at the Norwegian University of Science and Technology (NTNU) at the Department of Electric Energy (IEL).

Embarking on this project has proven to be a challenging yet fulfilling journey. It has granted me the opportunity to cultivate my research, engineering, and troubleshooting skills across a diverse range of subjects, such as power electronics, control theory, and PCB designs. In its entirety, this project has been a valuable and influential experience. I hope this work will make a meaningful contribution to the existing research literature concerning reliability improvements of SiC MOSFETs

This thesis would not have reached this level without the support of my supervisors. I would like to acknowledge and express my sincerest gratitude to my Supervisor, Professor Dimosthenis Peftitsis, and Co-Supervisor PhD-Candidate Daniel Alexander Philipps. Dimosthenis Peftitsis has provided invaluable guidance and support throughout the project. He has always been available to clarify any doubts I may have had. I would also like to express my greatest appreciation for the support and guidance Daniel Alexander Phillips has provided throughout this project. The hours working in the lab with him have been pivotal in shaping this thesis, and the insights shared in lengthy discussions have been instrumental in my understanding of key theoretical concepts. I have greatly benefited from his generous commitment in time for this project to be successful.

I would like to thank NTNU for providing the software and the research group Power Electronic Systems and Components (PESC) at NTNU for access to the power electronics lab with all of its equipment. This thesis addresses subjects that share a connection with the research project Adaptive Silicon Carbide Electrical Energy Conversion Technologies for Medium Voltage Direct Current Grids (ASiCC) funded by The Research Council of Norway. I am very grateful for the investment made in the necessary components and materials that were essential for my progress and for accomplishing the objectives of this project.

Finally, I would like to thank my girlfriend and all of my friends and family for their encouragement and motivation throughout this semester.

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Trondheim, June 2023
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Abstract

SiC power MOSFETs are susceptible to thermal effects, which can impact their reliability due to thermal-mechanical stress at the layer interface. To mitigate this, methods for reducing junction temperature fluctuations during load changes can enhance the longevity and reliability of these devices. Active Gate Drivers (AGD) enable the manipulation of SiC power MOSFET conduction and switching behavior at run-time. This includes the switching losses that constitute a major part of the total device losses, especially moving toward higher switching frequencies for high power density converters. Thus, this relatively new approach could be used to implement Active Temperature Control (ATC), which shows promising effects in extending the estimated lifetime of SiC MOSFETs and improving system reliability.

This master's thesis aims to provide an extensive overview of the methodology for exploring the efficacy of a proposed ATC. This ATC is based on a virtual heatsink approach for generating a smooth control reference. To develop an accurate and realistic model of the SiC power MOSFET behavior at different operating temperatures, temperature-dependent characteristic data were obtained by means of a Power Device Analyzer. For this purpose, the design and implementation of a controllable synchronous buck converter to regulate the temperature of a heatsink to be used as a heating plate was successfully executed. Precise ID-VDS and transfer characteristics of a C3M0075120D SiC MOSFET from Wolfspeed at various temperatures were accomplished.

The obtained experimental characterization and switching-loss data of an equivalent SiC MOSFET from an AGD study provided the necessary basis for an electrical power-loss model. The junction temperature was estimated by integrating a thermal model of the given TO-247 package and an RA-T2X-25E heatsink from Ohmite. The ATC simulation results indicate a feasible 14.97% reduction in temperature fluctuations at a given load profile for examining the step-response, with minimal impact on the converter operation. The selection of control variables to optimize the switching performance of the SiC MOSFET is comprehensively discussed. Experimental validation of the proposed ATC is still missing to confirm its accuracy and viability.

Sammendrag

SiC effekt MOSFETer er sårbar mot termiske effekter, noe som kan påvirke påliteligheten deres på grunn av termomekanisk stress ved laggrensesnittene. For å dempe dette kan metoder for å redusere temperatursvingninger i overgangene under lastendringer forlenge levetiden og påliteligheten til disse komponentene. Aktive gate-drivere (AGD) gjør det mulig å manipulere SiC effekt MOSFETs ledningsevne og koblingsatferd ved kjøretid. Dette inkluderer koblingstap som utgjør en betydelig del av de totale komponenttapene, spesielt ved høyere koblingsfrekvenser for omformere med høy effekttetthet. Dermed kan denne relativt nye tilnærmingen brukes til å implementere aktiv temperaturkontroll (ATC), som viser lovende potensiale i å forlenge den estimerte levetiden til SiC MOSFETer og forbedre systemets pålitelighet.

Denne masteroppgaven har som mål å gi en omfattende oversikt over metodikken for å utforske effektiviteten til en foreslått ATC. Denne ATCen er basert på en virtuell kjøleribbe-tilnærming for å generere en jevn kontrollreferanse. For å utvikle en nøyaktig og realistisk modell av SiC effekt MOSFETens atferd ved ulike driftstemperaturer, ble temperaturavhengige karakteristiske data hentet ved hjelp av en Power Device Analyzer. Til dette formålet ble design og implementering av en controllerbar synkron buck omformer utført for å regulere temperaturen til en kjøleribbe som skulle brukes som en oppvarmingsplate. Presis ID-VDS og overføringskarakteristikker for en C3M0075120D SiC MOSFET fra Wolfspeed ved ulike temperaturer ble oppnådd.

De innhentede eksperimentelle karakteriserings- og koblingstapdataene for en tilsvarende SiC MOSFET fra en AGD-studie ga det nødvendige grunnlaget for en elektrisk tapsmodell. Den indre grensesnitt temperaturen ble estimert ved å integrere en termisk modell av den gitte TO-247-pakken og en RA-T2X-25E-kjøleribbe fra Ohmite. ATC simuleringsresultatene indikerer en mulig reduksjon på $14,97\%$ i temperatursvingninger ved en gitt lastprofil for å undersøke trinnresponsen, med minimal innvirkning på omformerens drift. Valget av kontrollvariabler for å optimalisere svitsjeytelsen til SiC MOSFETen blir omfattende diskutert. Eksperimentell validering av den foreslåtte ATCen mangler fortsatt for å bekrefte nøyaktigheten og effekten.

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List of Abbreviations

AGD	Active gate driver
ALT	Accelerated lifetime tests
ATC	Active temperature control
B	Boron
BJT	Bipolar junction transistor
CGS	Current-source driver
CPLD	Complex Programmable Logic Device
CTE	Coefficient of thermal expansion
DBC	Direct bonded copper
DUT	Device under test
EMI	Electromagnetic interference
FEM	Finite element models
HTGB	High-temperature gate bias test
HTRG	High-temperature reverse bias test
IGBT	Insulated-gate bipolar transistor

MOSFET	Metal-oxide semiconductor field-effect transistor
P	Phosphorus
PC	Power cycling
PCB	Printed circuit board
PECS	Power electronic converter systems
PWM	Pulse-width modulation
RUL	Remaining useful life
SCI	Serial communication interface
Si	Silicon
SiC	Silicon carbide
SiO_2	Silicon dioxide
TC	Temperature cycling
THD	Total harmonic distortion
TS	Thermal shock
TSEP	Temperature sensitive electrical parameter

1 Introduction

There is an expanding integration of Power Electronic Converter Systems (PECS) in applications that exhibit a stochastic load pattern [1]. This is seen in aspects such as the electrification and development of society, where PECS interface photovoltaics, wind power, electric traction technologies, industrial equipment and aerospace applications to either the power grid or each other [2, 3, 4, 5]. Higher power density in advanced power electronic applications has increased the chip area's current density, resulting in larger temperature variations [6]. As a response, this has put an emphasis on the long-term reliability concerns of power modules such as Silicon Carbide (SiC) Metal-Oxide Semiconductor Field-effect transistors (MOSFETs), to mitigate a failure due to thermally induced strain [7, 8]. Adapting emerging semiconductor materials, such as SiC, in power devices requires a deep understanding of the characteristics [9]. Especially the reliability concerns regarding the package degradation need to be addressed for a wide-scale integration in safety-critical utilities [10].

SiC possesses exceptional material characteristics for switching devices in power conversion topologies, particularly for integration in systems that demand a high power density and efficiency [11]. Key material properties, such as elevated thermal conductivity, higher critical breakdown field strength, and wider energy band-gap, are enhanced compared to the widely used semiconductor material, silicon (Si) [12]. Wide band-gap semiconductor such as SiC enables higher operating temperatures due to their higher thermal conductivity. However, this leads to a larger temperature gradient in the packaging design with larger temperature swings [6]. The dominant degradation mechanism for MOSFET packages is thermo-mechanical stress due to the mismatching coefficient of thermal expansion (CTE) of interfacing layers [13]. The junction temperature T_j and temperature fluctuation ΔT_j are identified as the governing parameters that determine the acceleration of damage accumulation due to CTE in MOSFET modules [14]. Varying load conditions encountered during operation are the principal source of ΔT_j [15]. Lowering the absolute value of the ΔT_j swings has an exponential effect on the estimated lifetime of power devices [16].

A notable increase in research efforts towards improving the reliability of power devices to overcome this issue of thermally induced degradation has persisted [17]. Active temperature control (ATC) is expressed as a viable method to increase the reliability and performance of power modules [18, 19]. A reduction of the repeated temperature swings amplitude can prolong the devices lifetime [20]. Therefore, ATC schemes could facilitate a more reliable operation of MOSFETs. Several ATC approaches have been proposed using control parameters that influence the temperature. Some examples are frequency control, specific modulation schemes, switching loss manipulation by slowing the switching transient, or feedback-controlled external cooling systems [21]. For this purpose, adaptive gate drivers are suitable for online switching loss manipulation, enabling nearly lag-free control over power losses and consequently facilitating temperature control [19, 20]. The development of adaptive gate drivers has generated novel opportunities in thermal control to mitigate large ΔT_j. In addition, the AGD facilitates monitoring of electrical parameters of interest and extracting state of health data of power modules supporting a predictive maintenance scheme [3].

Objective

The objective of this master's thesis is twofold. Firstly, the thesis aims to carry out an electro-thermal characterization of a SiC MOSFET, specifically by examining the impact of temperature on the transfer and ID-VDS characteristics. This objective will be accomplished through the design and implementation of a DC/DC converter incorporating a temperature control scheme. Secondly, this thesis seeks to investigate the performance and feasibility of an ATC framework employing AGD for power-loss manipulation. Utilizing the data obtained from the electro-thermal characterization to develop an accurate electrical power-loss model integrated into the ATC scheme, including the temperature dependencies.

Report structure

This thesis is structured as follows:

Chapter 2 - Theoretical foundation and literature, consisting of theory regarding the structure and operation of SiC MOSFETs, focusing on temperature dependencies. The theoretical foundation of lifetime estimation, failure modes, and aging factors is covered. These topics support the interest in investigating an ATC for ΔT_j reduction. Further, the chapter reviews details regarding various AGD topologies and their operation. The last part of the chapter provides a comprehensive introduction to thermal models and thermal control, with a brief summary of temperature estimation techniques.

Chapter 3 - Methodology for electro-thermal characterization of SiC MOSFET, gives a thorough overview of the experimental approach followed in this thesis. The chapter addresses the procedure of obtaining the transfer and ID-VDS characteristics of the SiC MOSFET at various temperatures. The design and implementation of a controllable synchronous buck converter for temperature control are given in detail.

Chapter 4 - Active temperature control framework, presents the control scheme and simulation model for reducing the ΔT_j caused by load variations. It describes the elements of this framework, namely the AGD, the electrical loss model, and the thermal model. Moreover, it presents the load variation profiles and two approaches for multi-variable optimization of the control variables.

Chapter 5 - Results and discussion, presents the findings from the electro-thermal characterizations and an analysis of the results. The simulation cases are outlined for the ATC scheme, and the corresponding results are presented and examined. A comprehensive assessment of the accomplishment of the objectives is provided.

Chapter 6 & 7 - Conclusion and further work, provides some concluding final remarks, summarises the discussion, and suggests potential directions for further work.

Contribution from earlier work

This master's thesis builds upon the work of the specialization project conducted fall 2022 [22] and of the Master's thesis of Halvor Bratvold Ekrem [23]. Some elements from the sections listed below are reused from the specialization project. Therefore, the content and structure share similarities. However, the material is fully reworked and refined for strengthened clarity and precision. Additional content is incorporated, whereas irrelevant material is excluded. The ATC framework, presented in Chapter 4 is based on the previous model design in the specialization project. This model is improved for greater accuracy and realism, integrating two approaches for control parameter selection and experimental data obtained in this thesis. Furthermore, changes in the thermal model, load profiles, and power-loss model are implemented. The following chapters contain some reused material from the specialization project that will not be directly cited further. The original sources of the material will be referenced in the thesis.

- List of abbreviations
- Chapter 1 Introduction
- Chapter 2.1-2.8 Theoretical foundation
- Chapter 4.1-4.4 Active Temperature Control framework
- Chapter 7 Further Work

In the work of Ekren et al. [24], a four-voltage level AGD was able to influence the switching transients. The AGD proved to be able to manipulate the switching losses at both turn-on and turn-off. The switching loss data and its given conditions will be applied and analyzed in the simulations of an ATC scheme. The AGD aspects will be treated in Chapter 4.1.

2 Theoretical foundation and literature

This chapter reviews and provides an overview of the principal theoretical foundation and research for this master's thesis. First, the chapter examines the structure and general properties of SiC MOSFETs, highlighting conduction characteristics, switching characteristics, and power-losses. Further, the chapter discusses the junction temperature role in MOSFET package degradation, elaborating on failure modes, aging indicators, lifetime estimation and condition monitoring.

To improve the lifespan of SiC MOSFET modules, ATC frameworks to counteract the degradation of junction temperature fluctuations are investigated. Focusing on the implementation of frameworks based on switching loss manipulation. Various AGD topologies and thermal modeling approaches of SiC MOSFET modules are reviewed. Finally, the chapter covers the challenges that arise in junction temperature control caused by temperature estimation, as well as temperature and aging effects on materials and operational parameters for SiC MOSFETs.

2.1 MOSFET structure and operation

Semiconductors

MOSFET as a power device is achieved by means of semiconductor materials. Semiconductors such as Silicon (Si) and Silicon carbide (SiC) typically exhibit a lattice structure that can be altered by injecting impurities to modify the free charge carrier density. Therefore, influencing the conductivity of the semiconductor material is achievable [25]. In the crystal structure of Si, some atoms will be temporarily ionized because of the thermal motion, generating a free electron and a hole. This thermal ionization mechanism enables the movement of electrons and the apparent movement of holes due to recombination. The number of holes and electrons generated by thermal ionization labeled n_i, will in equilibrium, be equal and can be described as [25]

$$n_i^2 = Ce^{\frac{-qE_g}{k_bT}}. \tag{1}$$

C is a proportional constant, E_g is the band gap energy difference between the valence band and the conduction band, q is the electron magnitude, k_b is the Boltzmann's constant and T is the temperature [25].

Dopants commonly used are Phosphorus (P) with five valence electrons, and Boron (B) with three valence electrons. The introduction of Phosphorous in the crystal structure generates a free electron, whereas Boron introduces an empty bond. At thermal equilibrium with impurities, the product of the number of free electrons n_o and free holes p_o will remain equal to the original product and can be formulated as [25]

$$p_o n_0 = n_i^2. \tag{2}$$

MOSFETs

MOSFETs are voltage-controlled power electronic devices that can be utilized as high-frequency switches in various topologies for power conversion and management [26]. The structure consists of layers of semiconductor material with induced impurities of appropriate concentration and three electrodes acting as terminals labeled Gate(S), Drain(D) and Source(S). The gate electrode illustrated by Figure 1 is surrounded by a thin insulating oxide layer interfacing the body region and drift region [25, 26]. The semiconductor regions are designed with a specific doping profile generating a desired concentration of acceptors and donors [25]. MOSFETs can be categorized as N or P-channel, determined by whether the conductive channel in the base region is generating a conductive N-channel in a P-region or a conductive P-channel in a N-region. Figure 1 illustrates a N-Channel MOSFET having a $N^+PN^-N^+$ structure [25]. An opposite doping profile is called a

P-channel MOSFET. Hence, for a N-Channel MOSFET, the majority carrier is electrons, whereas holes are the majority carrier in P-Channel MOSFET. This is indicated by the arrow direction in the circuit symbol at Figure 2 [25].

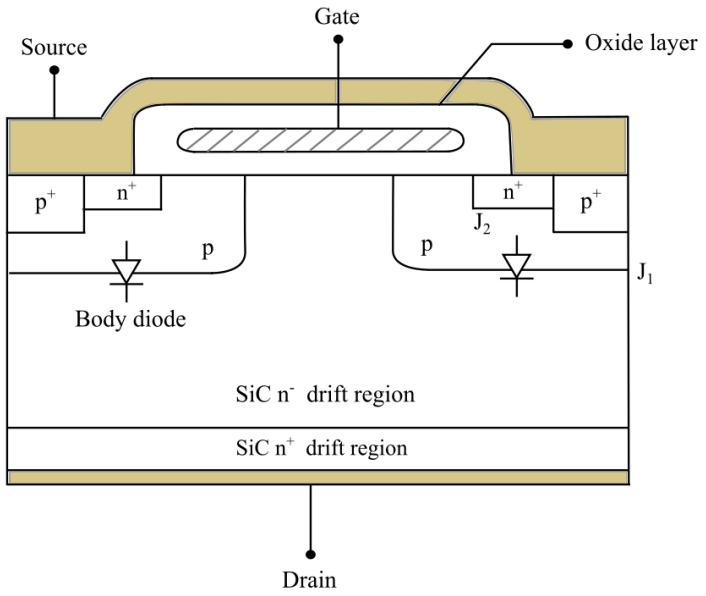


Figure 1: Overview of a cross-section of the cell structure for an N-Channel SiC MOSFET. Illustrating the doped regions and the terminals gate, drain, and source. Drawing is based on [8, 26].

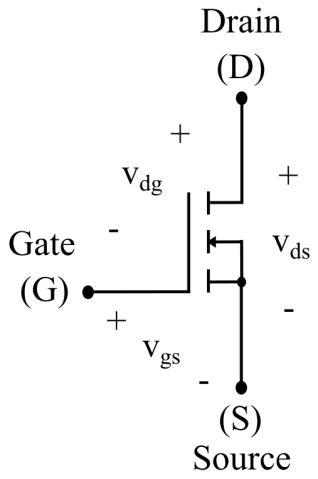


Figure 2: MOSFET circuit symbol for an N-Channel type, with the gate (G), drain (D) and source (S) locations, based on [25].

Structure

Illustrated in Figure 1, the structure of a cross-section of a MOSFET cell depicts two pn-junctions, J_1 and J_2. The N^+PN^- structure forms an internal bipolar junction transistor (BJT). To repress this parasitic BJT, a short-circuit of the J_2 junction is typically utilized by creating an overlap of the N^+ and P-body region to the source. This results in the presence of an intrinsic body diode at the J_1-junction [25, 26]. The N^- drift region is usually lightly doped to enhance the blocking voltage, and it primarily determines the on-resistance $R_{ds,on}$ and blocking voltage of the MOSFET [25, 26]. This intrinsic diode may be used as a freewheeling diode in topologies such as the half-bridge converter [25].

MOSFETs can be packaged as either discrete devices or as modules of parallel devices. As depicted in Figure 3. The package structure comprises single or multiple MOSFET dies in parallel soldered to a direct copper bonding (DCB) substrate. This substrate is designed to have good thermal conductivity while simultaneously acting as an electrically insulating layer to the baseplate and cooling system [17, 27].

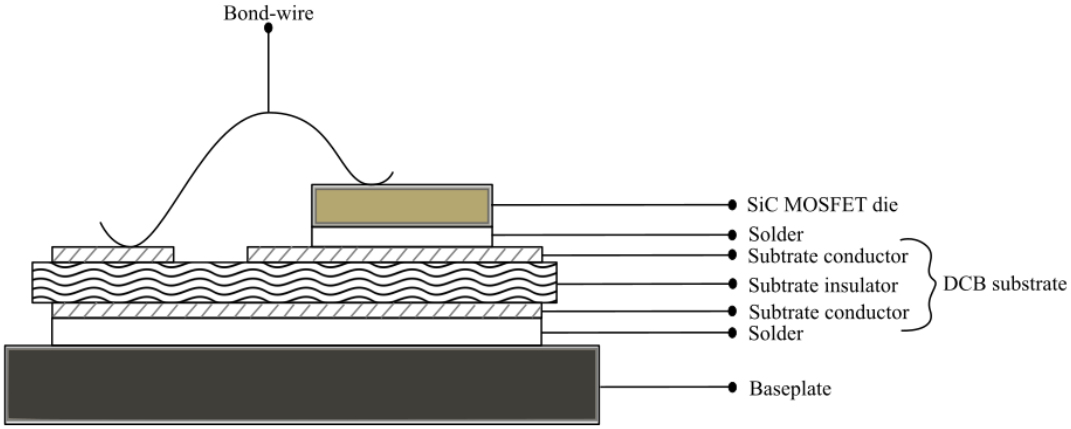


Figure 3: Vertical cross-section of a SiC MOSFET package structure. Reconstructed figure based on [8, 17].

Operation and device physics

The general operating principle of N-channel MOSFETs is that an applied voltage of sufficient magnitude over the gate-source terminals v_{gs}, with a positive bias, will produce a conductive channel at the surface of the body region and oxide layer [26]. This occurs when the electric field strength over the insulating oxide layer is of sufficient value. This is due to the gate structure acting as a capacitor, where charge accumulation on the gate terminal demands a negative charge accumulation at the lower electrode, the oxide-P surface region. This forms a depletion layer that will grow in width, determined by the applied v_{gs}. A charge accumulation at the interface of the body and insulator reaches a magnitude where the conductive channel is formed while simultaneously repelling majority-carrier holes. This channel is called the inversion layer and is a highly conductive path due to the high concentration of free electrons. The specific v_{gs} where the inversion channel is able to conduct current is known as the threshold voltage $V_{gs,th}$ [25].

MOSFETs can be grouped into two types, depletion and enhancement type. The depletion type is normally on and requires a negative bias gate-source voltage v_{gs} for inversion layer removal and turning the device off. Whereas, enhancement type only conducts when $v_{gs} > V_{gs,th}$ [6].

Silicon Carbide vs Silicon

SiC MOSFETs feature some clear advantages over Si MOSFETs in terms of higher breakdown voltages and lower on-resistance due to the wide energy band-gap of SiC [28, 12, 29]. In addition, the higher electron mobility, combined with the possibility to reduce the device size, lowers the parasitic capacitance and enables higher switching speeds [12]. The low on-state conduction due to the on-resistance and switching losses as a result of the fast switching speed makes SiC MOSFETs an attractive choice for high switching frequency operations. However, it is still affected by the cost of worse electromagnetic interference (EMI) due to the rapid voltage and current transients compared to Si [30]. Nevertheless, SiC MOSFETs can yield improvements in efficiency and in power densities, thereby potentially achieving reductions in device package dimensions compared to the Si counterpart [12, 29, 31].

SiC has a substantially greater thermal conductivity and higher melting point compared to Si, this makes the device more efficient at dissipating heat [12]. However, this implies a larger temperature

gradient. As a result, SiC MOSFETs are expected to experience larger temperature fluctuations ΔT_j and internal temperature variations [32]. The reliability of SiC in high-temperature conditions and specific thermal profiles is still uncertain, particularly due to the packaging materials and techniques for die-attachment [12, 13, 27]. Moreover, their higher cost and reliability issues under high-temperature operations do still need to be addressed [12].

2.2 Conduction and switching characteristics

Current-Voltage Characteristics

Further on, it is referenced to an N-channel enhancement type MOSFET. MOSFETs are unipolar devices. Therefore it operates in the first quadrant or conducts through the intrinsic diode in the third quadrant visualized in Figure 4 [6]. The four operation states are the ohmic-region, cutoff-region, active-region, and the avalanche-region [25]. The ID-VDS curves describe how the channel region is behaving at different states [26].

- Cutoff-region - In this region, the MOSFET is not conducting any current due to the applied $v_{gs} < V_{gs,th}$ indicating no conductive channel has been formed through the base region. As long as the drain-source voltage is lower than the breakdown voltage $v_{ds} < BV_{dss}$, no breakdown occurs [6, 25, 26].
- Active-region - During switching, the MOSFET typically traverses the active-region. This region is characterized by the drain-current i_d being solely dependent on the gate-source voltage, hence independent on the drain-source voltage v_{ds}. Significant power dissipation is expected due to a higher v_{ds} and a large current i_d occurring simultaneously [6, 25, 26].
- Ohmic-region - $v_{gs} - V_{gs,th} > v_{ds} > 0$ When the applied gate voltage is larger than the drain-source voltage, the MOSFET is driven into the ohmic-region. This region is characterized by low power dissipation and a linear dependency on the drain-current and drain-source voltage, described by $R_{ds,on}$. The boundary between the active and the ohmic-region can be derived as $v_{gs} - v_{gs,th} = v_{ds}$ [6, 25, 26].
- Avalanche-region - If the drain-source voltage increased beyond the breakdown voltage $v_{ds} > BV_{dss}$, an avalanche occurs over the J_2 junction and the drain-current rises exponentially, indicating a non-reversible breakdown [6, 25, 26].

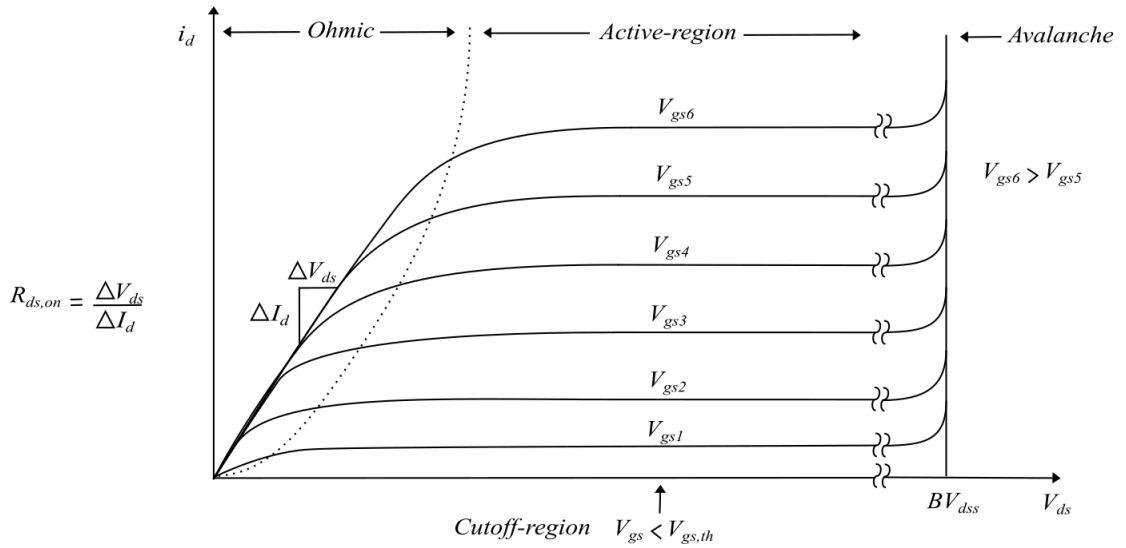


Figure 4: The ID-VDS characteristic for a MOSFET [25].

Transconductance g_m is a parameter describing the rate of change of i_d with respect to v_{gs} as illustrated in Figure 5. A large g_m is favorable, indicating a high drain-current sensitivity i_d to incremental steps in V_{gs}, facilitating higher switching speeds [26, 33]. However, a large g_m increases the i_d and v_{ds} overshoots [9].

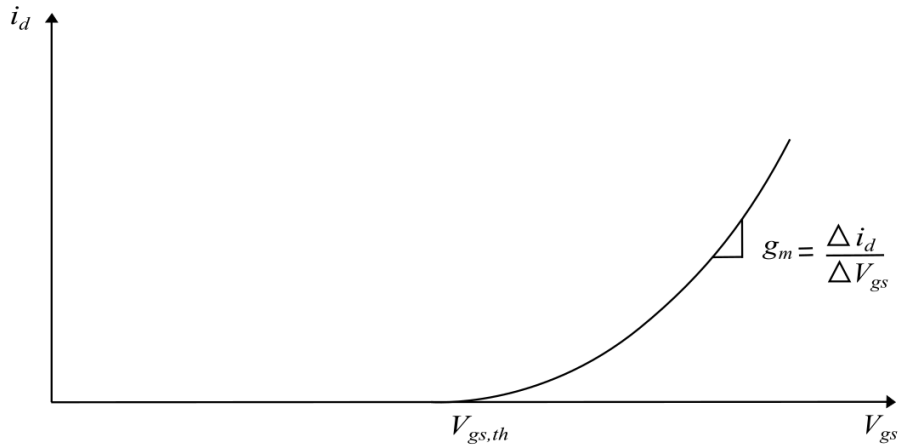


Figure 5: The transfer characteristic for a MOSFET based on [9].

The threshold voltage $V_{gs,th}$ is specifically temperature sensitive and will shift the transfer characteristic towards the left with a steeper curve [9]. This temperature dependency of $V_{gs,th}$ can be explained by the equation

$$V_{th} = \frac{\sqrt{4\epsilon_s k_b T N_A ln(N_A/n_i)}}{C_{ox}} + \frac{2k_b T}{q} ln\left(\frac{N_A}{n_i}\right). \tag{3}$$

Where ϵ_s is the SiC dielectric constant, k_b is Boltzmann's constant, T is the temperature, N_A is the P-base region doping concentration, n_i is the carrier concentration, q is the charge magnitude and C_{ox} is the oxide capacitance [9, 26].

The $V_{gs,th}$ for SiC power MOSFET structures have a negative temperature coefficient due to the increase in the intrinsic carrier concentration n_i at elevated temperatures, counteracting the apparent positive effect of the temperature T in equation (3) [26]. In the sensitivity study of Do et al. [34] the positive temperature coefficient of g_m and the negative temperature coefficient $V_{gs,th}$ are clearly evident.

Parasitic capacitance and inductance

As discussed in the previous sections, the MOSFET is a nonlinear power device. The internal capacitance between the three terminals and parasitic inductances impacts the transient switching behavior of the MOSFET [25, 26, 35]. The parasitic capacitances is shown in Figure 6. These capacitances are highly voltage-dependent [25]. Typically, three capacitance are referred to in the datasheets the input capacitance C_{iss}, the output capacitance C_{oss} and the feedback capacitance C_{rss} described as [35]

$$\begin{aligned} C_{iss} &= C_{gs} + C_{gd} \\ C_{oss} &= C_{ds} + C_{gd} \\ C_{rss} &= C_{gd}. \end{aligned} \tag{4}$$

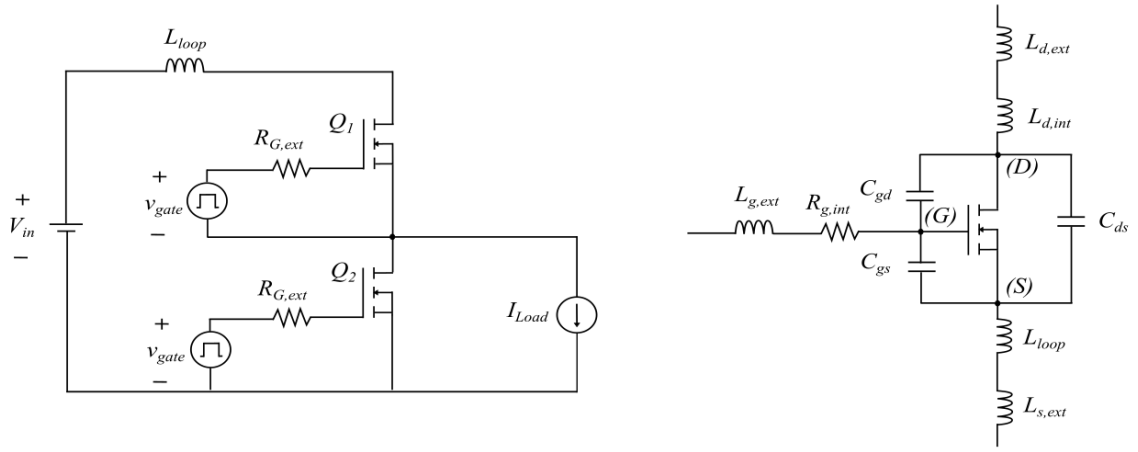


Figure 6: Parasitic inductances and capacitance location at the MOSFET terminals, with a half-bridge topology driving an inductive load for illustrative purposes. Drawing based on [35].

Parasitic inductances influence the switching behavior by limiting the rate of current change and giving rise to overvoltages and oscillations. The presence of these parameters imposes limitations on the switching speed of power MOSFETs. Consequently, this leads to considerable switching losses and demands larger safety margins to prevent voltage overshoots [25, 35].

The coupling effect of the intrinsic capacitances and stray inductances may cause oscillations in current or voltages, a phenomenon known as ringing. Oscillations can have adverse effects, such as electromagnetic interference (EMI) with other devices components or exceeding rated thresholds. This can cause reliability and stability issues. Therefore, it could be important to factor in these oscillations in the circuit designs, in addition to tuning the driver to prevent significant voltage and current overshoots to ensure secure and consistent operation [25, 36].

Switching characteristics

The MOSFET is often used in inductive circuits. Therefore, a diode-clamped inductive circuit model is typically used to examine the switching waveforms [25, 26]. For the MOSFET to turn-on, the parasitic capacitance C_{gs} must be charged. As illustrated in the Figure 7, v_{gs} climbs until it reaches the Miller plateau at a time-constant equal to the RC-circuit of R_g and a parallel connection of C_{gs}, and C_{gd}. The Miller plateau refers to the interval of clamped v_{gs} that appears during the switching transient shown in Figure 7. This constant V_{gs} region occurs as a result of the interconnection between the gate-drain capacitance C_{gd} and gate-source capacitance C_{gs} operating in parallel and the resulting non-linearity due to the voltage dependency on v_{ds}, which creates a negative feedback effect. In the instance when the drain current i_d flows through the channel, incremental increases in v_{gs} cause a displacement current i_{gd} being drawn from i_g. This results in a net-zero charge accumulation over C_{gs}. Consequently, $i_{gs} = 0$, and the gate-source voltage v_{gs} is clamped until v_{ds} falls after i_d carries the full load current. In this instance, the displacement current i_{gd} becomes insignificant and v_{gs} continues to climb exponentially until it reaches the applied driving voltage V_{gg}. [25, 30]. Therefore, the magnitude of the gate current i_g and the input capacitance C_{iss} are pivotal in determining the switching speed [37]. When turning off the MOSFET, the sequence reverses [25]. In the turn-off transient, an overshoot in v_{ds} may occur, caused by the rapid current change di/dt through the stray inductances [35].

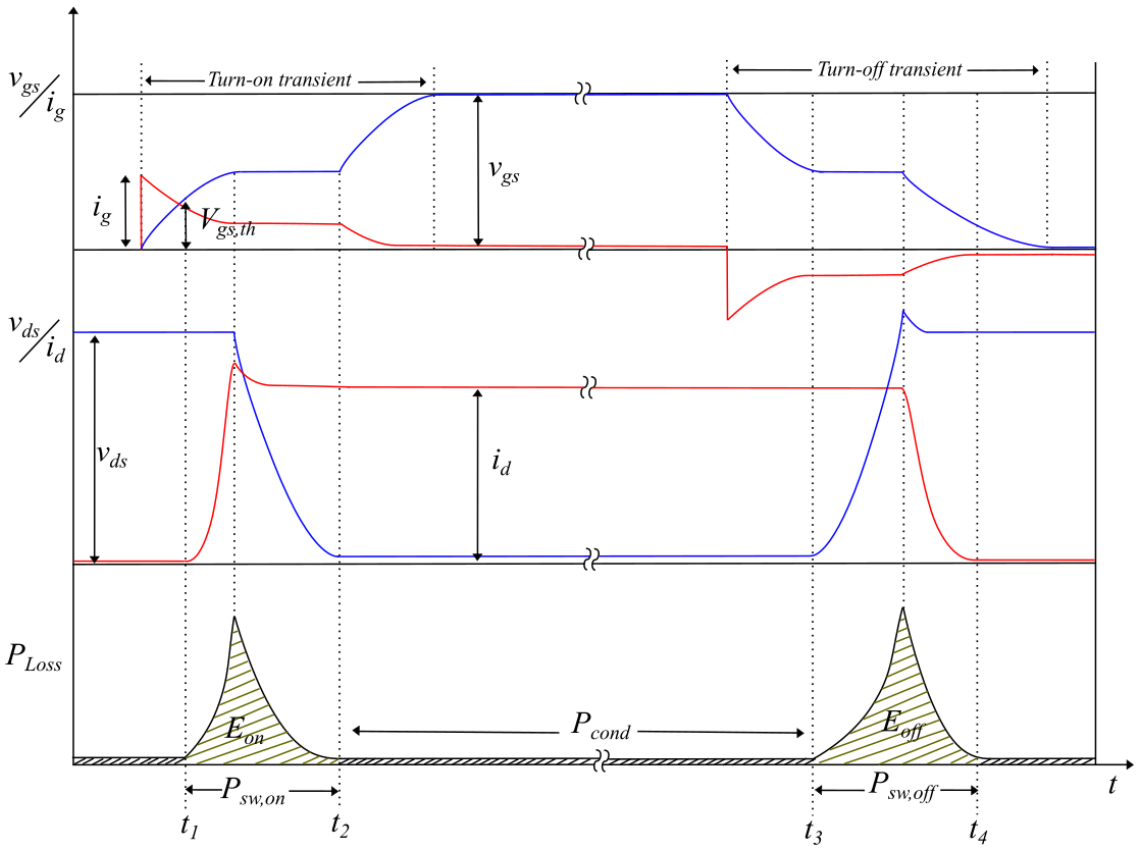


Figure 7: Switching and loss characteristics for a MOSFET. Recreated drawing based on [38].

Crosstalk

The half-bridge configuration illustrated in Figure 6 is a simple topology and building block of converters, Sometimes referred to as a phase-leg configuration when part of a full bridge or three-phase converter [39]. The floating voltage of the common node can cause problems arising from the upper MOSFET's floating source voltage and the direct coupling between the lower and upper MOSFETs [40]. During the switching transient, the discharge of charge from the parasitic capacitance C_{gd} in one switch can induce a voltage potential at the complementary gate-source terminal. As a result, this effect limits the switching speeds of MOSFETs in a phase-leg topology [40]. This interference phenomenon is known as crosstalk, which can accidentally trigger a wrongful switching response and cause a short-circuit of the half-bridge configuration in the case of a positive induced gate voltage v_{gs} [40]. In the case of a negative induced voltage, the gate structure may also be damaged if it surpasses the rated values [39, 41]. The switching devices, in this case, the adjacent SiC MOSFETs gate circuitry, interact with each other during turn-on and turn-off. SiC MOSFETs are more susceptible to cross-talk due to their lower $V_{gs,th}$ and inferior negative breakdown voltage tolerance, as well as their tendency to be exposed to higher di/dt and dv/dt compared to Si MOSFETs [35, 39].

2.3 Power-losses

The total power dissipation can be described as the sum of the switching losses and conduction losses when neglecting the blocking losses. This can be defined as [6]

$$P_{Tot} = P_{cond} + f_{sw}(E_{on} + E_{off}). \tag{5}$$

where P_{cond}, f_{sw}, E_{on} and E_{off} are the conduction losses, the switching frequency, and the switch-

ing energy loss at turn-on and turn-off respectively. Figure 7 illustrates these switching energies and conduction losses [38].

Conduction losses

As previously mentioned, the intrinsic resistance during turn-on $R_{ds,on}$ is lower for SiC compared to Si. The resistance depends on the geometric coefficients and the breakdown voltage. This leads to a compromise between high-voltage operation and efficiency [25]. In a MOSFET the conduction losses can be estimated as the ohmic losses caused by $R_{ds,on}$ and visualized in Figure 7. It can be represented as [6, 25]

$$P_{cond} = \frac{1}{T_{sw}} \int_0^{T_{sw}} R_{ds,on} \cdot i_d^2(t)\, dx = R_{ds,on} \cdot i_{d,RMS}^2. \tag{6}$$

T_{sw} is the switching period, corresponding to the full-time interval from a turn-on to the subsequent turn-on, and $i_{d,RMS}$ is the RMS drain current. The $R_{ds,on}$ in SiC MOSFETs possesses a positive temperature coefficient. Additionally, a positive temperature coefficient for $R_{ds,on}$ allows for multiple power MOSFETs to be connected in parallel to enhance the power-handling capacity. Thus, it establishes that the total current is shared effectively. Overall, this characteristic ensures that the device operates reliably under varying temperatures and load conditions [25, 26].

Switching losses

The switching losses can be estimated as the product of v_{ds} and the i_d during the switching transient. As previously presented in the switching characterization, there is a period during turn-on and turn-off, where v_{ds} and i_d both are of a significant magnitude. This is illustrated as the area during the switching event in Figure 7, therefore the energy loss for each transient can be expressed as [6]

$$E_{on} = \int_{t_1}^{t_2} v_{ds}(t) \cdot i_d(t)\, dt. \tag{7}$$

$$E_{off} = \int_{t_3}^{t_4} v_{ds}(t) \cdot i_d(t)\, dt. \tag{8}$$

$t_1 - t_2$ and $t_3 - t_4$ correspond to the start and end of the aforementioned periods seen at Figure 7. The switching losses exhibit a positive temperature coefficient, similar to the conduction losses as seen in the datasheet for the device under test (DUT) in this thesis, SiC MOSFET C3M0075120D from Wolfspeed [42].

2.4 Aging mechanisms and indicators

Power devices were identified as the most vulnerable component in PECS [43]. Hence, the importance of power devices reliability is put forth due to degradation influencing the system performance. The primary stressor is temperature and temperature cycles [44]. Power device failures are typically the result of fatigue, which can be classified as package and chip-related failures [5].

For SiC MOSFETs packaging, the primary cause of aging is thermal-mechanical stress at the interconnecting junctions [13]. As mentioned, SiC MOSFETs consist of a layered structure. Consequently, the mismatching coefficient of expansion (CTE) of materials deployed in the module generates shear stress at the interface when exposed to temperature cycles [13, 44]. Due to a higher Young's Modulus in SiC compared to Si, this stress is elevated by the lower elasticity [5]. This thermal-mechanical stress is primarily driven by load variations and ambient temperature

fluctuations [32]. Failure mechanisms such as solder fatigue and bond-wire lift-off are the two most critical failure modes resulting from the mismatch of the CTE [6, 13, 14, 44]. The locations where failure modes such as bond-wire lift-off and die-solder delamination occur are illustrated in Figure 8. This is in the interconnections where the SiC dies are attached by means of solder to the DCB substrates or aluminum bond-wires [13, 44]. The degradation of bond-wires is primarily influenced by rapid thermal cycling stress. In contrast, ambient temperature variations with slower dynamics have a more noticeable impact on the die-solder surface [32]. Humidity, vibration, and contamination could be noticeable factors influencing the RUL [45].

To counteract this effect, trade-offs to performance have to be made in the design or reinforcement of the structure [46, 44]. Danfoss Bond Buffer Technology is an example of a developed solution to reduce the thermo-mechanical stress caused by CTE at the top side of the packaging. Using a thermal buffer to even out the heat transfer improves the bond-wire connection's reliability [47].

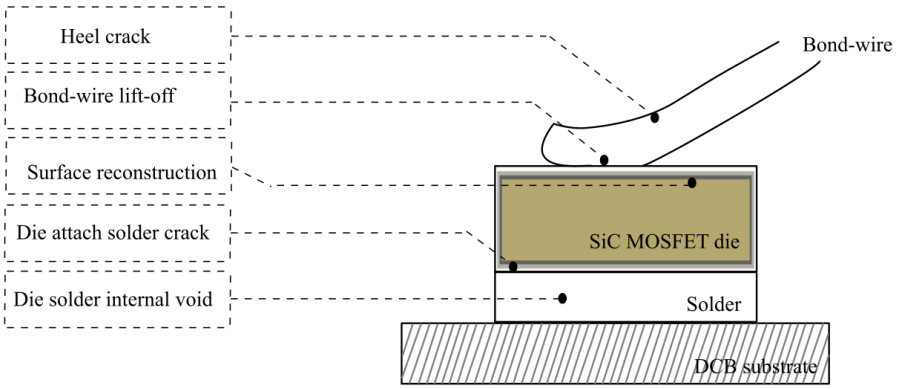


Figure 8: MOSFET Package structure with common failure modes indicating the specific areas. Based on [13].

Chip-related failures are frequently caused by gate-oxide degradation due to repetitive electric field stress causing a dielectric breakdown of the insulating SiO_2 layer [5]. A thin SiO_2 layers are employed in SiC MOSFETs to achieve acceptable $V_{gs,th}$ and g_m in comparison to Si MOSFETs due to the wider band-gap and higher doping concentrations in the P^+ region [13]. Furthermore, SiC's crystal structure inherently generates defects at the interface to SiO_2, causing a varying $V_{gs,th}$ [13]. If no parallel external Schottky diode is present, the intrinsic PiN body diode is vulnerable in third quadrant operations during the off-state when exposed to high reverse recovery currents. Stacking faults might result in bipolar degradation of the body diode, increasing both the forward diode voltage V_f and $R_{ds,on}$ [5].

Accelerated lifetime test

Accelerated lifetime tests (ALTs) are a methodology to determine the correlation between aging indicators trends, parameter shifts, and fatigue accumulation. Consequently, an approach for identifying any precursors to potential failure [48, 49]. ALTs are an approach for generating new lifetime models or for assessing their validity [17, 50]. To obtain valuable data for creating lifetime models, carefully designed accelerated cycling tests must be performed that can distinguish the various failure modes. This requires the definition of appropriate failure criteria [44]. Due to the focus of this thesis on the temperature-induced effects, two ALTS will be presented, accelerated power cycling (PC) and Accelerated Temperature Cycling (TC). The ALTs inducing degradation in the chip, High-Temperature Gate Bias test (HTGB) [17] and High-Temperature Reverse Bias test (HTRG) [17] will not be covered in this thesis.

Accelerated Power Cycling (PC) tests are conducted with the intention of causing bond-wire degradation or chip-solder degradation [17, 44]. This is achieved by inducing temperature cycles caused by defined conduction and cooling intervals. The heat dissipation origins from the die.

Therefore the close adjacent material layers, such as bond-wires connections or die-soldering are subjected to large changing temperature gradients [44]. Power cycling (PC) tests require failure analysis due to the interdependency of the failure modes [6, 17].

Accelerated Temperature Cycling (TC) tests purpose is to focus on the larger area interfaces such as DCB/Baseplate interconnection. The tests utilize temperature-controlled chambers to inflict ambient temperature variations on the power modules [44]. Thermal shock (TS) is a test method similar to TC, but it employs longer temperature cycles to ensure that the temperature in the power modules remains uniform [17]. PC tests are generally preferred over TC or TS tests for recognizing and characterizing aging indicators and lifetime estimation. This is because the PC tests have a more realistic profile than TC and TS tests [5].

Aging indicators

Some operational parameters of MOSFETs could be employed as indicators of aging due to their shift when degradation occurs, facilitating condition monitoring of the device [51]. $V_{gs,th}$ and gate leakage current I_{gss} are widely accepted aging indicators of chip-related degradation, having the tendency to increase due to gate-dioxide degradation [5]. $R_{ds,on}$ and the body diode forward voltage V_f are also indicators for chip aging. However, they are influenced by package degradation, so they should be examined together with other indicators [5]. The presence of an antiparallel diode in conjuncture with the MOSFET may limit the effectiveness of V_f as an aging indicator [13].

An increase of V_f or $R_{ds,on}$ could indicate a bond-wire lift-off [5, 44]. In addition, a rising $R_{ds,on}$ may indicate surface reconstruction [5]. An increase in the thermal resistance from junction to case $R_{th,j-c}$ can indicate solder fatigue, resulting from the propagation of cracks in the solder interface junction. The compromised heat conduction path of the semiconductor chip to the baseplate heatsink implies aging of the package structure [6, 44, 52]. Precise knowledge of the temperature is essential for distinguishing whether the shift in the aging indicators is due to aging or caused by elevated temperature [50]. Moreover, $V_{gs,th}$ and $R_{ds,on}$ of mass-produced SiC MOSFETs tend to exhibit greater variability compared to Si MOSFETs [50].

2.5 Lifetime estimation and condition monitoring

A major concern for a widespread adaptation of SiC MOSFETs is the ruggedness of SiC devices and their reliability, specifically when exposed to high temperature, repetitive short-circuit stress, and power cycling [10, 13]. Therefore, a broad integration of SiC MOSFET in safety-critical applications has put a focus on RUL prediction [10, 17]. An accurate prediction of SiC MOSFETs RUL and state of health could from a system point of view support maintenance scheduling and promote preemptive actions to avoid unanticipated failures. As a result, this could enhance system-level predictability and reliability [1]. Due to the uncertainty in the failure rate, statistical methods are employed to identify certain parameters for the different failure modes, such as the aging indicators presented, and to derive empirical lifetime models [17]. Figure 9 illustrates how the lifetime estimation could be implemented based on thermal-mechanical degradation due to PC [53]. This flowchart visualizes lifetime estimation based on a specific mission profile, generating a T_j profile. Classification and counting temperature cycles using cycle counting algorithms provide the data basis for empirically derived lifetime models. Accumulated damage models are employed to obtain the resulting figures for inflicted damage and lifetime estimation [53].

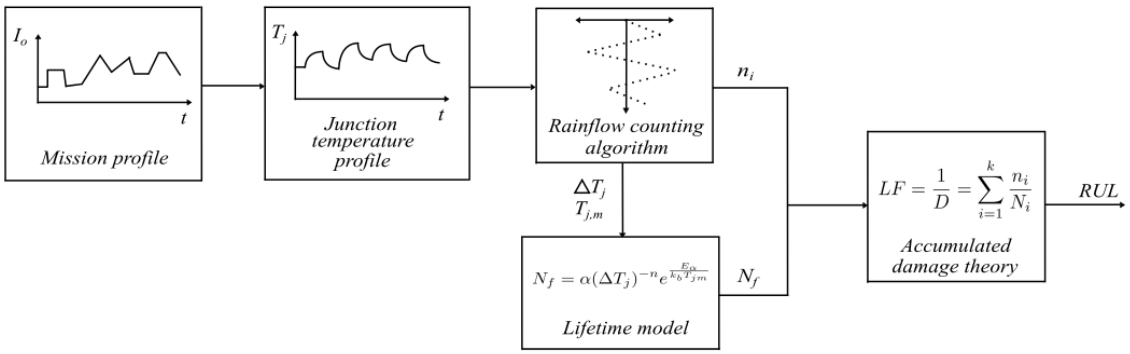


Figure 9: Flowchart to achieve lifetime estimation. Illustration is based on [53, 54].

Rainflow counting algorithm

Realistic load profiles may cause junction temperature fluctuations with varying frequency f, amplitude ΔT_j and mean temperature T_m [55]. To decompose the T_j cycles and categorize them, an algorithm such as the Rainflow Counting Algorithm can be utilized. This algorithm counts, classifies and organizes temperature cycles based on their ΔT_j and T_m [55, 56]. Thus, providing data useful for application in lifetime estimation models. Alternative cycle counting algorithms for the purpose of categorizing and examining temperature variations in SiC MOSFETs are Level Cross Counting, Peak Counting, and Simple Range Counting [8]. The Rainflow Counting Algorithm is the most widely utilized [8].

Physics of failure lifetime models

For describing the ΔT_j effect on the longevity of power devices, various lifetime model-based methods have been developed empirically on temperature cycles characterization [8]. Four-lifetime models will be presented, from the simplest to the more complex. The simple Coffin-Manson model estimates the lifetime of aluminum (Al) bond-wire to Si devices attachment with respect to ΔT_j and is represented as [57]

$$N_f = \alpha(\Delta T_j)^{-n}. \tag{9}$$

α and n are parameters obtained from curve fitting from experimental data. It should be noted that the Coffin-Manson model is only precise for predicting the consumed lifetime of materials and devices under temperature cycles with a temperature of $120°C$ or lower [53]. The Coffin Manson model is a precursor and basis for multiple power cycling lifetime models. These models estimate the number of cycles to failures N_f for specific ΔT_j [17]. Particularly ΔT_j has a dominant effect on N_f compared to the mean temperature T_m [16] for IGBT modules. However, T_m is still of significance. An improved model using the Arrhenius factor describes how the mean temperature induces an acceleration to the number of cycles to failures, which can be expressed as [57]

$$N_f = \alpha(\Delta T_j)^{-n} e^{\frac{E_\alpha}{k_b T_{jm}}}. \tag{10}$$

T_m is the mean junction temperature, k_b is the Boltzmann constant, and E_a is the activation energy. The Norris-Landzberg model refines the Arrhenius Coffin-Manson model, including the frequency of the temperature cycles f, and is defined as [56]

$$N_f = A f^{-n_2} (\Delta T_j)^{-n_1} e^{\frac{E_\alpha}{k_b T_m}}. \tag{11}$$

A and $n_{1,2}$ are similarly acquired by fitting experimental data. The Bayerer model introduces geometric and electric parameters, further improving the accuracy. This model is described by

$$N_f = A(\Delta T_j)^{-\beta_1} e^{\frac{\beta_2}{T_{j,min}+273}} \cdot t_{on}^{\beta_3} \cdot I^{\beta_4} \cdot V^{\beta_5} \cdot d^{\beta_6}. \tag{12}$$

t_{on} is the on heating time, I the bond-wire current, V is the blocking voltage and d is the wire diameter. β_{1-6} and A are parameters obtained from experiments data through curve fitting [58].

The accuracy of the aforementioned models for power modules is limited to certain temperature intervals. Lutz et al. [59] propose an augmented Bayerer model to reduce the error at small temperature fluctuation $\Delta T < 40K$ in a preliminary study. Other lifetime models based on material sciences like stress-strain hysteresis energy, crack propagation, stress, and plastic strain will not be covered [17]. Some data-driven models based on stochastic observed data utilize probability density function and regression to estimate RUL. However, these models are not currently applicable for lifetime prediction due to large confidence intervals [17].

Accumulation damage theory

For RUL prediction, the widely utilized Miner's rule of accumulation of damage assumes each temperature cycle independently contribute to the degradation of the solder interface, giving a linear model represented by the equation [8]

$$LF = \frac{1}{D} = \sum_{i=1}^{k} \frac{n_i}{N_i}. \tag{13}$$

Where n_i is the number of cycles in the stress range, N_i is the number of cycles to failure for the given temperature fluctuation, and D is the accumulated degradation. Therefore, the consumed lifetime (LF) can be expressed based on this accumulated stress model [8].

van der Broeck et al. [55] emphasize that this model primarily could be used for qualitative comparisons and not as a tool for absolute lifetime prediction. Similarly, Kovacevic-Badstuebner et al. [44] challenge the accuracy of this model for not taking into account the non-linearity and the time-dependent effect. Specifically, the sequence of stress and the stress interaction under cyclic loads are sources of error for the simple Miner's rule, Especially under varying load profiles [14, 60]. However, the estimated lifetime with Minor's rule for power modules was in line with the experimental results in the validation study of Hernes et al. [61] for specific stress conditions. To account for the nonlinear cumulative effect in damage accumulation, Several models have been developed, such as variants of the Manson-Halford model [60]. Meanwhile, non-linear models require extensive experimental data to weigh the appropriate parameters describing the dependencies on the accumulating rate of damage [14]. It is worth noting that the accuracy of the lifetime models depends on detailed T_j estimation [44].

2.6 Active gate drivers

Adaptive gate drivers

A gate driver is an auxiliary electronic circuit that controls the switching of a power device between its various operating states [25]. To do this effectively, the gate driver must be able to transfer sufficient charge to or from the gate of the power device through a low-impedance path [62]. Simultaneously, provide continuous charge to ensure stable operation during the different states. MOSFETs, which have an isolated gate terminal, do not require a continuous gate current i_g when fully on or off [62]. Gate drivers are critical for ensuring reliable operations, where failures could result in inconsistent performance or immediate converter malfunction [63]. Therefore, decoupling the logic signal from the power supply and the power circuit is important for signal quality and to

mitigate nonintentional shoot-troughs [25, 63]. Shoot-though is a fault occurring when both power devices in a half-bridge configuration turn on simultaneously [63]. In comparison to conventional gate drivers providing fixed switching patterns, AGDs can influence the switching transient by slope manipulation, loss control, or improve device utilization by for example sharing the current effectively in parallel SiC MOSFET topologies [37, 64, 65]. Adaptive gate drivers can be grouped based on three main topologies, adaptive voltage source gate drivers (AVGD), adaptive current source gate drivers (ACGD), and adaptive resistive gate drivers. AGDs operate by regulating the charging speed and trajectory of the C_{gs} to attain the desired performance [3]. Nevertheless, there are compromises to consider when using active gate drivers, such as their ability to provide sufficient strength and bandwidth [3].

Adaptive voltage source gate drivers

Adaptive voltage source drivers utilize rapid connection or disconnection of voltage sources to reach the desired v_{gs} waveform. In the integration of multi-level voltage sources, both the duration and the voltage levels are controllable, resulting in a scheme with multiple degrees of freedom and high versatility [66, 67]. AVGD rely on the effective implementation of rapid semiconductor switches and their methodically designed gate drivers for these switches [3]. The controllability depends on detection circuits and controllers for generating the appropriate logic signals to the switches. A proposed circuit is illustrated in Figure 10 where the four MOSFETs can provide the desired voltage to the gate across the specific on/off resistors [68]. Often the suppression of oscillations and overshoots by slowing down the transient generates higher switching loss. Therefore, this trade-off between better switching performance and efficiency must be considered [68, 67]. A number of AVGDs have been suggested, with the ability to adjust the switching transients to enhance certain performance parameters [23, 67, 68, 69].

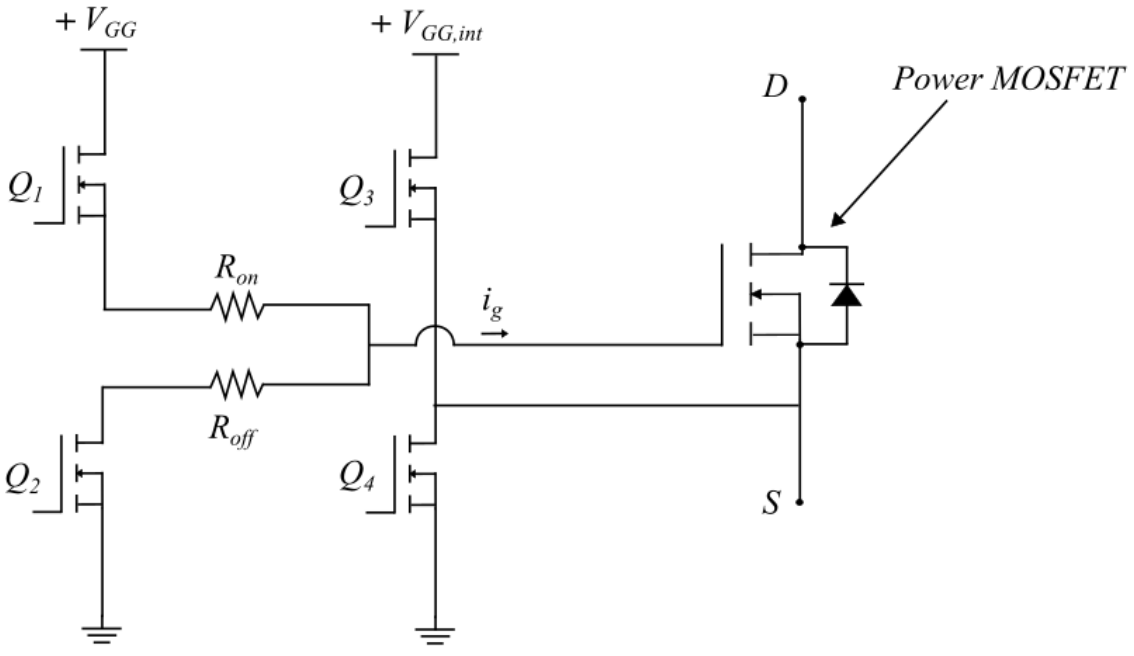


Figure 10: Schematic of an adaptive voltage-source gate driver. Reconstruction of drawing based on [68].

Adaptive current source gate drivers

Adaptive current-source drivers (ACGD) typically operates by preemptively charging the energy storage of an inductor, before releasing the energy as a gate current i_g [37]. This provides a more constant gate current rather than a rapidly decreasing current of the voltage source gate drivers,

caused by the decreasing voltage difference between the applied voltage source V_{gg} and v_{gs} [37, 70, 71]. Figure 11 visualizes the circuit diagram of a typical ACGD [70]. In the ACGD, accurate control of the four switches enables controllability of the initial gate current, thus the ability to manipulate the switching speed of the MOSFET. The effect of the constant current is illustrated in Figure 12 [71].

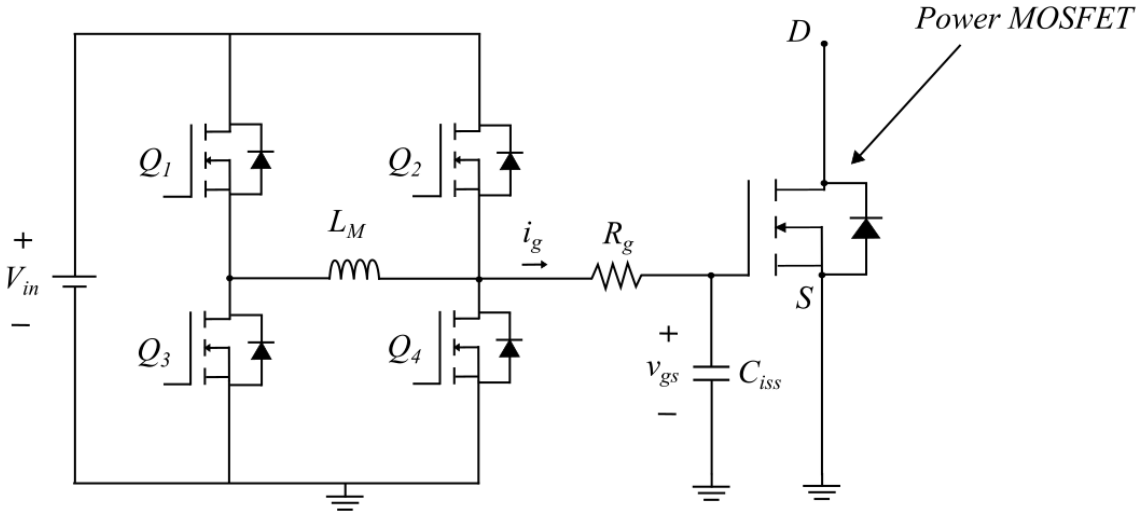


Figure 11: Circuit schematic of an ACGD. Based on [37, 70].

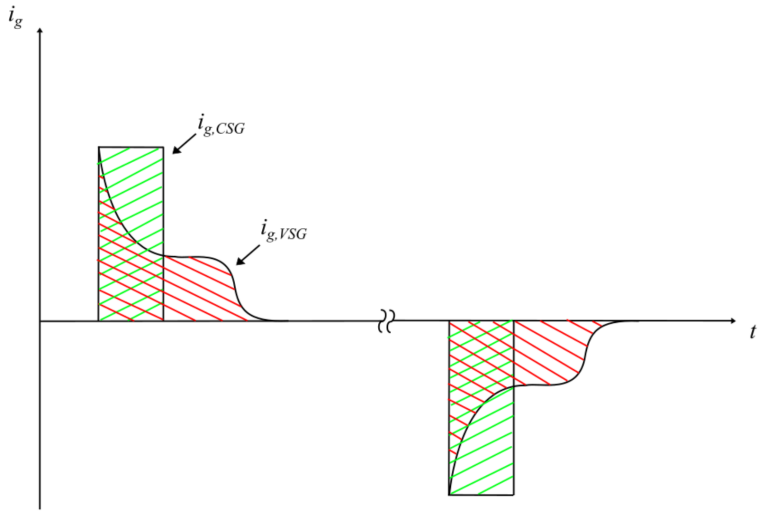


Figure 12: The gate current i_g comparison of current source and voltage source drivers. Based on [71].

Eberle et al. [70] claim that an ACGD offers the benefit of functioning as a current source, providing fast switching and minimal losses. The driver also offers the potential to recover energy from the gate capacitance instead of dissipating it [70]. The ACGD topology suffers from certain limitations, such as increased complexity and control demands, due to effectively converting a constantly changing input profile into a corresponding i_g waveform [3]. Nevertheless, ACGD allows for a greater i_g resolution compared to AVGD and adaptive resistive gate drivers [3].

Adaptive resistive gate drivers

Adaptive resistive gate drivers typically operate using multiple gate resistors $R_{g,i}$, in different channels, each with a designated value. After the calculation of the desired equivalent resistance R_{eq}, the controller can determine the combinations of resistors in parallel to alter the equivalent gate resistance R_{eq} [19]. This modification affects the switching transient and losses, and can with the right configuration occur dynamically during the switching transient [3]. However, due to the fixed number of resistors, operating conditions are limited and discrete [19, 20]. Increasing the number of resistors enhances the adaptability and resolution of the driver, but implies complex logic. Compared to the two other AGD topologies, it has a limited number of operational conditions, necessitating an effective gate driver layout and effective control circuitry to select the required R_{eq} [20]. This is typically done by means of a Complex Programmable Logic Device (CPLD) [19]. An illustrative adaptive resistive gate driver is shown in Figure 13 [20]. Henn et al. [3] argue that ACGD and adaptive resistive gate drivers are more suitable for wide band-gap devices such as SiC, owing to their elevated output bandwidth. Adaptive resistive gate drivers prove to have wide versatility. An example is the driver proposed by Tripathi et al. [72] that could reduce shoot-trough protection time and provide online state monitoring of parameters such as v_{ds} and temperature. The versatility of AGD extends to multiple areas of use, including the potential to enable device protection and monitoring [3].

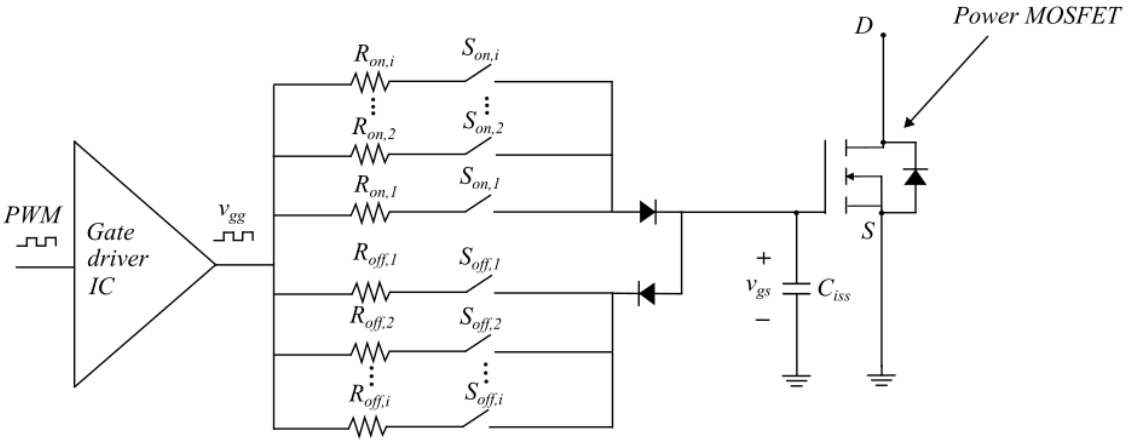


Figure 13: Schematic of an adaptive resistive gate driver. Reconstruction of drawing based on an illustration from [20].

2.7 Thermal structure and temperature estimation

Heat transfer mechanisms

Three primary heat mechanisms exist, conduction, convection, and radiation. With regard to electric systems, conduction is the main mechanism [73]. Heat-transfer, as conduction in a one-dimensional direction through a homogeneous isotropic material, can be described through the heat equation represented as [73]

$$\frac{\partial^2 T}{\partial x^2} = \frac{c_T \rho}{\lambda_{th}} \cdot \frac{\partial T}{\partial t}. \tag{14}$$

Where c_T, ρ and λ_{th} are respectively the specific thermal capacitance, the material density, and the specific heat conductance of the material and x is the propagation direction length [73].

Thermal Structure MOSFET

In a lumped parameter model such as the Cauer-model, the parameters R_{th} and C_{th} describe the steady-state and transient thermal behavior of the MOSFET structure [74].

$$R_{th} = \int_0^d \frac{1}{\lambda_{th} A_z}\, dz \qquad C_{th} = \int_0^d c_T \rho A_z\, dz \tag{15}$$

Where d is the material thickness in the propagation direction z, and A_z is the effective area at thickness z [74]. The effective area is typically based on a 45 degrees heat spread angle seen in Figure 14, however, the spread angle depends on the given MOSFET package structure [75]. Figure 15 visualizes the physical thermal structure of the SiC MOSFET.

The parameters for the R-C networks are typically extracted by means of 3-D finite element method (FEM) simulations [74]. 3-D FEM simulations provide a high degree of accuracy and visualization of the 3-dimensional heat flow and temperature distribution, however, computational-heavy and time intensive for high accuracy [52]. The accuracy of these models at high temperatures and different boundary conditions are still questioned [74]. The boundary conditions as in the power losses and coolant present a challenge due to how it varies, making it challenging to extract accurate thermal capacitance and resistances at different conditions, locations and layers [74]. The temperature sensitivities of the packaging materials influence the specific heat capacitance and thermal conductivity, therefore a temperature-dependent model will provide a higher degree of accuracy [74].

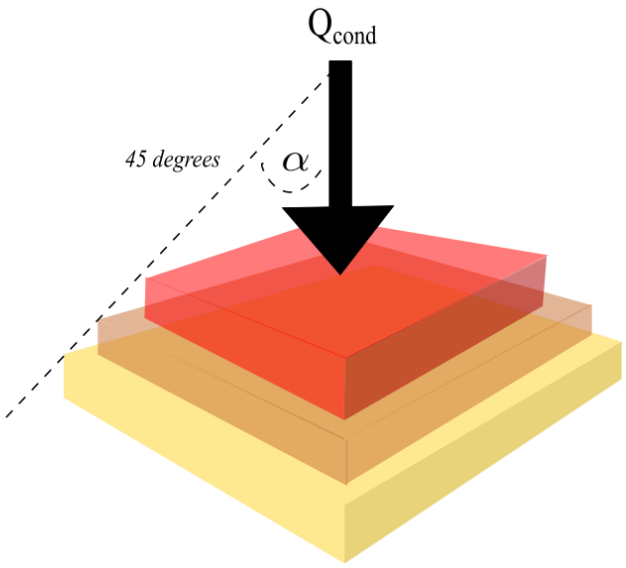


Figure 14: The propagation direction of the conduction heat transfer Q_{cond}. Inspiration from [76].

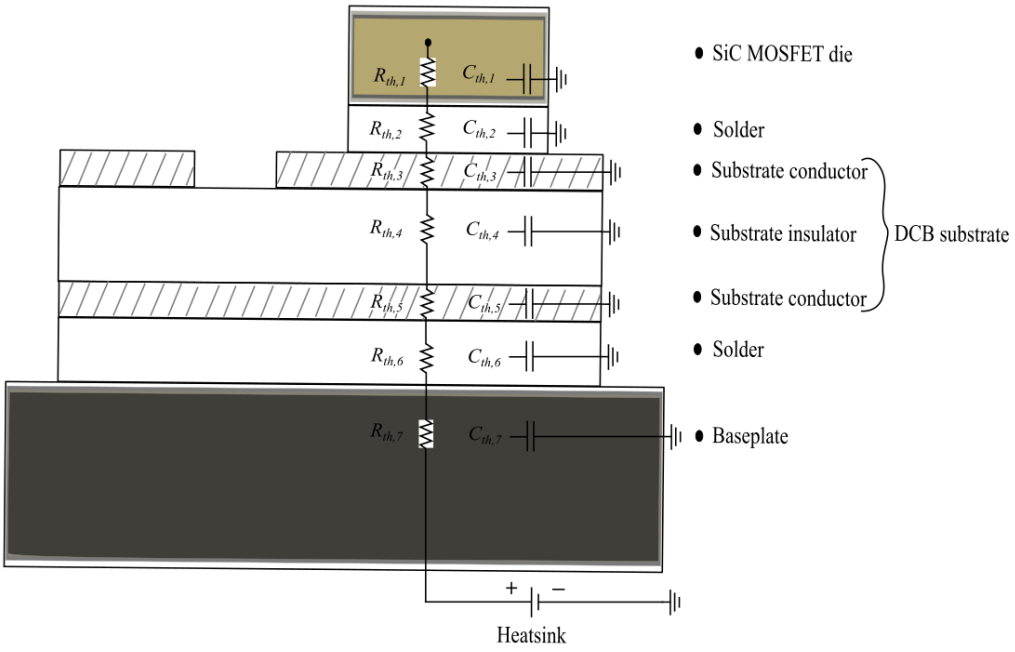


Figure 15: SiC MOSFETs thermal structure, based on [73].

Temperature estimation

The following sections will give a brief overview of some principal methods to estimate the T_j of MOSFETs with their advantages and constraints. As aforementioned, the junction temperature T_j is a critical parameter with regard to package degradation, lifetime estimation and condition monitoring [8, 13, 32]. Monitoring T_j online and with a high degree of accuracy is important for ensuring safe operations within temperature limits and for enabling ATC [77]. There are primarily four methods used for T_j estimation. These four approaches are grouped in the physical thermal sensor method, optical imaging, thermal network method, and temperature sensitive electrical parameters (TSEP) [78, 79]. TSEPs are expressed as the most viable approach for lag-free, precise temperature estimation [3].

Physical thermal sensor method and optical imaging

Physical thermal sensors can be achieved using a thermocouple or thermistor. Thermocouples are sensors based on the voltage difference of two metals joined together to form a junction. A voltage difference over this junction can be observed and measured corresponding to a given temperature utilizing calibrated tables. Measuring the T_j of SiC MOSFETs using standard thermocouples or optical imaging is generally not feasible due to the inaccessibility of the SiC chip and the swift temperature transients [14, 44, 80]. Packaging material must be removed for access and these methods are inferior compared to TSEP and thermal network models in estimating the T_j due to their slow response time [14, 44, 80].

Thermal network models

In order to provide an estimate of the internal T_j, thermal models are built based on the methodology of extracting thermal resistances R_{th} describing the steady state temperature distribution and thermal capacitances C_{th} models the transient thermal behavior as previously presented [44]. These thermal networks can be expressed as 3-D finite element models (FEM) [44, 55] or as 1-D networks analogous to electrical circuits [73]. An optimal thermal model should have both high accuracy and low computational complexity [52]. A 3-D temperature monitoring for estimating

the temperature distribution has been proposed by van der Broeck et al. [77]. This method factors in the cross-coupling effect if multiple devices are paralleled, compared to the 1-D models. Two 1-D lumped parameter thermal networks, the Cauer-network and Foster-network, suitable for calculating the dynamic behavior of the junction temperature will be presented.

The Cauer-model illustrated in Figure 16 is based on the thermal structure of the MOSFET. The nodes-voltages correspond to the temperatures at each intersection. R_{th} and C_{th} are related to the material properties of each layer in the thermal structure [27, 44, 73].

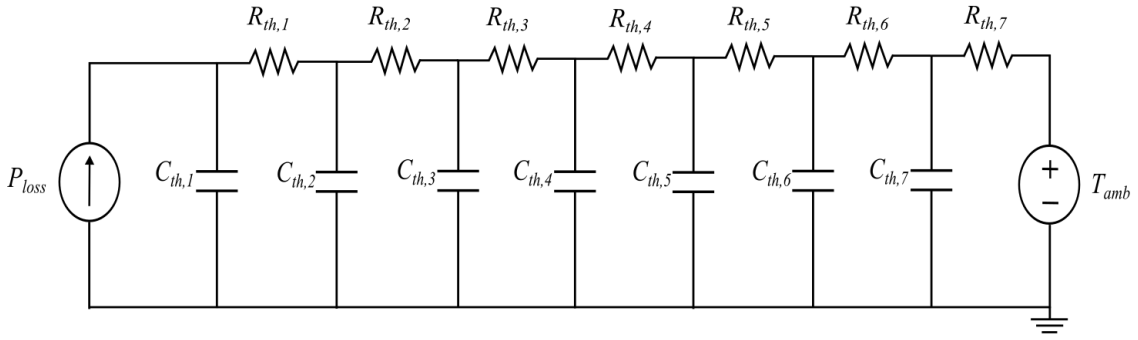


Figure 16: A thermal model expressed as a Cauer-network [73].

In contrast to the Cauer-network, the network parameters in the Foster-network do not have a direct correlation with the physical parameters, Therefore the nodes do not express the internal temperature distribution [27, 44, 73].

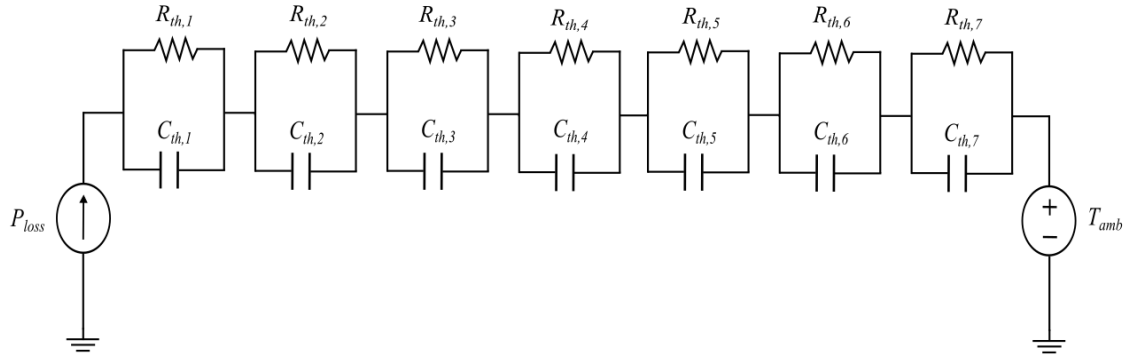


Figure 17: A thermal model expressed as a Foster network [73].

The primary advantage of the Foster model depicted in Figure 17 is that it offers a simple analytical expression for the thermal impedance Z_{th}. Each series thermal resistance $R_{th,i}$ and thermal capacitance $C_{th,i}$ contributes to a time constant τ, therefore Z_{th} can be described as [44]

$$Z_{th}(t) = \sum_{i=1}^{n} R_{th,i}(1 - e^{-\frac{t}{R_{th,i}C_{th,i}}}). \tag{16}$$

The thermal model parameters can be extracted from experimental measurements using curve fitting algorithms, through 3-D FEM simulations, or from the datasheet of the MOSFET [27]. The aging and temperature dependencies of the material are typically not included in these models. Chen et al. [27] and Heng et al. [74] have proposed temperature-dependent Cauer-network models taking into account the material properties' temperature sensitivity. This approach lets certain R_{th} and C_{th} be variable to increase accuracy while ensuring adequate computational effectiveness. An

issue with the lumped thermal network models is the oversimplification of the thermal capacitance of the thicker layers, for example, the baseplate claims Entzminger et al. [52].

Temperature sensitive electrical parameters (TSEP)

TSEPs have gotten acceptance as the most proficient way to estimate the T_j of MOSFETs, being a noninvasive approach [78, 81]. Several parameters have been proposed. Some viable TSEPs are indicated as the threshold voltage $V_{gs,th}$ [81, 82], the load current I_d [79, 82], the DC bus voltage overshoot [83], turn-on delay time $t_{d,on}$ [81, 84] and turn-off delay time $t_{d,off}$ [33]. In essence, the progress in intelligent and adaptive gate drivers directs the development of TSEPs. This is a result of the proximity giving the possibility of retrieving electrical parameters rapidly [3]. Utilizing pre-calibrated lookup tables, almost lag-free temperature estimation is achievable, only limited by the sensor-circuit layout [3, 78]. Thus, TSEPs could enable precise internal ATC [3, 85]. Aging causes some of the parameters to shift as previously presented. Therefore, calibration and aging compensation schemes must be addressed, introducing a layer of complexity [81].

2.8 Active temperature control

ATC is a concept that can be used to tackle the issue of thermal cycling degrading the life expectancy of power devices [3, 19]. Control of the junction temperature T_j, peak junction temperature $\hat{T}_j$, or average junction temperature T_m, implies a direct control over dominant aging factors [8], referring to Chapter 2.5 on lifetime models. To be able to precisely and effectively control the MOSFET with the objective of lower ΔT_j, an estimator providing real-time T_j measurements seamlessly with no delay is required [19, 77]. Several proposed ATC frameworks can be grouped into two categories, external and internal thermal management [20]. External temperature control frameworks are based on the external influence of heat dissipation systems. This could be altering the heat extraction performance of the cooling system, such as controllable fans [86] or liquid cooling techniques [87]. In the reduction of junction temperature fluctuations, these approaches have a limited bandwidth and an inherent delay and drawn-out response time [19]. Internal ATC, on the other hand, can be achieved by frequency control [88], switching loss control [19, 20], modulation schemes [16] or joint strategies approach [89]. ATC is applicable at the component or system levels [16]. Internal ATC at the component level will be reviewed in greater detail, in addition to presenting some state-of-the-art ATC schemes.

Internal active temperature control

Internal ATC can be achieved broadly grouped into two segments, loss reduction and loss compensation. Loss reduction could be attained by controlling the switching frequency or employing a modulation scheme with the intent of ΔT_j reduction. Within the loss compensation segment, gate control, reactive power circulating, power-sharing, and switching frequency control are viable strategies [16, 53]. Loss compensation schemes will be the focus of this thesis. This approach functions by amplifying the losses in instances when the load and temperature fall to prevent the system from cooling down. Some of the control schemes include hysteresis control [21], regional control [80], and a low-pass filter/virtual heatsink approach [19]. The drawback of some ATC approaches is that the system performance may suffer from effects such as decreased efficiency caused by the increased losses and increased total harmonic distortion (THD) [90]. Applying ATC will require balancing the impact of ΔT_j reduction and associated costs with the implementation of auxiliary circuitry [20, 53].

The main components of three internal ATC strategies based on switching loss manipulation will be presented. Concepts from the two first ATC schemes constitute the foundation for the proposed ATC framework presented in chapter 3. The third ATC strategy utilizes a controllable snubber circuit compared to the first two using AGDs.

van der Broeck et al. proposed an ATC framework for ΔT_j reduction based on switching loss

modulation utilizing adaptive resistive gate drivers. The gate drivers can achieve 16 effective gate resistance R_{eq} combinations [19]. The ATC approach was primarily intended for insulated gate bipolar transistors (IGBT)s. The framework is based on loss modulation, choosing the appropriate resistance sequence to achieve the loss command. The reference junction temperature is generated using a virtual heat sink. This virtual heatsink can be augmented to produce a slower time constant, multiplying the thermal model's thermal capacitances $C_{th,i}$ with a factor c_v. Hence, the dynamics of the virtual heatsink are slower than the real system. The operational reference resistance is chosen so the controller may increase or decrease the losses. A PI controller is utilized to command the loss modulator function. Aiming at reducing ΔT_j by inducing an increase or decrease in switching losses. Smooth T_j estimation is achieved by implementing a spatial observer from prior research [77]. Even though the experiments were conducted using IGBTs, van der Broeck et al. assert that the scheme is viable for MOSFETs, not specifying the type. In contrast, Ding et al. [20] argue that due to the lower switching losses, SiC MOSFETs require a larger resistor network for equivalent smoothing efficiency of T_j. This may limit the statement of van der Broeck et al. to Si MOSFETs.

Ding et al. [20] proposed an ATC framework demonstrating a ΔT_j reduction of 24.1%, resulting in a claimed lifespan increase of a factor of 3.92. This framework relies on a resistorless AGD. The gate driver-based switching loss scheme uses two axillary MOSFETs, for v_{gs} control during turn-on and turn-off, thereby manipulating the switching transients and the switching losses. Compared to the aforementioned ATC framework, this method enables a rather continuous and adjustable loss compensation compared to the resistive-network AGD. In addition, this gate driver-based scheme was verified experimentally on a SiC MOSFET. Ding et al. argue that the cost and topology complexity of this design is simpler compared to other proposed AGD-based temperature control schemes. The concepts of continuous loss modulation and virtual heatsink-generated reference are used as inspiration for the proposed ATC scheme presented in this thesis.

Compared to the former ATC approaches. Wang et al. [15] examined a strategy for turn-off switching-losses manipulation in SiC MOSFETs utilizing a controllable buffer capacitance in a snubber circuit to regulate the speed of the switching transient. Thus, regulating the switching losses. The ΔT_j is rapidly suppressed by continuously adjusting the equivalent capacitance in the range of $C \in [30 - 180]$nF with a constant buffer resistance $R = 5\Omega$. A delay time for a switch K_1 is introduced to regulate the equivalent capacitance, enabling this online capacitance adjustment seen in Figure 18.

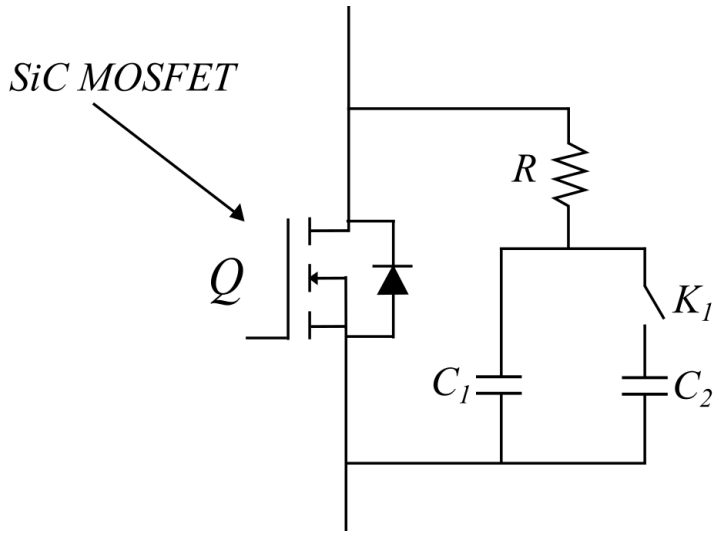


Figure 18: Schematic of the buffer capacitance adjustment approach. Drawing based on [15].

3 Methodology for electro-thermal characterization of SiC MOSFET

With the objective of examining an ATC scheme, knowledge of the MOSFETs behavior at varying temperatures is of critical importance. The initial step in achieving this goal is to obtain the electrical properties dependent on temperatures, such as the ID-VDS and transfer characteristics of the SiC MOSFET C3M0075120D from Wolfspeed. The outline of this methodology involves the design and implementation of a controllable synchronous buck converter for temperature regulation of a heatsink, to be used as a heating plate. In essence, a current-controller and a temperature controller are implemented for this purpose, employing a Texas Instrument developer board LAUNCHXL-F280049C, an infrared temperature sensor, and the C2000 embedded coder package in Simulink. The sought-after temperature-dependent data is obtained by utilization of a curve tracer/device analyzer. This experimental approach and its considerations will be thoroughly addressed in this Chapter.

3.1 Experimental approach

Experimental setup

The experimental setup is visualized in the Figure 19. In order to characterize the DUT C3M0075120D SiC MOSFET [42] at various temperatures, an experimental setup composed of a heatsink with heating resistors connected is used. The B1505A Keysight curve tracer/device analyzer [91] with the N1265A Keysight ultra-high current expander module [92] is employed for acquiring the experimental data. Accurate temperature control of the heatsink acting as a heating plate, stabilizes the temperature and ensures the acquisition of valuable results. This objective is accomplished through the design of a controllable synchronous buck converter. Thus, temperature control of the heatsink is achieved through the implementation of a current-control-based pulse width modulation (PWM) scheme. As depicted in Figure 20, the power dissipation from the resistors is directed to increase the temperature of the heatsink and the SiC MOSFET connected by means of thermal grease and a clip for uniform pressure distribution. The methodology of conducting temperature-dependent analysis has been conducted in previous research using the B1505A Keysight curve tracer/device analyzer [93]. However, in this research study, the heater was a commercial programmable air heater TP04390A Thermostream. This approach is expected to yield a more consistent and precise temperature compared to the method employed in this thesis due to the rather uniform air temperature surrounding the MOSFET. Nevertheless, within the same study and in the research study conducted by Yang et al. [81], a similar approach employing a heating plate was successfully implemented in double pulse tests, demonstrating promising outcomes in steady-state regulation of the SiC MOSFETs temperature. The utilization of a temperature-controlled heating plate is based on similar underlying principles as the methodology employed in this thesis, using a heatsink with high thermal capacitance. This indicates the viability of utilizing a heatsink to maintain relatively stable and uniform temperatures. The temperature and its rate of change can be validated by a thermocouple placed at the SiC MOSFET case. The power supply is of the type EX421GR Power supply, able to provide 42V and 10A [94]. Wires related to the control signals, as seen in Figure 20 are twisted for stray inductance reduction, improving the signal quality.

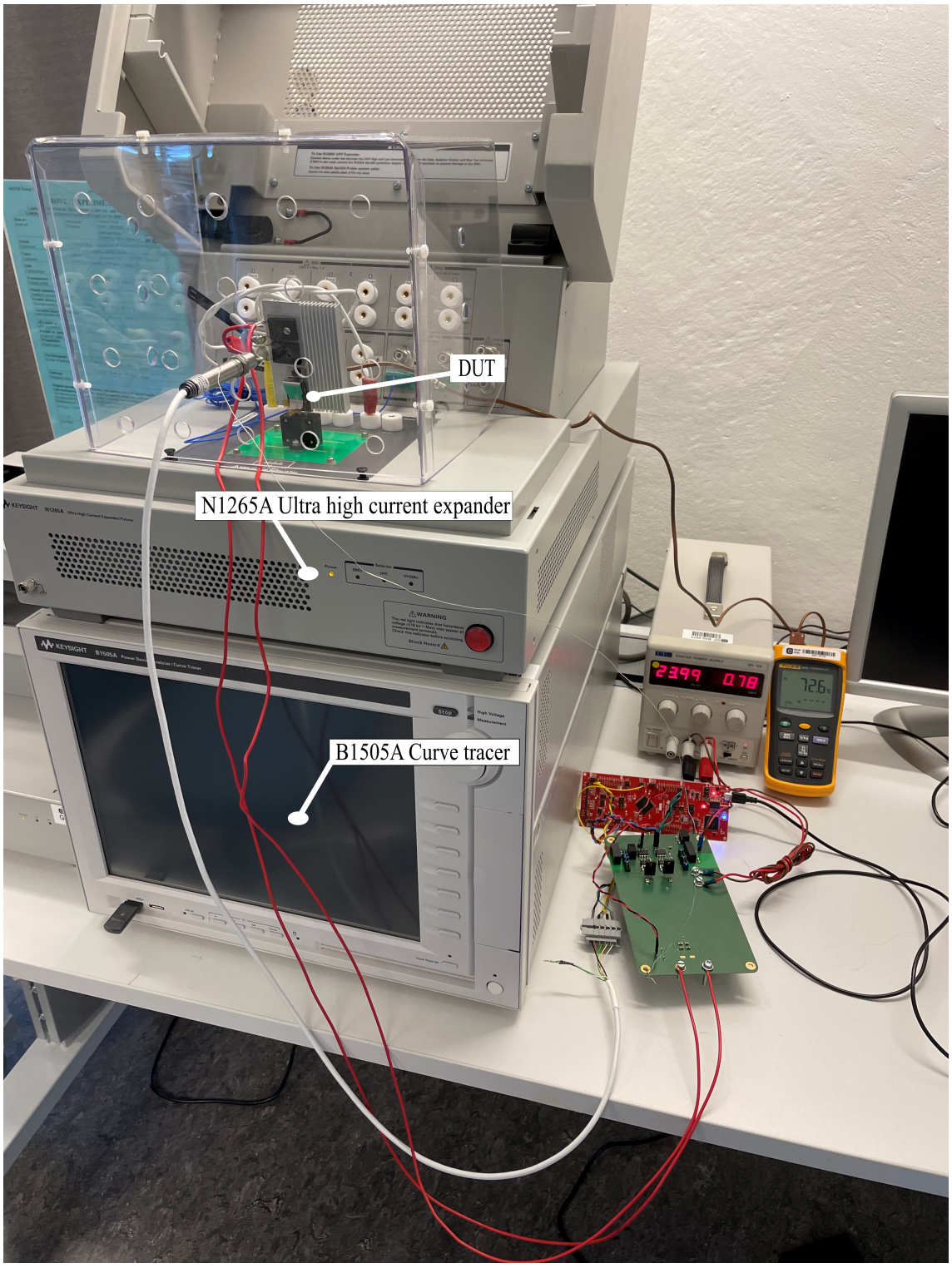
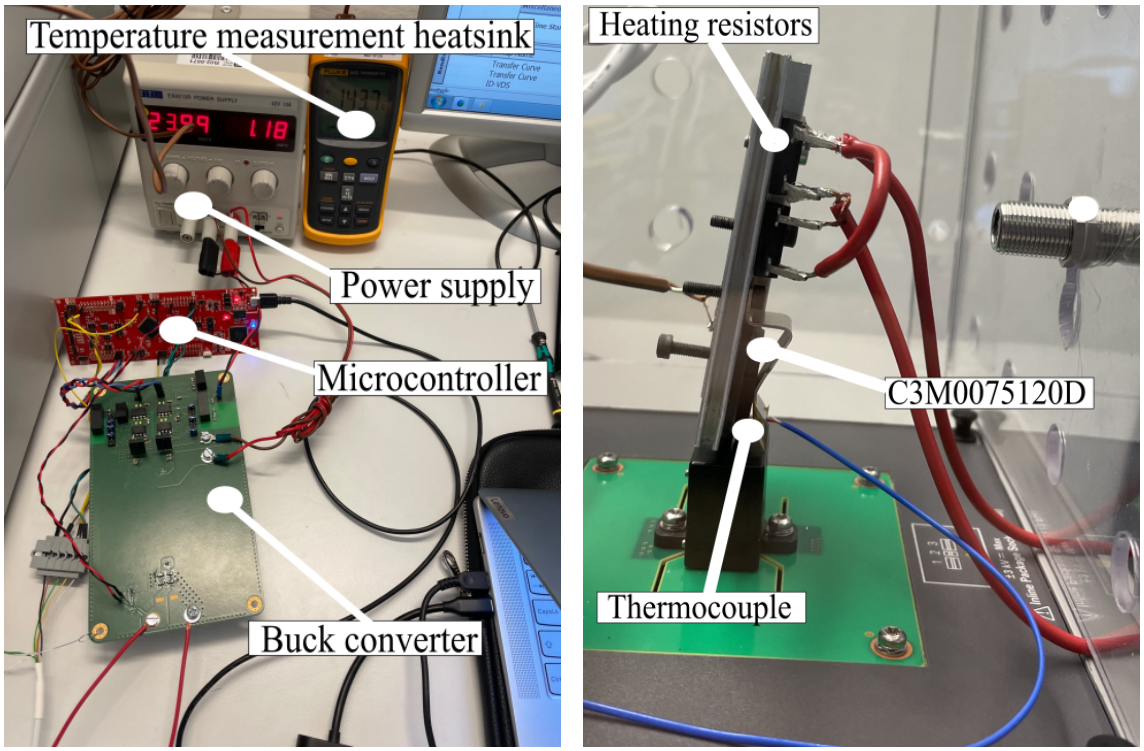


Figure 19: Experimental setup.



(a) The buck converter, power supply, heatsink temperature measurement, and microcontroller.

(b) Experimental setup with the DUT, the heatsink, and the curve tracer/device analyzer.

Figure 20: Component description of the experimental setup.

Temperature measurements and calibration

In this thesis, two type T thermocouples are used to estimate the temperature of the DUT for temperature measurements, calibration, and safety measures. One of the thermocouples is located at the heatsink connected to a fluke 54 ii [95] and the other at the case of the SiC MOSFET connected to the N1265A module. An infrared temperature sensor, as a third temperature sensor, is employed for the temperature feedback in the control algorithm. This sensor aims at the black resistors to avoid reflections from the clip of the SiC MOSFET attachment. Hence, the feedback temperature measurements are not of the SiC MOSFET, but rather the heating elements. However, Simulink [96] external mode interface facilitates live adjustment of the temperature reference, resulting in fast calibration for precise temperature control of the SiC MOSFET case temperature using the thermocouple measurements. Figure 21 visualizes the SiC MOSFET fastened by a clip for providing even pressure against a layer of thermal grease for high conductivity and uniform heat transfer. The two 22Ω resistors in parallel are shown in relatively close vicinity to the SiC MOSFET.

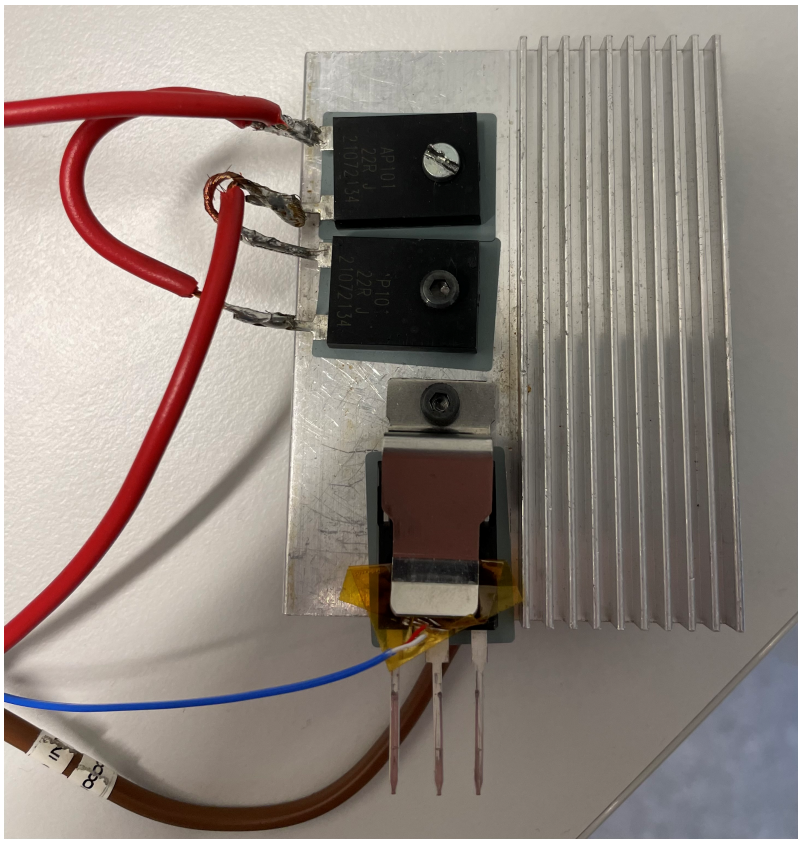


Figure 21: The heat propogation setup, with the DUT, temperature sensors, and load resistors.

Infrared temperature sensor

For temperature control purposes, the Optris CS LT 15 infrared sensor is employed [97]. The infrared temperature sensor is powered by a 5V power source from the microcontroller, operating in an analog configuration seen at Figure 22.

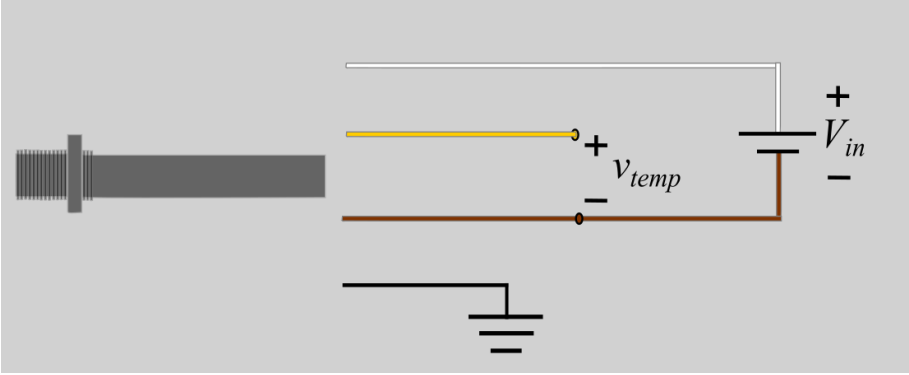


Figure 22: Infrared sensor connection schematic for analog output.

This results in an mV output between the yellow (OUT) and brown connection (gnd). The temperature sensor has a temperature resolution of $0.05K$ and an accuracy given in the range of $\pm 1.5K$. The response time of the microcontroller is 14ms. Thus, a small delay is induced in the control loop. However, due to the relatively slow temperature dynamics of the resistors and the heatsink, the selection of this particular hardware for the temperature feedback signal appeared to be suitable. The output signal is fed to an analog-to-digital converter (ADC) module of the microcontroller. The temperature measurements were calibrated with reference to one of the thermocouple-based

temperature sensors. Whereas the mV to the digital ADC levels were calibrated to the current controller at a given load resistor. This is accomplished by measuring the feedback voltage using a multimeter and recording the corresponding ADC values at different steady-state output voltages. This gave a conversion factor of (414/260). As visualized in Figure 22, to prevent potential noise and errors in the feedback voltage v_{temp} resulting from charge accumulation, grounding of the outer shield of the sensor was essential for ensuring a stable reference set point. The infrared sensor is shown in Figure 23.

Figure 23: The infrared sensor [97].

Curve tracer

The keysight B1505A is an apparatus that can provide a precision characterization of power devices with voltages up to 10kV and currents up to 1500A [91]. The interface of the ultra-high current module N1265A is visualized in Figure 24. The leftmost dark green temperature port was applied for temperature measurements of the SiC MOSFET case.

The first test performed in this thesis was a custom ID-VDS curve sweep with $V_{gs} \in [0, 19]$V, of 1V steps. The v_{ds} and i_d was limited to $[0 - 42]$ V and $[0 - 75]$A respectively. This limitation was imposed to ensure these tests were under the threshold of low-voltage experiments for both regulations and safety precautions.

The second test performed was characterizing the transfer curve at different temperatures. This test utilizes a constant V_{ds} and increments through $V_{gs} \in [0, 19]$V with 1V increments. The drain current i_d was limited to 80A. This test is conducted to investigate how the active region and $V_{gs,th}$ are affected by elevated temperatures.

Figure 24: The curve tracer B1505A with the N1265A module from Keysight [91, 92].

3.2 Synchronous buck converter

To be able to control the temperature, a synchronous buck converter is designed on a printed circuit board (PCB) to regulate the power dissipation of the two load resistors. This topology is chosen due to its simplicity regarding controllability and design. Controlling the PWM signal enables current control of the output, in turn, enables power control of the load resistors, providing the possibility of rapid temperature influence. The synchronous buck converter schematic can be seen in Figure 25. The converter is designed for frequency operation in the range of $20 - 50$kHz. This frequency interval is chosen to avoid frequency in the hearable sound spectrum while simultaneously avoiding the clock frequency of the microcontroller being a bottleneck for the PWM control. The layout and components selection will be addressed.

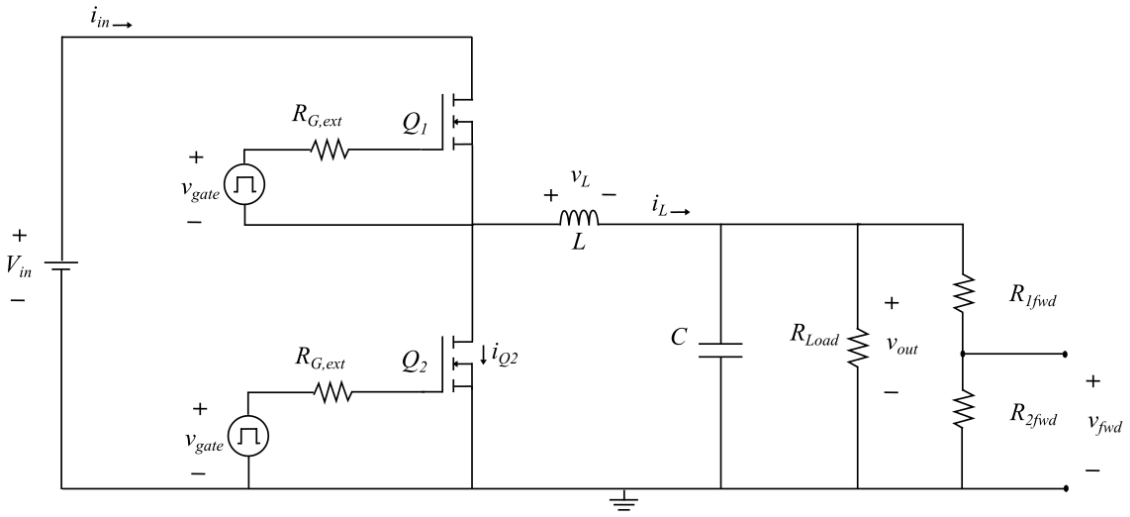


Figure 25: Synchronous buck converter circuit diagram.

Power-requirements

The power requirement for the heatsink seen in the configuration depicted in Figure 21 was estimated in the interval $P_{out} \in [0, 50]$W. An input voltage of $V_{in} = 24$V was estimated to be sufficient in this power range. This gives a maximum load current of approximately $I_{load} = 2.2$A. In the instance of power control of the heating resistors, the power quality and harmonics are assumed to be inconsequential factors for achieving steady-state temperature control of the SiC MOSFET package, thereby they are not determining factors in this design, and a low switching frequency is adequate for this goal. The experimental conditions are summarised in Table 1.

Table 1: Experimental conditions

Switching frequency	f_{sw}	20-50kHz
Input voltage	V_{in}	24V
Load Resistance	R_{load}	2x22Ω
output power	P_{out}	0-50 W
Output current	I_{load}	0-2.2A
Ambient temperature	T_{amb}	25 $°C$

Layout considerations

The converter was designed on a two-layer PCB to ease the soldering and component layout. This provides the opportunity of optimizing in regard to parasitic inductance to ensure a stable and successful operation of the drive circuit. The open-source software KiCAD 7 [98] was used for the PCB design, facilitating PCB and schematic editing. Figure 26 shows the PCB layout of the synchronous buck converter. Efforts were made to achieve a compact layout for the gate driver, with minimal routing length of the conductors for inductance reduction. The width of the copper tracks was carefully addressed to ensure significant current carrying capabilities and minimization of stray inductance. This reduces the oscillations and ensures a stable operation of the converter, seeking to circumvent the discussed negative consequences of parasitic inductance, such as non-intentional positive gate voltage bias [25]. In the power circuitry, large copper pour polygons were implemented due to the higher expected current. This lowers the current density, heat dissipation, and voltage drop in the power circuit. Thermal relive pads were incorporated to ease the soldering process. The PCB was manufactured by Elektronikk og prototypelaboratoriet (elprolab) at NTNU [99], whereas soldering to connect components was done by hand. The Si MOSFETs TK30A06N1,S4X from Toshiba [100] were used having a rated $I_d = 30$A and $V_{ds} = 60$V, which are sufficient for this converter.

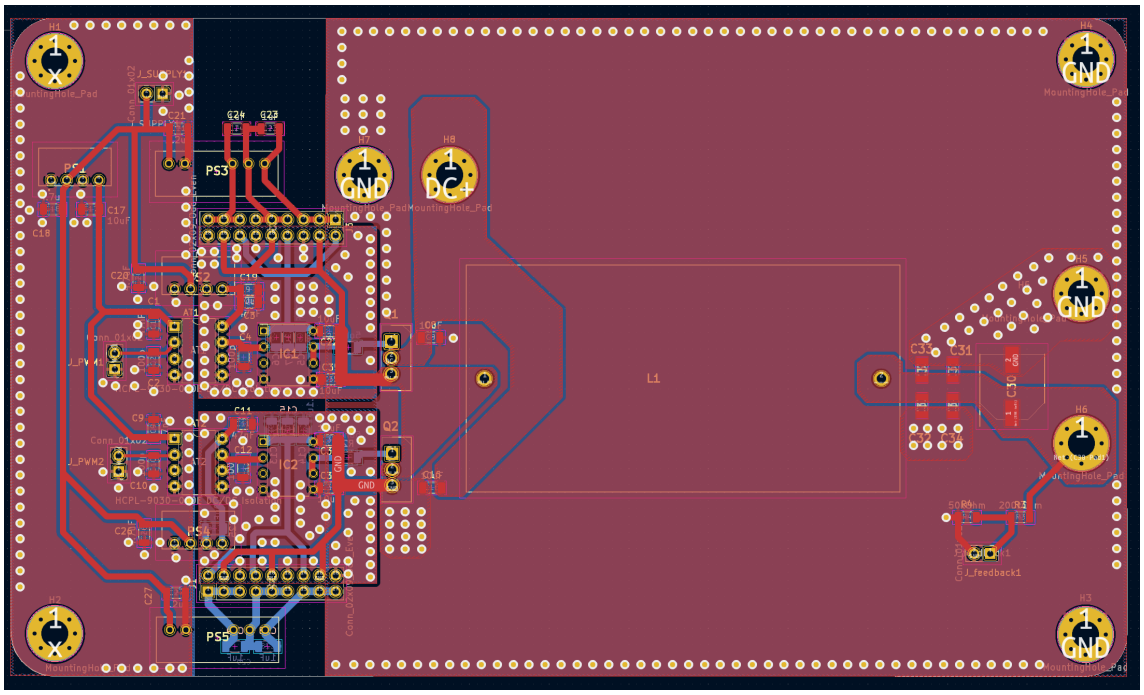


Figure 26: PCB layout of the synchronous buck converter.

Isolation and gate driver circuity

To ensure secure converter operation, isolation of the signals is essential to counteract signal interference. This is achieved by high-speed DC/DC digital isolation of the logic signal origin from the gate driver circuitry using HCPL-9030-000E from Broadcom [101]. For powering the digital isolator and the gate driver TC4420VPA from Microchip Technology [102], separate isolated DC/DC converters are utilized for each device to provide galvanic isolation. 1W TME2405S from Traco [103] are used for powering the HCPL-9030-000E. Where one TME2405S is used for powering both left sides, whereas two TME2405S are utilized for powering the separate right side of the two HCPL-9030-000E. Two 2W isolated DC/DC converters IHL0224D09 [104] are used for powering the gate drivers. The IHL0224D09 provides three output terminals with 0V and ±9V, leaving the opportunity to provide different voltage combinations. Therefore, two $2x9$ headers are used for modulating the given combinations of voltage sources for the gate driver while providing the opportunity for changing the gate driver voltage sources. Four separate 2-layer ground planes are used for decoupling the logic signal interface, the two gate drivers, and the power circuity, with a connection through multiple vias. This ensures good ground linkage and signal quality. The front and back of the assembled synchronous buck converter are shown in Figure 27 and Figure 28.

The injection of common-mode currents enforces requirements for isolation capacitance in the gate-driver circuit of the high-side devices due to their fast switching transients to stabilize the voltage. [63]. Thereby, separate ground planes and two capacitors are implemented for voltage stabilization and protection of the auxiliary gate driver circuitry. An external gate resistance $R_{g,ext}$ chosen to 5Ω gave an acceptable switching speed and switching waveform. For the feedback signal, a voltage divider of one $R_{1fwd} = 100k\Omega$ and one $R_{2fwd} = 10k\Omega$ gave a voltage conversion of 1/11, which provided a sufficient decrease to v_{fwd}, ensuring no violation of the 3.3V limit to the ADC module. An overview of the components is provided in Table 2.

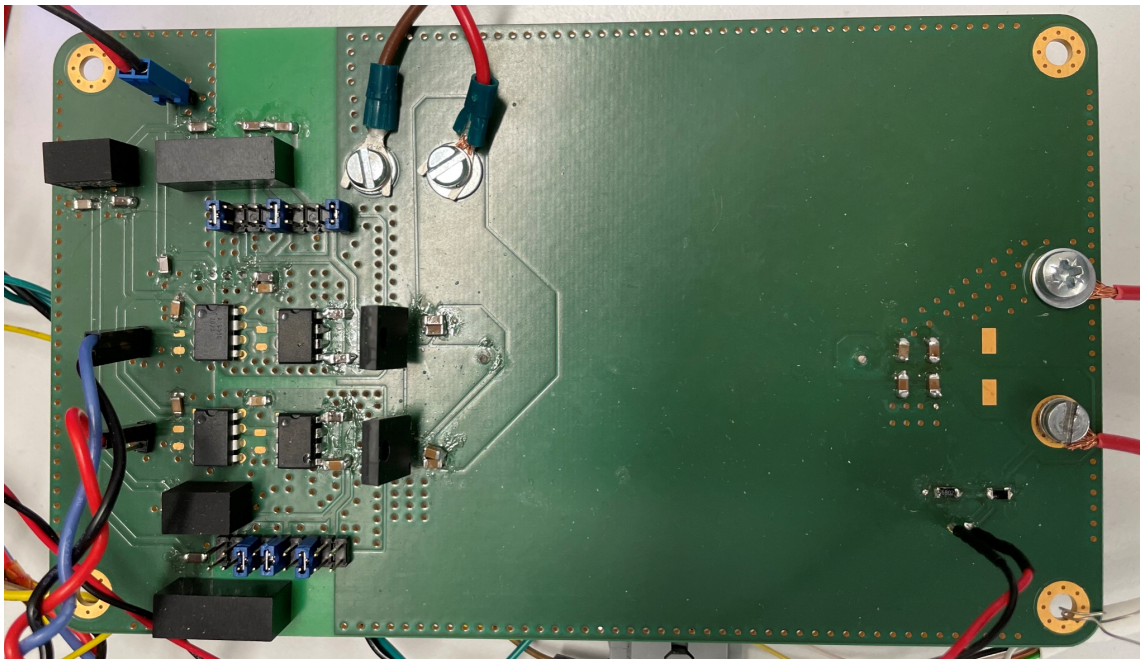


Figure 27: Front of the synchronous buck converter.

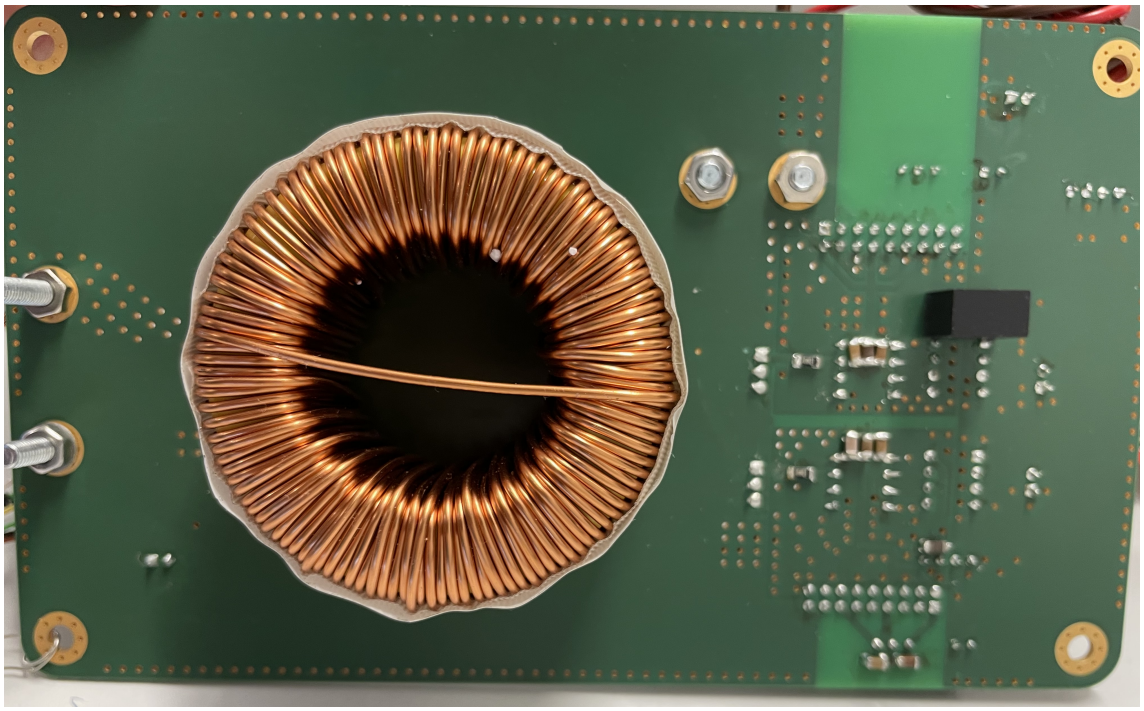


Figure 28: Back of the synchronous buck converter.

Capacitors

In the design of the output capacitance, an electrolytic capacitor was designed for the bulk of the capacitance value, while four $10uF$ ceramic capacitors are integrated in a parallel configuration to reduce the ripple and filter out the high-frequency noise [25]. In the assembly, the four ceramic capacitors proved to provide sufficient voltage stabilization. Hence, the installation of the electrolytic capacitor was disregarded.

Table 2: Synchronous buck converter components.

Si MOSFET	TK30A06N1,S4X
Gate driver	TC4420VPA
DCDC isolation	HCPL-9030-000E
Inductor 2.2mH	TJ92UEB222L
Power supply 1W	TME2405S
Power supply 2W	IHL0224D09
External gate resistors 5Ω	SMD-1206 package
Load resistors 2x22Ω	AP101
Feedback resistors 100k and 10kΩ	SMD-1206 package
Output capacitors 4x10μF	SMD-1206 package
Decoupling capacitors 100p-10μF	SMD-1206 package

Inductance selection

The inductance requirements were estimated based on the expression [105]

$$L = \frac{V_{out}(V_{in} - V_{out})}{\Delta i_L f_{sw} V_{in}}. \tag{17}$$

Given $V_{in} = 24V$ and a duty cycle of 0.5 gives roughly $V_{out} = 12$V assuming the ideal case. Based on a current of $I_L = 2.2$A, a current ripple of $\Delta I_L = 0.1 I_L$ and a switching frequency of the converter of $f_{sw} = 20$kHz. This gave the following inductance value $L = 1.4mH$. Two inductors with an inductance in this proximity and easily obtainable with the necessary maximum current ratings had an inductance in the range of $2.2mH$. They are referred to as the big choke and the small choke. An impedance characterization was conducted on the two inductances to ensure the self-resonating frequency was outside the operating switching frequency of the converter. The results of this analysis can be seen in Figure 29, indicating that both of the inductors had a self-resonant frequency outside the operational range of the converter. The large choke was selected based on it being the initially designed inductor in the PCB layout since both inductances fell within the required range.

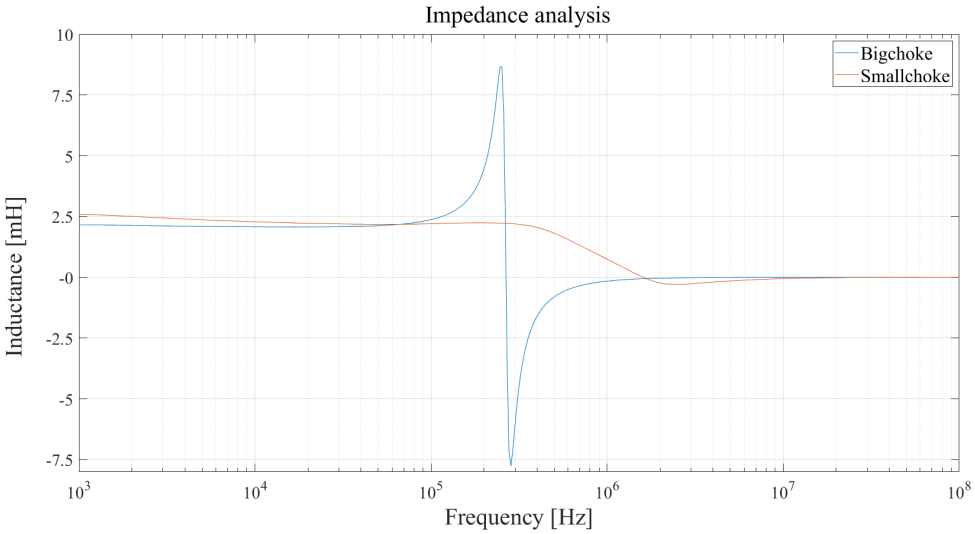


Figure 29: Impedance analysis of the two inductors.

3.3 Current and temperature control

C2000 Embedded Coder Package

For deployment of code generated from the Simulink models to the microcontroller, an Embedded Coder Support Package for Texas Instruments C2000 Processors was utilized [106, 96]. The add-on package produces C code and device driver block such as Analog to digital converter (ADC) and PWM. Furthermore, the Embedded Coder Support package facilitates the utilization of External mode (Monitor and tune) within Simulink. This allows for modifications of the reference parameters to the model through live serial communication with the microcontroller.

Microcontroller

The development board used is the LAUNCHXL-F280049C [107] in the C2000 series, based on the TMS320F280049C microcontroller chip from Texas Instrument [96, 108]. The features used are the PWM pins and analog-to-digital converters (ADCs) for signal processing of the analog current and temperature feedback with adjacent ground pins. The communication is implemented through the USB Micro-B ports and PC using an industry-standard communication protocol Serial communication interface (SCI) for online temperature reference adjustments. The microcontroller has a 100MHz CPU and flash size of 256KB [107]. The ADC modules have a 12-Bit resolution, providing sufficient resolution of 4095 levels with a selectable external reference chosen to 3.3V with a conversion time of 290ns [96, 108]. The resolution of the ADC and the conversion time are more than sufficient for the slow dynamic of temperature control of the resistors. Operating the synchronous buck converter with a switching frequency of 20 kHz, the clock frequency of the CPU and the flash memory proved to be abundant. The microcontroller is depicted below in Figure 30.

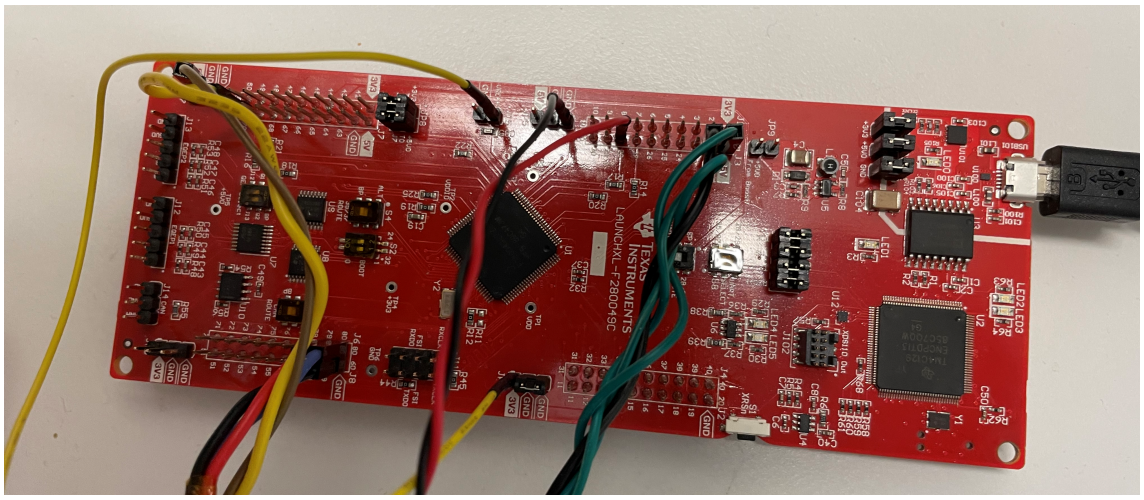


Figure 30: The development board LAUNCHXL-F280049C [107].

Current control

A current controller is implemented for the synchronous buck converter based on the dynamic stiffness method (DS) for high-performance command tracking and optimized disturbance rejection, utilizing the research of van der Broeck et al. [109] as inspiration. The controller uses a state-feedback design with a proportional and integral gain (PI). The derivations for K_p and K_i selections will be presented by first introducing a simplified electrical model of the converter and then presenting the dynamic stiffness (DS).

The equations representing the voltage difference and the current through the inductor are expressed as [25, 109]

$$u_L = u_{PWM} - u_{out} \qquad i_L = \frac{1}{L}\int_t^{t+T_{PWM}} u_L \, dx. \tag{18}$$

Where u_L is the inductor voltage, u_{PWM} is the voltage at the common node, and u_{out} is the voltage over the load resistor. T_{PWM} is the pulse width modulation period of the converter. As seen from the circuit diagram in Figure 31, the average of u_{PWM} applied generates an average inductor current i_L expressed by (18).

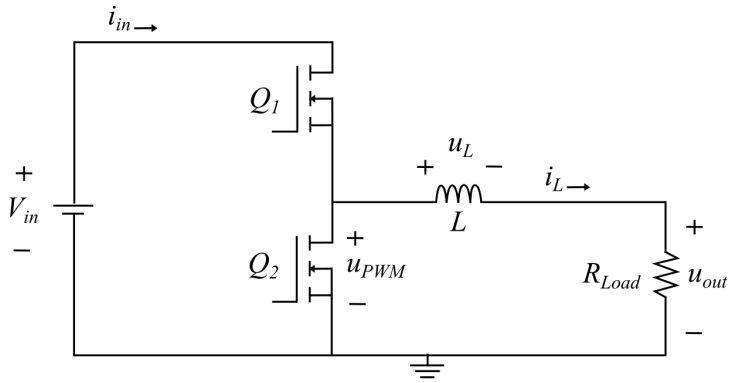


Figure 31: Circuit diagram simplified synchronous buck converter.

The modulator is assumed to be ideal $M(s) = 1$, which should be a valid assumption as long as the bandwidth is less than $f_{PWM}/10$ [109]. The block diagram of this model can be expressed as Figure 32 taking into account the derivation of the output power P_{out}.

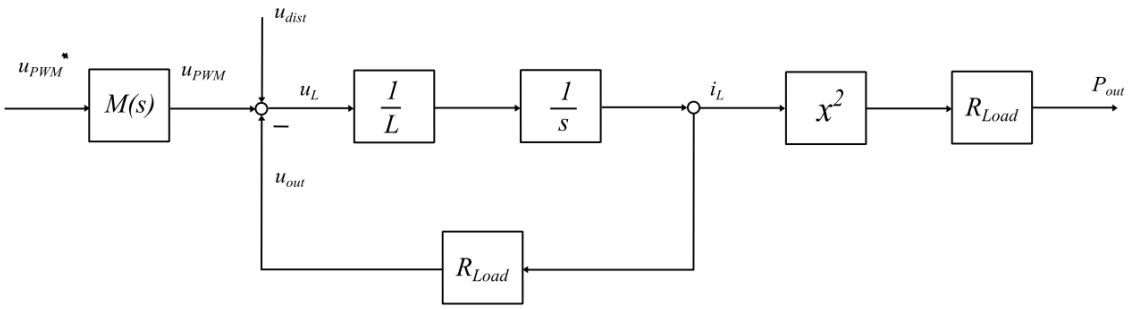


Figure 32: Block-diagram physical

Utilizing block diagram transformation, the transfer function of the physical system feed-back loop can be expressed as

$$G_{fwd}(s) = \frac{R_{Load}}{sL}. \tag{19}$$

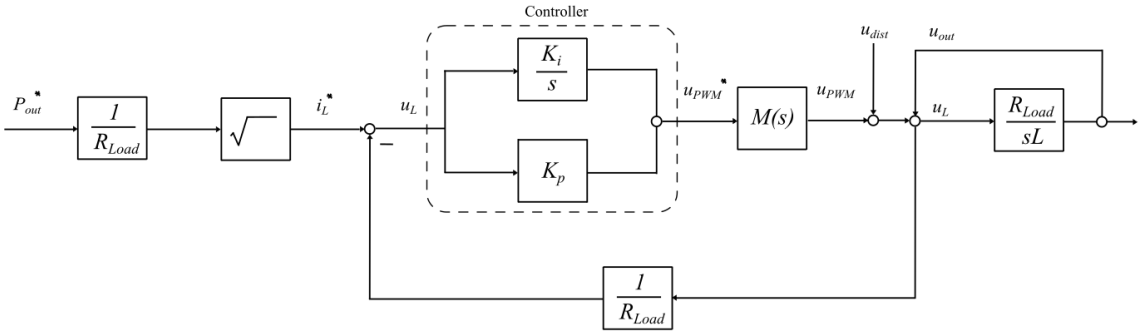


Figure 33: Block-diagram controller system

The block diagram can be reworked, such that the output power P_{out} is the reference, which is interesting for usage as an inner loop in a temperature controller point of view. The transfer function of the full block diagram with a controller given a proportional and integral state feedback control can as seen at Figure 33. The transfer function of the controller PI controller is

$$G_c(s) = (\frac{K_i}{s} + K_p). \tag{20}$$

Using Figure 33 the u_{out} through the closed-loop feedback with the controller can be derived utilizing $G_c(s)$ and $G_{fwd}(s)$ and expressed as

$$u_{out} = (u_{dist} - \frac{u_{out}}{R_{Load}} G_c) \frac{G_{fwd}}{1 + G_{fwd}}. \tag{21}$$

Therefore, the DS of the system can be derived as

$$\frac{u_{dist}(s)}{u_{out}(s)} = \frac{1 + \frac{1}{sL+R_{Load}}(\frac{K_i}{s} + K_p)}{\frac{R_{Load}}{sL+R_{Load}}} = 1 + \frac{K_p}{R_{Load}} + s\frac{L}{R_{Load}} + \frac{1}{s}\frac{K_i}{R_{Load}}. \tag{22}$$

The DS represents the impact of the disturbance on the output voltage, which in this case is closely related to the average current by R_{load}. In the frequency domain, the effect of the excitation frequency on the disturbance impact is given by the amplitude, as shown

$$|DS(j\omega)| = \left|\frac{U_{dist}(j\omega)}{U_{out}(j\omega)}\right| = \left|(1 + \frac{K_p}{R_{Load}}) + j\omega\frac{L}{R_{Load}} + \frac{1}{j\omega}\frac{K_i}{R_{Load}}\right|. \tag{23}$$

It is evident that the inductance is dominating at frequencies over the proportional frequency bandwidth. In between, the integral command frequency f_i and f_p, the proportional gain K_p is prominent. Whereas the integral gain K_i is predominant below f_i.

$$\left|\frac{U_{dist}(j\omega)}{U_{out}(j\omega)}\right| = \begin{cases} 2\pi f \frac{L}{R_{load}}, & f \geq f_p \\ 1 + \frac{K_p}{R_{Load}}, & f_i < f < f_p. \\ \frac{1}{2\pi f}\frac{K_i}{R_{Load}}, & f \leq f_i. \end{cases} \tag{24}$$

The maximum f_p^{max} is limited by the f_{PWM} and must stay a decade below to avoid resonance and ensure stable performance due to the bandwidth of $M(s)$ and the sampling delay [109]. For steady-state error rejection, the integral bandwidth should be less or equal to a fifth of the proportional

bandwidth to avoid a low dampening repose [109]. This is caused by the Eigenvalues related to the feedback path could cause a resonance behavior [109]. The limitation is summarized as

$$f_p^{max} < \frac{f_{PWM}}{10} \qquad f_i^{max} < \frac{f_p}{5}. \tag{25}$$

in this thesis the chosen values are $f_{PWM} = 20$kHz, giving a $f_p = 2kHz$ and $f_i = 400$ Hz. Derived from the equations in (24), expressions for f_p and f_i are given by

$$f_p = \frac{1}{2\pi}\frac{R_{Load} + K_p}{L} \qquad f_i = \frac{1}{2\pi}\frac{K_i}{R_{Load} + K_p} \tag{26}$$

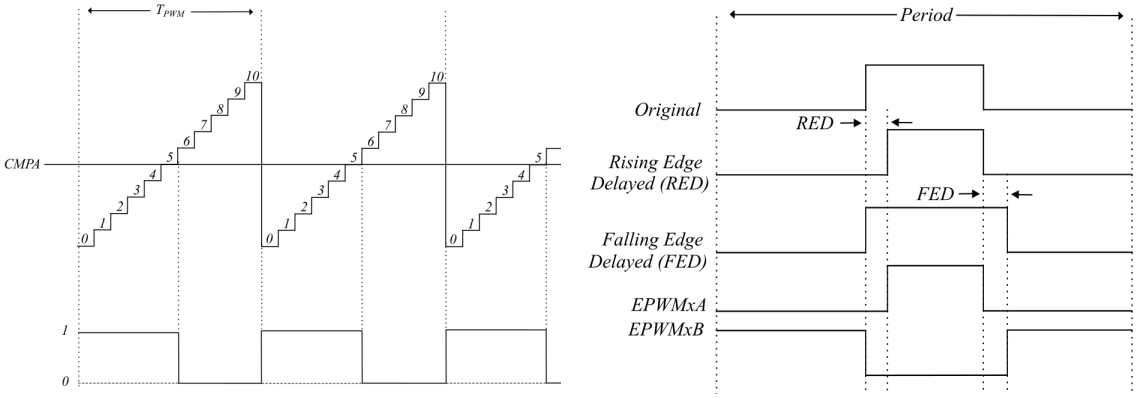
The equations in 26 can be algebraically manipulated to obtain an expression for K_p and K_i.

$$K_p = 2\pi f_p L - R_{Load} \qquad K_i = 2\pi f_i (R_{Load} + K_p) \tag{27}$$

With the given frequency bandwidths and $R_{load} = 11$, gives $K_p = 5.64$ and $K_i = 69467$.

PWM Modulation

The embedded software block ePWM is used for PWM generation [103, 106]. It is based on the discrete values of the period and the input compare register (CMPA) used as the modulating index with reference to the period time, illustrated in Figure 34. The logic PWM is generated based on the triangular up sequence. A comparison, whether the triangular signal is equal or larger than CMPA, the logic signal is 0. Figure 34 shows how the deadtime modulation is implemented in the ePWM block [103]. A saturation is implemented in the modulator, restricting the duty cycle $d \in [0.05, 0.95]$. This is implemented to ensure safe operation of the synchronous buck converter. An ideal modulator is assumed, giving $M = 1$. The PWMB signal is implemented using the inverse of the PWMA signal in the ePWM block. A dead time of $25ns$ is applied to prevent shoot-through by introducing a time delay in the commutation from a high signal in PWMA to PWMB. This gives the intrinsic capacitance time to discharge properly, suppressing crosstalk and a potential shoot-through due to a false trigger or the MOSFET not having time to turn-off before the other turn-on.



(a) PWM generation (b) Deadtime modulation

Figure 34: Discrete PWM modulation in the ePWM Simulink block [110].

Discrete simple moving average

To smooth out the signal from the ADC and eliminate high-frequency noise, a low-pass filter is implemented in the form of a simple discrete moving average (SMA). This effectively filters out

the small overshoots, with the intention of improving the controller performance. The transfer function for the simple moving average in the Z-domain $H(z)$ can be derived from the Z-transform of the impulse function $h(n)$ [111]

$$H(z) = \frac{1}{N} \frac{1 - z^{-N}}{1 - z^{-1}}. \tag{28}$$

N is the number of values averaged over, and n is the specific sample.

Temperature control

The temperature control is implemented as a cascaded control feedback loop, as seen in Figure 35. It comprises an inner current controller loop and an outer temperature control loop, providing the power reference for the current controller. The two voltage signals u_{out} and u_{temp} are extracted from the synchronous buck converter and the temperature sensor respectively. The inner loop is composed of the current controller previously presented. The inner discrete PI controller is tuned based on the derivations of the disturbance rejection based on the DS method. The commanded PWM voltage u_{PWM} is used to calculate the duty cycle, filtered with a discrete SMA where $N = 15$. Furthermore, this signal is fed into the PWM modulation block and scaled to the given period to get suitable CMPA input values for the PWM generation. The current reference is derived from the power reference P°_{out} shown at Figure 33, which is the output of the outer PID controller. The outer loop is composed of the discrete voltage signal from the infrared temperature sensor. This signal is filtered with an SMA with $N = 100$ for noise removal to ensure a stable but rapid response to temperature changes. As mentioned, calibration was performed to scale the voltage to obtain the corresponding temperature after the ADC conversion with a factor of 410/266. During the experiments, the reference temperature T_{ref} is rapidly adjustable online through the external mode in Simulink. This loop design proved to be viable due to the fast dynamic of the inner loop, whereas the outer loop is slow due to the nature of the temperature change in the heatsink setup with a significant thermal capacitance [112]. The PID controller gains were tuned using the Cohen-Coon tuning method, suitable for systems with prominent time delays, based on the estimated parameters $a = 1.4$, $L = 2$, and $T = 0.75$ [113]. This gave the following $K_p = 0.44$, $K_i = 0.35$ and $K_d = 2.12$.

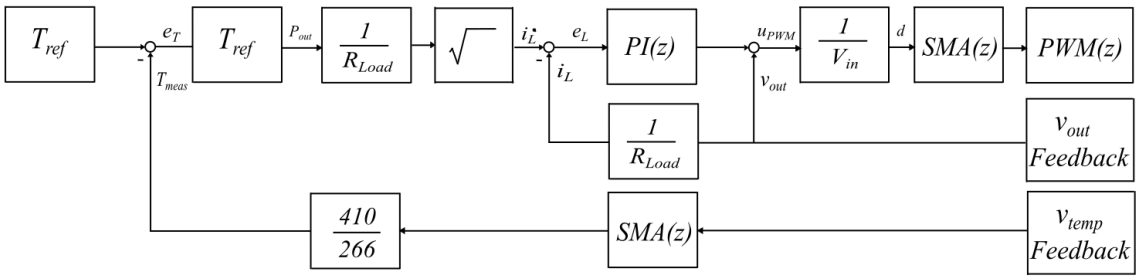


Figure 35: Temperature control scheme

4 Active temperature control framework

This chapter will present the proposed ATC scheme for ΔT_j reduction. Firstly, the features and characteristics of the four voltage levels AGD will be covered in detail. The general framework with its operational principles will be presented. Subsequently, the details of the specific elements of the framework, such as the electrical loss model, the thermal model, and the controller will be presented. The two load profiles used in simulations will be addressed. Two loss modulation schemes will be introduced at the end of the chapter. These were developed based on the switching-loss characteristic of the described AGD, with two different approaches for optimization of the control parameter selection with regard to the switching behavior.

4.1 Four voltage level active gate driver

This section introduces a four-voltage level active gate driver (4VLAGD) suitable for switching transient manipulation. The AGD is developed by Ekren et al. [23, 24], demonstrating the ability to alter the switching losses during turn-on and turn-off operation, in addition, to impacting the rate of current and voltage change dv/dt and di/dt during the commutation process.

The AGD circuit diagram is depicted in Figure 36. As seen, the topology consists of 3 half-bridges. Half-bridge 1 could either provide the supply voltages $V_{GG,on}$ or $V_{int,on}$ depending on whether Q_1 or Q_2 is conducting. Similarly, Half-bridge 3 determines if $V_{int,off}$ or $V_{GG,off}$ is provided by transmitting the appropriate gate signal to Q_5 and Q_6. Half-Bridge 2 selects if a charge or discharge process occurs for the DUT, referring to turn-on or turn-off operation if Q_3 or Q_4 is conducted. Three DC/DC adjustable low dropout regulators (LDOs) provide the given voltages seen Figure 36. Several isolated DC/DC converters provide the voltages applied to the adjustable LDOs [23]. Figure 38 illustrates the intermediate voltage supply levels $V_{int,on}$ and $V_{int,off}$ and their adjustable range and duration. This provides 4 degrees of freedom. In addition, the supply voltage $V_{gg,on}$ can be varied for conduction loss manipulation. The AGD is visualized in Figure 39.

Altering the switching process impacts the voltage overshoots V_{os} and reverse-recovery current overshoots I_{rr} at turn-off and turn-on respectively. A lower di/dt reduces the induced voltage due to the parasitic inductances causing the overshoots, whereas the switching transient duration influences the discharge process length of the intrinsic body diodes. Manipulating the duration of charge redistribution [23]. In the study of Ekren et al., a double pulse test (DPT) was conducted to examine the effect the AGD had on the overshoot and the switching losses. The DPT test setup can be seen in Figure 37.

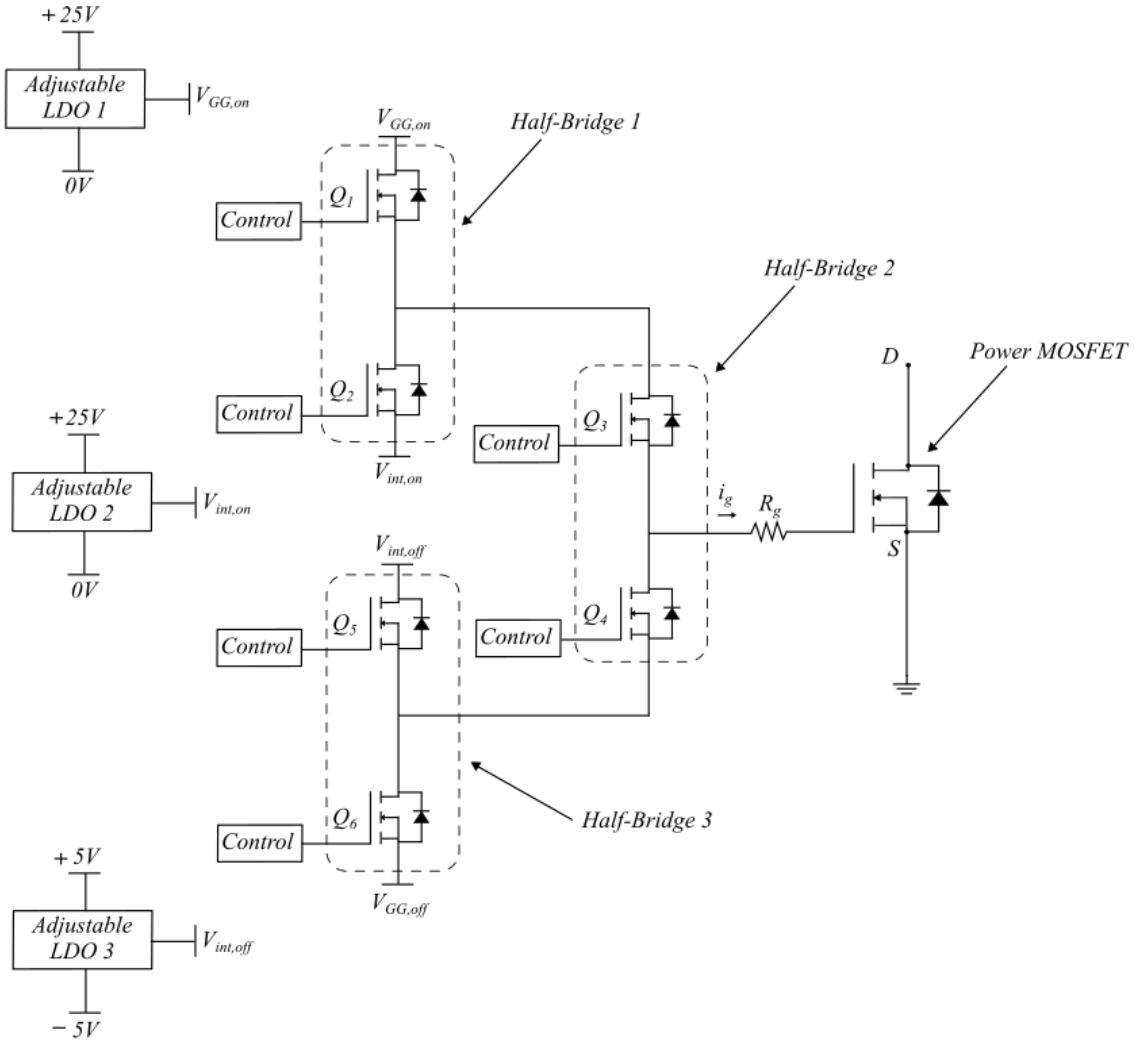


Figure 36: The schematic of the proposed active gate driver the simulations will be based on. Reconstruction of the schematic in [23].

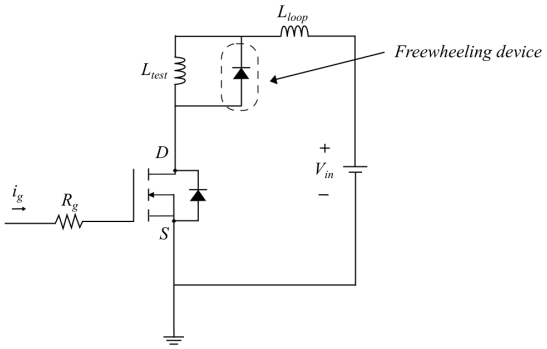


Figure 37: The double pulse test circuit with the AGD. Based on the schematic in [23].

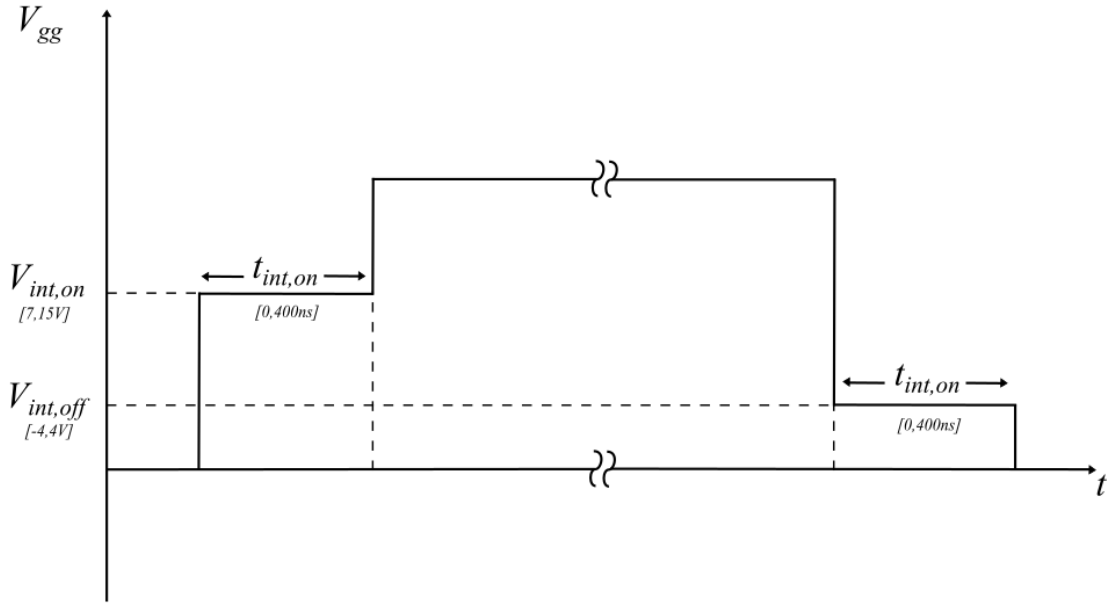
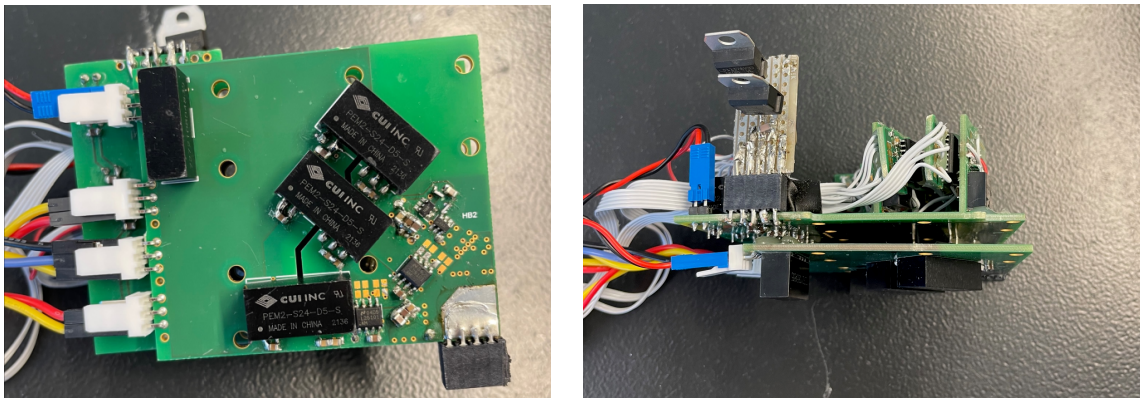


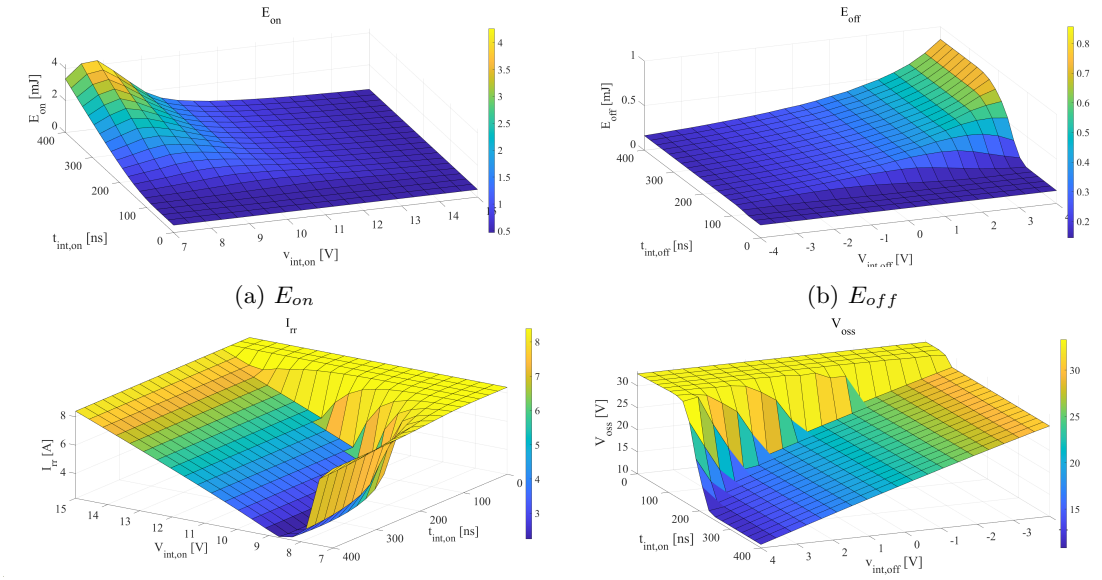
Figure 38: The schematic of the control variables for the four-level AGD, inspiration from [69].



(a) (b)

Figure 39: Photo of the four-voltage level active gate driver.

As indicated from Figure 40, altering the intermediate voltage levels and their duration could increase the switching energies E_{on} and E_{off}, hence, impacting the switching losses. It is evident from Figure 40, that the turn-on switching losses are three to five orders of magnitude larger than the turn-off switching losses. If looking at E_{on} and I_{rr} in a parallel analysis, a lower $V_{int,on}$ and larger $t_{int,on}$ provides a lower I_{rr}, until $v_{int,on}$ reaches 8V. Similarly, a side-by-side comparison of E_{off} and V_{os} indicates the same similarity. This is in accordance with the aforementioned theory, stating that a slower transient generated larger losses while reducing i_d and v_{ds} overshoots. It is also evident that when reaching a specific $t_{int,on}$ or $t_{int,off}$, a further increase does not lower the overshoot by any significant value.



(a) E_{on} (b) E_{off}

(c) I_{rr} (d) V_{os}

Figure 40: Loss and switching performance parameters [23].

The operational reference parameters, determining the steady-state performance for the two cases investigated in this thesis, are given in Table 3 and Table 4. This is respectively for the ideal and nonideal generation of references. Where the parameters from Table 4 provides the opportunity to both lower and increase the loss generation.

Table 3: Ideal reference intermediate voltages and durations

$V_{int,on,ref}$	$t_{int,on,ref}$	$V_{int,off,ref}$	$t_{int,off,ref}$
15V	0ns	-4V	0ns

Table 4: Nonideal reference intermediate voltages and durations

$V_{int,on,ref}$	$t_{int,on,ref}$	$V_{int,off,ref}$	$t_{int,off,ref}$
12V	100ns	0V	100ns

Switching loss normalization with respect to the load current

The switching-loss energies data E_{off} and E_{on} seen in Figure 40 were extracted at a load current of 20A by Ekren et al. [24]. In order to get a realistic value at a varying load profile, a normalization function based on the datasheet of the SiC MOSFET C3M0075120D [42] is employed. An exponential regression is implemented, providing the function in the form of

$$E_{norm,x} = E_x(0.3689 \cdot 1.0513^{I_{load}}). \tag{29}$$

The datasheet explicitly indicates a significant temperature dependence of the switching losses. Nevertheless, due to the uncertainty of how the temperature contributes to the performance of the AGD in switching-loss estimation, This thesis assumes this factor to be negligible. The assumption that the switching losses remain fairly unaffected by temperature in MOSFETs is supported by Mohan et al. [25].

4.2 Active junction temperature control framework

General framework

The objective of the ATC scheme is to reduce the ΔT_j, while simultaneously not influencing the converter operation to a large extent. The control framework is based on the aforementioned model by van der Broeck et al. [19], the active gate driver of Ekren et al. [23] and the thermal model of wang et al. [76]. A reference has to be generated, which is less susceptible to ΔT_j variations. A concept called virtual heatsink based on van der Broeck et al. [19] work is utilized for generating a superior reference with regard to ΔT_j reduction. For simulation purposes, accurate electro-thermal characterization is beneficial. Therefore, the findings from the aforementioned electro-thermal characterization experiment are utilized for conduction loss estimation. The switching loss estimation applies AGD data from Ekren et al. [23]. The ensuing simulation model will be subjected to analysis and presentation.

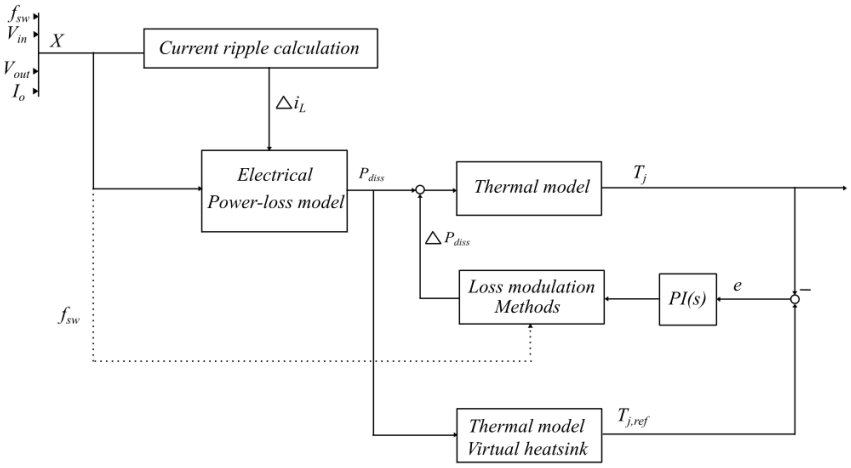


Figure 41: Framework of the proposed ATC.

The Matlab/Simulink [114] interface was employed for generating the model and for simulation purposes. As seen in Figure 41, the converter state parameter, such as the switching frequency f_{sw}, load current I_o, the input voltage V_{in} and the load voltage V_o for a synchronous buck converter is applied as a reference to the loss model. The current ripple Δi_L being of significance in the conduction losses and switching losses is calculated. The electrical loss model which will be described in detail, outputs a given power dissipation P_{diss} for the varying i_o. This power dissipation is given as an input to the thermal model and a virtual heatsink thermal model. The virtual heatsink model provides an output $T_{j,ref}$ profile that acts as a more optimal reference. The error from the given real T_j and the reference T_j from the virtual heatsink model is given as an input to the PI regulator, commanding a complimentary switching power-loss compensation for reference tracking, in the case of the converter operating at the optimal state. The total commanded power losses are given to a loss modulator for calculating the optimal combination values of the control variables. The components of this framework will be covered in detail in the following section. The ambient temperature T_a is assumed to be constant at 25° C under all simulations. The converter state parameters are described in the Table 5.

Loss model

To predict the heat dissipation and temperature distribution under different system conditions and load profiles, a synchronous buck converter topology was used as the basis for power loss dissipation for this ATC scheme. Thus, an estimation of electric behavior causing heat dissipation can be analyzed in this configuration. The circuit diagram is visualized in Figure 42.

Table 5: Operational parameters

Switching frequency f_{sw}	100kHz
Load current I_o	Load profiles
System voltage V_{in}	800V
Output voltage V_o	$400V$
Ambient temperature T_a	25° C
Inductance L	$2.2mH$

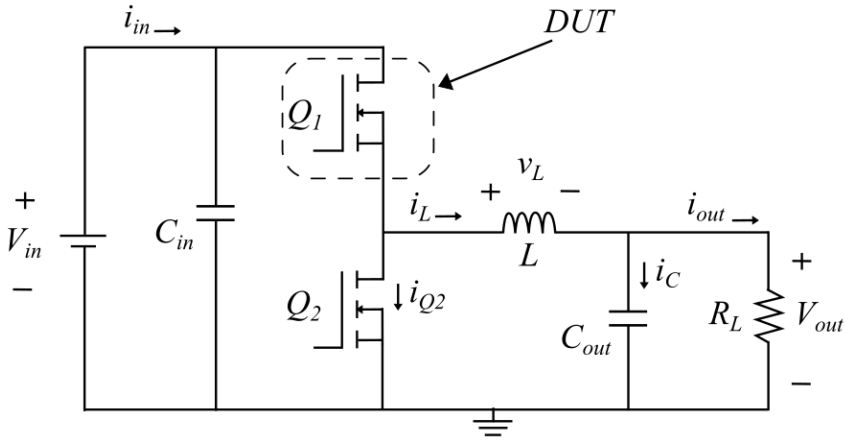


Figure 42: Synchronous buck converter circuit diagram.

The synchronous buck configurations are previously examined in Chapter 3 for the electro-thermal characterization experiment. The converter comprises a half-bridge of SiC MOSFET Q_1, Q_2, an inductor L, and a capacitor C for voltage filtering purposes [115]. C is assumed to be sufficient to stabilize the output voltage at a constant V_{out}. L was chosen to $2.2mH$, similar to the real converter in Chapter 3. The load is simulated as a varying load current i_{out} at a constant $V_{out} = 400V$.

The power losses associated with the SiC MOSFETs in this configuration are the conduction losses in both MOSFETs, the switching losses in the upper MOSFET, and body diode losses in the lower MOSFET. This is due to the voltage over the low-side MOSFET being clamped by the forward body diode voltage. This voltage is low in comparison to V_{in}. Hence, the switching losses of low-side MOSFET are neglected. For the sake of simplification, the losses attributed to the stored energy in C_{oss} and the losses associated with the gate driver are disregarded. Consequently, the overall losses for the converter can be represented as follows [115]

$$P_{tot} = P_{sw,Q1} + P_{cond,Q1} + P_{cond,Q2} + P_{bd,Q2}. \tag{30}$$

For investigating the ATC schemes effect on a discrete SiC MOSFET, the upper MOSFET is chosen as the DUT.

Switching losses

The switching losses, as mentioned in Figure 7 correspond to the instances of v_{ds} and i_d both being significant in value. Including the current ripple in a synchronous buck converter topology, the switching losses of the upper switch can be expressed based on [115] and the normalization to the load current

$$P_{sw,Q1} = E_{on}(0.3689 \cdot 1.0513^{(I_o - \frac{\Delta i_L}{2})}) \cdot f_{sw} + E_{off}(0.3689 \cdot 1.0513^{(I_o + \frac{\Delta i_L}{2})}) \cdot f_{sw}. \tag{31}$$

In the model used in this ATC framework, f_{sw} and the effect of the current ripple $I_o - \frac{\Delta i_L}{2}$ and $I_o + \frac{\Delta i_L}{2}$ is used with lookup tables of the switching energies E_{on} and E_{off} from the AGD for P_{sw} calculation.

Conduction-losses

Conduction losses in SiC MOSFETs can be derived as a function of the duty cycle D, load current I_o, and current ripple Δi_L, taking into account the temperature dependency of the internal resistance R_{DSon}. The conduction loss can be expressed as the following [115] in a simplified model

$$\begin{aligned} P_{cond,Q1} &= R_{HS,DSon}(T) \cdot I_o^2 \cdot D \cdot (1 + \frac{1}{12}\frac{\Delta i_{Lpp}^2}{I_o^2}) \\ P_{cond,Q2} &= R_{LS,DSon}(T) \cdot I_o^2 \cdot (1 - D) \cdot (1 + \frac{1}{12}\frac{\Delta i_{Lpp}^2}{I_o^2}). \end{aligned} \tag{32}$$

In the implementation of the model in Simulink, the factor $R_{DSon}(T)I_o^2$ is switched with the equivalent factor $V_{ds}(T) \cdot I_o$ from the ID-VDS data. As noted in [27, 42], R_{DSon} is highly sensitive to temperature in SiC MOSFETs.

Reverse recovery body-diode losses

The LS intrinsic diode will experience a significant body-diode loss during commutation. This can be expressed as the sum of the body diode reverse recovery losses P_{drr} and body diode conduction losses P_{dead} throughout the dead time

$$P_{bd,Q2} = P_{drr} + P_{dead} = V_{ds} \cdot Q_{RR} \cdot f_{sw} + V_f(I_o - \frac{\Delta i_{Lpp}}{2}) \cdot t_{dr} \cdot f_{sw} + V_f(I_o + \frac{\Delta i_{Lpp}}{2}) \cdot t_{df} \cdot f_{sw}. \tag{33}$$

Q_{rr} represents the reverse recovery charge of the body diode, where V_f denotes the forward voltage of the diode, t_{dr} and t_{df} refers to the dead time during turn-off, dead time during turn-on respectively [115].

Since the DUT in this thesis is the upper SiC MOSFET, these losses are not accounted for in the simulations as they refer to the lower SiC MOSFET. However, it was implemented for the versatility of the model in further investigations. The accuracy of this estimation may also be challenged as some of the charge Q_{rr} may be recovered during commutation.

Control algorithm

The resemblance to the resistor-less gate driver ATC, as proposed by Ding et al. [20] lies in the ability to make continuous adjustments. As mentioned, the adjustable LDOs can regulate the intermediate voltages $V_{int,on}$, $V_{int,off}$ and $V_{gg,on}$ and the duration in a continuous fashion. A PI regulator is implemented for the purpose of providing the ΔP_{sw} contribution for reference tracking, because of the difficulties of generating a mathematical relationship between the nonlinearity of the loss modulator and thermal model, the regulator is tuned to reduce the overshoot where $K_p = 10$ and $K_i = 20$ provided an adequate response. A saturation is implemented to eliminate any windup issues. The ΔP_{sw} is provided as the input for the two modulation schemes introduced later in this chapter for parameter selection.

The efficiency of the upper MOSFET in the converter, referred to in the text, is defined as

$$\eta = \frac{P_{out}}{P_{in}} = \frac{P_{out}}{P_{out} + P_{sw,Q1} + P_{cond,Q1}}. \tag{34}$$

4.3 Thermal model and virtual heatsink

Thermal model

To predict the heat dissipation and temperature distribution under different system conditions and load profiles, a Cauer-network is utilized as presented in Figure 16. The justification for this is the satisfactory accuracy and computation efficiency a 1D-lumped model provides for investigating the effect of this ATC scheme.

A Cauer-network modeling of the transient response can be presented as a state-space representation [55]. The distinct temperature distribution of all the layers of different materials can be extracted in the Cauer-network as compared to the Foster-network, referring to Figure 15. The state space representation used in this thermal model can be expressed as [55]

$$\frac{d\overline{T}}{dt} = A \cdot \overline{T} + B \cdot \overline{P_{diss}} \qquad \overline{T} = C \cdot \overline{T}.$$

In response to being subjected to excitation, the system matrix A represents the dynamic transition occurring within the system. The influence of inputs on the system states is expressed by the control matrix B, whereas the measurement matrix C can be augmented in order to achieve the desired output by adjusting its scale. $\overline{T}$ is the temperature distribution vector and $\overline{P_{diss}}$ is the power dissipation vector describing the heat transfer occurring at each layer [55]. In this instance, it describes the heat transfer that occurs at the location of the cell of the MOSFET module due to the electric power losses and the ambient temperature at the heatsink [55]. The derivation of the A matrix can be expressed as [76]

$$\begin{aligned}
\frac{dT_1}{dt} &= T_1\frac{-1}{C_1R_1} + T_2\frac{1}{C_1R_1} + P_{diss}\frac{1}{C_1} \\
\frac{dT_2}{dt} &= T_1\frac{1}{C_2R_1} - T_2(\frac{1}{C_2R_1} + \frac{1}{C_2R_2}) + T_3\frac{1}{C_2R_2} \\
\frac{dT_3}{dt} &= T_2\frac{1}{C_2R_2} - T_2(\frac{1}{C_3R_2} + \frac{1}{C_3R_3}) + T_3\frac{1}{C_3R_3} \\
&\vdots \qquad\qquad \vdots \qquad\qquad \vdots \qquad\qquad \vdots \\
\frac{dT_{n-1}}{dt} &= T_2\frac{1}{C_{n-1}R_{n-2}} - T_2(\frac{1}{C_{n-1}R_{n-2}} + \frac{1}{C_{n-1}R_{n-1}}) + T_3\frac{1}{C_{n-1}R_{n-1}} \\
\frac{dT_n}{dt} &= T_2\frac{1}{C_nR_{n-1}} - T_2(\frac{1}{C_nR_{n-1}} + \frac{1}{C_nR_n}) + T_{amb}\frac{1}{C_nR_n}.
\end{aligned} \tag{35}$$

$$A = \begin{bmatrix}
\frac{1}{C_1R_1} & \frac{1}{C_1R_1} & 0 & 0 & \cdots & 0 & 0 \\
\frac{1}{C_2R_1} & -\frac{1}{C_2R_1} - \frac{1}{C_2R_2} & \frac{1}{C_2R_2} & 0 & \cdots & 0 & 0 \\
0 & \frac{1}{C_3R_2} & -\frac{1}{C_3R_2} - \frac{1}{C_3R_3} & \frac{1}{C_3R_3} & \cdots & 0 & 0 \\
\vdots & \vdots & \ddots & \ddots & \ddots & \vdots & \vdots \\
\vdots & \vdots & \ddots & \ddots & \ddots & \vdots & \vdots \\
0 & 0 & 0 & \ddots & \ddots & \ddots & \vdots \\
0 & 0 & 0 & \cdots & \frac{1}{C_{n-1}R_{n-2}} & -\frac{1}{C_{n-1}R_{n-2}} - \frac{1}{C_{n-1}R_{n-1}} & \frac{1}{C_{n-1}R_{n-1}} \\
0 & 0 & 0 & 0 & \cdots & \frac{1}{C_nR_{n-1}} & -\frac{1}{C_nR_{n-1}} - \frac{1}{C_nR_n}
\end{bmatrix} \tag{36}$$

C_n is the thermal capacitance C_{th} and R_n is the thermal resistance R_{th} of each segment, respectively. For simulation purposes, the utilized Cauer thermal model parameters originated from a study of the thermal behavior of a discrete TO-247 Si MOSFET package. The parameters were estimated using a simulation analysis approach and summarized in Table 6 [116]. Referring to Figure 15, $R_{th,2}$ and $R_{th,3}$ corresponds to $R_{th,2}$ in Table 6 and similar for the thermal

capacitance. Therefore, the $R_{th,7}$ and $C_{th,7}$ will correspond to the heatsink parameters and not the baseplate. These parameters would likely differ some from the actual realistic values of the discrete C3M0075120D SiC MOSFET. However, it represents a thermal model that captures the rapid thermal dynamics of the inner material layers, with parameters in a similar range due to the similar package style.

A heatsink of the type RA-T2X-25E from Ohmite [117] is used for simulation purposes, assuming an air velocity of $1000 ft/min$ providing a $R_{th} = 0.5$. The thermal capacitance is estimated using the specific capacitance of aluminum 0.9 [J/gK] times the weight of 25g, providing a $C_{th} = 22.5$.

Temperature state	R_{th} $[°C/W]$	C_{th} $[J/°C]$
T_{jv}	0.00311	0.001056
T_{s1}	0.01074	0.0009371
T_{Cu1}	0.0698	0.0009228
T_{AIN}	0.1959	0.003488
T_{Cu2}	0.1959	0.01427
T_{s2}	0.1165	0.07497
T_c	0.5	22.5

Table 6: R_{th} and C_{th} parameters.

By incorporating constants in the second column, it becomes feasible to model fluctuations in the ambient temperature or implement the effect of fans or other cooling systems. Whereas the other input parameters are the power dissipation and ambient temperature T_a [76].

$$B = \begin{bmatrix} \frac{1}{C_1} & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & 0 \\ \vdots & \vdots & \vdots \\ 0 & 1 & \frac{1}{C_n R_n} \end{bmatrix} \tag{37}$$

$$C = I \tag{38}$$

Virtual Heatsink

The virtual heatsink design is revolved around increasing the dynamic time constant τ of the thermal model while providing the same steady-state response [19]. Therefore, by adjusting C_{th}, a similar steady-state behavior is achieved, whereas the dynamic response is significantly slower. This essentially acts as a low-pass filter, and the approach can be expressed as

$$\overline{C_{virt}} = c_v \cdot \overline{C_{th}}. \tag{39}$$

c_v is a factor used to augment the thermal capacitances vector to the original thermal structure. Applying the virtual heatsink as a reference generator, a trajectory with lower peaks is expected compared to the real thermal model due to the filtering of the high-frequency load variations. Therefore, the ΔT_j is expected to be lower when the MOSFETs are exposed to large load variations. In the instance of lower variations, the reference will follow the steady-state response due to the non-altered R_{th} [19].

The concept of a virtual heatsink reference can be visualized in Figure 43. It is evident that the reference generated at an elevated c_v reduces ΔT_j, at the same time, the average temperature T_m is in a similar order of magnitude.

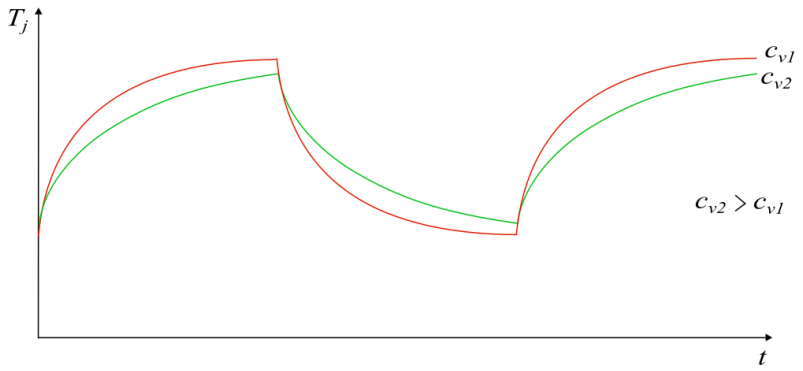


Figure 43: The virtual heatsink concept.

4.4 Load profiles

Step response

In order to examine the performance of the ATC, two load profiles are used. First, a step load profile provides the opportunity to analyze the effect of a load change. Thus, distinct responses can be observed when the ATC is configured with different c_v. The step response is fundamental for depicting how the ATC could increase the losses for tracking the reference trajectory of the virtual heatsink model. The step response employed for simulation purposes is illustrated in Figure 44 sharing similarities with the load profile in [16]. It consists of a 15A step, followed by two steps of ±3A and two steps of ±5A respectively.

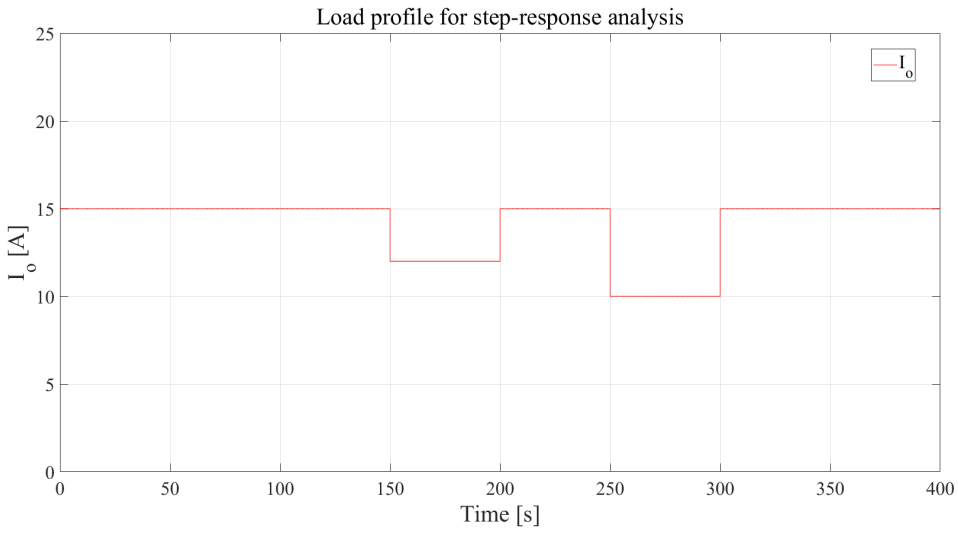


Figure 44: Load profile with steps for investigating the step response. Inspiration from [16].

Solar generated load profile

A more realistic load profile is used for investigating how the ATC would operate under a more stochastic load profile. Average global solar irradiance data is acquired from Norsk Klimaservicesenter [118] for the May 2nd 2023 at Gløshaugen weather station. This irradiance data profile is normalized with a factor of 20/1000 to gain a realistic output current within the limitations of the DUTs rated current. This results in the load profile depicted in Figure 45. The linear relationship of Irradiance and I_o for solar cells is valid for simplified models, supported by [119].

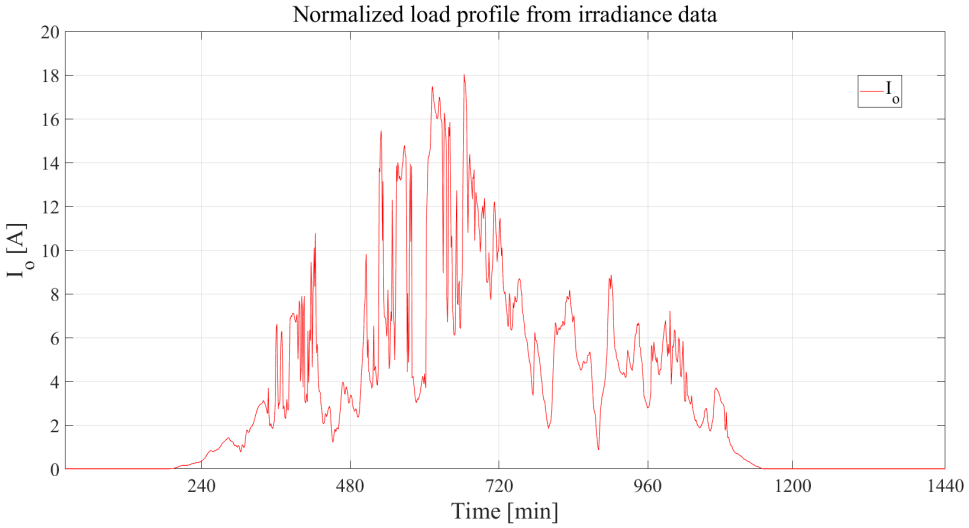


Figure 45: Load profile based on irradiance data on the May 2nd 2023 from Gløshaugen weather station [118].

4.5 Multivariable optimization of active gate driver operational parameters

The 4VLAGD provides the means to explore the optimization of switching parameters due to the 4 degrees of freedom. In this section, two approaches to optimizing the switching overshoot parameters V_{os} and I_{rr} with respect to $t_{int,on}$, $v_{gs,int,on}$, $t_{int,off}$, and $v_{gs,int,off}$ are presented. The optimization problem can be described as; Minimize the objective function

$$G = w_1 I_{rr}(t_{int,on}, v_{int,on}) + w_2 V_{os}(t_{int,off}, v_{int,off}), \tag{40}$$

subjected to

$$P_{req} = f_{sw}(E_{on}(t_{int,on}, v_{int,on}) + E_{off}(t_{int,off}, v_{int,off})). \tag{41}$$

Where f_{sw} and P_{req} is the switching frequency and the required power loss of the MOSFET, and the variables $t_{int,off}$ $v_{int,on}$, $t_{int,off}$ and $v_{int,off}$ are constrained to the aforementioned intervals in Chapter 3.5. I_{rr} and V_{os} are weighted with w_1 and w_2.

As Illustrated in Figure 40 the dataset of I_{rr}, V_{os}, E_{on} and E_{off} can be expressed as $20x20$ matrices. The multivariable optimization will be called for each sample time of the ATC simulation. The desired solution will provide the required feasible P_{req} where G is minimized. The switching losses E_{on}, E_{off} and performance parameters I_{rr}, V_{os} are normalized to the load current with the aforementioned function (29). Two approaches examined in this thesis will be presented.

Gradient descent method

This approach was first implemented for a fairly accurate solution at the cost of larger computational demand. An iterative method is introduced based on gradient descent. Therefore, the gradient of these four matrices needs to be computed. The algorithm moves from an initial guess of coordinates given a fraction of E_{on} and E_{off}, which combined is closest to E_{sw}. Then, based on the coefficient of the gradients of V_{os} and I_{rr}, the algorithm moves over the 20x20 coordinate plane. An inner loop, composed of a similar approach, ensures the E_{sw} is within a given tolerance band of 0.01 for the simulations conducted in this thesis. At a specified number of iterations, it exits the loop and provides the given control parameters $t_{int,on}$, $V_{int,on}$, $t_{int,off}$, and $V_{int,off}$.

Heuristic Optimization

A solution based on large sorted vectors is implemented to explore a heuristic approach that could be viable for implementation in real simulations. The outline of this method involves sorting a large data set of E_{sw}, a binary search algorithm, a minimum search function, and a backtracking algorithm illustrated by Figure 46.

First, a vector E_{sw} of all the possible combinations of switching energies is implemented. The indices of this vector can be backtracked to the given combination of E_{on} and E_{off}. This vector is then presorted, with another vector remembering the indices. A vector consisting of all the possible combinations of G is implemented in the same fashion. However, this vector is sorted with respect to the sorted indexes of the $E_{sw,sort}$.

A binary search algorithm [120] is then implemented for searching the sorted list for the E_{sw} requested by the controller, delivering the index and value of the E_{sw} nearest.

Further, the algorithm does a minimum search of a n large interval around the index of the binary search algorithm in G_{sort}. This interval can be specified for performance purposes. The index corresponding to the lowest value of G_{sort} is retrieved, with an index in proximity to the search from the binary search algorithm. Therefore, due to the size of 160000 combinations, a comparable E_{sw} to the value given by the binary search is expected unless in the outer ends of E_{sort}. Since the first vectors remember the indices, backtracking is realizable to obtain the corresponding $t_{int,on}$, $v_{int,on}$, $t_{int,off}$ and $v_{int,off}$. Therefore, the algorithm outputs the mentioned parameters and the switching losses $P_{sw} = E_{sw} f_{sw}$, where f_{sw} is the switching frequency of the converter.

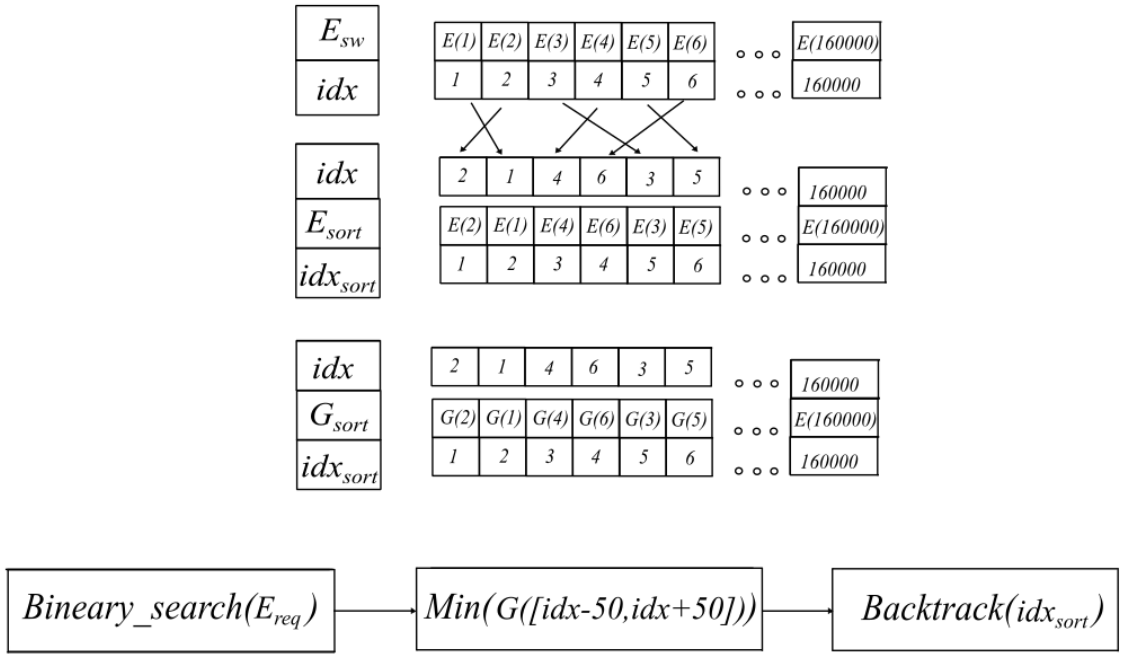


Figure 46: The index tracking of the heuristic approach.

5 Results and discussion

In this chapter, the findings from the electro-thermal characterization of the C3M0075120D SiC MOSFET are presented and discussed. In addition, remarks on the accuracy and validity of this approach for the electro-thermal characterization of a SiC MOSFET will be addressed. Secondly, the results from the simulations of the ATC framework for ΔT_j reduction will be presented. The T_j response to the step and more realistic normalized solar load profile is covered. Additionally, an assessment of the active temperature control framework with a comprehensive analysis of the simulation results will be provided. Highlighting the influence of the chosen method on the overall objective of this thesis and discussing the impact of the simplifications implemented within the model. In the end, the influence of the two loss-modulation schemes based on the aforementioned multivariable optimization algorithms will be emphasized.

5.1 Electro-thermal characteristic

Transfer characteristic

The result of the transfer characteristic is shown in Figure 47 of the static characterization experiment. T_j is the estimated junction temperature equal to the measured case temperature from the thermocouple. As discussed in Chapter 2.2, the transconductance g_m and the SiC MOSFETs behavior in the active region is temperature-dependent. This is prominent by a shift in the transfer curve towards the left, supported by Wang et al. [9].

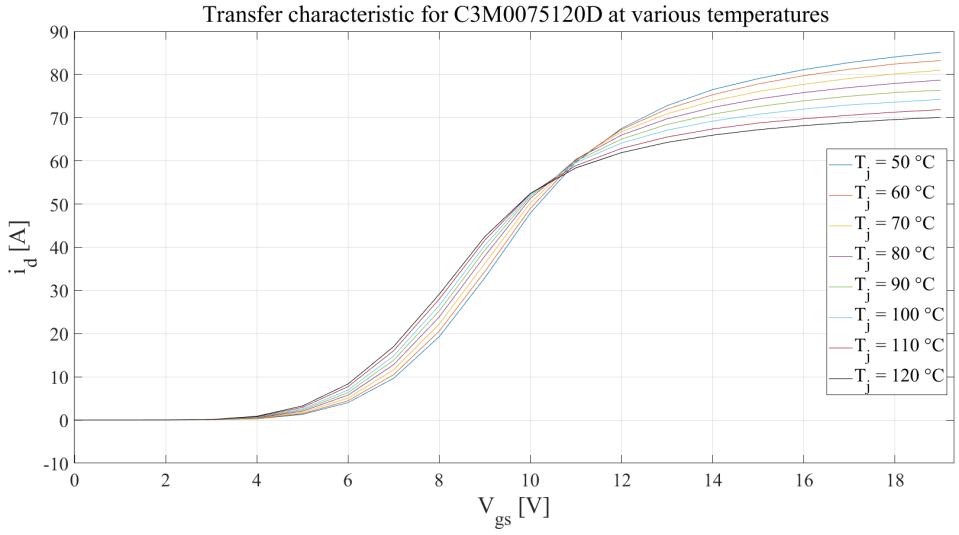


Figure 47: The transfer characteristic of the DUT.

In the Figure 47, $V_{gs,th}$ shifts to the left at elevated temperature, corresponding to a lower $V_{gs,th}$. This is in accordance with the presented theoretical foundation [4, 9] and the datasheet [42]. The transconductance g_m increases at low currents and low V_{gs}, evident by the steeper slope. As aforementioned, the increased g_m could indicate faster switching transient and higher switching speeds [26]. However, the SiC MOSFETs at high i_d and high V_{gs} are restricted by the increased $R_{ds,on}$ at elevated temperature, indicated by the transition around $V_{gs} = 10.5V$. There g_m has a negative temperature coefficient compared to the low-current region. This is consistent with Wang et al. [121], Ceccerali et al. [93], and Lu et al. [33] findings. Wang et al. [121] argue that this transition is due to the opposite temperature coefficient of the channel resistance and the drift-region resistance and their impact at different V_{gs}. The positive dependency of g_m on di/dt and dv/dt is presented in [9]. In the research studies of Ceccarelli et al. [93] and Wang et al. [121], the effect of the various temperatures on the switching waveforms are examined. It is observed that the increased temperature produces slightly larger oscillations in the i_d switching waveform. The

origin of this phenomenon could be associated with the dependency of di_d/dt on g_m. Ceccarelli et al. [93] emphasize that the parasitic capacitances are likely not the cause because of them being relatively unaffected by temperature variations. Moreover, the graph illustrates the issue of SiC MOSFET with a typically low $V_{gs,th}$ operating at high temperatures, being more susceptible to crosstalk due to the negative temperature coefficient [41].

ID-VDS characteristic

The results from ID-VDS characteristic for varying temperatures in the interval of $T_j \in [50, 120]$°C at $V_{gs} = 15$ V can be observed in Figure 48. At elevated temperatures, the ID-VDS curve has a significantly lower steepness for high V_{ds}. This is as presented in Figure 4 as a representation of the intrinsic resistance during conduction $R_{ds,on}$. The larger V_{ds} voltage drop at elevated temperatures corresponds to the theoretical foundation [6, 25, 26]. With the increased temperature, the carrier mobility in the drift region diminishes, indicating a positive temperature coefficient for $R_{ds,on}$ [25]. It can be seen for $V_{gs} = 9V$ in Figure 48 that the coefficient switches. This can be observed in connection with Figure 47. At $V_{gs} = 9$V and high temperature, the transfer characteristic indicated a higher g_m and lower $V_{gs,th}$. Therefore the SiC MOSFET turns on at a lower V_{gs}, and a have a higher current capability at low V_{gs}. As indicated by Wang et al. [121], the competition between the negative temperature coefficient of the channel resistance and the positive coefficient of the drift region resistance is evident. It is apparent in Figure 48 at $V_{gs} = 9$V that the active region is perceptible. The elevated temperature, as mentioned, indicates an increased $R_{ds,on}$ and a higher drain-source voltage drop V_{ds} at a given I_d. Therefore, in the transfer characteristic experiment at a constant V_{ds}, the i_d at high temperatures will be larger at lower V_{gs}, whereas the temperature effect on i_d switches closer to the ohmic-region when the MOSFET is fully turned on and the effect of the temperature on $R_{ds,on}$ exerts as a more determining factor. This aligns with a fully formed conductive channel in the base region when operating in the ohmic region.

The findings in the ID-VDS and transfer characterizations experiment share similarities with the referred research studies. This supports the indications of a successful experiment. Particularly, the quite uniform shift for each sample size indicates an effective and accurate temperature controller. The experimental measurements had temperature variations with a deviation of maximum ±0.6°C.

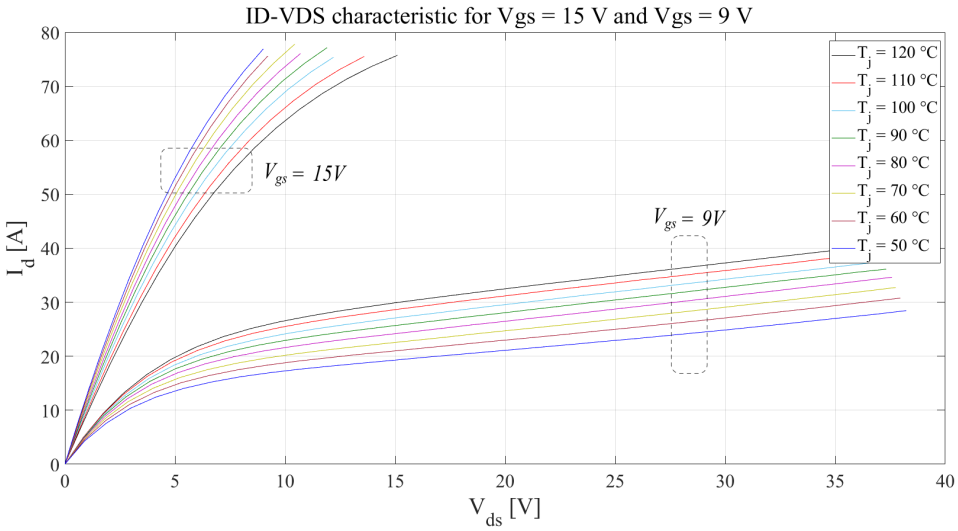


Figure 48: ID-VDS characteristics

For illustrative purposes and validation, the resulting ID-VDS graph for a temperature of 100°C is shown in Figure 49. The elevated conduction losses at higher temperatures are depicted in Figure 50 for a $V_{gs} = 15V$. A significant increase in the instantaneous power dissipation P_{cond} can be observed at raised temperatures.

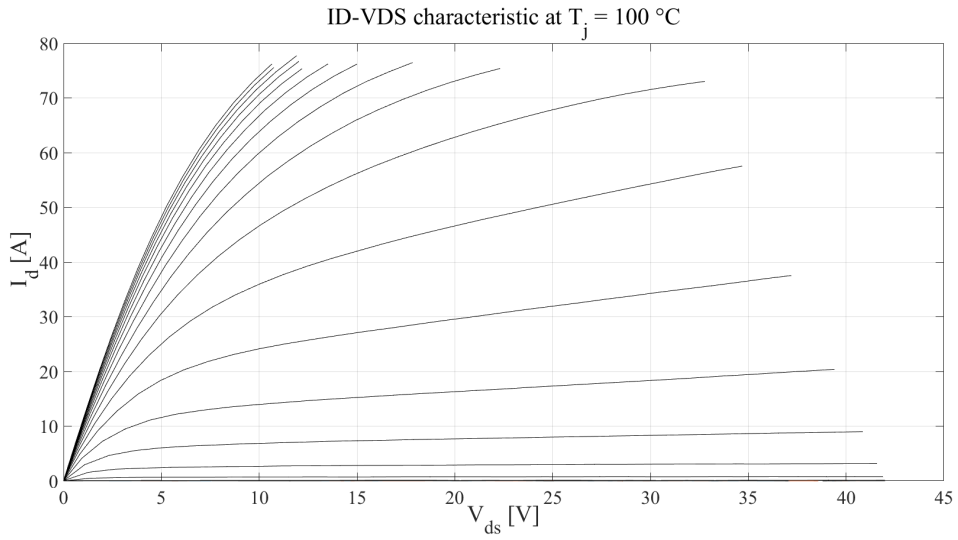


Figure 49: ID-VDS characteristics at $T_j = 100°C$.

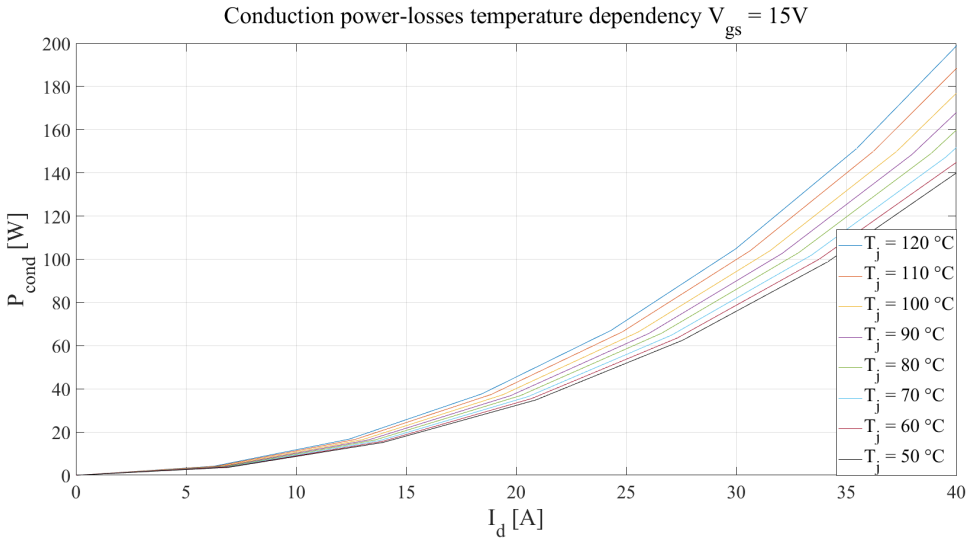


Figure 50: Conduction losses temperature dependencies at $V_{gs} = 15V$.

Temperature controller and the accuracy of the method

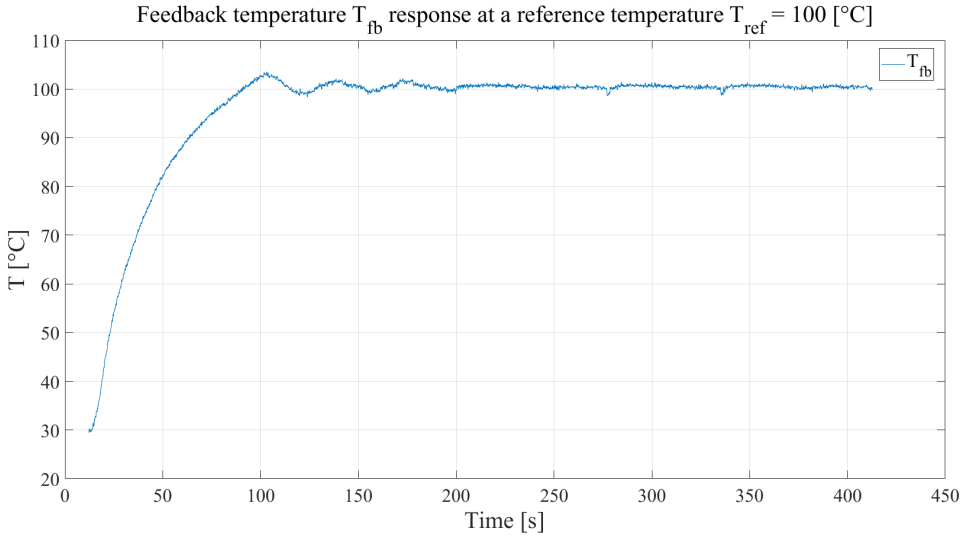


Figure 51: Temperature control with a $T_{ref} = 100°C$.

The response of the temperature controller in heating the resistors to a reference of $T_{ref} = 100°C$ using the Figure 35 is shown in Figure 51. The controller manages to follow the set reference. However, there are some damped oscillations. The large oscillations are in the $\pm 2°C$, whereas the occasional noise causes some dips in the $1°C$ interval. As presented in Chapter 3.3, the resolution of the infrared sensor could be one of the sources of the noise signals. The accuracy of the feedback signal is also dependent on the correct aiming at the black resistor and the emissivity of the aimed material. It should be noted that the feedback temperature reading is of the black resistors seen in the Figure 21, therefore the feedback of the temperature sensor is not of the temperature of the MOSFET due to the reflection of the steel clip attachment for fixing the MOSFET. As mentioned, a thermocouple was placed on the case for verification of the case temperature of the MOSFET, which is the temperature reading used for estimating the T_j. A fairly large temperature drop from the resistive heating element to the case temperature was observed. Due to the given placement of the thermocouple and the direction of heat transfer, the junction temperature of the MOSFET would likely be slightly higher than the estimated value. Indicating some uncertainty in the estimated junction temperature.

In hindsight, an alternative approach of using the thermocouple temperature measurements as feedback could have eased the calibration process and improved the accuracy slightly. Thus removing the necessary calibration effort for each test. The PID controller successfully tracked the reference T_{ref}. Nevertheless, further tuning could potentially result in amplified performance.

The highest obtainable temperature reading at the SiC MOSFET case was 120°C. This is due to the thermal rating of the resistors of 175°C. The heat dissipation performance of the heatsinks resulted in the restriction of achievable temperatures at the DUT. Trimming of the heatsink fins would likely increase the temperature range at the DUT of this experimental setup.

5.2 Active temperature control simulation ideal operational reference

Virtual heatsink references

To explain the ATC structure, we will look at the references generated by the virtual heatsink at varying c_v first, then propagate through the system from the control directive over the reference and the AGD parameter choice to the efficacy of the loss modulator. The ATC reference trajectories for the two load profiles will be presented first in this section. The step response can be depicted

in Figure 52, visualizing the smooth references for each c_v. The curve illustrated by $c_v = 1$ corresponds to the natural estimated T_j response from the thermal model when subjected to the step load profile. In other words, the expected temperature trend, since the thermal capacitances are not augmented. It can be seen that the fast dynamics of the inner material layers of the SiC MOSFET package provide a rapid temperature increase when subjected to the step profile. It is observed that the T_j reference trajectories for different c_v converge after an unspecified time. Illustrating the principle of equal steady-state behavior with this virtual heatsink scheme. It is evident that the reference for $c_v = 10$ generates the optimal reference of the ones simulated, seen by the reduction in ΔT_j, when subjected to the different load steps. These references are generated with the ideal operational parameters from Table 3.

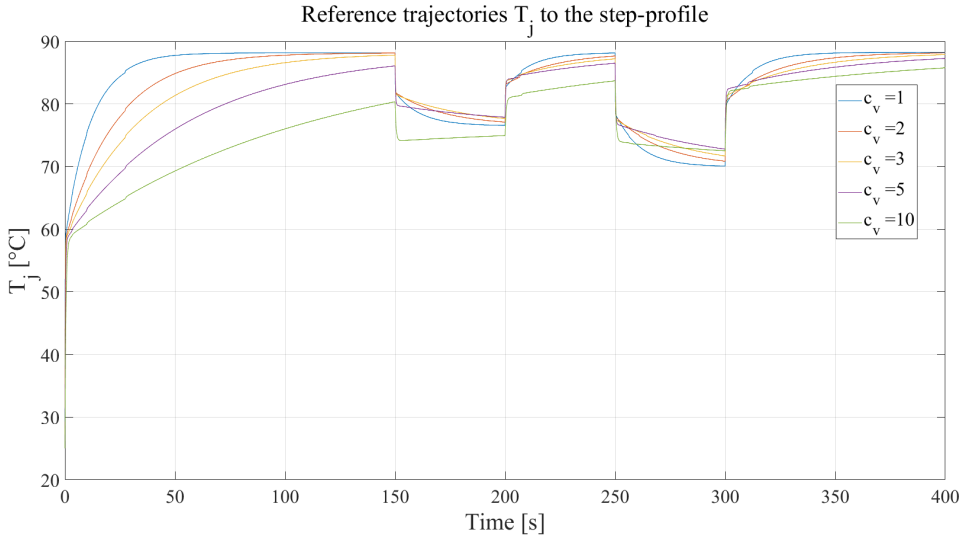


Figure 52: Trajectory reference for the ATC framework for a step response.

The reference generation for the solar load profile is shown in Figure 53. It is apparent that the virtual heatsink concept provides reference trajectories, which reduces the amplitude ΔT_j. This is particularly noticeable, at the occurrence of rapid load variations of great magnitude, evident at the 360 min mark, in contrast to the slow load variations observed at 240 min. One of the tradeoffs of the ATC approach can be observed in the gradual decline in load-current at a time equal to 840 min. In the instance of loss compensation, the optimal c_v would likely have to be determined with respect to the optimization of RUL and efficiency. This is due to the trade-off of compensating the losses for ΔT_j reduction and increased losses. Too large c_v would decouple the reference from the natural T_j trajectory, resulting in a reference that could not necessarily provide an option for the controller to generate more losses for ΔT_j reduction. This can be illustrated by the $c_v = 10$ for the step response since this reference is lower than the natural T_j profile at $c_v = 1$. Thus, the controller has no leverage to increase the losses for reference tracking.

The ambient temperature conditions are 25°C. Consequently, the non-zero switching losses due to the imperfect normalized load current function generate some heat dissipation, causing the temperature right before daylight to be slightly elevated. This is a potential improvement for further model development to improve the accuracy at low temperatures.

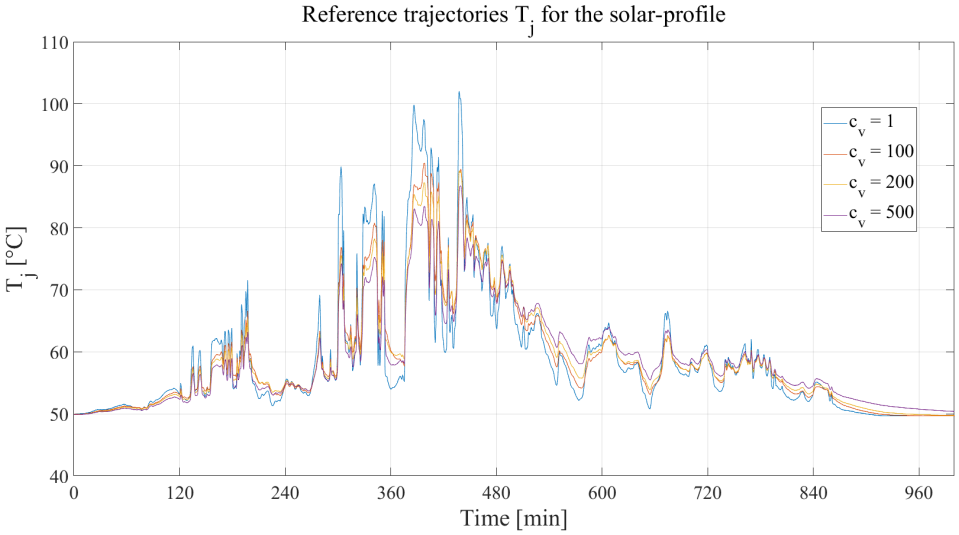


Figure 53: Trajectory reference for the ATC framework based on a normalized load profile of the irradiance may 2nd 2023.

Step response

In Figure 54, the T_j trajectory can be observed. The controller follows the reference, and lower ΔT_j can be observed with the gradient descent method. The heuristic approach generated a similar indistinguishable response since both approaches successfully mirrored the reference when possible. Thus only one of the figures is shown. This indicates the feasibility of this type of ATC scheme. A question that could be raised is the bandwidth of applicable values for c_v. In the case of the c_v moving towards infinity, the thermal capacitance would act as an infinitely large heatsink. Therefore, a reference equal to the ambient temperature would be expected because the time constant becomes infinite. In the case of a converter operating with the most efficient operational parameters, the T_j reference trajectory would be below the natural T_j path. Therefore, the controller would not be able to influence the ΔT_j leading to the ATC framework only having leverage to increase the losses as a means to reduce the fluctuations due to the reference being lower than the real system trajectory. Consequently, reduction of the upper part of the cycles will not be achievable, limiting the influence of the controller. This can be observed for $c_v = 10$ at the time of 300s, in the case of $c_v = 5$ providing a superior response for ΔT_j reduction.

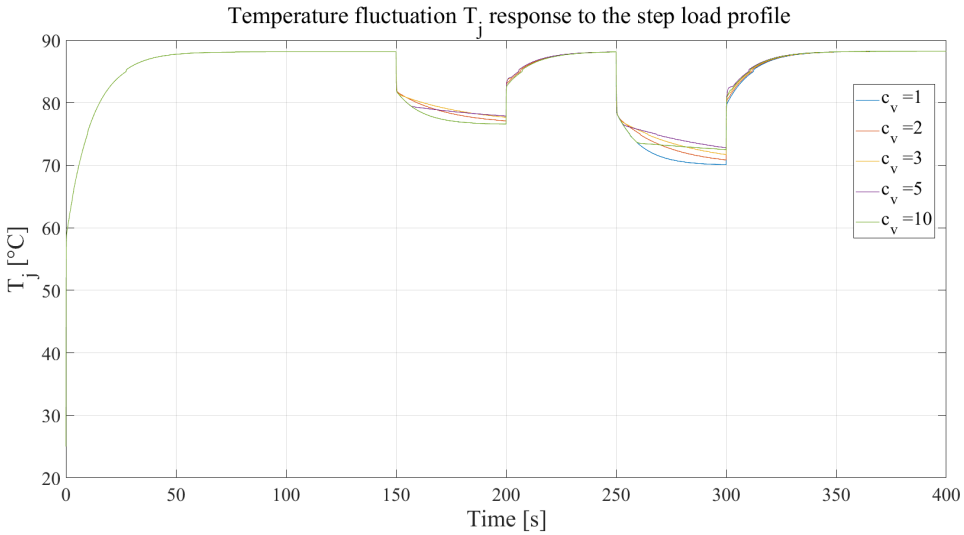


Figure 54: The step response of T_j using the gradient descent approach.

Table 7: ΔT_j in a step-response at increasing c_v for ideal reference parameters.

c_v	ΔT_j [°C]	% reduction
1	18.04	0.00
2	17.27	4.30
3	16.43	8.96
5	15.35	14.97
10	15.63	13.40

It is apparent that the rapid temperature dynamics of the SiC MOSFET package, compared to the heatsink dynamics, restricts the performance of this ATC. This can be illustrated by the decreasing effect at increments of c_v seen in Table 7 when reaching $c_v = 5$ and $c_v = 10$.

Solar profile

A similar observation can be seen for the T_j solar response as for the step response, where the controller may only influence the losses at the lower part of the cycle. For the solar-based load profile, it can be observed in Figure 55 that the mean temperature T_m is significantly higher for the trajectory of $c_v = 500$ compared to $c_v = 1$ being the non-influenced path. Specifically, for the larger drops in I_o, the ATC is able to reduce the ΔT_j. This could be advantageous because the larger ΔT_j has a significantly higher impact on the reliability than T_m, as mentioned in Chapter 2.5.

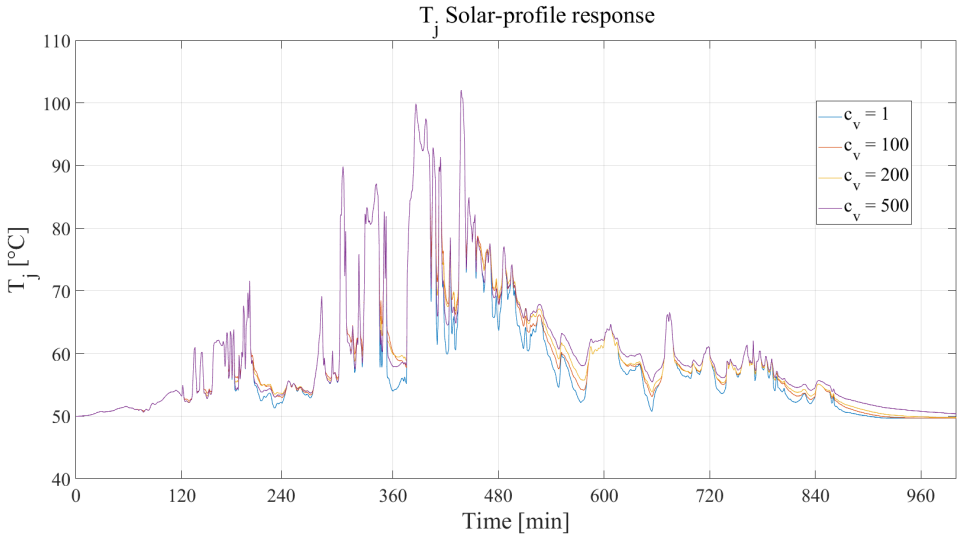


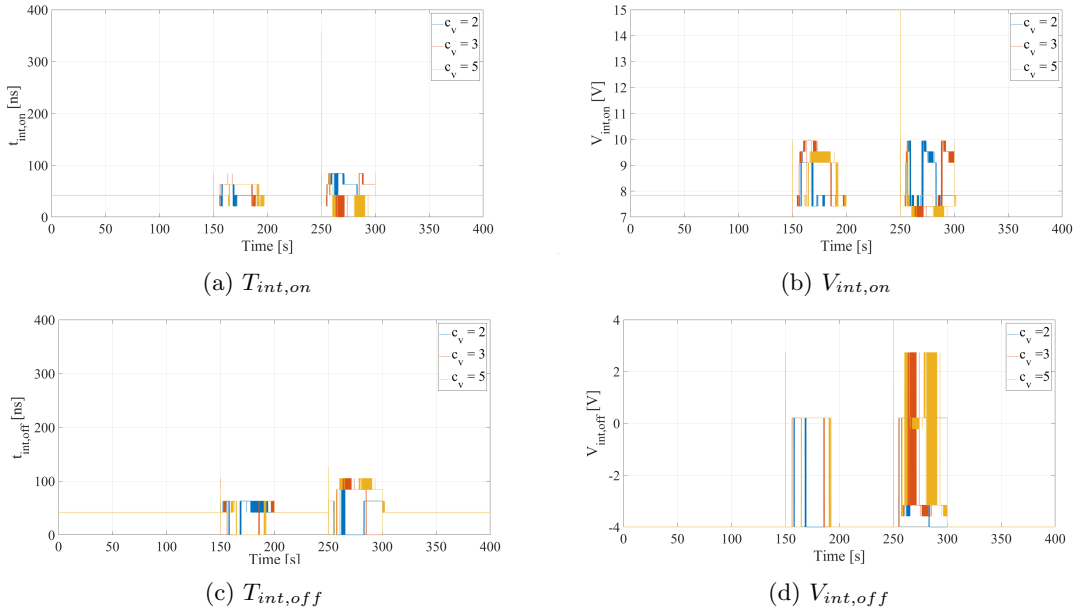
Figure 55: T_j trajectory based on a normalized load profile of the irradiance 2. mai 2023.

A significant increase in the scaling factor c_v is needed for reducing ΔT_j, indicating the restriction of the small-time constants of the inner SiC MOSFET material layers. This could be expected due to the need for an extensive increase in the time constants to filter out this T_j response. At little to no load changes, the T_j at different c_v trends towards the steady state, as seen at the start and end of the simulation. In the instance of larger c_v than 500, a continuously elevated temperature would be expected.

Parameters multi-variable gradient descent method

Figure 56 presents the control parameters for the gradient descent method. It can be observed, looking at Figure 40 in conjuncture with Figure 56, that the parameters corresponding to the lowest overshoots, in general, correspond to high switching losses. Specifically, $V_{int,on} = 8$V and

$t_{int,on} \in [250, 400]$ns provides the lowest reverse recovery current I_{rr}. For minimizing the voltage overshoot V_{os}, $V_{int,off} = 4$V and $t_{int,off} \in [250, 400]$ns are the optimal settings. However, looking at the results in Figure 56, the commanded switching energies from PI-controller for reference tracking are too low. Therefore, the optimization concerning the overshoots is hindered by this limitation. With the implementation of the first guess being weighed by a similar fraction for each iteration, a comparable result is expected for an approximately equal input. That could explain the slightly oscillatory response. A too low tolerance for exiting the loop could be a significant factor, supported by the oscillations in Figure 57. With the equal weights $w_1 = 0.5$ and $w_2 = 0.5$, the voltage overshoot V_{os} will be prioritized due to how it varies from $V_{os} \in [10.8, 32.7]$V compared to the interval $I_{rr} \in [2.4, 8.4]$A. This can be observed by the increased $V_{int,off}$ when sufficient E_{req} allows it. Keep in mind that the switching energies get normalized with respect to the load current.



(a) $T_{int,on}$ (b) $V_{int,on}$

(c) $T_{int,off}$ (d) $V_{int,off}$

Figure 56: Control parameters for the gradient method.

Figure 57 describes the switching energy the AGD provides with the gradient approach. The choice of parameters provides a definite number of increments for reference tracking with this optimization method. Implementation of an interpolation technique with tighter tolerance bands would increase the resolution. However, this type of approach has a trade-off to increased complexity and computation requirements.

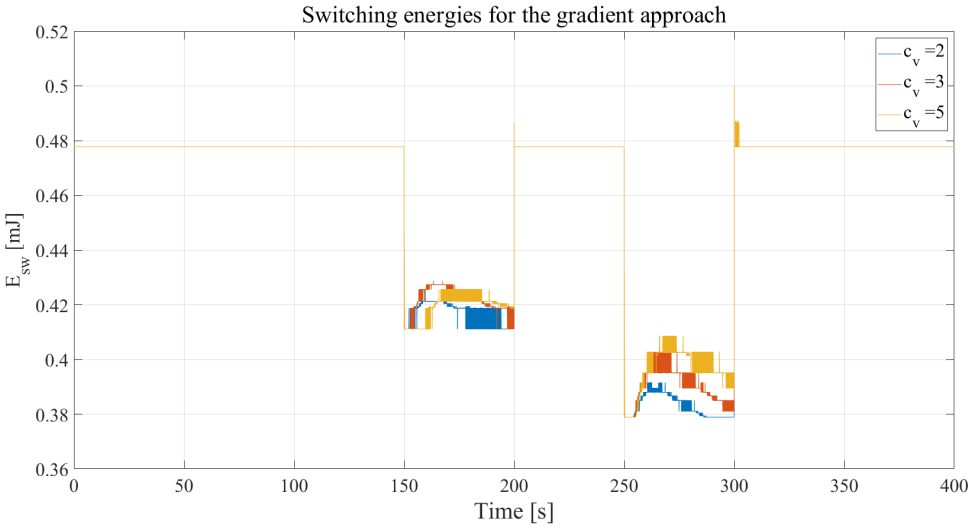
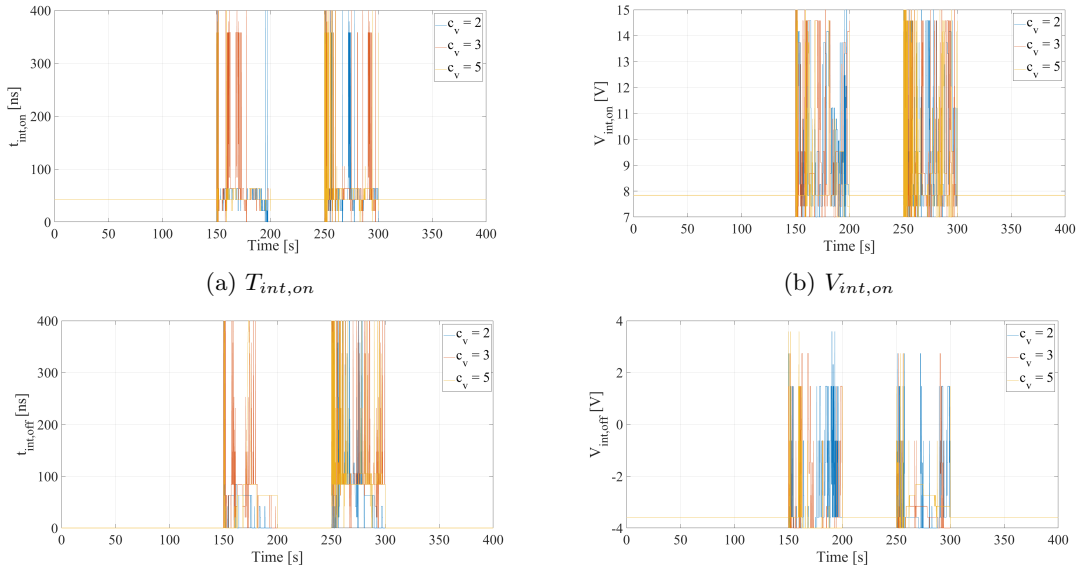


Figure 57: The required energy E_{req} for reference tracking for the gradient approach.

Variables multi-variable heuristic

Similarly to the gradient descent method, the heuristic approach produces an oscillatory selection of control parameters, as seen in Figure 58, however, with larger oscillations. It is apparent that $t_{int,off}$ tries to reach a value such that it is not at the upper plateau of V_{os}, referring to Figure 40. Due to the switching energy being too low, an oscillating combination of $t_{int,on}$ and $V_{int,on}$ is seen, and similarly for $t_{int,off}$ and $V_{int,off}$. In this instance, a conclusion is hard to be drawn from these results. The oscillating control parameters could be unfavorable in implementing a real experimental ATC. This is due to the response time of the LDOs to regulate the supply voltages in the ADC could be challenged if used in a high-frequency application.



(a) $T_{int,on}$ (b) $V_{int,on}$

(c) $T_{int,off}$ (d) $V_{int,off}$

Figure 58: Control parameters for the heuristic method.

It can be observed in Figure 59 in combination with Figure 54 that E_{sw} increases to compensate the losses for reference tracking at the intervals $[150, 200]$s and $[250, 300]$s. The switching energies for the heuristic approach are significantly smoother than the results obtained in the gradient descent

approach. This could indicate that the tolerance in the gradient descent algorithm was definitively too large or that the initial guess approach caused the algorithm to oscillate between two values satisfying the required switching energies, or a combination of the above. The smaller oscillations favor the gradient descent method compared to the heuristic approach for implementation in a real system. However, the heuristic approach is likely more optimal due to its computational time since the data is presorted with fewer computational steps, mainly requiring sufficient data storage. The heuristic method allows for more continuous E_{sw} increments.

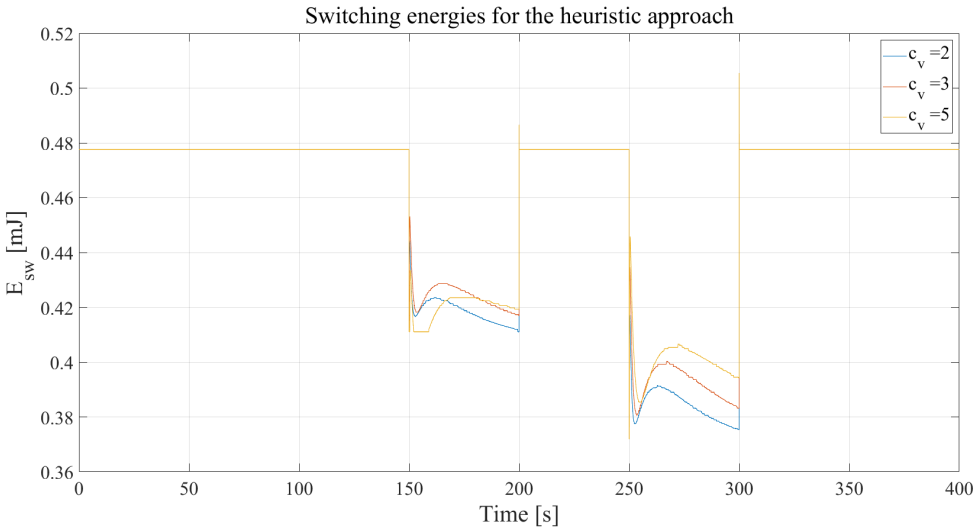


Figure 59: Switching energies for the heuristic approach.

5.3 Active temperature control simulation non-ideal operational reference

Non-optimal operational reference

In the case of non-optimal operational reference, the loss manipulation range gets shifted from the interval $E_{sw} \in [0, 4.51]$mJ to $E_{sw} \in [-0.45, 4.06]$mJ at a load current $I_o = 20$A. The ATC scheme could leverage this to either reduce the switching losses or increase the losses for reference tracking. It can be observed that the T_j reference generated in Figure 60 for the non-ideal reference operational parameter seen in Table 4 is significantly higher, compared to the previous T_j trend in Figure 52. A small bump is apparent at a time equal to 50s, due to a shift of the look-up table determining the conduction losses because of the temperature increase. Comparing this to Figure 52, the temperature increments at higher temperature levels cause a more notable conduction loss increase. This can be explained by Figure 50.

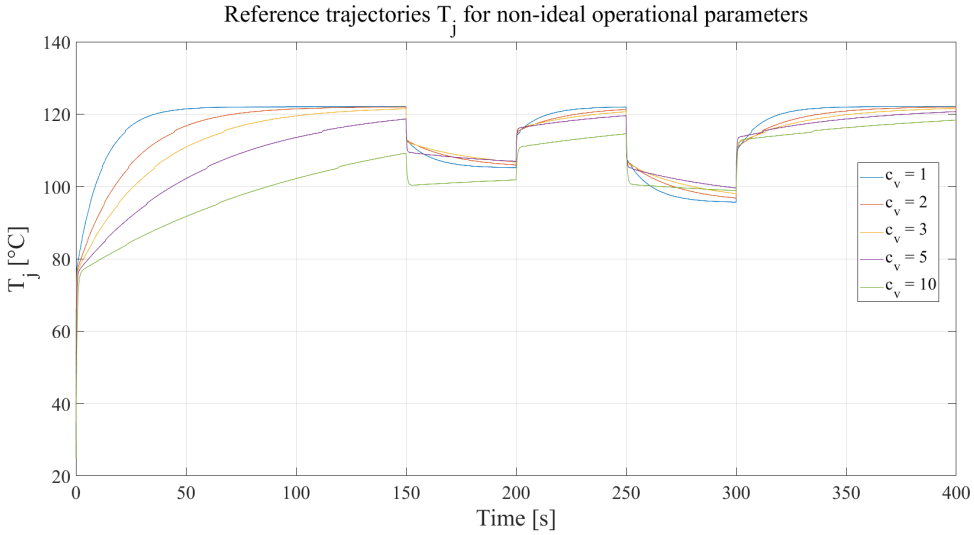


Figure 60: T_j trajectory reference for non-ideal reference parameters with the heuristic approach.

As indicated in the Figure 61. The controller now follows the reference in the upper and lower part of the cycles. Therefore, a larger reduction in absolute ΔT_j is achievable. In spite of an increased percentage reduction of ΔT_j is attainable as seen in Table 8. The absolute value of the ΔT_j at $c_v = 10$ is in a similar magnitude as the ideal case, despite the possibility of reducing and increasing the losses for reference tracking. For the case of a non-ideal operational reference, the elevated T_j counteracts the increased leverage of the controller for influence on both the upper and lower parts of the cycle. The positive temperature coefficient of $R_{ds,on}$ indicates that the increased proportion of P_{cond} restricts the range ΔT_j of reduction. Similarly, the unwanted effect of larger swings in temperature at higher power-losses and high temperature behaves contrarily to the objective of ΔT_j reduction and increased reliability. This is due to the elevated difference between T_a and the T_j increases the rate of change of T_j. Hence, the goal of slow dynamics with enhanced control range is counteracted by the more rapid dynamics at elevated temperatures from the greater $T_j - T_a$ difference. The data collected thus far does not make room for reaching a definitive conclusion. Larger c_v or more optimal load profiles may produce better results for the non-ideal reference operational parameters. As seen in Table 8, a trade-off between elevated temperatures and a reduction in temperature fluctuation potential is visible. This contrasts the aforementioned case with ideal reference parameters with more restricted possibilities for T_j reduction and lower T_m. Investigating this in conjunction with lifetime models, an optimal choice of reference parameters and c_v could be determined for the specific module or package design.

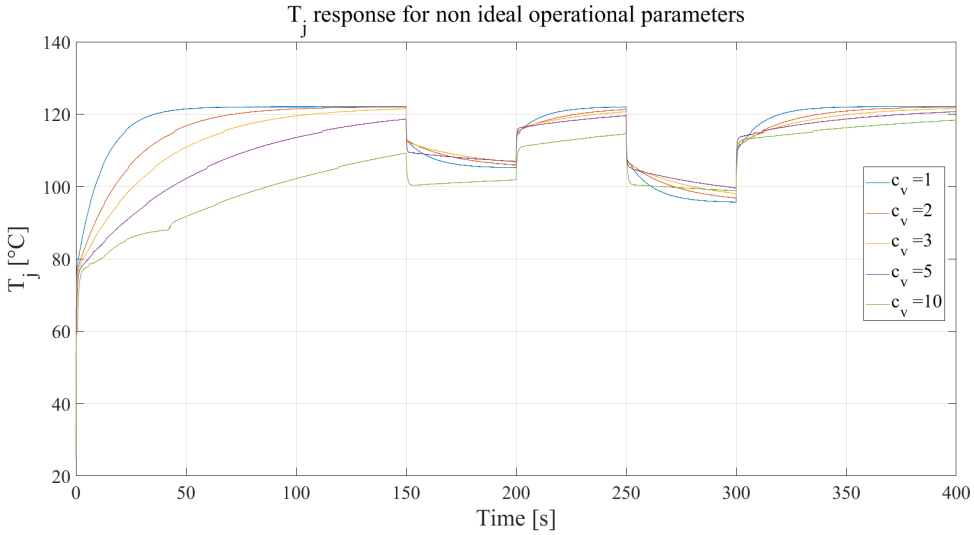


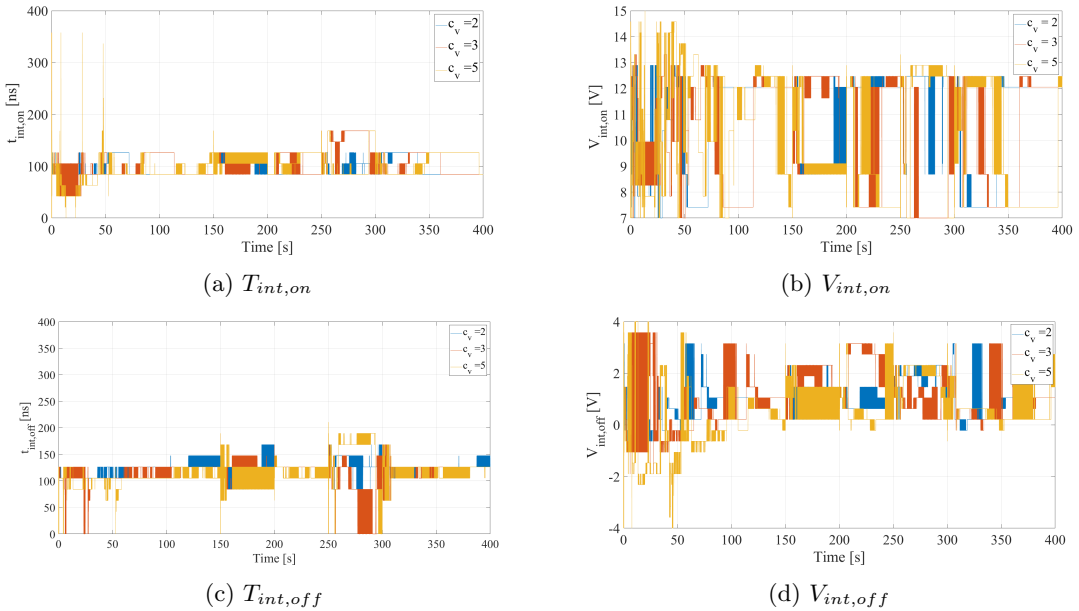
Figure 61: T_j trajectory for non-ideal reference operational parameters.

Table 8: ΔT_j in a step-response at increasing c_v for non-ideal reference parameters.

c_v	ΔT_j [°C]	% reduction
1	26.31	0.00
2	24.51	6.84
3	22.60	14.10
5	19.92	24.29
10	15.81	39.90

Parameters multi-variable gradient descent method

It can be observed for the gradient descent method in Figure 62 that the timing durations $t_{int,on}$ and $t_{int,off}$ are mainly restricted to the interval $[100, 150]ns$. Whereas the intermediate voltages $v_{int,on}$ and $v_{int,off}$ oscillate significantly more than the case with ideal reference parameters. As mentioned, with the weighting of $w_1 = 0.5$ and $w_2 = 0.5$, the V_{os} primarily determines the optimization function. It can be observed that $v_{int,off}$ specifically is elevated with the increased leverage of the loss modulation for the non-ideal reference parameters. As mentioned, the optimal $v_{int,off}$ is $4V$, which corresponds well with the results of elevated $v_{int,off}$.



(a) $T_{int,on}$ (b) $V_{int,on}$

(c) $T_{int,off}$ (d) $V_{int,off}$

Figure 62: Control parameters for the gradient method with non-ideal reference parameters.

It can be seen in Figure 63 that the controller has a more dynamic switching energy trend, providing lower switching energies at the start for the higher c_v to track the virtual heatsink reference, whereas it provides loss compensation during load drops. This could indicate that increasing c_v significantly could be a viable strategy. Similar to the ideal reference parameters case, the tolerance is likely too large with rapid oscillations between certain values.

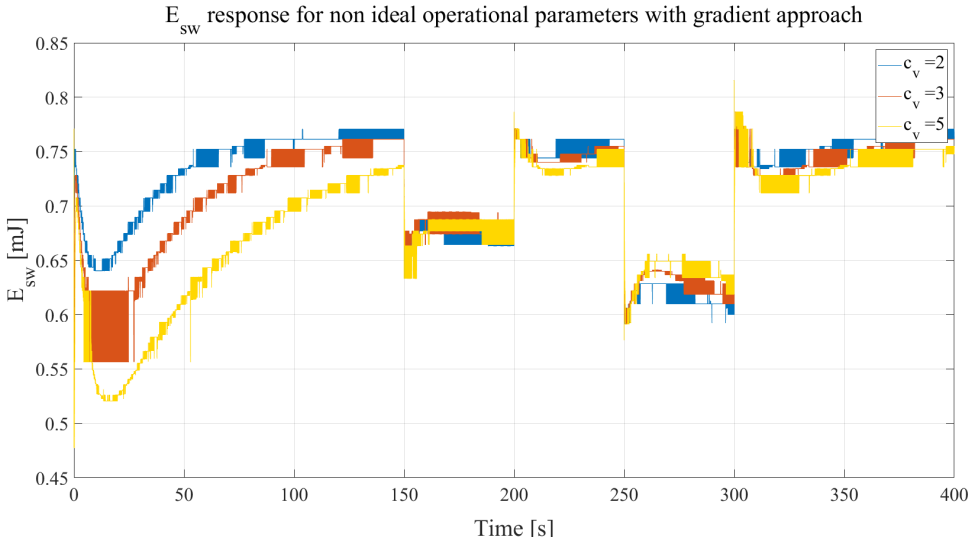
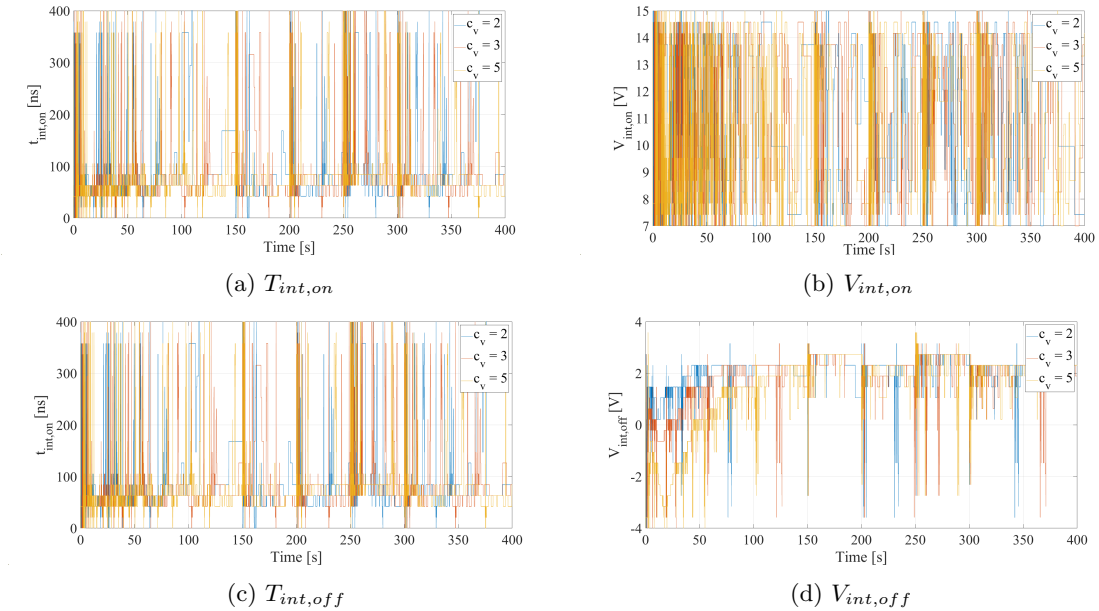


Figure 63: E_{sw} for the gradient method and non-ideal reference parameters.

Variables multi-variable heuristic

The heuristic approach provides a comparable, oscillatory response to the ideal reference parameters seen in Figure 64, however, now with significant oscillations for the entire duration. A pattern can be observed for $t_{int,on}$ and $t_{int,off}$. However, difficult to provide any meaningful analysis. $V_{int,on}$ rapidly oscillates for the entire duration. $V_{int,off}$ is continuously elevated, similar to the gradient approach. Hence, $V_{int,off}$ is probably the most significant parameter for this specific weighting of V_{os} and I_{rr}.



(a) $T_{int,on}$ (b) $V_{int,on}$

(c) $T_{int,off}$ (d) $V_{int,off}$

Figure 64: Control parameters for the heuristic method with non-ideal reference parameters.

The apparent cooling effort of the non-ideal reference parameters can be seen at Figure 65. A smoother E_{sw}, demonstrates the viability of the AGD as a more continuous loss compensation compared to the AGD in the ATC frameworks of van der Broeck [19] presented in Chapter 2.8. Experimental validation is still missing to confirm the precision and feasibility of the proposed ATC. The role of the temperature effect on the switching-loss manipulation is still uncertain. The realism of incorporating an optimization technique with regard to the overshoots in this fashion is still questionable due to the rapid oscillatory behavior between control parameters. Further refinements must be conducted in order for any of these two approaches to be suitable for experimental testing. However, the 160000 combinations of E_{sw} with the given dataset indicate the continuous switching loss compensation possibility of this AGD in a more refined ATC framework with an efficient loss modulator.

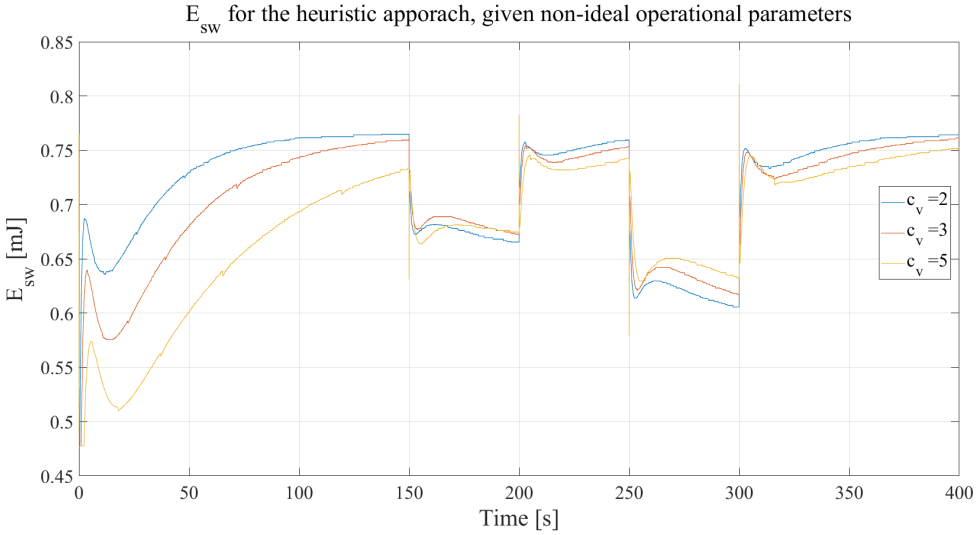


Figure 65: E_{sw} for the heuristic approach with non-ideal reference parameters.

6 Conclusion

In order to increase the reliability of SiC MOSFETs, an ATC framework has been considered. A successful investigation was carried out to obtain an accurate power-loss model for a SiC MOSFET C30075120D from Wolfspeed. This was done through an experimental approach for acquiring valuable characteristic temperature-dependent data using a device analyzer B1505A from Keysight. Temperature control of a heatsink acting as a heating plate was achieved by designing and building a controllable synchronous buck converter. Designing a current control based on disturbance rejection and an outer temperature control loop, the configuration was successful in controlling the temperature in the interval of $T \in [50 - 120]^{\circ}$C. The findings from the electro-thermal characterization of the SiC MOSFET were consistent with the theoretical foundation. Indicating a clear shift in V_{th} and a higher $R_{ds,on}$ at elevated temperatures. In essence, the effect on the saturation region at elevated temperatures and varying V_{gs} can be observed. Particularly the two regions of positive and negative temperature coefficient effect on the i_d current capabilities. The positive temperature coefficient of $R_{ds,on}$ in the ohmic region in the ID-VDS curves is apparent, indicating higher conduction losses at elevated temperatures for V_{gs} values corresponding to a fully developed conductive channel in the base region.

This thesis has provided an overview of an ATC framework based on switching loss manipulation utilizing an AGD. Both a step response and the response from a solar profile are examined. The ATC based on a virtual heatsink approach managed to have an effect on the dynamics of the junction temperature, especially for the slow dynamics caused by the heatsink. The controller was examined for two different operational references, one optimized for efficiency, only able to provide loss compensation at the lower part of the T_j cycles. The other reference parameter selection provided the opportunity to both lower and increase the losses for ΔT_j reduction, at the cost of elevated steady-state T_j. The results from two optimization techniques for lowering the overshoots were analyzed for the two cases.

In the light of the case, optimized with respect to efficiency. The ATC succeeded in providing loss compensation to reduce ΔT_j. Specifically, in instances with a large load drop. For the step profile examined, the ATC scheme yielded a ΔT_j reduction of 14.97 %, when exposed to a drop of 5A for a scaled virtual heatsink factor of $c_v = 5$. yet, the rapid T_j dynamics the SiC MOSFET package, compared to the slow dynamics of the heatsink, presents as a restriction of this ATC approach based on augmenting the thermal capacitances C_{th}.

For the case of a non-ideal operational reference, the elevated temperature counteracts the increased leverage of the controller for influence on both the upper and lower parts of the cycle. Compared to the case with optimal operational parameter reference, a larger ΔT_j 39.90 % was achieved. Nonetheless, the increased proportion of P_{cond} restricts the absolute value range of ΔT_j reduction due to the positive temperature coefficient of $R_{ds,on}$. Similarly, the unwanted effect of larger swings in temperature at higher power-losses and high temperature behaves contrarily to the objective of ΔT_j reduction. Indicating that references generated for the optimal parameters with respect to efficiency could be advantageous. Nevertheless, it is not possible to reach a concluding statement. This effect needs to be examined thoroughly through more experiments and simulations, where the temperature-dependency of the switching losses using the AGD is included. The optimal c_v still needs further examination for different load profiles, looking at the compromise of steady-state equivalent T_j tracking and reduction in ΔT_j, taking into account the limitations of the AGD.

7 Further work

In this thesis, several factors have been simplified, where some assumption has been made. This provides some avenues to further improved the accuracy of the ATC framework.

As aforementioned, the accuracy of the thermal model is pivotal for estimating the T_j. A natural step would be to do a FEM simulation with an experimental segment for verification, to precisely characterize the thermal behavior of the SiC MOSFET and the given heatsink configuration. Considering the temperature-dependent properties of the SiC MOSFET layers. A 3-D model, similar to van der Broeck et al. could be employed [55].

Conducting multiple experiments of the AGD with the SiC MOSFET at several load-current intervals could provide a dataset more suitable than the normalization function of the load-current employed in this thesis. The temperature dependency on the switching losses for this AGD could also be investigated.

As mentioned in the conclusion, a more thorough investigation is needed for examining the effect of c_v and reference operational parameters at various load profiles. The impact of f_{sw} and T_a on the ATC could prove to be an intriguing subject of investigation.

a logical progression would be to integrate the ATC scheme into an experimental setup. For this to be achievable, an observer T_j structure would need to be incorporated for T_j estimation. The spatial thermal observer structure of van der Broeck et al. could be a source of inspiration [77]. Conducting experiments used for validation of the ATC scheme would be valuable to verify the results and the accuracy of the different elements.

With a functioning ATC scheme employed, the effect of the ATC on the reliability of SiC MOSFETs incorporated in a realistic system could be examined, through conducting ALTs. Thus, the tangible impact of the ATC can be observed, with a more thorough assessment of its effectiveness.

In the end, these considerations could be used for examining the effect on SiC MOSFET modules, instead of the discrete C3M0075120D SiC MOSFET looked at in this thesis.

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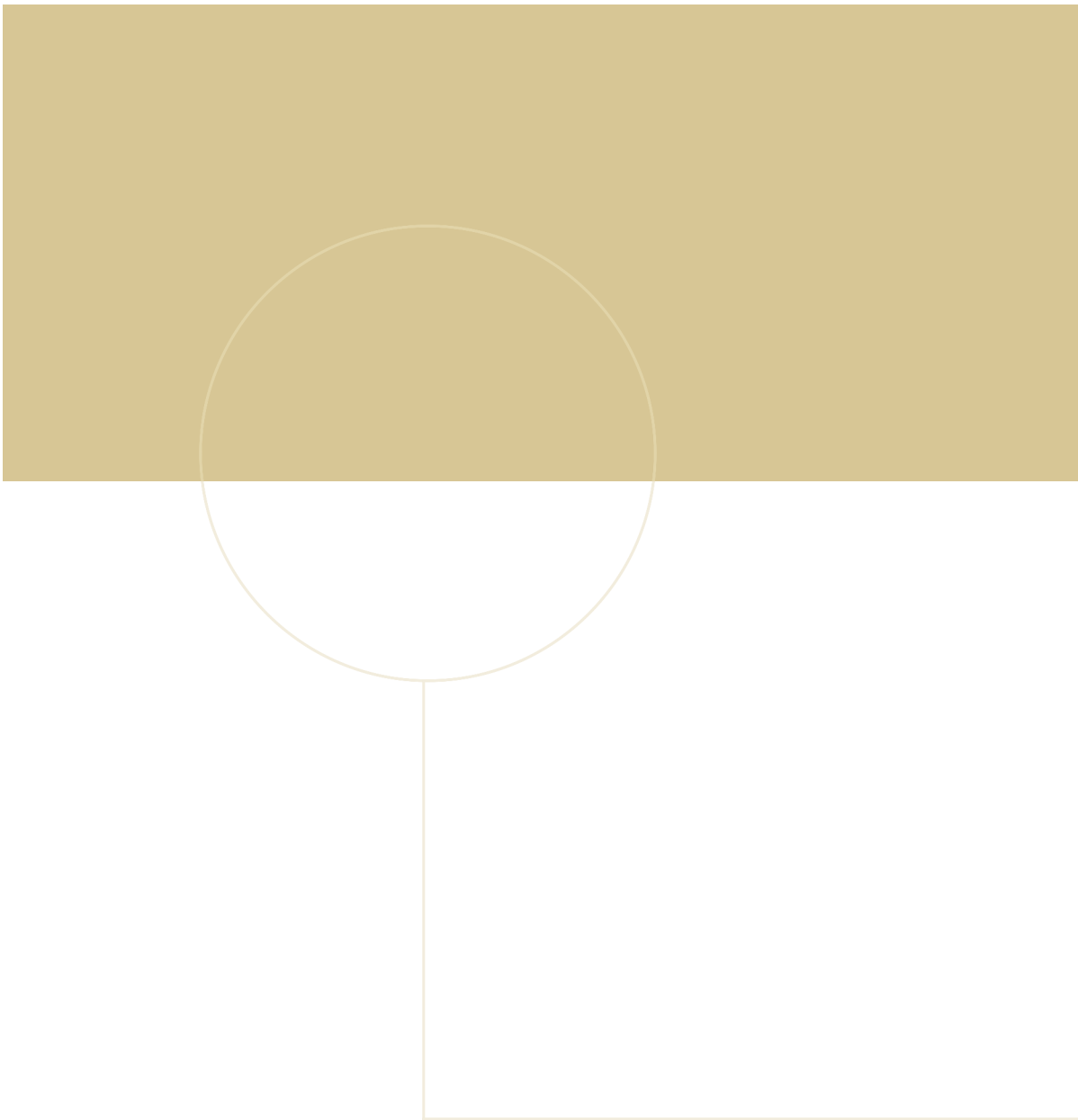

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