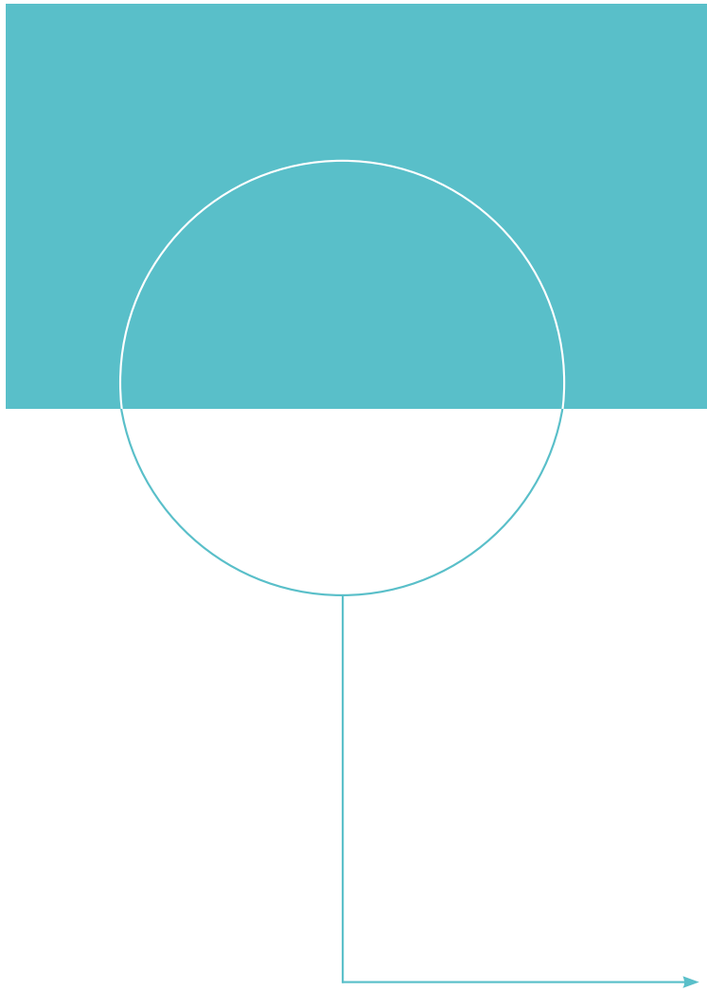


Master's thesis

2023

Jonathan Sæthre Ege, Sondre Hånes Egge

NTNU
Norwegian University of Science and Technology
Faculty of Information Technology and Electrical Engineering
Department of Electronic Systems

Jonathan Sæthre Ege
Sondre Hånes Egge

Design and implementation of a 0.01 mm² current-mode temperature sensor in 22 nm FD-SOI with a sensing range of -40 °C to 125 °C and 6.3 nW at 0.8 V

July 2023

NTNU
Norwegian University of Science and Technology

NTNU
Norwegian University of Science and Technology

NTNU

Norwegian University of
Science and Technology

Design and implementation of a 0.01 mm² current-mode temperature sensor in 22 nm FD-SOI with a sensing range of -40 °C to 125 °C and 6.3 nW at 0.8 V

Jonathan Sæthre Ege
Sondre Hånes Egge

Electronic Systems Design (Master's Programme)
Submission date: July 2023
Supervisor: Carsten Wulff

Norwegian University of Science and Technology
Department of Electronic Systems

Abstract

This work presents a temperature sensor implemented in the 22 nm Fully Depleted Silicon-On-Insulator (FD-SOI) technology by GlobalFoundries (GF). The work builds on the groundwork from our previous project work in [1], which is based on the 65 nm bulk Complementary Metal–Oxide–Semiconductor (CMOS) temperature sensor in [2]. This work aimed to make improvements and changes to the groundwork done in the project work [1]. The proposed temperature sensor of this work has been implemented in layout as the project work only implemented the design in schematic.

The proposed temperature sensor implementation consists of an analog and a digital system. The analog system comprises the three same primary circuits as in [1] and [2]: A bias and reference circuit, a slew-rate controlled relaxation oscillator, and a comparator. The digital system has been implemented in this work and comprises of four primary digital blocks: An Analog-to-Digital Converter (ADC), a pulse counter, a clock divider, and a Finite-State Machine (FSM).

The proposed temperature sensor implementation fulfills the specifications for both after a one- and two-point calibration. The temperature sensor operates according to specification within the full temperature range of the transistor models, achieving a range of -40 °C to 125 °C. Additionally, it can operate with supply voltages spanning ±10% from 0.8 V. The proposed sensor occupies an area of 9.8 kμm^2 and achieves an average off-power of 3.6 nW. The sensor achieves a resolution of about 0.5 °C with a 9.6 μs conversion time and a sampling clock of 128 MHz. Due to the flexibility of the system, higher resolutions can be achieved by using a higher sampling clock or a longer conversion time. A Resolution Figure of Merit (R-FoM) of 3.3 $pJ \cdot K^2$ was achieved with a 128 MHz clock and a resolution of 0.048 °C. One conversion with this resolution used 1448 pJ and could be accomplished within a 55.4 μs conversion time.

The temperature sensor implementation achieves inaccuracies within ±2% after both a one- and two-point calibration. This is achieved with a conversion time of 9.6 μs and a sampling clock of 128 MHz. The relative inaccuracy of the sensor is 1.87 % for two-point and 2.18 % for one-point calibration. The inaccuracy has a peak-to-peak error of -2 ∼1.1 °C for two-point and -2.4 ∼2.2 °C for one-point calibration. The sensor exhibits a 3σ of 1.71 °C due to mismatch in the range -40 °C to 125 °C. While noise-induced error to the system has a standard deviation of 2.06 °C at 27 °C and 2.41 °C at 125 °C.

Sammendrag

Dette arbeidet presenterer en temperatursensor implementert i en 22 nm Fullstendig Depletert Silikon på Isolator (FD-SOI) teknologi av GlobalFoundries. Arbeidet bygger på grunnarbeidet fra vårt tidligere prosjektarbeid i [1], som er basert på 65 nm Komplementær Metalloksidhalvleder (CMOS) temperatur sensoren i [2]. Dette arbeidet hadde som mål å gjøre forbedringer og endringer på grunnlaget som ble lagt i prosjektarbeidet [1]. Den foreslåtte temperatursensoren i dette arbeidet har blitt implementert i utlegg, da prosjektarbeidet kun implementerte designet i skjematikk.

Den foreslåtte implementeringen av temperatursensoren består av et analogt og et digitalt system. Det analoge systemet består av de samme tre primære kretsene som i [1] og [2]: En bias- og referansekrets, en slew-rate kontrollert relaksjons oscillator, og en komparator. Det digitale systemet er implementert i dette arbeidet og består av fire primære digitale blokker: En analog-til-digital omformer (ADC), en pulsteller, en frekvensdeler, og en tilstandsmaskin (FSM).

Det foreslåtte temperatursensorimplementeringen oppfyller spesifikasjonene både etter en- og to-punkts kalibrering. Temperatursensoren opererer i samsvar med spesifikasjonene innenfor hele temperaturområdet til transistor-modellene, og oppnår et område på -40 °C til 125 °C. I tillegg kan den operere med forsyningspenningsnivåer som spenner ± 10% fra 0,8 V. Den foreslåtte sensoren tar opp et areal på 9,8 kμm^2 og oppnår en gjennomsnittlig av-effekt på 3,6 nW. Sensoren oppnår en oppløsning på omtrent 0,5 °C med en konverteringstid på 9,6 μs og en samplingsfrekvens på 128 MHz. På grunn av systemets fleksibilitet kan høyere oppløsninger oppnås ved å bruke en høyere samplingsfrekvens eller lengre konverteringstid.

Implementeringen av temperatursensoren oppnår unøyaktigheter innenfor ±2% etter både en- og to-punkts kalibrering. Dette oppnås med en konverteringstid på 9,6 μs og en samplingsfrekvens på 128 MHz. Den relative unøyaktigheten til sensoren er 1,87% for to-punkts kalibrering og 2,18% for en-punkts kalibrering. Unøyaktigheten har en topp-til-topp på -2 ∼1,1 °C for to-punkts kalibrering og -2,4 ∼2,2 °C for en-punkts kalibrering. Sensoren viser en 3σ på 1,71 °C på grunn av mismatch i området -40 °C til 125 °C. Mens støyindusert feil i systemet har en standardavvik på 2,06 °C ved 27 °C og 2,41 °C ved 125 °C.

Contents

Figures

Tables

Code Listings

Acronyms

ADC Analog-to-Digital Converter. iii, v, 7, 15–18, 23–25

BJT Bipolar Junction Transistor. 33

BOX Buried Oxide. 65

CMOS Complementary Metal–Oxide–Semiconductor. iii, v, 2, 33, 35, 41

DBGR Differential Bandgap Reference. 2, 7, 8, 22, 27, 33, 35, 42

DRC Design Rule Check. 18, 39

FD-SOI Fully Depleted Silicon-On-Insulator. iii, v, 2, 3, 15, 29, 33, 41–43, 65, 66

ff fast-fast. xvii, 21, 22

FoM Figure of Merit. 29, 35

fs fast-slow. xvii, 21

FSM Finite-State Machine. iii, v, ix, 5–7, 15–18, 23, 24

GF GlobalFoundries. iii, 2, 15, 29, 41

IC Integrated Circuit. 1

IoT Internet of Things. 1

LVS Layout Versus Schematic. 18

MCMis Monte Carlo Mismatch. 28

MUX Multiplexer. 3, 13, 14, 17, 37, 38, 42

NMOS N-channel Metal-Oxide Semiconductor. xvii, 14, 37

NOC Non-Overlapping Clock. 8, 11, 22

OTA Operational Transconductance Amplifier. 10, 13

PMOS P-channel Metal-Oxide Semiconductor. xvii, 8, 9, 13, 35, 37

PTAT Proportional to Absolute Temperature. xvii, 2

R-FoM Resolution Figure of Merit. iii, 26, 34, 35, 41

SC Switched Capacitor. 6, 7, 11–13, 15

sf slow-fast. xi, xvii, 3, 13, 21, 29

SLVT Super Low V_T. 8, 15, 25, 38

ss slow-slow. xvii, 21, 22

Th temperature-high. xvii, 21

Tl temperature-low. xvii, 21

TR Transmission. 3, 10, 11, 13, 37, 38, 42

Tt temperature-typical. xvii, 21, 25

tt typical-typical. ix, xvii, 3, 9, 21, 23, 25, 27–29

UG Unity Gain. 10, 12, 13, 17, 19, 22, 38, 39

UHVT Ultra High V_T. 3, 8, 38

Vh voltage-high. xvii, 21

Vl voltage-low. xvii, 21

Vt voltage-typical. xvii, 21, 23, 25, 28, 29, 33

Glossary

corner A corner is a test case and can be a combination of several test cases, or corners. For instance, corners that describe the transistors such as fast-fast (ff), sf, typical-typical (tt), fast-slow (fs), and slow-slow (ss). These corners describe the NMOS and PMOS transistors as follows: NMOS-PMOS. Similarly, a corner can also be a case with a different supply voltage, such as voltage-low (Vl), voltage-typical (Vt), and voltage-high (Vh). Specific temperatures can be considered to be corners as well. Such as temperature-low (Tl), temperature-typical (Tt), and temperature-high (Th). ix, xi, 3, 9, 13, 21, 23, 25, 27–29, 36

PTAT Proportional to Absolute Temperature (PTAT). Something is PTAT when it varies in a way that is proportional to absolute temperature. 2, 5, 7–9, 11, 12, 18, 22, 61, 63

Chapter 1

Introduction

Temperature (in Kelvin) is a measure of the average kinetic energy of atoms in a system. As a result, it's not surprising that most integrated circuits, sensors, systems, and humans are affected by temperature. A temperature sensor can correct other systems due to changes in temperature. As an example, a temperature sensor was used in [3] to reduce the influence of temperature on the sensor output in the resonant pressure sensor described in [3].

Battery-driven devices like wearables, handhelds, and Internet of Things (IoT) devices all incorporate a range of sensors. The various sensors should have a low power consumption while achieving an acceptable accuracy [4]. By prioritizing energy efficiency, these sensors enable devices to operate for extended periods or even function independently through energy harvesting.

There are several benefits to reducing the area that circuits occupy. This would allow for smaller and more lightweight devices without necessarily having to sacrifice any features like battery capacity. Extra features could also be added in the space that has been cleared up. In [5], a highly compact and low-power temperature sensor is presented. Applications for such a small and low power temperature sensor would include having several copies of the same sensor on one Integrated Circuit (IC) for hot-spot measurement. Such a low-power temperature sensor would be ideal for the work in [6], where several battery-driven nodes are placed across a room for ambient temperature measurements. In [7], an ultra-low power temperature sensor for system reliability and performance applications is presented. Low power sensors like the one presented in [7] would be suitable for both global and hot-spot temperature sensing on-chip.

In addition to having a small, accurate, and energy efficient temperature sensor which could be used for the same applications as in [3–7]. A sensor which has a wide temperature range, variable sampling rate, variable resolution, and multiple acceptable clock frequencies makes the sensor flexible. This opens up the possibility to use one sensor for multiple applications.

1.1 Scope

This work aims to implement a fully functional temperature sensor system in the 22 nm FD-SOI technology by GlobalFoundries (GF). The sensing range of the temperature sensor system should be within the temperature range -40 °C to 125 °C. It should have an accuracy of at least ± 1 - 2 % and be able to achieve a resolution of 0.5 °C or lower. The accuracy specification should be achieved after a 1-point and 2-point calibration. The temperature sensor system should achieve the specified accuracy and approximate resolution with a conversion time of 10 μs or less. The temperature sensor system should be small in size and have a low power consumption. The sensor should have a simple interface with a digital output.

The current-mode temperature-to-frequency converter proposed in our previous project work [1] is a central part of this work. The proposed implementation in the project work will be extended upon and improved in this work. The basis for the changes to be made is the discussion and future work chapters from the project work. This includes redesigning the comparator from the project work, reducing the analog circuitry's power consumption in the powered-down state, and reducing leakage in the digital blocks. Digital logic should be implemented to control the analog circuitry and to simplify the interface with the temperature sensor implementation. The digital logic should also convert the output of the analog circuitry to a digital value. Finally, a layout should be made for the full temperature sensor implementation.

1.2 Key references

In our previous project work [1], a temperature sensor outputting a square wave with a Proportional to Absolute Temperature (PTAT) frequency was implemented. The 22 nm Fully Depleted Silicon-On-Insulator (FD-SOI) technology by GF was used to implement the temperature sensor in the project work. The aim of the project work was to implement a working schematic design based on the temperature sensor in [2]. The temperature sensor in [2] was implemented in a 65 nm Complementary Metal–Oxide–Semiconductor (CMOS) technology. As the project work aimed to implement a working schematic design, no layout was made.

The sensor implementation from the project work only consists of an analog part. For this reason, it does not output a digital value representing the converted temperature. The analog circuitry incorporates three primary circuits: two PTAT current generators and a comparator. The PTAT currents are used to generate a Differential Bandgap Reference (DBGR). The PTAT currents are also used to create a slew-rate controlled triangular relaxation oscillator. The DBGR voltages are used as clamping voltages for the triangular relaxation oscillator. The PTAT currents make the frequency of the triangular relaxation oscillator PTAT. A square wave that is PTAT is output from the comparator due to the triangular oscillations and the DBGR.

The sensor's operation requires three specific control signals, each with individual timing requirements. The output frequency conversion falls on the user, increasing usage complexity. Moreover, the early output pulses, within 5 μs of start-up, are not eligible for conversion due to the sensor being partially started up. During the inactive state in the typical-typical (tt) corner with a supply of 0.8 V, the sensor has a high current consumption of approximately 20 nA.

After a two-point calibration, the sensor implementation exhibits an inaccuracy of 1.45 °C in the temperature range 0 °C to 80 °C. In the temperature range -40 °C to 125 °C the sensor achieves an inaccuracy of 13.5 °C. Excluding the slow-fast (sf) corner a 3.5 °C inaccuracy is achieved. The sensor achieves a 3σ inaccuracy of ±1 °C due to mismatch in the range -40 °C to 125 °C. The high inaccuracy in the slow-fast (sf) corner was due to the comparator not being designed properly.

1.3 Key contributions

The key contributions of this work are the following:

- The comparator design has been improved. Because of this, the temperature sensor implementation now performs within specifications across all corners. This includes the slow-fast (sf) corner in which it performed poorly in the project work [1].
- Reduced power consumption of the analog circuit in the powered-down state by utilizing Transmission (TR) gates and Ultra High V_T (UHVT) pull-up and pull-down transistors. Additionally, a number of transistors have been resized to achieve lower leakage.
- Improved overall system linearity.
- A single equation can now be used to describe the temperature sensor implementation. This allows for one-point calibrations to be performed.
- Utilized the construction of FD-SOI transistors described in Appendix D to implement back-gate switching in TR gates and Multiplexers (MUX).
- Implemented digital control logic to control the analog circuit and simplify interaction with the sensor. The digital logic also outputs the measurements as a digital value as opposed to a frequency. Flexibility is gained through the possibility of choosing the conversion time and sampling clock. This also gives flexibility concerning power consumption, as a shorter conversion time and lower sampling clock can be used to consume less power.
- Layout for the complete sensor implementation has been designed and verified with post-layout simulations.

1.4 Outline

This report is organized as follows: Chapter 2 presents the overall implementation starting with an introduction before describing the analog circuitry and improvements and changes made to it, and finally, chapter 2 will describe the digital logic.

Chapter 3 gives some insight into the simulations that have been performed before presenting the results of the overall temperature sensor implementation. In Chapter 4 the temperature sensor implementation is discussed, while future work is considered in Chapter 5. Lastly, the conclusion is given in Chapter 6.

Chapter 2

Implementation

This chapter will start by giving an overview and description of the behavior of the temperature sensor implementation in section 2.1. The analog system and the improvements and changes made to it will be described in detail in section 2.2. The digital system that was implemented in this work will be described in detail in section 2.3. Lastly, the complete layout of the temperature sensor implementation will be presented in section 2.4.

2.1 Overview

The implementation is comprised of a digital and an analog system. The digital system, which is designed in this work, is used to start up and control the analog system using a Finite-State Machine (FSM). The digital system is also used to quantize and output the measurements. The analog system is comprised of the same three main subcircuits as in the project work [1]: a reference and bias circuit, a slew-rate controlled triangular relaxation oscillator, and a comparator.

Figure 2.1 is an illustration of the analog system and its behavior. The bias and reference circuit generates the two reference voltages V_A and V_B shown in Figure 2.1. The slew-rate controlled triangular relaxation oscillator has been simplified in Figure 2.1, and is drawn as the two current sources and the capacitor. The inverted output of the comparator $V_{\overline{CTRL}}$ is a control signal that decides which reference voltage is connected to V_{REF} and whether the capacitor C_{OSC} should be charged or discharged. The resulting behavior of the analog system is that $V_{\overline{CTRL}}$ becomes a square wave as illustrated in Figure 2.1. The frequency of $V_{\overline{CTRL}}$ is PTAT as it is proportional to the PTAT currents and is given by Equation (2.1).

$$f_{out} = \frac{\mathrm{I}}{2 \cdot (V_A - V_B) \cdot C_{OSC}} \tag{2.1}$$

Figure 2.2 is a simplified schematic of the analog system showing all three primary circuits. The bias and reference circuit, the triangular relaxation oscillator, and the comparator can be seen to the left, in the middle, and to the right

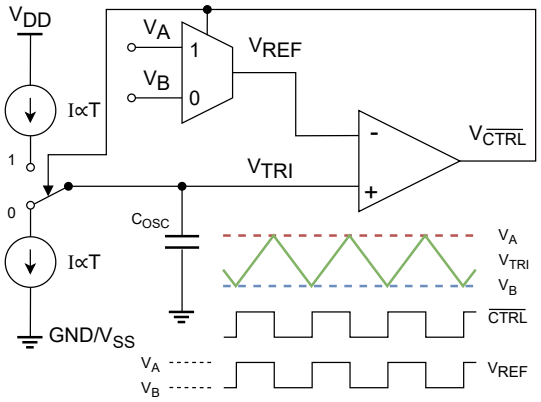


Figure 2.1: A simplified schematic with plots illustrating the analog system's behavior. This is a slightly modified version of [1, p. 9, Figure 3.1].

in Figure 2.2, respectively. The bias and reference circuit and the triangular relaxation oscillator both utilize a beta-multiplier which was thoroughly described in the project work [1], and can be read about further in Appendix C. The difference between the two beta-multipliers is that the one used in the triangular relaxation oscillator utilizes a Switched Capacitor (SC) circuit instead of a resistor. Each of the three primary circuits will be further described in section 2.2.

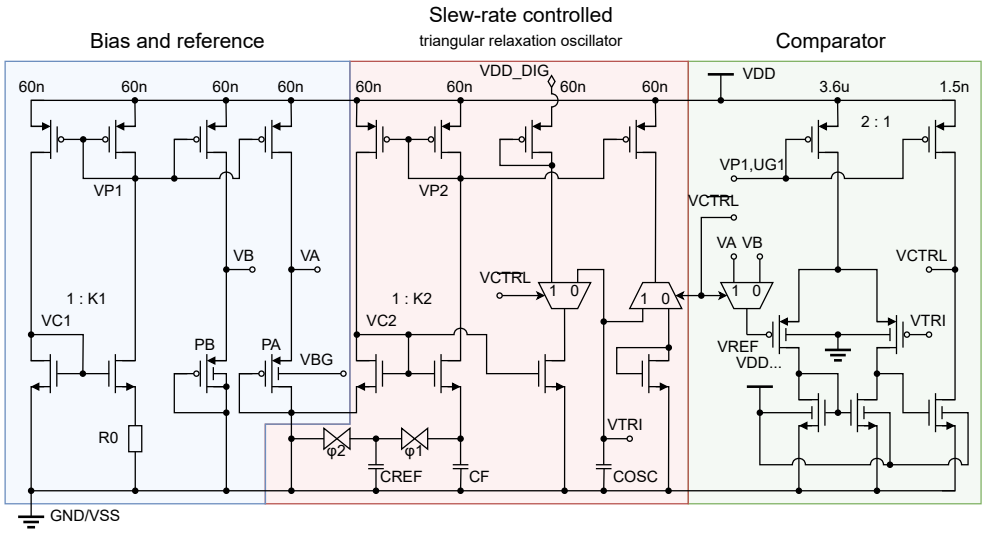


Figure 2.2: An illustration of the analog system showing how the three main subcircuits of the analog system are interfaced and built up. This is a slightly modified version of [1, p. 10, Figure 3.2].

Figure 2.3 illustrates how the digital and analog systems are interfaced. The temperature sensor can be enabled or disabled using the signal *ENABLE*. The digital system controls the analog system using a FSM, timed by a downclocked

version of the input on *CLK*. The analog system is started by the FSM when a sample is initiated using the external signal *SAMPLE*. This results in the output signal, *idle*, being driven to a low state, indicating that the temperature sensor is performing a measurement. The FSM in the digital system starts the analog system using the control signals *power_up*, *comp_control*, *set_tri*, and *startup_sc*. When the analog system has been started, it outputs a square wave with a PTAT frequency on the output $\overline{CTRL}$. The digital system counts the negative edges on this square wave until it has reached its target value given by the input signal, *target*. While the negative edges are being counted, another counter timed by *SAMPLE CLOCK* is running. The counter timed by *SAMPLE CLOCK* stops counting when the target number of negative edges has been reached. Its final value is an approximate measure of the time it took to count the target number of negative edges. The time it took to count the target number of negative edges is a number of periods on $\overline{CTRL}$ given by *target*. Thus, the final value of the counter timed by *SAMPLE CLOCK* is inversely PTAT and is output on *OUT*. The output signal, *idle*, is driven to a high state when the target number of negative edges has been reached, indicating that the value on *OUT* is ready to be read. The target number of negative edges is ignored if the signal *CONT* is high before the first pulse on $\overline{CTRL}$, and no digital output is produced by the Analog-to-Digital Converter (ADC). This allows the sensor to output a square wave continuously on $\overline{CTRL}$ until powered down or when *CONT* is pulled low. The measurement will proceed as usual if *CONT* is pulled low, counting the target number of negative edges. In this work, this is used to investigate the possibility of calibrating the DBGR by varying V_A with respect to the frequency of $\overline{CTRL}$. While performing a measurement, the clock on the input pin, *CLK*, on the analog circuit is used with the Switched Capacitor (SC) circuit in the triangular relaxation oscillator.

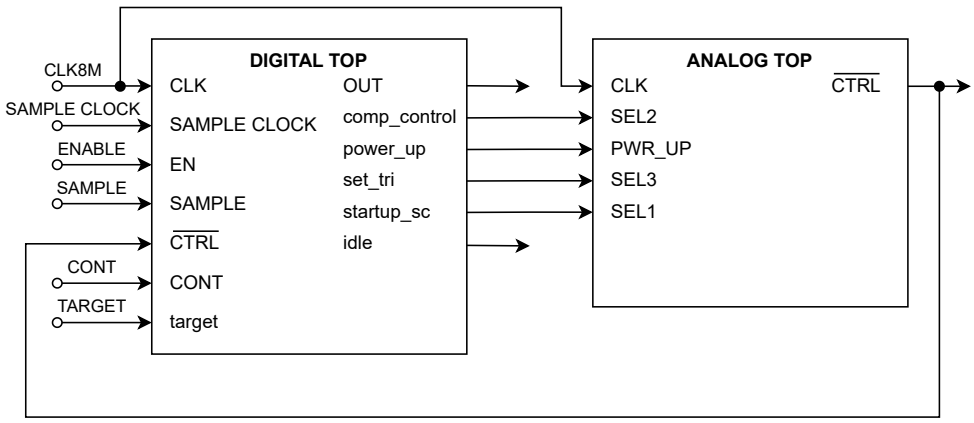


Figure 2.3: A block diagram illustrating how the digital and analog system of the sensor implementation are interfaced.

2.2 Analog

This work has made changes and improvements to the analog system initially designed in the project work [1]. This chapter will first describe some improvements made concerning power-saving measures in section 2.2. For the remainder of this chapter, each of the main circuits in the analog system and their associated circuits will be described. The improvements made to each of them will also be described, starting with the bias and reference circuit described in subsection 2.2.2. The purpose and design of the current mirror amplifiers associated with all the main circuits will be described in subsection 2.2.3. The Non-Overlapping Clock (NOC) generator used together with the triangular relaxation oscillator will be described in subsection 2.2.4. The triangular relaxation oscillator will be described in subsection 2.2.5. Finally, the comparator will be described in subsection 2.2.6.

2.2.1 Power-saving

In this work, power-saving measures have been made due to high power consumption in both the on and off state of the analog system from the project work [1]. The main contribution to the high power consumption was the high leakage in the digital components within the analog system. Power gating has been implemented using a PMOS transistor to remedy the leakage in the digital components. When the analog system is turned off, the PMOS is used to cut off the V_{DD} supply from the net V_{DD_DIG}, which is supplied to specific circuits inside the analog system. The relevant circuits are mainly logic blocks like inverters and AND gates. Another power-saving measure incorporated in this work is redesigned inverters, NAND gates, and AND gates that achieve lower leakage. There was considerably high gate leakage in the pull-up and pull-down transistors used in the power-up circuits and start-up circuits. To remedy this, the pull-up and pull-down transistors have been changed from Super Low V_T (SLVT) transistors to UHVT transistors with shorter lengths. This allows the reduction of gate leakage without increasing drain-source leakage.

2.2.2 Bias and Reference

The bias and reference circuit utilizes a beta-multiplier which is further described in Appendix C. The beta-multiplier is made up of N_1 and N_0 operating in subthreshold, P_1 and P_0 operating in saturation, and R_0 as shown in Figure 2.4. The beta-multiplier is used to generate a PTAT current given by Equation (2.2) found in Appendix C, where K_1 is the ratio between the widths of N_1 and N_0.

$$I_{REF} = \frac{V_T \cdot ln(K_1)}{R_0}, \qquad K_1 = \frac{(W/L)_{N_1}}{(W/L)_{N_0}} \tag{2.2}$$

The PTAT current is copied using P_2, P_3, and P_4 to generate two reference voltages V_A and V_B that are used as a DBGR. The reference voltages are different

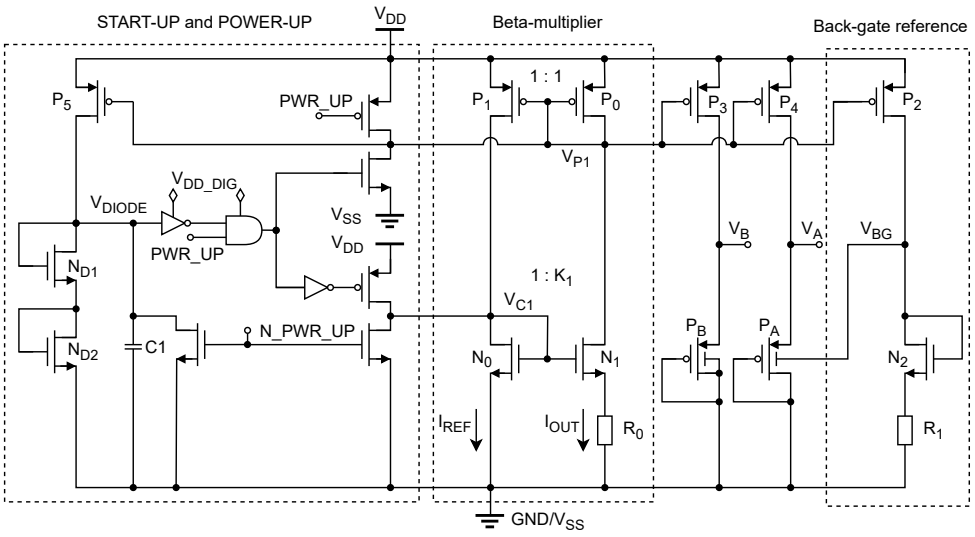


Figure 2.4: Schematic of the bias and reference circuit. This is a slightly modified version of [1, p. 11, Figure 3.3].

in amplitude due to the back-gate of P_A and P_B being connected to different potentials, namely the bandgap reference ,V_{BG}, and ground ,V_{SS}. The PTAT current is also copied using P_5 to form a start-up circuit.

The remainder of this section will describe the improvements and changes that have been made to the bias and reference circuit in this work. The ratio between N_0 and N_1 has been increased to $K_1 = 7/3$. This improved the linearity across corner simulations with a slight increase in power consumption. With R_0 being 400 kΩ, the current given by Equation (2.2) is slightly less than 60 nA at 27 °C in the typical (tt) corner.

The size of N_2 has been reduced for its geometry to be the same as that of N_0. This aimed to achieve better matching of N_0 and N_2. Consequently, the size of the resistor R_1 had to be increased while using the same geometry as R_0. This resulted in an overall improvement considering the mismatch.

The diode-connected transistors P_A and P_B were optimized to work better in harmony with the comparator. The amplitude of V_A and V_B were both lowered by reducing the length of P_A and P_B. This was done to make sure the PMOS differential pair in the comparator was well within the right operating region and to make the comparator faster.

The inverter at the node V_{DIODE} was changed to a regular inverter as opposed to a skewed inverter that was used in the previous project work. This is because the skewed inverter had high leakage after the reference and bias circuit had been started up. Further, the length of the diode-connected transistors N_{D1} and N_{D2} was increased to raise the final voltage of V_{DIODE}, turning the inverter more on, which reduces leakage. The purpose of the skewed inverter was to extend the time that the start-up circuit remained turned on, effectively starting up the bias and

reference circuit faster. The capacitor C_1 was added to achieve the same effect of keeping the start-up circuit on for longer as when the skewed inverter was used.

2.2.3 Current Mirror OTAs

Three current mirror Operational Transconductance Amplifiers (OTA) are used as Unity Gain (UG) amplifiers in the proposed implementation, with Figure 2.5 being a general schematic describing all of them. The Unity Gain (UG) amplifiers have small differences; for instance, UG1 has a pull-up transistor on the output, VOP, while UG2 and UG3 have a TR gate at the input, V_B. Additionally, the ratio K_3 is different for UG2 compared to UG1 and UG3, because of their loads. The primary purpose of the UG amplifiers is to start up the triangular relaxation oscillator.

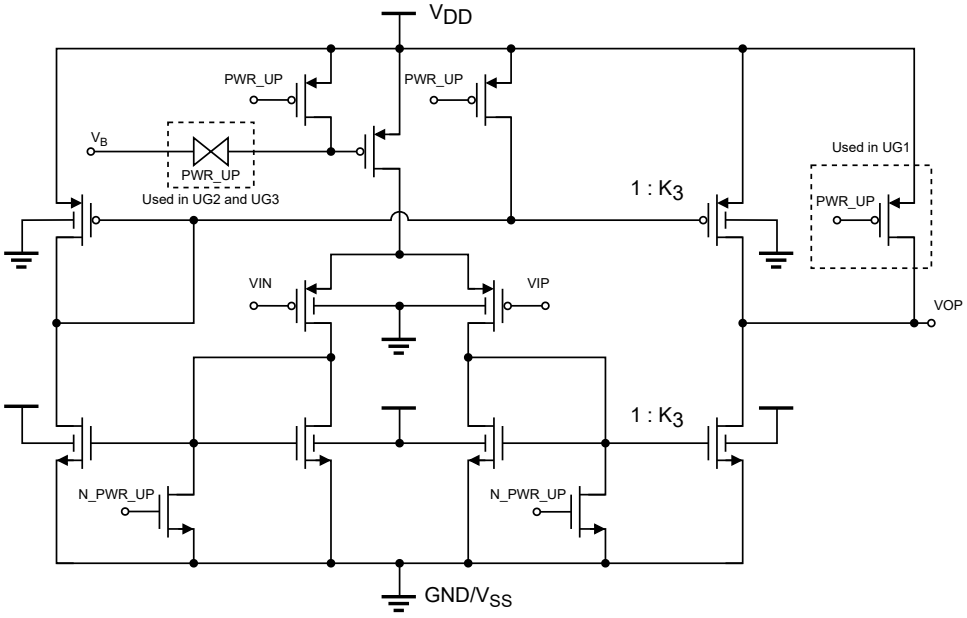


Figure 2.5: Schematic of current mirror OTA.

In the project work [1], the voltage V_{P1} generated in the bias and reference circuit was used to bias all three UG amplifiers as well as the comparator. In contrast to our previous project work, V_{P1} is now only used to bias UG1. In addition to aiding in starting up the triangular relaxation oscillator, UG1 is now used to bias the comparator and the two other UG amplifiers. This significantly reduces the capacitive load on V_{P1}, resulting in the bias and reference circuit starting up faster. Moreover, UG1 already produces an output sufficiently approximately equal to V_{P1}.

The TR gates, the pull-up transistors, and the pull-down transistors were added as a power-saving measure. With this addition, the UG amplifiers are only turned on when they are needed. Additionally, the TR gates, the pull-up transistors, and the pull-down transistors cause reduced power consumption when the

analog system is powered down.

2.2.4 Non-overlapping Clock Generator

Figure 2.6 shows a schematic of the Non-Overlapping Clock (NOC) generator. The purpose of the NOC generator is to provide the SC circuit in the triangular relaxation oscillator with two non-overlapping clocks. These clocks can be identified as φ_1 and φ_2 in Figure 2.2 and Figure 2.6.

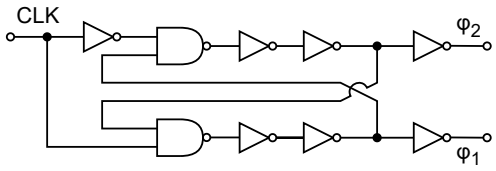


Figure 2.6: Schematic of the Non-overlapping Clock Generator. This is a slightly modified version of [1, p. 12, Figure 3.4].

The NOC generator remains mostly the same compared to the project work [1], with the exception of a few changes. The first change is the addition of one inverter at each output of the NOC generator. The additional inverters provide increased driving ability.

The second difference compared to the project work [1] is that power-saving measures have been added as described in subsection 2.2.1. Firstly, power gating has been implemented as described. This is used to turn off the NOC generator when powering down the analog system. Lastly, the NOC generator utilizes the improved digital logic gates that have less leakage.

2.2.5 Slew-rate controlled triangular relaxation oscillator

The slew-rate controlled triangular relaxation oscillator utilizes a beta-multiplier that is equivalent to the beta-multiplier used in the bias and reference circuit. The beta-multiplier is made up of N_0 and N_1 operating in sub-threshold, and P_0 and P_1 operating in saturation, illustrated in Figure 2.7. The ratio between the transistor N_0 and N_1 is $K_2 = 7/3$. This ratio has also been increased in this work to be equal to the relationship between the equivalent transistors in the bias and reference circuit shown in Figure 2.4. In contrast to the bias and reference circuit, this beta-multiplier does not use a resistor. Instead, an equivalent resistance given by Equation (2.3) is achieved by using a SC circuit made up of C_{REF} and two TR gates. The PTAT current generated by the beta-multiplier is then given by Equation (2.4) found in Appendix C. An 8 MHz clock and a 312.5 fF capacitor are used to achieve an equivalent resistance of 400 kΩ.

$$R_{EQ} = \frac{1}{C_{REF} \cdot f_{REF}} \tag{2.3}$$

$$I_{REF,SC} = \frac{V_T \cdot ln(K_2)}{R_{EQ}} = V_T \cdot ln(K_2) \cdot C_{REF} \cdot f_{REF} \tag{2.4}$$

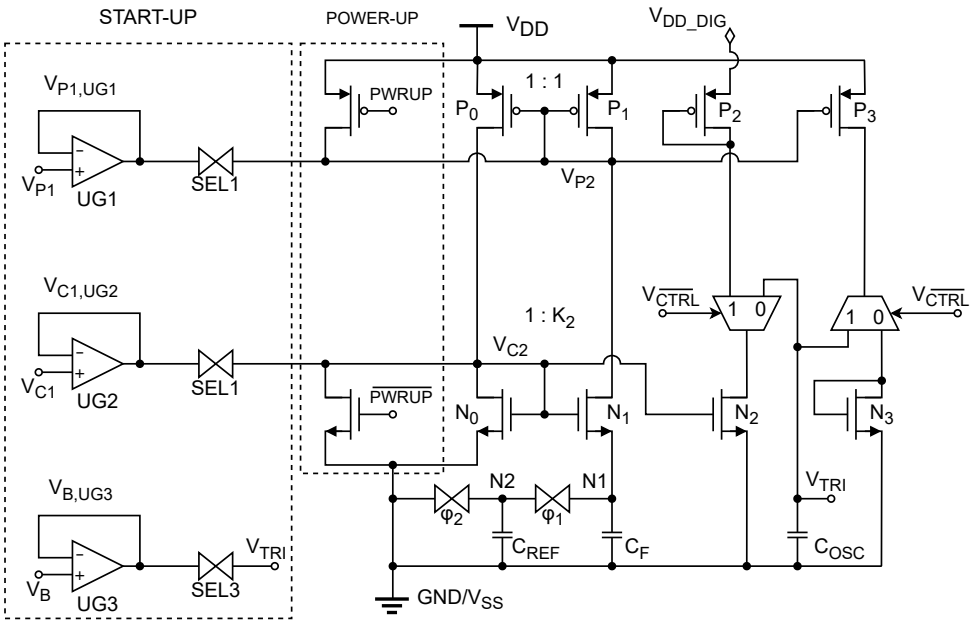


Figure 2.7: Schematic of the slew-rate controlled triangular relaxation oscillator. This is a slightly modified version of [1, p. 13, Figure 3.5].

The PTAT current is copied through P_3 and N_2 as shown in Figure 2.7, charging or discharging the capacitor C_{OSC} respectively. The rate at which the voltage V_{TRI} changes is given by Equation (2.5) where $C_{OSC} = 3 \cdot C_{REF}$. This equation shows that if properly matched, the variations in C_{REF} and C_{OSC} will cancel. As such, these capacitors have been made up of several equally sized capacitors to ensure good matching.

$$SR_{TRI} = \frac{dV_{TRI}}{dt} = \frac{I_{REF,SC}}{C_{OSC}} = V_T \cdot ln(K_2) \cdot \frac{C_{REF}}{C_{OSC}} \cdot f_{REF} \tag{2.5}$$

The capacitor C_F is used to reduce switching noise from the SC circuit. C_F is used as a dummy capacitor surrounding C_{REF} and C_{OSC} in the layout as matching of C_F is not necessary. Additionally, C_F is made up of capacitors of the same size as the ones used for C_{REF} and C_{OSC}, making it suitable as a dummy capacitor.

UG1 and UG2 are used to start up the beta-multiplier in the triangular relaxation oscillator. This is as opposed to using a start-up circuit similar to the one used in the bias and reference circuit. Since the beta-multiplier in the triangular relaxation oscillator is equivalent to the one in the bias and reference circuit, the node voltages of the beta-multipliers are approximately equal. Taking advantage of this, the triangular relaxation oscillator starts up more efficiently by copying

the voltages V_{P1} and V_{C1} from the bias and reference circuit into the equivalent nodes in the triangular relaxation oscillator, V_{P2} and V_{C2}.

UG3 is used to pre-charge V_{TRI} to prepare it for the triangular oscillations. V_{TRI} is charged up to a voltage approximately equal to the reference voltage V_B, generated by the bias and reference circuit. The triangular oscillations will begin earlier by setting V_{TRI} approximately equal to V_B, reducing the conversion time.

Improvements and changes made to the triangular relaxation oscillator will be described for the remainder of this section. In this work, the capacitor C_F has been increased to reduce the impact of switching noise without considerably impacting the start-up time of the circuit. Further, the width and length of the MUXs used to switch between charging and discharging of C_{OSC} have been reduced. This was done to reduce the effect of charge injection and capacitive coupling from gate onto V_{TRI}. The length of the TR gates used in the start-up circuit has been increased to reduce leakage into the beta-multiplier. The length of the TR gates used in the SC circuit has also been increased to reduce leakage. N_0 and N_1 have been split up into shorter transistors in series as recommended [8] for improved mismatch and improved performance over corners.

The dummy transistor P_2 has been tied to the digital supply voltage $V_{DD,DIG}$, which is also used to supply the MUXs. Tying P_2 to $V_{DD,DIG}$ prevents the supply from being shorted to ground when the MUXs are turned off. This does not affect the performance of the circuit, as P_2 is there only to ensure a flow of current through N_2 while C_{OSC} is being charged.

The TR gates and MUXs are now utilizing back-gate switching because the leakage through these led to nonlinearities in the currents flowing in the beta-multiplier. This allowed transistors with higher V_{Th} and longer lengths to be used in the TR gates and MUXs, reducing leakage between the ports without considerably compromising the TR gates' and the MUXs' ability to conduct current.

2.2.6 Comparator

The comparator is a two-stage OTA that is biased by UG1 as shown in Figure 2.8. The purpose of the comparator is to select whether V_A or V_B should be used as V_{REF} and whether V_{TRI} should be charging or discharging. The AND gate is used to let the comparator control $V_{\overline{CTRL}}$ when SEL2 is high. Substituting Equation (2.5) into Equation (2.1) gives Equation (2.6) which expresses the frequency of $V_{\overline{CTRL}}$ during a measurement.

$$f_{out} = \frac{SR_{TRI}}{2 \cdot (V_A - V_B)} = \frac{ln(K_2)}{2} \cdot \frac{C_{REF}}{C_{OSC}} \cdot \frac{V_T}{V_A - V_B} \cdot f_{REF} \tag{2.6}$$

In this work, the comparator has been completely redesigned to work across all corners, including the sf corner in which it failed in our previous project work [1]. It has also been made faster to remedy the effects of parasitic capacitances from the layout. This was achieved by increasing the size of the P-channel Metal-Oxide Semiconductor (PMOS) current mirror and reducing the lengths of the differential

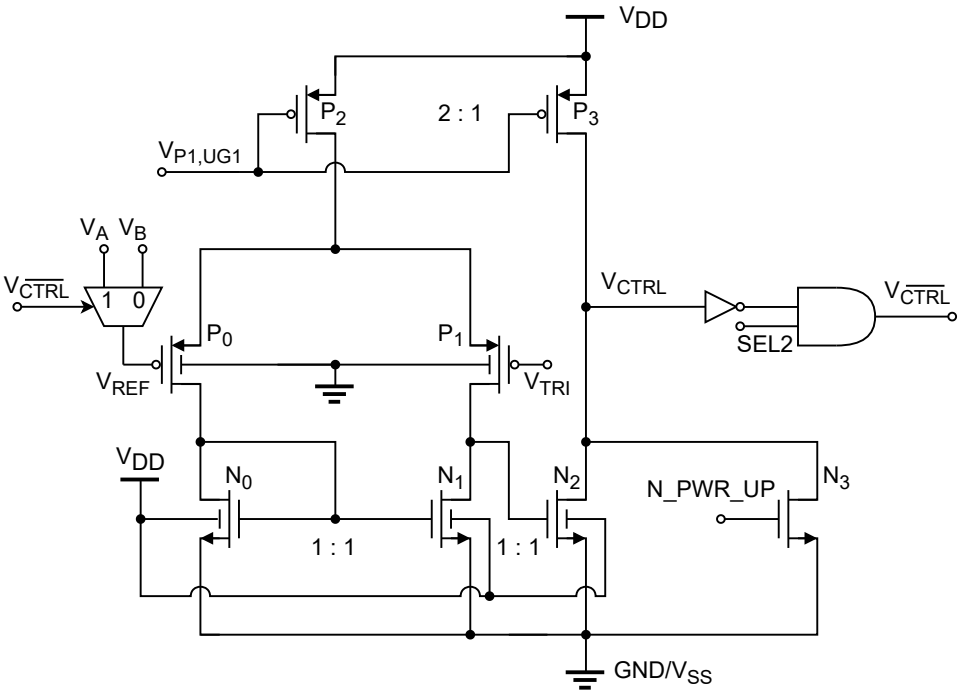


Figure 2.8: Schematic of the comparator. This is a slightly modified version of [1, p. 15, Figure 3.6].

pair and the N-channel Metal-Oxide Semiconductor (NMOS) current mirror. The width of the NMOS current mirror was increased as well. The area of the transistors in the NMOS current mirror was increased for improved noise performance.

The pull-down transistor N3 was added in this work as a power-saving measure. The purpose of this was to prevent V_{CTRL} from floating when the comparator is turned off, as that would cause high currents to flow in the inverter.

The MUX is now utilizing back-gate switching, increasing the MUX's ability to conduct current. Additionally, this allows the use of transistors with higher V_{Th} and longer lengths in the MUX. This was necessary to increase the speed at which V_{REF} is charged and discharged. Previously, V_{REF} was too slow compared to how fast V_{TRI} was charging and discharging, causing nonlinearities in the temperature measurements. Moreover, the leakage between the ports of the MUX was considerably high, also causing nonlinearities in the temperature measurements.

2.3 Digital

In this work, a digital system was designed in SystemVerilog using Vivado 2023.1, synthesized using Cadence Genus Synthesis Solution, and implemented using Cadence Innovus Implementation System. The synthesizing process generates a netlist which is used to generate a schematic in Cadence Virtuoso. A technology library

from INVECAS was the only one available for us to use in the synthesis process. The technology library only employed minimal length SLVT transistors from the 22 nm FD-SOI technology by GF. Innovus was used to place and route the digital system, creating the layout. The SystemVerilog code for all the designed digital blocks can be found in Appendix A.

The purpose of the digital system is to start up and control the analog system. In addition, the digital system will also convert the output of the analog system to a digital value. To achieve the specified functionality, the digital system comprises a FSM, a clock divider, a pulse counter, and an ADC as illustrated in Figure 2.9. This chapter will start off by describing the FSM and the clock divider in subsection 2.3.1. Lastly, the pulse counter and the ADC will be described in subsection 2.3.2.

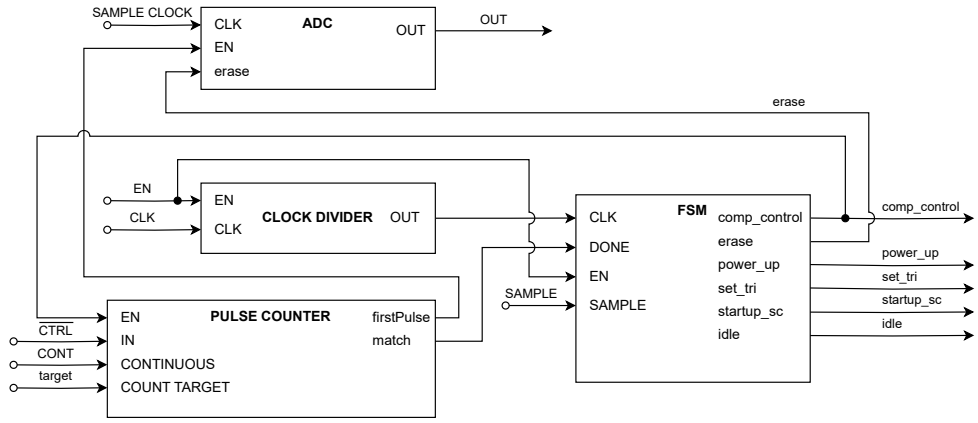


Figure 2.9: Schematic of the digital top.

2.3.1 FSM and Clock Divider

The FSM is a Mealy machine and is the most central part of the digital system. The FSM controls all the other logic blocks except the clock divider. Additionally, it is responsible for starting up the analog system. Figure 2.10 is a state diagram showing the six states in the FSM. The state diagram also shows the conditions for a state change to occur and the outputs of the FSM in each state.

Each state in the FSM except the MEASURE state lasts a specific number of clock cycles. The length of the MEASURE state is determined by the target number of negative edges and the output frequency of $\overline{CTRL}$. In this work, the clock divider reduces the 8 MHz clock used with the SC circuit in the analog system down to 2 MHz. The reduced clock is used with the FSM, ensuring that each state before the MEASURE state lasts long enough to start the analog system properly. Each of the states will be described in the following list:

- **IDLE**
  The initial state of the FSM is the IDLE state as indicated with two circles in

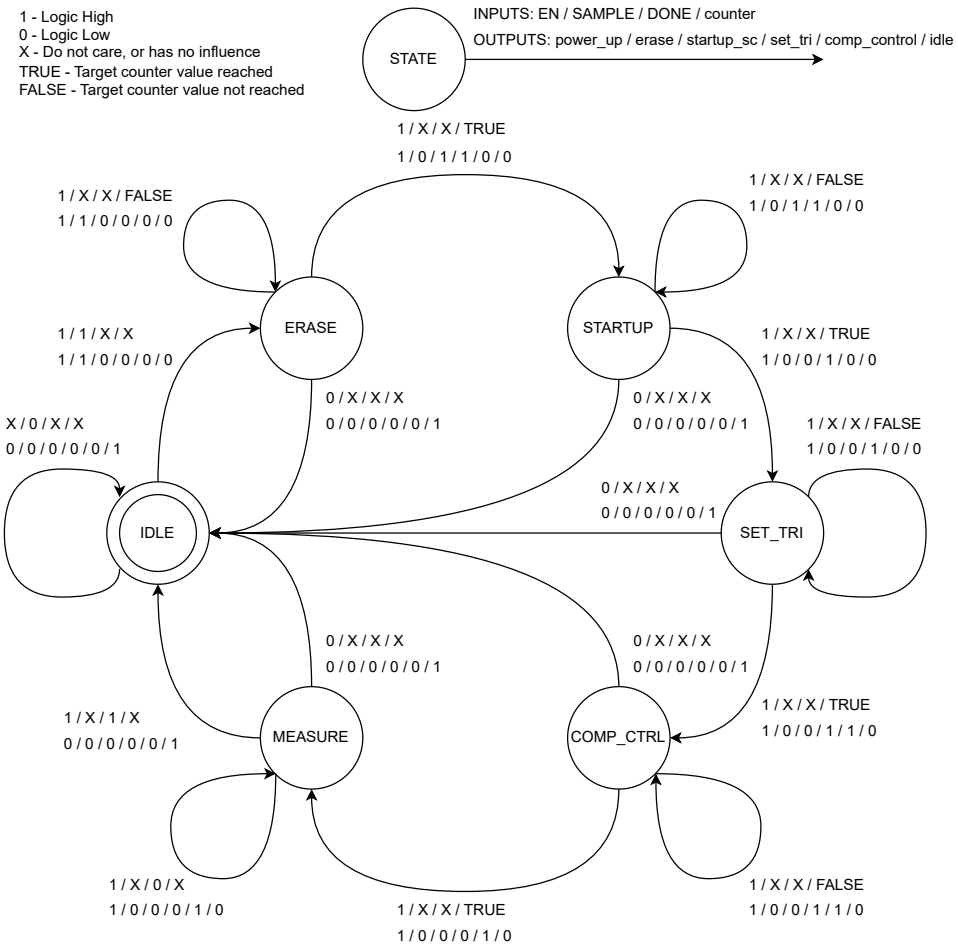


Figure 2.10: State diagram showing what the conditions for state transitions in the FSM are.

Figure 2.10. There are three cases causing the FSM to either transition to or remain in the IDLE state. Firstly, the FSM will transition to and remain in the IDLE state if it is disabled. Secondly, the FSM will remain in the IDLE state if no measurement is initiated with the *SAMPLE* signal. Lastly, the FSM will transition to the IDLE state if it is disabled while performing a measurement.

- **IDLE to ERASE**
  While the FSM is enabled and in the IDLE state, a temperature measurement is initiated when the SAMPLE signal is high. The FSM will then go into the ERASE state. In this state, the data in the ADC is cleared due to the output signal *erase* being pulled high. The output signal *idle* will be pulled low, indicating that the sensor is performing a measurement.

- **ERASE to STARTUP**
  After the ERASE state, the FSM transitions to the STARTUP state. The output *startup_sc* is set high in this state, starting up the beta-multiplier in the slew-rate controlled triangular relaxation oscillator. Pre-charging of the capacitor C_{OSC} is also started in the STARTUP state by setting the output *set_tri* high. $\overline{CTRL}$ is low in this case as the output signal *comp_control* is low. Because of this, the MUXs in the triangular relaxation oscillator are set to discharge V_{TRI} even though UG3 is used to pre-charge V_{TRI} in this state. This causes the actual voltage of V_{TRI} to be a little lower than V_B.

- **STARTUP to SET_TRI**
  The following state is SET_TRI. In this state, the output *set_tri* remains high. The beta-multiplier in the reference and bias circuit is equivalent to the one in the triangular relaxation oscillator as described in subsection 2.2.5. Despite this, their node voltages are different. For this reason, the output *startup_sc* is pulled low in this state, allowing the node voltages of the beta-multiplier in the triangular relaxation oscillator to transition towards their appropriate value.

- **SET_TRI to COMP_CTRL**
  The next state is COMP_CTRL. The output signal *comp_control* is set high, allowing the comparator to control the signal $\overline{CTRL}$. The output signal *set_tri* remains high in this state. This causes $\overline{CTRL}$ to go high since $V_{TRI} < V_{REF}$. Due to this, the MUXs in the triangular relaxation oscillator are set to charge V_{TRI}. The voltage of V_{TRI} will then charge to a voltage between V_A and V_B as UG3 is still used to pre-charge V_{TRI}.

- **COMP_CTRL to MEASURE**
  The MEASURE state is the final state before returning to the IDLE state. In this state the output signal *comp_control* remains high, and *set_tri* is set low, allowing V_{TRI} to charge and discharge towards V_{REF}. The measurement has been performed when the input signal DONE is high, returning the FSM to the IDLE state. This will cause the output *idle* to be pulled high, indicating that the measurement has been finished.

2.3.2 Pulse Counter and ADC

The pulse counter counts the number of negative edges on the signal $\overline{CTRL}$ when the output of the FSM signal *comp_control* is high. When the first negative edge on $\overline{CTRL}$ is registered by the pulse counter, the output signal *firstPulse* is set high. The signal *firstPulse* is used as the enable signal for the ADC, which counts the number of pulses on the sample clock when enabled. The output signal *match* is set high when the pulse counter reaches its target number of negative edges given by the input *COUNT TARGET*. As described in subsection 2.3.1, this results in the

FSM returning to the IDLE state, disabling the pulse counter and turning off the analog circuitry. The output signal *firstPulse* is set low when the pulse counter is disabled, which in turn disables the ADC. The output of the ADC is not cleared even though it is disabled, but it will be cleared when the FSM is in the CLEAR state as described in subsection 2.3.1.

The output value of the ADC is an approximate measure of the time it took to count the target number of negative edges on the signal $\overline{CTRL}$. The time it takes to count a number of negative edges on $\overline{CTRL}$ is given by the input on *COUNT TARGET* and the period of $\overline{CTRL}$. The period of $\overline{CTRL}$ is inversely PTAT as the frequency of $\overline{CTRL}$ is PTAT as seen in Equation (2.7).

$$f_{out} = \frac{SR_{TRI}}{2 \cdot (V_A - V_B)} = \frac{ln(K_2)}{2} \cdot \frac{C_{REF}}{C_{OSC}} \cdot \frac{V_T}{V_A - V_B} \cdot f_{REF} \tag{2.7}$$

This means that the output value of the ADC is also inversely PTAT and given by Equation (2.8). In this equation, NP is the target number of negative edges given by the input *COUNT TARGET*. f_s is the frequency of the sample clock, and f_{out} is the frequency given by Equation (2.7).

$$\text{OUT} = \frac{NP \cdot f_s}{f_{out}} = \frac{NP \cdot f_s}{f_{REF}} \cdot \frac{2}{ln(K_2)} \cdot \frac{C_{OSC}}{C_{REF}} \cdot \frac{V_A - V_B}{V_T} \tag{2.8}$$

Taking the inverse of Equation (2.8) gives Equation (2.9) which is PTAT.

$$\frac{1}{\text{OUT}} = \frac{f_{out}}{NP \cdot f_s} = \frac{f_{REF}}{NP \cdot f_s} \cdot \frac{ln(K_2)}{2} \cdot \frac{C_{REF}}{C_{OSC}} \cdot \frac{V_T}{V_A - V_B} \tag{2.9}$$

2.4 Layout

This work's full layout of the temperature sensor implementation is shown in Figure 2.11. The generated layout for the digital system is Layout Versus Schematic (LVS) clean, but not Design Rule Check (DRC) clean. An initial draft of the layout was made for the digital system to get an estimate of current consumption and how much area it would occupy. However, it would have to be DRC clean before tape-out. Excluding the layout of the digital system, the full temperature sensor layout is LVS and DRC clean, except for some minimum density errors in the DRC. The full layout occupies an area of $70\ \mu\text{m} \cdot 140\ \mu\text{m} = 0.0098\ \text{mm}^2$.

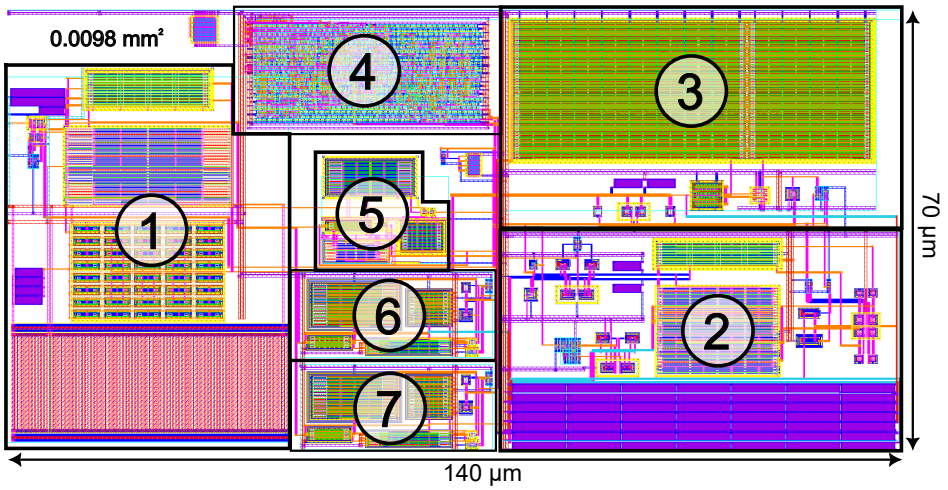


Figure 2.11: The full layout of this work's temperature sensor implementation. ① Bias and reference circuit ② Triangular relaxation oscillator ③ Comparator ④ Digital system ⑤ Unity Gain 1 (UG1) ⑥ Unity Gain 2 (UG2) ⑦ Unity Gain 3 (UG3)

Chapter 3

Simulation Results

This chapter will first describe the simulation methodology. Next, verification of the subcircuits will be presented. The following section will describe the top-level behavior of the temperature sensor implementation. The next section will present power consumption results, followed by results on accuracy. Finally, this work will be compared to the project work [1].

3.1 Simulation methodology

In this work, each subcircuit has been tested by itself to ensure that they function as desired. The subcircuits have then been tested together as a complete system to ensure overall functionality and specifications. The tests have been performed in Cadence Virtuoso as simulations across several corners for the analog system and the overall system. Furthermore, the tests have been performed in pre-layout and post-layout simulations. The digital system has been tested in Vivado 2023.1 as plain code, followed by being tested in Cadence Virtuoso together with the analog system as plain code, synthesized digital netlist, and implemented digital layout.

The relevant corners that have been used in the simulations in Cadence Virtuoso are slow-slow (ss), fast-fast (ff), fast-slow (fs), slow-fast (sf), and typical-typical (tt). The pre-layout and post-layout variant of these corners was used for schematic and post-layout extraction simulations, respectively. The simulations have also been performed with different supply voltages ranging from ±10% from the typical supply voltage (Vt) 0.8 V. The lowest supply voltage (Vl) is 0.72 V, and the highest supply voltage (Vh) is 0.88 V. Lastly, the simulations have been run across the full temperature range of the transistor models from -40 °C (Tl) to 125 °C (Th), where 27 °C is the typical temperature (Tt).

3.2 Subcircuit verification

The beta-multiplier in the bias and reference circuit as explained in subsection 2.2.2 has been verified to operate in the correct regions. N_1 and N_0, in

subthreshold and P_1 and P_0, in saturation are well within their regions over all corners which ensures proper operation. Thus the generated current which biases the other subcircuits exhibit PTAT characteristics which has a maximum linearity error of 1.22 °C. Low linearity error also ensures that the DBGR and V_{BG} are less affected by temperature. V_{BG} performs well over all corners but the have a slightly worse voltage variation for the ff of 3.22 mV, and the ss corner of 3.14 mV (Table B.1). This is reflected in the result from the DBGR where it achieves a 17.79 ppm/°C over typical corner and a worst case in the ff of 47.11 ppm/°C and ss 47.67 ppm/°C which can be seen in Table 3.1. Having a DBGR which is stable over temperature, ensures that the system's performance is robust. The supply variation is simulated to be around 3 % per volt. The DBGR has a 19.1% variation over corners (Figure B.1).

Table 3.1: Corner simulation results of temperature and line regulation performances of reference voltage V_{AB}. LAYOUT

Corner	V_{AB}@27°C (mV)	ΔV_{AB} (uV)	ppm/°C	%/V
tt	30.80	88.62	17.79	3.47
ff	28.32	207.00	47.11	3.53
fs	29.79	180.60	36.73	3.61
sf	31.80	56.17	38.22	3.33
ss	33.51	137.10	47.67	3.31

Similar tests were performed for the beta-multiplier in the triangular relaxation oscillator. The current have been verified to be PTAT with a similar linearity error as in bias and reference. This has been verified, as these currents directly impact the slew rate of the triangular oscillations and thus the digital output of the overall system. Moreover, this also verified the operation of the NOC generator. The startup time of the circuit has been checked, verifying the operation of the unity gain amplifiers. Furthermore, this verifies that the circuit has started properly before measuring temperature.

The stability of the UG amplifiers has been verified while connected to the full system to ensure proper operation. In addition, the UG amplifier's ability to produce an approximate copy of the input has been verified to be within 4 mV. From stability analysis simulations, all of the UG amplifiers achieve a phase margin of more than 45°.

Simulations were performed to verify the operation of the comparator. The speed of the comparator was checked to be high enough. This is because it would have caused V_{TRI} to charge or discharge too far compared to the relevant V_{REF} if it were too slow. Furthermore, a slow comparator could result in high and varying offsets between V_{TRI} and V_{REF}. This would cause the system not to behave as expected according to the equation describing the system. Also, it could affect the linearity of the output negatively.

3.3 Functional behavior of top level

The top level output behavior and FSM control of the implemented temperature sensor is shown in Figure 3.1. The waveforms in Figure 3.1 are extracted from simulation data in the tt corner without noise at 20 °C and a supply of Vt. The ADC is clocked by a 128 MHz clock, and the target number of negative edges has been set to four.

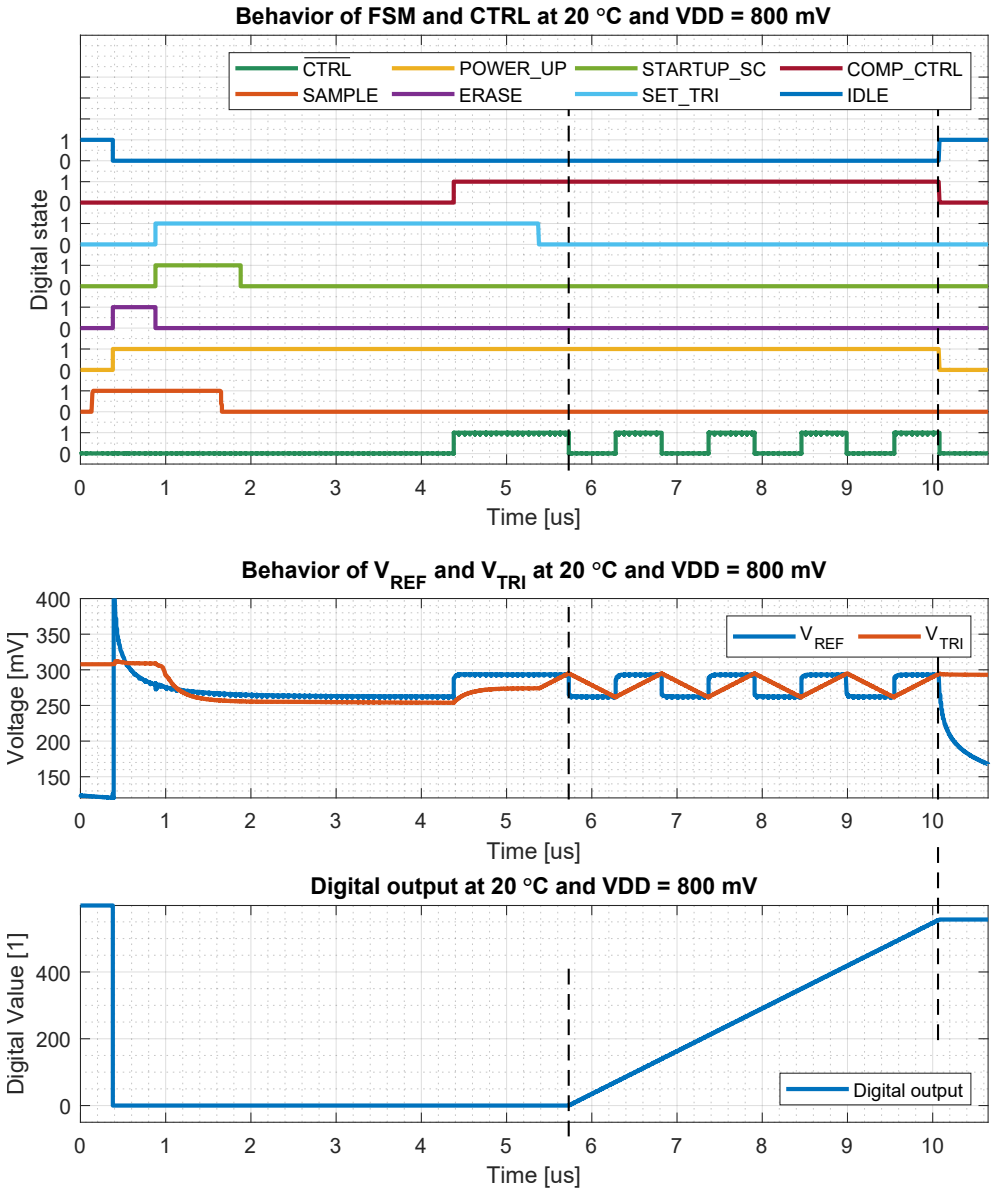


Figure 3.1: Behavior of the temperature sensor implementation in the tt corner without noise at 20 °C and a supply of Vt.

The following list describes the behavior shown in Figure 3.1 through the states of the FSM.

- **IDLE to ERASE**
  As shown in Figure 3.1, the sensor starts in the IDLE state indicated by the IDLE signal being high. Shortly after the SAMPLE signal goes high, the FSM enters the ERASE state. This causes the IDLE signal to go low and the ERASE signal to go high. Additionally, the POWER_UP signal goes high, starting up the analog circuitry. It can be observed that V_{REF} starts settling during the ERASE state due to the POWER_UP signal going high.

- **ERASE to STARTUP**
  On ERASE going low, the signals STARTUP_SC and SET_TRI go high. This indicates that the FSM has transitioned from the ERASE state to the STARTUP state. Pre-charging of V_{TRI} is started in this state, as can be observed from Figure 3.1 due to V_{TRI} settling to another voltage than it started at.

- **STARTUP to SET_TRI**
  On STARTUP_SC going low, the FSM transitions from the STARTUP state to the SET_TRI state. SET_TRI remains high in this state, keeping V_{TRI} at the same voltage as before.

- **SET_TRI to COMP_CTRL**
  The comparator is allowed to control the signal $\overline{CTRL}$ when the signal COMP_CTRL is pulled high, as can be observed from Figure 3.1. This indicates that the FSM has transitioned from the SET_TRI state to the COMP_CTRL state. Due to $V_{TRI} < V_{REF}$ when COMP_CTRL is pulled high, the signal $\overline{CTRL}$ is pulled high.

- **COMP_CTRL to MEASURE**
  When SET_TRI goes low, it can be observed that V_{TRI} starts increasing at a constant rate. This indicates that the FSM has transitioned from the COMP_CTRL state to the MEASURE state. On the first negative edge on $\overline{CTRL}$, the ADC starts counting, as can be observed from the bottom subplot in Figure 3.1.

- **MEASURE to IDLE**
  As the target number of negative edges on $\overline{CTRL}$ is reached, it can be observed from Figure 3.1 that the signal IDLE is pulled high. This indicates that the measurement has finished and that the FSM has transitioned from the MEASURE state to the IDLE state. Because of this, the FSM turns off the analog circuitry by pulling the signal POWER_UP low. Additionally, the FSM pulls the signal COMP_CTRL low, causing the ADC to stop counting. Finally, it can be observed that the final output value of the ADC is retained after

the measurement has finished, allowing for the output value to be read in between measurements.

3.4 Power consumption

The background for the measurement of the temperature sensor implementation's power consumption is post-layout simulations in the tt corner at 27 °C (Tt) and a supply of 0.8 V (Vt). The ADC in the digital system was clocked with a sampling clock of 128 MHz, and the target number of negative edges to be counted on $\overline{CTRL}$ was set to four. The temperature sensor implementation operated at a duty cycle of around 0.1% over a 10 ms period.

The peak power consumption of the temperature sensor implementation was 0.49 mW. The average power consumption over the 10 ms period was 29.0 nW. The average power consumption during the 9.6 μs conversion period was 26.7 μW. Finally, the average power consumption during the off period was 3.63 nW.

The pie chart in Figure 3.2 shows an overview of the average power consumption of each part of the sensor implementation over the 10 ms period. From the pie chart, it can be seen that the digital system consumes the most power, followed by the comparator. This is to be expected as the comparator was made faster, and the digital system utilizes minimum length SLVT transistors. From the simulation results, the digital system and the comparator contributed the most during conversion. The unity gain amplifiers had the biggest contribution of around 70% while the circuit was powered down.

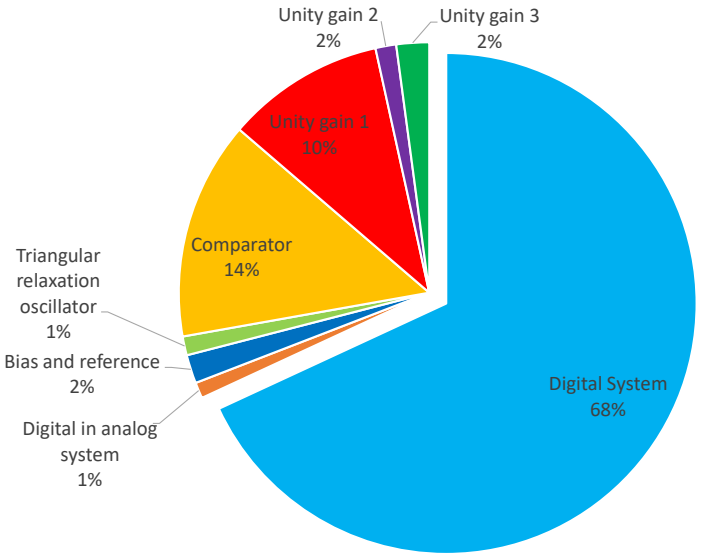


Figure 3.2: Pie chart of the system's total power consumption with a 128 MHz sample clock.

In Figure 3.3 it can be seen that our work competes with other sensors in energy efficiency. There are possibilities to become more energy efficient, which will be discussed in chapter 4. The purple Resolution Figure of Merit (R-FoM) lines illustrated in Figure 3.3 are given by Equation 3.4, where a lower R-FoM is better.

$$Resolution-FoM = \frac{Energy}{Conversion} \cdot Resolution^2 \tag{3.1}$$

By varying either the sampling clock or the amount of target negative edges on $\overline{CTRL}$, a different resolution can be achieved. The target number of negative edges has been varied by setting it to 4, 24, and 48 for three different frequencies as shown in Figure 3.3. This increases the conversion time from 9.6 µs to 30.2 µs and 55.4 µs, respectively. A 128 MHz sampling clock with 4 pulses achieves a resolution of around 0.5 °C while maintaining under 9.6 µs conversion time as set by the specification. The energy consumption during conversion in this case is simulated to be 256 pJ, and the R-FoM can be calculated to be 88.3 $pJ \cdot K^2$. The highest resolution was simulated to be 0.048 °C with 48 sampling edges using the 128 MHz sampling clock. This achieves a better R-FoM of 3.3 $pJ \cdot K^2$, with 1448 pJ used for the conversion.

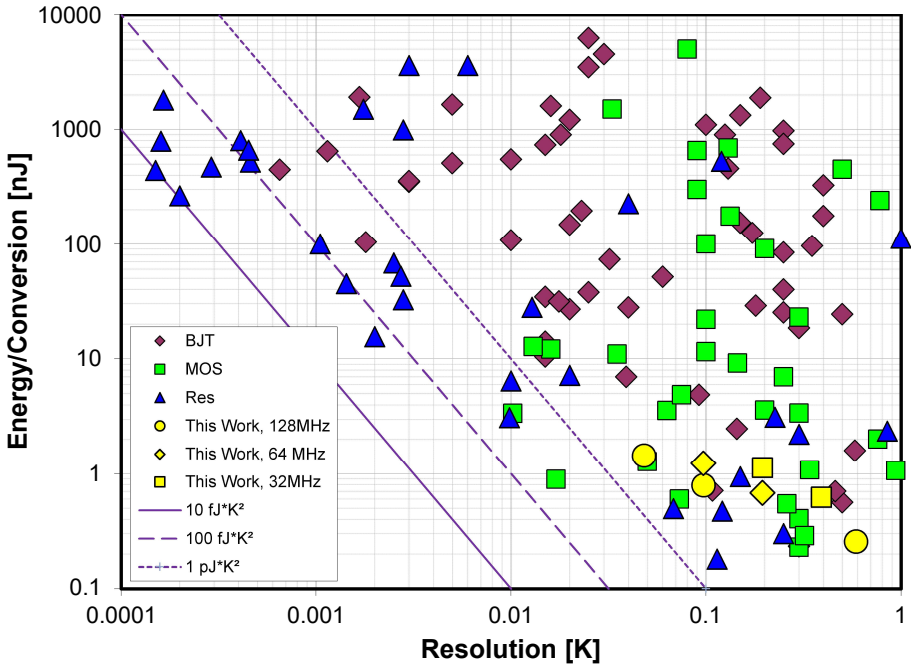


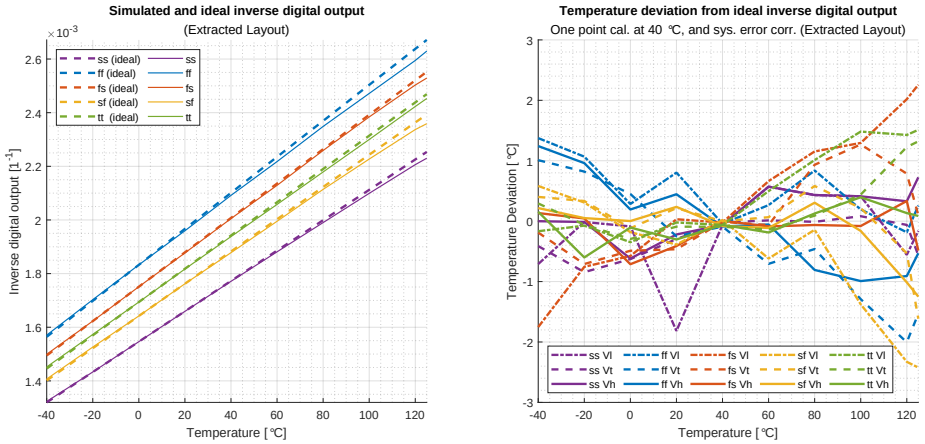
Figure 3.3: Energy efficiency comparison between previous sensors [9]

3.5 Temperature accuracy

The system's performance over the range -40 °C to 125 °C was simulated with the target number of negative edges set to four and a 128 MHz sampling clock. This resulted in a resolution of approximately 0.5 °C in the tt corner.

In Figure 3.4 and Figure 3.5, the results across post-layout corner simulations are presented. For the temperature sensor implementation to achieve an accuracy according to the specifications, it requires at least a one-point calibration. This is necessary due to the spread of the measurements across corners, which can be observed in Figure 3.4a. The ideal lines in Figure 3.4a are calculated using Equation (2.9) repeated here in Equation (3.2), where every variable except the DBGR, V_{AB}, is the same for each ideal line.

$$\frac{1}{\text{OUT}} = \frac{f_{out}}{NP \cdot f_s} = \frac{f_{REF}}{NP \cdot f_s} \cdot \frac{ln(K_2)}{2} \cdot \frac{C_{REF}}{C_{OSC}} \cdot \frac{V_T}{V_A - V_B} \tag{3.2}$$



(a) Comparison between the ideal and simulated digital output for extracted layout.

(b) One point calibration with systematic error correction

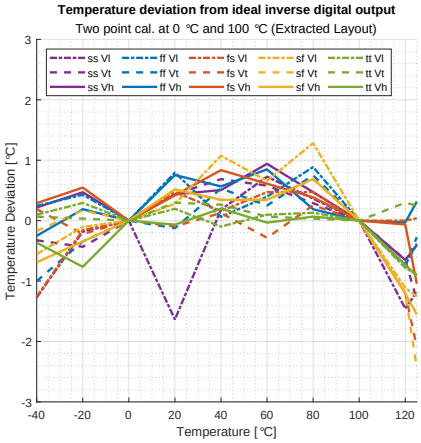
Figure 3.4: Overall system performance over worst case process corners and supply variation with 1-point calibration

Two known sources have a large contribution to the spread in the measurements. First, from the observed bias and reference results in section 3.2, it can be observed that V_{AB} has a dependence on corners. Thus, the measurements have a dependency on corners as V_{AB} directly impacts them. Second, an offset has been observed on V_{TRI} which impacts the oscillation frequency, and will be discussed in section 4.5. The offset on V_{TRI} can be adjusted to some degree by adjusting the V_{AB} of the ideal lines as done in Figure 3.4a.

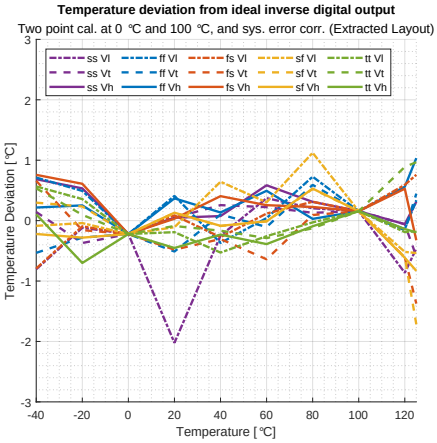
From Figure 3.4a, it can be seen that the system's digital output follows Equation (3.2) closely after a one-point calibration. Except for at higher temperatures,

the measurements are gradually reduced compared to the ideal lines. The temperature deviations with respect to the ideal lines after a systematic error correction are shown in Figure 3.4b. It can be seen from the figure that the worst-case peak-to-peak inaccuracy that can be achieved is an inaccuracy of -2.4 °C to 2.2 °C. While a worst-case peak-to-peak inaccuracy of -5.7 °C to 2.7 °C is achieved without the systematic error correction as can be seen in Figure B.5. On the other hand, pre-layout simulations performed on the schematic did not require systematic error correction, achieving a worst-case peak-to-peak inaccuracy of -1.5 °C to 2.9 °C, as can be seen from Figure B.3.

Figure 3.5a and Figure 3.5b shows the result after a two-point calibration. It can be observed from Figure 3.5a that the worst case peak-to-peak inaccuracy is -2.3 °C to 1.3 °C without systematic error correction. From Figure 3.5b it can be seen that with systematic error correction, a worst-case peak-to-peak inaccuracy of -2 °C to 1.1 °C is achieved.



(a) Two point calibration



(b) Two point calibration with systematic error correction

Figure 3.5: Overall system performance over worst case process corners and supply variation with 2-point calibration

To determine the system's noise performance, noise simulations were performed in the tt corner over the range -40 °C to 125 °C with 1 GHz noise and a supply of 0.8 V (Vt). The simulations were set up with a target number of negative edges of four and a sample clock of 128 MHz. Each simulated temperature was measured ten times in each simulation, resulting in a standard deviation of 1.24 °C at -40 °C, 2.06 °C at 27 °C, and 2.41 °C at 125 °C. This shows an increasing trend with increasing temperature. The increased standard deviation can be explained by both the increased temperature and the temperature sensor's reduced resolution. A higher resolution could give a more representative indication of the standard deviation.

From Monte Carlo Mismatch (MCMis) simulations, a 3σ 1.71 °C were

achieved. The simulations were performed in the tt corner over the range -40 °C to 125 °C with a supply of 0.8 V (Vt). The target number of negative edges to be counted was set to four, and a sampling clock of 128 MHz was used.

3.6 Comparison to state at end of project

Table 3.2 compares this work with the project work [1]. Both sensor implementations have been made in the 22 nm FD-SOI technology by GF, but a layout has only been made for this work. They both operate at the same supply voltage and work across the full temperature range of the technology's transistor models. The area of this work is about three times larger than the estimated area of the project work. The difference in area between the project work and this work will be discussed in section 4.2.

Table 3.2: Performance comparison between the temperature sensor implementation from this work and our previous project work [1]. The inaccuracies in parentheses exclude the sf corner.

Sensor	Previous project work [1]		This work				
Simulation type	Schematic		Layout				
Technology	22 nm FD-SOI		22 nm FD-SOI				
Supply Voltage [V]	0.8		0.8				
Trim	2		2			1	
Temperature range [°C]	0 ~80	-40 ~125	0 ~80	-40 ~125		0 ~80	-40 ~125
Inaccuracy [°C]	1.45	13.5 (3.5)	-1.7 ~0.7 [a]	-2.3 ~1.3	-2 ~1.1[a]	-1.8 ~1.2 [a]	-2.4 ~2.2 [a]
Relative Inaccuracy [%]	1.81	8.18 (2.12)	3.00 [a]	2.18	1.87[a]	3.75 [a]	2.18 [a]
Area [mm^2]	0.003		0.0098				
Conversion time [μs]	10		9.6				
Resolution [°C]	N/A		0.58				
$\frac{Energy}{Conversion}$ [pJ]	38		256				
Resolution FoM [pJ·K^2]	N/A		88.3				

[a] With systematic error correction.

The layout of this work achieves an inaccuracy and relative inaccuracy that is close to that of the schematic from the project work. This is considering the full temperature range and a two-point calibration. The inaccuracy of the layout from this work is 3.6 °C as opposed to 3.5 °C. The relative inaccuracy of this work's layout is 2.18 % and can be found from Equation 3.6. The relative inaccuracy of the project work is 2.12 %. This is expected, considering that layout simulations are expected to perform worse than schematic simulations. Also, that is only if we exclude the sf corner in the project work due to the comparator design. Otherwise, it would have a considerably worse inaccuracy and relative inaccuracy of 13.5 °C and 8.18 %, respectively. With systematic error correction applied to

the simulation results, the layout of this work achieves a better inaccuracy and relative inaccuracy of 3.1 °C and 1.87 % compared to the project work.

$$\text{Relative Inaccuracy} = \frac{\text{Peak-to-peak inaccuracy}}{\text{Temperature Range}} \cdot 100\% \tag{3.3}$$

The performance of the layout in a temperature range of 0 °C to 80 °C is worse than that of the project work with a two-point calibration. The layout of this work achieves an inaccuracy and relative inaccuracy of 2.4 °C and 3 °C, respectively. While the project work achieves an inaccuracy and relative inaccuracy of 1.45 °C and 1.81 °C, respectively.

In contrast to the project work, a one-point calibration has been performed in this work. In the range 0 °C to 80 °C, an inaccuracy and relative inaccuracy of 3 °C and 3.75 % are achieved, respectively. In the range -40 °C to 125 °C, an inaccuracy and relative inaccuracy of 4.6 °C and 2.18 % are achieved, respectively. The inaccuracy in both temperature ranges is better than the full temperature range case in the project work.

The average power consumption and energy consumption of the project work [1] and this work is compared in Table 3.3. They are both compared to each other with a duty cycle of 100% and a duty cycle of about 0.01%.

The average power during the active period is lower for the project work compared to this work by a factor of 6.82. Because of this, the project work achieves a better energy consumption per conversion of 38 pJ compared to the 256 pJ of this work at 100% duty cycle. The digital system implemented in this work greatly contributes to the average power during the active period. This can be seen from Table 3.3 as the analog system represents about 1/4 of the total average power consumption. This has also been illustrated in Figure 3.2. Additionally, the redesigned comparator also has a large contribution to the average power. These were both subjects of the future work discussion of our previous project work and thus considered to be necessary additions to this work.

Table 3.3: Comparison of power consumption between the project work and this work.

Sensor	Previous project work [1]		This Work	
Simulation type	Schematic		Layout	
Conversion time [μs]	10	100 000	9.6	100 000
Duty Cycle [%]	100	0.01	100	~0.01
Average Power [μW]	3.82	0.0163	26.7	0.0063
$\frac{Energy}{Conversion}$ [pJ]	38	1636	256	630
Active Power [μW]	3.82		26.7	
Inactive Power [μW]	0.0159		0.0036	
Analog System's Active Power [μW]	3.82		6.32	

The temperature sensor implementation of this work achieves a lower energy per conversion compared to the project work at lower sampling rates. With a duty

cycle of about 0.01%, this work achieves an average power of 6.3 nW. This is a factor of 2.5 times lower than the average power of the project work, which is 16.3 nW. The resulting energy per conversion of this work is then 630 pJ as opposed to the 1636 pJ of the project work. The low average power and energy consumption per conversion are achieved due to this work's low average inactive power. Compared to the project work, a reduction in average inactive power of about 4.4 times has been achieved.

Chapter 4

Discussion

This chapter starts with comparing the proposed temperature sensor implementation of this work to prior state-of-the-art sensors in section 4.1. The difference in the estimated area and the area of the current work and suggestions to reduce the area of the current work are discussed in section 4.2. A one-point calibration method that adjusts the back-gate potential of P_A to vary the DBGR, V_{AB}, is described in section 4.3. The effects of dynamic element matching and where it could be utilized are discussed in section 4.4. The reason behind the offset introduced on V_{TRI} is described in section 4.5 with suggestions to reduce the offset. Possible power-saving measures are discussed at the end of this chapter. Using a different library for the digital system is discussed in section 4.6. Power gating of the unity amplifiers is considered in section 4.7. Lastly, shortening of the pre-charge period of V_{TRI} is discussed section 4.8.

4.1 Comparison to prior art

Figure 4.1 shows a graphical comparison between this work and other sensors from prior art with respect to process node and relative inaccuracy. The temperature sensor implementation of this work performs well compared to other CMOS and Bipolar Junction Transistor (BJT) sensors, as seen from Figure 4.1. A trendline has been added to illustrate how lower-process node sensors are more inaccurate. Despite the trend showing an increasing relative inaccuracy with smaller nodes, this work performs better than given by the trendline after a 2-point calibration.

Table 4.1 compares this work with temperature sensors from different papers. Some initial differences are the technology of choice, the supply voltage, area, and sensing range. Of the sensors being compared, this work is the only sensor implemented in the FD-SOI technology. Additionally, the sensor in this work is supplied with 0.8 V (Vt), which is the lowest supply voltage. The area of the temperature sensor implementation in this work is the second smallest, with the sensor in [10] being the smallest. This work's temperature sensor implementation has the widest sensing range of the sensors, with the possibility of both one- and two-point calibration.

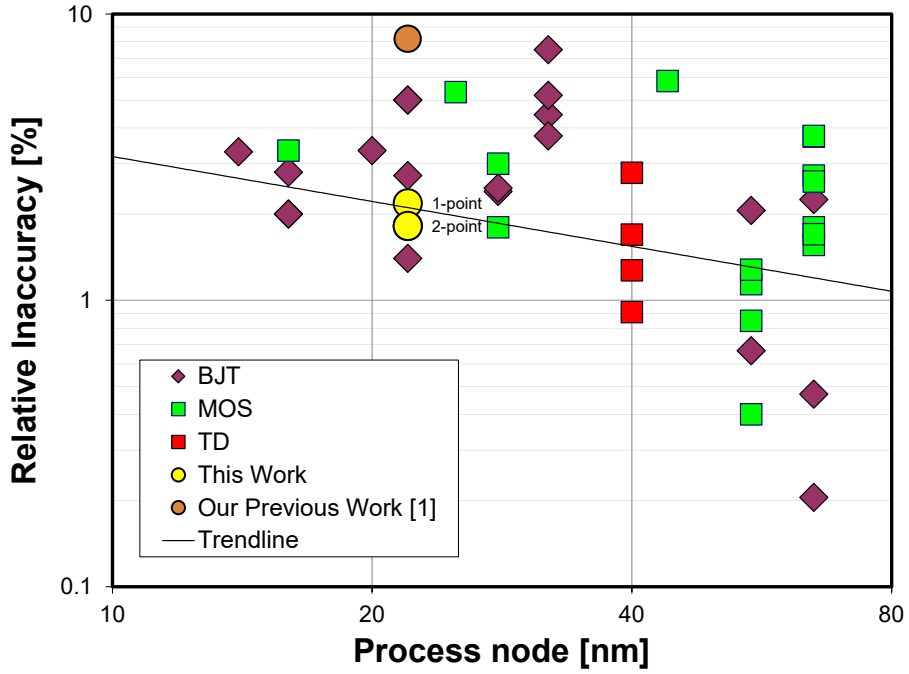


Figure 4.1: Relative inaccuracy versus sensors in close proximity to the technology used [9]

As previously observed from Figure 4.1, the inaccuracy of lower technology nodes increases with a reduction in node size. This can also be seen from Table 4.1, where the sensors in the three smallest nodes have the highest inaccuracy. This includes the sensor of this work, with a worst-case inaccuracy of -2.4 ~2.2 °C after a one-point calibration. On the other hand, the sensor of this work achieves the best inaccuracy of the sensors in the three smallest nodes after a 2-point calibration. Additionally, the relative inaccuracy of this work's sensor is comparable to that of the two sensors in the largest nodes.

The sensor implementation of this work achieves the best energy per conversion compared to the other sensors, as seen from Table 4.1. This is the case even for conversions that are 8500 μs long with a duty cycle of about 0.1%. Despite this, the R-FoM is between 2 - 3 times higher than the R-FoM of the other sensors due to the high resolution

Increasing the sample clock or target number of negative edges of this work can achieve a lower R-FoM. As seen in section 3.4, an R-FoM of 3.3 pJ·K^2 can be achieved using a 128 MHz sampling clock with the target number of negative edges set to 48. With this configuration, the energy consumption per conversion is 1448 pJ, and the resolution is 0.048 °C. Compared to the other sensors in Table 4.1, this work still does not consume the most energy per conversion. The sensor in [12] consumes the most energy per conversion but achieves a better R-FoM due to the high resolution. This work's achieved R-FoM of 3.3 pJ·K^2 is also

Table 4.1: Performance comparison between the temperature sensor implementation from this work and prior art [9].

Sensor	This work		M.K. Law [7]	Y. Kim [11]	S. Park [12]	Y. Lempel [10]
Technology	22 nm FD-SOI		180 nm CMOS	25 nm CMOS	28 nm CMOS	16 nm FinFET
Supply Voltage [V]	0.8		1	1.1	1	1.2
Area [mm^2]	0.0098		0.032	0.02	0.017	0.0007
Temperature range [°C]	-40 ∼125		0 ∼100	20 ∼95	-10 ∼90	-20 ∼110
Trimming	2	1	2	1	1	2
Inaccuracy [°C]	-2 ∼1.1	-2.4 ∼2.2	-0.8 ∼1	± 2	± 0.9	± 2
Relative Inaccuracy [%]	1.87	2.18	1.8	5.3	1.8	3.1
Conversion time [μs]	8500	9.6	1000	142	100	6.9
Power [μW]	0.033	26.7	0.4	9.0	33.75	41.8
$\frac{Energy}{Conversion}$ [pJ]	286	256	405	1278	3375	288
Resolution [°C]	0.589	0.589	0.3	0.05	0.01	0.32
Resolution FoM [pJ·K^2]	99.5	88.3	36.45	3.20	0.35	29.53

comparable to the second best R-FoM of 3.20 pJ·K^2 by [11], but the energy per conversion of [11] is lower.

4.2 Area in the project work versus this work

In the project work, an initial approximation of the area was made where minimum well spacing and transistor placement were not accounted for. The layout of this work grew to be larger than the initial estimation due to this and the changes that were made to the design. The main contributions were the added digital system and a bigger PMOS current mirror in the comparator. Better planning of the layout could further improve the utilization of space in the implementation. The digital system would not necessarily need to be implemented as a solid block but could rather float around the edges of the analog system. Another space-saving measure would be placing the capacitor array used in the triangular relaxation oscillator over a different component, such as the resistor in the bias and reference circuit or the PMOS current mirror in the comparator.

4.3 Calibration of V_{AB}

Scaling of the back-gate voltage of P_A, V_{BG}, is a different approach to 1-point calibration. Trimming the back-gate voltage of P_A will change the amplitude of the DBGR, V_{AB}. This will directly impact the output frequency of $\overline{CTRL}$ as described by the equation for the frequency of $\overline{CTRL}$, Equation (2.7), repeated here in Equation (4.1).

$$f_{out} = \frac{SR_{TRI}}{2 \cdot (V_A - V_B)} = \frac{ln(K_2)}{2} \cdot \frac{C_{REF}}{C_{OSC}} \cdot \frac{V_T}{V_A - V_B} \cdot f_{REF} \tag{4.1}$$

Typically, the results from corner simulations do not overlap as previously seen in Figure 3.4a. Through initial schematic simulations with an ideal 8-bit resistor network used for trimming, it can be seen from Figure 4.2 that the results across corners approximately overlap if $\overline{CTRL}$ is calibrated to the same frequency at the same temperature in every corner. This is due to Equation (4.1) being a good approximation of the behavior of the temperature sensor implementation. By performing a calibration like this, a possible inaccuracy of ±2 °C across corners can be achieved as shown in Figure B.7.

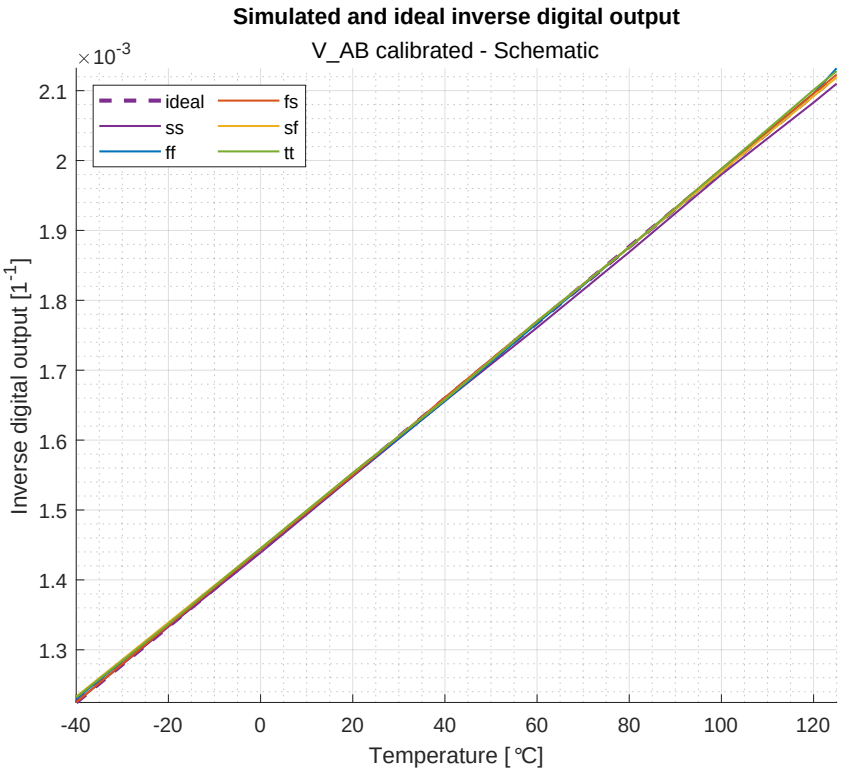


Figure 4.2: Comparison between the ideal and simulated digital output for schematic after calibrating V_{AB}. Calibrated using an ideal 8-bit resistor network.

4.4 Dynamic element matching

The presented work performs within specifications, but still have room for improvement. There are an abundant of possible complex implementations that could improve the performance of the system. One of these implementations are dynamic element matching. One of the main contributors to mismatch in Monte

Carlo simulations was observed to be the current mirrors used in the bias and reference circuit and the triangular relaxation oscillator circuit. In [13], dynamic element matching is used to better the performance of current mirrors, as precise layout alone would not be sufficient to achieve a temperature error resulting from mismatch to be ± 0.01 °C. By utilizing dynamic element matching, mismatch errors could be averaged out and overall improve the performance of the system.

4.5 Offset on V_{TRI}

It has been observed from simulations that considerable offset is introduced on V_{TRI}, causing gain errors as mentioned in section 3.5. The root cause of this was two things initially. The first is charge injection and capacitive coupling, which has been reduced in this work as described in subsection 2.2.5. The second cause has been identified as the voltage difference between V_{TRI} and the drain of both P_3 and N_2.

The MUXs used to charge and discharge V_{TRI} could be modified to reduce the effects of charge injection and capacitive coupling even more. The MUXs are now made up of TR gates consisting of both an NMOS and a PMOS. Charge injection and capacitive coupling could be reduced if the TR gates inside the MUXs were swapped out with a single transistor. The MUX used to discharge V_{TRI} could utilize two NMOS transistors instead of the current TR gates. The MUX used to charge V_{TRI} could utilize two PMOS transistors instead of the current TR gates. To reduce the charge injection further, transistors of the same type with half the length could be added on each side of the transistors that have replaced the TR gates in each MUX. These would then be switched oppositely to that of the transistor that replaces the TR gate.

The voltage difference between V_{TRI} and the drain of both P_3 and N_2 is currently the main contributor to the offset introduced on V_{TRI}. As the MUXs switch over to either charge or discharge V_{TRI}, the difference in voltage between V_{TRI} and the node it is connected to through the MUXs is large enough to offset V_{TRI}. This has been observed to be able to cause the voltage of V_{TRI} to change with about 1 mV. The voltage at the drain of P_3 and N_2 does not cause the same amount of offset on V_{TRI}. Because of this, the period of V_{TRI} changes as an effect of the introduced offset. As described in section 3.5, the offset causes a reduction in the frequency of $\overline{CTRL}$.

To reduce the offset introduced on V_{TRI} by the drain of both P_3 and N_2, the branches with the dummy transistors, P_2 and N_3, should be considered. Initial simulations where the length of P2 and width of N3 were increased showed reduced offsets. This is because the changes caused the voltage difference between V_{TRI} and the drains of P_3 and N_2 to be reduced.

4.6 The digital system's power consumption

The digital system represent around 70% of the temperature sensor implementation's power consumption. This is to be expected with the library used to implement the digital system in mind, as it was the only one available. The transistors used by the library are of minimal length and of the SLVT type, both being reasons for high power consumption. To then reduce the power consumption, a library with longer transistors can be used. Alternatively, a library with transistor types that have higher V_{Th} like the UHVT transistors could be used to reduce the power consumption.

4.7 Power gating of the unity gain amplifiers

The UG amplifiers have a large contribution to the system's power consumption as illustrated in Figure 3.2. The overall power consumption of the analog system can be reduced by power gating the UG amplifiers. By doing this, a possible reduction of more than 50% can be achieved in the analog system's powered-down state. The power consumption during conversion can also be reduced by utilizing power gating. This can be achieved by removing the TR gates and the pull-up and pull-down transistors from the UG amplifiers. Instead, power gating can be used to turn on and off the UG amplifiers during conversion.

4.8 Pre-charging of V_{TRI}

Power is being wasted while V_{TRI} is being pre-charged by UG3. This is due to V_{TRI} also being either charged or discharged through one of the MUXs while being pre-charged. This is because the triangular relaxation oscillator only has two states while powered on, charge and discharge. Because of this, UG3 has to keep pre-charging V_{TRI}, preventing it from starting the triangular oscillations. A third state can be implemented in the triangular relaxation oscillator to reduce the time spent pre-charging V_{TRI}. In this third state, neither of the MUXs should be configured to charge or discharge V_{TRI}. The triangular relaxation oscillator would exit the third state after the analog system has started up fully. This would make UG3 the only contributor to the voltage of V_{TRI} during pre-charge. Thus, reducing the time and power spent pre-charging V_{TRI}. This would also allow for UG3 to be powered down earlier during conversion, which would also save power.

Chapter 5

Future work

To compete with state-of-the-art sensors, future power-saving measures should be implemented. There are several things that can be considered as previously discussed. First, another library with either longer transistors or transistors of higher V_{Th} should be used to implement the digital system. Second, power gating of the UG amplifiers should be implemented. Lastly, the pre-charge period of V_{TRI} should be shortened down. The pre-charge period of V_{TRI} could be reduced by implementing a new state in the triangular relaxation oscillator. In this state, V_{TRI} is not being charged or discharged at the same time as it is being pre-charged.

There is room to improve the inaccuracy of the proposed sensor implementation by remedying the offset on V_{TRI}. By doing this, the sensor could achieve inaccuracies closer to that of higher technology nodes. Additionally, the sensor would follow Equation (2.9) more closely, which is the equation that describes the system. This would be beneficial for both one- and two-point calibrations.

Dynamic element matching is a viable method to achieve a better performance closer to state-of-the-art. The bias and reference circuit and triangular relaxation oscillator are possible circuits that could benefit from this method. This would further improve system performance as in [13]. Dynamic element matching would average mismatch errors and improve the performance of the system.

The temperature sensor implementation should be taped-out for practical measurements. Before this can be done, the layout of the digital system must first be made DRC clean. This is because the layout of the digital system in this work was an initial draft that was not DRC clean.

Chapter 6

Conclusion

This work has successfully implemented a temperature sensor layout in the 22 nm Fully Depleted Silicon-On-Insulator (FD-SOI) technology by GlobalFoundries (GF). This work is a continuation of the previous project work by us [1], based on the 65 nm bulk Complementary Metal–Oxide–Semiconductor (CMOS) temperature sensor in [2]. The proposed temperature sensor incorporates a digital system with a simple interface and outputs the measurements as converted digital values as opposed to a frequency. The layout of the temperature sensor implementation of this work occupies a small area of 9.8 kμm^2. It has a sensing range of -40 °C to 125 °C, which is the fully supported temperature range of the transistor models. The sensor operates according to specification with supply voltages in the range 0.72 V to 0.88 V, where 0.8 V is the typical operating voltage. A low average power consumption of 6.3 nW is achieved with a sampling rate of 10 Hz and a duty cycle of about 0.01%. The resulting energy per conversion is 630 pJ, about 2.6 times lower than in the project work. An approximate resolution of 0.5 °C is achieved with a sampling clock of 128 MHz and a conversion time of under 10 μs. Due to the flexibility of the system, a lower resolution can be achieved by using a higher sampling clock or a longer conversion time. A Resolution Figure of Merit (R-FoM) of 3.3 $pJ \cdot K^2$ was achieved with a 128 MHz clock and a resolution of 0.048 °C. One conversion with this resolution used 1448 pJ and could be accomplished within a conversion time of 55.4 μs.

The proposed sensor in this work fulfills the specifications in the scope for both one- and two-point calibration, achieving an inaccuracy within ±2%. This is achieved with a conversion time of 9.6 μs and a sampling clock of 128 MHz. The relative inaccuracy of the sensor is 1.87 % for two-point and 2.18 % for one-point calibration. The inaccuracy has a peak-to-peak error of -2 ∼1.1 °C for two-point and -2.4 ∼2.2 °C for one-point calibration. The sensor exhibits a 3σ of 1.71 °C due to mismatch in the range -40 °C to 125 °C. While noise-induced error to the system has a standard deviation of 2.06 °C at 27 °C and 2.41 °C at 125 °C.

The proposed work features a redesigned comparator, improving overall system performance. Power-up circuits have been added, and existing power-up circuits have been improved to lower leakage and reduce power consumption in

the off-state. The proposed temperature sensor has been implemented in layout, and it has been verified in post-layout simulations. The properties of the FD-SOI technology has been utilized to employ back-gate switching in Transmission (TR) gates and Multiplexers (MUX). The same properties are utilized to employ back-gate biasing. One key circuit in which back-gate biasing is utilized is in the bias and reference to generate a Differential Bandgap Reference (DBGR). This is opposed to using transistors of different flavors as in the paper that the project work was based on [2].

Bibliography

[1] J. S. Ege and S. H. Egge, 'Temperature-to-frequency converter in 22 nm fd-soi with a sensing range of -40 °c to 125 °c operating at 0.8 v,' Specialization project, Dec. 2022.

[2] H. Shi, B. Zhou and F. Zhao, 'A high-linear low-power temperature-to-frequency converter with high robustness,' in *2019 IEEE 3rd Advanced Information Management, Communicates, Electronic and Automation Control Conference (IMCEC)*, 2019, pp. 828–831. DOI: 10.1109/IMCEC46724.2019.8984114.

[3] C.-F. Chiang, A. B. Graham, B. J. Lee, C. H. Ahn, E. J. Ng, G. J. O'Brien and T. W. Kenny, 'Resonant pressure sensor with on-chip temperature and strain sensors for error correction,' in *2013 IEEE 26th International Conference on Micro Electro Mechanical Systems (MEMS)*, 2013, pp. 45–48. DOI: 10.1109/MEMSYS.2013.6474172.

[4] A. A. Silverio, 'Design of a wide temperature range, high linearity time domain cmos-based temperature sensor for wearable iot applications,' in *2021 2nd International Conference on Innovative and Creative Information Technology (ICITech)*, 2021, pp. 226–230. DOI: 10.1109/ICITech50181.2021.9590119.

[5] S. Lu, D. Wu and L. Wu, 'Design of a highly compact on-chip temperature sensor with ultra-low power based on 40nm cmos,' in *2022 IEEE 16th International Conference on Solid-State & Integrated Circuit Technology (ICSICT)*, 2022, pp. 1–3. DOI: 10.1109/ICSICT55466.2022.9963407.

[6] T. duc Chung and R. B. Ibrahim, 'Building ambient temperature measurement using industrial wireless mesh technology,' in *2019 IEEE Student Conference on Research and Development (SCOReD)*, 2019, pp. 146–151. DOI: 10.1109/SCORED.2019.8896316.

[7] M. K. Law and A. Bermak, 'A 405-nw cmos temperature sensor based on linear mos operation,' *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 56, no. 12, pp. 891–895, 2009. DOI: 10.1109/TCSII.2009.2034201.

[8] Dominik Przyborowski, *Matching of transistors in 22 nm FD-SOI*, Personal communication, Analog IC Designer at Nordic Semiconductor ASA, 2022.

[9] K.A.A. Makinwa. 'Smart temperature sensor survey.' (16th May 2023), [Online]. Available: http://ei.ewi.tudelft.nl/docs/TSensor_survey.xls (visited on 25/08/2022).

[10] Y. Lempel, R. Breuer and J. Shor, 'A 700-μm^2, ring-oscillator-based thermal sensor in 16-nm finfet,' *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 30, no. 2, pp. 248–252, 2022. DOI: 10.1109/TVLSI.2021.3137338.

[11] Y. Kim, W. Choi, J. Kim, S. Lee, S. Lee, H. Kim, K. A. A. Makinwa, Y. Chae and T. W. Kim, 'A 0.02mm2 embedded temperature sensor with ±2°c inaccuracy for self-refresh control in 25nm mobile dram,' in *ESSCIRC Conference 2015 - 41st European Solid-State Circuits Conference (ESSCIRC)*, 2015, pp. 267–270. DOI: 10.1109/ESSCIRC.2015.7313878.

[12] S. Park, Y. Kim, W. Choi, Y. Lee, S. Kim, Y. Shin and Y. Chae, 'A dtmost-based temperature sensor with 3σ inaccuracy of ±0.9°c for self-refresh control in 28nm mobile dram,' in *2020 IEEE Custom Integrated Circuits Conference (CICC)*, 2020, pp. 1–4. DOI: 10.1109/CICC48029.2020.9075873.

[13] M. Pertijs, K. Makinwa and J. Huijsing, 'A cmos smart temperature sensor with a 3/spl sigma/ inaccuracy of /spl plusmn/0.1/spl deg/c from -55/spl deg/c to 125/spl deg/c,' *IEEE Journal of Solid-State Circuits*, vol. 40, no. 12, pp. 2805–2815, 2005. DOI: 10.1109/JSSC.2005.858476.

[14] B. Razavi, *Design of Analog CMOS Integrated Circuits*, 2nd ed. McGraw-Hill Education, Jan. 2017, ISBN: 9780072524932.

[15] R. J. Baker, *CMOS Circuit Design, Layout, and Simulation*, 3rd ed. John Wiley and Sons, Ltd, Aug. 2010, ISBN: 9780470891179. DOI: 10.1002/9780470891179.

[16] L. H. F. T. C. P. R. L. MORENO, 'An ultra-low-voltage ultra-low-power weak inversion composite mos transistor: Concept and applications,' *IEICE TRANSACTIONS on Electronics*, vol. E91-C, no. 4, pp.662–665, 2008. DOI: 10.1093/ietele/e91-c.4.662.

[17] anysilicon.com. 'The ultimate guide: Fdsoi.' (), [Online]. Available: https://anysilicon.com/fdsoi/ (visited on 03/12/2022).

[18] E. Hong, Mixel and N. Jedrzejewski. 'The ultimate guide: Fdsoi.' (21st Jan. 2021), [Online]. Available: https://www.eetimes.com/its-time-to-look-at-fd-soi-again/ (visited on 03/12/2022).

[19] STMicroelectronics. 'Fd-soi fully depleted silicon on insulator.' (), [Online]. Available: https://www.st.com/content/st_com/en/about/innovation---technology/FD-SOI.html (visited on 03/12/2022).

Appendix A

SystemVerilog

Code listing A.1: This is the full code from the file ANALOG2DIGITAL.sv.

```
1  //
       //////////////////////////////////////////////////////////////////////////////////
2  // Company:
3  // Engineer:
4  //
5  // Create Date: 05/21/2023 04:48:22 PM
6  // Design Name:
7  // Module Name: TEMPEST_ANALOG2DIGITAL
8  // Project Name:
9  // Target Devices:
10 // Tool Versions:
11 // Description:
12 //
13 // Dependencies:
14 //
15 // Revision:
16 // Revision 0.01 - File Created
17 // Additional Comments:
18 //
19 //
       //////////////////////////////////////////////////////////////////////////////////
20
21 module ANALOG2DIGITAL(
22     input VDD,
23     input VSS,
24     input bit EN,
25     input bit CLK,
26     input bit erase,
27     output bit [15:0] OUT           // Digital output
28     );
29
30     wire VNW_N, VPW_P;              // Needs to be here for synthesis
31
32     always_ff @(posedge CLK or posedge erase) begin
33         if(erase) begin
34             OUT = 0;
35         end else if (EN) begin
36             OUT = OUT + 1;
37         end
38     end
```

```
39 endmodule
```

Code listing A.2: This is the full code from the file CLOCK_DIVIDER.sv.

```
1  //////////////////////////////////////////////////////////////////////////////////
2  // Company:
3  // Engineer:
4  //
5  // Create Date: 05/21/2023 04:48:22 PM
6  // Design Name:
7  // Module Name: TEMPEST_CLOCK_DIVIDER
8  // Project Name:
9  // Target Devices:
10 // Tool Versions:
11 // Description:
12 //
13 // Dependencies:
14 //
15 // Revision:
16 // Revision 0.01 - File Created
17 // Additional Comments:
18 //
19 //////////////////////////////////////////////////////////////////////////////////
20
21 module CLOCK_DIVIDER(
22     input VDD,                      // Needs to be here for synthesis
23     input VSS,                      // Needs to be here for synthesis
24     input bit EN,                   // ENABLE the ClockDivider
25     input bit CLK,                  // The driving clock
26     output bit [1:0] OUT            // The output of the ClockDivider
27     );
28
29     wire VNW_N, VPW_P;              // Needs to be here for synthesis
30
31     always_ff @(posedge CLK) begin
32         if (EN) begin
33             OUT++;
34         end else begin
35             OUT = 0;
36         end
37     end
38 endmodule
```

Code listing A.3: This is the full code from the file FSM.sv.

```
1  //////////////////////////////////////////////////////////////////////////////////
2  // Company:
3  // Engineer:
4  //
5  // Create Date: 05/21/2023 04:48:22 PM
6  // Design Name:
7  // Module Name: FSM
8  // Project Name:
9  // Target Devices:
10 // Tool Versions:
11 // Description:
```

```
12 //
13 // Dependencies:
14 //
15 // Revision:
16 // Revision 0.01 - File Created
17 // Additional Comments:
18 //
19 //////////////////////////////////////////////////////////////////////////////////


20
21
22 module FSM #(
23     //-----------------------------------------------------------
24     // State duration in clock cycles
25     //-----------------------------------------------------------
26     parameter  c_erase         = 1,
27     parameter  c_startup       = 2,
28     parameter  c_comp_on       = 5,
29     parameter  c_sc_on         = 2,
30     parameter  c_startup_done  = 19
31     )(
32     input VDD,                          // Needs to be here for synthesis
33     input VSS,                          // Needs to be here for synthesis
34     input bit EN,                       // ENABLE the FSM
35     input bit CLK,                      // The driving clock
36     input bit SAMPLE,                   // A trigger signal which sets the FSM in
           motion.
37     input bit DONE,                     // Measurement finished
38     output bit idle,                    // output state signal
39     output bit erase,                   // output state signal
40     output bit power_up,                // output state signal
41     output bit comp_control,            // output state signal
42     output bit startup_sc,              // output state signal
43     output bit set_tri                  // output state signal
44     );
45
46     //-----------------------------------------------------------
47     // State Machine
48     //-----------------------------------------------------------
49     enum bit [2:0] {IDLE, ERASE, STARTUP, SET_TRI, COMP_CTRL, MEASURE} state;
50
51     wire VNW_N, VPW_P;                  // Needs to be here for synthesis
52
53     bit [9:0]          state_counter;
54     bit DONE_DETECTED;
55
56     always @(state or DONE or EN) begin
57         if(~EN) begin
58             DONE_DETECTED = 0;
59         end else begin
60             case(state)
61                 IDLE: begin
62                     DONE_DETECTED = 0;
63                 end
64                 MEASURE: begin
65                     if(DONE) begin
66                         DONE_DETECTED = 1;
67                     end
68                 end
69             endcase
70         end
71     end
```

```
72
73      always @(state or DONE_DETECTED) begin
74          if(DONE_DETECTED) begin
75              idle         = 1;
76              erase        = 0;
77              power_up     = 0;
78              comp_control = 0;
79              startup_sc   = 0;
80              set_tri      = 0;
81          end else begin
82              case(state)
83                  IDLE: begin
84                      idle         = 1;
85                      erase        = 0;
86                      power_up     = 0;
87                      comp_control = 0;
88                      startup_sc   = 0;
89                      set_tri      = 0;
90                  end
91                  ERASE: begin
92                      idle         = 0;
93                      erase        = 1;
94                      power_up     = 1;
95                      comp_control = 0;
96                      startup_sc   = 0;
97                      set_tri      = 0;
98                  end
99                  STARTUP: begin
100                     idle         = 0;
101                     erase        = 0;
102                     power_up     = 1;
103                     comp_control = 0;
104                     startup_sc   = 1;
105                     set_tri      = 1;
106                 end
107                 SET_TRI: begin
108                     idle         = 0;
109                     erase        = 0;
110                     power_up     = 1;
111                     comp_control = 0;
112                     startup_sc   = 0;
113                     set_tri      = 1;
114                 end
115                 COMP_CTRL: begin
116                     idle         = 0;
117                     erase        = 0;
118                     power_up     = 1;
119                     comp_control = 1;
120                     startup_sc   = 0;
121                     set_tri      = 1;
122                 end
123                 MEASURE: begin
124                     idle         = 0;
125                     erase        = 0;
126                     power_up     = 1;
127                     comp_control = 1;
128                     startup_sc   = 0;
129                     set_tri      = 0;
130                 end
131             endcase
132         end
133     end
134
```

```
135
136     // Control the state transitions.
137      always_ff @(posedge CLK or negedge EN) begin
138          if(~EN) begin
139              state = IDLE;
140              state_counter  = 0;
141          end else begin
142              case (state)
143                  IDLE: begin                                    // Do not do
                         anything.
144                      if(SAMPLE) begin
145                          state = ERASE;
146                          state_counter  = 0;
147                      end
148                  end
149                  ERASE: begin                                   // Reset / Prepare
                         the digital logic for a new sample.
150                      state_counter = state_counter + 1;
151                      if(state_counter == c_erase) begin
152                          state = STARTUP;
153                          state_counter  = 0;
154                      end
155
156                  end
157                  STARTUP: begin                                 // General startup.
                         Power up goes high, and VCTAT and VPTAT in TRI_GEN is pre-
                         charged.
158                      state_counter = state_counter + 1;
159                      if(state_counter == c_startup) begin
160                          state = SET_TRI;
161                          state_counter  = 0;
162                      end
163                  end
164                  SET_TRI: begin                                 // Pre-charge V_TRI
165                      state_counter = state_counter + 1;
166                      if(state_counter == c_comp_on) begin
167                          state = COMP_CTRL;
168                          state_counter  = 0;
169                      end
170                  end
171                  COMP_CTRL: begin                               // Allow the
                         comparator to control the signal CTRL
172                      state_counter = state_counter + 1;
173                      if(state_counter == c_sc_on) begin
174                          state = MEASURE;
175                          state_counter  = 0;
176                      end
177                  end
178                  MEASURE: begin                                 // Performing
                         temperature measurement
179                      if(DONE_DETECTED) begin
180                          state = IDLE;
181                      end
182                  end
183                  default: begin
184                      state = IDLE;                              // Go into IDLE if
                             the state is not recognised/defined
185                  end
186              endcase
187          end
188      end
189  endmodule
```

Code listing A.4: This is the full code from the file PULSE_COUNTER.sv.

```
//
    //////////////////////////////////////////////////////////////////////////////////
// Company:
// Engineer:
//
// Create Date: 05/21/2023 04:48:22 PM
// Design Name:
// Module Name: TEMPEST_PULSE_COUNTER
// Project Name:
// Target Devices:
// Tool Versions:
// Description:
//
// Dependencies:
//
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
//
//
    //////////////////////////////////////////////////////////////////////////////////

module PULSE_COUNTER (
    input VDD,                      // Needs to be here for synthesis
    input VSS,                      // Needs to be here for synthesis
    input bit EN,                   // Enable the pulseCounter
    input bit IN,                   // Input signal whos pulses will be counted
    input bit continuous,
    input bit [15:0] countTarget,
    output bit [15:0] pulseCount,
    output bit firstPulse,
    output bit match                // The target count value has been reached
    );

    wire VNW_N, VPW_P;              // Needs to be here for synthesis

    always_ff @(negedge IN or negedge EN) begin
        if(~EN) begin
            pulseCount = 0;
            firstPulse = 0;
            match = 0;
        end else if (EN) begin
            if(!continuous) begin
                if (firstPulse == 0) begin
                    firstPulse = 1;
                end else begin
                    pulseCount = pulseCount + 1;
                    if (pulseCount == countTarget) begin
                        match = 1;
                    end
                end
            end
        end
    end

    /*always_ff @(negedge IN or negedge EN) begin
        if(~EN) begin
            match = 0;
        end else if (pulseCount == countTarget) begin
```

```
58                  match = 1;
59              end
60          end*/
61  endmodule
```

Appendix B

Test results

Table B.1: Post layout corner simulation results of temperature and line regulation performances of reference voltage V_{BG}.

Corner	V_{BG}@27°C (mV)	ΔV_{BG} (mV)	ppm/°C	%/V
tt	470.32	1.73	31.97	2.39
ff	456.20	3.22	42.78	2.47
fs	452.34	1.72	68.11	2.53
sf	488.32	1.79	30.87	2.25
ss	484.98	3.14	51.64	2.23

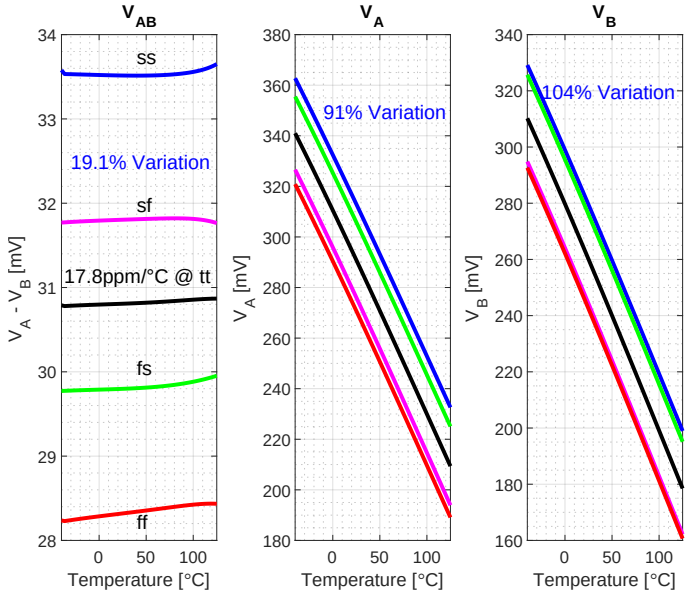


Figure B.1: Post layout simulation of temperature performances for the reference voltages: single-ended vs. differential

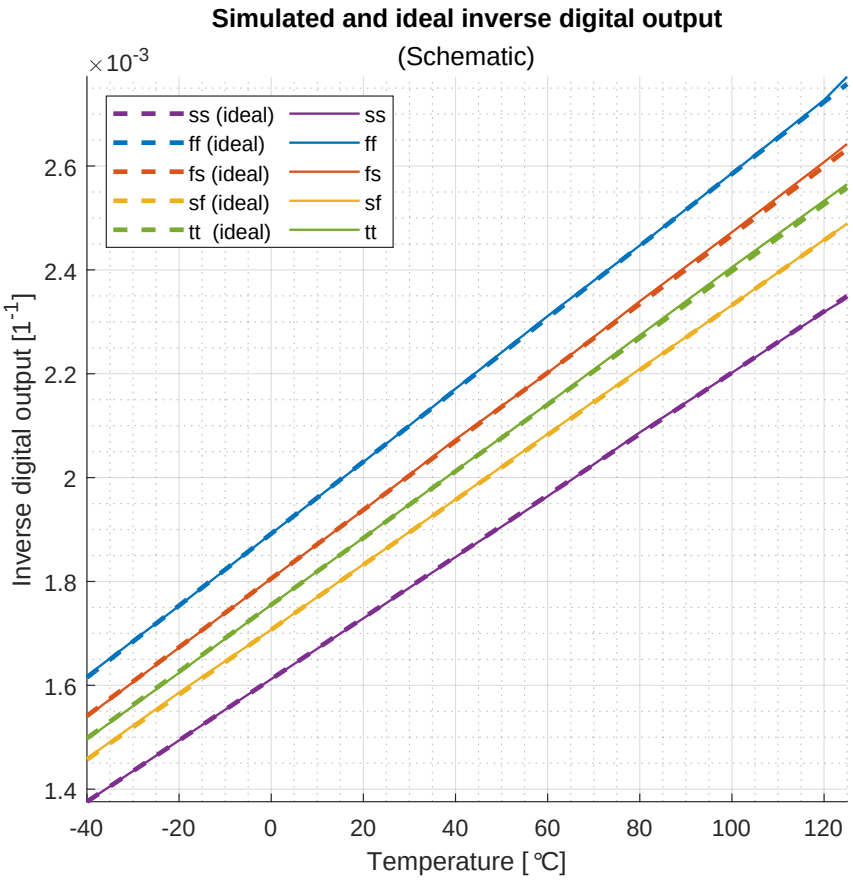


Figure B.2: Comparison between the ideal and simulated digital output for schematic.

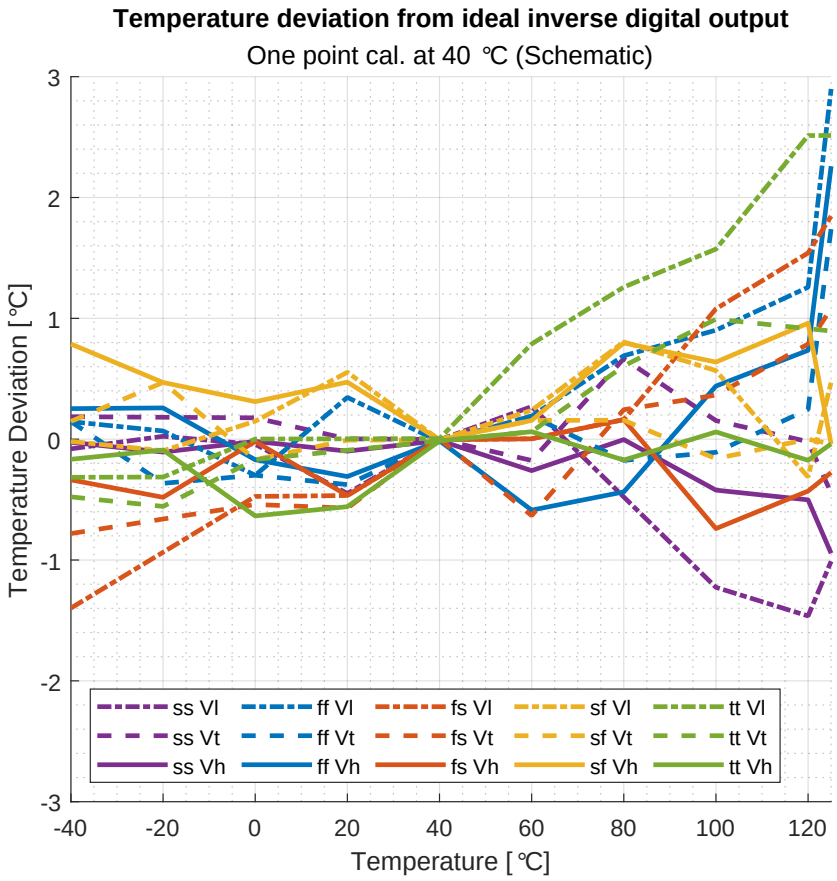


Figure B.3: Deviation between the simulated and ideal output for schematic after 1 point calibration at 40 °C.

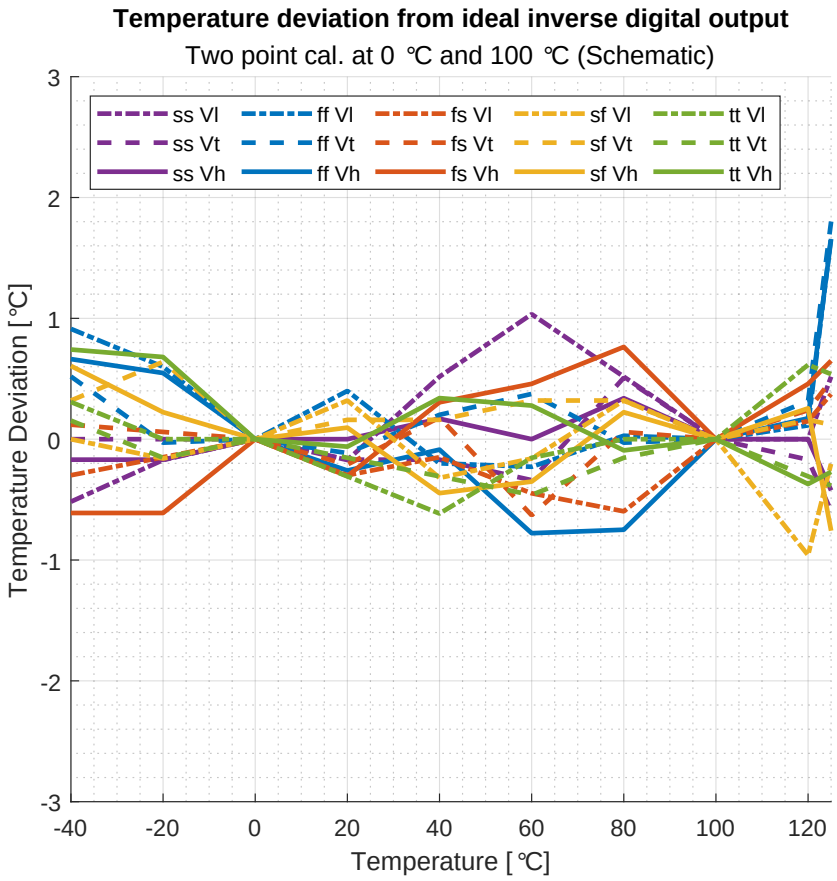


Figure B.4: Deviation between the simulated and ideal output for schematic after a two-point calibration.

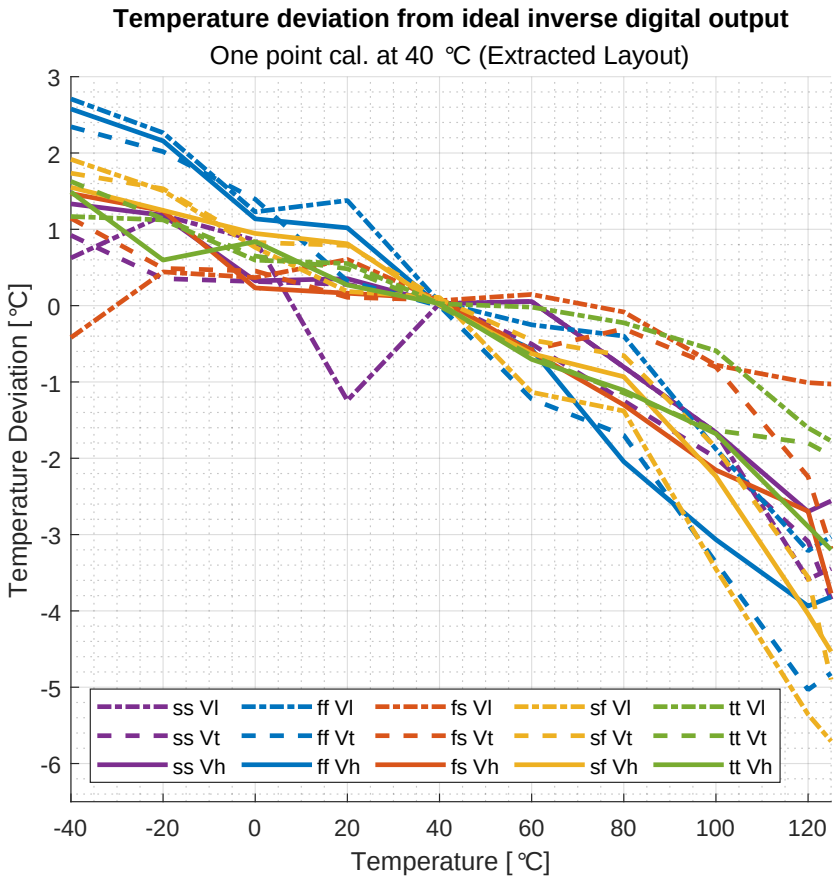


Figure B.5: Deviation between the simulated and ideal output for extracted layout after 1 point calibration at 40 °C.

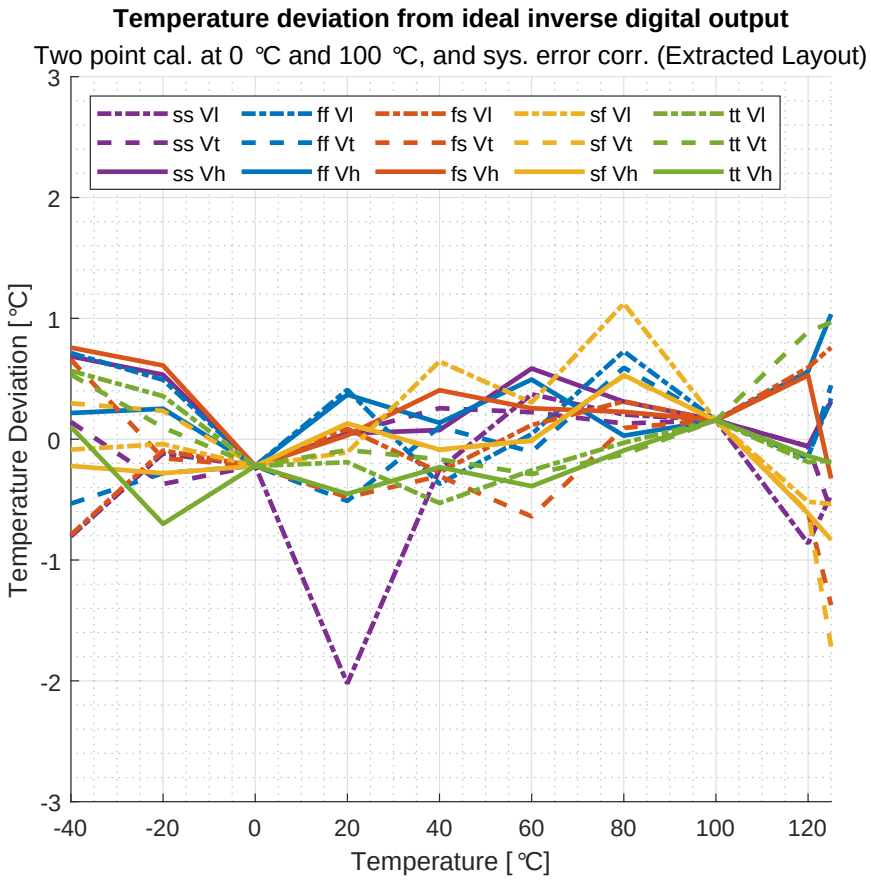


Figure B.6: Deviation between the simulated and ideal output for extracted layout after a two-point calibration at 0 °C and 100 °C with systematic error correction.

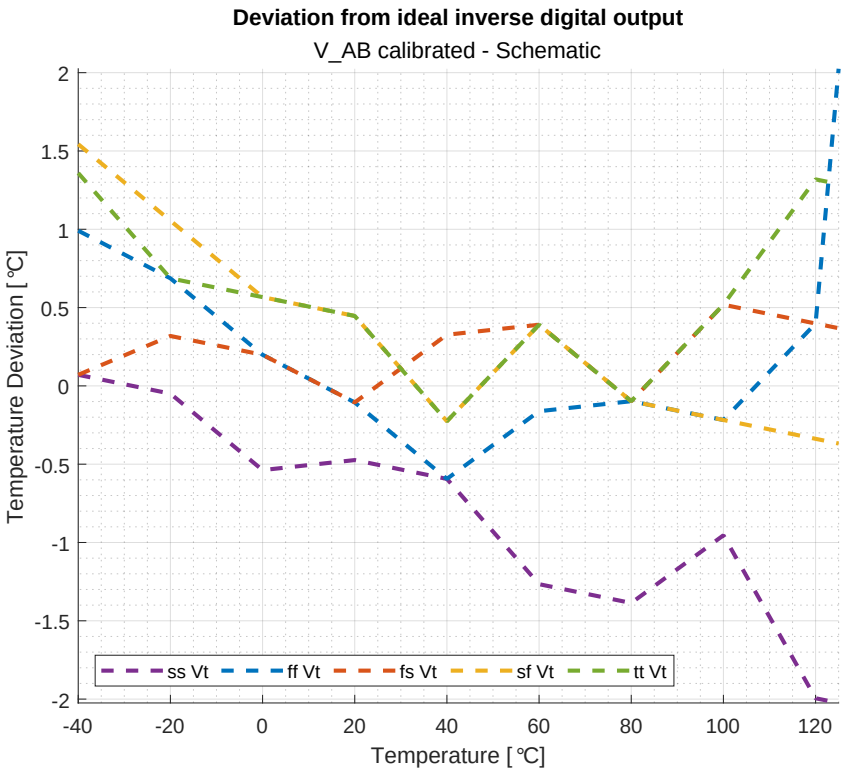


Figure B.7: Deviation between the simulated and ideal output for schematic after calibrating V_{AB}. Calibrated using an ideal 8-bit resistor network.

Appendix C

Beta-multiplier

This appendix is an extract of section 2.2 from the theory chapter in [1].

A beta-multiplier such as the one shown in Figure C.1, is a circuit that can be used as a supply-independent bias current circuit, constant-Gm bias circuit [14], as well as a PTAT current generator. To generate a constant current or Gm using this circuit, all transistors must be operated in strong-inversion and saturation ($V_{GS} > V_{TH}$ & $V_{DS} \geq V_{GS}$ - V_{TH}). On the other hand, if transistors M1 and M2 are operated in sub-threshold and saturation ($V_{GS} < V_{TH}$ & $V_{DS} > 3V_T$), a current that is PTAT will be generated. The existence of degenerate bias points in supply-independent circuits such as the beta-multiplier requires the use of a start-up circuit. The start-up circuit ensures that the circuit starts up at all and speeds up the start-up process [14].

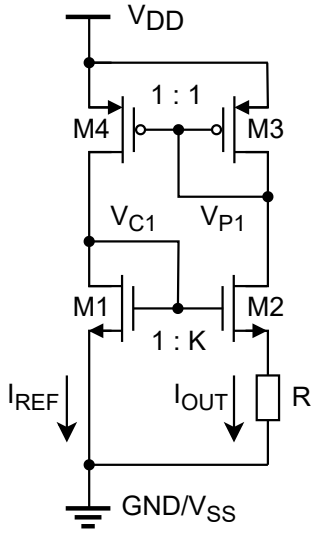


Figure C.1: A circuit diagram of a beta-multiplier based on [15, p. 624, fig. 20.14] and [14, p. 510, fig 12.3].

In [15], a transconductance parameter for NMOS is defined by Equation (C.1), which is further used to define another transconductance parameter in Equation (C.2). The transconductance parameter β is the basis for the name of the beta-multiplier. We can see that the width of M2 being K times larger than the width of M1 results in β_2 being K times larger than β_1.

$$KP_n = \mu_n \cdot C'_{ox} = \mu_n \cdot \varepsilon_{ox}/t_{ox} \tag{C.1}$$

$$\beta = KP_n \cdot W/L \tag{C.2}$$

The PMOS current mirror in the beta-multiplier is used to make the current through M2 equal to the current through M1. To achieve this successfully, β_2, or W_2, of M2 is made K times larger than β_1 such that M2 can conduct I_{REF} with less gate-source voltage than M1. This is necessary due to the resistor at the source of M2 [15].

The beta-multiplier is used to generate a PTAT current in the temperature sensor implementation written about in this report. Thus, how this current is generated will be looked into more closely here. Firstly, the drain current in sub-threshold given in Equation (C.3) must be considered as the transistors M1 and M2 are both operated in sub-threshold and saturation.

$$I_D = \frac{W}{L} \cdot I_{D0} \cdot e^{\frac{V_{GS}-V_{TH}}{\eta \cdot V_T}} \cdot \left(1 - e^{\frac{-V_{DS}}{V_T}}\right) \tag{C.3}$$

Where I_{D0} is given by Equation (C.4).

$$I_{D0} = \mu_n \cdot C_{ox} \cdot (\eta - 1) \cdot V_T^2 \tag{C.4}$$

And, the thermal voltage, V_T, is given by Equation (C.5). Here k_B is Boltzmann constant, and q is the magnitude of the electric charge of a single electron. T is the temperature in Kelvin.

$$V_T = \frac{k_B \cdot T}{q} \tag{C.5}$$

The last term in Equation (C.3) can be approximated to 1 when $V_{DS} > 3V_T$, and can thus be simplified and written as in Equation (C.6).

$$I_D = \frac{W}{L} \cdot I_{D0} \cdot e^{\frac{V_{GS}-V_{TH}}{\eta \cdot V_T}} \tag{C.6}$$

The voltage V_R across R in Figure C.1 can be expressed as in Equation (C.7).

$$V_R = V_{GS1} - V_{GS2} \tag{C.7}$$

The gate-source voltages in Equation (C.7) can be derived from the expression in Equation (C.6).

$$V_{GS1} = \eta \cdot V_T \cdot ln\left(\frac{I_{D1}}{I_{D0} \cdot \left(\frac{W}{L}\right)_1}\right) + V_{TH1} \tag{C.8}$$

$$V_{GS2} = \eta \cdot V_T \cdot ln\left(\frac{I_{D2}}{I_{D0} \cdot \left(\frac{W}{L}\right)_2}\right) + V'_{TH2} \tag{C.9}$$

Where V'_{TH2}, which accounts for the body effect of M2 [16, eq. (2)], is given by Equation (C.10).

$$V'_{TH2} = V_{TH2} + (\eta - 1) \cdot V_{SB} = V_{TH2} + (\eta - 1) \cdot V_R \tag{C.10}$$

Assuming that $V_{TH1} = V_{TH2}$, V_R can be derived by substituting Equation (C.8) and Equation (C.9) into Equation (C.7).

$$V_R = I_{REF} \cdot R = V_T \cdot ln\frac{(W/L)_2}{(W/L)_1} \tag{C.11}$$

And thus, I_{REF} can be written as in Equation (C.12). Where K is given by Equation (C.13). From Equation (C.12) it can be seen that I_{REF} is proportional to V_T which is proportional to temperature. Therefore, I_{REF} is PTAT as long as the resistance of R does not vary over temperature, or approximately PTAT if R is stable over temperature.

$$I_{REF} = \frac{V_T \cdot ln(K)}{R} \tag{C.12}$$

$$K = \frac{(W/L)_2}{(W/L)_1} = \frac{\beta_2}{\beta_1} \tag{C.13}$$

Appendix D

FD-SOI

This appendix is an extract of section 2.1 from the theory chapter in [1].

FD-SOI technology utilizes an isolating material called the Buried Oxide (BOX) to isolate the drain, source, and channel of the transistor from the bulk, as shown in Figure D.1. Some benefits of using this technology will be further described in this section.

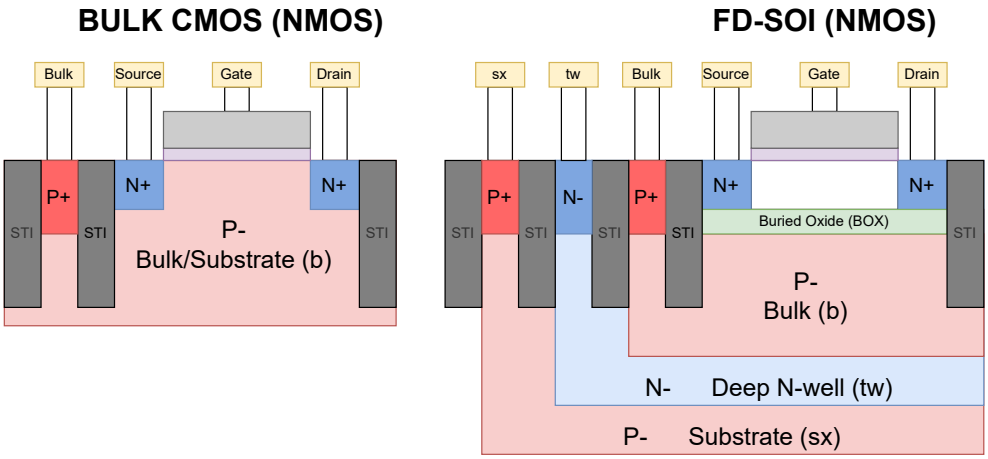


Figure D.1: A sketch illustrating how FD-SOI differs from BULK CMOS with an NMOS as an example.

One benefit of this as opposed to regular bulk CMOS technology is that the leakage from the drain, source, and channel, to the bulk, is reduced greatly. Another is that the channel can be undoped, which is referred to as being fully depleted. This means that variations in transistor characteristics that otherwise would arise due to varying doping across the chip can be eliminated. The channel can still be doped if desired to achieve a higher or lower threshold voltage. This would result in doping variations leading to a higher degree of mismatch between the doped transistors compared to the undoped transistors. Body biasing in bulk

CMOS is limited as opposed to FD-SOI where the bulk may be used as a gate and is often referred to as a back-gate or buried gate [17][18] [19].