A quasi-offline condition monitoring method of DC-link capacitor banks in accelerator power converters

Timm Felix Baumann[1, 2], Konstantinos Papastergiou[2], Raul Murillo Garcia[2], Dimosthenis Peftitsis[1]
[1]DEPARTMENT OF ELECTRIC POWER ENGINEERING NTNU - NORWEGIAN UNIVERSITY OF SCIENCE AND TECHNOLOGY
[2]CERN - EUROPEAN ORGANIZATION FOR NUCLEAR RESEARCH
[1]Gløshaugen, Trondheim, Norway
[2]Esplanade des Particules 1, Geneva, Switzerland
E-mail: timm.felix.baumann@cern.ch

Keywords

« DC-link », « Capacitors », « Condition Monitoring », « Data analysis », « Accelerators »

Abstract

This paper proposes a condition monitoring scheme for DC-link electrolytic capacitors used in regenerative medium power converters. The monitoring scheme is based on capacitor bank voltage measurements in quasi-offline mode. The aim of this work is to identify the voltage measurement precision and sampling requirements to enable a reproducible and reliable capacitance calculation. The proposed method is analysed theoretically and supported by simulation results and validated experimentally.

1. Introduction

In large-scale power converter farms a key objective is the reliable operation that is achieved with an optimum maintenance schedule. A common way to enhance reliability and expand their lifespan is by derating the converters' operation at a lower power in order to reduce the anticipated electrothermal stress for the components. One of the converter's components that is sensitive to aging is the DC-link capacitor [1]. Capacitors exhibit degradation effects during normal usage, which are usually caused by the degradation of the dielectric material. Degradation of the dielectric is pronounced with capacitors in cycling applications due to the internal heating of terminals and the higher RMS current. This results in lower capacitance, higher leakage current and an increased series impedance. Considering the operating constraints of the converter, these degradation effects might be tolerated within an acceptable range. However, a significant degree of degradation deteriorates the performance of the converter, in terms of voltage and current ripple and increased power losses.

Therefore, a condition monitoring (CM) scheme is valuable for assessing the health condition of the capacitors and for determining maintenance and replacement intervals before degradation reaches a critical level or failure of the component.

The operation of condition monitoring systems is based on data acquisition and offline data processing. There are different methods to acquire these data. The most straightforward way is to measure these data using sensing circuits. However, such circuits are cost intensive and can be a further source of failure, whereas they can -in the worst case- decrease the reliability of the application. A way to overcome this challenge, is to utilize data which are already measured for control purposes of the power converter, or to just model and simulate the degradation under the given load profile. Nevertheless, the second approach necessitates the development of accurate electrothermal models by also considering the accurate modelling of various materials comprising the physical components. Such models are based on a large amount of experimental data acquired under a large variety of operating conditions that usually require long testing procedures, unless field-data on failures are available [2].

There are three different data acquisition methods for CM as shown in Fig. 1. These methods are classified based on whether they require online or offline measurements. Online measurements refer to data acquired during the normal operation of the power converter, and while the measurement circuit does not interfere with the converter's operation. Online measurements usually suffer from lower accuracy and must also be designed and executed in a way to have the lowest possible impact on the converter's operation. On the other hand, offline measurements require the converter or the components to be disconnected from the applications before performing CM measurements. Offline measurements are more accurate than the online method, but they are cost-intensive and require an interruption of the electrical energy conversion process. In addition to these methods, it is possible to perform CM measurements when the converter is not in operation but still connected with the source and load. This type of measurement is termed *quasi-offline* and they are utilized in the presented work [3].

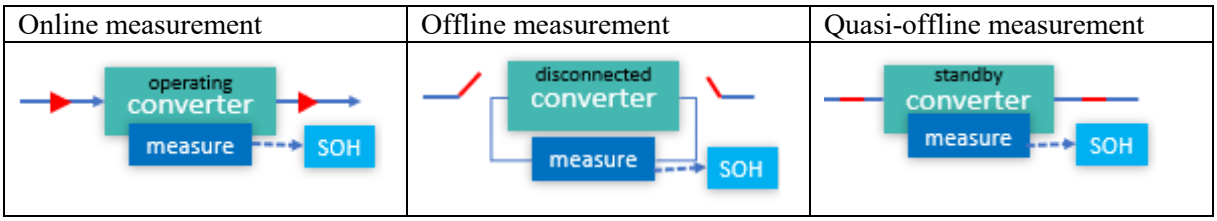


Fig. 1: Classification of CM methods.

Each of these four basic CM principles exhibits advantages, which depend on the specific application [3] , [4]. This study focuses on CM by using the existing sensors already incorporated on the power converters, making the measurements of type quasi-offline.

The performance indicators for electrolytic capacitors are mainly the values of the capacitance and the equivalent series resistance (ESR). This combination can also be described as a loss angle or dissipation factor and utilised as a CM parameter [5]. It is also possible to analyse the frequency dependence of the series impedance [6]. This can be done by assessing the switching harmonics during normal operation or by injecting signals superimposed with the modulation to get a specific frequency response [7]. However, for this application injecting superimposed signals is not tolerable because of the high precision output current control. Most of such online measurements require accurate voltage and current measurements in combination with a high sampling rate. Moreover, especially for existing converters, the remining processing and network capacity during operation is quite limited for doing online CM. Another possible method to determine the capacitance and ESR is to perform a discharge with a network of different switchable resistors, which can be realized as quasi-offline CM [8]. However, it should work without hardware changes.

This paper proposes a quasi-offline CM scheme for DC-link capacitors that can be implemented without the need for disconnecting the capacitors from the power converters. Moreover, the proposed scheme eliminates the need for external sensing circuits for monitoring the state of health (SOH) of capacitors, and it makes use of standard sensing circuits already implemented on the converters for their control.

More specifically, the capacitor's voltage decay is recorded each time the power converter is switched off by the accelerator operators. A low-tolerance and low-thermal drift discharge resistor, that is already connected in the converter's DC-link, is used for dissipating the energy. The voltage is recorded by the DC-link voltage measurement sensor and post-processed to identify the capacitors' SOH.

The paper is organized as follows. Section 2 introduces the design and operating principles of the accelerator converters at CERN. Then, Section 3 analyses the prospered CM system, including the mathematically background for optimal sampling intervals. The experimental validation of the CM scheme is presented in Section 4. Finally, the conclusions are summarized in Section 5.

2. Design and operating principles of power converters at CERN

Particle accelerators facilities employ hundreds of power converters for the steering of particle beams towards a particle storage ring, such as the Large Hadron Collider, or towards targets that create secondary particle beams for experiments, such as the CLOUD experiment. The power converters supply powerful electromagnets often in a cycling mode operating 24 hours a day and 7 days a week.

To control and monitor more than 5000 power converters at the European Laboratory of Particle Physics, their control hardware is connected to a technical network that gives access to significant diagnostic information. This includes state of various critical components as well as real time measurements from sensors inside the power converters. Eventually, the magnet current is recorded with a 10-kHz sampling rate by sensors offering a measurement accuracy in the order of 1 part per million (ppm).

One of the recent developments is the SIRIUS [9] power converter, that employs energy storage in electrolytic capacitors for recovering the magnet energy after each cycle. A simplified schematic of SIRIUS converters is depicted in Fig. 2.

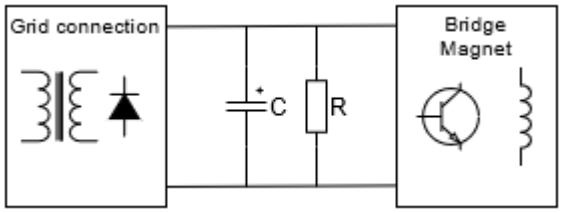


Fig. 2: Schematic diagram of the fundamental circuit of a SIRIUS accelerator converter [9]

Table I: Data of SIRUIS converter (one brick, basic configuration) [9]

SIRIUS key data	
Grid connection	3ph/400V/32A_{rms}
Output voltage	450V
Output current peak	450A
Output current RMS	200A

Electrolytic capacitors in SIRIUS are subject to more than 15 million cycles per year and, hence, a systematic monitoring is required as part of the preventive maintenance plan.

3. Proposed condition monitoring scheme for DC-link capacitors

In power converters a number of measurements such as the DC-link voltage, input and output currents are used for control and regulation while other signals such as the state of switchgear and thermal switches are used for the safety of the equipment [10]. In the majority of the present systems, failures of individual components will shut down the system immediately. On the contrary, a CM can predict the SOH of the components allowing the converter operators to schedule the replacement or maintenance of the components before a failure occurs.

Usually, discharging resistors are connected to DC-link capacitors enabling a safe way to dissipate their stored energy when a converter's shut-down is requested. It is important that these capacitors are discharged for safety and maintenance reasons within a certain time interval. In the simplest case there is a parallel-connected resistor that enables the discharging process within a few minutes. The capacitors are connected in series (e.g., C_1, C_2 in Fig. 3) to reach higher operating voltages. Due to manufacturing tolerances (i.e., capacitance and leakage current variations), balancing resistors (R_{B1}, R_{B2} in Fig. 3) are required across each series-connected capacitor to balance the steady-state voltages and avoid voltage drifts. These balancing resistors have the same effect as the discharging resistor. Fig. 3 shows an example of a capacitor bank with the already analysed discharging ohmic paths. The leakage current of the capacitors is modelled as parallel-connected resistors, R_{L1} and R_{L2}

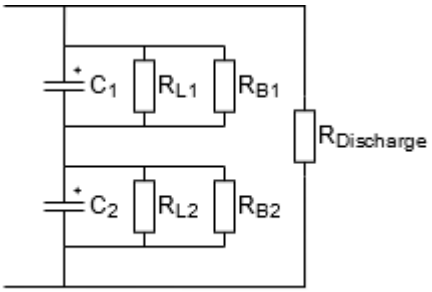


Fig. 3: Schematic diagram of a typical capacitor bank with the discharging resistors.

Using the discharging process of the DC-link capacitors after shutting down the converter is an ideal condition for conducting measurements. Since the power semiconductor devices are not switching, such measurements will not be impacted by electromagnetic noise. In this case the capacitor bank is only discharged through the discharging resistor, balancing resistors, and leakage current paths.

The discharging process follows the well-known Equation 1 for resistive discharging of a capacitor:

$$V_c(t) = V_0 \cdot e^{\frac{-t}{\tau}};\ \tau = R \cdot C \tag{1}$$

This equation expresses the capacitor voltage V_C as a function of the initial voltage V_0 at $t=0$ and the time constant τ. V_0 refers to the voltage of the capacitor bank when the converter shuts down. The time constant τ is a function of the discharging resistance R and capacitance C, where R is the resulting resistance of all ohmic paths (discharge, balance, and leakage current modelled as resistor) of the bank and C is the resulting capacitance of all capacitors.

The values of the discharging and balancing resistors do not change significantly due to degradation, but the leakage current modelled as further ohmic path will do. The decreasing capacitance and increasing leakage current will both cause a quicker discharge resulting in a shorter time constant τ. Thus, it makes sense to use the change of this time constant as a degradation indicator. The series impedance of the capacitor will increase due to degradation, but it will still be negligible in this slow discharging process, which usually takes several minutes.

The input to the proposed CM scheme is the recorded capacitor bank voltage. In principle, it is sufficient to measure the voltage at two different time instants during the discharging process and calculate the time constant τ by rearranging Equation 1 as shown in Equation 2, where (V_1, t_1) refers to the first sample and (V_2, t_2) refers to the second sample.

$$\tau = -\frac{t_2 - t_1}{ln(\frac{V_2}{V_1})} \tag{2}$$

Due to measurement inaccuracies and remining noise, it is is crucial to choose the time instants to acquire the voltage samples in a sophisticated way . Therefore, Equation 2 is analysed to study the impact of time and voltage accuracy. In order to find a general solution, it is possible to normalize the discharge in the voltage and time domain. This is done in time domain by defining $x = t/\tau$ and in amplitude domain by defining $y = V_c(t)/Vo$. By doing this, a general discharge according to Equation 3 can be found. Such a discharge is plotted in Fig. 4. This plot corresponds basically to τ=1s and Vo=1V.

$$y(x) = e^{-x},\ y = \frac{V_C}{V_0}, x = \frac{t}{\tau} \tag{3}$$

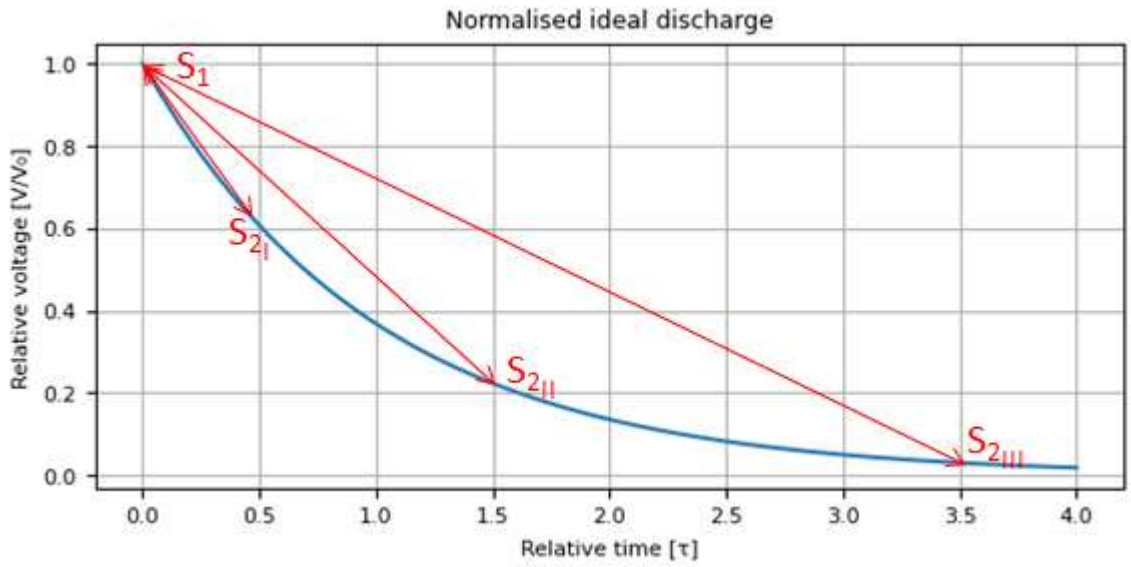


Fig. 4: Normalized discharge curve with sample pair suggestion.

Each sample has a timestamp, $t_{timestamp}$, with a limited time accuracy. Equation 4 shows the two different errors that might be contained in the timestamps of the sample point ($t_{samplepoint}$).

$$t_{timestamp} = (t_{samplepoint} + t_{shiftConstant} + t_{jitter}) \tag{4}$$

This additional time errors can be constant ($t_{shiftConstant}$) or random (t_{jitter}). Examples for such additional time errors are network latency, impact of pre-emptive multitasking systems and analogue digital conversion.

For the additive errors, they must be strictly distinguished between the constant part and the random part. Because of the time difference calculation, constant time shifts ($t_{shiftConstant}$) have no influence on accuracy of τ calculation. From Equation 5, it is shown that $t_{shiftConstant}$, which is equal for both sample points, disappears in the time difference calculation.

$$\begin{aligned} \Delta t &= t_2 - t_1 \\ &= (t_{2samplepoint} + t_{shiftConstant} + t_{2jitter}) - (t_{1samplepoint} + t_{shiftConstant} + t_{1jitter}) \\ &= t_{2samplepoint} - t_{1samplepoint} + t_{2jitter} + t_{1jitter} \\ &= t_{2samplepoint} - t_{1samplepoint} + t_{jitterResulting} \end{aligned} \tag{5}$$

Therefore time shifts of the system clock and constant dead-times in the processing chain are not relevant. The jitter of both sample times can be modulated as a resulting jitter. By taking a higher time difference, the influence of time jitter becomes less relevant.

The voltage measurement can be influenced by two error types. This is an additional error (V_{Err}) and a linear error ($Err_{Amplify}$) according to Equation 6. Additional errors are noise and offset from amplifiers in the circuit. Linear errors are due to resistor tolerances in voltage dividers or incorrect amplification factors.

$$V_{measured} = (V_{real} + V_{Err}) \cdot (1 - Err_{Amplify}) \tag{6}$$

For the τ calculation, only the relative relation of the two samples is relevant, because of the division of the two voltage samples (see Equation 6).

$$\frac{V_2}{V_1} = \frac{(V_{2real} + V_{2Err}) \cdot (1 - Err_{Amplify})}{(V_{1real} + V_{1Err}) \cdot (1 - Err_{Amplify})} = \frac{V_{2real} + V_{2Err}}{V_{1real} + V_{1Err}} \tag{7}$$

This means that only a linear representation of the voltage is required, and the linear error ($Err_{Amplify}$) has no impact on the operation of the CM scheme.

In Equation 8 the τ calculation formula with all relevant errors is presented and a relative error of τ can be calculated using Equation 9.

$$\tau_{withErr} = -\frac{(t_2 - t_1 + t_{jitter})}{ln(\frac{V_2 + V_{2Err}}{V_1 + V_{1Err}})} \tag{8}$$

$$Err_{\tau relative} = abs(\tau - \tau_{withErr}) \tag{9}$$

By filling in the errors in Equation 8 and calculate an absolute error according to Equation 9, an optimal time between two samples can be found in the normalised time and voltage domain (see Equation 3). The relative error on τ is defined according to Equation 10. To minimise the effect of noise on the voltage (V_1), the first sample is taken at the beginning of the discharging curve (x_1=0). With these simplifications (see Equation 11), the error function (Equation 12) is defined.

$$Err_{\tau relative} = abs\left(1 - \frac{-(x_2 - x_1 + x_{jitter})}{ln(\frac{V_{RelativIdeal}(x_2) + V_{2ErrRelaiv}}{V_{RelativIdeal}(x_1) + V_{1ErrRelativ}})}\right) \tag{10}$$

$$\mathrm{V_{RelativIdeal}}(\mathrm{x}) = e^{-\mathrm{x}}\ , x_1 = 0 \tag{11}$$

$$Err_{\tau relative}(x_2) = abs(1 + \frac{(x_2 + x_{jitter})}{ln(\frac{e^{-x_2} + V_{2ErrRelaive}}{1 + V_{1ErrRelative}})}) \tag{12}$$

Equation 12 is analysed numerically to assess the impact of the measurement errors and optimization potential. An example demonstrating the impact of the measurement errors by setting each error contribution to 1% as shown in Table II has been considered. The results of this analysis are plotted in Fig. 5.

Table II: Error calculating basic

$V_{1ErrRelaive}$	$V_{2ErrRelative}$	x_{ijtter}
-0.01	0.01	0.01

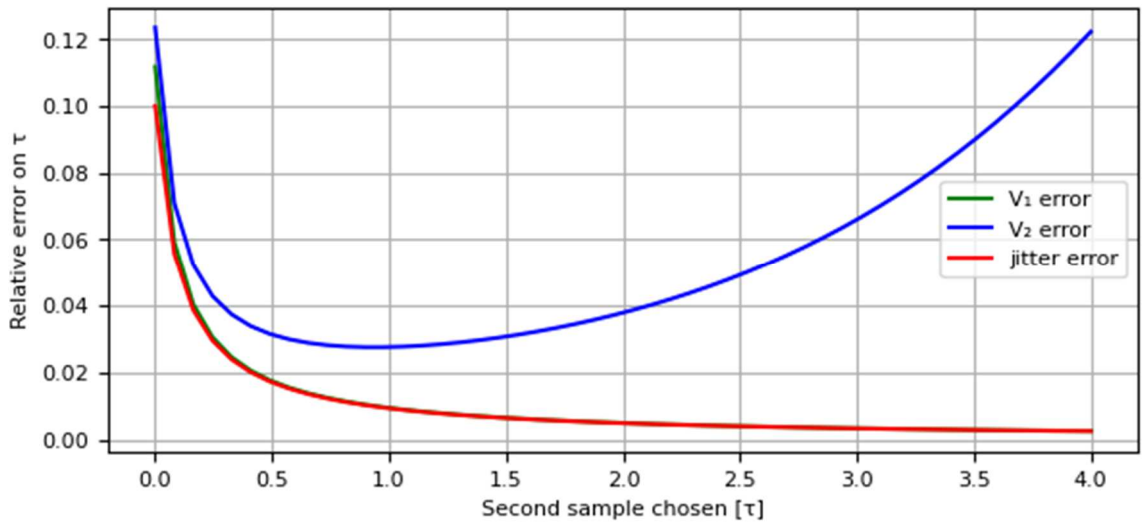


Fig. 5: Impact of the choice of the second time stamp on different errors

As shown in Fig. 5, the inaccuracy of V_1 and time jitter becomes less relevant for a delayed choice of sample 2. Most interesting is the impact of V_2 error. For this error the optimal sampling point is at τ. It should be noted that both voltage samples are sensed from the same sensor which means that they are impacted by the same noise level. In general, the superposition of the different errors cannot be calculated in a simple way. According to this calculation, it is found that $t_2 = \tau$ where the error on V_2 has a minimum impact and the other error contributions are still quite low. Of course, the exact τ value is unknown, but it can be approximated based on analytical calculations or by plotting a discharge record.

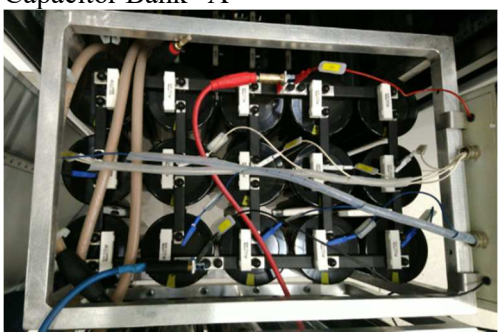
For further reduction of noise, it is possible to filter the signal and to consider the average values of different sampling pairs. To be robust against outliners, the median principle can improve monitoring. It is noted that the amount of noise is just an indicator for the quality of the measurement but has no impact on the assessment of the capacitors bank's SOH. However, low noise levels are required for detecting the slight changes of the time constant, which will indicate capacitors degradation.

4. Experimental validation

This section analyses experimentally the impact of optimal voltage sampling on the validation of the capacitance measurement. Fig. 6 shows photos of the experimental setup of the SIRIUS converter and the capacitor banks at CERN laboratory, which were used for performing the experimental evaluation of the proposed CM scheme. Two types of DC-link capacitor banks having slightly different characteristics have been used. To observe the difference in the time constant, measurements with two different capacitor banks (Bank "A" and Bank "B") were conducted. The circuit of the capacitor bank remains the same, but different capacitor types are used. Despite the same nominal data, the type "B" has a slightly higher typical capacitance values compared to type "A" counterparts.

SIRIUS converter

Capacitor Bank “A”



Capacitor Bank “B”

Fig. 6: Photos of the laboratory prototypes of SIRIUS converter and the two different capacitor banks

Optimal voltage sampling

When a converter is shut down or trips due to an internal or external fault, the data acquisition process starts. A voltage sample is collected every 30 s until the voltage reaches 20 V. Usually, the first sample has a lower voltage than the nominal direct voltage of 900 V, because the initialization of the recording is a bit delayed.

In optimal conditions, the value of τ should always be the same irrespective of the samples’ choice. Due to different types of noise and measurement errors, there are differences between the outcomes. As analysed in the previous section, the accuracy can increase by choosing the optimal time between two samples. For assessing this further, experimental data of a discharging process has been recorded and plotted in see Fig. 7. To study the impact of sample pair choices, two methods are compared. Method 1 calculates τ just by taking into account two adjacent samples. On the other hand, Method 2 takes the second sample with the optimal time distance. This optimal time distance is approximately 1τ later, which corresponds to 11 samples later in the analysed discharge. In Fig. 7 an example pair for Method 1 is marked in with a yellow arrow and for Method 2 with a green arrow.

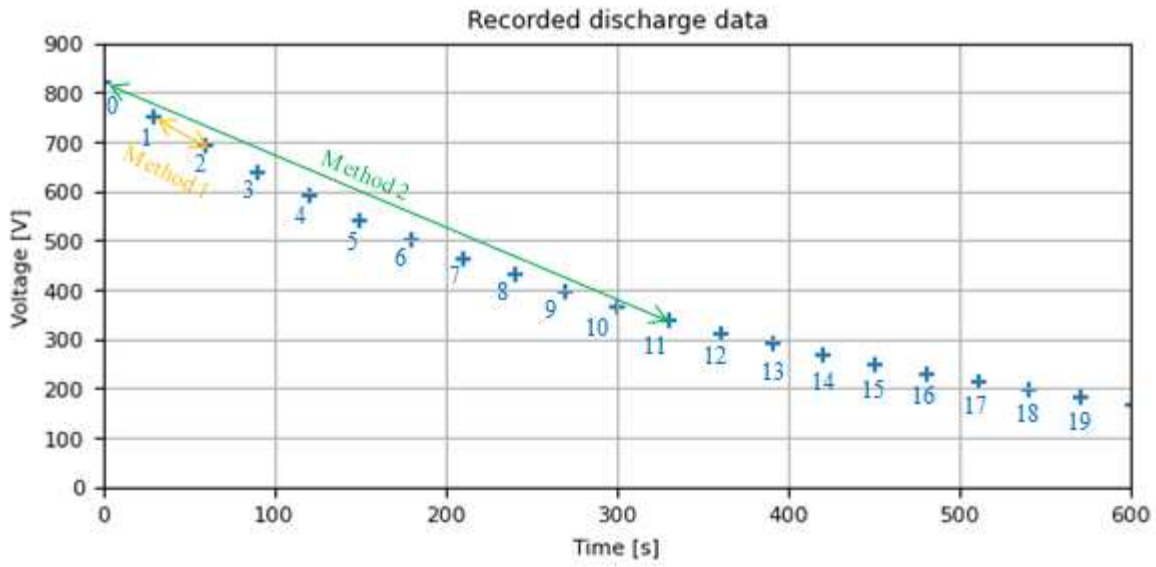


Fig. 7: Example of a recorded discharge data points. The yellow arrow shows a sample pair to calculate τ according to Method 1 and the green arrow according to Method 2.

To enable a statistical analysis of the data, τ is estimated from several sample pairs using both methods. The calculated outcome is indexed with the index of the first sample (S_1). In Table III the mean and Standard Deviation (SD) values are calculated for τ using both sampling methods. These two statistical indicators bases on the first five calculated τ, and again for the following next five calculations, and so on. This to show the impact of early and late samples.

Table III: Differences of sampling methods

	Method 1		*Method 2*	
Index of S_1	mean [s]	SD	mean [s]	SD
0 … 4	328.0	9.38	339.7	2.18
5 … 9	335.7	5.00	339.4	1.41
10 … 15	340.3	5.66	342.2	2.87
15 … 20	338.7	29.11	343.7	5.56

A good indicator of the robustness of the calculation is the SD. Table III shows that with Method 2 the SD is lower compared to Method 1 for each sampling case. Furthermore, the SD is lower for earlier samples, even when in the given data the SD of the τ of the first five samples indicates a higher value. It seems to be an effect of an outliner in the samples.

Therefore, potentially the best practise is to calculate τ from the first sample and the sample one τ later. Because of the remaining noise also on these two samples, it is wiser to use a higher number of τ calculations based on different sampling points and estimate an average value of τ. In the current implementation, τ is calculated with Method 2 from the first five sample pairs. From these values, the median is calculated, as the result for the discharge analysis. With the median principle, the τ calculation is more stable against outliners when compared to the case when only the mean is considered.

Verification of measurement principle

First an analysis of all the capacitors and resistors of the SIRIUS DC-link is done, to calculate the expected τ. The nominal value of the DC-link capacitance is 58.1 mF with a parallel resistance of 6.04 kΩ. Therefore, the nominal expected τ is 351.4 s.

For the two configurations with Bank “A” and Bank “B” the time constant is calculated analytically by doing network analysis to get reference values for the measurements. This is done by calculating the

resulting capacitance and the resulting resistance for the DC-link. These values are listed for both configurations in Table IV.

Table IV: Test configuration

Test configuration	**Bank "A"**	**Bank "B"**
DC-Link voltage	900V	
Calculated total capacitance	54.7mF	61.3mF
Calculated total resistance	6.04kΩ	
Calculated τ	330.4s	370.4s

Discharging tests were performed for both types of capacitor banks. For each bank, the test was performed three times, to validate the reproducibility. On each occasion, the converter was turned-on and when the DC-link reached 900V, it was turned-off to record the capacitor discharge. In Fig. 8 the recorded data points from the first measurement of the capacitor banks "A" and "B" are plotted.

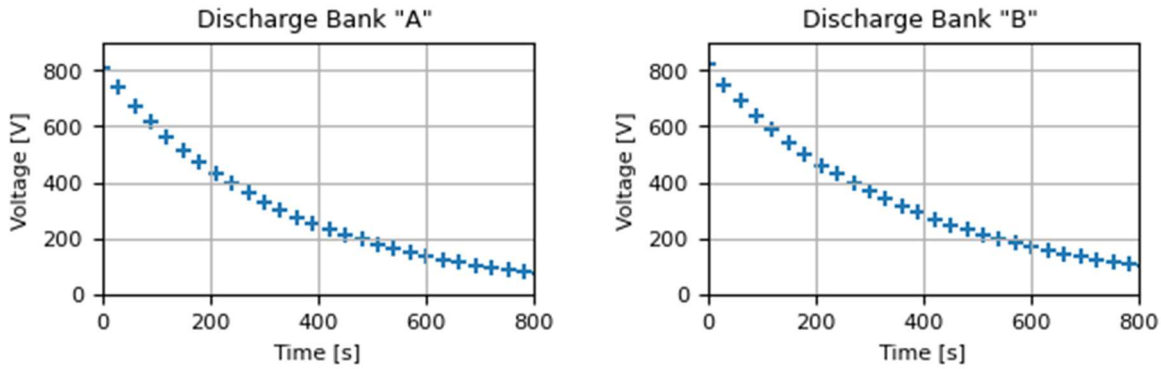


Fig. 8: Experimental discharging plots for capacitor Bank "A" and "B" (measurement 1).

From this data points, τ is calculated and the results for the three repeated measurements with both banks are summarized in Table V.

Table V: Estimated τ values based on experimental data

Test results	**Bank "A"**	**Bank "B"**
Calculated τ	330.4s	370.4s
τ measurement 1	*336.3s*	*381.2s*
τ measurement 2	*336.7s*	*379.9s*
τ measurement 3	*336.3s*	*381.2s*

The repetition of the experiments has shown a good reproducibility of the measurements, and the extracted τ values are close to the calculated ones. All the measurements are conducted in sequence to minimize the effect of temperature changes.

Measuring the time constant in the proposed way can be used as an indicator for the capacitor bank CM. The change of the capacitor type from "A" to "B" has increased the capacitance by 12%, which is a quite significant change to validate the scheme. The proposed method makes a one-point overall measurement of all capacitors connected to the DC link. This gives a good overview of the condition of the connected banks.

However, the anticipated limitation using this method is the weakness of assessing the health status of each single capacitor, especially in the cases when several capacitor banks were connected to the converter. In the current investigations thermal dependencies were neglected, which also influence the

value of the capacitance and the resistors. An increase of temperature of the discharging resistor increases of 5% yields an increase of τ from 330.4 s to 340.2 s for Bank "A" of capacitors. Therefore, such aspects must be taken into the calculation to accurately estimate τ.

With the proposed method the focus is on the ageing mechanism of the capacitance decrease and leakage current increase. For many applications, a low series impedance is essential. An increase of this impedance will not be detected by the proposed method.

5. Conclusion

This work proposes the use of standard precision (~0.1-1%) measurements using the DC-link voltage sensor to acquire a capacitive voltage decay. Using an experimental setup with two different types of capacitor banks (54.7mF and 61.3mF) it was demonstrated that it is possible to detect up to 1mF of capacitance difference. Noise and measurement inaccuracy has lowest impact when the time difference between two voltage samples is 1τ. This system is, therefore, able to detect a capacitance decrease of 10% due to degradation which is the degradation alert threshold for the application under study.

It is possible to perform the voltage measurement with the existing sensors as used for control. This helps to reduce cost and keeps the hardware complexity low. Therefore, this system can even be introduced for existing converters without any hardware changes. The use of the regular shut-down periods of the converters for performing quasi-offline measurements enable automatized measurements with reduced noise impact. Moreover, computing power of the converter controller and network capacity for CM will be available after the operational turn-off. The voltage sampling can be performed in an optimal way to reduce the impact of noise and the limited measurement accuracy.

References

[1] S. Peyghami, Z. Wang and F. Blaabjerg, "A Guideline for Reliability Prediction in Power Electronic Converters," *IEEE TRANSACTIONS ON POWER ELECTRONICS,* vol. 35, no. 10, pp. 10958-10968, 2020.

[2] S. Zhao and H. Wang, "Enabling Data-Driven Condition Monitoring of Power Electronic Systems With Artificial Intelligence: Concepts, Tools, and Developments," *IEEE POWER ELECTRONICS MAGAZINE,* pp. 18-27, 23 March 2021.

[3] Z. Zhao, P. Davari, W. Lu, H. Wang and F. Blaabjerg, "An Overview of Condition Monitoring Techniques for Capacitors in DC-Link Applications," *IEEE TRANSACTIONS ON POWER ELECTRONICS,* vol. 36, no. 4, p. 3692, 2021.

[4] P. Sundararajan, M. Sathik, F. Sasongko, C. Seng Tan, J. Pou, F. Blaabjerg and A. K. Gupta, "Condition Monitoring of DC-Link Capacitors Using Goertzel Algorithm for Failure Precursor Parameter Goertzel Algorithm for Failure Precursor Parameter," *IEEE TRANSACTIONS ON POWER ELECTRONICS,* vol. 35, no. 6, pp. 6384 - 6396, 2020.

[5] M. Ghadrdan, S. Peyghami, H. Mokhtari, H. Wang and F. Blaabjerg, "Dissipation Factor as a Degradation Indicator for Electrolytic Capacitors," *Emerging and Selected Topics in Power Electronics.*

[6] M. Asoodar, M. Nahalparvari, C. Danielsson, R. Söderström and H.-P. Nee, "Online Health Monitoring of DC-Link Capacitors in Modular Multilevel Converters for FACTS and HVDC Applications," *IEEE TRANSACTIONS ON POWER ELECTRONICS,* vol. 36, no. 12, pp. 13489-13503, 2021.

[7] T. Li, J. Chen, P. Cong, X. Dai, R. Qiu and Z. Liu, "Online Condition Monitoring of DC-Link Capacitor for AC/DC/AC PWM Converter," *IEEE TRANSACTIONS ON POWER ELECTRONICS,* vol. 37, no. 1, pp. 865-878, 2022.

[8] W. Yu and X. Du, "A VEN Condition Monitoring Method of DC-Link Capacitors for Power Converters," *IEEE TRANSACTIONS ON INDUSTRIAL ELECTRONICS,* vol. 66, no. 2, pp. 1296-1306, 2019.

[9] "SIRIUS," CERN Medium Power Converters Section, 20 June 2022. [Online]. Available: https://section-mpc.web.cern.ch/content/sirius. [Accessed 20 June 2022].

[10] "Documentation SIRIUS," CERN Medium Power Converters Section, 19 December 2021. [Online]. Available: https://section-mpc.web.cern.ch/content/documentation#Sensors%20and%20interfaces. [Accessed 19 December 2021].