Master's thesis

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Modelling and control of a fault-tolerant bidirectional hybrid microgrid for marine applications

Master's thesis in Energy and Environmental Engineering
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Preface

This master thesis contains my final works as a student at the Department of Electric Power Engineering at the Norwegian University of Science and Technology(NTNU). The master thesis is written in collaboration with Siemens Offshore Marine Centre in Trondheim and is a continuation of a preliminary specialization project completed in the fall of 2019 [1].

I wish to thank my supervisor at NTNU, Prof. Elisabetta Tedeschi. Through the specialization course titled "Power Electronics in Future Power Systems," she has provided me with outermost necessary knowledge prior to the master thesis. Her expertise and guidance have been a great resource throughout my work. I am especially thankful for her availability and always willing to assist. I want to thank Dr. Atle Rygg, who initiated the cooperation leading to the master thesis. An interesting and challenging topic has made the last year an exciting journey. Atle has a unique understanding of the subject, and his knowledge has been vital.

Abstract

This master thesis investigates the possibility of forming a robust bidirectional hybrid AC/DC marine power system with a voltage source converter(VSC) as the critical interfacing unit. Figure 1 shows the system studied in this thesis. The DC grid contains a switch-connected battery and a controllable current source representing the grid. The AC grid is constituted by a three-phase voltage source, a Thevenin series inductance and an LCL-filter used for switching frequency attenuation.

The work is particularly aimed towards the development of a flexible VSC control strategy able to maintain the DC voltage in case the main unit responsible for DC voltage control, i.e the battery, is disconnected. The DC grid forming responsibility is then put on the interfacing converter powered by the AC grid. Instantaneous fault detection and proper change in converter control mode from power management to DC voltage control is proposed. Finally, actions to minimize voltage deviation and recovery time should be implemented in a robust way to ensure seamless operation.

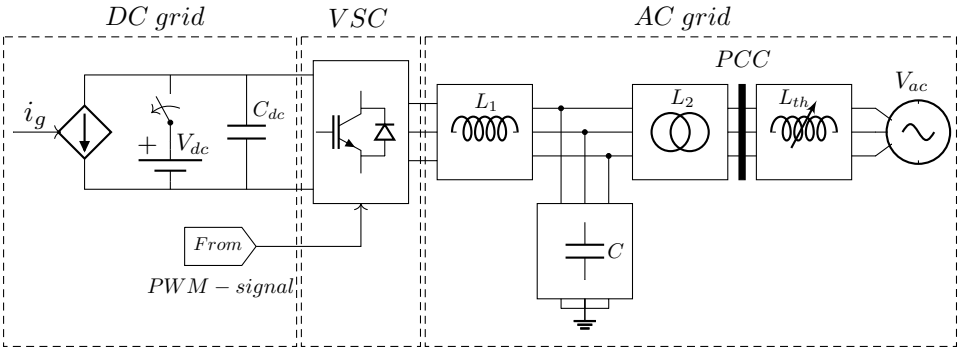

Figure 1: The system studied in this thesis.

To obtain realistic simulation results, the system is discretely implemented with accurate measurement sampling delays. Active damping of the LCL-filter resonance is incorporated to maintain flexible operation with respect to changing grid conditions, i.e., varying grid inductance L_{th}, and power flow. With no DC to DC converter present at the DC terminal, the VSC is prone to operate in the overmodulation range. Emphasis is consequently put on reactive power compensation and harmonic voltage attenuation to comply with marine power system regulations.

Reactive compensation has shown to effectively reduce the degree of overmodulation. From a stability point of view this is crucial during power control mode of operation, when the system is exposed to weak grid conditions, i.e, large values of the grid inductance. In DC voltage control mode, the absence of reactive compensation cause immediate insta-

bility. Reactive compensation limits voltage total harmonic distortion(THD) to levels below 11% at point of common coupling(PCC). By further introducing a selective harmonic compensation strategy, the 5th order voltage harmonic is compensated, and the resulting voltage THD holds levels below 6% for all grid conditions. This is within the permitted limits of 8% voltage THD given by the marine power system standard.

When the battery is disconnected, the implemented change of control mode ensures retained DC voltage. The transient peaks are increased with increasing grid inductance and power transfer prior to the fault. Introducing transient current reference impulses in the control system has shown to fast reverse the power flow and reduce the peak of the transient. When rated active power is transferred to the DC grid or to the AC grid prior to the fault, the peak of the voltage transient is reduced by 43% and 50%, respectively, compared to the voltage level at fault detection, with transient current references added in the control system.

Samandrag

Denne masteroppgåva ser på moglegheita til å forme eit robust hybrid AC/DC marint kraftsystem med ein spenningskjelde omformar(VSC) som kritisk koplande komponent. Figur 2 viser systeme som er studert i denne oppgåva. DC-distribusjonsnettet inneheld eit brytarkopla batteri og ei variabel straumkjelde som representerar nettet. AC distribusjonsnettet består av ein trefase spennigskjelde, ein Thevenin serie induktans og eit LCL-filter til å fjerne støy. Arbeidet er særleg retta mot å konstruere ein fleksibel VSC kontroll strategi som er i stand til å oppretthalde DC spenninga dersom hovedkomponenten ansvarlig for DC spenningskontroll vert fråkopla. Ansvaret for å oppretthalde DC spenninga vert lagt på spenningskjeldeomformaren med kraft frå AC nettet. Rask feildeteksjon og passande endring i omformar kontroll strategi frå effektkontroll til DC-spenningskontroll er foreslått. Til slutt, metodar for å minimere spenningstransient amplitude og varigheit vert implementert på ein robust måte for å sikre sømlaus drift.

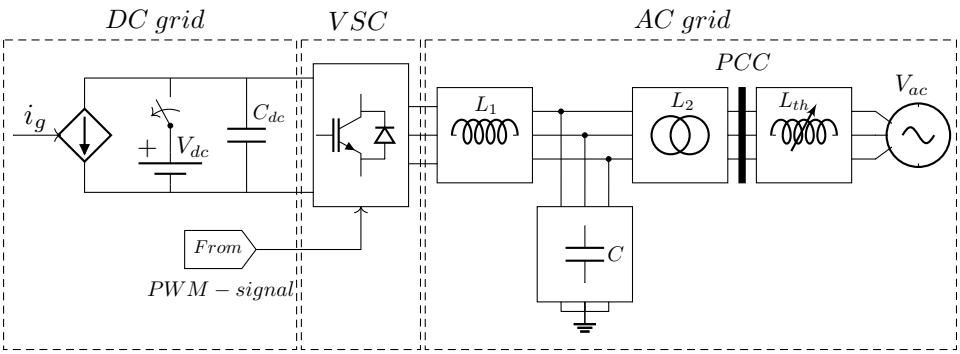

Figure 2: Systemet under etterforskning.

For å oppnå realistiske simuleringsresultat er systeme diskret implementert med nøyaktig forsinkelse på målingar. Aktiv demping av LCL-filter resonans er inkludert for å sikre fleksibel drift med hensyn til endrande nettforhold, dvs. varierande nettimpedans L_{th}, og kraftflyt. Utan DC til DC omformar ved DC terminalen er VSC-en utsatt for å operere med overmodualsjon. Insats er derfor brukt til reaktiv effektkompensering og demping av harmonisk spenning for å overholde reguleringar for kraftsystemet. Reaktiv effektkompensering har vist seg å effektivt redusere graden av overmodulering. Frå eit stabilitetsperspektiv, så er dette kritisk under effektstyring ved svakt nett, dvs. høg nettimpedans. Under DC spenningskontroll, vil fravær av reaktiv effektkomensering skape et umiddelbart ustabilt system. Reaktiv effektkompensering begrensar total harmonisk støy(THD) i spenninga til nivå under 11% ved AC terminal. Ved vidare å introdusere ein selektiv harmonisk kompanseringsstrategi, kan 5. harmonisk spenning verte kompensert og resulterande THD

bli begrensa til nivå under 6% for alle nettforhold. Dette er innanfor kravet på maks 8% spennings-THD bestemt av maritim kraftnettstandard.

Når batteriet vert frakopla, vil endring i VSC kontrollstrategi sørge for vedlikeholdt spenningsnivå. Transientens magnitude vert auka ved aukande nettinduktans og effektflyt forrut for hendinga. Ved å introdusere transient spenningsreferanse impulsar i kontrollsystemet, kan effektflyten raskt reverserast noko som igjen vil føre til ein mindre transient spenningsmagnetude. Når nominell aktiv effekt vert overført til DC side eller til AC side forut for feilen, vil transient magnituden verter redusert med hendholsvis 43% og 50% samanlikna med spenninga forut for feilen. Dette med transient straumreferanse inkludert i kontrollsystemet.

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Abbreviations

AC	=	Alternating Current
APF	=	Active Power Filter
DC	=	Direct Current
ESS	=	Energy Storage System
IGBT	=	Insulated Gate Bipolar Transistor
LCC	=	Line Commutated Converter
PCC	=	Point of Common Coupling
PID	=	Proportional Integral Derivative
RMS	=	Root Mean Square
THD	=	Total Harmonic Distortion
VFD	=	Variable Frequency Drive
VSC	=	Voltage Source Converter
VSI	=	Voltage Source Inverter
WBG	=	Wide Band-gap

Chapter 1

Introduction

1.1 Background and perspective

The worlds energy demand is increasing. A growing global population combined with an overall higher standard of living, add pressure on natural resources. Through the Paris agreement, almost every country has committed to strengthening the global response to the threat of climate change by cutting their pollution form greenhouse gasses[2]. However, the increasing demand for energy is challenging to cover with renewable energy sources, and the CO_2 emissions have continued to grow[3].
Great leaps towards fulfilling the Paris Agreement can be made through the development of a more sustainable maritime sector. The passenger ferry has proven to be an important part of the city's transportation system, with almost 40% of the world's population living in coastal areas surrounded by waterways like channels, rivers, and fjords. For shipping, the industry is considered as a significant part of the global economy, transporting over 90% of international trade[4]. The quality of the different marine fuel oils is often low, with high levels of carbon dioxide, nitrogen oxides, sulfur dioxide, and particulate matter shown to reduce the population's life expectancy and to have a negative impact on the environment[5]. The potential to reduce negative externalities by integrating renewable energy in the marine power system is significant when considering traditional combustion engines being used as a power source in almost every marine vessel today.
A massive integration of carbon-neutral fuels and a more efficient exploitation of traditional fuels is enabled thanks to energy storage systems(ESS)[6]. The rapidly evolving battery technology, including lithium-ion with high power storage and fast energy transfer capabilities, is a game-changer. With steadily improving power electronic technologies, the possibility to store energy greatly impacts how energy is generated, distributed, and consumed. Future berthed ships may have the opportunity to receive power from the terrestrial grid and leave the harbor with carbon-neutral fuel. Energy management systems(EMS) are becoming more efficient, utilizing concepts as peak shaving and optimized load sharing in terms of fuel consumption and wear and tear of machinery and power system components. In tomorrows marine vessels, both onboard hotel loads and propulsion

systems are powered by electricity. Pressure is consequently added to the maritime power system in terms of stability and reliability.
A promising power distribution system is the direct current(DC) distribution system[7][8]. The DC distribution has high power transfer capabilities and facilitates easier integration of ESS and variable frequency drives(VFD) as appose to traditional alternating current(AC) distribution system. However, onboard hotel loads still demand AC power distribution, and hybrid solutions are getting more and more attention. The possibility to benefit from properties of both sub-grids combined with added robustness of the overall power system is key.

The voltage source converter(VSC) is particularly suitable as an interfacing unit of a hybrid distribution system thanks to its inherent drive system. The drive system allows for high flexibility with inbuilt capability to control both active and reactive power individually. By changing the direction of the current through the converter, the power flow is reversed. A significant advantage compared to the more traditional line commutated converter(LCC), where the voltage polarity of the converter must be changed to obtain reversed power flow.

1.2 Problem formulation

This master thesis continues the previous work that was done in the specialization project [1]. In the specialization project, current and voltage control of a marine hybrid AC/DC two-level pulse width modulated VSC was developed in the synchronous reference frame. The controllers were tuned according to novel methods and individually tested through simulations. In the master thesis, a more exact setup will include accurate sampling delay and controllers that can handle weak grid conditions. The master thesis further adopts a more ”system-level approach” compared to the specialization project that was more focused on the VSC as a component. Figure 1.1 illustrates the system of investigation. The DC distribution includes a switch-connected battery together with a capacitor. The capacitor act as short term energy storage device. To model the power generation and consumption of the grid, a controllable current source is included. The DC distribution system is connected to the AC distribution system through an interfacing converter and an LCL-filter. The grid conditions at the PCC of the AC grid are modeled with a varying Thevenin series inductance L_{th}.

The investigation of the thesis is specially focused on supporting the DC voltage if the main unit responsible for DC voltage,i.e. the battery, is disconnected. Simple fault detection schemes must be implemented, and the VSC should be able to quickly switch from power management(P-control) to DC voltage control and prevent outage of the DC distribution system. Finally, actions to minimize voltage deviation and recovery time should be implemented to ensure seamless operation.

One particular concern regarding the AC distribution power quality is connected to overmodulation of the VSC. Overmodulation contributes significantly to total harmonic distortion(THD) and must be discussed and limited. The upper allowable limit of THD in the marine power system is 8% with a maximum contribution per harmonic order of 5% [9].

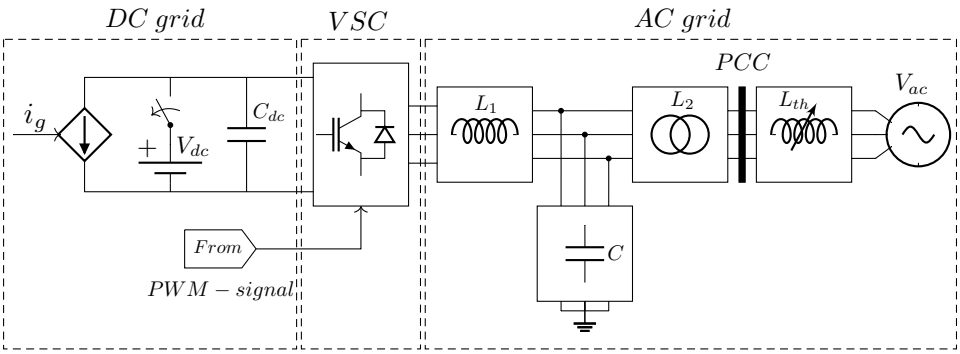


Figure 1.1: The system under investigation.

1.3 Objectives

In this master thesis the main objectives are to:

- Develop a control of the VSC capable of controlling both active power and DC terminal voltage under different grid conditions.
- Discuss different fault detection schemes in case the main unit responsible for DC voltage control is disconnected.
- Propose and discuss VSC control strategies aimed to reduce the DC voltage transients and recovery time.
- Ensure compliance of the power system in terms of current and voltage ratings and power quality regulations.
- Develop an original MATLAB/Simulink model to investigate system performance.

1.4 Report outline and limitations

To cover the above-mentioned objectives, the thesis is divided into nine chapters. The first chapter holds the introduction. Next, in Chapter 2, system parameters are given with a presentation of the per unit system. Chapter 3 establishes the basic theory of VSC modelling and control. This includes an introduction of pulse-width modulation, phase-locked loops, controller development and tuning. The material is refined, based on information presented in the specialization project [1]. Chapter 4 is further dedicated to the characteristics of the LCL-filter. The filter resonance is under discussion where both passive and active damping methods are presented. In Chapter 5, the performance of the power control and the DC voltage control is individually tested through simulations utilizing MATLAB/Simulink. Findings from Chapter 5 indicate that the VSC is inevitably operating in overmodulation, causing significant THD levels. Therefore, measures to reduce THD to stay within marine

power system regulations needed to be addressed. Consequently, Chapter 6 was aimed to investigate the harmonic distortion and frequency spectrum. It further proposes harmonic filters where a VSC- integrated selective harmonic compensation strategy is chosen and verified. Chapter 7 investigates controller action when outages of generation units occur. More specifically, this includes a change in control mode from active power to DC voltage when the DC grid-connected battery is disconnected. Simple fault detection schemes are discussed and tested. In Chapter 8, methods to reduce the voltage transient and recovery time during the change of control mode is proposed and verified.

The conclusion is finally drawn in Chapter 9. This chapter also includes suggestions for further work based on findings in the thesis.

Chapter 2

System description

In this chapter, the system under investigation is presented. Necessary parameters are given, and the per unit(PU) system is introduced.

2.1 System parameters

The system parameters were provided by Siemens Offshore Marine Centre in Trondheim and are listed in table 2.1. The grid inductance L_{th}, has been reported to stay in the range of 0.2 mH and 0.3 mH under normal operating conditions. However, grid impedance values from $0.05mH$ to over 0.4 mH are expected. Varying grid impedance values is a key consideration of the VSC controller tuning and is further discussed in Chapter 3.

Table 2.1: System values.

Converter Switching Frequency	f_{sw}	2000Hz
Sampling Frequency	f_{samp}	4000Hz
AC terminal Frequency	f_n	50Hz
Nominal Apparent Power	S_n	1.5MVA
AC terminal Nominal Line to Line Voltage	v_n	690V
DC terminal Nominal Voltage	$v_{n,dc}$	1000V
Filter Inductance	L_1	$60\mu H$
Filter Inductance	L_2	$50\mu H$
Filter Capacitance	C	$2mF$
DC terminal Capacitance	C_{dc}	$25mF$
Internal Resistance	R_{L_1}, R_{L_2}, R_C	$1.6m\Omega$

2.2 The per unit system

A more generalized system is obtained by expressing system parameters as a fraction of set base values. The base values are often based on nominal or maximum values of power and current as well as normal operating voltage and frequency levels. Equation (2.1) show the AC terminal base values. The power base is equal to the apparent nominal power, the voltage base is equal to the peak nominal phase voltage, and the current base is equal to the peak nominal phase current. Further, the base impedance is equal to the base voltage divided by the base current.

$$S_b = s_n, V_b = \frac{\sqrt{2}}{\sqrt{3}} v_n, I_b = \frac{\sqrt{2} s_n}{\sqrt{3} v_n}, Z_b = \frac{v_n^2}{s_n} \tag{2.1}$$

The base capacitance and inductance values are presented in Equation (2.2) given by the base impedance and angular frequency ω_b.

$$\omega_b = 2\pi f_n, L_b = \frac{Z_b}{\omega_b}, C_b = \frac{1}{Z_b \omega_b} \tag{2.2}$$

The voltage base of the DC terminal is equal to the nominal DC terminal voltage. This gives the DC terminal base values, as presented in Equation 2.3.

$$V_{b,dc} = v_{n,dc}, I_{b,dc} = \frac{Sn}{v_{n,dc}}, Z_{b,dc} = \frac{v_{n,dc}^2}{I_{n,dc}}, C_{b,dc} = \frac{1}{Z_{b,dc} \omega_b} \tag{2.3}$$

The pu capacitance of the DC terminal is found using Equation (2.4). Further explanation of the choice of DC terminal per unit capacitance is given in [1].

$$C_{dc_{pu}} = \frac{C_{b,dc}}{C_{dc}} \tag{2.4}$$

2.2.1 Per unit system values

Table 2.2 show the system values in pu.

$L_{1_{pu}}$	6%
$L_{2_{pu}}$	5%
$C_{_{pu}}$	20%
$C_{dc_{pu}}$	19%
$R_{L1_{pu}}$,$R_{L2_{pu}}$,$R_{C_{pu}}$,$R_{C_{dc,pu}}$	0.5%

Table 2.2: System values in pu.

Chapter 3

VSC modelling and control

This chapter builds on the specialization project presented in[1]. The content is rewritten with some extra material added, and figures have been redrawn to provide better explanations. This way, the master thesis can be read without having to read the specialization project. As the VSC is the fundamental component of the thesis, its study is particularly relevant. However, with countless articles on the topic, this chapter will provide a simplified review of the essential elements. This includes an explanation of the VSC model, VSC modulation, phase-locked loops, basic controller strategies, and tuning techniques.

3.1 The VSC model

A model of the two-level VSC is shown in Figure 3.1. The configuration contains six individually controlled switches connected with anti parallel diodes. $\vec{v}^a$, $\vec{v}^b$ and $\vec{v}^c$ are the AC terminal phase voltages and V_{dc} is the DC terminal voltage.

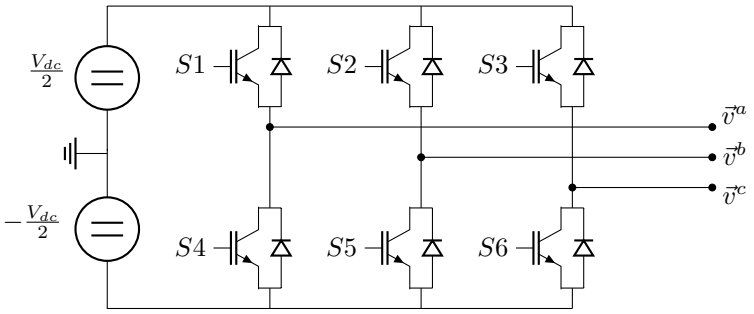


Figure 3.1: Voltage source converter model.

The VSC can be said to either operate as an inverter by changing direct power to alternating power, or operate as a rectifier by changing alternating power to direct power.

The output phase voltage is shaped by turning the switches of a bridge leg on and off. One switch(S1) of a converter bridge leg is always complimentary in relation to the other switch(S4) of the same bridge leg. This means that the maximum phase to neutral AC voltage is limited by half the DC voltage. By mutually displacing the switching signals of each converter bridge leg by 120° a three-phase voltage can be obtained. The switching signals are often generated by the use of pulse width modulation(PWM) further explained in the next section.

3.2 PWM methods

Pulse width modulation presents a method to control the amplitude and frequency of the fundamental output voltage of a converter. The voltage of each bridge leg is individually controlled by comparing the phase to neutral control voltage V_c to a triangular carrier V_{tri}. The modulation index M, represents the ratio between the fundamental part of the control voltage, $\hat{V}_c$, and the triangular carrier $\hat{V}_{tri}$.

$$M = \frac{\hat{V}_c}{\hat{V}_{tri}} \tag{3.1}$$

The most basic configuration contains a sinusoidal control voltage, termed SPWM. The control voltage is then $Msin(2\pi f_0 t)$ with amplitude M and frequency f_0. The SPWM technique is linear up to M equal to 1, after that overmodulation occurs[10].

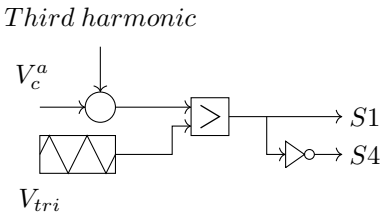


Figure 3.2: One-phase schematic diagram of the THIPWM.

The linear range of the line voltage can be increased by adding a third harmonic control voltage to the original control voltage(THIPWM) as shown in fig. 3.2. The zero sequence triple harmonics contained in the phase-to-neutral waveforms are eliminated from the line-to-line waveforms. Choosing an amplitude of one-sixth of the amplitude of the fundamental voltage, a 15% higher output line voltage is obtained without overmodulation[11][12]. Figure 3.3 shows the fundamental phase to neutral voltage and its corresponding THIPWM control signal. The frequency of the triangular carrier decides the frequency of the gate signal, i.e., the converter's switching frequency.

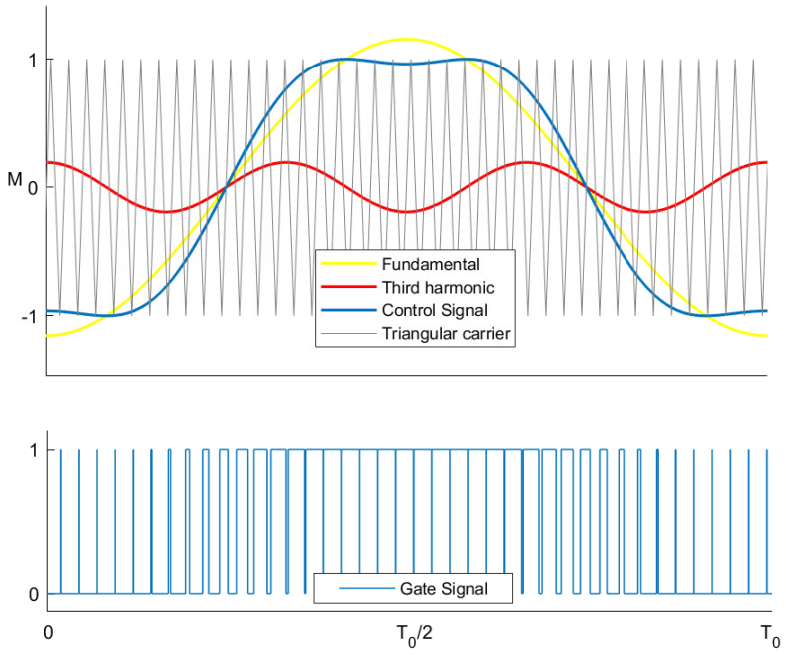


Figure 3.3: Continous control signal with third harmonic injection(THIPWM).

3.3 Reference frames and transformations

3.3.1 $\alpha\beta 0$ - transform

Balanced three-phase signals can be transformed into a two-dimensional space without loss of information in terms of magnitude and phase angle. The $\alpha\beta 0$-transform, also termed Clarke transform, thus simplifies the signal handling.

Let $\vec{i}^a(t) = \hat{I}cos(\omega t - \delta)$ be the phase-a current, balanced with $\vec{i}^b(t)$ and $\vec{i}^c(t)$. This means that the phase currents are mutually displaced by 120° and have the same amplitude $\hat{I}$. Then with a phase angle δ the transformation yields

$$\begin{aligned} \vec{i}^{\alpha}(t) &= \hat{I}cos(\omega t - \delta) \\ \vec{i}^{\beta}(t) &= \hat{I}sin(\omega t - \delta) \\ \vec{i}^{0}(t) &= 0 \end{aligned} \tag{3.2}$$

The new current vectors are now rotating with an angular velocity ω referred to the stationary two-axis $\alpha\beta 0$ reference frame. The transformation and inverse transformation are given in tabular form in Appendix A.

3.3.2 $dq0$ - transform

The dq0-transform, also termed Park transform, is an expansion of the $\alpha\beta0$-transform. The difference is that the dq0 reference frame rotates with an angular velocity equal to the three-phase balanced signal. A dq0 representation will let the three-phase AC signals appear as DC equivalents, which is particularly useful in a control environment. The relationship between the two reference systems is given in Equation 3.3.

$$\vec{i}^{dq} = \vec{i}^{\alpha\beta} e^{j\omega t} \tag{3.3}$$

The transformation and inverse transformation are given in tabular form in Appendix A.

3.4 Phase-locked loops

Grid synchronization can be obtained utilizing a phase-locked loop(PLL) to track the oscillating input voltage frequency and phase angle. The technology is widely employed in modern electronic devices and is key to the control of grid-connected VSCs. Although there are multiple PLL typologies and implementations, a common system includes a phase angle comparator, a low-pass filter, and a voltage-controlled oscillator. The PLL used in this master thesis is shown in fig. 3.4.

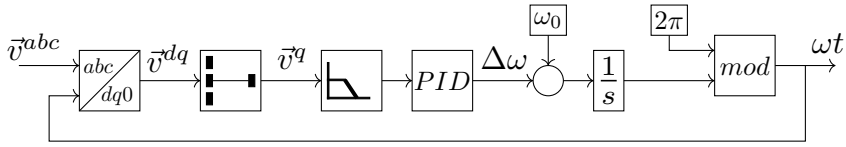


Figure 3.4: Phase-locked loop.

The goal is to track the phase angle of the grid voltage $\vec{v}^{abc}$ so that the Park's transformed system can be oriented such that the q-component of the voltage, v^q is equal to zero. The orientation is here obtained with a PID controller. The expected reference angular frequency ω_0 is fed forward, and the modulus operator ensures values between zero and 2π for the Park's transformation matrix block. The controller of the PLL must be tuned emphasizing on the stability of the grid with grid-connected unbalanced loads as a key consideration. [13]

3.5 VSC control strategies

The VSC control system is based on an inner current control loop handling the AC current and outer controllers, which supply references to the inner controller. The inner controller operates faster than the outer controller in order to ensure proper decoupling of the two. DC voltage control, AC voltage control, active power control, reactive power control, and frequency control are all examples of outer controllers. In this thesis, the DC voltage

control and the P-control will be the main outer controllers supplying references to the d-axis current. Whereas, a reactive power control loop operates by supplying reference to the q-axis current. Figure 3.5 illustrates a DC distribution system and an AC distribution system interconnected through a VSC and an LCL-filter.

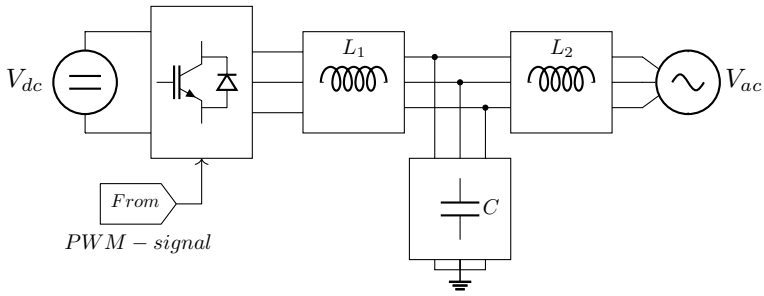


Figure 3.5: VSC based hybrid AC/DC power system.

3.5.1 Current control

The current can be controlled through the filter inductor L_1. An equivalent circuit from the converter output voltage, $\vec{v}_{conv}^{abc}$ to the filter capacitor voltage, $\vec{v}_C^{abc}$ is presented in fig. 3.6. R_{L_1} is the internal resistance of the filter inductor L_1. The on-state and switching resistance of the converter are neglected in this model as they are small compared to the filter inductor resistance.

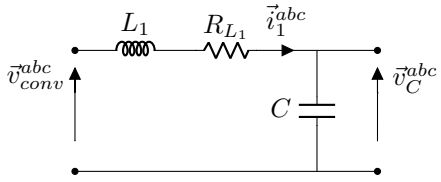


Figure 3.6: Eq. circuit: Current control.

From the equivalent circuit, Equation (3.4) is obtained.

$$L_1 \frac{d\vec{i}_1^{abc}}{dt} + R_{L_1} \vec{i}_1^{abc} = \vec{v}_{conv}^{abc} - \vec{v}_C^{abc} \tag{3.4}$$

The corresponding Park's transformed and per unit representation of the system is presented in Equation (3.5). Derivations and further explanations are available in [1].

$$\frac{L_{1_{pu}}}{\omega_b} \frac{di_{1_{pu}}^d}{dt} + R_{L_{1pu}} i_{pu}^d - \underbrace{\omega_{pu} L_{1_{pu}} i_{1_{pu}}^q}_{\text{Decoupling Term}} = v_{conv_{pu}}^d - \underbrace{v_{C_{pu}}^d}_{\text{Feed Forward}} \tag{3.5a}$$

$$\frac{L_{1_{pu}}}{\omega_b}\frac{di^q_{1_{pu}}}{dt} + R_{L_{1pu}} i^q_{1_{pu}} + \underbrace{\omega_{pu} L_{1_{pu}} i^d_{pu}}_{\text{Decoupling Term}} = v^q_{conv_{pu}} - \underbrace{v^q_{C_{pu}}}_{\text{Feed Forward}} \tag{3.5b}$$

It can be observed from Equation (3.5) that the d- and q-components of the current i_1 are coupled through the term $\omega_{pu} L_{1_{pu}} \vec{i}^{dq}_{1_{pu}}$. As the effect of the coupling term will appear in the system, the converter controller can account for this effect by canceling the coupling term from the converter reference signal with a corresponding feed-forward term. The absence of such a feed-forward term will cause a slower and more unstable control. For faster control, the measured or steady-state voltage over the capacitor, $\vec{v}^{dq}_{C_{pu}}$ can be fed forward the same way.

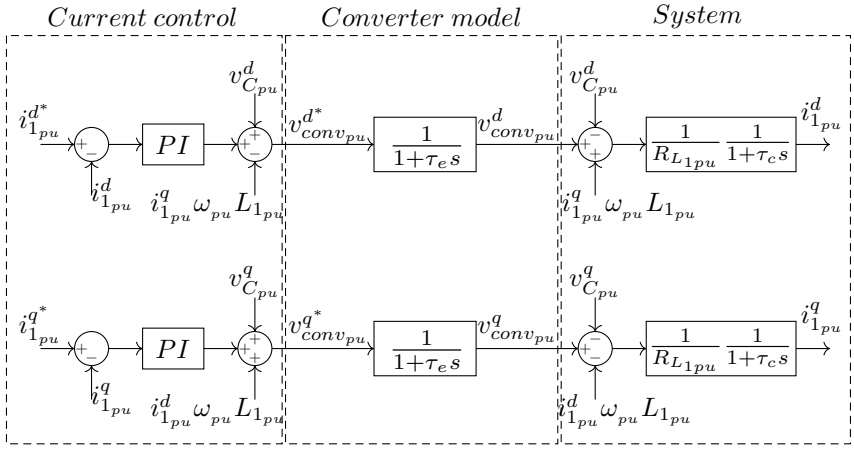


Figure 3.7: Block diagram: Current control.

Figure 3.7 illustrates the pu control scheme of the current controller with PI regulator and the system as described in Equation (3.6) with system time constant, τ_c given in Equation (3.7). The time delay τ_e, is the average modulation time delay plus the analog to digital to analog conversion time delay. Reference parameters are marked $*$.

$$\frac{\vec{i}^{dq}_{1_{pu}}(s)}{\vec{v}^{dq}_{conv_{pu}}(s)} = \frac{1}{R_{L_{1pu}}}\frac{1}{1+\tau_c s} \tag{3.6}$$

$$\tau_c = \frac{L_{1_{pu}}}{\omega_b R_{L_{1pu}}} \tag{3.7}$$

3.5.2 DC voltage control

The DC terminal voltage is controlled in cascade with the inner current control. Figure 3.8 illustrate the DC side equivalent circuit where i_{dc} is the current fed from the converter, $i_{C_{dc}}$ is the capacitor current and $i_{dc_{grid}}$ is the dc grid current.

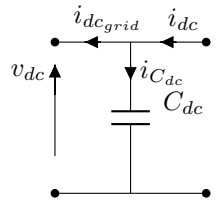


Figure 3.8: Eq. circuit: Voltage control.

The DC voltage is controlled by manipulating the current in the capacitor, C_{dc}. The voltage is then given by Equation (3.8).

$$v_{dc} = \frac{1}{C_{dc}} \int i_{C_{dc}} dt \tag{3.8}$$

To be able to control the capacitor current $i_{C_{dc}}$, utilizing the current control presented in section section 3.5.1, active power balance can be assumed across the converter. Now, if the synchronous reference frame is aligned such that the q-component of the voltage, v^q is equal to zero, i_{dc} is obtained as a function of i_1^d described by Equation (3.9).

$$i_{dc} = \frac{3}{2} \frac{v^d i_1^d}{v_{dc}} \tag{3.9}$$

The current balance equation then becomes.

$$C_{dc} \frac{dv_{dc}}{dt} = \frac{3}{2} \frac{v^d i_1^d}{v_{dc}} - \underbrace{i_{dc_{grid}}}_{\text{Feed Forward}} \tag{3.10}$$

Now, because Equation (3.10) is nonlinear, a linearization of the function around a reference point is necessary. The voltage reference point is at one pu. Further explanation of the linearization and per unit transformation is given in the previous work of the specialization project [1]. The linearized and simplified per unit system is shown in Equation (3.11) with system time constant from Equation (3.12). The DC grid current can be considered as a feed-forward.

$$\frac{\Delta v_{dc_{pu}}(s)}{\Delta i_{pu}^d(s)} = \frac{1}{\tau_v s} \tag{3.11}$$

$$\tau_v = \frac{1}{\omega_b C_{dc_{pu}}} \tag{3.12}$$

The outer voltage control block diagram is illustrated in Figure 4.5. Here, τ_{eq} represents the equivalent time delay of the inner current control. A first order approximation of the dynamics of the internal closed loop current controller is made for simple design of the outer control loop.

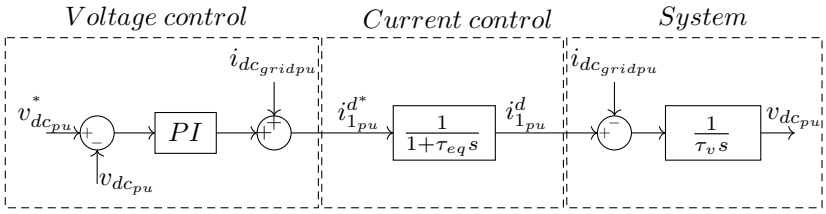


Figure 3.9: Block diagram: Voltage control.

3.5.3 Active and reactive power control

The active and reactive power of the converter can be controlled in cascade with the current control. Again assuming that the synchronous reference frame is oriented such that v^q is equal to zero, active and reactive power are controlled by adjusting the current i^d and i^q, respectively, according to Equation (3.13).

$$P_{pu} = v^d_{pu}\, i^d_{pu} \tag{3.13a}$$

$$Q_{pu} = v^d_{pu}\, i^q_{pu} \tag{3.13b}$$

Figure 3.10 show the block diagram of the PQ-control.

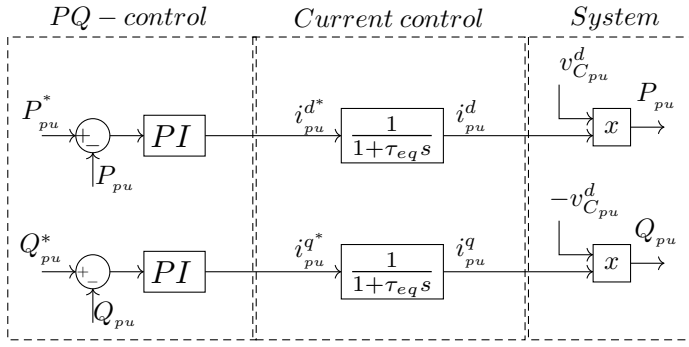


Figure 3.10: Block diagram: PQ-control.

3.5.4 Controller tuning methods

The modulus optimum and the symmetrical optimum tuning criteria will be evaluated for the inner and outer PI controllers, respectively.

Modulus optimum

The objective of the modulus optimum criteria is to obtain a closed loop system with a crossover frequency as large as possible. At any frequency lower than the crossover

frequency, the closed loop gain is equal to one. For plants containing one large time constant and other minor time constants, this is achieved by canceling the largest time constant. Figure 3.11 shows the closed loop current control block diagram discarding the terms compensated by the feed-forward terms.

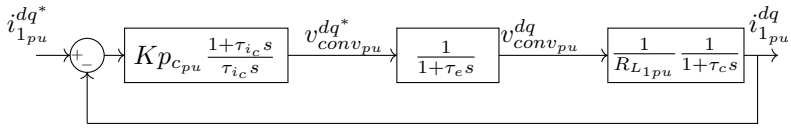


Figure 3.11: Simplified Block Diagram: Current control.

The current control open loop transfer function is given in Equation (3.14).

$$G_{OL_C}(s) = \underbrace{Kp_{c_{pu}} \frac{1+\tau_{i_c} s}{\tau_{i_c} s}}_{\text{PI controller}} \frac{1}{1+\tau_e s} \frac{1}{R_{L_{1pu}}} \frac{1}{1+\tau_c s} \tag{3.14}$$

Following the modulus optimum criterion, the PI controller time constant τ_{i_c}, is set equal to the current control system time constant τ_c.

$$\tau_{i_c} = \tau_c = \frac{L_{1_{pu}}}{\omega_b R_{L_{1pu}}} \tag{3.15}$$

The resulting second order closed loop transfer function is then compared to the characteristic second order polynomial[1].

$$A(s) = s^2 + 2\delta\omega_0 s + \omega_0^2 \tag{3.16}$$

The closed loop transfer function follows from Equation (3.17).

$$G_{CL_C}(s) = \frac{G_{OL_C}(s)}{1 + G_{OL_C}(s)} = \frac{\frac{Kp_C \omega_b}{L_{2_{pu}} \tau_e}}{s^2 + \frac{1}{\tau e} s + \frac{Kp_{C_{pu}} \omega_b}{L_{2_{pu}} \tau_e}} \tag{3.17}$$

Equation (3.18) show the proportional gain obtained with respect to the relative damping factor ζ. The integral gain is the proportional gain divided by the controller integral time constant.

$$Kp_C = \frac{L_{1_{pu}}}{4\omega_b \delta^2 \tau_e} \tag{3.18}$$

Symmetrical optimum

In cases where the open loop transfer function of the control system has two poles at the origin, the symmetrical optimum tuning criteria is suitable. The idea is to maximize the phase margin at the crossover frequency. As the phase margin is maximized, the system will tolerate more considerable time delays. Figure 3.12 show the closed loop DC voltage control block diagram discarding the terms compensated by the feed-forward terms.

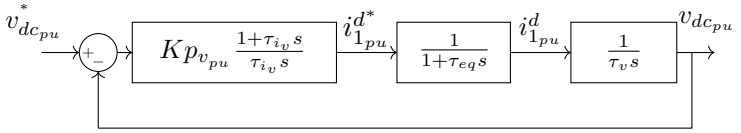


Figure 3.12: Simplified Block Diagram: Voltage control.

The voltage control open loop transfer function is given in Equation (3.19).

$$G_{OL_v}(s) = \underbrace{Kp_{v_{pu}} \frac{1+\tau_{i_v} s}{\tau_{i_v} s}}_{\text{PI controller}} \frac{1}{1+\tau_{eq} s} \frac{1}{\tau_v s} \tag{3.19}$$

The DC voltage time constant is,

$$\tau_v = \frac{1}{\omega_b C_{dc_{pu}}} \tag{3.20}$$

and the current control equivalent time delay τ_{eq}, is a first order approximation of the second order current control transfer function time delay given by 3.21. A justification of the simplification is given in [1].

$$\tau_{eq} = 2\tau_e \tag{3.21}$$

The integral time constant of the controller τ_{i_v} is given as a function of phase margin $\phi_{M_{dc}}$, following the symmetrical optimum tuning criteria[1].

$$\tau_{i_v} = \tau_{eq} \frac{1 + sin\phi_{_{M_{dc}}}}{1 - sin\phi_{_{M_{dc}}}} \tag{3.22}$$

The proportional gain is obtained knowing that the magnitude of the transfer function is equal to one at crossover frequency(3.23). The integral gain is the proportional gain divided by the controller integral time constant.

$$Kp_{v_{dc_{pu}}} = \frac{1}{\omega_b C_{dc_{pu}} \sqrt{\tau_{i_v} \tau_{eq}}} \tag{3.23}$$

Chapter 4

Filter design and resonance damping

4.1 VSC-attached passive filters

To attenuate the high switching frequency components generated by the converter, a filter is needed. The simplest possible solution is to place a large inductance in series with the converter. The filter is termed an L filter and has properties that greatly reduce the current harmonics around the switching frequency of the converter [14]. However, a big inductance will reduce the reaction time and the operational range of the converter. To improve system dynamics and further reduce costs and power losses connected to a large inductance, a capacitor can be placed in parallel. The capacitance of the LC-filter provides a low-impedance path for the high frequency current components and will greatly mitigate the content from the grid. High values of capacitance allows for a reduction in inductance, but can also arise concerns like high inrush currents and high capacitance current at the fundamental frequency [15]. If the grid impedance is assumed inductive, the LC filter can be perceived as an LCL filter with a varying grid side inductance[16]. A disadvantage of the LC-filter is the possibly strong coupling with grid parameters. The answer is to include another inductance in series with the grid forming an LCL filter. The grid side inductance protects the capacitance from large inrush currents at the point of common coupling. The LCL filter will then provide much of the advantages of the LC-filter and offer better decoupling between the filter performance and grid parameters. In power system applications, a transformer is often attached as the second filter inductance. Another advantage of the LCL filter compared to lower order filters is the added attenuation of frequencies above the cutoff frequency. The LCL filter provides 60 dB/decade attenuation compared to 40 dB/decade of the LC filter. The added attenuation allows for a lower range of PWM switching frequencies without complications of amplification in the cutoff frequency region. In this thesis, a low switching frequency (2 kHz) is used. At the same time, both weak and strong grid conditions are expected, consequently an LCL-filter is employed and further

discussed. However, more complex filter designs are proposed in literature based on traps with series resonances resulting in better switching frequency attenuation [17][18]. The main advantage of such typologies is the reduced size of the passive components at the cost of added complexity.

4.2 LCL-filter characteristics

The one phase electrical circuit of the LCL-filter is illustrated in Figure 4.1. R_{L_1},R_{L_2} and R_C are the internal resistances of the passive components, L_1, L_2 and C respectively.

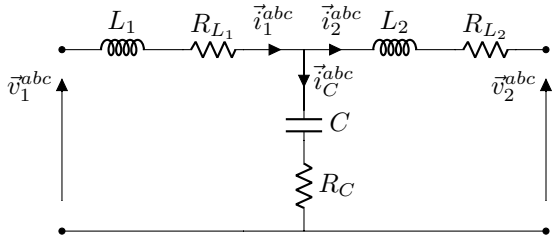


Figure 4.1: LCL-filter.

An important property to observe is how the filter input phase voltage, $\vec{v}_1^{abc}$ affects the output current, $\vec{i}_2^{abc}$. The transfer function then becomes as in Equation (4.1) with resonance frequency given by Equation (4.2). The transfer function is derived in the specialization project[1]. Other transfer functions can be obtained, and the key information they hold is the frequency location of the resonance.

$$\frac{\vec{i}_2^{abc}(s)}{\vec{v}_1^{abc}(s)} = \frac{sR_CC+1}{sL_1L_2C\Big(s^2+s\Big(\frac{1}{L_1}(R_1+R_C)+\frac{1}{L_2}(R_2+R_C)\Big)+(2\pi f_{res})^2\Big)+R_1+R_2} \tag{4.1}$$

$$f_{res} = \frac{1}{2\pi}\sqrt{\frac{1}{L_1C}+\frac{1}{L_2C}+\frac{1}{L_1L_2}(R_1R_2+R_1R_C+R_2R_C)} \tag{4.2}$$

With changing grid parameters, the resonance will be located at varying frequencies. The bode plot of the LCL-filter with varying L_2 is seen in Figure 4.2. Additional parameters are listed in Chapter 3. The resonance frequency is only limited by the very small internal resistance of the filter components. The resonance frequency is observed to be low under weak grid conditions($L_2 = 0.5pu$) and high under strong grid conditions($L_2 = 0.1pu$), 490 Hz and 604 Hz respectively. A good attenuation of the switching frequency of 2000 kHz is consequently obtained under all conditions. However, if the grid side inductance of the LCL-filter and the grid inductance becomes too low, the resonance peak will amplify distortion in the area of the switching frequency. On the contrary, if the grid side inductance of the LCL-filter and the grid inductance together becomes too high, the resonance frequency will fall into the low-frequency domain. Both cases require damping of the resonance peak further discussed in the next two sections.

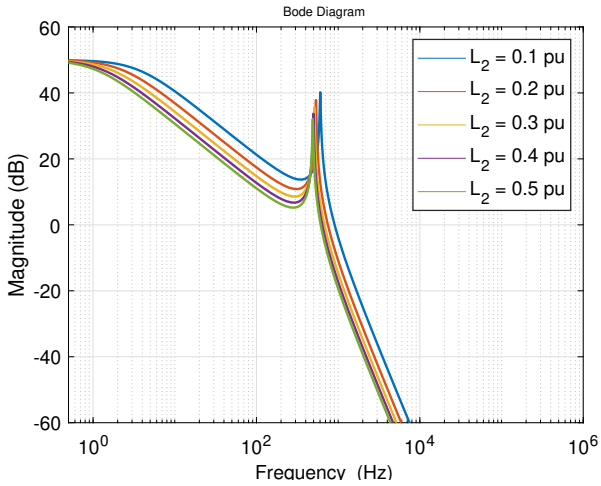


Figure 4.2: Bode Plot: LCL-filter with varying L_2.

4.3 Passive damping

A conventional and simple way to damp the resonance peak of the LCL-filter is to introduce resistance in the circuit. The resistance can either be placed in series or in parallel to the filter components. The most widespread method is to place the resistance in series with the filter capacitance[19].

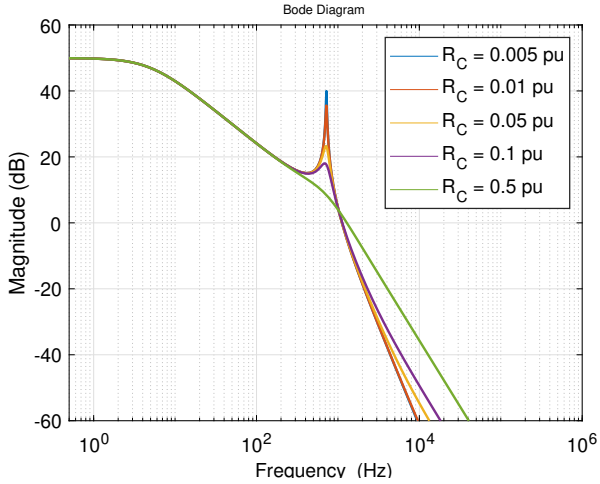


Figure 4.3: Bode Plot: LCL-filter with varying R_C.

Figure 4.3 illustrates the bode plot of the LCL-filter with varying capacitor series resistance R_C. Additional parameters are listed in Chapter 3. The added resistance offers a trade-off between better damping at the cost of increased power losses and worsened attenuation of the frequencies above the resonance. By connecting an inductance in parallel with the resistance, a low inductance path is made available for the low frequencies, and the power losses can be significantly reduced[20].

4.4 Active damping

For varying grid conditions, passive damping methods may not be sufficient. In this thesis, a wide range of grid inductance values are expected, and proper passive damping is not possible at all conditions. A more adaptable implementation of damping is obtain by introducing active damping. Active damping can be implemented as an add-on feature to power converters and can be especially effective by utilizing feedback information.

4.4.1 Virtual resistance

The main advantage of virtual resistance damping methods is to reduce losses connected to real resistance. The positioning of the virtual resistance is the same as for passive damping. The concept is explained in a simple way by first considering the passively damped LCL-filter block diagram of Figure 4.4.

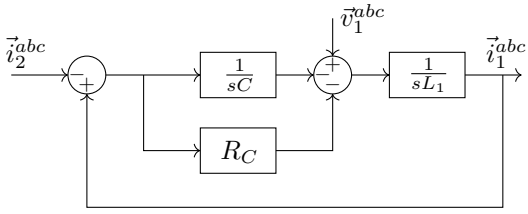


Figure 4.4: Block diagram: LCL filter with resistance(R_C) in series with the capacitance.

By removing the passive resistance, R_C of the original circuit, a similar damping behavior can be obtained by emulating the resistance with a feed-forward of the capacitor current in the control loop. The feed-forward term then becomes sCR_v, where R_v is the virtual resistance. The main disadvantage of a virtual resistance placed in series with the capacitor is the need for extra capacitor current sensors. If only the capacitor voltage measurement is available, the virtual resistance can be connected in parallel to the capacitor. Another solution is to utilize capacitor current or voltage estimation[21].

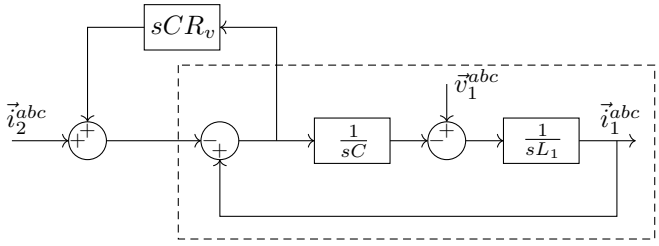


Figure 4.5: Block diagram: LCL filter with virtual resistance(R_v) in series with the capacitance.

Even though the virtual resistance behaves as a passive resistance, a fixed resistance value would have to fit all grid conditions. In theory, the virtual resistance could be changed in order to generate optimal damping under all grid conditions. In practical cases, this is not achievable due to the absence of such grid information.

4.4.2 Active damping based on filter capacitor voltage feedback

Oscillations occurring between the AC network and the filter capacitor are, in general, not controllable with inductor current feedback only. However, an additional control loop can be added to dampen the oscillations with either capacitor voltage or capacitor current feedback. Figure 4.6 illustrate the active damping circuit utilized in this thesis.

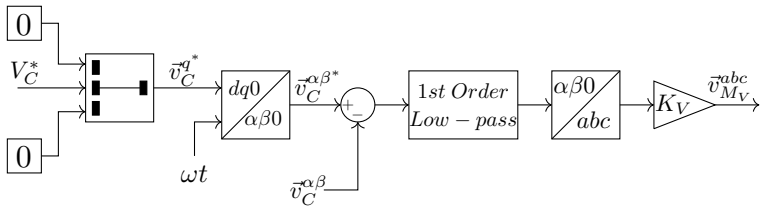


Figure 4.6: Capacitor voltage feedback active damping circuit.

The method extracts the oscillating components from the fundamental capacitor voltage and injects a compensating signal directly in the converter reference. With the capacitor voltage already available utilized in the main control system, no extra measurements are needed. The $\alpha\beta$ components of the capacitor voltage $\vec{v}_C^{\alpha\beta}$, is subtracted from its reference $\vec{v}_C^{\alpha\beta^*}$ and filtered through a first order low-pass filter. The converter reference voltage signal is obtained in abc-coordinates with a gain, K_V. Both the low-pass filter time constant and the gain are application dependent. In this thesis, good damping results was obtained with $K_V = 0.4$ and $\tau_{filter} = 0.02$.

Chapter 5

The control system

In this chapter, the control system will be evaluated under normal operating conditions. Normal operation in this context refers to individual control performance without considering a change in control mode. The performance of both the DC-side voltage control and the P-control is evaluated. The P-control is tested with the DC grid battery connected, whereas the voltage control is tested with the battery disconnected. The main objective is to obtain controller tuning parameters based on traditional tuning techniques and further discuss modifications to successfully operate within a wide range of grid impedance values. A reactive compensation strategy is further proposed and implemented to reduce the degree of overmodulation.

5.1 Control system setup and tuning

Figure 5.1 illustrates the control system setup, including the inner current control and two outer controllers. The two outer controllers are the DC side voltage control and the P-control. The outer controllers operate individually by sending a reference current $\vec{i}^{d*}_{1_{pu}}$, to the inner current control. Both the filter inductance current $\vec{i}^{abc}_{1_{pu}}$, and the capacitor voltage $\vec{v}^{abc}_{c_{pu}}$, are measured. They are transformed into the synchronous reference frame and filtered through a simple first order low-pass filter. Without proper low-pass filtering, high-frequency disturbance would pass through to the control system and cause immediate instabilities. The DC grid current $\vec{i}^{dc}_{pu}$ is utilized as a feed-forward in the voltage control for fast and more accurate voltage response. Further, the system phase angle is obtained by a PLL synchronized to the capacitor voltage. The closed loop active damping, represented by $\vec{v}^{abc}_{M_V}$, is added forming the modulation signal $\vec{v}^{abc}_{M}$. To obtain the final gate signal G^{abc}, a THIPWM is utilized.

When the main objective is to observe voltage transients due to the disconnection of the main DC grid voltage source, realistic time delays are important to obtain reliable results. The control system is consequently discrete, with a sampling rate of twice the converter switching frequency. In MATLAB/SIMULINK, this is obtained by placing the

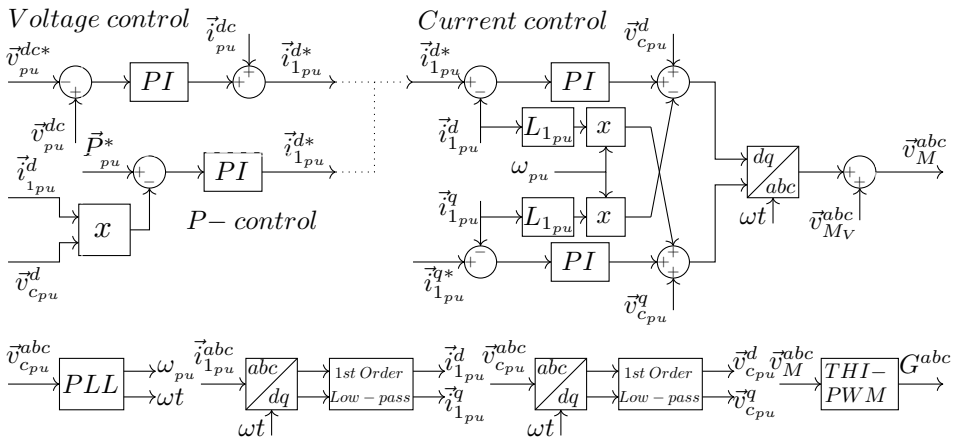


Figure 5.1: Converter control setup.

control system into a triggered subsystem block. The subsystem is then triggered every half period of the triangular carrier, $V_{tri} = -1$ and $V_{tri} = 1$. Every time the subsystem is triggered, new measurements are made available for the control system.

5.1.1 Main controller tuning

In theory, dynamically changing tuning parameters would be beneficial to adapt to different values of grid impedance. Fast operating controllers are desired and may work well under strong grid conditions. Weak grids demand a more relaxed control response for the system to remain stable. In the industry, the grid impedance is changing rapidly and can be hard to estimate. The simplicity and robustness of fixed tuning parameters are therefore highly valuable.

$Parameter$	$Value$
$K_{p_{ic}}$	0.2546
$K_{i_{ic}}$	6.6667
$K_{p_{Vdc}}$	5.9853
$K_{i_{Vdc}}$	572.96
K_{p_P}	0.8254
K_{i_P}	54.08

Table 5.1: Controller tuning parameters.

Controller tuning parameters are listed in Table 5.1. The inner current control parameters were obtained using the modulus optimum tuning criteria, and the outer voltage control parameters were obtained with the symmetrical optimum tuning criteria. The

phase margin was chosen to be 60° based on simulations. Both methods are previously described in Chapter 3. For the P-control, the parameters were determined solely based on simulation results.

5.1.2 Phase-locked loop tuning

The PLL used for grid synchronisation and the PLL used to obtain the THIPWM signal have the same gain parameters. The gains were obtained by simulation trial and erro and are listed in 5.2.

$Parameter$	$Value$
K_p	180
K_i	3200
K_d	1

Table 5.2: PLL tuning parameters.

5.2 Anti-Windup

Anti-Windup constrains the output of an integral controller. When a deviation between the controlled system variable and its reference set-point occurs, an error is passed to the controller. The integrator will then start to accumulate, and if the error persists over time, a concept termed integral windup occurs. Integral windup mainly arises as a limitation of physical systems, compared with ideal systems, where the reference set-point is physically not achievable. The control system is then no longer able to influence the physical system, and the controller output is steadily increasing or decreasing. If the system variable set-point is changed within reach of the physical system, the accumulated error will start to unwind by offsetting in the other direction. With a large time duration of the integral windup, the system will face significant delays in an attempt to reach the new reference set-point. Another undesirable effect of integral windup is introduced when a system variable reference is changed in a big step. The integral windup may then cause a large overshoot. Even with a small-signal, perfectly stable system, the system may now become oscillatory and even unstable.

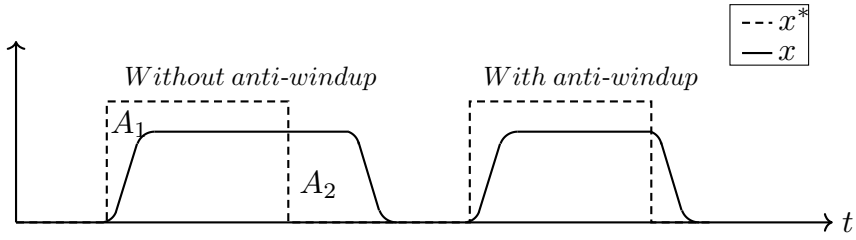


Figure 5.2: Example of control response with and without anti-windup.

There are different methods to implement anti-windup in the control system[22]. If the time instant for the integral-windup occurrence is observed, the integral controller output can be fixed to the value before the event. Another way would be to limit the integral term from accumulating above or below predetermined bounds or even disable the integral function. Figure 5.2 illustrates the concept of anti-windup. The control response is drawn by the solid line, whereas the dotted line represents the reference signal. Undergoing a step in reference, both the control system without anti-windup(left) and with anti-windup(right) react similarly. However, when the reference signal steps back down, the control response is different. Without anti-windup, the control action is delayed by the fact that the wound up area, represented by A_1, must be wound back down by means of the are A_2. In the case of anti-windup, the control system reacts immediately.

In applications where PI-controllers are used in the control of VSCs, the anti-windup function is particularly important. An example is when the controller steps into overmodulation, and the converter is unable to generate the desired output voltage or current in time. The result can be performance degradation in terms of oscillations or even instability. Figure 5.3 illustrates an anti-windup function implemented in a PI-controller. The back-calculation method limits the output of the controller and, at the same time, provides negative feedback to the integrator. The negative feedback prevents the integrator from winding up when the controller output signal exceeds the predefined upper and lower bounds.

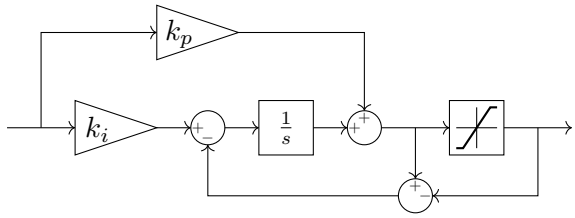


Figure 5.3: PI controller with anti-windup using back-calculation.

5.3 Overmodulation and power quality

Overmodulation occurs when the fundamental component of the control voltage exceeds the DC terminal voltage capacity. With no DC-to-DC converter present at the DC terminal, the VSC can be forced to operate with overmodulation in order to supply power from the DC to the AC grid with a fixed DC terminal voltage. This will cause undesired clipping of the voltage output and result in poor power quality at the AC terminal. Different low order harmonics of the AC fundamental voltage will emerge due to a reduction in the number of pulses generated by the modulator. Overmodulation must be limited due to the potential difficulties of removing low order harmonics. From a stability point of view, overmodulation is particularly unwanted due to the loss of gain in the controller. This concept is further discussed in Chapter 8. Overmodulation can be limited by reactive compensation.

5.4 Reactive compensation

Reactive power can be managed to improve the performance of the AC system. In general, this includes load compensation and voltage support. In applications where VSCs are prone to overmodulation due to a limited voltage supply, reactive power can be injected to lower the capacitor voltage, thus increase the voltage drop over the filter inductance. The solution will then assist the flow of active power and prevent overmodulation. This is possible due to the individual control of active and reactive power enabled by manipulation of the d- and q current components, respectively.

Figure 5.4 show a simple reactive compensation scheme. In the scheme, the d component of the modulation signal $\vec{v}_M^d$, is compared to a certain predefined upper limit $\vec{v}_{M_{lim}}^d$. Whenever the limit is reached, the controller injects reactive power to the AC grid by acting on the reference current $\vec{i}_{1_{pu}}^{q*}$. When the PI controller steps into operation, the integral action is reset to zero. This is to prevent unwanted transients when a potentially large accumulated error is unwound when the controller goes from inactive to active.

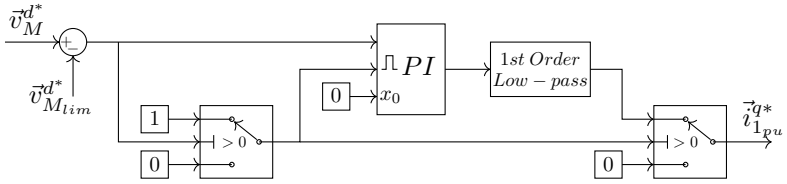


Figure 5.4: Reactive compensation circuit.

The controller parameters for the reactive compensation scheme was found by simulation trial and error, and are listed in 5.3. Different parameters were necessary for the two outer controllers. The modulation index upper limit $\vec{v}_{M_{lim}}^d$, was set to 1.18. This is when the modulation index is defined as unity at the end of the linear region of the THIPWM.

$Parameter$	$Value$
$K_{p_{Q,vdc}}$	1.465
$K_{i_{Q,vdc}}$	335.1
$K_{p_{Q,P}}$	0.366
$K_{i_{Q,P}}$	31.41

Table 5.3: Reactive compensation tuning parameters.

5.5 Simulation results

As it is rather difficult to obtain tuning parameters purely based on theoretical models, a simulation tool is valuable. By running simulations, the performance of the complete control system can be evaluated. This includes the current control, the voltage control, the P-control, the reactive power control, the active damping and the PLL. Properly chosen measurement filter parameters, as well as tuning of the PLL utilized in the THIPWM, proved to be critical from a stability point of view.

For precise control verification, a discrete simulation model was built in MATLAB/Simulink. The model can be seen in appendix B. A valuable control performance indicator is to apply a step in the controller reference. The step response demonstrates the response time, the response overshoot, and whether the system has robust stability properties. As the Thevenin inductance L_{th} $[pu]$ possesses values within 0.2 and 0.3 during normal operating conditions, the system response is verified with these parameters. This will also uncover the controller performance with respect to changing grid conditions.

5.5.1 P-control

A large step is applied to the reference of the P-controller. Figure 5.5 show the P-controller response when active damping and reactive compensation is included in the control system. The total rated active power is first, injected from the AC to the DC terminal, and secondly, from the DC to the AC terminal.

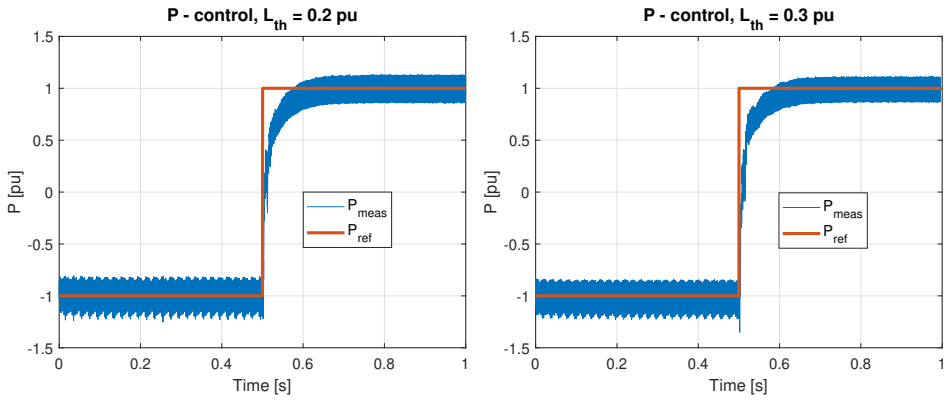


Figure 5.5: P-control step response.

The effectiveness of the active damping function is demonstrated. Figure 5.6 shows the controller step response when active damping is disabled. The step response is less smooth, containing more oscillating components. When the power is supplied from the AC terminal, the ripple has clearly increased. The ripple further increases with increasing grid Thevenin inductance.

Figure 5.7 shows the controller step response when reactive power compensation(Q-control) is disabled. The response time has increased with a controller now moving considerably into overmodulation. Overmodulation occur as the flow of active power is now

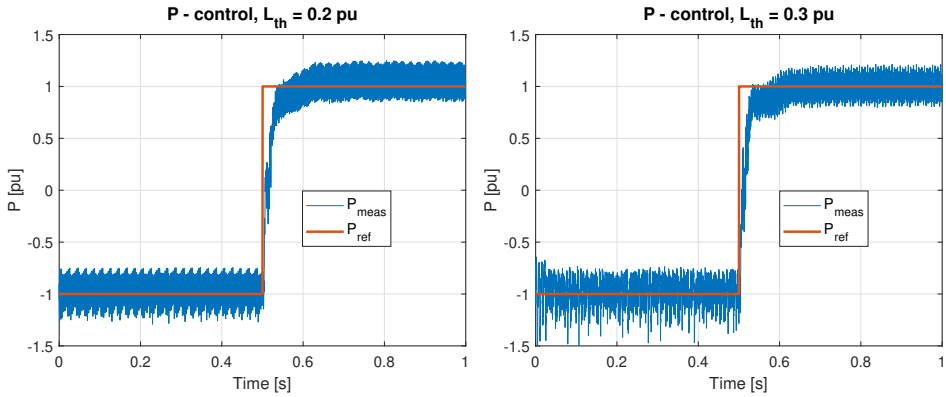


Figure 5.6: P-control step response with active damping disabled.

longer assisted by reactive power. The upper saturation limit of the d-axis current PI-controller has been reached, and anti-windup ensures a stable system with a constant slope of the rising curve. When the controller reaches its new reference point, a large overshoot, as well as subsequent oscillations occurs. Without anti-windup, the system becomes unstable.

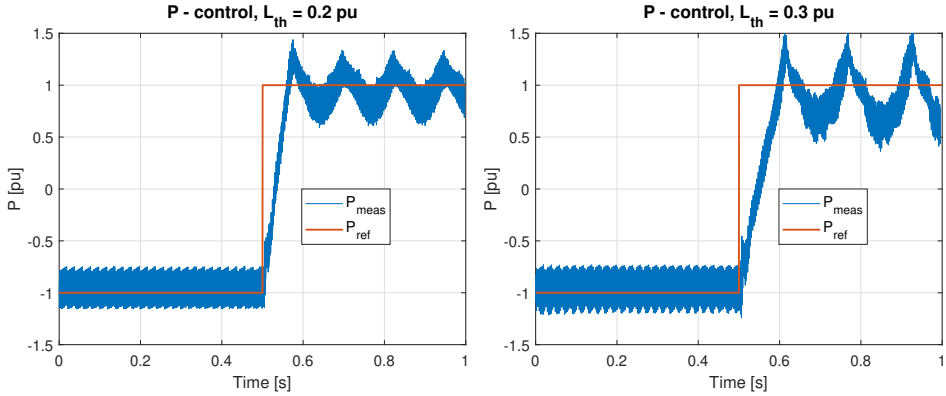


Figure 5.7: P-control with reactive compensation disabled.

5.5.2 Voltage control

A step is applied to the reference of the voltage controller. Figure 5.8 shows the response of the controller when active damping and reactive compensation is included. The voltage reference is changed from 0.9 to 1 pu. When the voltage control moves away from the point in which it is linearized(1 pu), the oscillations increases. Without reactive compensation, the controller becomes unstable with Thevenine inductances above 0.05 pu.

The effectiveness of the active damping function is demonstrated. Figure 5.9 shows

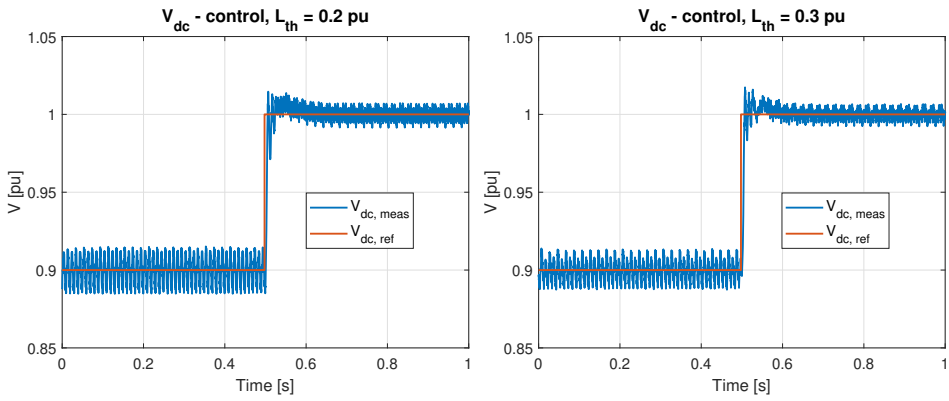


Figure 5.8: Voltage control step response.

the controller step response when active damping is disabled. The internal resistance of the passive components has a limited damping effect. The results are increased oscillations and an increased response time of the voltage. Active damping also has an advantage compared to passive damping strategies. Figure 5.10 shows the controller step response when passive damping is applied in terms of resistance added in series with the filter capacitor. The size of the damping resistance is, R_d = 0.1 pu. The passive damping resistance has reduced damping properties with increasing Thevenin inductance.

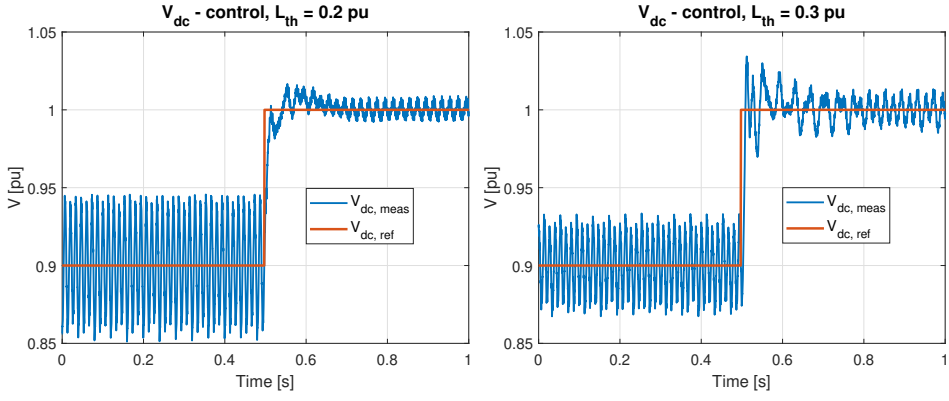


Figure 5.9: Voltage control step response with active damping disabled.

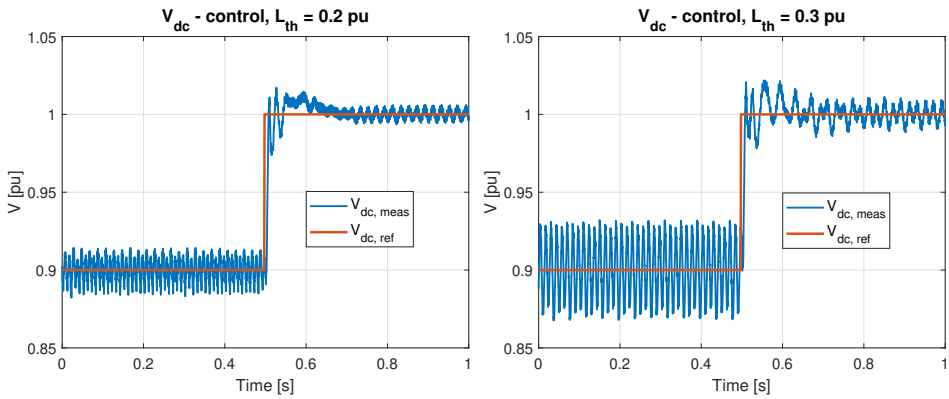


Figure 5.10: Voltage control step response with passive damping resistance in series with filter capacitor, $R_d = 0.1$ pu.

The voltage control performance is finally evaluated with a step in the DC grid current. The response is illustrated in Figure 5.11. The DC grid current is changing from -0.6 pu to 0.6 pu, which implies 0.6 pu active power produced and consumed by the DC grid, respectively. The voltage transient is increased with increasing Thevenin inductance.

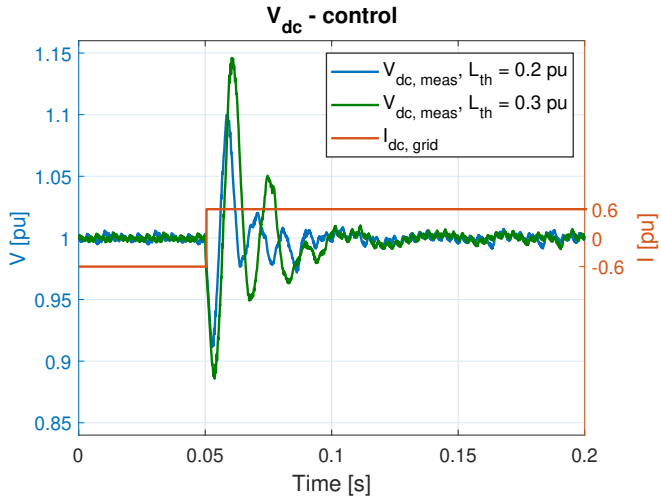


Figure 5.11: Voltage control with step in DC grid current.

5.6 Discussion

The control system was evaluated under normal operating conditions. Increased presence of oscillations occurs whenever the voltage deviates from 1 pu. This is because the control system has been linearized around this operating point. Further, reactive compensation has

shown to be vital from a stability point of view. In the voltage control mode of operation, the absence of reactive compensation cause immediate instability. In P-control, this leads to increased response time and oscillations whenever the power is transferred from the DC- to the AC grid. The response time and oscillations further increase with increasing grid impedance. This is due to the increased degree of overmodulation for increasing grid impedance. In the overmodulation range, there is a nonlinear relation between the fundamental component of the output line voltage and the control voltage of the converter. This can be interpreted as reduced controller gains causing under-damped behavior.

Passive damping has shown to have reduced damping effects with increasing grid impedance. This is because of the drop in the filter resonance frequency for increased grid side inductance. To ensure proper damping for weak grid conditions, the passive damping resistance can be increased. The effects are increased power losses and reduced filter effectiveness on switching frequency attenuation. This is because the added resistance blocks the low impedance path provided by the capacitor for high frequencies. The effect can also be interpreted when considering a bode plot of the filter transfer function. Increased damping resistance causes worsened attenuation of frequencies above the resonance. The results demonstrate the need for active damping, which has proven adaptable to grid changes.

Overmodulation has a negative impact on the power quality of the AC terminal. Even though reactive compensation is introduced, some degree of overmodulation must be tolerated in order to obtain sufficient power flow. With high levels of THD present, the next chapter will be dedicated to addressing this problem.

Chapter 6

Power quality

In this chapter, the power quality of the AC-terminal is being discussed. In Chapter 5, a reactive compensation strategy was presented as a method to lower the filter capacitor voltage and prevent overmodulation of the VSC. However, a certain degree of overmodulation must be tolerated to obtain sufficient power flow in the converter. In the overmodulation range, different low order harmonics will emerge and can potentially be removed. A voltage harmonic is a voltage waveform with frequency at a multiple of the fundamental voltage frequency. Different order harmonics can potentially cause multiple problems in the AC power system. This includes thermal overloading of rotating power system components, i.e. electrical motors or generators, and transformers as well as increased dielectric stressing[23]. Complications are increased maintenance costs, increased total power consumption, unreliable operation of electronic equipment, tripping of breakers and fuses, and failed capacitor banks. A voltage controlled selective harmonic compensation strategy is implemented in an attempt to attenuate harmonics caused by overmodulation.

6.1 Investigation of harmonic distortion

Total harmonic distortion(THD) is applied to quantify the quality of the AC terminal voltage. The THD is found using equation (6.1), where X_1 is the fundamental component and X_h is the h_{th} harmonic order of the fundamental.

$$THD = \frac{\sqrt{\sum_{h=2}^{\infty} X_h^2}}{X_1} \tag{6.1}$$

6.1.1 Voltage total harmonic distortion

Table 6.1 shows total harmonic distortion(THD) in the phase voltage at PCC with respect to Thevenin inductance, L_{th} $[pu]$ and active power, P $[pu]$. The THD increases with increasing Thevenin inductance and violates the allowable limit of 8% for L_{th} $[pu]$ above

0.05. Reactive compensation has shown to effectively limit the range of overmodulation and prevent THD from reaching levels above 11%.

$P\ [pu]$	$L_{th}\ [pu]$					
	0.05	0.1	0.2	0.3	0.4	0.45
1	5.32%	8.51%	10.20%	10.31%	9.78%	9.50%
0.5	5.27%	8.51%	10.37%	10.61%	10.67%	10.82%
0.25	5.35%	8.42%	10.45%	10.75%	10.80%	10.73%
0	5.41%	8.49%	10.28%	10.40%	10.12%	10.48%
−0.25	5.32%	8.58%	9.86%	9.97%	10.79%	10.58%
−0.5	5.37%	8.42%	10.41%	10.49%	10.33%	9.67%
−1	5.49%	8.54%	10.02%	10.01%	9.60%	9.68%

Table 6.1: THD of the voltage at PCC with respect to $P\ [pu]$ & $L_{th}\ [pu]$.

6.1.2 Frequency spectrum

The frequency spectrum of the power system voltage contains important information on the different order harmonics present. An important property is to observe whether some harmonic orders are particularly dominant and if they are consistent through different grid conditions and load variations. Overmodulation of power system converters may introduce different order harmonics at different degrees of overmodulation and can be hard to compensate. To decide if harmonic compensation is applicable, the frequency spectrum must be investigated for different grid conditions and power flows. The frequency spectrum of the voltage at the PCC with $P\ [pu]$ = 1 and $L_{th}\ [pu]$ = 0.2 is shown in Figure 6.10. The waveform of the voltage at PCC for the same case is shown in Figure 6.2.

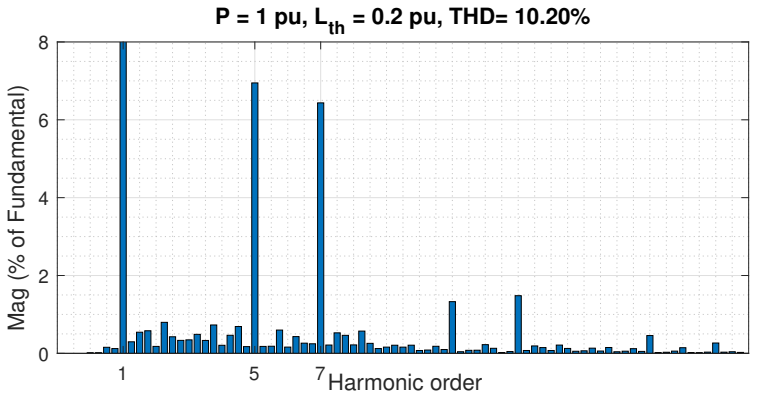


Figure 6.1: Frequency spectrum of the voltage at PCC with $P\ [pu]$ = 1 & $L_{th}\ [pu]$ = 0.2

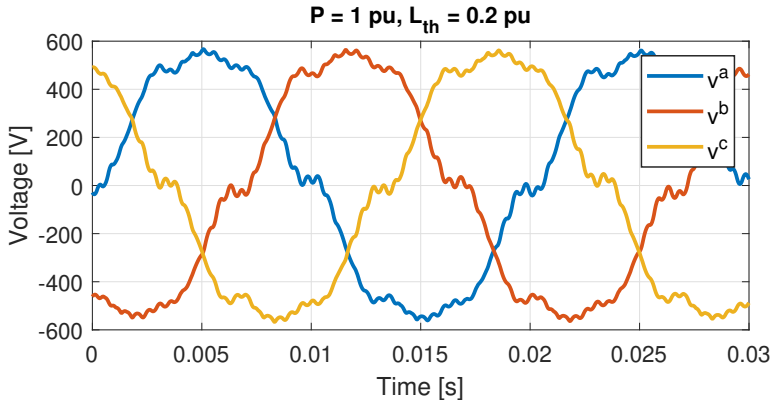


Figure 6.2: Voltage waveform at PCC with P $[pu]$ = -1 & L_{th} $[pu]$ = 0.3

Further, the frequency spectrum of the voltage at the PCC with P $[pu]$ = -1 and L_{th} $[pu]$ = 0.3 is shown in Figure 6.4. The waveform of the voltage at PCC for the same case is shown in Figure 6.5.

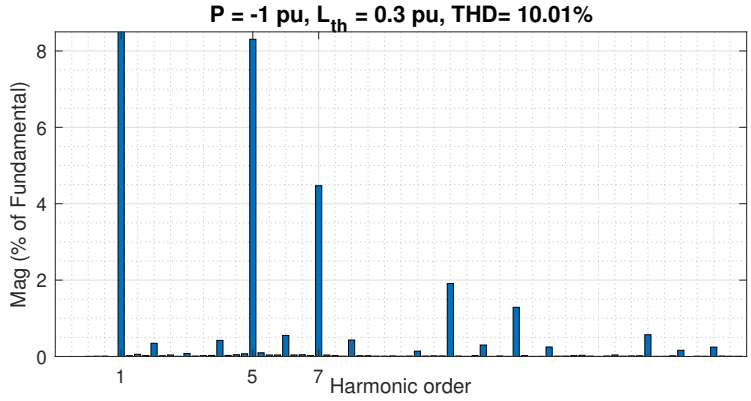


Figure 6.4: Frequency spectrum of the voltage at PCC with P $[pu]$ = -1 & L_{th} $[pu]$ = 0.3

When investigating the frequency spectrum of the different cases of power flow and grid conditions, given in Table 6.1, 5th and 7th order harmonics are present and the most dominant. Harmonic filters are consequently further discussed to compensate for the present voltage harmonics.

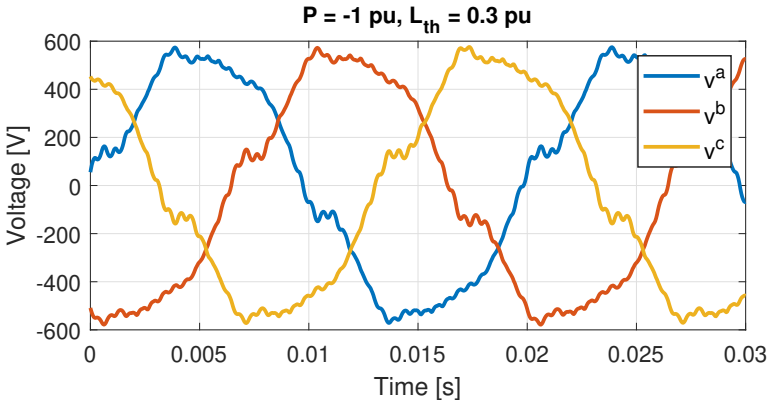


Figure 6.5: Voltage waveform at PCC with P $[pu]$ = -1 & L_{th} $[pu]$ = 0.3

6.2 Harmonic filters

Passive filters are extensively used to attenuate harmonics at PCC or at the connection point of distributed loads. Different filters are then individually tuned with capacitors, reactors, and resistors to handle different sets of harmonic orders. The solution is cost-effective, but has certain drawbacks. A particularly concerning problem occurs when a system resonance is located near a harmonic order[24]. A typical example is if an LC-filter is installed in shunt to attenuate harmonic currents from a disturbing load. Parallel resonance between the filter and the load will occur if the driving point impedance of a particular harmonic is increased. With passive filter components, the filtering property is not adaptive in case of changing grid parameters.

6.2.1 Active power filters

Active power filters(APFs) are good alternatives to passive filters. They utilize high frequency switched converters and have the ability to act as a harmonic current or voltage source. Solutions with both current source converters(CSCs) and VSC exist. In recent years, the VSC has been the preferred alternative due to steadily decreasing costs of semiconductor-based switches with reduced size and switching losses at high frequencies. The main advantage of APFs is the fast dynamic response as opposed to passive filters. In addition, APFs can obtain filtering at a different position than the point of connection. APFs can be connected in series or in shunt with the grid. If connected in series, the whole load current would have to pass through the filter and cause significant power losses. Consequently, shunt connected APFs are the most popular[25].

6.2.2 Integrated active filters

Integrated active filters(IAFs) is the concept of applying active filtering properties to an already existing power system converter. The solution is cost-effective as the necessary

system components already exist. The main drawback of utilizing an interlinking hybrid AC/DC converter to perform harmonic compensation is that large currents pass through the converter switches. Consequently, a low switching frequency must be chosen to reduce losses. The result is reduced bandwidth of the closed loop filter control.

6.3 VSC-integrated selective harmonic compensation

With 5th and 7th order harmonics visible in the phase voltage at the PCC, a selective harmonic compensation strategy is discussed[26]. Another method is broadband harmonic compensation used to compensate for a wide spectrum of harmonic orders [27][28]. To comply with marine power system regulations where the THD level needs to be less than 8%, focusing on compensating the 5th order harmonic is sufficient. In cases where the AC grid contains disturbing loads, canceling higher order harmonics would potentially be necessary. In this thesis, the focus will not be on finding optimal harmonic cancellation strategies, but to investigate if harmonic cancellation can be used in case of overmodulation. Figure 6.6 illustrates a voltage controlled IAF where the 5th order harmonic of the capacitor voltage $\vec{v}_C^{abc}$, is compensated. A more sophisticated implementation could focus on the voltage at PCC directly. The voltage at PCC would then have to be estimated or measured.

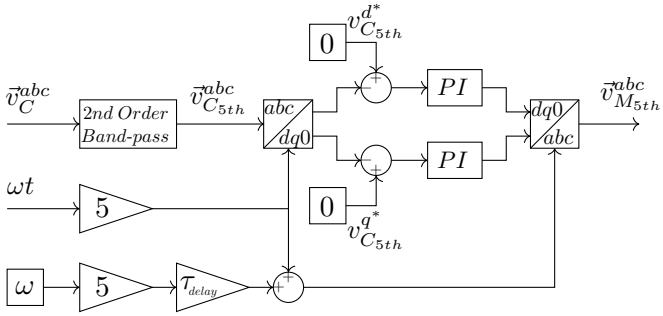


Figure 6.6: The VSC-integrated active filter.

Utilizing existing capacitor voltage measurements, the 5th order harmonic is extracted with a second order band-pass filter further explained in the next section. The voltage harmonic is transformed into the synchronous reference frame with an angular frequency of five times the fundamental. As the 5th order harmonic is a negative sequence harmonic, a negative sequence Park transform is utilized. The negative sequence Park transformation matrix is given in Appendix A. Further, the d- and q-components of the voltage are subtracted from its reference, in this case, zero. The error is passed to the PI controllers. The PI controller gains are transformed back to abc-coordinates with an added phase angle, $\omega 5\tau_{delay}$. The time delay τ_{delay}, include measurement processing, controller, and modulation delay. The phase angle is proportional to the harmonic order, and an exact estimation is consequently critical for the cancellation of higher order harmonics. A small error in the time delay estimation for high order harmonics will result in a large angular frequency

deviation. This will again lead to worsened compensation or even increase the presence of the harmonic component in the voltage. The time delay is estimated to be 0.495ms, which corresponds to a phase angle of $44.6°$ of the 5th order harmonic. Another way to align the compensating harmonic voltage in counter-phase to the original harmonic voltage is to introduce a time delay. A phase angle is subtracted, which leads to a slower time response. The final compensation strategy forms a closed loop system that can be incorporated as an add on feature to the original PWM signal.

6.3.1 The band-pass filter

In order to distinguish the 5th order voltage harmonic, a second order band-pass filter is utilized. A band-pass filter has the property to let a specific frequency through and thus block out all the others. Equation (6.2) show the transfer function of the band-pass filter.

$$H(s) = \frac{2\zeta\omega_c s}{s^2 + 2\zeta\omega_c s + \omega_c^2} \tag{6.2}$$

Figure 6.7 show the bode plot of the band-pass filter transfer function. The band pass-filter damping coefficient δ is chosen equal to 0.003, primarily based on simulation performance. In practical, no band pass filters are ideal, and the filter does not attenuate all frequencies outside the pass-band. The phenomenon is termed filter roll-off and is often expressed in dB of attenuation per decade. An accurate filter has a narrow roll-off, which is desirable. However, an accurate band-pass filter may come at the cost of band pass ripple.

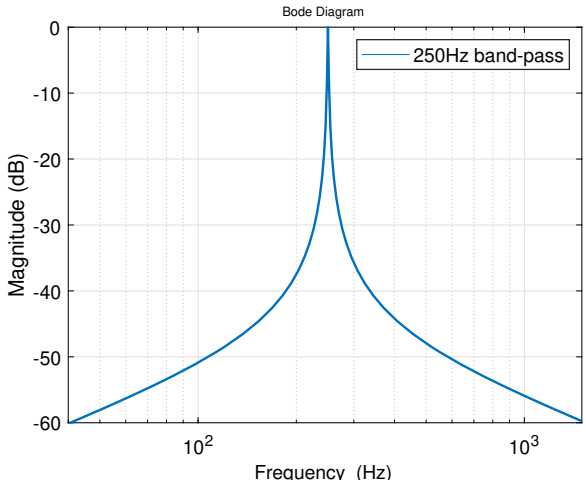


Figure 6.7: Second order band-pass filter.

6.4 Resulting harmonic distortion

6.4.1 Frequency spectrum

The resulting frequency spectrum of the voltage at PCC with $P\ [pu]$ = 1 and $L_{th}\ [pu]$ = 0.2 is shown in Figure 6.10. The waveform of the voltage at PCC for the same case is shown in Figure 6.2.

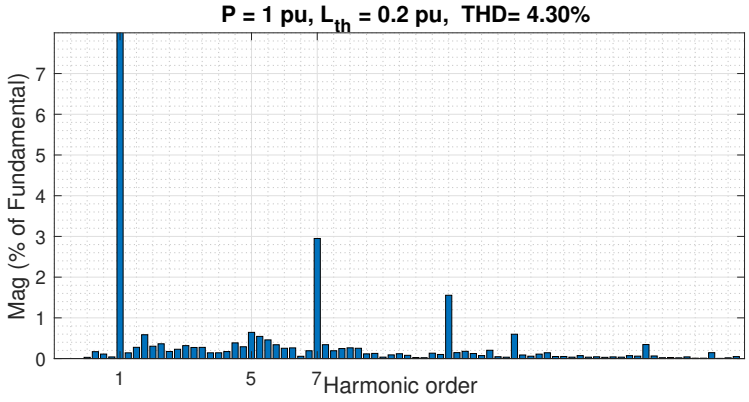


Figure 6.8: Frequency spectrum of the voltage at PCC with $P\ [pu]$ = 1 & $L_{th}\ [pu]$ = 0.2

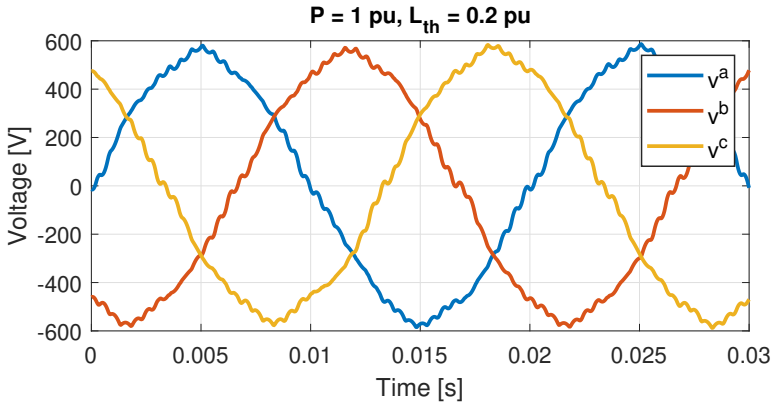


Figure 6.9: Voltage waveform at PCC with $P\ [pu]$ = 1 & $L_{th}\ [pu]$ = 0.2

Further, the resulting frequency spectrum of the voltage at PCC with $P\ [pu]$ = -1 and $L_{th}\ [pu]$ = 0.3 is shown in Figure 6.4. The waveform of the voltage at PCC for the same case is shown in Figure 6.5.

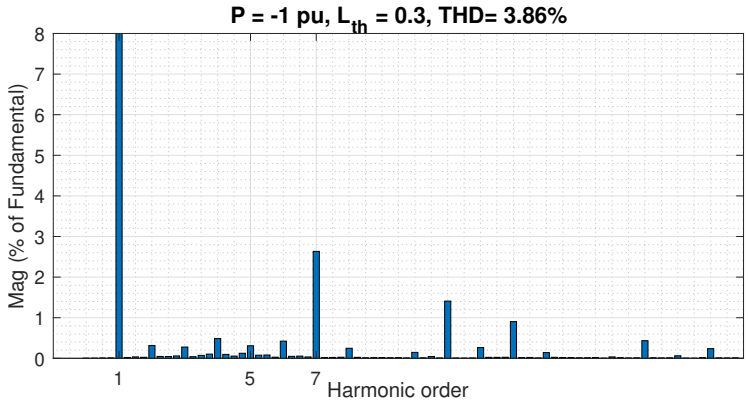


Figure 6.11: Frequency spectrum of the voltage at PCC with P $[pu]$ = -1 & L_{th} $[pu]$ = 0.3

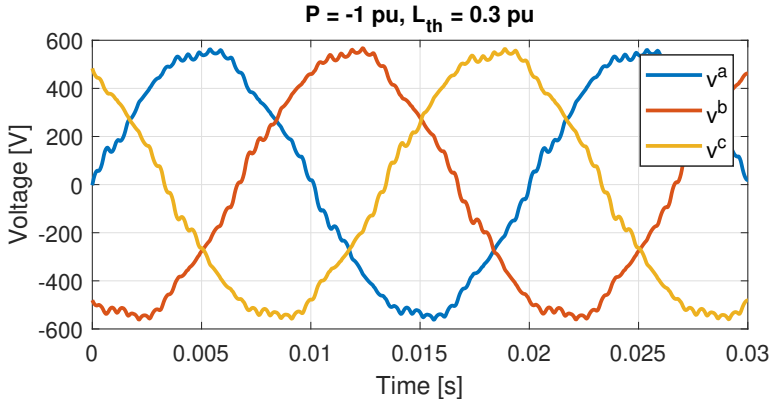


Figure 6.12: Voltage waveform at PCC with P $[pu]$ = -1 & L_{th} $[pu]$ = 0.3

6.4.2 Voltage THD with harmonic compensation

With the 5th order harmonic compensated in the capacitor voltage, almost complete attenuation is obtained in the voltage at PCC. The resulting voltage harmonic distortion at PCC is shown in Table 6.2.

$P\ [pu]$	$L_{th}\ [pu]$					
	0.05	0.1	0.2	0.3	0.4	0.45
1	2.28%	3.31%	4.30%	4.25%	3.49%	3.41%
0.5	2.86%	3.41%	4.50%	4.79%	4.90%	4.83%
0.25	2.67%	3.39%	4.69%	5.04%	5.10%	5.35%
0	2.33%	3.87%	4.81%	4.58%	5.02%	5.56%
−0.25	2.95%	3.75%	4.35%	5.27%	4.97%	5.87%
−0.5	3.20%	3.69%	4.46%	5.18%	5.01%	4.93%
−1	3.07%	3.46%	4.11%	3.86%	3.55%	3.65%

Table 6.2: Resulting voltage THD at PCC with respect to $P\ [pu]$ & $L_{th}\ [pu]$.

6.5 Discussion

The IAF has shown to effectively reduce the 5th order harmonic of the voltage at PCC. The filtering comes at the price of a small increase in converter and LCL-filter current. However, with no passive damping resistance present, the added losses are minimal. Figure 6.13 compares the voltage THD at the PCC with and without IAF.

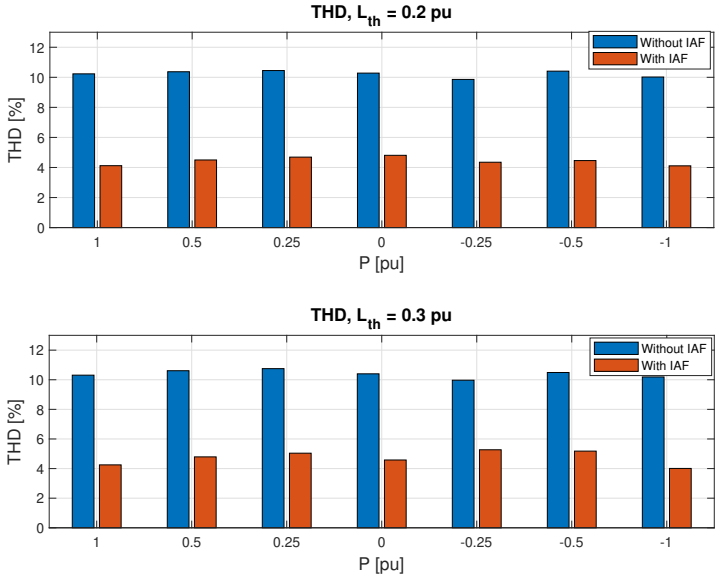


Figure 6.13: Resulting voltage THD at PCC with respect to $P\ [pu]$ & $L_{th}\ [pu]$

Chapter 7

Fault detection

Despite the hybrid marine power system is operating well under normal conditions, another aspect is how to respond to outages. In case the unit responsible for DC voltage control is disconnected, the interfacing converter must be able to react instantaneously by changing its operational mode. In this context, the change of operational mode is referred to as a change in control objective from P-control to DC voltage control. The DC grid forming responsibility is then put on the interfacing converter powered by the AC distribution system. The ultimate goal is to obtain a more robust power system that can withstand generation failure and maintain unaffected operation. In this thesis, the generation failure is represented by a disconnection of the battery. Figure 7.1 show the converter control setup.

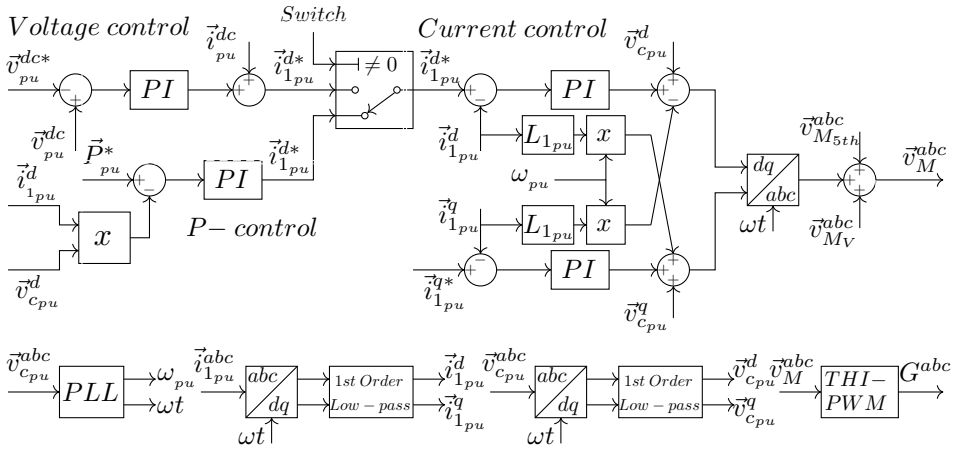


Figure 7.1: Converter control setup.

7.1 Fault detection methods

Proper fault detection techniques are crucial to fast and accurate decide if a change of control mode is necessary when the goal is to maintain the DC system voltage level within restricted boundaries. The sooner a fault event is identified, the easier it is for the system to return to a normal state. The offshore standard for electrical installations state a voltage tolerance of -15% to +30% of nominal DC system voltage[9]. The upper limit is set to protect power system components from damaging over-currents.

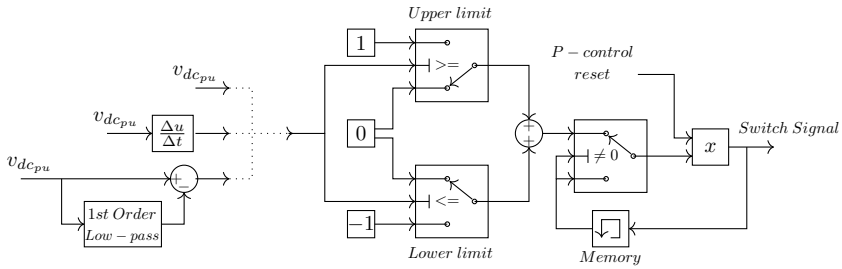


Figure 7.2: Fault detection scheme.

Figure 7.2 present three fault detection methods shown to the left in the figure. The simplest method is to compare the DC voltage $v_{dc_{pu}}$, to an upper and a lower threshold value. If the voltage is higher than the upper limit or lower than the lower limit, the switch signal receives 1 or -1, respectively. The scheme distinguishes between an upper and a lower voltage violation as the information becomes important later in Chapter 8. The voltage transient is then attempted limited with compensating controller action. Under normal operation conditions(P-control), the switch signal has the value zero. A memory block is included to prevent the switching from jumping back to P-control when the voltage level returns to the allowed voltage level area. To reset the switch, back to P-control, a short zero-pulse is fed to the memory block.

Another fault detection strategy is to consider the voltage derivative. The idea is to quickly detect abnormally fast drops or rises in the voltage level by comparing the derivative to a lower and an upper limit. With a DC grid consisting of battery power supplies only, the solution can be a quick alternative compared to the voltage level detection strategy. Potentially much less voltage deviation is necessary in order for the switch to be triggered. However, if the DC grid contains fast-acting generators, high voltage derivatives are always present, and fault events can not be distinguished by this method.

A third strategy is similar to the voltage level detection method. The difference is that the upper and lower limits now are dynamically changing. This can be realized by subtracting the low-pass filtered voltage measurement from the original measurement. If the output reaches predefined upper or lower values, which means that the voltage level has changed adequately during a short period of time, the switch is triggered. The boundaries are thus following the voltage level with a delay set by the filter time constant. A particular advantage of this method, compared to the voltage level detection method, is that it will allow a smaller upper and lower boundary interval and consequently reduce the voltage

deviation before the switch is triggered. In case of significant drifting of the voltage level, the method can potentially be combined with the first method to prevent the bounds from extending above or below the original fixed bounds.

7.2 Integrator reset

Controllers containing integral action have the property to accumulate the controller input error and effectively prevent a steady-state offset of the controlled system variable. When a controller containing integral action steps into operation, a reset of the integrator can be beneficial. The reset function erases the accumulated error of the integrator and replaces it with a selected value. This value can either be predefined or inherited from another controller. The method protects against transients caused by large accumulated errors when controllers go from inactive to active.

In applications where multiple controllers act interchangeably on the same system variable under different modes of operation, inheriting the integrator output from the previously active controller is favorable. This way, the system behavior becomes more predictable, and large transients can be avoided during change of control mode.

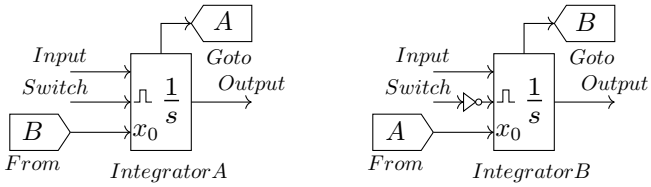


Figure 7.3: Integrator reset.

Figure 7.3 illustrates how the integral action is communicated between two controllers, A and B. In MATLAB/SIMULINK this is obtained by sharing an integrator state parameter. If the integrator output is shared directly, an algebraic loop will occur during startup as no output of integrator B is present when integrator A goes active. When no integrator output is present, the state parameter returns zero.

7.3 Impact of sampling time

In a discrete system, there is a time delay from measurements are made, sampled, and made available to the control system. When rapid changes occur in the system voltage, the sampled measurement becomes more inaccurate. In case the unit responsible for DC voltage control is suddenly disconnected, the voltage will either drop or rice with a slope decided by the magnitude and direction of the system power flow prior to the fault. Now, if the upper or lower acceptable voltage limit is reached, the sampling time becomes important in terms of the fault detection reaction time. With a steep voltage slope, a corresponding significant violation of the limits may occur before detection. The time delay from voltage violation until detection will vary in the range between zero and the sampling time τ_{samp}.

In discrete control systems with low sampling frequencies, a worst case scenario with fault detection reaction time equal to the sampling time should be considered.

7.4 Simulation results

Simulations were made to investigate the voltage transients when the battery source is disconnected. The VSC changes control mode from P-control to voltage control in order to maintain the voltage level. The transients were investigated with $L_{th}\ [pu]$ equal to 0.2 and 0.3 for different events of converter power transfer $P\ [pu]$. When fault detection was obtained using the voltage derivative, a large interval was necessary between the upper and lower limits. This was due to large values of voltage derivatives during power control mode of operation. As a direct consequence, the voltage derivative detection method proved to be slower than the more simple voltage level detection method.

Figure 7.4 and 7.5 show the voltage transients when the battery is disconnected with $L_{th}\ [pu]$ equal to 0.2 and 0.3 respectively. Fault detection was obtained with upper and lower voltage limits fixed equal to 1.1 and 0.95 pu respectively. When $P\ [pu]$ is positive, power is transferred from the the DC to the AC grid prior to the fault. Similarly when $P\ [pu]$ is negative, power is transferred from the the AC to the DC grid prior to the fault.

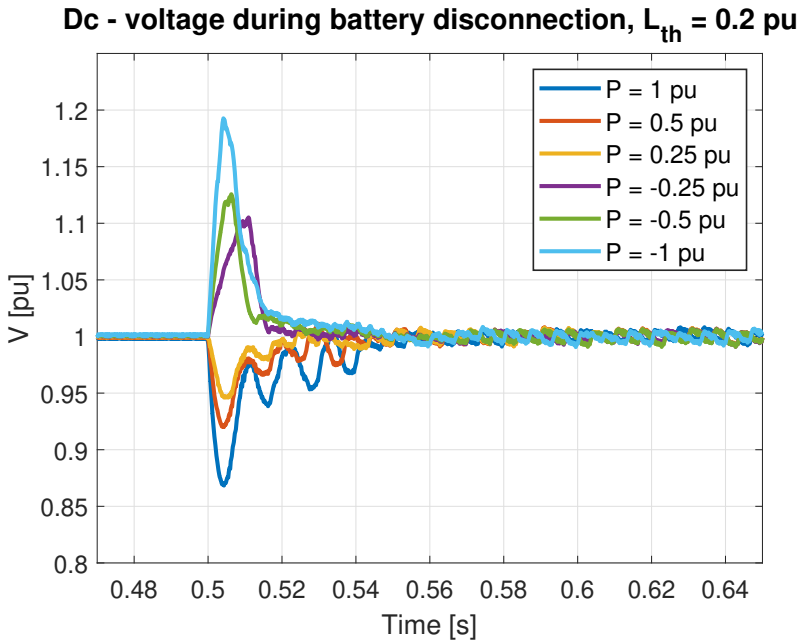


Figure 7.4: DC voltage during battery disconnection with $L_{th}\ [pu] = 0.2$

It is observed that the transient peak is increased with increasing $L_{th}\ [pu]$ and power transfer prior to the fault. The settling time from the battery is disconnected until the voltage is maintained within a 2% error band, is around 40 ms. The presence of oscillations

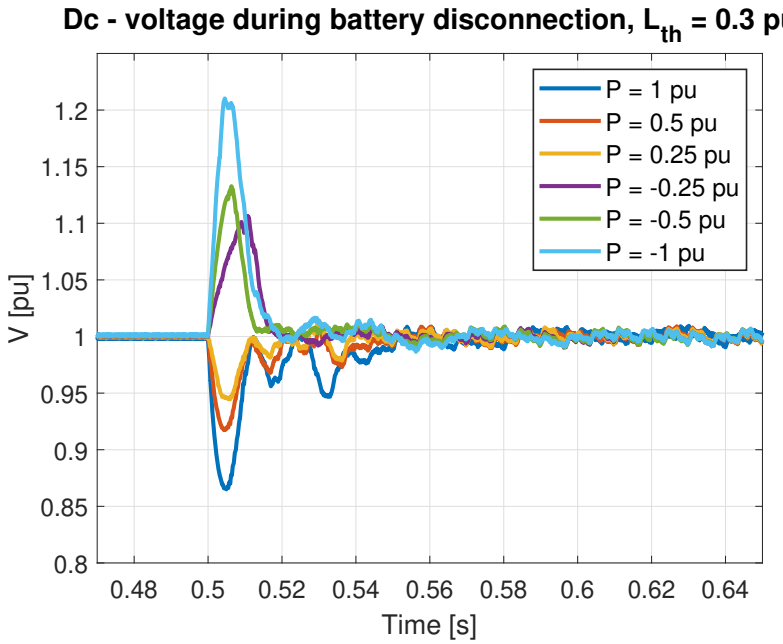


Figure 7.5: DC voltage during battery disconnection with $L_{th}\ [pu] = 0.3$

increases with increasing $L_{th}\ [pu]$.

7.5 Discussion

As the battery is the only unit responsible for DC voltage maintenance, a disconnection of the battery leads to an immediate voltage change. A sudden disconnection will cause the voltage to rise when the battery is preliminary charged with power from the AC grid. The voltage rise occurs as the charging current now flows to the DC grid capacitor. The capacitor voltage starts to build up with a slope determined by the current or power delivered to the battery prior to the fault. If the battery is oppositely delivering power to the grid, a voltage drop will occur. The current or power is then supplied from the DC grid capacitor to the AC grid.

When discussing fault detection strategies, the voltage derivative method proved to be slower than the voltage level detection method. This is due to the low sampling frequency. When the sampling frequency is increased, the upper and lower limits can be decreased. It is worth mentioning that if the power system would have fast-acting gen-sets, the voltage derivative detection method is unsuitable regardless of the sampling frequency. Voltage detection with dynamically changing voltage limits can further reduce the fault detection time if the DC voltage is prone to drifting. The otherwise fixed boundaries would then have to be increased to prevent fault detection caused by drifting. When a battery is responsible for DC voltage maintenance, no such drifting will occur and the allowed voltage level

interval can be small.

The sampling time delay brings a small variation in the magnitude of the transient voltage peak. If maximum power is transferred from the AC to the DC grid with $L_{th}\ [pu] = 0.3$, the result is roughly 0.005 pu when the time from voltage level violation to detection varies from 0 to τ_{samp}. The small variation is not relevant in further discussion of the proposed change of control mode presented in chapter 8.

Chapter 8

Proposed VSC control strategies for reduced voltage transients

In Chapter 7, the VSC changes control mode from P-control to voltage control in order to maintain the DC voltage level when the battery source is disconnected. In this chapter, methods to reduce the voltage transient and recovery time undergoing fault is proposed. The magnitude of the transient is determined by the time duration of the fault detection, the power flow prior to the fault, the grid side impedance, and the control system. Now, with fault detection already discussed, the next step is to improve the control system. The idea is to maximise the power transfer potential and still stay within power system regulations in case of battery disconnection. The grid impedance is expected unknown, and both weak and strong grid conditions must be considered.

8.1 Transient controller reference

When the main unit responsible for voltage control is disconnected, a fast recovery of the voltage level can be obtained by introducing transient references in the control system. The idea is to rapidly reverse the power flow and thus fast limit the voltage transient from reaching unacceptable levels. The concept can be particularly useful to compensate for slow operating control systems. Transient references can be introduced in both the voltage and current controllers. Figure 8.1 illustrate the control scheme where the transient current references $\vec{i}^{d^*}_{t_{pu}}$ and $\vec{i}^{q^*}_{t_{pu}}$ are added to the original current references.

The gain k, and time duration τ_t, of the transient current references must be selected with care taking into account the power flow prior to the fault. The d-axis current will assist the power flow directly, whereas the q-axis current will provide fast reactive compensation. With unknown grid parameters, both weak and strong grid conditions need to be considered. Different shapes of the transient reference can be an impulse or a step that is ramped back.

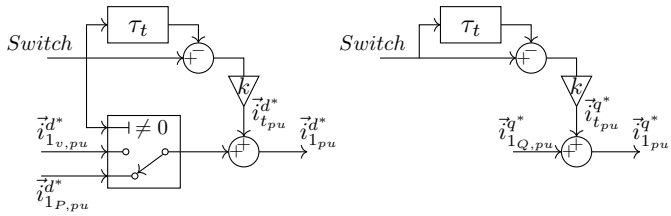


Figure 8.1: Transient current reference control scheme.

8.2 Controller gain compensation in the overmodulation range

The VSC is operating in the linear region whenever the fundamental component of the control voltage is equal to the fundamental component of the AC output voltage. This holds for control voltage amplitudes at a maximum of $0.5V_{dc}$ for the SPWM and about $1.15 \cdot 0.5V_{dc}$ for the THIPWM. When the fundamental component of the output voltage exceeds these values, the VSC is operating in a state of overmodulation where the fundamental component of the output voltage is smaller than the fundamental component of the control voltage. This can be interpreted as a reduced gain of the control system.

Reduced controller gain in the overmodulation range is particularly unwanted during voltage transients. The system is then often forced into overmodulation in order to quickly obtain voltage stability. Lowered controller gains will reduce the response time and potentially cause oscillations. In the literature, various attempts have been made to estimate and followingly compensate for the loss of controller gain in the overmodulation region[29][30]. The methods are based on Fourier analysis of the fundamental output voltage component with respect to the control voltage.

Whenever the THIPWM technique is utilized, the over-modulation range is divided into two regions[29]. The first region starts when the control voltage signal exceeds the amplitude of the triangular carrier. Saturation will then occur every quarter period due to the added third harmonic component. The second region starts when the control voltage signal significantly exceeds the amplitude of the triangular carrier so that saturation occurs every half period. Finally, if the carrier voltage signal increase towards infinity, a six-step operation will occur with maximum fundamental output voltage equal to $\frac{2}{\pi}V_{dc}$.

Accurate estimations of the controller gains with respect to the modulation index can be obtained by evaluating the two aforementioned overmodulation regions. If a discrete control system is utilized with low sampling frequencies, such estimations are insufficient. Figure 8.2 illustrates this concept showing a SPWM signal and its corresponding THIPWM signal. The sampling frequency is 4000Hz. The shapes are far from the theoretical modulation signals that are the basis for the estimations.

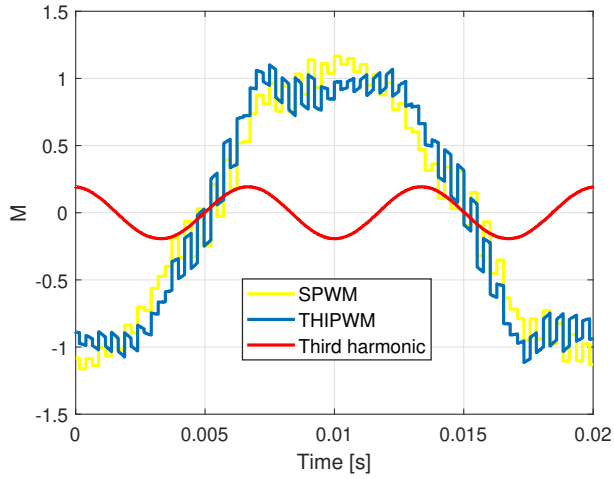


Figure 8.2: Modulation signal.

To obtain more accurate estimations of the gain reduction in the overmodulation range, simulations were made in MATLAB/Simulink. The fundamental component of the converter output line voltage was found with respect to a change in the modulation index. The fundamental component f(t) of a periodic signal can be found based on Fourier analysis expressed by Equation (8.1). The fundamental component of the voltage is calculated over a running window of one cycle of the fundamental frequency, $T = \frac{1}{f_0}$.

$$f(t) = acos(\omega_0 t) + bsin(\omega_0 t) \tag{8.1a}$$

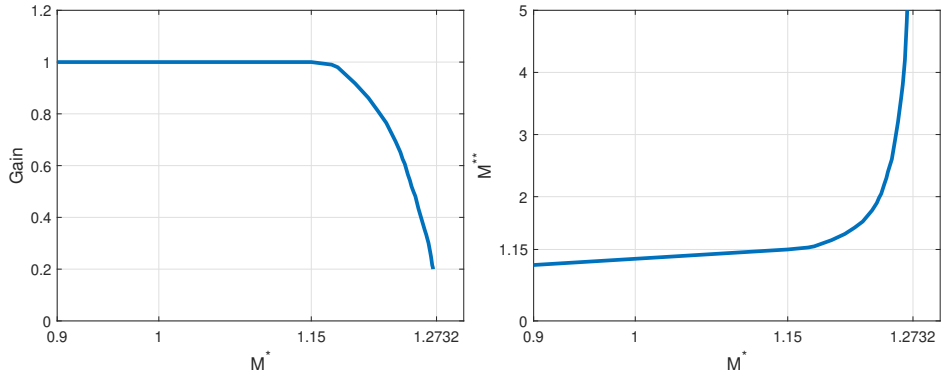
$$a = \frac{2}{T}\int_{t-T}^{t} f(t)cos(\omega_0 t)dt \tag{8.1b}$$

$$b = \frac{2}{T}\int_{t-T}^{t} f(t)sin(\omega_0 t)dt \tag{8.1c}$$

The magnitude of the fundamental is further calculated by Equation (8.2).

$$Magnitude = \sqrt{a^2 + b^2} \tag{8.2}$$

Figure 8.3a show the normalized converter gain with respect to the modulation index $M^* = \hat{V}_{out}/0.5V_{dc}$. M^* is defined as the magnitude of the fundamental output phase voltage divided by half the DC terminal voltage. Utilizing THIPWM, the gain is unity up to M^* = 1.15 and decreases towards zero when M^* reaches its maximum value of $\frac{2}{pi} \approx 1.2732$.



(a) Normalized gain with respect to M^*.

(b) Compensated modulation index.

Figure 8.3: Normalized gain and compensated modulation index with respect to M^*.

Figure 8.3 shows the transfer function M^{**}/M^*, where M^{**} is the compensated modulation index. The function has an inverse relationship compared to Figure 8.3a in order to compensate for the gain losses. The result is a new modulation index which linearizes the converter in the overmodulation range. Figure 8.4 illustrates the control scheme where the original modulation index M^* is transformed to the compensated modulation index M^{**} .

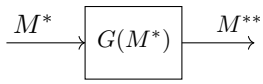


Figure 8.4: Converter gain compensation scheme.

8.3 Simulation results

Simulations were made to investigate the voltage transient during battery disconnection. The simulation model is shown in Appendix B. The simulation sample time is

$$\tau_{sample} = 1 \cdot 10^{-6} s \tag{8.3}$$

8.3.1 Controller gain compensation in the overmodulation range

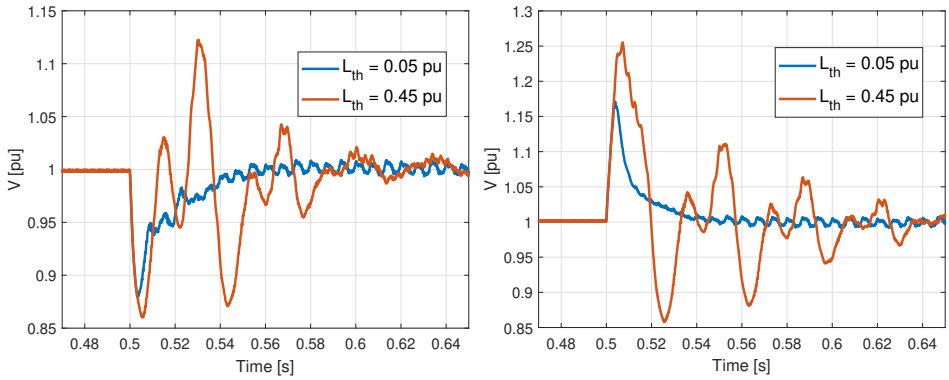
Gain compensation in the overmodulation range was introduced by including a lookup table in MATLAB/Simulink. The lookup table holds the values shown in Figure 8.3b. The modification resulted in immediate instability of the system. To further investigate if gain compensation has the potential to improve system performance, more moderate compensation were applied in terms of small linear gain increase in the overmodualtion range. Simulations show that, when the control system moves into overmodulation after battery disconnection, the added gain limits the transient. However, with a fast maintenance of the voltage, subsequent oscillations occur which vorsen the situation.

8.3.2 Transient current reference

Three different cases were investigated introducing transient current reference. The reference has the shape of an impulse. The first case with constant time duration τ_t, and varying magnitude $\vec{i}^{d^*}_{t_{pu}}$ or $\vec{i}^{q^*}_{t_{pu}}$. The second case with constant magnitude and varying time duration. The final case proposes an optimal combination of the impulse magnitude and time duration in terms of resulting voltage deviation at all grid conditions. Since the converter switches and other components have limited current tolerance, the converter current must be considered. The time duration of the reference needs to be at a multiple of the sampling time τ_{samp}.

Since the transient current reference can be adjusted relative to the power flow prior to the fault, the study will focus on the worst-case scenario which is for maximum power flow. As grid conditions are unknown, the transient reference must be selected considering a wide range of grid parameters. The cases were consequently run with extreme grid conditions,i.e $L_{th}\ [pu]$ equal to 0.05 and 0.45. If good performance can be obtained with these values, good performance is expected for all conditions. The upper and lower voltage limits in terms of fault detection are 1.1 and 0.95 pu, respectively. The large allowable voltage level area is chosen to tolerate fast acting gen-sets present in the power system.

Figure 8.5a and 8.5b show the voltage transient for weak grid conditions($L_{th}\ [pu] = 0.45$) and strong grid conditions($L_{th}\ [pu] = 0.05$) with $P\ [pu]$ equal to 1 and -1 prior to the fault respectively. They will be the basis to determine the effectiveness of the different case scenarios. With $P\ [pu]$ = 1, the voltage transient reach 0.88 and 0.86 pu during strong and weak grid conditions respectively. Whit $P\ [pu]$ = -1, the voltage transient reach 1.17 and 1.26 pu during strong and weak grid conditions respectively.



(a) $P\ [pu] = 1$ **(b)** $P\ [pu] = -1$

Figure 8.5: DC voltage during battery disconnection.

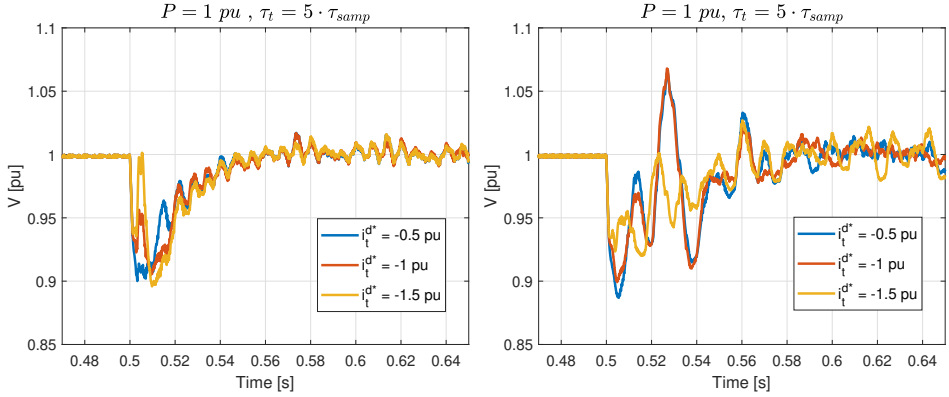
Case 1: Varying magnitude $I_{t_{pu}}^{d^*}$ and $I_{t_{pu}}^{q^*}$

This case investigates the voltage transients when the time duration of the reference impulse is fixed, whereas the magnitude is varied. A transient impulse in $\vec{i}_{t_{pu}}^{d^*}$, has proven its effectiveness to force the voltage back up after a voltage drop. However, if the voltage is oppositely rising, the converter moves into overmodulation. A large positive reference current is then needed to force the voltage back down due to the loss of gain in the overmodulation range. Such a large current reference has proven to be unpredictable in terms of resulting voltage behavior and exposure to over-currents in the converter. A much more effective and predictable solution is to introduce a positive transient impulse in $\vec{i}_{t_{pu}}^{q^*}$. This provides temporary reactive compensation in terms of reactive power delivered to the AC grid. The filter capacitor voltage is consequently lowered, and the flow of active power is assisted.

Figure 8.6a shows the voltage transient during strong grid conditions when rated active power is transferred from the DC- to the AC grid prior to the fault. The reference impulse lasts for five sampling periods. It can be seen that the current $\vec{i}_{t_{pu}}^{d}$ is quickly forcing the voltage to rise and consequently reducing the peak of the transient. However, with increasing magnitudes, the voltage has a tendency to experience a second drop when the reference impulse ends. The converter current is measured at a maximum value of 1.5 pu during the transient with $\vec{i}_{t_{pu}}^{d^*}$ = -1.5. Figure 8.6b shows the voltage transient for the same case during weak grid conditions. A large current reference magnitude is seemingly beneficial to reduce the transient peak. The converter current is measured at a maximum value of 1.35 pu during the transient with $\vec{i}_{t_{pu}}^{d^*}$ = -1.5.

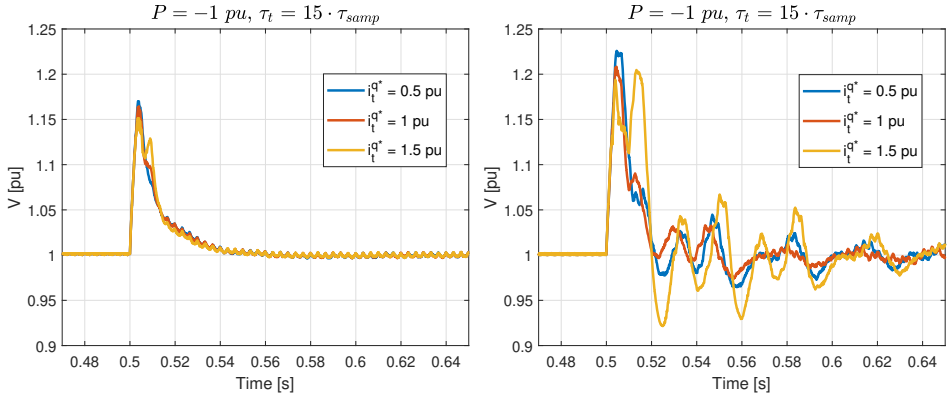
Figure 8.7a shows the voltage transient during strong grid conditions when rated active power is transferred from the AC- to the DC grid prior to the fault. The reference impulse lasts for fifteen sampling periods. The time duration of the q-axis current impulse is chosen larger than the time duration of the d-axis current impulse to obtain equally good transient attenuation. It can be seen that the current $\vec{i}_{t_{pu}}^{q}$ is effectively reducing the peak of the transient. The converter current is measured at a maximum value of 1.4 pu during

the transient with $\vec{i}^{q^*}_{t_{pu}}$ = -1.5. Figure 8.7b show the voltage transient for the same case during weak grid conditions. A large current reference magnitude is seemingly beneficial to reduce the transient peak. However, with increasing magnitudes, the voltage tends to experience a second rise. The converter current is measured at a maximum value of 1.2 pu during the transient with $\vec{i}^{q^*}_{t_{pu}}$ = -1.5.



(a) $L_{th}\ [pu]$ = 0.05 **(b)** $L_{th}\ [pu]$ = 0.45

Figure 8.6: Varying magnitude $\vec{i}^{d^*}_{t_{pu}}$.



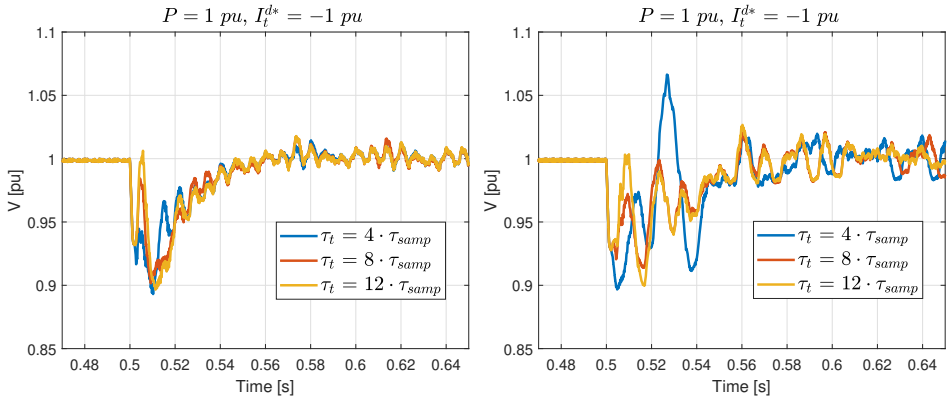
(a) $L_{th}\ [pu]$ = 0.05 **(b)** $L_{th}\ [pu]$ = 0.45

Figure 8.7: Varying magnitude $\vec{i}^{q^*}_{t_{pu}}$.

Case 2: Varying time duration τ_t

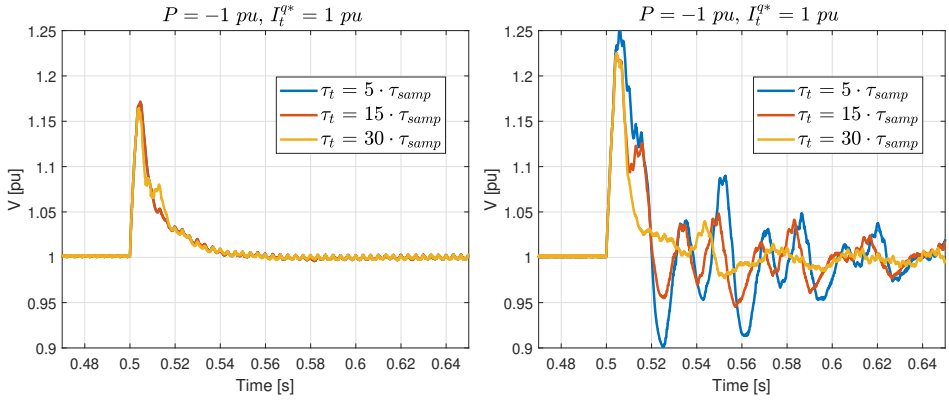
This case investigates the voltage transients when the magnitude of the reference impulse is fixed, whereas the time duration is varied. Figure 8.8a shows the voltage transient during strong grid conditions when rated active power is transferred from the DC- to the

AC grid prior to the fault. The reference impulse has a magnitude of -1 pu. It can be seen that increasing the time duration of the current $\vec{i}^{d}_{t_{pu}}$ has similar effects as increasing the magnitude. With increasing time duration, the voltage has a tendency to experience a second drop. The converter current is measured at a maximum value of 1.5 pu during the transient with $\tau_t = 12 \cdot \tau_{samp}$. Figure 8.8b shows the voltage transient for the same case during weak grid conditions. The converter current is measured at a maximum value of 1.35 pu during the transient with $\tau_t = 12 \cdot \tau_{samp}$.



(a) $L_{th}\ [pu]$ = 0.05 **(b)** $L_{th}\ [pu]$ = 0.45

Figure 8.8: Varying time duration τ_t.



(a) $L_{th}\ [pu]$ = 0.05 **(b)** $L_{th}\ [pu]$ = 0.45

Figure 8.9: Varying time duration τ_t.

Figure 8.9a shows the voltage transient during strong grid conditions when rated active power is transferred from the AC- to the DC grid prior to the fault. The reference impulse has a magnitude of 1 pu. It can be seen that increasing the time duration of the current $\vec{i}^{q}_{t_{pu}}$ has similar effects as increasing the magnitude. The converter current is measured

at a maximum value of 1.45 pu during the transient with $\tau_t = 30 \cdot \tau_{samp}$. Figure 8.9b show the voltage transient for the same case during weak grid conditions. The voltage is forced to drop. The converter current is measured at a maximum value of 1.35 pu during the transient with $\tau_t = 30 \cdot \tau_{samp}$.

Case 3: Proposed transient current reference

This case proposes an optimized combination of time duration and magnitude of the transient current reference impulse. The voltage transients are minimized with respect to a maximum tolerated converter current of 1.4 pu. Figure 8.10 shows the voltage transient for different grid conditions when rated active power is transformed from the DC- to the AC grid prior to the fault. Figure 8.11 shows the resulting voltage transient when a d-axis transient current reference impulse is added. The impulse has a magnitude of 1.2 pu lasting for five sampling periods. The peak of the voltage transient is effectively reduced for all grid conditions with a maximum voltage deviation of 9%. From the stage of fault detection at 0.95 pu voltage, the voltage violation is reduced by 50%.

Figure 8.12 shows the voltage transient for different grid conditions when rated power is transformed from the AC- to the DC grid prior to the fault. Figure 8.13 shows the resulting voltage transient when a q-axis transient current reference impulse is added. The impulse has a magnitude of 1.3 pu lasting for fifteen sampling periods. The peak of the voltage transient is effectively reduced for all grid conditions with a maximum voltage deviation of 19%. From the stage of fault detection at 1.1 pu voltage, the voltage violation is reduced by 43%.

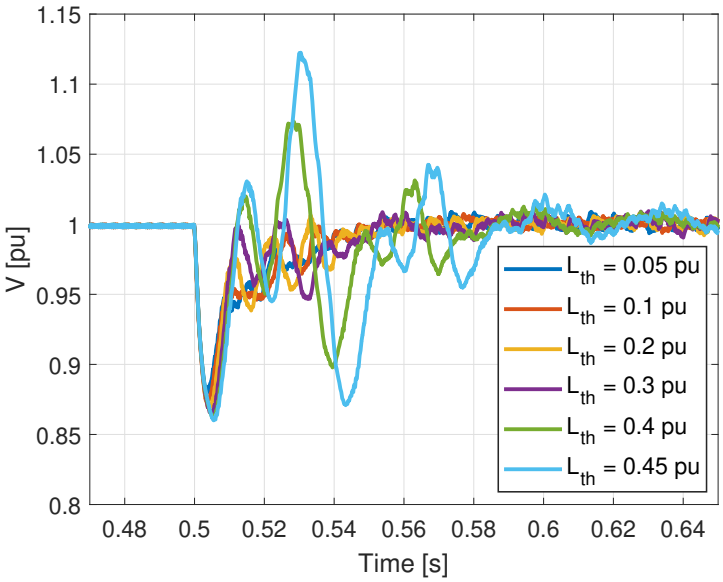


Figure 8.10: DC voltage during battery disconnection with $P\ [pu] = 1$

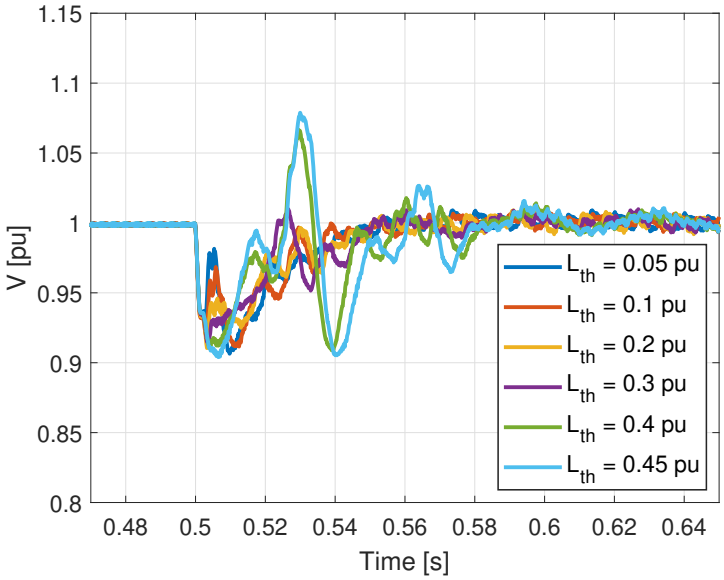


Figure 8.11: DC voltage during battery disconnection with $P\ [pu] = 1$, $\vec{i}^{q^*}_{t_{pu}} = 1.2$, $\tau_t = 5 \cdot \tau_{sample}$.

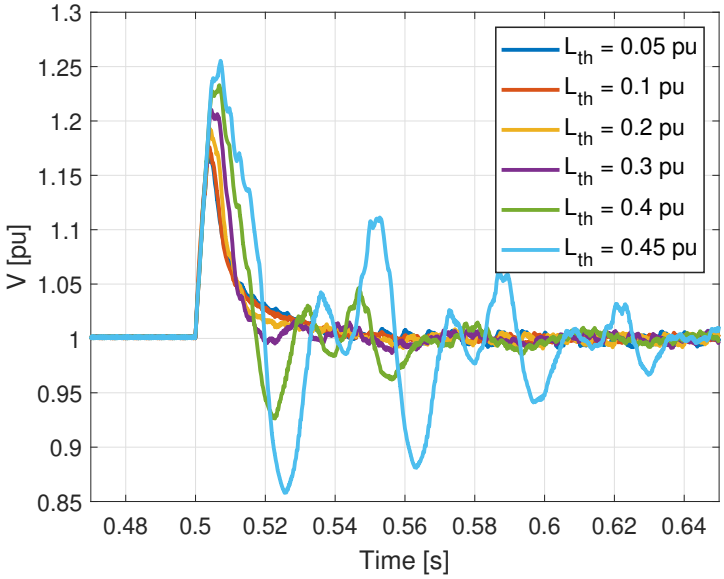


Figure 8.12: DC voltage during battery disconnection with $P\ [pu] = -1$

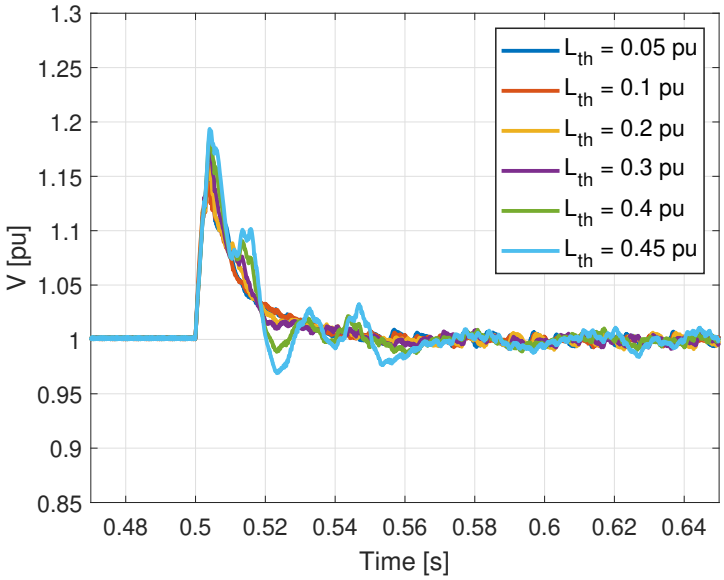


Figure 8.13: DC voltage during battery disconnection with $P\ [pu]$ = -1, $\vec{i}^{q^*}_{t_{pu}}$ = 1.3, $\tau_t = 15 \cdot \tau_{sample}$.

8.4 Discussion

The controller gain compensation in the overmodulation range proved to diminish the stability properties of the DC grid voltage. In a discrete system, the control voltage of the modulator is shaped in steps. The sampling frequency decides the sizes of these steps. For low sampling frequencies, the steps will become large. Now, if the converter operates in overmodulation and controller gain compensation is applied, these large steps of the modulation signal may be largely amplified. This amplification again brings increased oscillations and instability.

A second attempt to reduce the voltage transients, was made by introducing transient references in the control system. When comparing transient references in the current control vs. the voltage control, the first was clearly favorable. With transient references applied in the voltage controller, the resulting behavior showed to be more unpredictable. Moreover, worsened attenuation of the voltage transient, as well as increased oscillations, was observed.

Simulations indicate that d- and q-axis current impulses can respectively reduce the voltage drop or rise at the DC terminal during battery disconnection. The d-axis current reverses the power flow, whereas the q-axis current assist the d-axis current by lowering the capacitor voltage. With unknown grid parameters, the impulse magnitude and time duration must be chosen with care to fit all grid conditions. In a strong grid, the power system is more prone to over currents, which is a limiting factor of the applied current impulse. Another limiting factor of the current impulse is a second drop or rise in the voltage occurring when the impulse ends. The effect is particularly evident for a large impulse

magnitude during strong grid conditions and for a combined large impulse magnitude and time duration during weak grid conditions. More sophisticated alternatives to a reference impulse were investigated. An example is a reference step with a following ramp back to zero. However, no improvement in terms of transient voltage reduction was obtained.

The proposed d- and q axis reference current impulses were chosen to minimize the voltage transient while keeping the converter current below 1.4 pu. When power is supplied from the DC grid during battery disconnection, the transient voltage drop has a maximum deviation of 9% with the proposed impulse. From the stage of fault detection at 0.95 pu voltage, the voltage violation is reduced by 50%. When power is oppositely supplied to the DC grid, the voltage transient rise has a maximum deviation of 19%. From the stage of fault detection at 1.1 pu voltage, the voltage transient is reduced by 43%.

Chapter 9

Conclusion and further work

9.1 Conclusion

This master thesis has investigated the possibility of forming a robust hybrid AC/DC marine power system with a VSC as the critical interfacing unit. The work has been specially aimed towards the development of a flexible VSC control strategy able to support the DC voltage in case the main unit responsible for DC voltage control is disconnected. The grid forming responsibility is then put on the VSC powered by the AC grid. A discrete simulation model was built, including active power control and DC terminal voltage control in the synchronous reference frame. In order to obtain realistic results, a converter switching model was chosen, and an accurate sampling delay introduced.

Through simulations, overmodulation showed to be inevitable. The problem particularly arises when power is transferred to the AC grid under weak grid conditions. In voltage control mode of operation, this leads to immediate instability due to reduced controller gains in the overmodulation range. In order to limit the degree of overmodulation, reactive compensation was implemented. Active damping was further introduced based on filter capacitor voltage feedback. The solution proved more adaptable to varying grid parameters in comparison to passive damping. It also provided better damping of voltage transients.

The power quality of the AC terminal was quantified in terms of voltage THD. Levels around 10% were observed, which violates marine power system regulations, where a maximum of 8% is tolerated. Examination of the frequency spectrum showed high levels of the 5th and 7th order voltage harmonic consistent through different grid conditions and load variations. A selective harmonic compensation strategy was consequently implemented. By focusing on 5th order harmonic attenuation, the levels of THD dropped to half the original levels.

Regarding the change of control mode, three different fault detection methods were discussed. Voltage derivative detection proved to be slower than voltage limit detection. Voltage detection with dynamically changing voltage limits can further reduce the fault detection time if the DC voltage is prone to drifting. Gain compensation in the overmodu-

lation range proved destructive from a stability point of view. However, by adding transient references in the control system, the transient voltage peak was limited. Both adding transient references in the voltage control and the current control were examined, with the last one to be the clearly most effective. An impulse in the d-axis current reverses the power flow, whereas the q-axis current assists the d-axis current by lowering the capacitor voltage.

With unknown grid parameters, the impulse magnitude and time duration must be chosen to fit all grid conditions. The proposed d- and q axis reference current impulses were chosen to minimize the voltage transient while keeping the converter current below 1.4 pu. When power is supplied from the DC grid during battery disconnection, the transient voltage drop has a maximum deviation of 9% with the proposed impulse. From the stage of fault detection at 0.95 pu voltage, the voltage violation is reduced by 50%. When power is oppositely supplied to the DC grid, the voltage transient rise has a maximum deviation of 19%. From the stage of fault detection at 1.1 pu voltage, the voltage transient is reduced by 43%.

9.2 Further work

A realistic simulation model of a VSC interfaced hybrid AC/DC marine power system with an accurate sampling delay has been developed. Reactive compensation, active damping, and harmonic compensation are important concepts that form the basis for further work. When the main unit responsible for DC voltage control is disconnected, a proposed VSC control mode change operation ensures fast maintenance of the DC grid voltage. For increased robustness of the overall power system, the control system should also be able to detect and cope with generation outages in the AC grid. The power system should be evaluated in a lab environment with fast-acting gensets included in the power system. This will allow a more realistic comparison of the fault detection methods when gensets are present. The influence of the gensets on the voltage behavior during transients is also of interest and demands a more complex setup. For bidirectional power flow of the converter, overmodulation is a major concern. Further work should consequently evaluate if a DC to DC converter can be added for overall improved efficiency and power quality.

A summary of the proposed further work is listed below:

- Detect and handle generation outages in the AC grid.
- Evaluate the power system in a lab environment.
- Evaluate if a DC to DC converter can be added for overall improved efficiency and power quality.

Bibliography

[1] Ole Martin Flatjord. Control of two-level pwm vsc for marine hybrid ac-dc power systems. Dec 2019.

[2] United Nations Climate Change. *The paris agreement*. URL https://unfccc.int/process-and-meetings/the-paris-agreement/the-paris-agreement. Accessed: 07.04.2020.

[3] Co2 emissions from fuel combustion. URL https://unfccc.int/process-and-meetings/the-paris-agreement/the-paris-agreement. Accessed: 07.04.2020.

[4] UNCTAD. Review of maritime transport 2019. *The United Nations Conference on Trade and Development*.

[5] Transport and Environment. *Air pollution from ships*. URL https://www.transportenvironment.org/what-we-do/shipping/air-pollution-ships. Accessed: 27.04.2020.

[6] O. Alnes, S. Eriksen, and B. Vartdal. Battery-powered ships: A class society perspective. *IEEE Electrification Magazine*, 5(3):10–21, 2017.

[7] E. Skjong, R. Volden, E. Rødskar, M. Molinas, T. A. Johansen, and J. Cunningham. Past, present, and future challenges of the marine vessel's electrical power system. *IEEE Transactions on Transportation Electrification*, 2(4):522–537, 2016.

[8] ABB. *On board DC grid The step forward in power generation and propulsion*. URL http://www04.abb.com/global/seitp/seitp202.nsf/0/292d42e87306453dc12579ad0050a457/$file/12_10_OnboardDCGrid_Technical-Information.pdf. Accessed: 27.04.2020.

[9] DNV-GL. *Offshore Standard, Electrical installations*, 2015. Accessed: 14.04.2020.

[10] William Robbins Med Mohan, Tore Undeland. *Power Electronics; Converters, Applications, and Design*, 2003.

[11] J. A. Houldsworth and D. A. Grant. The use of harmonic distortion to increase the output voltage of a three-phase pwm inverter. *IEEE Transactions on Industry Applications*, IA-20(5):1224–1228, Sep. 1984. ISSN 1939-9367. doi: 10.1109/TIA.1984.4504587.

[12] J. Holtz. Pulsewidth modulation for electronic power conversion. *Proceedings of the IEEE*, 82(8):1194–1214, 1994.

[13] Guan-Chyun Hsieh and J. C. Hung. Phase-locked loop techniques. a survey. *IEEE Transactions on Industrial Electronics*, 43(6):609–615, Dec 1996. ISSN 1557-9948. doi: 10.1109/41.544547.

[14] M. El-Habrouk, M. K. Darwish, and P. Mehta. Active power filters: a review. *IEE Proceedings - Electric Power Applications*, 147(5):403–413, 2000.

[15] F.L.M Antunes and S. V. Araujo. Lcl filter design for grid-connected npc inverters in offshore wind turbines. *The 7th International Conference in Power Electronics*, pages 1233–1138, Oct. 2007.

[16] R. N. Beres, X. Wang, M. Liserre, F. Blaabjerg, and C. L. Bak. A review of passive power filters for three-phase grid-connected voltage-source converters. *IEEE Journal of Emerging and Selected Topics in Power Electronics*, 4(1):54–69, 2016.

[17] W. Wu, Y. Sun, M. Huang, X. Wang, H. Wang, F. Blaabjerg, M. Liserre, and H. S. Chung. A robust passive damping method for llcl-filter-based grid-tied inverters to minimize the effect of grid harmonic voltages. *IEEE Transactions on Power Electronics*, 29(7):3279–3289, 2014.

[18] W. Wu, Y. He, T. Tang, and F. Blaabjerg. A new design method for the passive damped lcl and llcl filter-based single-phase grid-tied inverter. *IEEE Transactions on Industrial Electronics*, 60(10):4339–4350, 2013.

[19] M. Liserre, F. Blaabjerg, and S. Hansen. Design and control of an lcl-filter-based three-phase active rectifier. *IEEE Transactions on Industry Applications*, 41(5): 1281–1291, 2005.

[20] T. C. Y. Wang, Zhihong Ye, Gautam Sinha, and Xiaoming Yuan. Output filter design for a grid-interconnected three-phase inverter. In *IEEE 34th Annual Conference on Power Electronics Specialist, 2003. PESC '03.*, volume 2, pages 779–784 vol.2, 2003.

[21] W. Gullvik, L. Norum, and R. Nilsen. Active damping of resonance oscillations in lcl-filters based on virtual flux and virtual resistor. In *2007 European Conference on Power Electronics and Applications*, pages 1–10, 2007.

[22] S. Tarbouriech and M. Turner. Anti-windup design: an overview of some recent advances and open problems. *IET Control Theory Applications*, 3(1):1–19, 2009.

[23] V. E. Wagner, J. C. Balda, D. C. Griffith, A. McEachern, T. M. Barnes, D. P. Hartmann, D. J. Phileggi, A. E. Emannuel, W. F. Horton, W. E. Reid, R. J. Ferraro, and W. T. Jewell. Effects of harmonics on equipment. *IEEE Transactions on Power Delivery*, 8(2):672–680, 1993.

[24] Chi-Jui Wu, Jung-Chen Chiang, Shih-Song Yen, Ching-Jung Liao, Jin-Shyr Yang, and Tzong-Yih Guo. Investigation and mitigation of harmonic amplification problems caused by single-tuned filters. *IEEE Transactions on Power Delivery*, 13(3): 800–806, 1998.

[25] H. Akagi. Active harmonic filters. *Proceedings of the IEEE*, 93(12):2128–2141, 2005.

[26] P. Mattavelli. A closed-loop selective harmonic compensation for active filters. *IEEE Transactions on Industry Applications*, 37(1):81–89, 2001.

[27] S. Buso, L. Malesani, and P. Mattavelli. Comparison of current control techniques for active filter applications. *IEEE Transactions on Industrial Electronics*, 45(5): 722–729, 1998.

[28] Zhiling Qiu, Jie Kong, and Guozhu Chen. A novel control approach for lcl-based shunt active power filter with high dynamic and steady-state performance. In *2008 IEEE Power Electronics Specialists Conference*, pages 3306–3310, 2008.

[29] A. M. Hava, R. J. Kerkman, and T. A. Lipo. Carrier-based pwm-vsi overmodulation strategies: analysis, comparison, and design. *IEEE Transactions on Power Electronics*, 13(4):674–689, 1998.

[30] T. M. Rowan, R. J. Kerkman, and T. A. Lipo. Operation of naturally sampled current regulators in the transition mode. *IEEE Transactions on Industry Applications*, IA-23 (4):586–596, 1987.

Appendix

Appendix A

Reference frame transformations

The amplitude invariant Clarke transform :

$$\vec{x}^{\alpha\beta 0} = P\vec{x}^{abc} = \frac{2}{3}\begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} \times \begin{bmatrix} x^a \\ x^b \\ x^c \end{bmatrix} \tag{A.1}$$

Figure A.1: The amplitude invariant Clarke transformation matrix

The inverse amplitude invariant Clarke transform :

$$\vec{x}^{abc} = P^{-1}\vec{x}^{\alpha\beta 0} = \frac{2}{3}\begin{bmatrix} 1 & 0 & 1 \\ -\frac{1}{2} & \frac{\sqrt{3}}{2} & 1 \\ -\frac{1}{2} & -\frac{\sqrt{3}}{2} & 1 \end{bmatrix} \times \begin{bmatrix} x^\alpha \\ x^\beta \\ x^0 \end{bmatrix} \tag{A.2}$$

Figure A.2: The inverse amplitude invariant Clarke transformation matrix

The amplitude invariant Park transform:

$$\vec{x}^{dq0} = P\vec{x}^{abc} = \frac{2}{3}\begin{bmatrix} \cos\theta & \cos\left(\theta - \frac{2\pi}{3}\right) & \cos\left(\theta + \frac{2\pi}{3}\right) \\ -\sin\theta & -\sin\left(\theta - \frac{2\pi}{3}\right) & -\sin\left(\theta + \frac{2\pi}{3}\right) \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} \times \begin{bmatrix} x^a \\ x^b \\ x^c \end{bmatrix} \tag{A.3}$$

Figure A.3: The amplitude invariant Park transformation matrix

The inverse amplitude invariant Park transform:

$$\vec{x}^{abc} = P^{-1}\vec{x}^{dq0} = \begin{bmatrix} \cos\theta & -\sin\theta & 1 \\ \cos\left(\theta - \frac{2\pi}{3}\right) & -\sin\left(\theta - \frac{2\pi}{3}\right) & 1 \\ \cos\left(\theta + \frac{2\pi}{3}\right) & -\sin\left(\theta + \frac{2\pi}{3}\right) & 1 \end{bmatrix} \times \begin{bmatrix} x^d \\ x^q \\ x^0 \end{bmatrix} \tag{A.4}$$

Figure A.4: The inverse amplitude invariant Park transformation matrix

The amplitude invariant negative sequence Park transform:

$$\vec{x}^{dq} = P_{neg}\vec{x}^{abc} = \frac{2}{3}\begin{bmatrix} \cos\theta & -\cos\left(\theta - \frac{2\pi}{3}\right) & -\cos\left(\theta + \frac{2\pi}{3}\right) \\ -\sin\theta & \sin\left(\theta - \frac{2\pi}{3}\right) & \sin\left(\theta + \frac{2\pi}{3}\right) \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} \times \begin{bmatrix} x^a \\ x^b \\ x^c \end{bmatrix} \tag{A.5}$$

Figure A.5: The amplitude invariant negative sequence Park transformation matrix

The inverse amplitude invariant negative sequence Park transform:

$$\vec{x}^{abc} = P_{neg}^{-1}\vec{x}^{dq0} = \begin{bmatrix} \cos\theta & -\sin\theta & 1 \\ -\cos\left(\theta - \frac{2\pi}{3}\right) & \sin\left(\theta - \frac{2\pi}{3}\right) & 1 \\ -\cos\left(\theta + \frac{2\pi}{3}\right) & \sin\left(\theta + \frac{2\pi}{3}\right) & 1 \end{bmatrix} \times \begin{bmatrix} x^d \\ x^q \\ x^0 \end{bmatrix} \tag{A.6}$$

Figure A.6: The inverse amplitude invariant negative sequence Park transformation matrix

Appendix B

Simulink models

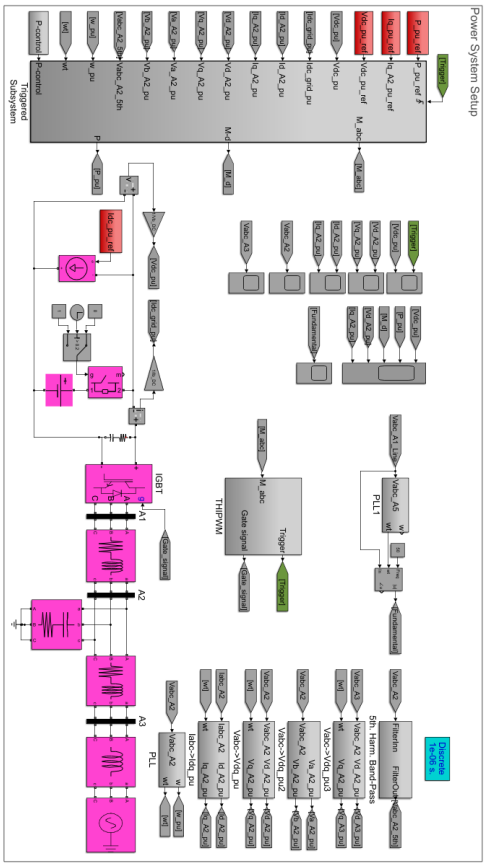


Figure B.1: The power system setup.

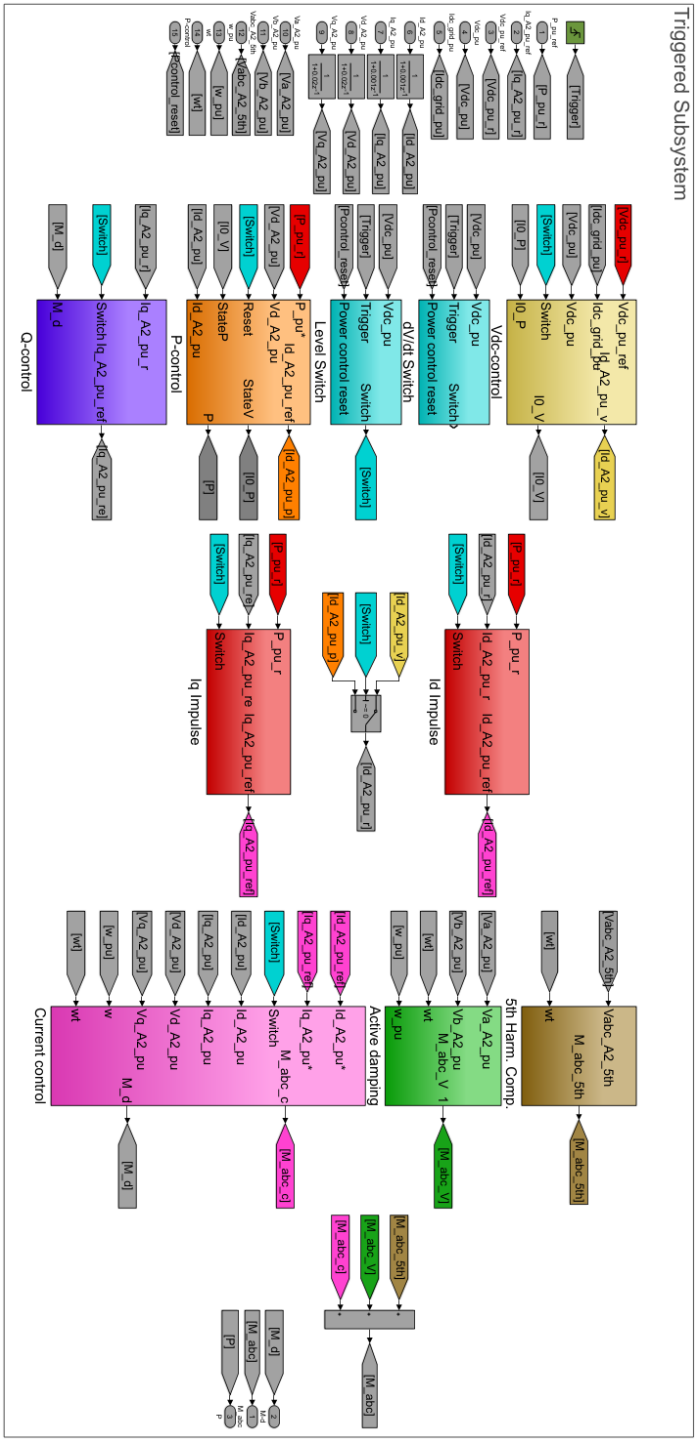
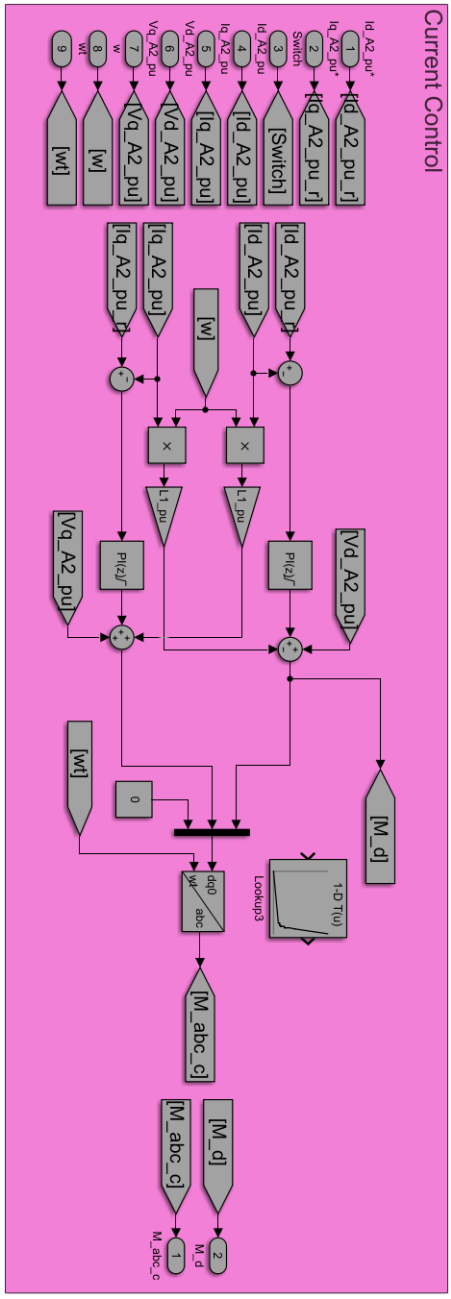
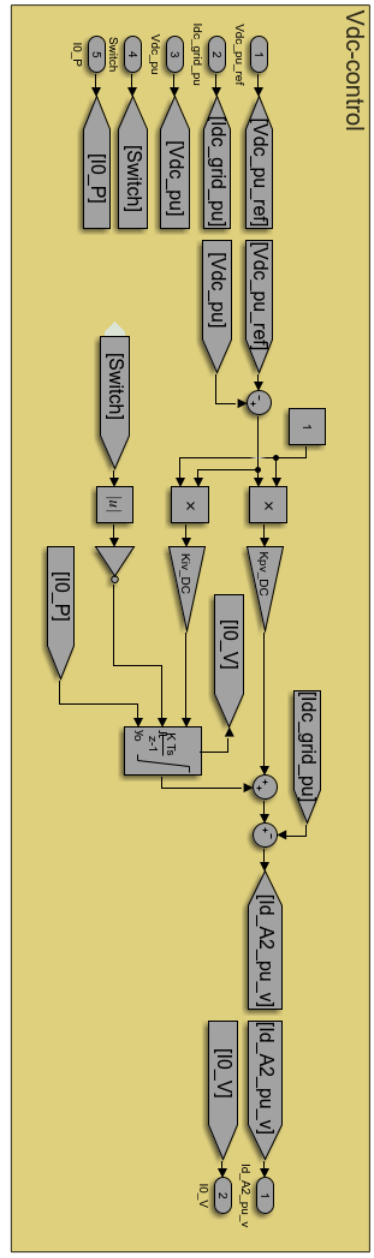


Figure B.2: The control system.

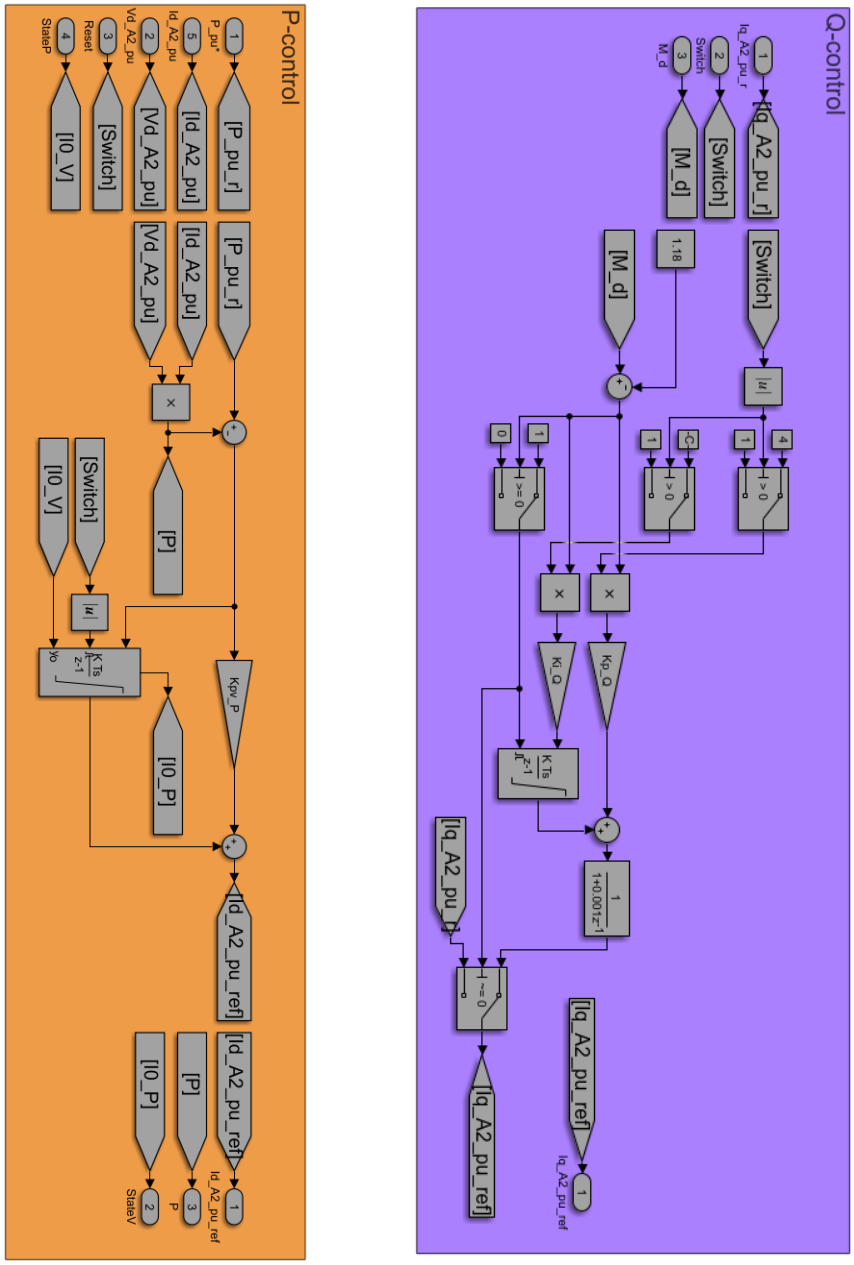


(a) Current control.



(b) Vdc-control.

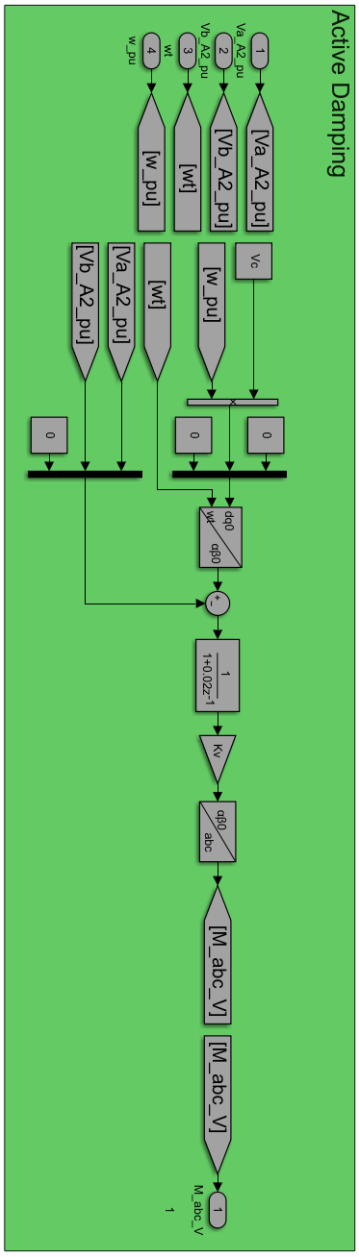
Figure B.3: Current and DC voltage control schemes.



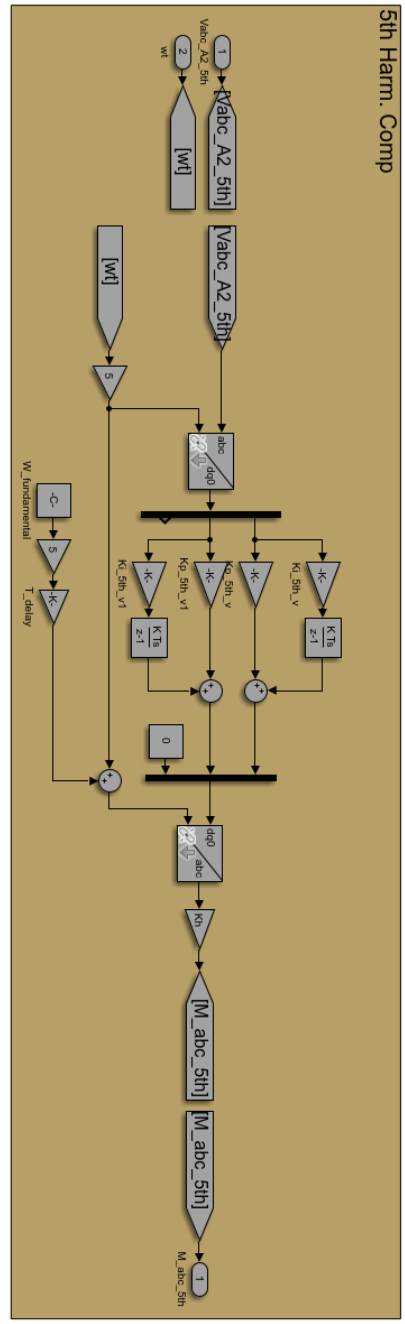
(a) P-control.

(b) Q-control.

Figure B.4: Active and reactive power control schemes.

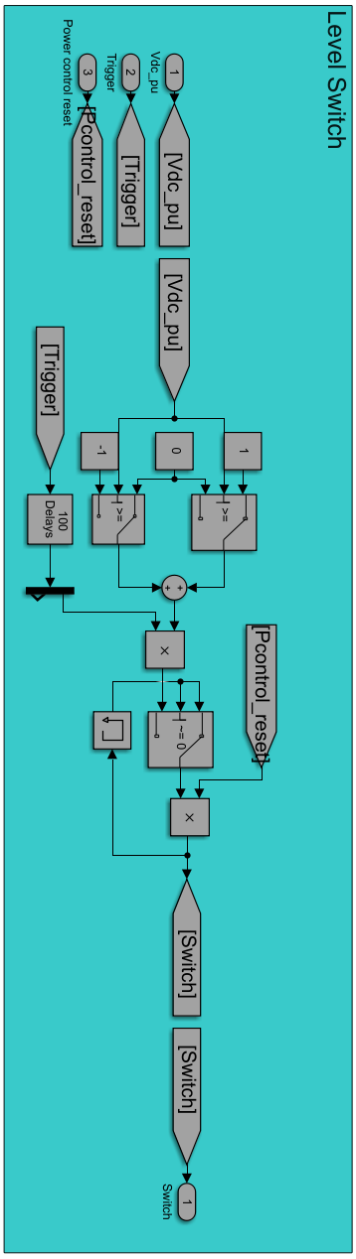


(a) Active damping.

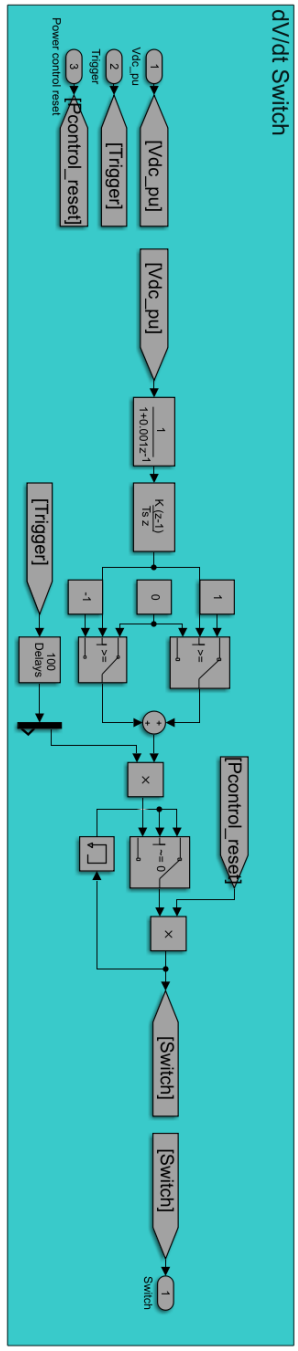


(b) 5th Harm. Comp.

Figure B.5: Active damping and harmonic compensation control schemes.

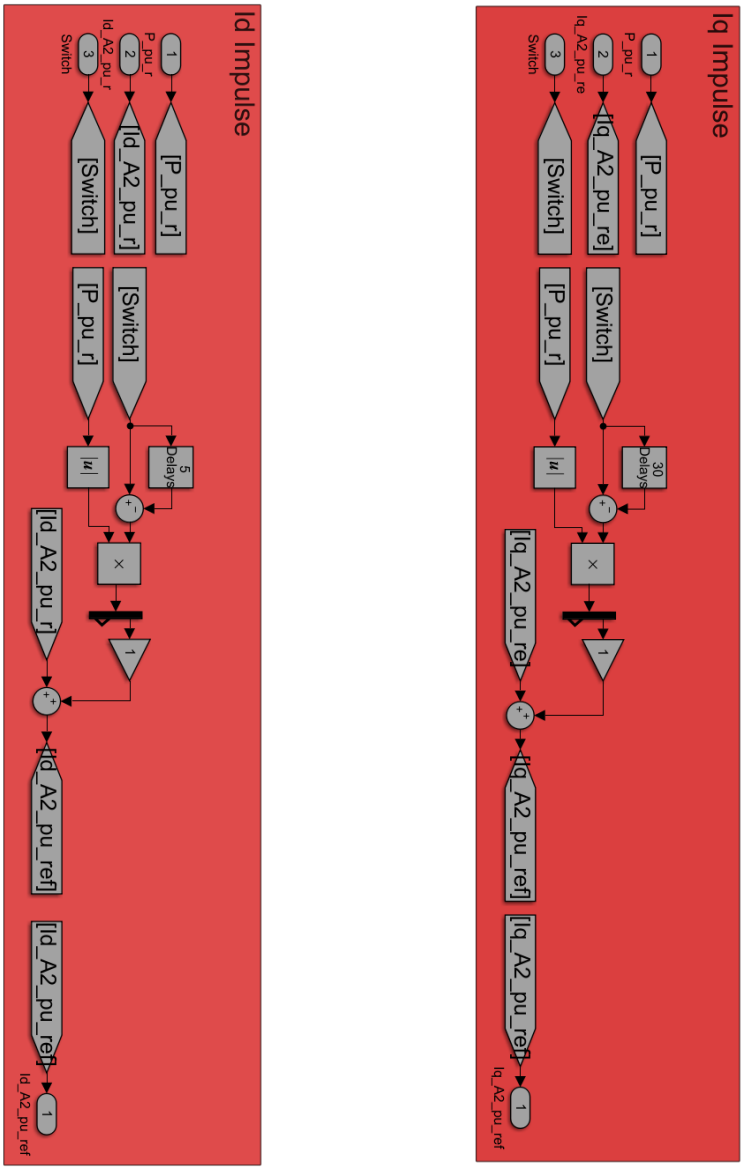


(a) Level switch.



(b) dV/dt switch.

Figure B.6: Fault detection control schemes.



(a) Id impulse.

(b) Iq impulse.

Figure B.7: Current reference impulse control schemes.

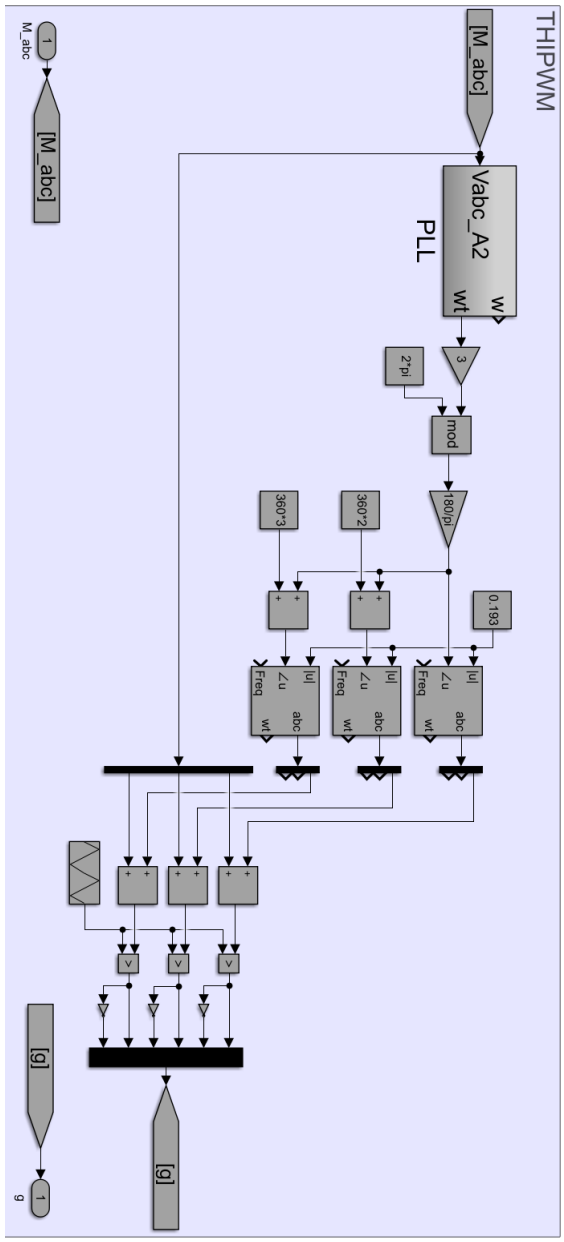
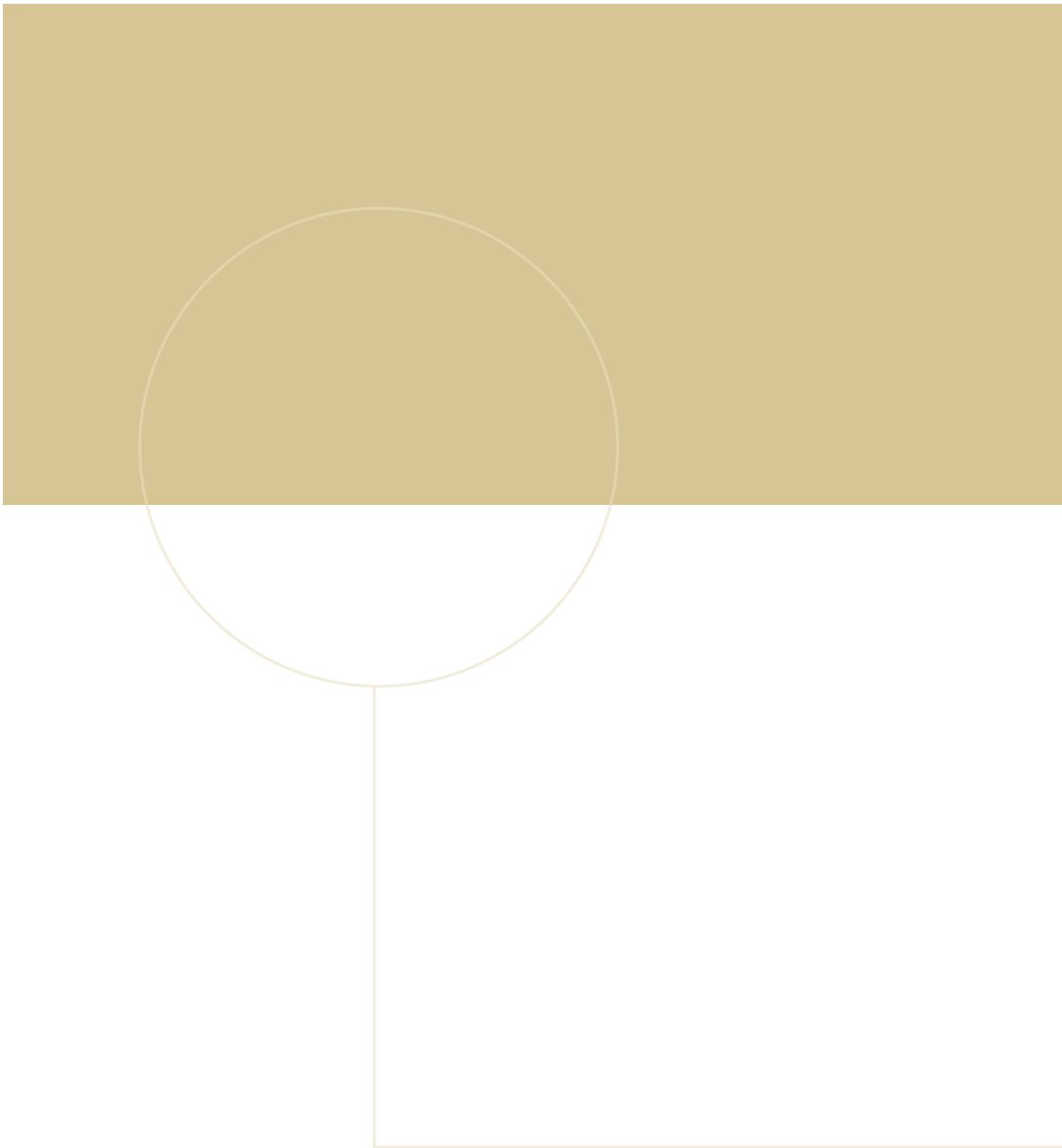


Figure B.8: The third harmonic injected pulse-width modulation(THIPWM) control scheme.



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