IEEE Open Journal of
Industry Applications

Received 11 January 2023; revised 28 March 2023; accepted 11 April 2023. Date of publication 13 April 2023;
date of current version 26 April 2023. The review of this article was arranged by Associate Editor Luca Solero.

Digital Object Identifier 10.1109/OJIA.2023.3266882

Harmonic-Invariant Scaling Method for Power Electronic Converters in Power Hardware-in-the-Loop Test Beds

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This work was supported in part by the PETROSENTER scheme, under the "Research Centre for Low-Emission Technology for Petroleum Activities on the Norwegian Continental Shelf" (LowEmission) under Grant 296207, and in part by the program PETROMAKS2 of the Research Council of Norway, within the project "Smart Platform," under Grant 308735.

ABSTRACT Power hardware-in-the-loop (PHIL) is an experimental technique that uses power amplifiers and real-time simulators for studying the dynamics of power electronic converters and electrical grids. Power hardware-in-the-loop (PHIL) tests provide the means for functional validation of advanced control algorithms without the burden of building high-power prototypes during early technology readiness levels. However, replicating the behavior of high-power systems with laboratory scaled-down converters (SDCs) can be complex. Inaccurate scaling of the SDCs coupled with an exclusive focus on instantaneous voltages and currents at the fundamental frequency can lead to PHIL results that are only partially relatable to the high-power systems under study. Test beds that fail to represent switching frequency harmonics cannot be used for studying harmonic penetration or loss characterization of large-scale converters. To tackle this issue, this article proposes a harmonic-invariant scaling method that exploits the volt-ampere rating of preexisting laboratory SDCs for more accurately replicating harmonic phenomena in a PHIL test bench. First, a theoretical analysis of the proposed method is presented and, subsequently, the method is validated with MATLAB simulations and experimental tests.

INDEX TERMS Hardware-in-the-loop, large-scale systems, power conversion harmonics, real-time emulation, voltage source converter.

I. INTRODUCTION

Power hardware-in-the-loop (PHIL) testing bridges the gap between laboratory prototypes and real operational devices. It represents a sensible final step before deployment of an electric power component in the real world [1]. The applications of PHIL span high performance motor drives [2], microgrids [3], renewable energy [4], and control of high-power converters [5]. Also, the research work that could not be validated with real-world systems due to lack of resources, time, and space could gain additional confidence with a conscious fusion of real and virtual systems as software or simulations in the loop [1].

In most cases, a device under test (DUT) is a power conversion equipment in a laboratory setup interfaced through power amplifiers with a simulated complex system in a real time simulator. The easiest scenario is when the voltage and power levels of the DUT, power amplifier, and the simulated system are of similar magnitude. But, practically, this is rare as most of the DUTs in academic or industrial laboratories are low-voltage (LV) equipment with limited voltage and current capabilities adhering to standard safety practices and the power systems that are emulated are at higher voltage/power levels typically in MW scale. Also, the capital expenditure (CapEx) to own power amplifiers capable of driving high

power DUTs is significantly higher. Due to these practical limitations, SDCs are commonly used as DUTs to emulate real full-size converters (FSCs) [6], [7], [8]. However, an accurate scaling and interface methodology is essential for a realistic PHIL simulation, especially when the physical system is a reduced-scale DUT and the concerned study focuses on FSC harmonic injection or absorption. Without these, benefits of choosing only controller hardware-in-the-loop simulations [9], [10], [11], [12] or offline digital simulation outweigh those of PHIL due to their simplicity in implementation.

On one side, traditional scaling methods utilize rated values of voltages, currents, and power of the SDC to directly normalize and match performance with the FSC [7], [13], [14]. In [7], for instance, a 300 MW wind farm is emulated by a reduced-scale 3 kW permanent-magnet synchronous generator (PMSG) connected to a full-power back-to-back power electronic converter (PEC). The test aims to study the behavior of the PMSG for frequency regulation support and the entire wind farm is modeled as a controllable current source passed through a low-pass filter (100 Hz cut-off) leaving behind the harmonics. In [6], a scaled-down 3 kW modular multilevel converter (MMC) is employed to emulate a 1500 MW full-scale MMC using average models neglecting the switching harmonics. Type 3 and 4 [15] wind turbines of 2 MW and 600 kW, respectively, are emulated with 75-kVA voltage source converters (VSCs) by Huerta et al. [8], who perform the scaling up to the emulated high-power system through a controlled power source while mentioning the advantage of using similar L filters both in the simulated and physical systems but do not discuss the impedance mismatch of the L filter. These mentioned scaling methods assume power flow only at the fundamental frequency. Thus, stability studies of the PHIL simulation with the SDCs may not fully conform with their high power systems as the harmonic interactions with the grid have been simplified. This is due to the impedance mismatch resulting from coupling transformer, inductive–capacitive–inductive (*LCL*) filter, and also higher switching frequency of the SDC when compared with FSC. Given the limited assortment of available SDCs, it is a challenge to find specific sets of converters, transformer, and inductive–capacitive (*LC*) filter that represent reasonably the FSC.

On the other side, the authors in [16] and [17] report issues in interfacing methods related to parasitic resonance between the impedances of the DUT and grid simulators, mismatch in reconstructed real voltage over its simulated signal, and problems with phase delays. These issues are typically solved by modifying, as part of the interfacing algorithms, either the hardware or software impedance. Although the focus of this article is not on interfacing algorithms, it is worth mentioning that some impedance-based interface algorithms alter the power circuit of the SDC [18] and this could further deteriorate the representation of the SDC as FSC for high-frequency transients including the ones related to pulsewidth modulation (PWM) switching. Most of the PHIL results [13], [19], [20] do not present outcomes that match voltages and currents at the switching frequency range of the FSC. Hence, there is a research gap in validating SDCs as replicas of FSCs for both line frequency and harmonic interactions with PHIL simulations.

In summary, there is no "one size SDC fits all" solution for establishing an accurate PHIL test bench and no two SDCs of different converter sizes, *LCL* filters, and make of line transformers with direct scaling at rated voltage and current produce identical PHIL results representing the same FSC. It is noteworthy that, to the extent of the authors' knowledge, the flexibility of varying the base kilovolt-ampere (kVA) ratings of SDCs is often ignored and rarely discussed in the literature. Hence, this article proposes a novel harmonic-invariant scaling method (HISM) to exploit the base kVA rating of an SDC to scale up and match the performance of the FSC not only at line frequency but also for harmonic interactions up to the switching frequency. In other words, the voltage and current waveforms of the SDC when scaled up accurately match the FSC's in the spectrum between the fundamental and the switching frequency. This harmonic invariant feature in the scaled-down converter is important when power quality and harmonic disturbances are scrutinized; a proper match of the converter PWM frequency and the *LCL* filter should be guaranteed. Only then research concerning harmonic reduction/mitigation techniques using advanced PWM techniques and the design of passive filters to meet various emerging grid code requirements can be experimentally tested in the prototype stage. This is the main strength of the proposed method, which features a script to vary SDC base values of voltages and currents (in turn base kVA rating) and selects the base value that gives the best match with the FSC.

This article presents the following contributions.

1) Guidelines for performing PHIL simulations that can be adapted to academic and industrial laboratories.
2) Novel HISM to exploit the base kVA rating of SDC for an accurate match with FSC.
3) Scaling method independent of the filter topology (*L/LC/LCL*) between the converter and the grid.
4) Simplified script, made publicly available at [21], to integrate with PHIL control code constrained by operating limits of the converter, available passive components in the laboratory, and a predefined error in normalized quantities.

This article is organized as follows. The scaled-down PHIL test bench at the National Smart Grid Laboratory in Norway is presented in Section II. The mismatch in per-unit (p.u.) values when the SDC is operated at nominal rating is highlighted in Section III. The proposed HISM concept introduced as systematic procedure using a flowchart is presented in Section IV. In Section V, the HISM is applied to a practical example representing a 5-MVA battery energy storage system (BESS) power conversion equipment [22] with an SDC in the laboratory. The theoretical analysis is, then, validated by comparing offline digital simulations and PHIL results in Section VI, and finally, Section VII concludes this article.

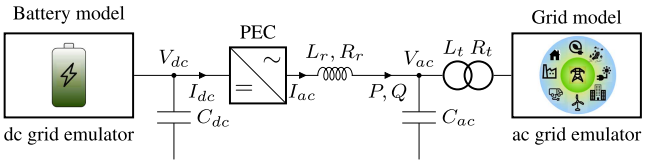

FIGURE 1. Scaled-down PHIL test rig.

II. SCALED-DOWN POWER HARDWARE-IN-THE-LOOP TEST SETUP

Fig. 1 shows the single line diagram of the PHIL setup. On the left side, the dc-grid emulator is connected to the dc link of the converter. The capacitor at the dc link is denoted by C_{dc} and the voltage across this capacitor is named V_{dc}. The current flowing into the dc side of the PEC is named I_{dc}. The dc-grid emulator operates as a controlled voltage source. On the right side, the ac-grid emulator is connected to the converter transformer, which stands for one of the inductances of the *LCL* filter. The short-circuit impedance of the transformer is denoted by L_t (inductive part) and R_t (resistive part). The values of the short-circuit inductance and resistance are the ones seen from the converter side terminals of the transformer. The ac-grid emulator operates as a controlled voltage source. The voltage at the middle of the *LCL* filter is named V_{ac}. The capacitive branch of the *LCL* filter is represented by C_{ac}. The converter reactor is modeled by the inductance L_r with a parasitic resistance R_r. The current leaving the converter is denoted by I_{ac}.

In this article, the superscript *fs* denotes quantities related to the FSC and the superscript *sd* denotes quantities of the SDC. Capital letters refer to quantities in SI units, whereas lowercase letters are employed for normalized (i.e., divided by a base value) quantities. Also, the described scaling method does not change time. Hence, quantities in seconds and hertz are unaffected. Therefore, the following values are assumed equal for both full-size and scaled-down systems:

1) rated ac frequency F_n in hertz and correspondent angular frequency $\omega_n = 2\pi F_n$ in rad/s;
2) switching frequency F_{sw} in hertz of the converters.

Note that laboratory SDCs are able to operate at higher switching frequencies (5–10 kHz) [23] than megawatt-sized real-life converters (on the range of 2–3 kHz) [22]. It is, however, simple to lower the SDC switching frequency in the laboratory.

III. NORMALIZATION OF FSC AND SDC QUANTITIES

The goal of the scaling is to match the normalized quantities describing the FSC and SDC. To begin with, a set of normalizing bases for the quantities in the ac and dc side must be defined and applied to both FSC and SDC. First, base values for apparent power (S_b) and ac voltage (V_{bac}) and current (I_{bac}) are defined

$$S_b = \sqrt{3}\, V_{\text{bac}} I_{\text{bac}}\ [\text{VA}]. \tag{1}$$

For the FSC, S_b^{fs}, V_{bac}^{fs}, and I_{bac}^{fs} are typically defined as the rated values of the converter designed for an application. However, for a ready-to-use or laboratory SDC, either absolute maxima mentioned on the nameplate or derated values as provision for overloading capacities are chosen for S_b^{sd}, V_{bac}^{sd}, and I_{bac}^{sd}. The p.u. bases for the impedance (Z_b), inductance (L_b), and ac capacitance (C_b) are defined by the choices made for V_{bac} and I_{bac} as follows:

$$Z_b = \frac{V_{\text{bac}}}{\sqrt{3} I_{\text{bac}}}[\Omega],\ L_b = \frac{V_{\text{bac}}}{\omega_n \sqrt{3} I_{\text{bac}}}[\text{H}],\ C_b = \frac{\sqrt{3} I_{\text{bac}}}{\omega_n V_{\text{bac}}}[\text{F}]. \tag{2}$$

It is worth recalling that ω_n is equal for both full-scale and scaled-down converters. Also, for simplicity, the power bases on the ac and dc sides are assumed equal, i.e., the converter losses are ignored and the power factor is assumed to be unity.

$$S_b = V_{\text{bdc}} I_{\text{bdc}} = \sqrt{3}\, V_{\text{bac}} I_{\text{bac}}. \tag{3}$$

The main purpose of the dc-link capacitance is to serve as an energy buffer. It keeps the dc-link voltage relatively constant during transitory unbalances in power exchange through the converter. For normalization, an option is to use an analogous of the inertia constant H of synchronous machines [24], which is defined as the kinetic energy stored in the rotor divided by the machine's apparent power. For the converters, the analogous H is equal to the energy stored in the capacitor at rated dc voltage divided by the converter's rated apparent power.

$$H = \frac{C_{\text{dc}} V_{\text{bdc}}^2}{2 S_b}\ [\text{s}]. \tag{4}$$

Table 1 shows the quantities before and after normalization, computed with (1)–(4), for an FSC and a laboratory ready-to-use SDC. It can be clearly seen that the normalized quantities for the SDC computed both at nameplate values and close to rated values have a mismatch compared to the FSC.

IV. PROPOSED (HISM)

It is fairly common for laboratories to feature sets of ready-to-use converters that can be chosen as SDCs to represent specific FSCs in different PHIL setups. However, the direct scaling of these converters can lead to large discrepancies in p.u. values of components of the FSC and SDC. As it is not always feasible to procure a tailor-made SDC for each and every PHIL setup, it is essential to develop a matching procedure between available SDCs and an FSC. To address this problem, this article proposes the HISM that minimizes mismatches by searching for optimal sets of p.u. base values within the SDC kVA range. A summarized version of this procedure is shown in Fig. 2. The mismatches are assessed for combinations of V_{bac}^{sd} and I_{bac}^{sd} assuming that those only take up discrete values between minimum and maximum voltage and current.

TABLE 1. Mismatch in p.u. Values Between an SDC Scaled At Nameplate and At Close to Rated Values and an FSC

Quantity		Full-scale converter		Scaled-down converter (Nameplate values)		Scaled-down converter (Close to rated values)	
Apparent power	S_b	5 MVA		70 kVA		45 kVA	
Voltage ac	V_{bac}	690 V		400 V		363 V	
Current ac	I_{bac}	4184 A		100 A		72 A	
Voltage dc	V_{bdc}	1100 V		650 V		579 V	
Current dc	I_{bdc}	4546 A		100 A		78 A	
Transformer ratio		13.8 kV / 690 V		400 V / 400 V		363 V / 363 V	
Short-circuit inductance	L_t	24.2 µH	0.08 p.u.	316 µH	0.043 p.u.	316 µH	0.034 p.u.
Short-circuit resistance	R_t	0.476 mΩ	0.005 p.u.	49.4 mΩ	0.021 p.u.	49.4 mΩ	0.017 p.u.
Converter reactor inductance	L_r	77.5 µH	0.256 p.u.	500 µH	0.068 p.u.	500 µH	0.054 p.u.
Shunt capacitance	C_{ac}	1.8 mF	0.055 p.u.	50 µF	0.036 p.u.	50 µF	0.046 p.u.
LCL resonance	F_{res}	863.7 Hz		1.61 kHz		1.61 kHz	
DC capacitance	C_{dc}	20 mF	$H = 2.42$ ms	14 mF	$H = 42.3$ ms	14 mF	$H = 52.8$ ms

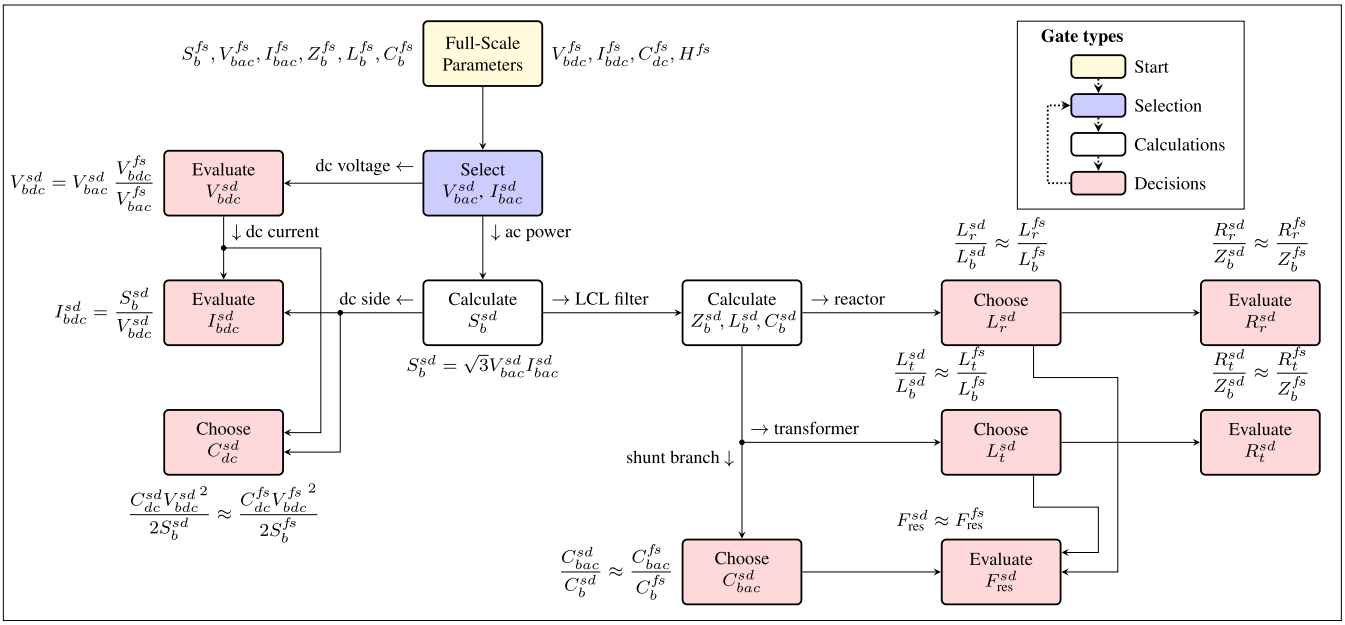

FIGURE 2. Method for matching scaled-down and full-scale converters.

A. SELECT PAIR V^{sd}_{BAC}, I^{sd}_{BAC} AND EVALUATE V^{sd}_{BDC} AND I^{sd}_{BDC}

First, select V^{sd}_{bac} according to the following constraints:

1) the operational range of the ac grid emulator;
2) the turns ratio and rated voltage of the converter transformer;
3) rating of the SDC and *LCL* devices;
4) converter minimum operating voltage for detection and synchronization using phase-locked loop (PLL).

The choice of V^{sd}_{bac} also determines the dc base voltage V^{sd}_{bdc} as follows:

$$V^{sd}_{\text{bdc}}[\text{V}] = V^{sd}_{\text{bac}} \frac{V^{fs}_{\text{bdc}}}{V^{fs}_{\text{bac}}}. \tag{5}$$

Notice that the FSC voltages V^{fs}_{bdc} and V^{fs}_{bac} are predetermined and not variables within the method. Additionally, the resulting V^{sd}_{bdc} from (5) must be within the operating range of the SDC, as well as within the range of the dc grid emulator.

Second, select an appropriate base current I^{sd}_{bac} for the SDC taking into consideration the following constraints:

1) the rated currents of the transformer;
2) the rated current of the *LC* filter devices;
3) the rated current of the SDC;
4) possible overloaded cases to be analyzed in the PHIL tests.

The selected pair V^{sd}_{bac}, I^{sd}_{bac} yields the base apparent power S^{sd}_b for the SDC (see (1)) that can be lower than the rated (nameplate) value of the SDC. Moreover, the ac voltage and

current base pair determines I^{sd}_{bdc} with (3) and the impedance bases on the LV side of the scaled-down transformer with (2). Now, the components of the *LCL* filter can be selected.

B. CONVERTER REACTOR L^{sd}_r AND R^{sd}_r

In this step, the converter-side L of the *LCL* filter is chosen. The inductance in p.u. of the converter reactor (l_r) of the SDC is compared with that of the FSC. In practice, there will be a mismatch between l^{sd}_r and l^{fs}_r, particularly in cases of limited availability of SDC reactors. If l^{sd}_r can be freely chosen, it should be made equal to l^{fs}_r.

The following equation expresses the inductance in p.u. of the converter reactor of the SDC and FSC:

$$l^{sd}_r[\text{p.u.}] = \frac{L^{sd}_r[\text{H}]}{L^{sd}_b[\text{H}]} \approx l^{fs}_r[\text{p.u.}] = \frac{L^{fs}_r[\text{H}]}{L^{fs}_b[\text{H}]}. \tag{6}$$

When L^{sd}_b in (6) is rewritten with L_b from (2), l^{sd}_r becomes

$$l^{sd}_r[\text{pu}] = L^{sd}_r \omega_n \sqrt{3} \frac{I^{sd}_{\text{bac}}}{V^{sd}_{\text{bac}}}. \tag{7}$$

As it can be seen from (7), the values of the base voltage and current influence l^{sd}_r. Thus, if L^{sd}_r cannot be changed, then V^{sd}_{bac} and I^{sd}_{bac} can be altered to bring l^{sd}_r closer to l^{fs}_r.

The resistance in p.u. of the converter reactor of the SDC should be approximately equal to that of the FSC. This is expressed in the following equation:

$$r^{sd}_r[\text{p.u.}] = \frac{R^{sd}_r[\text{H}]}{Z^{sd}_b[\text{H}]} \approx r^{fs}_r[\text{p.u.}] = \frac{R^{fs}_r[\text{H}]}{Z^{fs}_b[\text{H}]}. \tag{8}$$

When R^{sd}_b in (8) is rewritten with R_b from (2), r^{sd}_r becomes

$$r^{sd}_r[\text{p.u.}] = R^{sd}_r \sqrt{3} \frac{I^{sd}_{\text{bac}}}{V^{sd}_{\text{bac}}}. \tag{9}$$

The resistance in p.u. of the SDC converter reactor can rarely be chosen freely as it largely depends on the quality, in efficiency terms, of the reactor. Nevertheless, a mismatch between resistances in p.u. is usually expected as kVA-range laboratory reactors can have lower efficiencies, i.e., higher relative resistive losses, than industry-grade large scale reactors. Furthermore, as seen in (7) and (9), if the p.u. bases are adapted to increase l^{sd}_r, the resistance r^{sd}_r also increases. Thus, a compromise has to be made between matching the inductances and matching the resistances of the converter reactor of the SDC and FSC.

Another way of matching the converter reactor is to match the ripple current in p.u. in the SDC and FSC. One should aim to make the ripple current in p.u. for both the SDC and FSC to be as similar as possible. The peak-to-peak ripple in the converter reactor current (ΔI^{sd}_r) is given by [25]

$$\Delta I^{sd}_{L_r}[\text{A}] = \frac{V^{sd}_{\text{bdc}}}{8 L^{sd}_r F_{\text{sw}}}. \tag{10}$$

By substituting V^{sd}_{bdc} from (5) and by normalizing $\Delta I^{sd}_{L_r}$ with the peak value of I^{sd}_{bac}, one obtains

$$\Delta i^{sd}_{L_r}[\text{p.u.}] = \frac{\Delta I^{sd}_{L_r}}{\sqrt{2} I^{sd}_{\text{bac}}} = \frac{1}{8\sqrt{2} L^{sd}_r F_{\text{sw}}} \frac{V^{sd}_{\text{bac}}}{I^{sd}_{\text{bac}}} \frac{V^{fs}_{\text{bdc}}}{V^{fs}_{\text{bac}}}. \tag{11}$$

Even when the converter reactor can easily be swapped, the set of available reactors in a laboratory is usually limited. Therefore, the flexibility of adapting base voltage V^{sd}_{bac} and base current I^{sd}_{bac} should be used to match ripple currents in p.u. for the SDC and FSC. It is, however, important to notice in (11) that the ratio $V^{fs}_{\text{bdc}}/V^{fs}_{\text{bac}}$ is fixed by the FSC design.

C. CONVERTER TRANSFORMER L^{sd}_t AND R^{sd}_t

There is usually not much flexibility for choosing the SDC transformer, i.e., the grid-side L of *LCL*, in a laboratory as the set of ready-to-use transformers tends to be limited. Also, procuring tailor-made scaled-down transformers might not be economically feasible within some project budgets. Therefore, one must try to match the converter transformer p.u. inductance of the SDC and FSC by choosing the base voltage and current of the SDC.

The following equations express the p.u. value of the inductance and resistance of the SDC and the FSC:

$$l^{sd}_t[\text{p.u.}] = \frac{L^{sd}_t[\text{H}]}{L^{sd}_b[\text{H}]} \approx l^{fs}_t[\text{p.u.}] = \frac{L^{fs}_t[\text{H}]}{L^{fs}_b[\text{H}]} \tag{12}$$

$$r^{sd}_t[\text{p.u.}] = \frac{R^{sd}_t[\Omega]}{Z^{sd}_b[\Omega]} \approx r^{fs}_t[\text{p.u.}] = \frac{R^{fs}_t[\Omega]}{Z^{fs}_b[\Omega]}. \tag{13}$$

In general, a p.u. value of inductance of the SDC transformer that is similar to that of the FSC transformer should be aimed for. Likewise, a similar p.u. value should be aimed for the transformer resistance. However, it will be difficult to have a close match between the transformer resistances of the SDC and FSC as the efficiency of an LV low-power transformer in the laboratory is usually lower than that of a high-voltage high-power transformer [26].

When L^{sd}_b in (12) and R^{sd}_b in (13) are rewritten as the bases in (2), the following equations are obtained:

$$l^{sd}_t[\text{p.u.}] = L^{sd}_t \omega_n \sqrt{3} \frac{I^{sd}_{\text{bac}}}{V^{sd}_{\text{bac}}} \tag{14}$$

$$r^{sd}_t[\text{p.u.}] = R^{sd}_t \sqrt{3} \frac{I^{sd}_{\text{bac}}}{V^{sd}_{\text{bac}}}. \tag{15}$$

It can be seen from (14) and (15) that the base voltage and current can be chosen to match the p.u. inductance and p.u. resistance of the SDC transformer with those of the FSC. However, it should be noted that the choice that matches p.u. inductances will likely lead to a mismatch in p.u. resistances. Thus, a compromise between the mismatches in inductance and resistance has to be made.

D. SHUNT BRANCH OF THE LCL C_{AC}^{sd}

The normalized capacitance of the SDC *LCL* filter should be made as similar as possible to that of the FSC, i.e.,

$$c_{\text{ac}}^{sd}[\text{p.u.}] = \frac{C_{\text{ac}}^{sd}[\text{F}]}{C_{b}^{sd}[\text{F}]} \approx c_{\text{ac}}^{fs}[\text{p.u.}] = \frac{C_{\text{ac}}^{fs}[\text{F}]}{C_{b}^{fs}[\text{F}]}. \tag{16}$$

By using (2) and rewriting (16) as (17), one notices that c_{ac}^{sd} is proportional to V_{bac}^{sd} and inversely proportional to I_{bac}^{sd}.

$$c_{\text{ac}}^{sd}[\text{p.u.}] = C_{\text{ac}}^{sd}\,\frac{\omega_n}{\sqrt{3}}\,\frac{V_{\text{bac}}^{sd}}{I_{\text{bac}}^{sd}}. \tag{17}$$

When it is impractical to change C_{ac}^{sd}[F], c_{ac}^{sd}[p.u.] can be matched with c_{ac}^{fs}[p.u.] by adapting the SDC base voltage and base current. Notice that the ratio of bases in (17) is the inverse of the ones in (7), (9), (14), and (15). Therefore, a choice of bases that increases c_{ac}^{sd}, decreases l_r^{sd} and l_t^{sd}.

E. EVALUATE RESONANCE FREQUENCY F_{res}^{sd}

The *LCL* resonance frequency can be calculated using the following equation [25]:

$$F_{\text{res}}^{sd}[\text{Hz}] = \frac{1}{2\pi}\sqrt{\frac{L_t^{sd}+L_r^{sd}}{L_t^{sd}L_r^{sd}C_{\text{ac}}^{sd}}} \approx F_{\text{res}}^{fs}[\text{Hz}] = \frac{1}{2\pi}\sqrt{\frac{L_t^{fs}+L_r^{fs}}{L_t^{fs}L_r^{fs}C_{\text{ac}}^{fs}}}. \tag{18}$$

In general, the resonance frequency of the SDC should be approximately equal to that of the FSC.

F. CONVERTER DC-LINK CAPACITANCE C_{DC}^{sd}

The H constant of the SDC as defined in (4) should ideally be made equal to the one of the FSC. When changes to the SDC capacitor bank are not feasible, the values of V_{bdc}^{sd} and S_b^{sd} can be adapted to improve the match of H. It is important to remark that H should be carefully scaled when the real-life converter is expected to regulate the dc-voltage through an active current loop. In such cases, a proper modeling of interactions between the converter controller and the dc capacitance is critical. However, H is not as critical when the FSC dc link is fed by an active source like a battery as in the scenario depicted in Fig. 1.

G. APPLICATION STRATEGIES

It is clear from the previous subsections that the mismatches in the inductance of the converter reactor, the capacitance in the *LCL*, the constant H of the dc-link capacitance, and transformer reactance can be minimized by varying the base voltage V_{bac}^{sd} and base current I_{bac}^{sd}, thus the base volt-ampere (VA) rating of SDC. The process begins by sweeping in small steps the base current from a minimum to a maximum value for a given base voltage. Once the full range of the base current has been explored for this given base voltage, another current sweep is performed for a incremented value of the base voltage. At every base pair, the mismatch in the parameters is calculated. This process continues until the mismatch has been evaluated at all possible combinations of base voltages and base currents. Depending on the application purpose of the PHIL simulation, a twofold strategy has to be adapted to choose the right solution.

1) Minimizing the mismatch on one normalized quantity: The mismatch error in one normalized quantity is calculated at all possible combination of base voltage V_{bac}^{sd} and base current I_{bac}^{sd}. For multiple solutions around the predefined mismatch error, base voltage V_{bac}^{sd} and base current I_{bac}^{sd} that makes the maximum VA rating are selected for the better utilization of the SDC.
2) Compromised minimization of mismatch on all the normalized quantities: As it may be practically impossible to minimize the mismatch on all the normalized quantities without physical replacement of any component, a higher predefined mismatch error is considered and the pair of base voltage V_{bac}^{sd} and current I_{bac}^{sd} that makes the maximum VA rating is selected.

The following section presents the application of the HISM's first strategy on a practical example of a BESS power conversion stage.

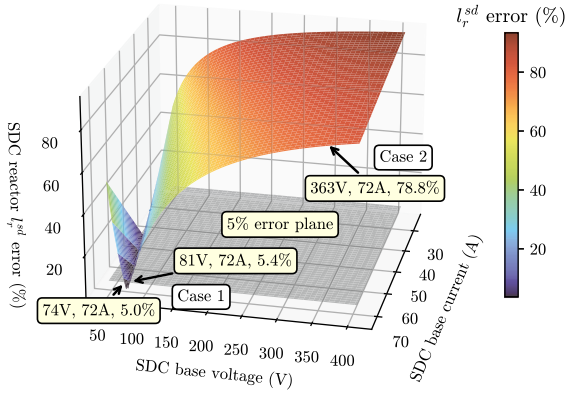

FIGURE 3. HISM applied to the converter reactor.

TABLE 2. TDD of the Converter Currents in Fig. 5(c)

	SDC Case 1	SDC Case 2	FSC
TDD	2.456 %	9.401 %	2.462 %

V. PRACTICAL EXAMPLE–BESS

The design parameters for the FSC shown in Table 1 are based on a practical grid-scale BESS that can be employed for various grid ancillary services such as frequency and voltage support, peak shaving of distributed generation, etc. It is impractical to invest on deploying the entire power conversion system in the laboratory especially for studies related to PWM techniques, harmonic penetration into the grid, and impact on power quality. The PHIL system presented in Fig. 1 can easily be made to represent a practical BESS. This is done by controlling the dc and ac emulators to respond as a battery

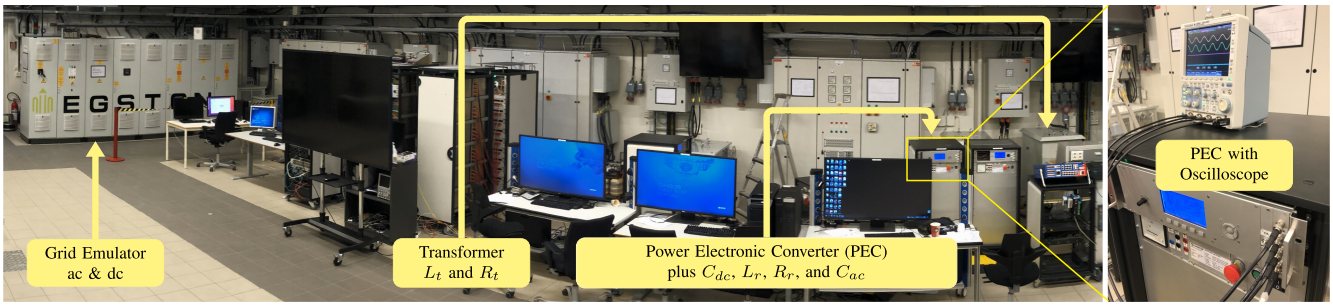

FIGURE 4. National smart grid laboratory at the norwegian university of science and technology.

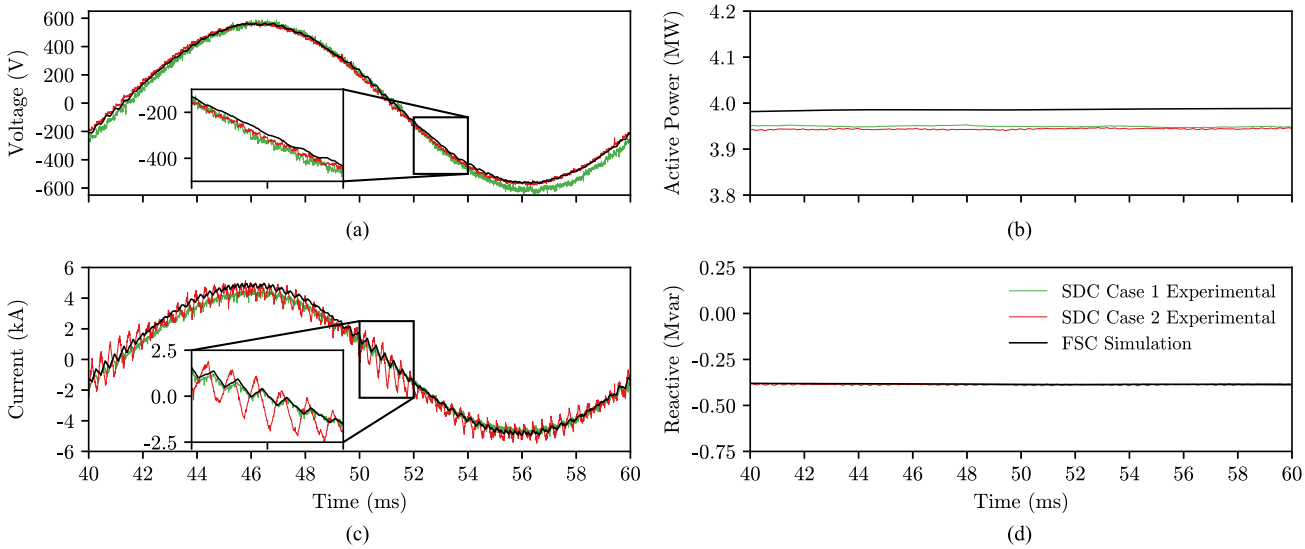

FIGURE 5. Computer simulation and PHIL results. (a) Phase to neutral voltage. (b) Active power. (c) Line current. (d) Reactive power. SDC Case 1 experimental results in solid green, SDC Case 2 experimental results in solid red, and FSC simulation results in solid black.

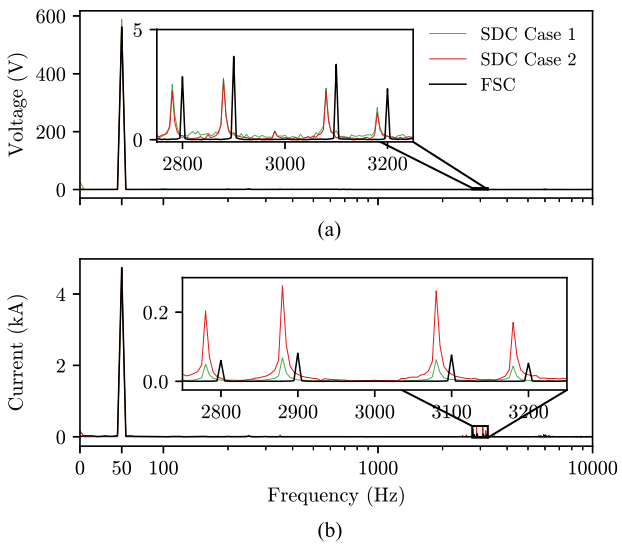

FIGURE 6. FFTs of the voltages and currents from Fig. 5.

bank and as an electric grid, respectively, and by physically representing the FSC with the SDC, as shown in Fig. 1.

Although the mentioned PHIL is a well-established technique for the BESS, the criticality is only identified when this PHIL setup needs to be used for harmonic penetration of the BESS power conversion system into the grid and to estimate the conduction and switching power losses in the FSC. For both of these aspects, it is necessary to match voltage and currents of SDC with FSC at the bandwidth of the switching frequency (3 kHz). This explains the necessity of a scaling methodology, which is independent of the rating of SDC and filter impedance (*L/LC/LCL*) between the bridge and the grid. Hence, this problem demands an alternative scaling approach to the existing PHIL setup with minimal or no physical modifications in the available SDC.

Based on mathematical computations of the proposed methodology (strategy 1) in Section IV, a MATLAB script is developed which computes an error estimate of normalized quantities between SDC and FSC while varying base values of voltage (50 to 363 V) and current (5 to 72 A) in small

steps. The sizes of these steps, which are programmable, are chosen as 1 A and 1 V for the base current and base voltage, respectively. A surface plot in Fig. 3 with varying base current and base voltage shows the error in the normalized value of l_r^{sd} compared to l_r^{fs} along with a predefined mismatch error plane of 5 %. Two cases are considered: case 1 points to base values where the error in l_r^{sd} compared to l_r^{fs} is low and is chosen to be around 5 %, case 2 points to base values, which give large error in l_r^{sd} compared to l_r^{fs}. These two contrasting cases are chosen to highlight the impact of mismatch in the converter reactor on the harmonic spectrum of the voltage across the shunt capacitor and the current across the converter reactor. Two data points for Case 1 and one data point for Case 2 are shown on the plot and further analysis will be focused around these cases. For case 1, the point with the higher VA rating of the SDC is chosen in accordance with strategy 1. Hence, the choice is made as $V_{\text{bac}}^{sd} = 81\,\text{V}$ and $I_{\text{bac}}^{sd} = 72\,\text{A}$. For Case 2, however, base values close to the rated quantities of the SDC ($V_{\text{bac}}^{sd} = 363\,\text{V}$ and $I_{\text{bac}}^{sd} = 72\,\text{A}$) are chosen. Hence, using HISM, the base VA rating of SDC is adjusted to $\sqrt{3} * 81 * 72 = 10.1$ kVA instead of $\sqrt{3} * 363 * 72 = 45.3$ kVA for minimizing the error on the inductance in p.u. of the converter reactor (l_r). Based on the application requirement, the user can freely decide between strategies 1 and 2 while using the HISM.

The performance comparison of the SDC using both HISM-based selection (Case 1) and with close to rated value (Case 2) is benchmarked against the computer simulation of a practical BESS FSC in the following section.

VI. SIMULATED AND PHIL RESULTS

The PHIL tests with the SDC are performed at the National Smart Grid Laboratory; see Fig. 4. An oscilloscope with a bandwidth of 20 MHz, no extra filtering nor smoothing, is employed for measuring two phases of the phase-to-ground voltage across the shunt capacitor and two phases of the current across the converter reactor which are indicated by V_{ac} and I_{ac} in Fig. 1, respectively. The measurements, scaled up to FSC levels, are presented in Fig. 5(a) and (c). The active and reactive power [see Fig. 5(b) and (d)] are calculated from the scaled up voltages and currents. They represent the power flow at the point indicated by P and Q in Fig. 1. A moving average filter with window equal to 20 ms is applied to the power measurements. The voltages, active power, and reactive power, obtained with Case 1 (green) and Case 2 (red) are similar to the ones obtained with a computer simulation (black) of the FSC. However, the switching ripple in the current across L_{ac} for Case 2 is clearly worse when compared to the computer simulation and to Case 1. To properly analyze the distortions and ripple in the voltages and currents, the fast Fourier transform (FFT) can be employed.

Fig. 6 shows the FFT of voltages and currents presented in Fig. 5. A time window of 200 ms, i.e., ten grid cycles, is chosen for the FFT, which yields a resolution of 5 Hz in the frequency spectrum. The frequency axis is linear between zero and 100 Hz and logarithmic between 100 Hz and 10 kHz. The amplitude of the fundamental frequency (50 Hz) of the voltage and current are similar for the FSC computer simulation (black), SDC Case 1 (green), and Case 2 (red). The distortions caused by the PWM switching in the range of 3 kHz are highlighted by insets. Case 1 greatly matches the magnitude of switching harmonics when compared to Case 2 and to the computer simulation of the FSC. For a better assessment, the total demand distortion (TDD) of the currents are calculated according to [27] with the interharmonic components in the spectrum up to 10 kHz grouped at their respective closest integer harmonic of 50 Hz. As seen in Table 2, the SDC Case 1 manages to match the TDD of the FSC and both are below the limit of 5 % established by [28], whereas the SDC Case 2 amplifies the switching frequency components, and thus, the TDD, wrongly representing the FSC in the PHIL simulation. It is worth remarking that, in the laboratory test, the current is measured at the converter terminals, i.e., before the shunt capacitance and grid-side inductance of the *LCL* filter. The authors in [28], however, defines the TDD limit for the current delivered at the point of common connection.

VII. CONCLUSION

Reduced-scale PHIL tests in academic or industrial laboratories can greatly reduce the burden of building high-power converter prototypes in early technology readiness level stages. However, as any other modeling technique, the depth of detail in which the laboratory SDC mimics the real-life FSC has to be adapted to the phenomena one intends to investigate with the PHIL tests. When power quality and harmonic disturbances are under scrutiny, a proper match of the converter PWM frequency and the *LCL* filter should be guaranteed. In this article, a method that aims to reproducing the distortions and harmonic content of real-life power converters in the laboratory by adapting the p.u. bases of preexisting scaled-down equipment is presented. The performance of the method in question, named HISM, was tested by comparing the harmonic content of the output current of a simulated FSC with the measured ones of an SDC in a PHIL setup. The HISM, as demonstrated in this article, can be used by researchers to avoid being misled towards controller stability issues when higher ripple currents are seen during PHIL simulations. In fact, such issues could be caused by bad scaling methods as seen in the Case 2 results in Section VI. In summary, the HISM provides the means to better reproduce harmonic distortions and power quality phenomena of real-life full-size power converters in PHIL tests reducing the need for customization of available laboratory power converters.

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