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A Dual-Source Self-Balanced Switched-Capacitor Reduced Switch Multilevel Inverter With Extending Ability

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ABSTRACT Multilevel inverters (MLIs) with switched-capacitor (SC) combinations are widely recognized to improve the power quality and efficiency of the renewable energy and high-frequency power distribution systems. Self-balancing of SCs and voltage boosting ability are the salient features of the recently developed SC MLIs. This work presents a new SC MLI structure using a reduced number of switches and two dc sources. For increasing the voltage levels, the basic units of the proposed MLI can be extended without increasing the number of dc sources. By suitable charging-discharging patterns, the SCs are self-balanced and voltage boosting is achieved. Comparative analysis with prior-art MLIs demonstrates the merit of topological advancement. Further, extensive simulation and experimental results confirm the feasibility of the proposed MLI under different loading and dynamic operating conditions.

INDEX TERMS DC-AC power conversion, multilevel inverter (MLI), reduced components, self-balancing, switched-capacitor, voltage gain.

I. INTRODUCTION

Multilevel inverters (MLIs) are the suitable choice for renewable power generation, variable speed drives, and high-frequency power distribution [1]–[3] due to the abilities such as enhanced power quality, high modularity, improved efficiency, and low voltage stress. The conventional neutral point clamped MLI (NPC MLI) and flying capacitor MLI (FC MLI) uses a single dc source, whereas the cascaded H-bridge MLI (CHB MLI) consists of several isolated dc sources. The conventional CHB MLI dominates over the other two types due to the features such as high modularity, smooth fault handling capability, and high reliability [2], [4]. However, these conventional structures need a large number of switches, driver circuits, and passive components. Moreover, the additional voltage balancing and inverter module failure issues [5] also exists in the NPC MLI and FC MLI. Therefore, the research interest is growing to redesign the MLI using a

lower number of components and to enable inherent voltage boosting.

In view of different applications, many alternative topologies are developed in recent years that take into account reduction in both the number of switches and source count [1], [6]. These MLIs can be broadly categorized into two types, *i.e.*, switched-dc/diode (SD) type and switched-capacitor (SC) type. Further, these MLIs can be single-dc or multi-dc type. The multi-dc MLIs can be symmetric or asymmetric type based on the magnitude of the dc sources. Multi-terminal SD MLI as disclosed in [7] reduces the switch count, but the number of dc sources remains the same as the conventional MLI. The generalized SD MLI in [8] avoids the back-end full-bridge to synthesize negative voltage levels and thus reduces the voltage stress. To achieve higher number of voltage levels at the output, the CHB MLI topology is modified in [4], [9] by connecting level doubling circuit to it. Self-balanced capacitors are used to reduce the utilization of the dc source significantly. SD MLI topology disclosed in [10] for the photovoltaic (PV) application uses the similar concept.

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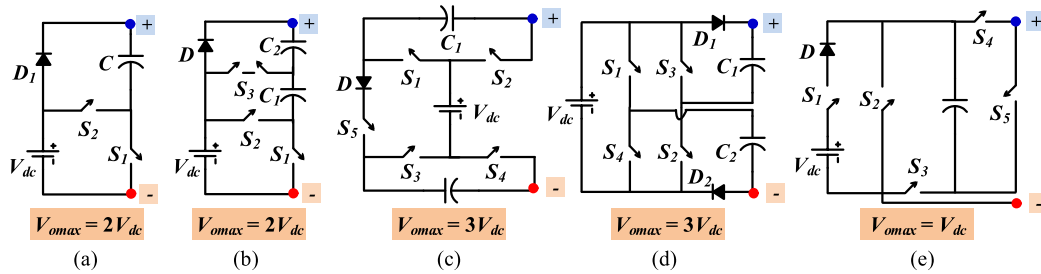


FIGURE 1. Switched-capacitor modules proposed in (a) [14], [17], [21], (b) [22], (c) [19], (d) [27], (e) [31].

The structure presented in [11] can be extended for producing higher voltage steps and it is suitable for the standalone PV systems. These structures reduce the switch/drivers count considerably and possess a simpler control circuit. However, these MLIs lack the ability to boost the voltage.

A novel approach is suggested in [12] to reduce the dc source count utilizing capacitors in the circuit. This topology can operate in symmetrical as well as in asymmetrical mode. Thus, maximum voltage steps can be created at the output by selecting the magnitude of the dc sources asymmetrically. The SC MLIs proposed in [13] requires additional sensors and voltage balancing controller to regulate the capacitor voltage. Unlike these topologies, new reduced switch SC MLIs are proposed to inherently boost the output voltage without using large-sized transformers and inductors. The generalized SC MLI structures introduced in [14]–[16] can inherently charge the capacitors and features high voltage boosting. The capacitors are self-regulated at the desired voltage using the series-parallel charging-discharging technique. The SC MLI structure proposed in [17], [18] also features high voltage gain, but a modified H-bridge is used in the circuit and thus, the voltage stress is very low. Multi-dc SC MLIs are further explored in [19], [20], which avoids the use of conventional H-bridge. The SCs in the MLI proposed in [21], [22] are charged to asymmetrical voltage and thus can generate more levels using less number of switches. The SC MLI structures disclosed in [23], [24] uses only two dc sources. These topologies have the possibility of cascaded extension for enhancing the voltage level, however; the topology in [24] doesn't require the additional dc sources in doing so.

Furthermore, single dc SC MLIs have been proposed in [3], [15], [25], which uses a back-end H-bridge for changing the polarity. High voltage boosting is achieved in [15], [25], but at the cost of a large number of switches. Due to the presence of series-diodes in the conducting path, the topology [25] is inadequate for operating with high inductive loading. The capacitor current spikes are effectively reduced using the SC MLI proposed in [3]. However, this topology is inefficient to boost the voltage magnitude. Also, without using the conventional H-bridge new single dc SC MLIs have been emerged. The disclosed MLI in [26] generates 5-level output with twice voltage boosting. The MLIs in [27] and [28], [29] can generate a 7-level output with 3 times and 1.5 times voltage

boosting, respectively. The former topology features single-phase extendibility, whereas the latter has the flexibility to extend in three-phase as well. A single-dc extendable MLI proposed in [30] requires a large number of switches. Single dc 9-level and 17-level SC MLIs proposed in [31] and [32], respectively have the quadrupled boosting ability. The voltage stress reduction is significantly achieved, sacrificing the switch count. The evolution of self-balanced SC modules is depicted in Fig. 1.

Motivated by the recent developments, this work presents a novel MLI topology with following salient features:

- i. Total number of switches and capacitors per level is significantly reduced.
- ii. Only two dc sources are employed to produce N_l -level output, thus reduces total cost of the MLI.
- iii. The capacitors used in the proposed topology are charged through a common switch, possess self-balancing ability and assists voltage boosting.
- iv. Less than 50 % of the switches are in conduction for any voltage level and more than 50 % of switches operate at a lower frequency. Thus, the total power loss is very less.
- v. The proposed MLI can satisfactorily operate under high as well as low power factor loads.

The next section introduces the proposed topology including the capacitor sizing and self-balancing mechanism. A comparison with the prior-art MLIs in Section III confirms the topological advancement by extensive comparison. Section IV and V discuss extensive simulation and experimental investigation, respectively, for different dynamic conditions to validate the workability of the 25-level SC MLI. Concluding remarks are provided in Section VI.

II. PROPOSED TOPOLOGY AND DESIGN ANALYSIS

A. RECENTLY DEVELOPED 25-LEVEL SC MLIs

The circuit schematic of the recently proposed 25-level multi-input SC MLIs for renewable energy applications is shown in Fig. 2. The developed MLI in [19] consists of four sub-modules. Each module can boost the voltage magnitude to three-times. For synthesizing a 25-level output, this topology requires 4 dc sources, 8 capacitors, and 30 switches. Similar to this MLI, the topology proposed in [20] can operate in both symmetrical and asymmetrical modes. This MLI however, lacks the ability to boost the voltage. The source count is also increased for the 25-level operation considering the

symmetrical topology. Topology developed in [16] requires only 2 asymmetrical dc sources in the ratio 1:2 and 2 capacitors for generating a 25-level output. The switch count is almost halved compared to the other two types. On the other hand, the source count increases when the topology is extended for high voltage levels. The 25-level topology presented in [24] requires only two input dc sources and a very large number of switches. However, due to the presence of internal boost converter a high voltage gain can be obtained. Moreover, additional dc sources are not required in order to synthesize higher voltage levels.

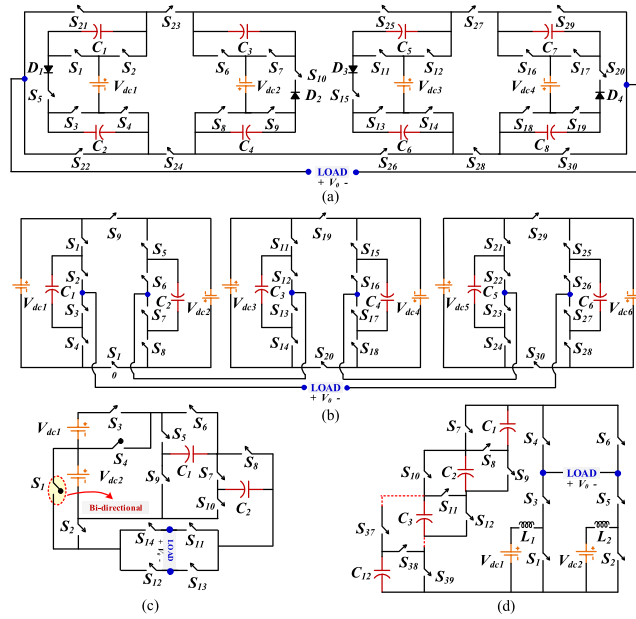


FIGURE 2. Recent-art 25-level SC MLIs: (a) [19], (b) [20], (c) [16], (d) [24].

B. PROPOSED SC MLI TOPOLOGY

The proposed dual-source switched-capacitor (DSC) MLI comprising of two input sources (N_{dc}) and several repeating units (RU) is shown in Fig. 3(a). The RU consists of two switches, one capacitor, and a diode. Two input sources are chosen with a proportional factor of ‘x’, which can be any integer, but the optimal value of it to synthesize symmetrical voltage steps can be selected using (1). The required number of switches (N_{sw}), drivers (N_{driv}), diodes (N_{dd}), capacitors (N_c), and the number of voltage levels (N_l) in terms of the n RUs is given in (2-5). Moreover, total standing voltage (TSV) is computed as per (6) for the proposed MLI by adding the individual voltage stress of the switches. The diodes D_1 - D_n and the switch S_c is used to provide a path for charging of the capacitors C_1 to C_n .

$$x = n + 2 \tag{1}$$

$$N_{sw} = N_{driv} + 1 = 2n + 10 \tag{2}$$

$$N_{dd} = n \tag{3}$$

$$N_c = n + 1 \tag{4}$$

$$N_l = 8n + 9 \tag{5}$$

$$TSV = [(14n + 12)/(n + 2)] V_{dc} \tag{6}$$

In the present work, two RUs ($n = 2$) are considered. Thus, the DSC MLI synthesizes a 25-level staircase output voltage (V_o) for which the circuit operation is shown in Fig. 3(b). The two inputs (V_{dc} & $V_{dc}/4$) of the MLI appear at the output through the switches S_{1a} (bidirectional) and S_{2a} . The capacitors C_1 and C_2 are symmetrically charged to the low-input voltage magnitude ($V_{dc}/4$) through the devices D_1 , D_2 , and S_c during the B- to C+ switching states. A key advantage of the proposed MLI is that the capacitors C_1 , C_2, \dots, C_n are self-charged through a common switch S_c . These capacitors can also be charged to the higher input source magnitude. However, this may be avoided as it will block the conduction of the inbuilt diode of switches S_1 and S_3 . Moreover, C_1 and C_2 discharge to the load through S_2 and S_4 , respectively. The capacitor C_b is alternatively charged throughout the negative-half cycle and discharges to the load in a similar pattern in the positive-half cycle. S_{5b} and S_{6b} are used to connect C_b in series with the load and to bypass it, respectively. The voltage across the capacitor C_b is maintained such that it creates the intermediate voltage steps, which double the number of levels. Fig. 3(b) illustrates the circuit operation of the 25-level proposed MLI up to G+ and G- states. Subsequent voltage steps are generated in a similar fashion, but by complementing the states of S_{1a} and S_{2a} . The complete switching mechanism of the proposed MLI to synthesize 25-level along with capacitor charging (\uparrow) and discharging (\downarrow) modes are illustrated in Table 1. Due to operation of four switches at fundamental frequency, the total power loss is very less. Further, the proposed MLI can satisfactorily operate under high and low power factor loads due to the existence of both forward and backflow current path.

C. DESIGN AND SELF-BALANCING OF THE CAPACITORS

Longest discharging period (LDP) of the capacitors over a fundamental period is taken into account to determine the capacitance values [15], [27]. LDP is the time duration during which a capacitor discharges the maximum stored charge, as indicated in Fig. 4(a). The discharging quantity of the capacitor depends on both LDP and type of loading, which is given in (7-9). Thereby, the optimal value of the capacitance for the DSC MLI is expressed in (10), where γ is the acceptable percentage voltage ripple.

$$\Delta Q_{C1} = 2 \int_{t_9}^{T/4} I_{omax} \sin(\omega t - \Phi) dt \tag{7}$$

$$\Delta Q_{C2} = 2 \int_{t_{11}}^{T/4} I_{omax} \sin(\omega t - \Phi) dt \tag{8}$$

$$\Delta Q_{Cb} = 6 \int_{t_{11}}^{t_{12}} I_{omax} \sin(\omega t - \Phi) dt \tag{9}$$

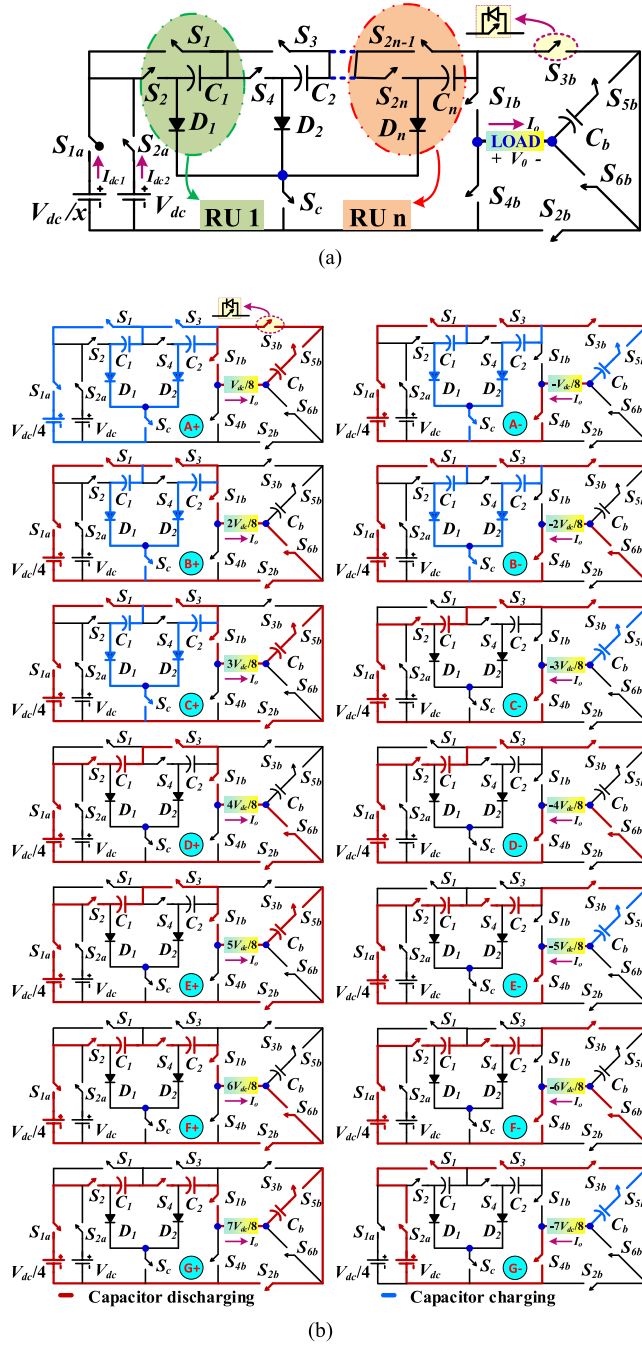


FIGURE 3. (a) Generalized structure of the proposed DSC MLI, (b) Circuit operation of 25-level DSC MLI.

$$C_1 \geq \frac{\Delta Q_{C1}}{\gamma V_{c1}}, C_2 \geq \frac{\Delta Q_{C2}}{\gamma V_{c2}} \text{ and } C_3 \geq \frac{\Delta Q_{C3}}{\gamma V_{c3}} \quad (10)$$

where Φ is the lagging angle between the load current (I_o) and fundamental voltage, I_{omax} is the peak fundamental load current. Considering 240 V (V_{dc}), 80 Ω -variable inductive loading, and the output frequency of 50 Hz, variation in capacitance with respect to phase angle (Φ) is shown in Fig. 4(b)-(d) for different value of γ (5 %, 7 %, 10 % and 15 %). The figure implies that capacitors can be optimally

TABLE 1. Conduction states of the 25-level DSC MLI.

States	Conducting devices	C_b	C_1	C_2	V_o
L+	$S_{2a}-S_2-S_4-S_{1b}-S_{6b}-S_{2b}$	-	↓	↓	$12V_{dc}/8$
K+	$S_{2a}-S_2-S_3-S_{1b}-S_{5b}-S_{2b}$	↓	↓	-	$11V_{dc}/8$
J+	$S_{2a}-S_2-S_3-S_{1b}-S_{6b}-S_{2b}$	-	↓	-	$10V_{dc}/8$
I+	$S_{2a}-S_1-S_3-S_{1b}-S_{5b}-S_{2b}$	↓	-	-	$9V_{dc}/8$
H+	$S_{2a}-S_1-S_3-S_{1b}-S_{6b}-S_{2b}$	-	-	-	$8V_{dc}/8$
G+	$S_{1a}-S_2-S_4-S_{1b}-S_{5b}-S_{2b}$	↓	↓	↓	$7V_{dc}/8$
F+	$S_{1a}-S_2-S_4-S_{1b}-S_{6b}-S_{2b}$	-	↓	↓	$6V_{dc}/8$
E+	$S_{1a}-S_2-S_3-S_{1b}-S_{5b}-S_{2b}$	↓	↓	-	$5V_{dc}/8$
D+	$S_{1a}-S_2-S_3-S_{1b}-S_{6b}-S_{2b}$	-	↓	-	$4V_{dc}/8$
C+	$S_{1a}-S_1-S_3-S_{1b}-S_{5b}-S_{2b}$	↓	↑	↑	$3V_{dc}/8$
B+	$S_{1a}-S_1-S_3-S_{1b}-S_{6b}-S_{2b}$	-	↑	↑	$2V_{dc}/8$
A+	$S_{5b}-S_{3b}-S_{1b}$	↓	↑	↑	$V_{dc}/8$
O	$S_{1b}-S_{6b}-S_{3b}$	-	↑	↑	0
A-	$S_{1a}-S_1-S_3-S_{3b}-S_{5b}-S_{4b}$	↑	↑	↑	$-V_{dc}/8$
B-	$S_{1a}-S_1-S_3-S_{3b}-S_{6b}-S_{4b}$	-	↑	↑	$-2V_{dc}/8$
C-	$S_{1a}-S_2-S_3-S_{3b}-S_{5b}-S_{4b}$	↑	↓	-	$-3V_{dc}/8$
D-	$S_{1a}-S_2-S_3-S_{3b}-S_{6b}-S_{4b}$	-	↓	-	$-4V_{dc}/8$
E-	$S_{1a}-S_2-S_4-S_{3b}-S_{5b}-S_{4b}$	↑	↓	↓	$-5V_{dc}/8$
F-	$S_{1a}-S_2-S_4-S_{3b}-S_{6b}-S_{4b}$	-	↓	↓	$-6V_{dc}/8$
G-	$S_{2a}-S_1-S_3-S_{3b}-S_{5b}-S_{4b}$	↑	-	-	$-7V_{dc}/8$
H-	$S_{2a}-S_1-S_3-S_{3b}-S_{6b}-S_{4b}$	-	-	-	$-8V_{dc}/8$
I-	$S_{2a}-S_2-S_3-S_{3b}-S_{5b}-S_{4b}$	↑	↓	-	$-9V_{dc}/8$
J-	$S_{2a}-S_2-S_3-S_{3b}-S_{6b}-S_{4b}$	-	↓	-	$-10V_{dc}/8$
K-	$S_{2a}-S_2-S_4-S_{3b}-S_{5b}-S_{4b}$	↑	↓	↓	$-11V_{dc}/8$
L-	$S_{2a}-S_2-S_4-S_{3b}-S_{6b}-S_{4b}$	-	↓	↓	$-12V_{dc}/8$

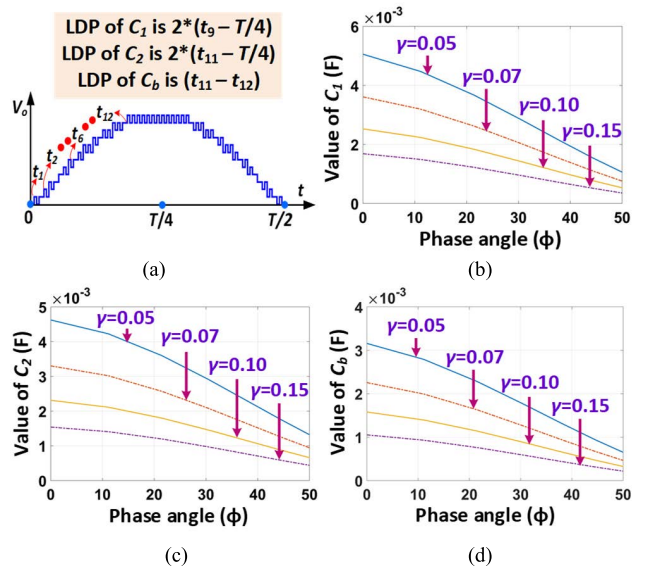


FIGURE 4. (a) Half cycle of the 25-level output with LDP, (b) Value of C_1 vs Φ , (c) Value of C_2 vs Φ , (d) Value of C_b vs Φ .

selected keeping in mind the allowable voltage ripple limit and the loading value.

Furthermore, all the capacitor voltages in the DSC MLI are inherently balanced at the desired value without the need of any closed-loop control circuit. The voltage across the capacitors C_1 , C_2 of the proposed DSC MLI are self-regulated at the desired level ($V_{dc}/4$) using series-parallel technique [25] and suitable sizing of capacitors. These capacitors discharge in series with the source according to the conduction states in

Table 1. The capacitors are brought in parallel with the source to charge in each cycle, thus maintaining the desired voltage across it.

Alongside, the voltage across the capacitor C_b is self-balanced using the level doubling principle [10], which is mathematically verified here. Fig. 5 delineates the equivalent circuit and current flow path during charging-discharging of C_b to generate $\pm 7V_{dc}/8$ at the output. The average current flowing through the capacitor (I_{cb}) during these instances with net impedance z is expressed as follows:

$$I_{cb}(+) = \frac{2V_{dc}/8 + 4V_{dc}/8 - 7V_{dc}/8 + V_{Cb}}{Z} \quad (11)$$

$$I_{cb}(-) = \frac{V_{dc} - V_{Cb} - 7V_{dc}/8}{z} \quad (12)$$

Therefore, net charge (q) absorbed or delivered by C_b over a period of T can be expressed as,

$$q = [I_{cb}(+) - I_{cb}(-)]T = \left[\frac{2V_{Cb} - 2V_{dc}/8}{z} \right] T \quad (13)$$

Net charge absorbed or delivered by C_b in the steady-state is zero. Thus, simplifying (13) gives $V_{Cb} = V_{dc}/8$. Therefore, the voltage across C_b automatically reaches the desired level ($V_{dc}/8$) and thereby enhances the voltage level.

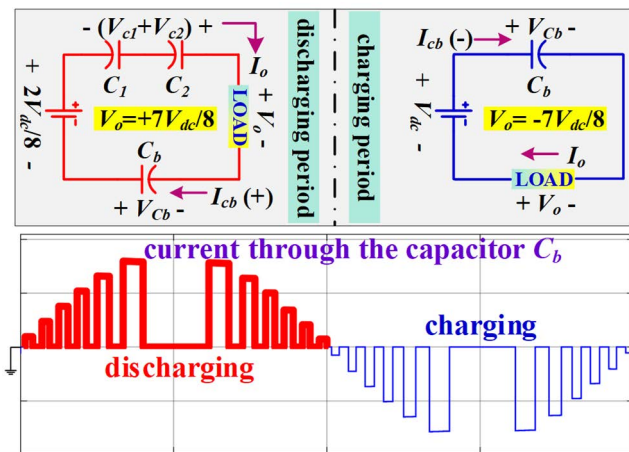


FIGURE 5. Charging and discharging of capacitor C_b with current through it.

III. COMPARATIVE ANALYSIS

In order to investigate the merits of the proposed DSC MLI, a comparison with several state-of-art MLIs is carried out. It is evident from Table 2 that the proposed DSC MLI involves 14 semiconductor switches and 13 drivers, which is lowest among all the recent-art topologies. The single-dc MLI in [31] requires a large number of switches to generate the same output but with minimum stress across the switches. Fig. 6(a) depicts the N_l -level DSC MLI also requires least switch count when compared against similar extendable MLIs (T1 [25], T2 [15], T3 [3], T4 [22], T5 [7], T6 [21], T7 [27], T8 [30], T9 [14], T10 [29], T11 [31]). Compared to the proposed MLI, the single-dc MLI in [25] requires a significantly

more series diodes in the load current flow path, thus this topology does not have the inductive loading ability (ILA). The proposed MLI ranks the second-lowest in terms of the capacitors requirement. The MLI disclosed in [16] requires a minimum number of capacitors, whereas the stress across all the capacitors is more than or equal to the total input voltage (N_{cs}), in contrast to the proposed MLI. With reduction in total switch count, the number of maximum devices in conduction (N_{mc}) also drastically reduced for the proposed circuit. Despite using a large number of capacitors and multiple sources in the 25-level circuit [20], the capacitor voltages cannot be added with the dc sources during maximum voltage level generation. Thus, except the MLIs disclosed in [20], all other compared MLIs, including the proposed MLI have the boosting ability (BA).

Moreover, the cost factor (CF) is evaluated for the MLIs considering the sum of number of components (N_{sw} , N_{driv} , N_{dd} , N_c , N_{dc}) and per unit TSV [8]. The weightage coefficient (w) is considered 1, in case of equal weightage to the switch count and the TSV. For more weightage to the number of switches, $w < 1$ and $w > 1$ when more weightage to the TSV is considered. The proposed MLI stands superior with respect to the overall CF, as can be verified from Table 2 and Fig. 6(b). The comparison in terms of output frequency demonstrates the SC MLIs are suitable in high-frequency power distribution systems. Various controllers are used to test the feasibility of the MLIs at different power levels, which is also summarized in Table 2. The distinctive features of the proposed DSC MLI ascertain the proposed MLI is one of the suitable alternatives to synthesize high-quality output voltage using the least number of components.

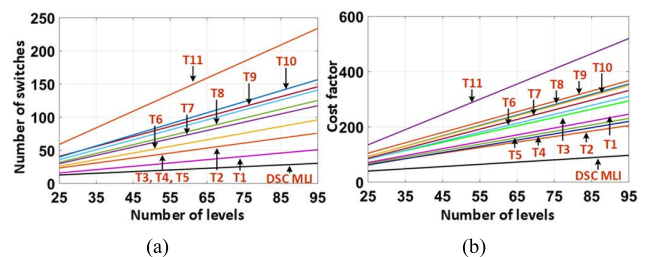


FIGURE 6. Comparison of the extended MLIs: (a) Number of switches vs number of levels, (b) CF ($w = 1$) vs number of levels.

IV. SIMULATION ANALYSIS

The simulation analysis of the proposed MLI with two RUs to generate 25-level output is performed in the MATLAB/SIMULINK environment. The dual dc sources are selected as 60 V (V_{dc1}) and 240 V (V_{dc2}). The IGBTs with an anti-parallel diode are taken as the switching devices, capacitor C_1 , C_2 is chosen as 4700 μ F and C_b as 3300 μ F. The carrier frequency and output frequencies are chosen as 5 kHz and 50 Hz, respectively. Phase-disposition PWM control scheme based on high switching frequency [26], [29], [31] is adopted to control the proposed MLI.

TABLE 2. Comparison of 25-level state-of-art SC MLIs.

Topologies	N_{sw}	N_{driv}	N_{du}	N_c	N_{dc}	N_{mc}	N_{cs}	CF/ N_i ($w = 0.5$)	CF/ N_i ($w = 1$)	CF/ N_i ($w = 1.5$)	output frequency (Hz)	output power ($\approx W$)	ILA	BA	Controller type
[31]	59	59	11	11	1	35	11	5.74	5.84	5.94	50 & 1k	200	Yes	Yes	DSP
[30]	41	34	10	12	1	27	12	4.06	4.19	4.33	50 & 500	1k	Yes	Yes	ATMEGA16
[29]	40	40	0	12	4	24	4	3.95	4.05	4.16	50	250	Yes	Yes	DSP
[24]	39	39	0	12	2	25	12	3.82	3.96	4.10	50	300	Yes	Yes	dSpace
[27]	32	32	8	8	4	24	8	3.47	3.57	3.68	400	200	Yes	Yes	DSP
[21]	30	30	6	6	6	15	0	3.22	3.32	3.42	50	800	Yes	Yes	PIC
[19]	30	30	4	8	4	22	4	3.15	3.27	3.38	50	250	Yes	Yes	dSpace
[20]	30	30	0	6	6	15	0	2.96	3.04	3.12	50	4k	Yes	No	dSpace
[23]	28	22	0	4	4	12	4	2.43	2.53	2.64	50	60	Yes	Yes	ATMEGA16
[17]	26	26	10	10	2	11	10	3.09	3.22	3.35	50	1k	Yes	Yes	--
[22]	26	20	3	6	3	15	6	2.41	2.51	2.60	50	1k	Yes	Yes	PIC
[25]	16	16	22	11	1	25	11	2.76	2.87	2.99	50 & 400	350	No	Yes	--
[26]	16	14	8	4	2	14	4	1.85	1.94	2.03	50	500	Yes	Yes	DSP
[16]	16	14	2	2	2	9	2	1.60	1.76	1.92	50	500	Yes	Yes	RTDS
DSC MLI	14	13	2	3	2	9	0	1.49	1.63	1.76	50 & 500	1k	Yes	Yes	DSP

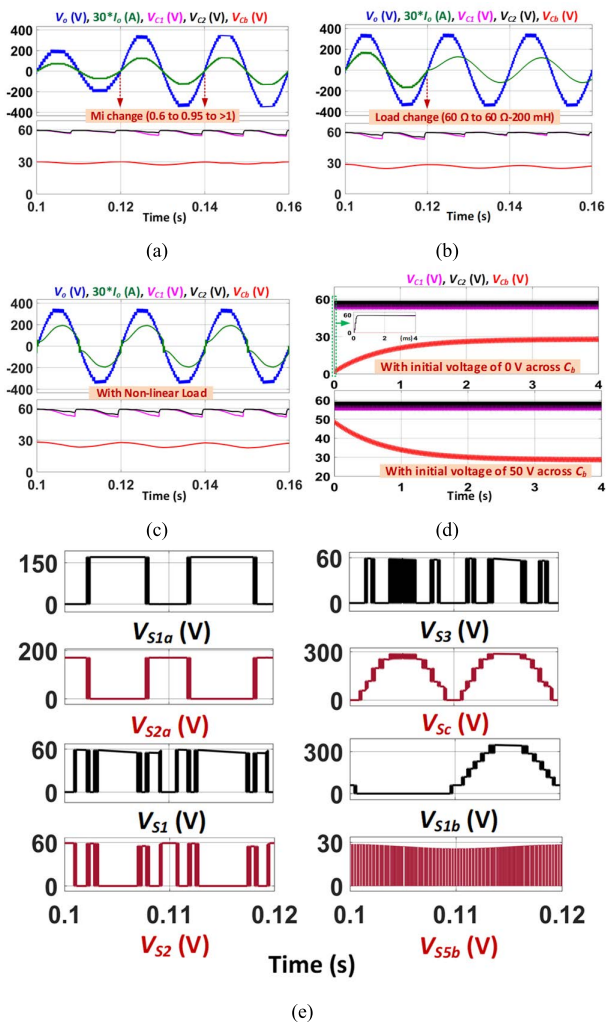


FIGURE 7. Simulation analysis: V_o , I_o , V_{C1} , V_{C2} , and V_{Cb} under (a) Change in M_i , (b) Dynamic loading condition, (c) Non-linear loading, (d) Capacitor voltages with different initial voltage across C_b , (e) Standing voltage across few switches.

First, the MLI is tested under varying modulation index (M_i) and fixed loading (80Ω) condition. It can be

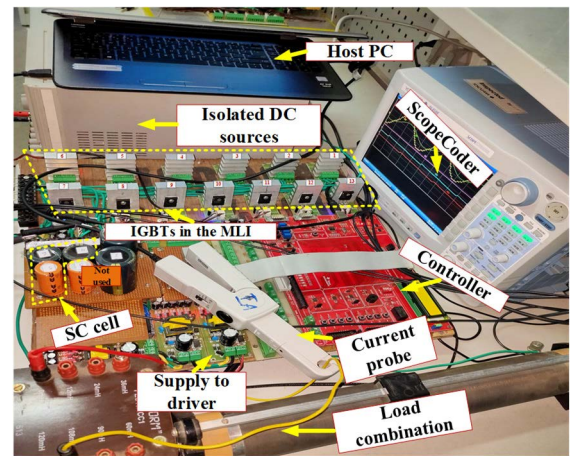


FIGURE 8. Experimental test setup developed in the laboratory.

observed from Fig. 7(a) that, at 0.6 M_i some voltage steps are elapsed and the MLI operates at reduced voltage levels. At $M_i > 1$, the voltage level is disturbed that contributes to more harmonics in the output voltage. Therefore, M_i is fixed at 0.95 to validate the effective working in other dynamic test cases. Fig. 7(b) shows the operation of the DSC MLI under dynamic loading condition, where loading is changed from unity power factor (PF) to low PF. Output current (I_o) is a 25-level stepped waveform similar to output voltage (V_o) during pure resistive loading, however, attains a sinusoidal-like waveform for the inductive type loading. The capacitor voltages (V_{Cb} , V_{C1} , & V_{C2}) are also presented, which implies the decrease in capacitor voltage ripple as the load is switched to highly inductive. The working of the proposed MLI is also verified under non-linear loading condition. A diode bridge rectifier is used as a non-linear load with 50Ω -50 mH loading and the output waveform is illustrated in Fig. 7(c). All the voltage levels in V_o are retained, although the ripples in the capacitor voltages are comparatively more. The average value of the capacitor voltages is maintained at the desired magnitude under all the above operating conditions. Results

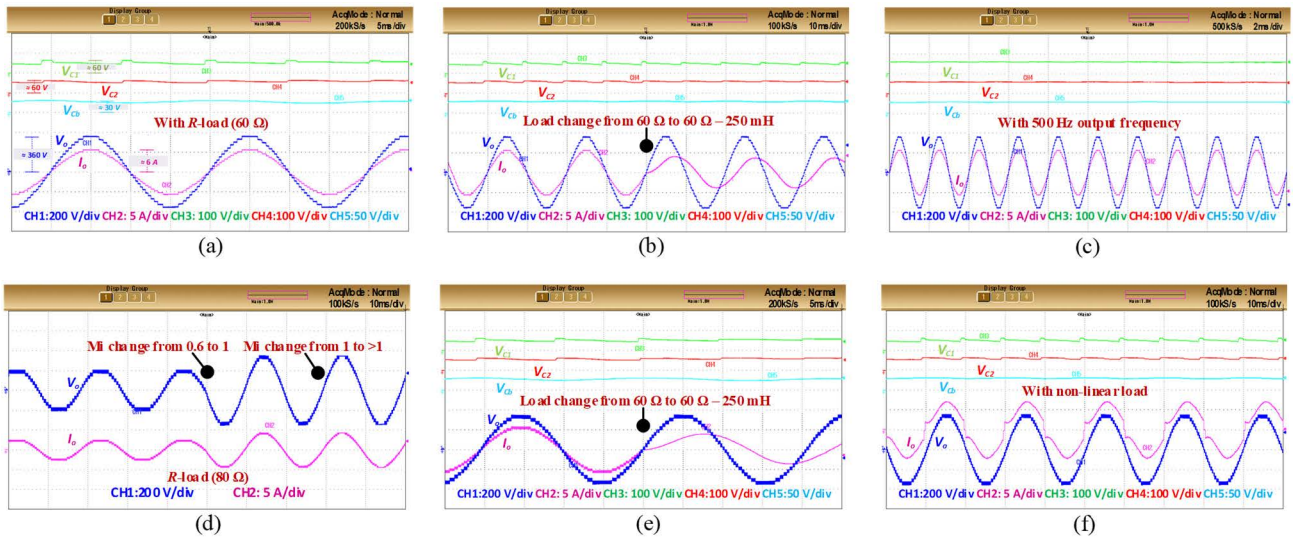


FIGURE 9. Experimental analysis: fundamental frequency modulation: (a) under pure resistive loading, (b) results under dynamic loading (R to RL), (c) results under 500 Hz output frequency, high-frequency modulation: (d) under varying M_i condition, (e) results under dynamic loading (R to RL), (f) results under non-linear loading.

acquired in Fig. 7(d) with a different initial voltage across the capacitor C_b implies the inherent-balancing ability of the capacitors.

To verify the blocking voltage of the switches, voltage stress across the switches is presented in Fig. 7(e). For the 25-level operation, the switches S_{1a} , S_{2a} blocks the voltage $3V_{dc}/4$, switches S_1, \dots, S_4 blocks the voltage $V_{dc}/4$, switch S_c blocks the voltage $5V_{dc}/4$, switches S_{1b}, \dots, S_{4b} blocks the voltage $3V_{dc}/2$, and switches S_{5b} , S_{6b} blocks the voltage $V_{dc}/8$. Therefore, the TSV of the 25-level DSC MLI is $10V_{dc}$, which is in accordance with the expression (6).

V. EXPERIMENTAL VERIFICATION

In order to verify the feasibility of the proposed 25-level DSC MLI, an experimental test circuit as shown in Fig. 8 comprising IGBT switches (12N60A4D:600 V) and discrete diodes (MUR860:600 V) is devised in the laboratory. The value of the three capacitors C_1 , C_2 and C_b are chosen as $C_1, C_2 = 4700 \mu\text{F}$ ($R_{int} = 31 \text{ m}\Omega$), $C_b = 3300 \mu\text{F}$ ($R_{int} = 56 \text{ m}\Omega$), considering the voltage ripple of 5-7%. The input supply voltages are set to 60 V (V_{dc1}) and 240 V (V_{dc2}) using programmable dc supplies. A DSP controller is utilized for the real-time pulse generation. Pulses are generated using MATLAB/Simulink-DSP interfacing. The Simulink model of the 25-level MLI is created in CC studio and downloaded to the DSP. The pulses from the controller are amplified using the TLP250 driver circuit, which also provides the required isolation between the control and power circuit. All the output waveforms are acquired with the help of a ScopeCoder (DL850E) and the power quality analysis is carried out using the analyzer (WT1800). The experimental tests are conducted using both a fundamental frequency switching

scheme [10], [11] and high-frequency modulation scheme [26], [29], [31].

Fig. 9(a)-(c) depicts the results under the fundamental frequency switching scheme. The results are shown in Fig. 9(a) and (b) with R -load and sudden change in load from R to RL , respectively for a 50 Hz output frequency. The desired 25-level output, self-balancing of capacitors, change in ripple and change in load current pattern due to sudden variation in loading can be inferred from the results. As highlighted earlier, SC MLIs are widely used in high-frequency power distribution systems due to its advantages such as reduction in capacitor voltage ripple, low inrush current and high-quality output voltage. To verify the feasibility of the proposed MLI in high-frequency systems, waveforms are acquired in Fig. 9(c) with 500 Hz output frequency. It is noteworthy that, appearance of high inrush current (about 10-15 times the load current) in the capacitors during the charging process is apparent in all the SC MLIs reported to date. However, the inrush current is though difficult to mitigate completely but can be reduced significantly (\approx about 5-10 times the load current) using a small inductor in the charging path. Suitable inductance can be chosen based on the current ripple, ripple voltage, input voltage and loading value to avoid unwanted delay in charging. The other methods of reducing the inrush current is to choose suitable equivalent series resistance or impedance based source integration with the SC configuration [33].

The test results are acquired under the high-frequency (switching frequency of 5 kHz) modulation scheme in Fig. 9(d)-(f). Similar to the simulation results, the output voltage of the MLI is shown under dynamic varying M_i condition in Fig. 9(d) and sudden load transient in Fig. 9(e). It can be observed that at M_i value near to unity, the desired

symmetrical 25-levels are attained and the voltage waveform is undistorted with the change in loading. Fig. 9(f) depicts the non-linear load handling ability of the proposed circuit. The change in only load current waveshape without affecting the load voltage verifies the operation. The inherent capacitor voltage balancing under different transient conditions fully establish the workability of the proposed MLI.

Furthermore, power losses are evaluated under 60 Ω-50 mH loading and fundamental switching scheme. Fig. 10(a) depicts the ohmic loss and switching loss on the switches (P_{oh-sw} , P_{s-sw}) and anti-parallel diodes (P_{oh-dd} , P_{s-dd}). The total power loss excluding the ripple power loss is about 18.03 W for ≈1 kW output power. The power quality analyzer results under 60 Ω-50 mH loading and 60 Ω-250 mH loading are shown in Fig. 10(b). The active power (P) decreases from ≈1 kW to 400 W and the reactive power (Q) increases with the change in PF (λ). The frequency of the output voltage is maintained at 50 Hz. The measured efficiency (η) of the proposed MLI, voltage THD and current THD are also depicted in the result. However, it is noteworthy that the efficiency may vary with the loading and device/power rating of the MLI.

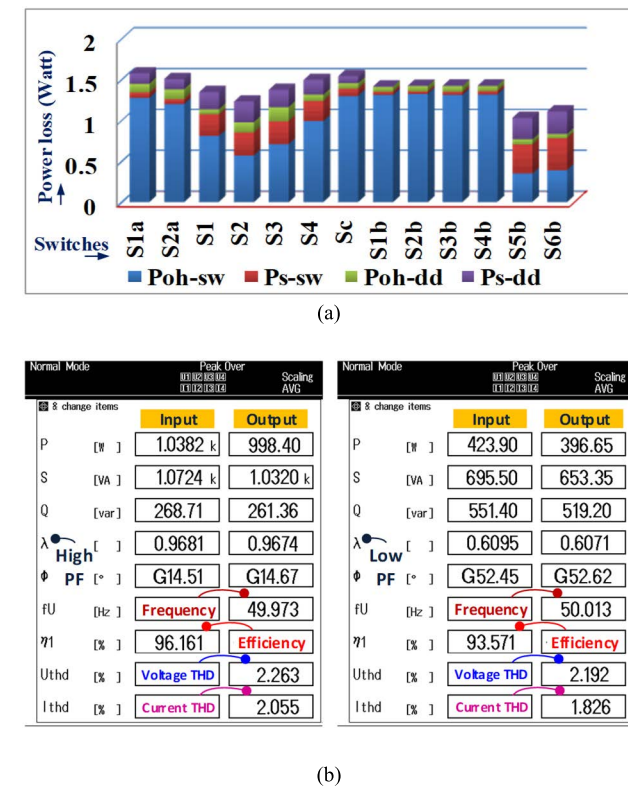


FIGURE 10. (a) Losses on the switches, (b) Performance parameters obtained using the WT1800 analyzer under different loading (high PF and low PF).

VI. CONCLUSION

A novel DSC MLI with extending ability using a reduced number of switches and two dc sources has been introduced

in this work. For the 25-level operation, minimum number of switches with two diodes, and three capacitors are employed. Capacitors are arranged in such a way that, the source count is reduced as well as the use of external balancing control is avoided. The design and voltage balancing ability of the capacitors has been established. The capacitors C_1 and C_2 are self-charged using series-parallel charge balancing principle and assist the voltage magnitude boosting. On the other hand, the capacitor C_b is self-balanced using the level doubling principle that assists voltage level enhancement. The distinct features of the proposed MLI have been verified with a fair comparison with state-of-art MLIs. Simulation results under dynamic Mi change and linear/non-linear loading conditions validates the successive operation of 25-level MLI. The experimental analysis further demonstrates the real-time workability and inherent balancing features of the DSC MLI.

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