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Nwise and Pwise: 10T Radiation Hardened SRAM Cells for Space Applications With High Reliability Requirements

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ABSTRACT SRAM cells are widely used to design memory blocks of, e.g., caches, register files, and translation lookaside buffers. Depending on the SRAM application, the design requirements are different. For instance, in space applications, alongside energy efficiency, reliability is a main issue since the system is launched into space with a limited energy budget and stays exposed to high doses of radiation strikes for a long time. The Nwise cell has recently been proposed by the authors of this paper as the first highly reliable radiation hardened SRAM cell designed with 28nm FD-SOI. In this paper, inspired from the Nwise cell, we introduce another highly reliable radiation hardened SRAM cell, the Pwise cell, which is also designed with 28nm FD-SOI technology. Through comprehensive simulations of state-of-the-art cells, we show that both the Nwise and Pwise cells are competitive radiation hardened SRAMs to use in different memory blocks for space applications: 1) Both have the highest level of Single Event Upsets (SEU) tolerance capability for the temperature range deployed in space applications; further, both have the highest level of the tolerance capability to Multi Event Upsets (MEU). 2) Compared with the simulated cells that have comparable tolerance capability, the Nwise cell has low read delay and read power consumption, hence, it can be a good choice for space application cache designs, while the Pwise cell can be a proper candidate for space application register file designs since it has low write and read delay.

INDEX TERMS 28nm FD-SOI, Nwise cell, Pwise cell, radiation hardening, reliability, multiple event upset (MEU), single event upset (SEU), soft errors, space applications, SRAM design.

I. INTRODUCTION

SRAM cells are widely used to design storage blocks of digital processing systems such as cache memories, register files, and translation lookaside buffers. Hence, they occupy a large part of the processors [1] and play a key role in determining the performance and power consumption of the systems. In the electronics space industry, having energy efficient and robust SRAM cell designs is an important key factor because the systems stay exposed to high doses of radiation strikes for a long time with a limited energy budget [9].

If a radiation strike hits an SRAM cell node and alters the stored data of the SRAM, a Single Event Upset (SEU) occurs [9]. This happens when the charge deposited by the particle strike at the hit node is greater than the critical charge Qcrit. Qcrit is the minimum charge that has to be deposited at a node in order to change the state of the data stored in the SRAM cell [19], [21]. If two or more adjacent nodes share the deposited charge and are involved in the state change, we have what is denoted a Multi Event Upset (MEU) [19].

SEUs (MEUs) may lead to system function disorder causing serious or even fatal errors. Therefore, it is necessary to design SRAM cells with the ability to mitigate the effects of SEUs (MEUs) [9], or phrased differently, with higher tolerability. Several solutions have been proposed focusing on various aspects at the architecture and circuit level to reduce the effects of SEUs (MEUs) in memory designs [2]–[38].

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Although technology scaling according to Moore's law considerably improves computing technology [47], it has led to several unintended consequences. For example, it intensifies radiation effects on SRAM cells because transistors are more prone to noise at lower supply voltages and smaller feature sizes [9]. This motivates researchers to explore alternative solutions to maintain the ability of further scaling.

The Fully Depleted Silicon On Isolator (FD-SOI) technology has emerged as a promising candidate with attractive characteristics such as reduced power consumption and improved reliability compared with corresponding circuits designed with Bulk CMOS technology. FD-SOI is a planar process technology that incorporates an ultra-thin layer of insulator in the substrate to dramatically reduce the leakage current. It also reduces the parasitic capacitance between the source and the drain, thus, improving the electrostatic properties of the transistor, which results in better mobility and less variability and increases the performance of FD-SOI circuits. In addition, the transistor channel, implemented by a very thin silicon film, makes the transistor fully depleted without the need for any channel doping [48], [71]. These valuable properties make FD-SOI an attractive technology for building integrated circuits [56].

Authors of this paper have previously proposed the Nwise cell as the first highly reliable radiation hardened SRAM cell designed with 28nm FD-SOI [55]. Inspired by the Nwise cell, in this paper we introduce another highly reliable radiation hardened SRAM cell, the Pwise cell. Using a different combination of PMOS and NMOS transistors, Pwise is optimized for low write and read delay, compared to low read delay and read power consumption for Nwise, and thus for different types of applications. Like the previous Nwise cell design, we leverage 28nm FD-SOI technology to design the Pwise cell, but in this case both cells are modelled and simulated at layout level. In this paper we also compare Nwise and Pwise with state of the art, using a comprehensive selection of previously proposed area efficient radiation hardened cells that can be used to design high dense memory structures for space applications. The layouts of all cells are drawn with Cadence Virtuoso using a commercial 28nm FD-SOI technology. The simulations are done with Cadence Spectre at nominal voltage level and temperature (1V and 27°C).

The contributions of the paper are as follows:

1- We present an extensive review of previously proposed design solutions on the wide variety of aspects that contribute to providing robustness of memory designs.

2- According to the comprehensive simulations related to robustness, we show that our proposed Nwise and Pwise cells are proper choices for space application designs where the memory circuits stay exposed to high doses of radiation strikes.

3- Compared with the simulated cells that have comparable SEU tolerance capability, the Nwise cell has low read delay and read power consumption making it the right choice for cache memory designs of space application. The Pwise cell can be a proper candidate for register file designs of space applications since it has low write and read delay compared with the simulated cells that have comparable SEU tolerance capability.

4- To the best of our knowledge, the Nwise and Pwise cells are the first area efficient radiation hardened SRAM cells that have been designed with FD-SOI 28nm technology.

The rest of the paper is organized as follows: Section II Preliminaries has three parts; in the first part, we review the SEU injection modeling that we deploy in this paper. In the second part, we briefly describe the FD-SOI structure and its priority over CMOS Bulk designs from a reliability point of view. In the last part, we review recent proposed robust memory designs. In Section III Memory Cell Design Details, we review the Nwise cell [55] and introduce our new proposed Pwise cell. We explain the characteristics of both cells including schematic description, operational behavior, and analyses of SEU and MEU robustness. In Section IV Design Methodology and Simulation Results, we analyze and compare cell costs including area, read and write delay times, read and write power consumption, and three different static noise margins (Hold, Write and Read Static Noise Margins, i.e., HSNM, WSNM, and RSNM) of all tested cells. We also compare robustness simulations including SEU recovery and its behavior during temperature changes, as well as tolerance capability to MEU. Finally, Section V concludes this paper.

II. PRELIMINARIES

In the first part of this section, we review modeling of SEU injection in memory cells. In the second part, we briefly describe the FD-SOI structure as well as its advantages compared with CMOS Bulk. In the last part, we study previous solutions that have been proposed on a wide variety of aspects, at both architecture level and circuit level, to provide robust memory designs.

A. SEU INJECTION MODELING

A Single Event Upset (SEU), changing the data value stored in the SRAM cell, happens when the charge deposited by a particle strike at a hit node is greater than Q_{crit}. Q_{crit} is proportional to supply voltage as well as to the node capacitance and is an accepted metric used to evaluate SEU occurrence [19]. To simulate the effects of a particle strike injection onto a cell node, we employ the model in Equation 1. It was first suggested in [40] and has since been widely used by researchers, for instance in [6], [20], [63]:

$$I(t) = \frac{Q_{dep}}{\tau_f - \tau_r}(e^{\frac{-t}{\tau_f}} - e^{\frac{-t}{\tau_r}}) \tag{1}$$

The equation models a transient double exponential current source where Q_{dep} is the total charge deposited at the hit node due to particle strike. τ_r is the collection time constant of the junction and τ_f is the ion-track establishing time constant. Both are material dependent time constants [40]. According to [41], we set $\tau_r = 1ps$ and $\tau_f = 5ps$ for the considered 28nm FD-SOI technology node.

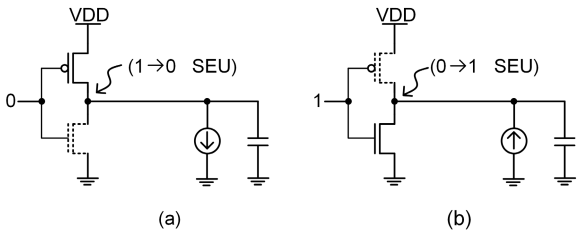

FIGURE 1. Equivalent circuits used to simulate (a) a negative and (b) a positive injected noise.

Fig. 1 shows equivalent circuits for simulation of negative and positive injected noise [62] resulting from the charge caused by the particle strike. To mimic the negative injected noise, a negative current as given by Equation (1) (1→0) is injected to the drain of the NMOS. Similarly, to mimic the positive injected noise, a positive current as given by Equation (1) (0→1) is injected to the drain of the PMOS. For MEU fault injection simulations, multiple current sources are applied to the cell nodes to model the effects of charge sharing [19].

To find the critical charge of a given node in an SRAM cell, we gradually increase Q_{dep} in Equation (1) in our simulation until the data value stored in the SRAM cell changes. The minimum critical charge among all sensitive nodes, as defined in Section III-C, gives Q_{crit} for the SRAM cell as a whole.

B. FDSOI STRUCTURE

Fully Depleted Silicon On Insulator, or FD-SOI, is a planar process technology that incorporates an ultra-thin layer of insulator (the buried oxide) within the substrate to dramatically reduce the leakage current. This also lowers the parasitic capacitance between the source and the drain, improving transistor electrostatic characteristics, which causes better mobility and less variability and enhances the performance of FD-SOI circuits. Furthermore, the transistor channel that is implemented by a very thin silicon film makes the transistor fully depleted without any channel doping requirement [48], [71]. These properties make FD-SOI an appealing technology for integrated circuits fabrication [56].

However, what makes FD-SOI an attractive technology to apply for space applications is its capability to operate in harsh radiation environments because of lower probability of SEU due to the extremely small sensitive volume [48], [56]. Meanwhile, the probability of MEU are lower in SOI SRAMs than Bulk SRAMs because of the reduced coupling between the devices and the memory cells [59], [60], which simplifies the design of dense memory structures [61]. SOI fabrication costs are, however, higher than for bulk CMOS [42], [43].

C. PREVIOUS RADIATION HARDENED MEMORY CELL DESIGNS

To provide fault tolerant protection, several conventional solutions such as error correction coding (ECC) [2], dual modular redundancy (DMR) [3] and triple modular redundancy (TMR) [4] are employed at the architectural level to mitigate SEU issues in memory blocks. However, these techniques cause considerable area overhead and power consumption as well as increasing the delay and adding the complexity of the system. Therefore, they are usually not suitable techniques for small memory blocks, especially when operating at low voltage levels [5].

In contrast, circuit-level techniques to enhance SEU immunity add to the size of individual memory cells but avoid the architectural overhead. This can make them more effective in reduction of area overhead and delay as well as power consumption. Here we review the most notable techniques with a focus on read and write power consumption, read and write delay, area, noise margins, SEU, MEU, and Q_{crit}. Note that when we below write that a memory cell is SEU immune, this is only for deposited charges below Q_{crit}. Above Q_{crit} the cell will change state. If, on the other hand, one or more nodes of a cell is not SEU immune, a state change to the node will always result in a change to the state of the whole cell.

1) PREVIOUS CELL DESIGNS THAT CANNOT PROVIDE SEU TOLERANCE

Authors in [13] propose a 10T hardened SRAM cell named Quatro. Compared to previous designs such as [8], it is more area efficient and more reliable in low voltage applications with larger noise margin and less leakage current [13]. Furthermore, it can completely recover from 1→0 SEU by using negative internal feedbacks. This technique increases the critical charge of the cell nodes. It does not provide full immunity to other SEUs, however, and some internal nodes are not sufficiently robust and may flip during 0→1 SEU [9], [10]. Moreover, it does not have MEU tolerance [14]. Furthermore, Quatro may suffer from weak read/write margins during technology scaling. To increase the write stability of Quatro as well as read margin, some recent techniques have been proposed [15] that splits the read/write paths and changes the internal topology of the cell structure. This does not mitigate the SEU or MEU challenges of Quatro.

In [16] two types of 10T RHBD memory cells, PMOS stacked (PS) and NMOS stacked (NS), are proposed using a stacked structure in their designs. However, they cannot provide full SEU immunity. PS can only recover from 1→0 SEU and not 0→1 SEU. NS is only able to resist 0→1 SEU and when the nodes are flipped from 1→0, the state of the cell is changed. Furthermore, neither NS nor PS are immune to multiple node upsets [9].

Authors in [21] improve the 13T memory design and propose a new hardened memory structure (RHD13) that enhances the shared critical charge to improve the reliability. However, it provides neither full immunity against MEUs nor sufficient robustness against SEUs. RHBD14T proposed in [74] can recover from MEUs but cannot recover from a 1→0 SEU induced at one of its nodes [76].

2) PREVIOUS CELL DESIGNS THAT PROVIDE SEU TOLERANCE BUT WITH LOW Q_{crit}

Using circuit-level hardening techniques, a new 10T Radiation-Hardened-By-Design (RHBD) memory cell is proposed with low area overhead compared to previous radiation hardened memory cells [10]. However, it is shown that the proposed 10T cell suffers from high read access time that may affect its application wherever high speed is indispensable [6], [10]. Furthermore, even if providing SEU tolerance regardless of the upset polarity, the tolerance capability (Q_{crit}) is lower than in previously proposed cells [6].

SRRD12T [77] and SRRD12T [78] are improved versions of [76] and exhibit higher WSNM. However, none of them have high Q_{crit}. An RHBD 10T SRAM cell proposed in [80] provides full SEU immunity and can recover from both $0\rightarrow1$ and $1\rightarrow0$ SEUs on any one of its nodes. Their proposed design is also acceptable with respect to area. However, the noise recovery time is very long while Q_{crit} is low, therefore the design is not suitable for cache cells.

3) PREVIOUS CELL DESIGNS THAT PROVIDE SEU TOLERANCE, BUT HAVE HIGH READ ACCESS TIME

The Dual interlocked storage cell DICE is a 12 transistor (12T) memory cell with a well-known hardening design approach widely used in latch, flip-flop and memory designs thanks to its full tolerant capability to SEU [8]. One of the advantages is that it is not necessary to increase the transistor sizes or capacitances of the nodes [8], [9]. The DICE cell consists of two interlocked latch pairs to store the complementary values so that an affected node can be recovered to its previous value using the positive feedback [10]. Using dual node feedback control provides full SEU fault immunity, however, cannot fully tolerate multiple node upsets because of negative effects of charge sharing induced by particle strikes [9], [11]. Furthermore, the area overhead, power consumption and delay are high compared to the conventional 6T SRAM cell [10], [12], [13]. Especially its high area overhead restricts the applicability where area efficiency is essential [9].

Authors in [17] propose a low-power radiation hardened 12T cell based on both circuit level and layout-level SEU mitigation techniques. The design is derived from the PS cell proposed in [16], and by adding two stacked NMOS transistors, the circuit can tolerate SEUs at any sensitive nodes regardless of upset polarity. Furthermore, it can tolerate MEUs induced by charge sharing on two fixed nodes, but not on all nodes in general. However, it suffers from large area overhead, relatively high read access time, and very low read static noise margin (RSNM). The same authors propose an alternative version of the mentioned cell [18], derived from the NS cell proposed in [16] by changing two NMOS access transistors to PMOS as well as adding two stacked PMOS transistors. It is robust against SEUs regardless of upset polarity and is MEU tolerant. However, it suffers from large area overhead as well as high read and write access times.

Two robust single-ended hardened SRAM cells, the 13T and 11T cells, are proposed in [19] and [20], respectively. Both designs deploy a similar technique to improve the reliability: using a refreshing mechanism and periodically cutting off the loop paths to block the particle strike effects. This is done by taking advantage of two extra transistors as switches added in the feedback paths. Moreover, the proposed circuit in [19] is enhanced further with two more transistors to improve robustness against multiple event upsets, though it provides only SEU immunity and not full MEU immunity. Moreover, the required peripheral circuitry has high area overhead and longer operation time due to extra transistors in the refreshing mechanism. Furthermore, the designs are not able to perform differential write and read operations due to the single-ended structures, which can increase the operation times and are uncommon for custom memory designs. They also consume more power than recent smaller designs.

Circuit techniques are combined with modification in layout-topology in a new 12T RHBD cell proposed in [38], providing high radiation robustness and high stability. However, its access time is too high, which limits its application where speed is a crucial parameter.

4) PREVIOUS CELL DESIGNS THAT PROVIDE SEU TOLERANCE, BUT HAVE HIGH AREA OVERHEAD

A 15T SRAM cell proposed in [79] provides SEUs tolerance. The cell can also recover from MEUs. However, these improvements are at the expense of longer read delay and higher area overhead that make the cell less suitable as cache memory cells. A memory cell proposed in [14], RHD12T, improves robustness against SEU by deploying circuit level hardening techniques together with layout-level approaches. However, this memory cell suffers from high area overhead and power consumption.

A low-voltage radiation-hardened 13T memory cell, LA13T, is proposed in [28] that employs a novel dual-driven separated- feedback mechanism to keep high robustness as well as functionality at low voltages. However, undesired paths from VDD to GND are formed during upset occurrences, which cause large energy consumption. A solution proposed in [29] can block the undesired paths and save energy consumption, but at the expense of area overhead to reach the same drive capability as the original LA13T cell. This area overhead is added to the cell already designed with 13 transistors, which further diminishes the design applicability for space applications.

Two 18T and 24T cells are proposed in [32] that provide complete tolerance against SEUs but at the cost of considerable area overhead. Similarly, the cells proposed in [33] and [34] have high area overhead making them less suitable for cache designs.

Two quadruple cross-coupled storage cells, the so-called QUCCE 10T and QUCCE 12T, are proposed in [6]. QUCCE 10T is a proper cell design for high-speed applications, while the QUCCE 12T cell is a promising candidate for low-voltage and high reliability. Their SEU tolerance are lower than

several previous designs such as [8], [13], and [15], though QUCCE 12T has high Q_{crit} at the expense of larger area. Therefore, the proposed cells may be less suitable for space applications that need high cell robustness and low area.

5) PREVIOUS CELL DESIGNS THAT PROVIDE SEU TOLERANCE, BUT HAVE HIGH RECOVERING TIME

A 12T radiation hardened memory cell is proposed in [35] that can tolerate MEUs in the near threshold voltage regime. Despite smaller read and write access times, and lesser area as compared to the some reported SEU hardened memory cells, the noise recovery time (the required time to recover the initial states after a charged particle strike) is too high making it not suitable for cache memory cell designs.

RSP14T [31], an improved version of RHD12T [14], cannot only tolerate SEUs, but also have MEU immunity better than that reported for RHD12T. Its write access time and power consumption are also significantly improved. However, high area overhead and high recovering time after the noise injection make it unsuitable for cache memory designs of space applications.

A 12T radiation hardened SRAM cell, called SRRD12T, is proposed in [75]. SRRD12T can recover from both SEUs and MEUs. The proposed cell has higher read and write stability and lower write access time compared to other tested cells but at the expense of longer read access time and higher area. In addition, the recovery time after noise injection is relatively high, which makes it an unsuitable option for cache designs. RHPD12T [37] can recover from both SEUs and MEU. However, the design has high noise recovery time with a larger area and power overhead. A 12T SRAM cell is presented in [81] with a novel crossbar-based peripheral circuit (CBPC) to reduce SEU effects and improve the cell immunity. However, the noise recovery time is too high. Therefore, the design is unsuitable for cache memory cell designs.

A 14T RHBD SRAM cell proposed in [82] provides full SEU immunity. The design can also provide MEU immunity. However, the recovering time is too high. The area overhead and the read delay are also too high making the cell unsuitable in cache designs for space applications. Authors in [83] propose a 14T high reliability radiation hardened memory cell (called RH-14T) that provides MEU tolerance, but with a larger area penalty and more power consumption. Meanwhile, the recovering time is too high, which makes the cell an unsuitable choice for cache memory designs.

The Gain Cell eDRAM (GC-eDRAM) [22] is an alternative design to SRAM that offers lower leakage current, smaller area overhead, and in spite of extra periodic refreshing cycles to retain data reliably, it is a promising design for low-voltage applications [23] as well as space applications [5]. The retention power is lower than the leakage power of a standard 6T SRAM cell [24], but the required periodic refresh cycles reduce both memory availability and access bandwidth [25]. Furthermore, during technology scaling, data refreshing must be done more frequently due to the reduced parasitic storage capacitance and increased leakage currents [26], [27]. RHMD10T [76] is another proposed cell which has both SEUs and MEU tolerance, but it has a high write failure probability.

III. MEMORY CELL DESIGN DETAILS

In this section, we review Nwise cell characteristics [55] and describe Pwise cell characteristics. Our area-efficient Nwise and Pwise cells consist of 10 transistors and are suitable for high-density designs for space applications. Here we describe the circuit structures as well as the operation analyses of both cells. We show that both cells can operate correctly like typical SRAM cells during reading and writing operations. Meanwhile, their feedback paths help the storage nodes recover to their initial value after particle strikes and provide enough robustness under high-radiation conditions. In addition, both Nwise and Pwise cells take advantage of the design with FD-SOI 28nm technology, and they can recover when adjacent cell nodes become involved during particle strike [61]. Both SEU and MEU recovery analyses of Nwise and Pwise cells are depicted in this section. Details on transistor sizes, energy, read and write times, and noise margins are reported and compared with state of the art in Section IV.

A. CELL SCHEMATICS

1) Nwise CELL SCHEMATIC

Fig. 2(a) shows the circuit structure of the Nwise cell [55]. A cross-coupled pair consisting of two NMOS transistors (N1 and N2) provides the main storage part of the cell while another cross-coupled pair of two NMOS transistors (N5 and N6) acts as the backup part. Therefore, the Nwise cell has four storage nodes Q, QB, P, and PB, where Q and QB keep the stored data correctly and P and PB provide the redundant stored data for Q and QB. The access transistors, N7 and N8, connect the bit-lines, BL and BLB, to the main storage nodes Q and QB, respectively. N7 and N8 are controlled by the word line (WL). Hence, when WL is in high mode, transistors N7 and N8 are turned on, and read/write operations can be done. Transistors P1-N4 and P2-N3 provide two feedback paths for the Nwise cell and help the storage nodes recover to their initial value after particle strikes and secure robustness under high-radiation conditions. A comparison between this structure and the RHBD cell presented in Section II-C can be found in Section III-A2.

2) Pwise CELL SCHEMATIC

Fig. 2(b) shows the circuit structure of our proposed Pwise cell. Two cross-coupled PMOS transistor pairs, P1-P2 and P5-P6, shape two latches where one creates data redundancy for the other. Therefore, the Pwise cell has four storage nodes U, UB, V, and VB, where V and VB provide the redundant stored data for U and UB. Furthermore, the access transistors, NMOS pass gates N3 and N4, which are controlled by the word line (WL), connect the bit-lines (BL and BLB) to the main storage nodes U and UB, respectively.

Like the Nwise cell, two feedback paths, N1-P4 and N2-P3 are provided for the Pwise cell to help storage nodes recover to their initial value after particle strikes, securing robustness under high-radiation conditions. The Nwise and Pwise cell feedback structures consist of both NMOS and PMOS transistors to increase the tolerance capability as confirmed through our simulations reported in Section IV.

The Nwise and Pwise cell structures have similarities with the circuit structure of RHBD proposed in [10] with some important differences: 1- RHBD consists of two cross-coupled transistor pairs, but unlike Nwise and Pwise, one is made of two NMOS transistors and the other of two PMOS transistors where the PMOS-transistor pair creates data redundancy for the NMOS-transistor pair. 2- Similar to Nwise and Pwise cells, RHBD is equipped with two feedback paths to enhance the tolerance capability, but the feedbacks consist of two PMOS transistors instead of one NMOS and one PMOS.

B. OPERATION ANALYSES

Fig. 3 shows the test bench circuit used in our work consisting of a one-column set containing 64 Nwise (Pwise) cells and associated peripheral circuitry including a precharge circuit, a write circuit, and an output sense amplifier [49], [50]. In this section, we demonstrate how a cell located in the column set operates, both through text and simulation results. We will come back to the simulation setup in Section IV.

1) Nwise MEMORY CELL DESIGN

Signal WL is low during hold mode, hence, transistors N7 and N8 are OFF. If the state of the memory cell is 1 then Q = 1, QB = 0, PB = 0, and P = 1 (see Fig. 2(a)), transistors N2, N4, N6, and P1 are ON, and the other transistors are OFF. Hence, the Nwise cell will keep the initial stored value.

Fig. 4 shows transient simulation results of an Nwise cell located in the test bench column set for a sequence of operations "Write 1, Read 1, Write 0, Read 0". It confirms that the write and read operations are completed successfully. To start the write data 0 operation, for instance, we set BL and BLB to 0 and VDD respectively. Afterwards, when WL is changed to VDD, Q is discharged to 0, and QB is charged to VDD. Thus, transistors N1, N3, N5, and P2 are turned on, and transistors N2, N4, N6, and P1 are turned off. Hence, the logical value of the Nwise cell is properly changed to state 0, and the write operation is completed correctly. Since the Nwise cell has a symmetrical structure, similar descriptions are assumed for writing data 1 into the Nwise cell (nodes and transistors are replaced by their symmetric pairs in the above explanation).

BL and BLB are precharged to VDD before starting the read operation. This is done by activating the precharge circuit. Thereafter, the two access transistors N7 and N8 are turned on when signal WL is set to VDD, hence, the read operation begins. The following explanation relates to a read data 1 operation, i.e., nodes have values Q = P = 1 and QB = PB = 0. Hence, the voltage of BL remains unchanged while

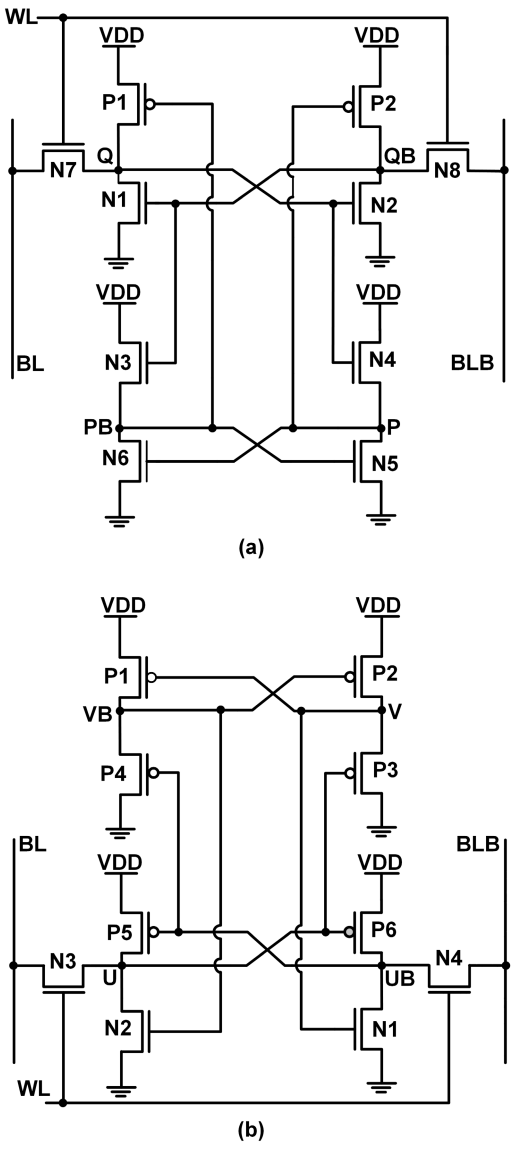

FIGURE 2. The circuit structure of (a) the Nwise cell [55] and (b) the new proposed Pwise cell.

BLB is discharged through transistor N2 since N2 is ON and creates a path from BLB to GND. Afterwards, the voltage difference between BL and BLB is detected and amplified by the connected differential sense amplifier (Fig. 3).

Initially the sense amplifier is OFF. When BL and BLB are being precharged high with the precharge circuit, the internal nodes of the sense amplifier are being precharged as well. The bitlines (BL and BLB) are also equalized (EQ is low) so that any mismatch between the precharges of BL and BLB is suppressed [73]. When WL is asserted for the read operation, EQ and PCB are lifted and precharging of the sense amplifier is stopped. Afterwards, when enough voltage difference is developed between two nodes of the sense amplifier, the sensing is done and the state of the stored data is output. Therefore, the read operation is completed properly [73].

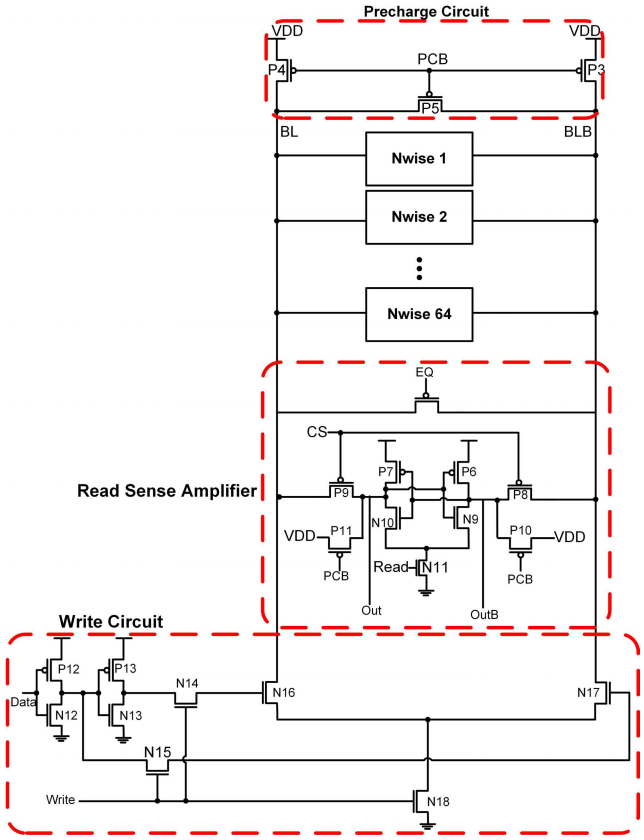

FIGURE 3. The test bench circuit that consists of a one-column set that containing 64 Nwise (Pwise) cells, a precharge circuit, a write circuit, and an output sense amplifier [55], [73].

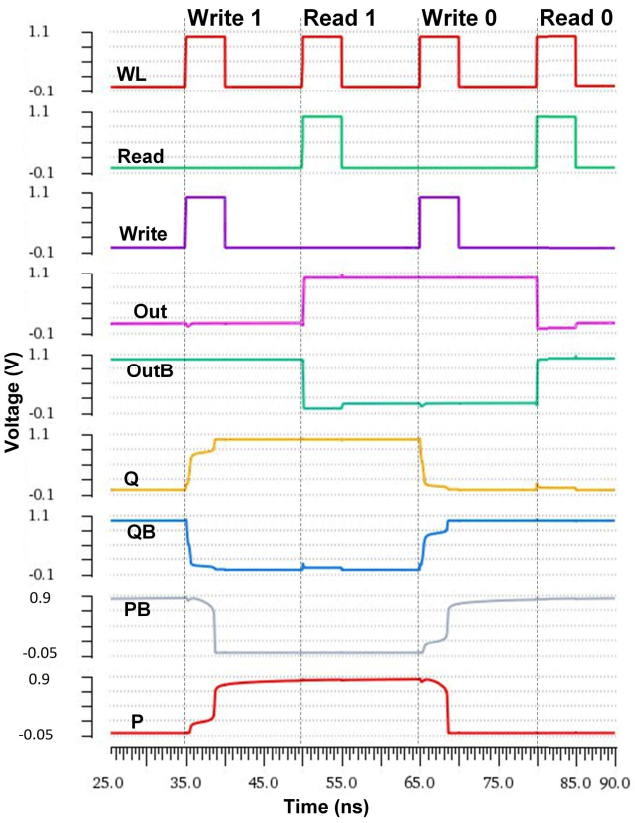

FIGURE 4. The simulation waveform of Nwise cell for a sequential set of operations Write 1, Read 1, Write 0, Read 0.

When signal WL is set to 0, the storage nodes (Q, QB, P, and PB) maintain their stored values. Since the Nwise cell has a symmetrical structure, similar explanations are given for read data 0 from the cell (nodes and transistors are replaced by their symmetric pairs in the above description).

2) Pwise MEMORY CELL DESIGN

In hold mode, signal WL is set to low and thus transistors N3 and N4 are OFF. If the state of the Pwise cell is 1 then U = 1, UB = 0, V = 1, and VB = 0 (see Fig. 2(b)), transistors P5, P4, P2, and N1 are ON, and the others are OFF. Hence, the Pwise cell will keep the initial stored value.

Fig. 5 shows transient simulation results of a Pwise cell located in the test bench column set for a sequence of operations "Write 1, Read 1, Write 0, Read 0". It confirms that the write and read operations are completed successfully. To start the write data 0 operation, we set BL and BLB to 0 and VDD respectively. Afterwards, U is discharged to 0, and UB is charged to VDD when WL is changed to VDD. Thus, transistors P1, P3, P6, and N2 are turned on, and transistors P2, P4, P5, and N1 are turned off. Hence, the logical value of the Pwise cell is properly changed to state 0, and the write operation is completed correctly. Since the Pwise cell has a symmetrical structure, similar descriptions are assumed for writing data 1 into the Pwise cell (nodes and transistors are replaced by their symmetric pairs in the above explanation).

BL and BLB are precharged to VDD before starting the read operation. This is done by activating the precharge circuit. Thereafter, the two access transistors N3 and N4 are turned on when signal WL is set to VDD, hence, the read operation begins. The following explanation relates to a read data 1 operation, i.e., nodes have values U = V = 1 and UB = VB = 0. Hence, the voltage of BL remains unchanged while BLB is discharged through transistor N1 since N1 is ON and creates a path from BLB to GND. Afterwards, the voltage difference between BL and BLB is recognized and amplified by the connected differential sense amplifier, and thus, the state of the stored data is output. Therefore, the read operation is completed properly. When signal WL is set to 0, the storage nodes (U, UB, V, and VB) maintain their stored values. Since the Pwise cell has a symmetrical structure, similar explanations are given for read data 0 from the cell (nodes and transistors are replaced by their symmetric pairs in the above description).

C. Nwise AND Pwise CELLS SEU RECOVERY ANALYSES

In this section, we review the SEU robustness of the Nwise cell and analyze the SEU robustness of the Pwise cell, both through text and simulation as depicted in Fig. 6 and Fig. 7. The simulation setup will be considered in Section IV.

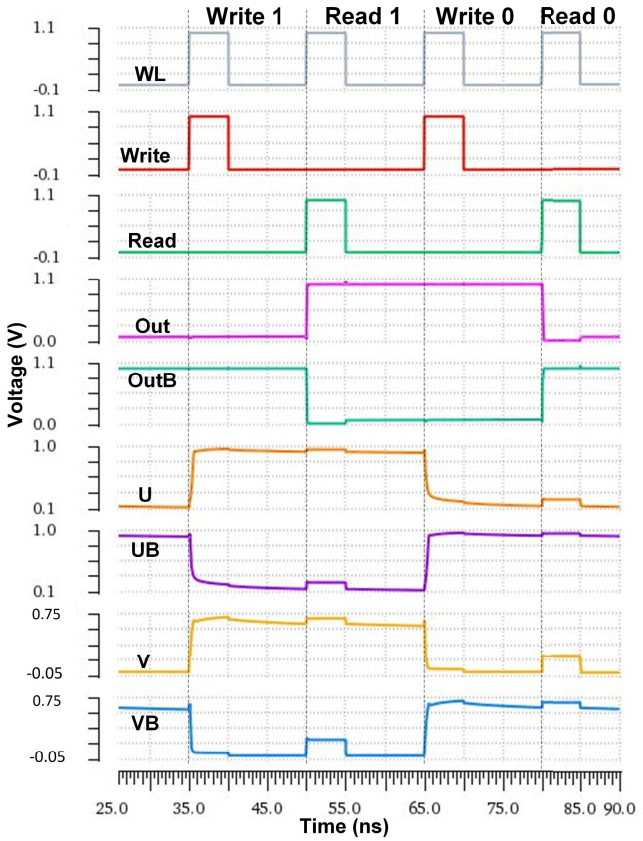

FIGURE 5. The simulation waveform of Pwise cell for a sequential set of operations Write 1, Read 1, Write 0, Read 0.

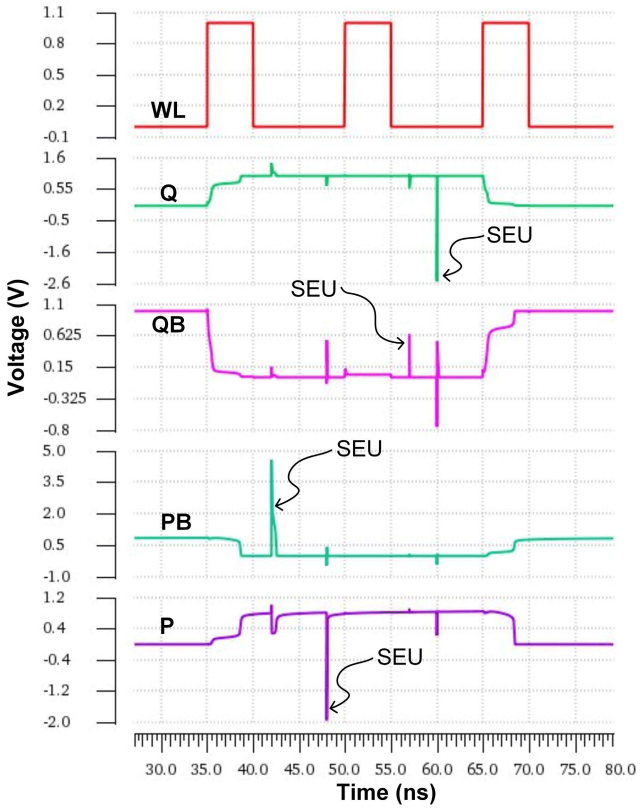

FIGURE 6. SEU tolerance simulation of Nwise cell.

When an energetic particle passes through a semiconductor device, electron-hole pairs are created along its path as it loses energy [5], [18], [28]. If such an energetic particle hits a reverse-biased junction depletion region, the injected charge is transported by drift current and leads to an accumulation of extra charge at the node [18]. This causes a transient current pulse that changes the value of the node when the injected charge exceeds the critical charge collected in the node [18], [28]. Therefore, sensitive nodes of the cell are the nodes surrounded by the reverse-biased drain junction of transistor(s) biased in the OFF state [51]. Hence, when a radiation particle strikes a PMOS transistor, only a positive transient pulse ((0→1 or 1→1)) can be generated, while, when a radiation particle strikes an NMOS transistor, only a negative transient pulse (1→0 or 0→0) can be induced [51].

We assume that the Nwise cell is in state 1 (i.e., Q = 1, QB = 0, PB = 0, and P = 1), hence, transistors N2, N4, N6, and P1 are ON, and the others are OFF. With this state of the cell, Q, QB, and P are sensitive nodes while PB is not sensitive to the particle strike. For Pwise, we assume that the cell is in state 1 (i.e., U = 1, UB = 0, V = 1, and VB = 0) with transistors P2, P4, P5, and N1 ON, and the others OFF. With this state of the Pwise cell, U, UB, and VB are sensitive nodes while V is not sensitive to the particle strike.

In the following simulations we inject charges at cell nodes using the model outlined in Section II-A. A charge just below the critical charge of the given node is injected in order to show how this affects the node voltage and how the SRAM cell recovers its original state. Note that if a charge equal to or greater than the critical charge is injected, the SRAM cell would not be able to recover. We mark the positions where charge is injected with SEU in the following figures, even though they here do not in the end change the SRAM cell data value. This is in accordance with the notation used in earlier work, e.g., [21].

1) Nwise CELL SEU RECOVERY ANALYSIS

i) If a 1→0 SEU affects node Q while storing a state 1, N2 and N4 will become temporarily OFF, therefore, P and QB will be floated. Thus, their initial state 1 and 0 will be kept because the high impedance state does not have effect on the state of the node [6]. Hence, N1 stays OFF. Meanwhile, the state of node PB remains unchanged (0). Controlled by PB, transistor P1 stays ON and finally recovers the state of node Q through the pull-up path.

ii) If a 0→1 SEU affects node QB while storing a state 0, the node starts to change from state 0 towards state 1, followed by N1 and N3 starting to change from OFF to ON. While N1 and N3 are not yet turned on, P which is still at the level of 1, keeps P2 OFF. Consequently, there is not any ON path connected to VDD to keep the high state of QB. Q has not

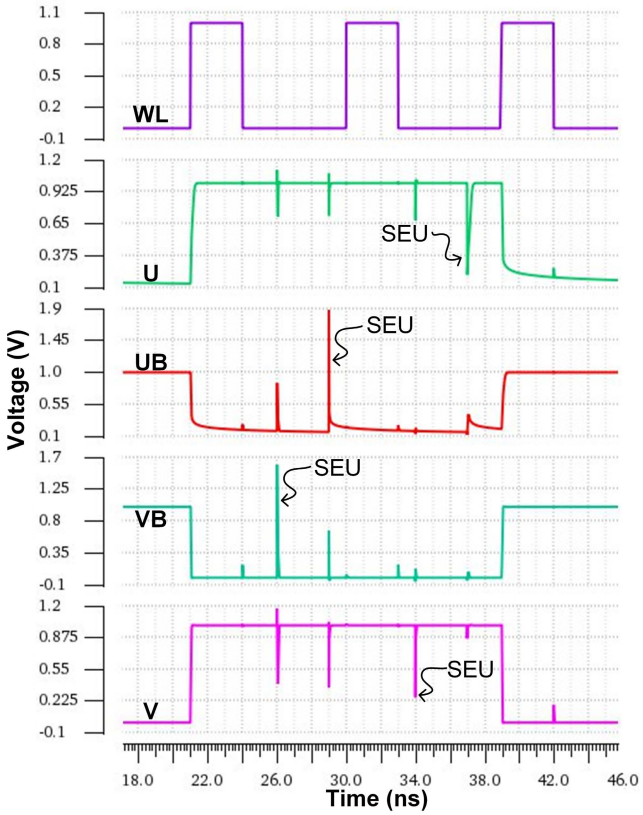

FIGURE 7. SEU tolerance simulation of Pwise cell.

changed yet so N2 is still ON, and hence node QB discharges through the ON path of N2 to its initial state. The recovery time is very short so as not to allow a high QB voltage level.

iii) If a 1→0 SEU affects node P while storing a state 1, transistors N6 and P2 will become OFF and ON, respectively. Consequently, node PB will become floated, and its state will not be changed. Therefore, transistor P1 stays ON; thus, node Q stays unchanged and keeps transistor N4and N2 ON pulling node P up to its initial state through ON transistor N4.

Since the Nwise cell has a symmetrical structure, similar recovery behavior is seen for state 0 of the cell (nodes and transistors are replaced by their symmetric pairs in the above descriptions). This shows that the Nwise cell can recover the flipped storage nodes irrespectively of the upset polarity.

In the simulations depicted in Fig. 6, SEU fault injections happen at 42ns, 48ns, 57ns, and 60ns, respectively. At 42ns, a 0→1 transient fault occurs at node PB. We see from the simulations that node PB recovers to its initial state, and followed by PB, other nodes return to their initial state. At 48ns, a 1→0 transient fault occurs at node P. Again, the internal nodes of the Nwise cell recover their initial state after the injected fault. At 57ns, a transient 0→1 fault hits node QB. Again, QB comes back to its initial state, followed by the other internal nodes. Finally, at 60ns, a 1→0 transient fault occurs at node Q that is recovered to its initial state, and followed by this node, other nodes of the Nwise cell recover their initial state after the injected fault.

2) Pwise CELL SEU RECOVERY ANALYSIS

i) If a 0→1 SEU affects node UB while storing a state 0, transistors P4 and P5 become temporarily OFF, hence, U and VB will become floated. Therefore, their 1 and 0 state will be kept since the high impedance state does not have effect on the state of the node [6]. Hence, transistor P2 remains ON and the state of node V remains unchanged (1). Controlled by V, transistor N1 remains ON and eventually discharges the state of node UB through the pull-down path.

ii) If a 0→1 SEU affects node VB while storing a state 0, transistor P2 becomes OFF, hence V keeps its state (1) and transistor P1 remains OFF. Hence there is no ON path connected to VDD to keep the high state of VB. On the other hand, transistor P4 is already ON hence node VB discharges through the ON path of P4 to its initial state.

iii) If a 1→0 SEU affects node U while storing a state 1, transistors P3 and P6 start to change from OFF to ON. As long as P3 and P6 are not yet turned on, node VB which is still at the level of 0, keeps P2 ON and N2 OFF. Consequently, there is not any ON path connected to GND to keep the flipped low state of U. On the other hand, node UB has not changed yet so P5 is still ON. Hence, node U is pulled up through the ON path of P5 to its initial state. Since the Pwise cell has a symmetrical structure, similar recovery behavior is seen for state 0 of the cell (nodes and transistors are replaced by their symmetric pairs in the above description). This shows that the Pwise cell can recover the flipped storage nodes irrespectively of the upset polarity.

As depicted in Fig. 7, SEU fault injections happen at 26ns, 29ns, 34ns, and 37ns, respectively. At 26ns, a 0→1 transient fault occurs at node VB. We see from the simulations that node VB recovers to its initial state, and followed by VB, other nodes return to their initial state. At 29ns, a 0→1 transient fault occurs at node UB. Again, the internal nodes of the Pwise cell recover their initial state after the injected fault. At 34ns, a transient 1→0 fault hits node V. As we can see, V comes back to its initial state, followed by the other internal nodes. Finally, at 37ns, a 1→0 transient fault occurs at node U that is recovered to its initial state. Followed by this node, other nodes of the Pwise cell recover their initial state after the injected fault.

D. MEU RECOVERY ANALYSES OF Nwise AND Pwise CELLS

Fig. 8 shows MEU tolerance simulation for nodes P, Q, and QB of the Nwise cell when two of them are affected by a charged particle strike at the same time. Since PB is not a sensitive node, the cases for the PB-P, PB-QB or PB-Q pairs of nodes are the same as those of single nodes P, QB or Q, respectively which were covered in the Section III-C1. Again, we inject the maximum charges possible on each node that still allows the SRAM cell to recover its original data value. As for SEU, we mark the injection positions in the figures

with MEU, even if the cell in the end does not change data value.

As shown in Fig. 8, MEU fault injections happen at 46ns, 53ns, and 55ns, respectively. At 46ns, both Q and P are affected by particle strikes (Q: 1→0, P: 1→0). We observe that nodes Q and P recover to their initial state, and followed by them, other nodes return to their initial state. At 53ns, both QB and P are affected by particle strikes (QB: 0→1, P: 1→0). Again, the internal nodes of the Nwise cell recover their initial state after the injected fault. Finally, at 55ns, both Q and QB are affected by particle strikes (Q: 1→0, QB: 0→1). As we can see, nodes QB and Q come back to their initial state, and followed by them, other internal nodes recover their initial state after the injected faults. Similar reasoning as in Section III-C1 can be used to motivate why we get these simulation results.

Note that the occurrence of multiple-node upsets with more than two nodes is unlikely to make a state change due to the extensive charge diffusion occurring in the storage element and wider spread of the incident strike [18], [19], [64].

According to Fig. 8, we observe that MEUs are much less prevalent in SOI technologies than in bulk technologies which has already been confirmed with several tests on SOI SRAMs and Bulk SRAMs [61]. This happens because the buried insulating layer below the thin active layer limits the volume for generation and collection of ion induced charge [59], which reduces coupling between the devices, hence, leads to less charge sharing in adjacent nodes than bulk silicon technologies that induces MEUs [61].

Fig. 9 shows MEU tolerance simulation of the Pwise cell. In this case V is not a sensitive node, and the V-U, V-UB or V-VB pairs of nodes are reduced to SEU on U, UB and VB, respectively. As shown in Fig. 9, MEU fault injections happen at 26ns, 34ns, and 37ns, respectively. At 26ns, both UB and VB are affected by particle strikes (UB: 0→1, VB: 0→1). We observe that nodes UB and VB recover to their initial state, and followed by them, other nodes return to their initial state. At 34ns, both UB and U are affected by particle strikes (U: 1→0, UB: 0→1). Again, the internal nodes of the Nwise cell recover their initial state after the injected fault. Finally, at 37ns, both U and VB are affected by particle strikes (U: 1→0, VB: 0→1). As we can see, nodes U and VB come back to their initial state, and followed by them, other internal nodes recover their initial state after the injected faults.

Like the Nwise cell case, the occurrence of multiple-node upsets with more than two nodes is unlikely to make a state change due to the extensive charge diffusion occurring in the storage element and wider spread of the incident strike [18], [19], [64].

Similar to the simulations depicted in Fig. 8, MEU tolerance simulations shown in Fig. 9 confirm that MEUs are much less prevalent in SOI technologies than in bulk technologies because the thin buried insulating layer below the thin active layer limits the volume for generation and collection of ion induced charge [59].

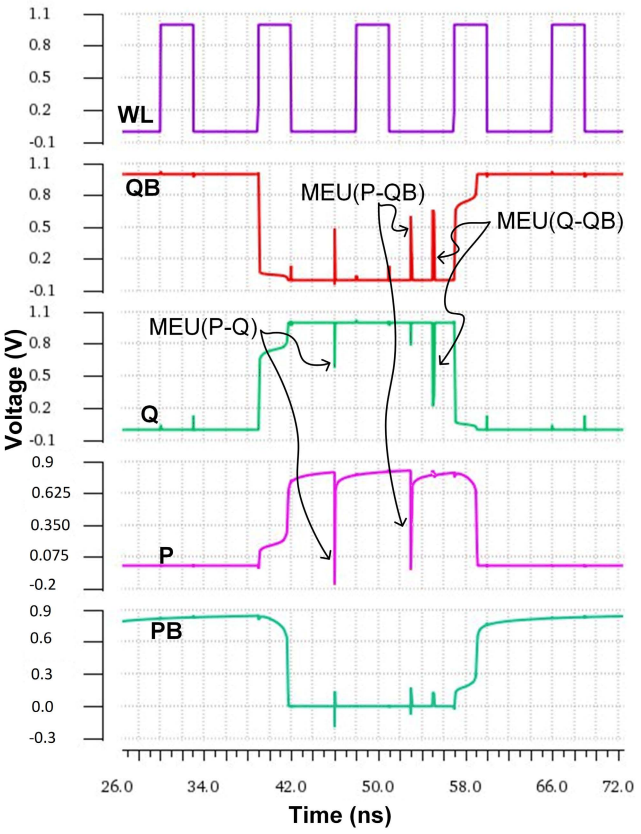

FIGURE 8. MEU tolerance simulation of Nwise cell.

IV. DESIGN METHODOLOGY AND SIMULATION RESULTS

To show the effectiveness of our designs, we compare the Nwise and Pwise cells with a selection of the previously published radiation hardened cells reviewed in Section II. The considered cells are as follows: a standard SRAM_6T cell (Fig. 10), the Quatro cell being an area-efficient well-known radiation hardened cell [13] (Fig. 11), the RHBD cell as a recently proposed area-efficient radiation hardened cell [10] (Fig. 12), the NS and PS cells being two stacked radiation hardened cells [16] (Fig. 13 and Fig. 14), and finally QUCCE, which is also a recently proposed 10T area-efficient radiation hardened cell designed for high-speed applications [6] (Fig. 15).

As explained in Section III, a one-column set consisting of 64 SRAM cells and associated peripheral circuitry is selected as the test bench. For Nwise and Pwise cells as well as other tested SRAM cells, this column-set is designed and simulated as explained below. The column is, e.g., assumed used in a cache memory as proposed and described in [49] and [50]. Necessary signal drivers and wire capacitances are added to the bitlines (BL and BLB) and wordlines (WL) based on parameters extracted from SRAM layouts. Transistor sizes of SRAM cells are optimized to get the maximum robustness, minimum read/write power consumption, minimum read/write access times, and minimum area. However, robustness has been given higher priority when the

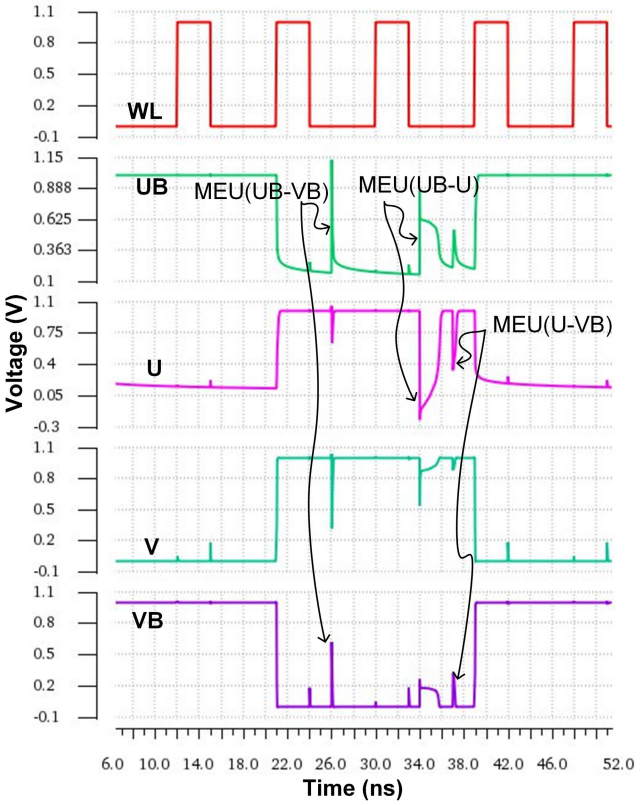

FIGURE 9. MEU tolerance simulation of Pwise cell.

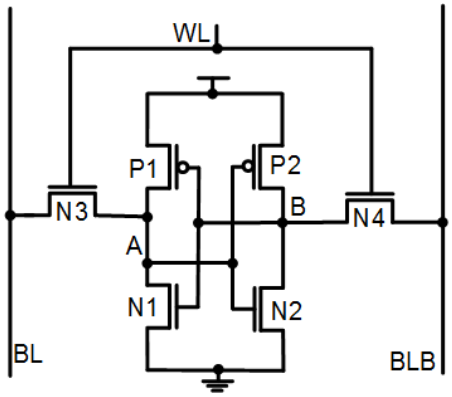

FIGURE 10. The circuit structure of the SRAM_6T cell.

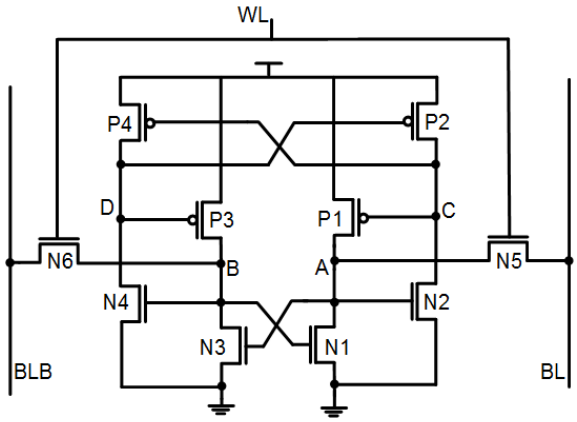

FIGURE 11. The circuit structure of the Quatro cell [13].

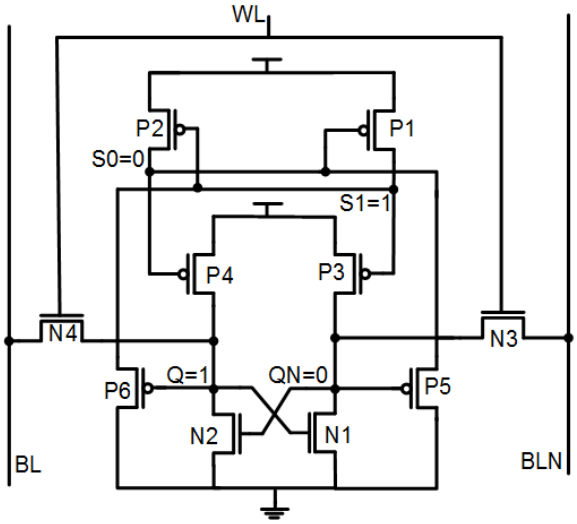

FIGURE 12. The circuit structure of the RHBD cell [10].

optimization goals have been conflicting. We use standard manual optimization, tuning transistor sizes to find a global optimized solution.

The layouts of all selected cells mentioned above are drawn with Cadence Virtuoso using a commercial 28nm FD-SOI technology. As example views, Fig. 16 and Fig. 17 shows the layout of the Nwise and Pwise cells, respectively. All the memory cells are implemented with regular threshold voltage (RVT) transistors [65], [66] in order to minimize leakage current. The RVT transistors are implemented in the layout with conventional well, i.e., N-channel devices reside in P-well and P-channel devices in N-well. FD-SOI provides a wide range of back-gate biasing voltage levels in order to regulate the threshold voltages of the transistors. We do not apply this technique in this paper, however, and leave it for our future work. Therefore, a VDD voltage is applied to the back-gate connection of PMOS transistors (NWELL) while a GND voltage level is connected to the back-gate connection of NMOS transistors (PWELL) of all memory cells. The layouts were all analyzed with a QRC parasitic extraction tool, and the netlists with added parasitic extracted parameters were simulated at nominal voltage level and temperature (1V and 27°C).

From the Cadence Virtuoso simulations, we find read and write power consumptions, read and write delay times, three different static noise margins (Hold, Write and Read SNMs, i.e., HSNM, WSNM, and RSNM), minimum critical Q, and area. SNMs express the voltage immunity of the memories during read, write, and hold operations, and they are calculated based on information found in [52].

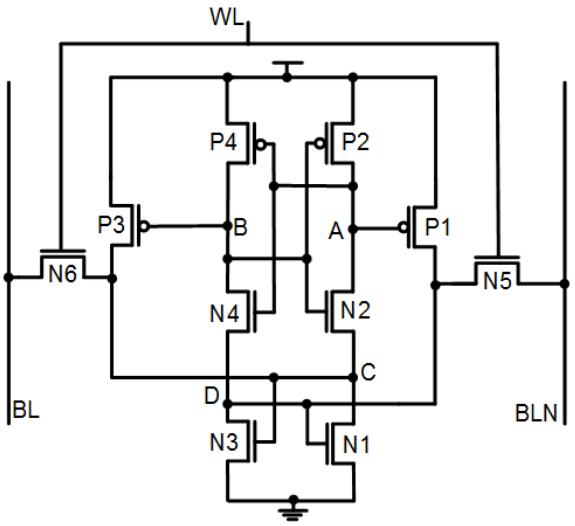

FIGURE 13. The circuit structure of the NS cell [16].

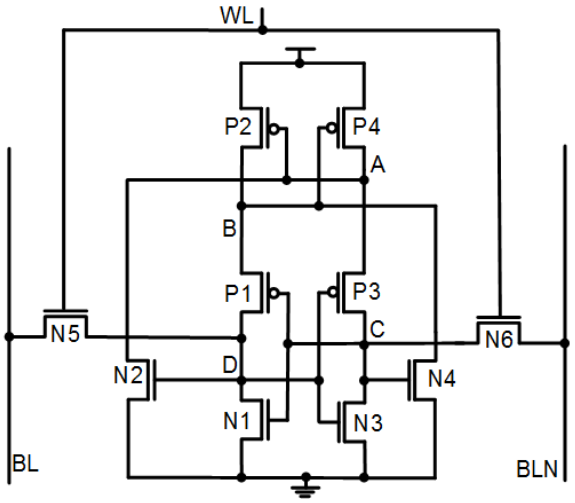

FIGURE 14. The circuit structure of the PS cell [16].

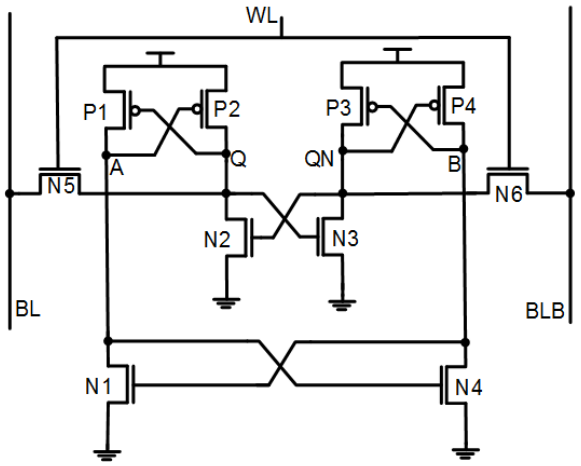

FIGURE 15. The circuit structure of the QUCCE cell [6].

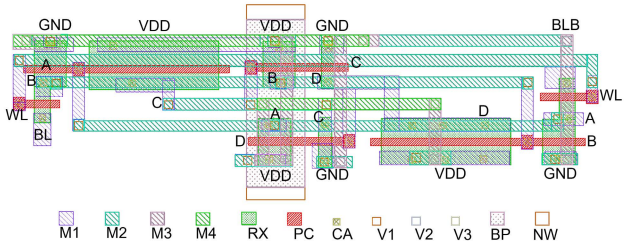

FIGURE 16. Layout view of Nwise cell design.

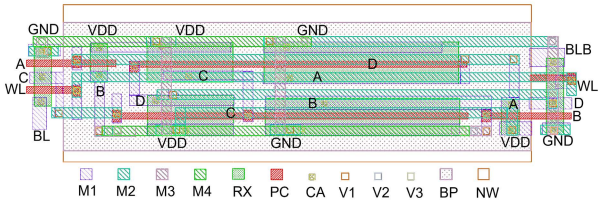

FIGURE 17. Layout view of Pwise cell design.

A. COMPARATIVE COST ANALYSES

Fig. 18 through Fig. 25 present the full performance comparison of the Nwise and Pwise cells together with the other simulated radiation hardened cells. The comparisons include power consumption during read and write operations, read access time, write access time, different static noise margins (HSNM, WSNM, and RSNM), and the total area of our considered cells. Similar trends to our reported cost values for individual cells have been reported for the Quatro, NS, PS, QUCCE, and RHBD cells in previous articles such as [6], [16], [18], and [10].

1) COMPARISON OF POWER CONSUMPTION

Fig. 18 reports write power comparisons between all considered cells. Nwise and Pwise cells have the highest write power consumption while Quatro has the lowest write power consumption. Again, Quatro cannot provide full fault immunity, however.

In Fig. 19 the read power of all tested cells is compared. Quatro, RHBD, and Nwise cells have the lowest level of read power consumptions while PS, NS, and Pwise cells present the highest level of read power consumption, respectively. The read power of the Nwise cell is 1.1× and 0.5× of the Quatro and PS cells, respectively (those have the lowest and the highest level of read power consumption), while the read power of the Pwise cell is 1.9× and 0.9× of Quatro and PS cells, respectively. Both are in the same range as the other tested cells but the Nwise cell is particularly useful in application with higher rate of read operations since it has lower read power consumption than the Pwise cell and most other cells.

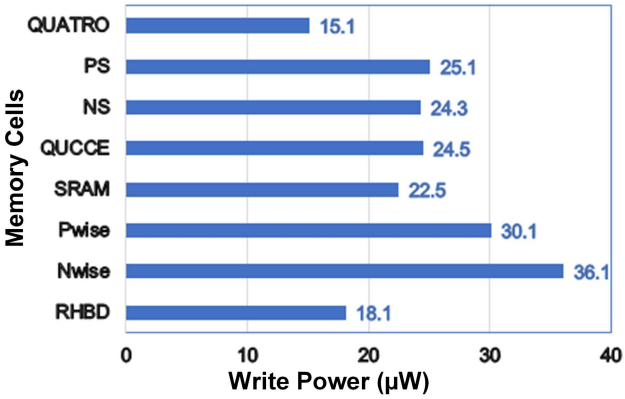

FIGURE 18. Write power comparisons between all considered cells.

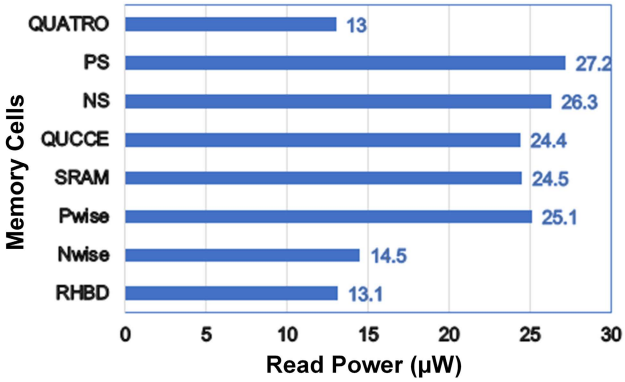

FIGURE 19. Read power comparisons between all considered cells.

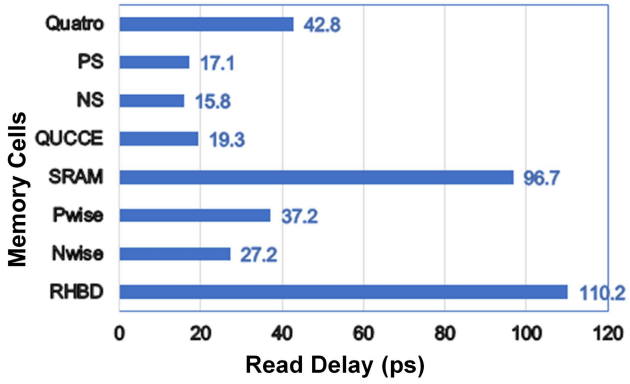

FIGURE 20. Read delay comparisons between all considered cells.

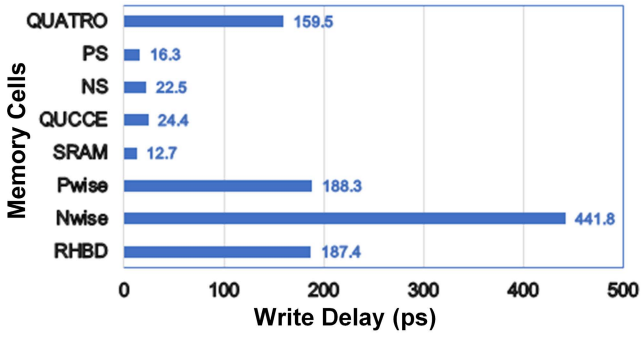

FIGURE 21. Write delay comparisons between all considered cells.

2) COMPARISON OF ACCESS TIMES

In Fig. 20 the read delays of all considered cells are compared. According to our simulations, the RHBD cell has the highest read delay, 4.0× and 2.9× of the Nwise and Pwise cells, respectively. This happens since more PMOS transistors are ON during a read in RHBD. The NS, PS and QUCCE cells have lower read delay than the Nwise and Pwise cells. However, because of their low Q_{crit}, they are less suitable for space applications.

In Fig. 21 the write delay of all considered cells are compared. It is observed that the Nwise cell has the highest write delay of the tested cells. This is because the N3 and N4 transistors, that have been added to the feedback paths to enhance the robustness of the cell, increase the driving loads in Q and QB, thus making the write operation slower. The SRAM, QUCCE, PS, and NS cells present the lowest write delays, but their low Q_{crit} again make them unsuitable for space applications. The write delay of the Pwise cell is close to that of the RHBD and Quatro cells (1.18× and 1.0× of Quatro and RHBD cells, respectively). The RHBD cell has low Q_{crit}, however, while the Quatro cell cannot provide full SEU immunity, hence neither of these are proper choices for space applications.

3) COMPARISON OF STATIC NOISE MARGINS

Fig. 22 shows write static noise margins of all considered cells. According to our simulations, RHBD and QUCCE have the lowest and the highest levels of WSNM, respectively. The Nwise cell has the third highest WSNM among all the simulated cells. The WSNM of Nwise and Pwise cells are 0.8× and 0.3× of QUCCE cell, respectively.

In Fig. 23 read static noise margin of all considered cells are compared. Pwise, Nwise and PS have the highest, second highest, and lowest levels of RSNM, respectively. The RSNM of the Pwise and Nwise cells are 1.2× and 1.0× of the Quatro cell, which has the third highest level of RSNM.

Fig. 24 shows the hold static noise margin results of all considered cells. The Pwise, RHBD, and Nwise cells have the three highest levels of HSNM, respectively. The HSNM of the Pwise cell is 1.10× and 1.12× of RHBD and Nwise while the HSNM of the Nwise cell is 0.88× and 0.97× of the Pwise and RHBD cells.

4) AREA

Fig. 25 compares the area of all considered cells. Pwise and Nwise are the largest of the simulated cells, though only 1.01× and 1.00× of RHBD.

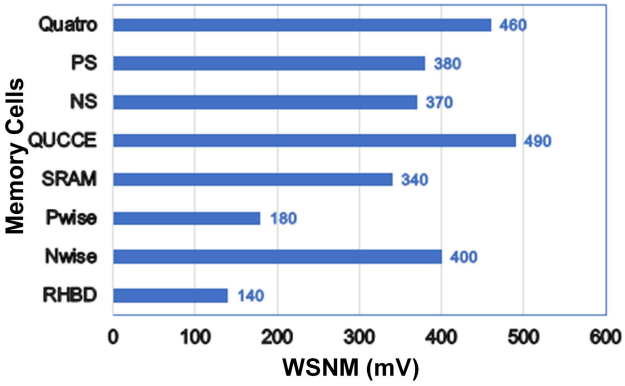

FIGURE 22. WSNM comparisons between all considered cells.

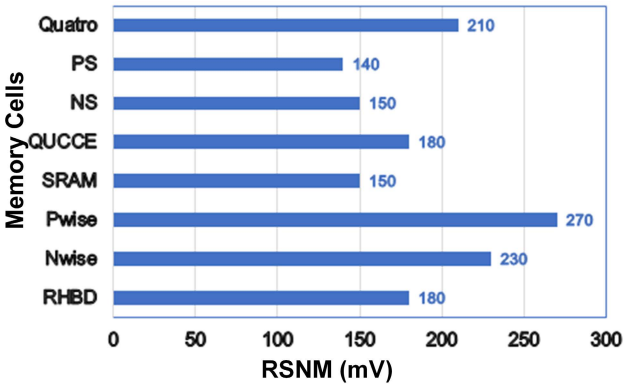

FIGURE 23. RSNM comparisons between all considered cells.

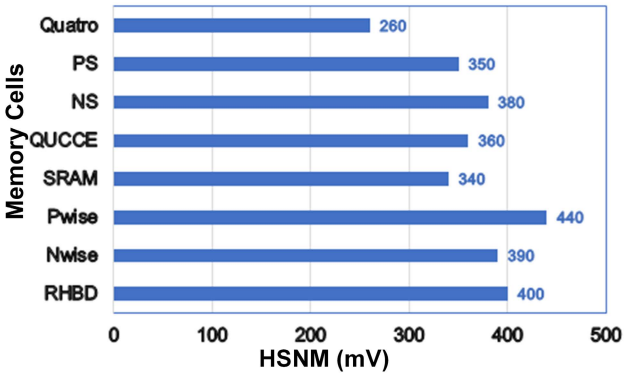

FIGURE 24. HSNM comparisons between all considered cells.

5) VERIFICATION AND COMPARISON OF ROBUSTNESS

Fig. 26 shows Q_{crit} for all considered cells. The Pwise and Nwise cells have higher critical charge than the PS, NS, QUCCE, SRAM and RHBD cells, making our proposed cells a better choice for space application designs since they can withstand a larger injected charge. The Pwise and Nwise cells have 1.69× and 1.67× times the Q_{crit} compared with the best among the PS, NS, QUCCE, SRAM_6T and RHBD cells, i.e., NS. Q_{crit} of the Quatro cell is almost as high as those of

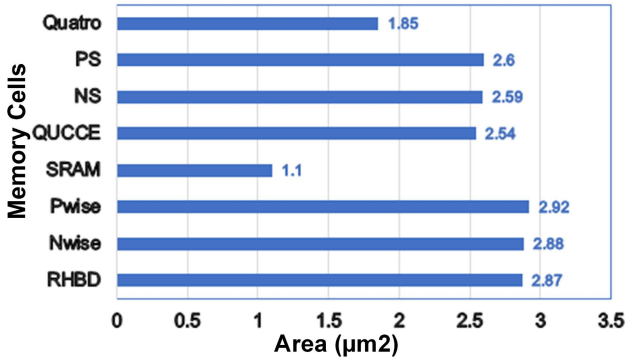

FIGURE 25. Area comparisons between all considered cells.

the Nwise and Pwise cells (0.97 versus 0.99 and 1, respectively), but, as it is described in Section II, Quatro cannot provide full tolerance against SEUs. It is therefore not a suitable choice for harsh environments.

The most important feature of the Nwise and Pwise cells are their high Q_{crit} which is due to the higher capacitance of their critical nodes. We explain this in more detail in comparison with the RHDB cell: 1- Similar to Section III-B1, we assume Nwise to be in state 1 (i.e., Q = 1, QB = 0, PB = 0, and P = 1), hence, transistors N2, N4, N6, and P1 are ON, and the others are OFF. Node QB is the critical node of Nwise. The capacitor of QB consists of drain capacitors of two OFF and one ON transistors (N8, P2, and N2 respectively), and gate capacitors of two OFF transistors (N1 and N3). 2- Similar to Section III-B2, we assume Pwise is in state 1 (e.g. U = 1, UB = 0, V = 1, and VB = 0), hence, transistors P2, P4, P5, and N1 are ON, and the others are OFF. Node U is the critical node of Pwise. The capacitor of U consists of drain capacitors of two OFF and one ON transistors (N2, N3, and P5 respectively), and gate capacitors of two OFF transistors (P6 and P3). 3- As explained in [10], we assume RHBD to be in state 1 (e.g. Q = 1, QN = 0, S0 = 0, and S1 = 1), hence, transistors N1, P1 and P4 are ON and the others are OFF (See Fig. 1 in [10]). Node S0 is the critical node of RHBD. The capacitor of S0 consists of drain capacitors of one OFF and one ON transistor (P2 and P5), and gate capacitors of two ON transistors (P4 and P1).

Transistor capacitances are combinations of extrinsic, intrinsic, and overlap parts, mostly dependent on the bias and geometry of transistors [44], [46]. Based on results from the optimization process described in the introduction of Section IV, we have used the transistor sizes shown in Table 1 for the tested cells. See figures with circuit diagrams in the publications related to each cell for explanations of transistor names.

According to the above description and transistor dimensions, the critical node capacitances of the Nwise and Pwise cells are higher than the other tested cells. Hence, the Nwise and Pwise cells have higher Q_{crit} since Q_{crit} is related to that

TABLE 1. Transistor sizes of all tested cells.

Cell Type	Transistor Sizes
Nwise	$W_{P1} = W_{P2} = 200nm, W_{N1} = W_{N2} = 200nm, W_{N3} = W_{N4} = 170nm, W_{N5} = W_{N6} = 80nm, W_{N7} = W_{N8} = 110nm.$
Pwise	$W_{P1} = W_{P2} = 80nm, W_{P3} = W_{P4} = 400nm, W_{P5} = W_{P6} = 300nm, W_{N1} = W_{N2} = 80nm, W_{N3} = W_{N4} = 100nm.$
RHBD [10]	$W_{P1} = W_{P2} = 80nm, W_{P3} = W_{P4} = 200nm, W_{P5} = W_{P6} = 343nm, W_{N1} = W_{N2} = 175nm, W_{N3} = W_{N4} = 100nm.$
Quatro [13]	$W_{P2} = W_{P4} = 120nm, W_{P1} = W_{P3} = 100nm, W_{N2} = W_{N4} = 150nm, W_{N1} = W_{N3} = 200nm, W_{N5} = W_{N6} = 80nm.$
SRAM_6T	$W_{P1} = W_{P2} = 100nm, W_{N1} = W_{N2} = 200nm, W_{N3} = W_{N4} = 100nm.$
NS [16]	$W_{P4} = W_{P2} = 100nm, W_{N4} = W_{N2} = 200nm, W_{N1} = W_{N3} = 150nm, W_{N5} = W_{N6} = 100nm, W_{P3} = W_{P1} = 150nm.$
PS [16]	$W_{P1} = W_{P3} = 100nm, W_{N1} = W_{N3} = 200nm, W_{N2} = W_{N4} = 150nm, W_{N5} = W_{N6} = 100nm, W_{P2} = W_{P4} = 150nm.$
QUCCE [6]	$W_{P1} = W_{P4} = 220nm, W_{P2} = W_{P3} = 80nm, W_{N2} = W_{N3} = 144nm, W_{N1} = W_{N4} = 100nm, W_{N5} = W_{N6} = 80nm.$

TABLE 2. Cost comparisons for all tested cells.

Cell Name	Write Power (uW)	Read Power (uW)	Write Access Time (ps)	Read Access Time (ps)	WSNM (mV)	RSNM (mV)	HSNM (mV)	Area (um2)	Qcrit (fF)
Nwise	36.1	14.5	27.2	441.8	400	230	390	2.88	0.99
Pwise	30.1	25.1	37.2	188.3	180	270	440	2.92	1
RHBD	18.1	13.1	110.2	187.4	140	180	400	2.87	0.31
Quatro	15.1	13	42.8	159.5	460	210	260	1.85	0.97
SRAM	22.5	24.5	96.7	12.7	340	150	340	1.1	0.38
NS	24.3	26.3	15.8	22.5	370	150	380	2.59	0.59
PS	25.1	27.2	17.1	16.3	380	140	350	2.6	0.57
QUCCE	24.5	24.4	19.3	24.4	490	180	360	2.54	0.41

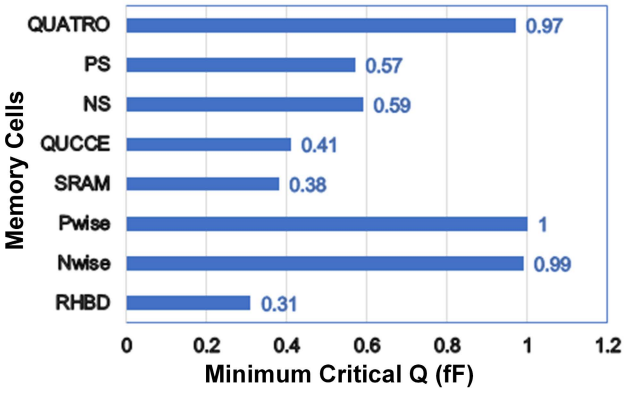

FIGURE 26. Minimum critical charge all considered cells.

node capacitance [44]–[46]. The structure of the circuits is also important since the capacitance of critical nodes become larger with added feedback transistors. Only Quatro has comparable Q_{crit} with Nwise and Pwise. However, Quatro does not support full SEU immunity.

In this paper, all the compared cells are designed and simulated with 28nm FD-SOI. Nwise and Pwise characteristics are, however, not dependent on the used technology and they can be achieved with Bulk technology as well.

Fig. 27 compares minimum critical charge between all considered cells for the temperature range of -55 to $+125°$, i.e., the temperature range normally used for space applications [67]–[69]. It is observed that at the minimum temperature, the Nwise, Quatro and Pwise cells have the highest Q_{crit} while at the maximum temperature, Pwise, Nwise and Quatro have the highest Q_{crit}. The differences between maximum and minimum Q_{crit} with respect to temperature variation are $0.62fF$, $0.15fF$ and $0.16fF$ for the Pwise, Nwise and Quatro cells, respectively. However, Quatro cannot provide full tolerance against SEUs, and are therefore not a suitable choice for harsh environments. Hence, the Nwise and Pwise cells have the highest Q_{crit} in the whole space temperature range compared with the other space relevant cells.

In order to investigate the tolerance capability of the considered cells to MEU, two independent current sources are injected to all possible susceptive node-pairs of each cell. We already have found the critical node for each cell (the node with the lowest critical charge as reported in Fig. 26), which we call the primary node. The combination of the primary node with all other nodes are then examined to identify the most vulnerable node-pair of each cell. The other node is called the secondary node, and the most vulnerable node-pair is called critical pair (which consists of the primary node and the secondary node pair) [19], [20]. Fig. 28 depicts Q_{crit} of the primary node versus the secondary node for all tested cells. Since the area below the curve is proportional to the tolerance, any combination of charge pairs that falls above

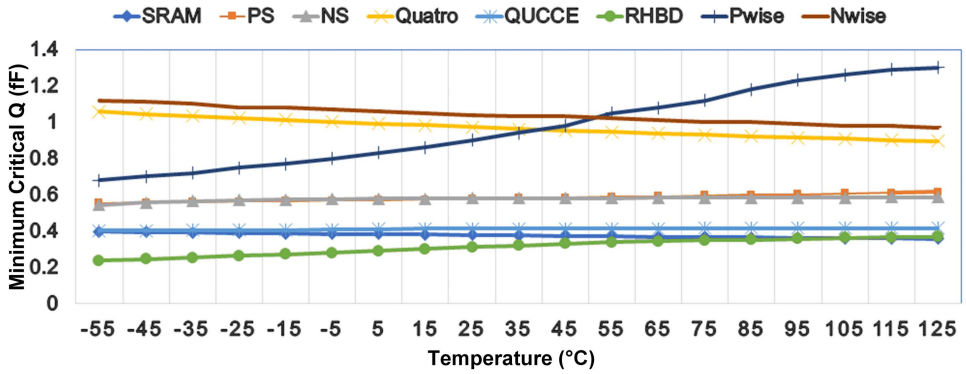

FIGURE 27. Minimum critical charge comparison between all considered cells for the temperature range of −55 to +125 °.

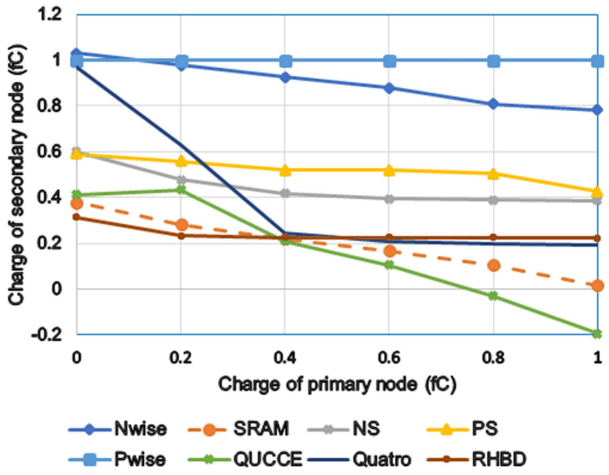

FIGURE 28. Critical charge plot on the critical pair for considered cells.

the curve will cause an upset [19], [20], and change in the stored SRAM data value. Therefore, a cell with a larger area under the plotted curve shows higher tolerance of the cell to MEUs. Hence, according to Fig. 28, the Nwise and Pwise cells have significantly higher multiple-node upset robustness compared with other cells.

6) DISCUSSION

The cost comparisons for all considered cells are summarized in Table 2. The Nwise and Pwise cells have the highest Q_{crit}, which is the most important feature of our proposed cells. As we outline in Section IV-A5, the capacitances of the critical nodes of the Pwise and Nwise cells are larger than the other tested cells contributing to the higher Q_{crit}. The structure of the cells is also important since the transistors that are in the feedback paths increase the capacitance of the critical nodes. Only Quatro has comparable Q_{crit} with Nwise and Pwise. Quatro does not support full SEU immunity, however.

Nwise and Pwise consist of two cross-coupled transistor pairs, one is made of two cross-coupled NMOS transistors and the other of two cross-coupled PMOS transistors. Each of the Nwise and Pwise cells are also equipped with two feedback paths, the feedbacks consist of one NMOS and one PMOS. Since different PMOS or NMOS transistors with different sizes are placed in the read and write paths we get different cost results for each cell. For instance, the Nwise cell has higher write delay. This is because the N3 and N4 transistors, that have been added to the feedback paths to enhance the robustness, increase the driving loads in Q and QB, thus making the write operation slower. Other reported results have similar justifications.

It is observed that, compared with the simulated cells with comparable SEU tolerance capability (Nwise, Pwise, and Quatro), the Nwise cell has low read delay and read power consumption while the Pwise cell has low write and read delay. Therefore, Nwise can be a right choice for cache memory designs of space applications, because in most of cache typical applications, the number of reads is considerably higher than the number of writes [53], [54]. Hence, a cell candidate with low read delay and read power consumption appears more useful. On the other hand, the Pwise cell can be a proper candidate for register file designs of space application because in most typical register files, performance is an essential necessity [72], and a cell candidate with faster read and write operation appears more useful.

V. CONCLUSION

In this paper we propose the Pwise cell, a highly reliable radiation hardened SRAM cell, which is designed with 28nm FD-SOI and inspired from our previously proposed highly reliable radiation hardened SRAM cell, the Nwise cell. In addition, in this paper, the Nwise and Pwise cells and a selection of previously proposed radiation hardened cells, which can be used to design high dense memory structures for space applications, are comprehensively simulated and compared with each other. The simulation of all cells is based on optimized layout in a commercial 28nm FD-SOI technology.

Our simulations confirm that the Nwise and Pwise cells are promising candidates for radiation hardened SRAM designs

to use in different memory blocks for space applications: Compared with all the simulated cells, both designs have the highest level of SEUs tolerance capability for the temperature range deployed in space applications; meanwhile, both have the highest level of the tolerance capability to MEUs. Furthermore, compared with the simulated cells that have comparable tolerance capability, the Nwise cell has low read delay and read power consumption, hence, it can be a good choice for cache designs in space application, while the Pwise cell can be a proper candidate for register file designs since it has low write and read delay.

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