Low Inductive Platform for Long- and Short-term Dynamic Charaterization of SiC MOSFETs

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***Abstract*—State-of-the art Silicon Carbide Power MOSFETs switch at unprecedented speed. Therefore, special attention must be paid to the circuit design of dynamic characterization setups. Only if parasitic layout inductances are minimal, the electrical behavior during switching transients is dominated by the MOSFET characteristics, fast switching is compatible with low overshoot and ringing, and measurement data constitutes reliable characterization data. This paper presents a low inductive test platform for devices in a TO-247-3 housing. The test platform contains measurement terminals for high bandwidth measurement of both current and voltage. The experiments presented in this paper prove that high-fidelity dynamic characterization data can be obtained from Double-Pulse Tests (DPTs) using the presented test platform. Equally accurate measurements can be obtained in long-term tests and under both hard- and soft-switching conditions.**

***Keywords*—Power MOSFET, SiC, Dynamic Characterization**

I. Introduction

Silicon Carbide (SiC) Power MOSFETs are becoming increasingly attractive for Power Electronic Converter applications because of their superior thermal behavior and faster switching speeds compared to Silicon counterparts [1]–[3]. Using SiC instead of Silicon (Si) devices, either higher breakdown voltages can be realized for the same on-state performance, or lower on-state losses for the same breakdown voltage [1]–[3].

For the successful integration of such power switches into converter systems, accurate data on their characteristics are required. Both converter and characterization circuits must be carefully designed with respect to parasitic components causing undesired switching effects. If the efforts undertaken to reduce parasitic circuit parameters are insufficient, the circuit layout will dominate the electrical behavior, resulting in suboptimal conversion or measurement data that is not usable for characterization purposes.

Many DPT setups for hard-switching dynamic characterization can be found in literature [4]–[6]. However, most of the presented designs lack the possibility of performing soft-switching tests. Test setups offering this function are often either voluminous and need many components [7] or use snubber circuits [8] that alter the actual characteristics of the Device Under Test (DUT).

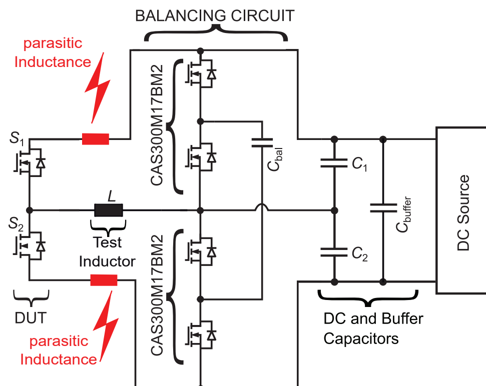
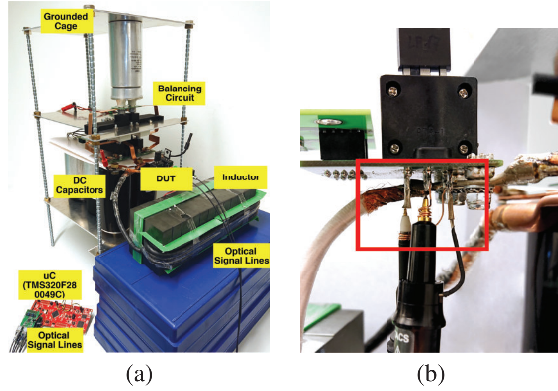


Fig. 1. Previous test setup schematic diagram with emphasized parasitic inductances.

Therefore, ”natural” soft switching [9], [10], i.e. soft switching due to parasitic device capacitances, cannot be investigated.

A test setup enabling both long- and short-term tests under soft- and hard-switching conditions has been developed previously [11]. Fig. 1 presents a circuit diagram of this test setup and Fig. 2 contains photos, showing an overview (Fig. 2a) and custom probing points (Fig. 2b) that ensure low measurement loop inductance. The previous test setup contains several capacitors that provide a maximum DC voltage of $1.8\,\mathrm{kV}$ as well as half of this DC voltage at a midpoint terminal between two series connected capacitors. A switched capacitor circuit is used for balancing the midpoint voltage during long-term or multiple short-term tests.

Despite its flexibility and versatility, the measurement results of this previous test setup are of limited use for dynamic power switch characterization. The DUT is attached to the DC capacitors using a $5\,\mathrm{cm}$ long stranded wire which is partly visible on the right side of Fig. 2b. The resulting large contributions to the power loop inductance are marked red in Fig. 1. Furthermore, the gate driver is placed on a separate Printed Circuit Board (PCB). It is connected to the switching devices using $2.4\,\mathrm{mm}$ spaced header pins and sockets, that can be seen on the left side of Fig. 2b. This connection and the additional tracks that are necessary due to the socket size, add inductance in the gate loop. Altogether, excessive parasitic inductances lead to intense oscillations and large



(a) (b)

Fig. 2. Photos of the Previous Test Setup. (a) Overview. (b) Probing points with wire attachment. From [11].

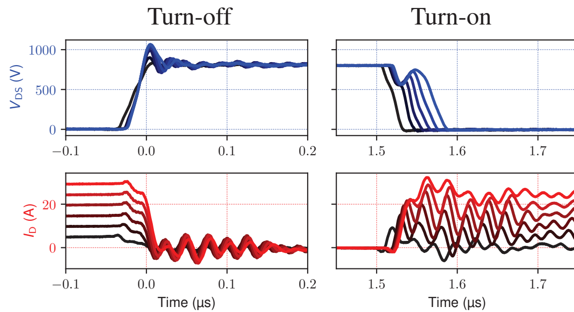


Fig. 3. Voltage and Current Waveforms of Previous Test Setup (Rohm SCT3080KL [12], $R_G = 5.4\ \Omega$, $V_{test} = 800$ V, $I_{test} = 5$ A...30 A in 5 A steps)

overshoot in both device currents and voltages, as can be observed on the turn-on and turn-off switching transients shown in Fig. 3. Due to this strong distortion, the results do not represent the actual device behavior well.

This paper presents an improved low-inductive version of the previously proposed characterization test circuit for SiC MOSFETs, suitable for hard- and soft-switching tests. Detailed guidelines for designing such characterization circuits are presented. The paper is organized as follows. Section II describes the circuit layout, its components, and what measures where taken to improve the dynamic behavior of the circuit. Section III analyzes the most crucial challenges of designing and operating such test circuit. Experimental results are shown in Section IV and the Conclusions are given in Section V.

II. Low Inductive Test Platform

To augment the previous test setup, a test platform was developed that fulfills the following design goals:

1) The new circuit should feature an interface to the existing test setup, so that the long-term test capability is preserved by establishing a connection to the existing test setup.
2) The parasitic layout influence is minimized. The focus is on the power loop inductance.
3) Terminals must be designed for the integration of high-bandwidth voltage and current measurement systems.
4) Exchange of DUTs should be fast and cause only little wear.
5) The optical signal interface should be preserved to ensure compatibility.

These design goals were addressed by the following measures:

1) A new PCB was designed. It contains three pads for electrically connected it to the balancing circuit as well as additional DC capacitors.
2) Measures taken to minimize parasitic effects of the circuit layout include:
   a) Both foil and ceramic capacitors were placed as close as possible to the DUT. The ceramic capacitors have a lower Equivalent Series Inductance (ESL) and can therefore provide energy faster than the foil capacitors. The foil capacitors have a higher capacitance; thus, they can provide more energy. In combination, they provide sufficient filtering capability.
   b) Tracks are kept as short as possible to minimize layout inductance.
   c) A copper layer thickness of $400\,\mu\mathrm{m}$ ensures a low track resistance and high current carrying capability.
   d) The PCB features a gate driver, ensuring low parasitic inductance in the gate loop. It is a conventional gate driver employing the IXYS IXDN610YI [13] totem-pole integrated circuit. It switches between fixed gate voltage levels for turn-on (+20 V) and turn-off (-5 V) and incorporates a fixed gate resistor, referred to as the "external gate resistor" in the following.

   The circuit layout was modeled and simulated using Finite Element Method (FEM) tools. From these simulations, parasitic inductances of $7.75\,\mathrm{nH}$ in the power loop and $14\,\mathrm{nH}$ in the gate loop have been found.
3) The PCB provides probing points:
   a) As in the previous test setup, terminals allow the connection of passive voltage probes close to the PCB. This decreases measurement loop inductance and thereby enables high measurement bandwidth.
   b) SMA connector pads are provided for optional installation of alternative custom probes. Such probes may be active and thereby increase the measurement sensitivity. Attention must be paid to the voltage rating of the SMA connectors in question.
   c) For the current measurement, multiple

approaches can be chosen. A Rogowski Coil and a current clamp were attached using a wire loop. A Rogowski Coil (CWTMini HF6 [14]) had also been chosen in the previous test setup. Therefore, a comparative evaluation of the old and new platforms is possible. However, the Rogowski Coil used for the new platform (CWT UM CWT06 [15]) is a different model due to placement constraints.

d) A socket for TO-247-3 devices was developed. It offers flexibility while alleviating parasitic effects.

e) The on-board gate driver employs the same optical interface as the gate driver used in the previous test setup.

Fig. 4 shows the low-inductive platform from three different angles. Fig. 4a shows an overview from an elevated angle in the front. The custom socket (in red) with a DUT can easily be identified. An oscilloscope probe is used to measure the Gate-Source voltage and is connected to the circuit using an SMA-BNC-probe-tip adapter and the SMA connector on the PCB. The integrated gate driver is located towards the front side of the PCB. High-voltage decoupling film capacitors (in grey) are placed close to the DUT. The ceramic decoupling capacitors are visible in Fig. 4b that shows the test platform from below. Besides, the screw connections to the DC capacitors as well as the balancing circuit are visible to the left. Fig. 4c shows the platform from a PCB level angle in the front. The passive high-voltage probe (grey, Keysight 10076C) is depicted in the middle of the picture and is attached to the circuit using a ground spring connector (white) and its tip inside a tube that is soldered to the drain and source connectors of the DUT socket. Right next to it, a wire loop soldered to the PCB serves as a probing point for the current measurement by means of a current clamp and a Rogowski Coil.

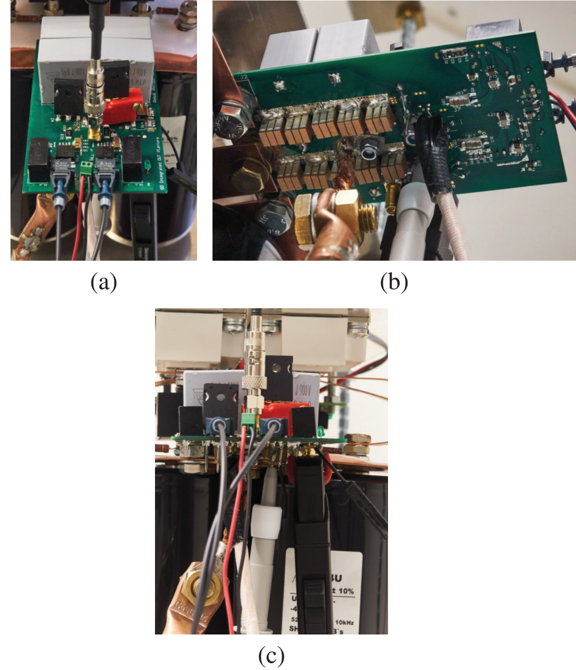


Fig. 4. Photos of the Low Inductive Test Platform. (a) Top. (b) Bottom. (c) Front.

III. Challenges in Low-Inductive Test Platform Design

During the design phase of the low inductive test platform, major challenges were faced pursuing the design goals. The copper track thickness of $400\,\mu\mathrm{m}$ introduces additional heat capacitance. This prolongs the soldering time of components to the PCB. The thermal specifications of devices must be checked carefully.

The spacing of components needs to be reduced significantly to minimize the parasitic effects of PCB tracks. Moving towards high test voltages, a trade-off arises: The insulation of high voltages increases space requirement, but from a parasitic inductance reduction perspective, short tracks are preferred.

Another trade-off is the reduction of parasitic layout effects. Ideally, a DUT is directly soldered on the board, which, however, reduces flexibility. Considering the increased thermal capacitance, an exchange of the DUT takes long time and stresses both the PCB and components close to the DUT as well as the DUTs themselves. Alternatively, a socket that enables plugging and unplugging DUTs can be used. However, such a socket introduces additional inductance and a contact resistance on all terminals. An existing commercial solution for TO-247-3 devices, the PTR-1 socket [16], counteracts circuit minimization because of its large size. Therefore, a custom socket was designed to preserve flexibility on the one hand, and, on the other hand, alleviating the issues mentioned above. Compared to the PTR-1 socket with dimensions of 24 mm x 28 mm x 16 mm (h x w x d), the custom socket only measures 15 mm x 30 mm x 10.5 mm. Especially the reduced socket height leads to a reduction of added parasitic inductance. Further improvement is achieved by using wider conductors inside the socket. In addition, enlarged slit sizes allow for a larger contact areas and thus lower contact resistance. Fig. 5 shows the two sockets in comparison. Both the outside and the inside of the sockets can be seen. The CAD model of the socket is shown in Fig. 6. Fig. 6 (a) shows the socket without screws and the 3D printed plastic in white instead of red. In Fig. 6 (b), a side-cut view of the socket is depicted to clearly show where the electrical contact is established.

IV. Results

Hard-Switching DPTs were conducted using the previous test setup design and the newly designed low-inductive test platform. The test voltage level was set at $800\,\mathrm{V}$ and the current level was varied from $5\,\mathrm{A}$ to $30\,\mathrm{A}$, with the 1.2kV-class SiC Power MOSFET SCT3080KL by Rohm Semiconductor [12] as DUT. The device parameters are listed in Table I. Two devices were soldered

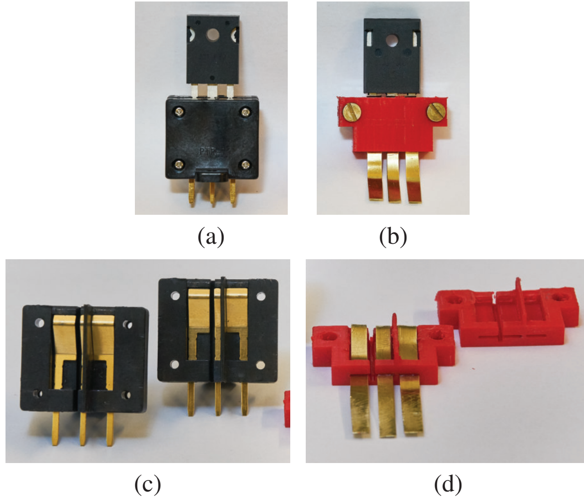


Fig. 5. TO 247-3 device sockets in comparison. (a) Commercial PTR1 socket with DUT. (b) Custom socket with DUT. (c) Inner structure of the PTR1. (d) Inner structure of the custom socket.

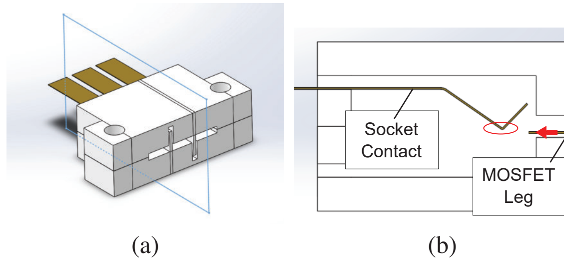


Fig. 6. Custom TO-247-3 socket design in overview (a) and side-cut view with the contact region marked with a red ellipse (b)

on the PCB forming a half-bridge with the lower switch as DUT.

Fig. 7 shows time domain measurements using an external gate resistor of $R_{\mathrm{G}} = 5.4\,\Omega$. Fig. 8 shows time measurements under identical conditions except for an external gate resistor of $R_{\mathrm{G}} = 10\,\Omega$. As can be seen by comparing these results, the newly developed low-inductive test platform realizes the design goals successfully.

The steepness of both drain current and drain to source voltage are significantly increased compared to the previous test setup. This results from the lower parasitic power loop inductance allowing for a steeper voltage trajectory for the same current slope.

Besides, the circuits show a different sensitivity to changes of the external gate resistor. The switching behavior of the previous test setup is governed by the parasitic power loop inductance of the circuit. Increasing

TABLE I. ROHM SCT3080KL PROPERTIES [12]

Property	Value
Breakdown Voltage Rating	1200 V
Continuous Drain Current Rating	31 A
On-state Resistance (R_{DS}) at Room Temperature ($T = 25\,°\mathrm{C}$)	$80\,\mathrm{m}\Omega$
Package	TO-247-3

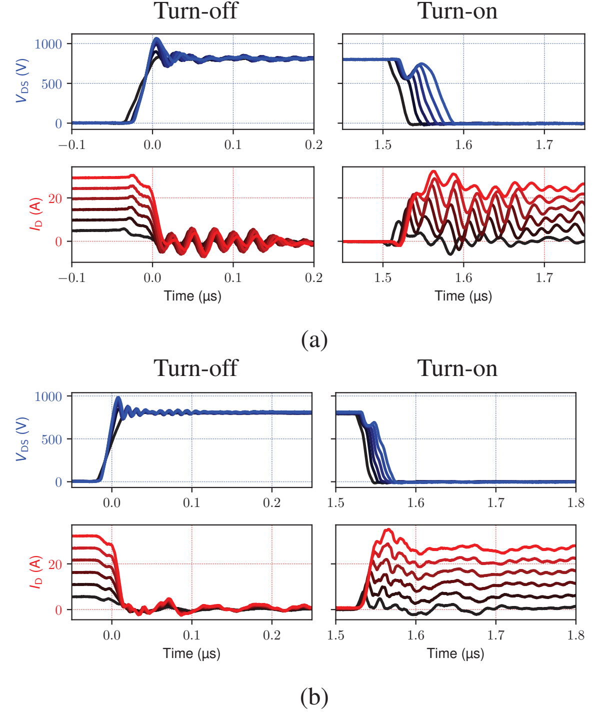


Fig. 7. Voltage and Current Waveforms (Rohm SCT3080, $R_{\mathrm{G}} = 5.4\ \Omega$, $V_{\mathrm{test}} = 800$ V, $I_{\mathrm{test}} = 5$ A...30 A in 5 A steps). (a) Previous Test Setup. (b) Low Inductive Test Platform.

the external gate resistor, oscillations in the current measurement are damped visibly. However, an examination of the measurement data does not clearly indicate the expected increased current rise time. As opposed to that, the influence of the external gate resistance becomes very clear in measurements obtained from the low inductive test platform. Apart from the obvious damping effect on the switching oscillations, both voltage and current steepness change visibly. The low-inductive test platform thereby does not only enable characterizing the device behavior adequately but also enables Gate Driver Unit (GDU) evaluation. For this purpose, the GDU of choice is connected to multi-use pads located very close to the switching devices on the PCB.

It must be noted that the MOSFET used in the experiments (Rohm SCT3080KL MOSFET [12]) contains an internal gate resistance of $12\,\Omega$. Changing the external gate resistor will therefore have a more subtle effect on the behavior of this MOSFET than comparable devices with lower internal gate resistance. Hence, the observable impact of changing the external gate resistance by a little less than $5\,\Omega$ is weak, even when using the low inductive test platform.

To expand this comparison, the switch current frequency content of the DPT experiments with an external gate resistance of $5.4\,\Omega$ are compared to each other. To apply a Fast Fourier Transform (FFT), the regions between the first and the second turn-off instances have been isolated to cut out data that is irrelevant for the dynamic signal content. Excerpts of the resulting frequency spectra

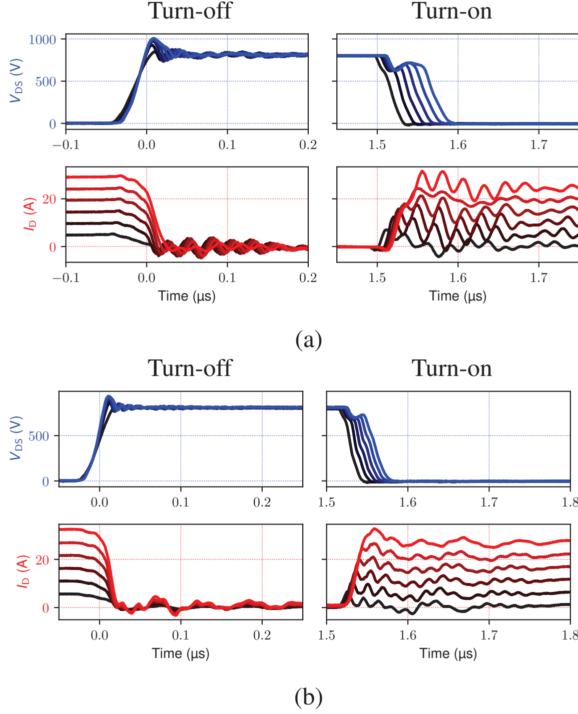


Fig. 8. Voltage and Current Waveforms (Rohm SCT3080, $R_G = 10\ \Omega$, $V_{test} = 800$ V, $I_{test} = 5$ A…30 A in 5 A steps). (a) Previous Test Setup. (b) Low Inductive Test Platform.

are shown in Fig. 9. Furthermore, the fourier coefficients of an ideal square wave with an amplitude of 30 A and the same timing as the DPT have been calculated. The black dots in Fig. 9 represent the non-zero absolute values of the fourier coefficients resulting from this analysis. They serve as an ideal case scenario to compare the measurement transformations to.

The FFT of the current measurements of both the previous design and the low inductive test platform follow the ideal fourier coefficiens well below a frequency of 20 MHz. At higher frequencies, however, they deviate from the fourier coefficients for several reasons.

- The inductor current rises while the lower switch is turned on. Therefore, the current trajectory is actually closer to a trapezoid than a square wave.
- The Rogowski Coils used for current measurements have a limited bandwidth of 30 MHz [14], [15]. With the filter design of the Rogowski Coils, frequency contents above the bandwidth limit are dampened.
- However fast MOSFETs switch, rise and fall times are limited. In addition, the outer circuitry poses limitations on what how fast switching transitions can be. Therefore, the switch current is expected to have lower high frequency content than an ideal square wave.

However, large differences between the previous design and the low inductive test platform can be observed.

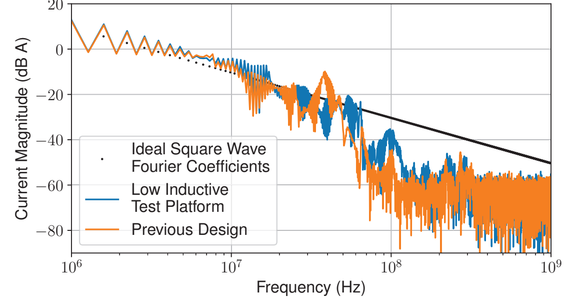


Fig. 9. Frequency Spectra of Drain Currents (Rohm SCT3080KL, $R_G = 5.4\,\Omega$, $V_{test} = 800\,$V, $I_{test} = 30\,$A) and Absolute Fourier Coefficient Values of a 30 A Ideal Square Wave

Between 30 MHz and 40 MHz, the current level of the previous design is elevated by up to 15 dB compared to the ideal fourier coefficients, and more than 20 dB compared to the low inductive test platform. These large frequency components are caused by the parasitic oscillations due to the high parasitic power loop inductance. This hypothesis is supported by that there is no additional damping introduced in the low inductive test platform that would explain the drop in frequency content in this region. In addition, the frequency contents of the previous design measurements drop steeply for higher frequencies, until they reach noise level at around 70 MHz to 90 MHz. The large power loop inductance acts as a very strong low pass filter for frequencies beyond its main oscillatory peak.

Measurements made with the low inductive test platform show main current oscillation frequencies between 50 MHz and 60 MHz instead, with a maximum of only 6 dB more than the ideal fourier coefficients. This shift to higher frequencies and the significantly reduced amplitudes illustrate the superior dynamic behavior of the presented low inductive test platform. The change of the current sensor is expected to have a minor influence on the measurement comparison. The bandwidth specification is identical and also rise times show very similar values [14], [15].

V. Guidelines for Low Inductive Circuit Design

The low inductive design of the proposed test platform for SiC MOSFET characterization follows principles that are vital for softening the influence of parasitic circuit elements on measurement data. A circuit designer facing challenges with the reduction of Electromagnetic Interference (EMI), strong oscillations and device performance that falls behind component specification may revisit the following aspects in their product.

- **Track length.**
  The most important aspect when creating a low inductive circuit is to cut back on what introduces inductance. Tracks on the PCB contribute most to parasitic inductance that is avoidable. Other

contributors are device packages, and especially the internal electrical connections between dies and package terminals. Track length minimization is, however, partly limited by component geometry, as well as clearance and creepage demands depending on the voltage level.

- **Decoupling.**
  Decoupling means to introduce capacitors that provide energy from the supply, close to the DUT. Oscillations can be suppressed, if this energy is large enough and not separated from the device electrically by a too large inductance. If space constraints make it difficult to place capacitors close to the DUT, small outline components should be used despite their low capacitance. It is advisable to use capacitors of different size and technology for their different filtering properties. Placing small capacitors near the DUT will help provide the energy needed for a fast commutation while larger capacitors further away will act as an energy source for the load current.
- **Measurement Equipment.**
  Probes for measuring electrical quantities introduce parasitic capacitance (voltage sensors) and inductance (current sensors). Choosing the right sensor technology is therefore important to increase the reliability of the measurement data. Another aspect to take into account is the specification of the sensors, particularly the sensor bandwidth. Finally, adequate probing points need to be chosen. They should be close to the device, so as to not introduce too much inductance since this would falsify the measurement results as it reduces measurement bandwidth and make the sensor more prone to coupling with fast changing fields in the surrounding circuitry. To further improve EMI resilience, shielding is advisable. Probe manufacturers proved PCB tip adapters that can help with shielding. For low voltages, also standard coaxial adapters have been found to improve signal quality.

VI. Conclusion

A low-inductive test platform for TO-247-3 devices has been developed. It augments a previously designed test setup that has both short- and long-term test capability under hard- and soft-switching conditions. Circuit miniaturization through careful component placement and parasitic inductance reduction through track length minimization enable high quality characterization measurements. In addition, a custom TO-247-3 socket enables quick and non-destructive DUT replacement. It thereby preserves high flexibility in the process of characterizing multiple devices.

VII. Acknowledgement

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