Four Level Voltage Active Gate Driver for Loss and Slope Control in SiC MOSFETs

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***Abstract*—Silicon Carbide power semiconductors exhibit fast dynamic behavior. This facilitates the design of high efficiency and high power density converters. However, the resulting current and voltage changing rates demand extensive filtering to avoid electromagnetic interference and ensure safe operation. In addition, temperature fluctuations due to varying load currents from renewable energy sources pose challenges for power semiconductor device lifetime and reliability. Active temperature control can reduce temperature fluctuations, but affects switching slopes simultaneously. This leads to variable electrical stress on both device and circuit level. In this paper, a four-level active voltage-source gate driver for SiC MOSFETs is proposed, enabling manipulation of switching and conduction losses. Switching losses are manipulated by controlling the duration as well as amplitude of intermediate gate voltage pulses during switching transients. Conduction losses can be influenced by adjusting the positive gate voltage. Simulations indicate that the proposed gate driver allows decoupling switching loss and slope control. To validate the gate driver concept, a prototype has been built and evaluated in double pulse test experiments.**

***Index Terms*—Silicon Carbide, WBG, Active Gate Driver, Active Temperature Control**

I. Introduction

Silicon Carbide (SiC) based Metal–Oxide–Semiconductor Field-Effect Transistors (MOSFETs) exhibit faster switching dynamics and lower on-state resistance for the same blocking voltages compared to their Silicon (Si) Insulated-Gate Bipolar Transistor (IGBT) counterparts [1]. Their fast switching speed means high voltage change rates (dv/dt) and current change rates (di/dt), that can cause strong Electro-Magnetic Interference (EMI), crosstalk, and potentially, a shoot-trough fault [2].

In addition, Renewable Energy Sources (RES) such as photovoltaics and wind power, have an intermittent power generation profile that translates into a varying converter load current. The resulting switching device loss and temperature fluctuations expedite bond-wire lift-off and solder delamination, which are major failure modes in power semiconductor devices [3]. Active Temperature Control (ATC) can reduce the amplitude of temperature stress cycles and thereby improve device reliability and lifetime [4], [5].

Several active gate driver (AGD) concepts that enable ATC by providing power loss manipulation during switching events as well as the conduction phase, have been presented in literature [2], [4]–[9], [12]. Current-source gate drivers allow precise gate capacitance charging and thereby switching transient control [6]–[8]. However, current control necessitates a high precision variable voltage source and a high bandwidth signal path to control it. This is needed to either set the operating point of a current mirror or saturation current source configuration of a semiconductor switch. As a consequence, current source type gate drivers are complex and prone to parameter drift as well as EMI.

Step-wise gate drivers alter the gate charging dynamics by activating a variable number of parallel output stages with different or identical serial resistors [3], [10], [11]. This approach exhibits an easier control than current source gate drivers because unlike controlled current sources, the paralleled output stages are simple topologies, and high precision resistors are easily available. With emerging digital electronics, a large amount of parallel output stages enables fine grain control of the gate charging process [10]. However, large digital bandwidths or complex digital signal sources such as Complex Programmable Logic Devices (CPLDs) or Field Programmable Gate Arrays (FPGAs) are needed on the gate driver, increasing EMI vulnerability. Besides, the necessary circuit layouts and components are both complex and costly.

Multilevel voltage gate drivers offer a compromise between power switch controllability and gate driver complexity. Intermediate voltage pulses with an amplitude between the positive and negative gate voltage during the switching transitions are produced by this gate driver type. Either the amplitude [2] or the timing [9] of these intermediate voltage pulses are controlled. This allows for switching loss, switching slope, and voltage as well as current overshoot control. Controlling either intermediate voltage pulse amplitude or timing however, leaves

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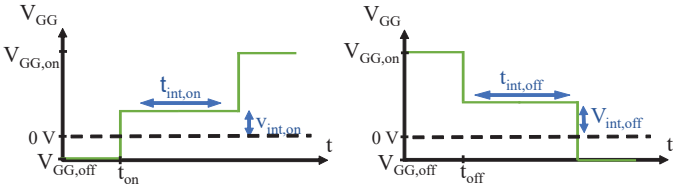


Fig. 1: V_{GG}-waveform during turn-on (a) and turn-off (b)

transient slopes and switching loss coupled and inseparable of each other.

This paper introduces a four level voltage active gate driver capable of manipulating switching losses and transient slopes of a discrete SiC MOSFETs. Variable intermediate voltage levels are supplied to the gate with a configurable duration during turn-on and turn-off. The proposed gate driver can influence the switching losses, switching slopes as well as voltage and current overshoot of SiC MOSFETs, extending the capabilities of earlier presented gate drivers [2], [9]. In addition, conduction losses are controllable by an adjustable positive gate voltage.

The rest of the paper is organized as follows: In Section II, the proposed gate driver is introduced and the operational principle is explained. Section III shows the simulation results and IV presents the experimental results. In addition, the impact of the gate driver on the SiC MOSFET performance is discussed and the results are analyzed in these sections. Finally, conclusions are presented in Section V.

II. Proposed Four Level Voltage Active Gate Driver

The aim of the proposed active gate driver is to control the switching slopes and the switching loss of SiC power MOSFETs. To achieve this goal, a multilevel voltage gate driver applies an intermediate voltage level during switching that is between the positive and negative driving voltages. Thereby, the gate charging process can be controlled, which in turn influences the voltage and current transitions of the switching device and thus, the switching loss.

Figs. 1a and 1b show the proposed turn-on and turn-off gate driver voltage (V_{GG}) pattern. Before the turn-on switching instance ($t < t_{\mathrm{on}}$), V_{GG} equals the turn-off driving voltage ($V_{\mathrm{GG,off}}$), and the MOSFET is kept in the off state. At $t = t_{\mathrm{on}}$, the driver voltage is raised to the intermediate turn-on voltage ($v_{\mathrm{int,on}}$). This voltage level is held for the duration of the intermediate turn-on voltage level ($t_{\mathrm{int,on}}$). Afterwards, V_{GG} is switched to the turn-on driving voltage ($V_{\mathrm{GG,on}}$) and held at this voltage value until the next switching instance. At turn-off, this procedure is repeated. Both the intermediate turn-off voltage ($v_{\mathrm{int,off}}$) and the duration of the intermediate turn-off voltage level ($t_{\mathrm{int,off}}$) are chosen independently from their correspondents at turn-on.

In a conventional gate driver, a simple step is applied to the gate. Introducing an intermediate voltage step will add a degree of freedom to the gate charging speed. If, for example, a

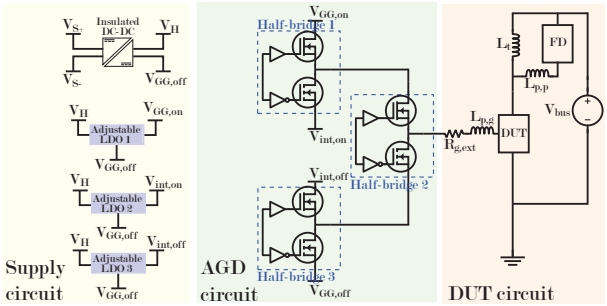


Fig. 2: Schematic diagram of the proposed gate driver

lower intermediate voltage level than the positive gate voltage is applied to the gate at turn-on, the gate charging process is slowed down. Depending on the duration of the intermediate voltage level, the slower gate charging process will slow down the current and voltage transitions. In addition, the switching loss is increased by prolonging the switching process.

Different operation schemes have been presented in literature [2], [9]. These differ from the proposed scheme of driving the multilevel voltage gate driver. Between the intermediate voltage level intervals and the high driving voltage, an interval of low driving voltage is inserted [2], [9] and varied in duration [9].

Initially, introducing a variable time delay before the intermediate voltage level was considered. However, simulations showed that altering these time delays had a similar impact to altering the duration of the intermediate voltage levels ($t_{\mathrm{int,on}}$ and $t_{\mathrm{int,off}}$ in Fig. 1a and 1b). Therefore, the delay variation was not further investigated.

A circuit that can provide the desired voltage pattern has been derived. The schematic diagram of this proposed gate driver is shown in Fig. 2. The gate-drive circuit consists of two parts, the AGD circuit and the supply circuit. As can be seen from Fig. 2, three half-bridge circuits are used to provide the four voltage levels to the gate. Three of the four voltage levels are variable. They are provided by adjustable low-dropout regulators (LDOs), which can be seen in the supply circuit part of Fig. 2. This particularly includes the positive gate voltage, permitting control of the active region of the power MOSFET and thereby conduction losses.

To verify the functionality of the gate driver topology seen in Fig. 2, a gate driver prototype was built and tested. A photo of prototype circuit is shown in Fig. 3. The supply circuit, which is not shown in the picture, is located behind the main gate driver board. The output voltage of each adjustable LDO is controlled using a digital potentiometer inside the LDO feedback loop. This digital potentiometer is controlled over SPI.

Both the signals required to create the desired patterns and the SPI signals to set the intermediate voltage levels are generated by a C2000 series microcontroller by Texas Instruments [14]. This microcontroller also provides the gate signals for the balancing circuit of the test setup that compensates for

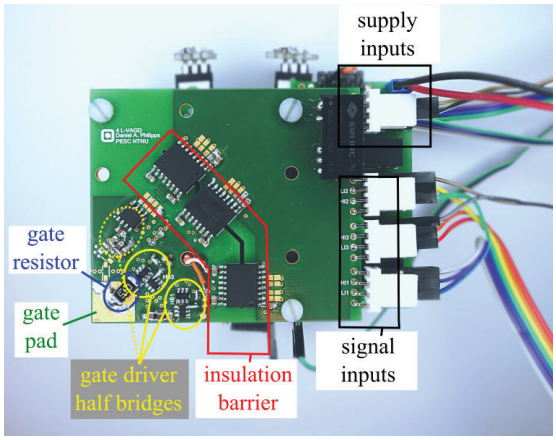


Fig. 3: Photo of proposed AGD. The source pad is located on the back side of the PCB, directly behind the gate pad.

TABLE I: Circuit parameters used during simulations

V_{bus}	I_{load}	$R_{\text{g,ext}}$	L_{t}	$L_{\text{p,g}}$	$L_{\text{p,p}}$	T_{amb}
800 V	20 A	25 Ω	110 µH	1 nH	5 nH	25 °C

any imbalances that result from repeated double pulse tests [21].

III. Simulation Results

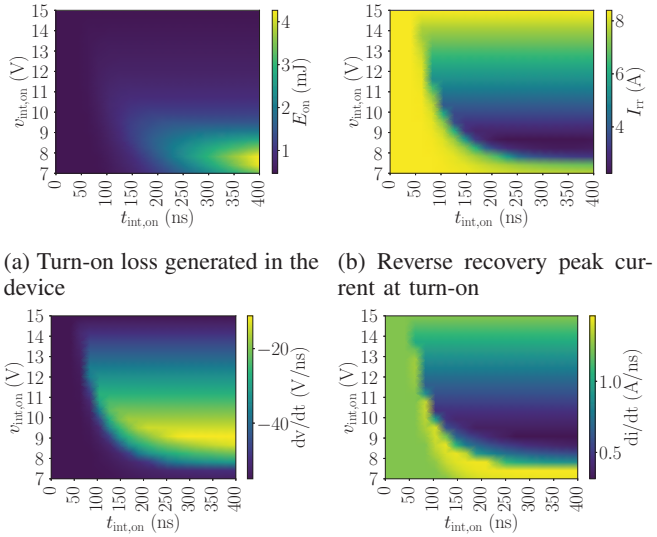
To investigate the functionality and the electrical performance of the gate driver topology seen in Fig. 2, a simulation study was conducted. In this simulation study, hard-switching conditions of a double-pulse test were imposed on a MOSFET model that is driven by a model of the gate driver.

A. Circuit Modelling

The circuit parameters used in the simulation are summarized in Table I. V_{bus} is the DC-link bus voltage, I_{load} the load current and $R_{\text{g,ext}}$ the external gate resistance. The load inductance is L_{t}, while $L_{\text{p,g}}$ and $L_{\text{p,p}}$ are the parasitic inductances in the gate and power loop respectively. T_{amb} denotes the ambient temperature. A model of the Wolfspeed Silicon Carbide Power MOSFET C3M0075120K was used both as the device under test (DUT) and the free-wheeling device (FD). This model is a modified version of the manufacturer model, optimized for eliminating convergence errors [13].

B. Gate Driver Modelling

An idealized model of the proposed gate driver was used for the simulations. It consists of an ideal voltage source providing the proposed gate voltage pattern and an external gate resistor. The voltage changing times of the voltage source were set to 1 ns. In a real application, the low power MOSFETs of the output stage are expected to provide slightly slower slopes. However, the power MOSFET input capacitance is so large, that this is expected to dominate the gate voltage dynamics instead of the low power MOSFETs. Hence, modelling the gate driver as described above is considered adequate.



(a) Turn-on loss generated in the device

(b) Reverse recovery peak current at turn-on

(c) dv/dt at turn-on generated in the device

(d) di/dt at turn-on generated in the device

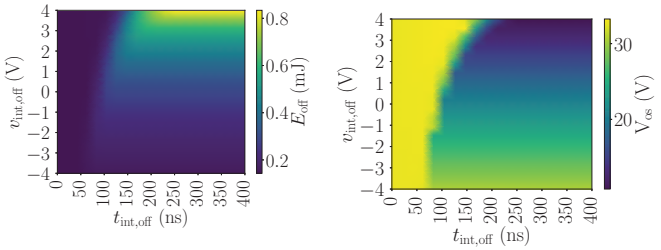
Fig. 4: Influence of $v_{\text{int,on}}$ and $t_{\text{int,on}}$ on performance parameters during turn-on

The values of $v_{\text{int,on}}$ were varied from 7 V to 15 V, and $v_{\text{int,off}}$ from −4 V to 4 V. The pulse durations $t_{\text{int,on}}$ and $t_{\text{int,off}}$ were varied from 0 ns to 400 ns. The turn-on driving voltage was set to $V_{\text{GG,on}} = 15\,\text{V}$ and the turn-off driving voltage was set to $V_{\text{GG,off}} = -5\,\text{V}$. The performance of the proposed gate driver was examined by looking at the turn-on switching loss (E_{on}), reverse recovery peak current (I_{rr}), turn-off switching loss (E_{off}), voltage overshoot (V_{os}), dv/dt, and di/dt. I_{rr} is calculated from the simulation results as the difference between peak reverse recovery current and load current. Similarly, V_{os} is determined as the peak overshoot voltage minus the DC bus voltage. Turn-on and turn-off transients were investigated separately.

C. Simulation Results Discussion

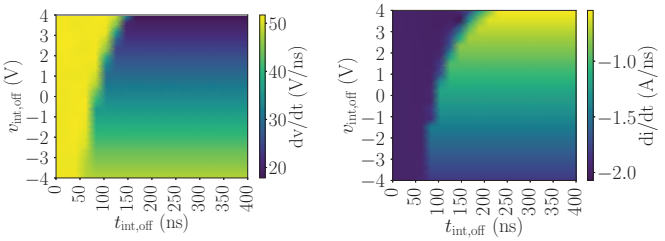
Fig. 4 illustrates various switching characteristics at turn-on under variation of $t_{\text{int,on}}$ and $v_{\text{int,on}}$. From Fig. 4, the impact of altering $t_{\text{int,on}}$ and $v_{\text{int,on}}$ is clearly visible. For some $v_{\text{int,on}}$ values, changing $t_{\text{int,on}}$ has no significant effect on the presented performance parameter values. For $v_{\text{int,on}}$ values $\lessapprox 12\,\text{V}$, increasing $t_{\text{int,on}}$ leads to higher E_{on}. If $v_{\text{int,on}} \gtrapprox 12\,\text{V}$, altering $t_{\text{int,on}}$ has a negligible impact on E_{on}. The impact of $v_{\text{int,on}}$ and $t_{\text{int,on}}$ on I_{rr} and di/dt is very similar. If $t_{\text{int,on}}$ is below approximately 50 ns, changing $v_{\text{int,on}}$ has almost no impact. For the turn-on switching transient, there is a clear region where the AGD is able to impact I_{rr} and di/dt. This region is where $t_{\text{int,on}} \gtrapprox 50\,\text{ns}$ and $v_{\text{int,on}} \in [\,8\,\text{V}, 13\,\text{V}]$. The behavior of dv/dt (Fig. 4c) is similar to I_{rr} and di/dt, but the impact of $v_{\text{int,on}}$ and $t_{\text{int,on}}$ is inverted.

Fig. 5 illustrates various switching characteristics at turn-off under variation of $t_{\text{int,off}}$ and $v_{\text{int,off}}$. Altering $t_{\text{int,off}}$ and $v_{\text{int,off}}$ has a similar impact on all four switching characteristics.



(a) Turn-off loss generated in the device

(b) Voltage overshoot at turn-off



(c) dv/dt at turn-off generated in the device

(d) di/dt at turn-off generated in the device

Fig. 5: Influence of $v_{\text{int,off}}$ and $t_{\text{int,off}}$ on performance parameters during turn-off

As can be seen in Fig. 5, there is a range of $t_{\text{int,off}}$ values where altering $v_{\text{int,off}}$ has a negligible impact on the switching characteristics. This range increases with increasing $v_{\text{int,off}}$. At $v_{\text{int,off}} = -4\,\text{V}$, $t_{\text{int,off}}$ must be greater than approximately $60\,\text{ns}$ before a large change in the switching characteristics is observed. When $v_{\text{int,off}} = 4\,\text{V}$ the large change happens when $t_{\text{int,off}} \gtrapprox 175\,\text{ns}$. In general, E_{off} and di/dt increases by increasing $v_{\text{int,off}}$, while V_{os} and dv/dt decrease by increasing $v_{\text{int,off}}$.

The simulation results show that the proposed AGD enables control of the switching performance of discrete SiC MOSFETs. By introducing an intermediate voltage level during switching, the voltage drop across the external gate resistor can be actively lowered. The result is a lower gate current, charging the MOSFET input capacitance more slowly and thus the switching transients are slowed down. Since the external gate resistor is fixed, the amplitude of the intermediate voltage level, i.e. $v_{\text{int,on}}$ or $v_{\text{int,off}}$ respectively, determines the gate current and thus, the switching slope. This can be seen in Fig. 4 for $t_{\text{int,on}} \gtrapprox 75\,\text{ns}$ and $v_{\text{int,on}} \gtrapprox 7.5\,\text{V}$. In this region, changing $v_{\text{int,on}}$ affects the switching slope. Decreasing $v_{\text{int,on}}$ slows down the switching slope causing increased E_{on} and dv/dt, while reducing I_{rr} and di/dt. Increasing $v_{\text{int,on}}$ has the opposite effect on the switching characteristic.

The intermediate voltage amplitude is not immediately reflected at the gate of the MOSFET since the external gate resistor and the MOSFET input capacitance form a low-pass filter. Varying the duration of the intermediate voltage level therefore determines, for how long the slowdown described above is in effect, if it is shorter than the time constant of the RC low-pass filter mentioned above. If it is significantly longer, it determines the operating point that the MOSFET is held in with the respective $v_{\text{int,on}}$ and $v_{\text{int,off}}$ values. In Fig. 4 and 5, this impact can be seen. If the duration of the intermediate voltage levels ($t_{\text{int,on}}$ and $t_{\text{int,off}}$) are too short, $v_{\text{int,on}}$ and $v_{\text{int,off}}$ have a strongly reduced influence. This can be seen in Fig. 5, where a short $t_{\text{int,off}}$ value causes $v_{\text{int,off}}$ to have a negligible impact on the switching performance. The duration of $t_{\text{int,off}}$ required for $v_{\text{int,off}}$ to have a large impact on switching performance changes based on the value of $v_{\text{int,off}}$. For values of $v_{\text{int,off}}$ closer to $V_{\text{GG,off}}$, already shorter durations of $t_{\text{int,off}}$ lead to large changes in switching performance compared to more positive values of $v_{\text{int,off}}$. That is because more positive $v_{\text{int,off}}$ values slowing down the switching process.

D. Switching Transient Control

For each switching instance, there are two control variables to manipulate the MOSFET switching performance: $v_{\text{int,on}}$ and $t_{\text{int,on}}$ for turn-on; $v_{\text{int,off}}$ and $t_{\text{int,off}}$ for turn-off. Designing an effective and stable control, the following aspects have to be considered. Controlling the MOSFET behavior requires less precision in the control system in regions, where the controlled variable exhibits small gradients. For example, Fig. 4c shows that for $t_{\text{int,on}} \gtrapprox 250\,\text{ns}$, varying $v_{\text{int,on}}$ from $7\,\text{V}$ to $9\,\text{V}$ has the same effect as varying it from $15\,\text{V}$ to $9\,\text{V}$. However, the gradients are greatly different. As earlier mentioned, high precision voltage control is challenging. Hence, a variation of $v_{\text{int,on}}$ between $9\,\text{V}$ to $15\,\text{V}$ is more desirable for dv/dt control.

On the other hand, to achieve decoupling of the voltage and current slopes (dv/dt and di/dt) and the switching loss, additional requirements on the choice of control variable combinations must be accepted. For the turn-on transient (Fig. 4), $v_{\text{int,on}} \approx 7\,\text{V}$ and $t_{\text{int,on}} \in [\,150\,\text{ns}, 400\,\text{ns}]$, the turn-on energy E_{on} can be altered without large changes in dv/dt and di/dt by varying $t_{\text{int,on}}$. If $v_{\text{int,on}} \in [\,11\,\text{V}, 15\,\text{V}]$ and $t_{\text{int,on}} \in [\,100\,\text{ns}, 400\,\text{ns}]$, dv/dt and di/dt can be manipulated without incurring large changes in E_{on}. For the turn-off transient (Fig. 5), the voltage and current slopes can be changed without large changes in E_{off} if $t_{\text{int,off}} \gtrapprox 100\,\text{ns}$ and $v_{\text{int,off}} \lessapprox -2\,\text{V}$.

E. Exemplary Time Domain Simulation Data Evaluation

To investigate the accuracy of the simulations and to directly compare simulations to experiments, exemplary time domain simulation data is shown in Fig. 6. The $v_{\text{int,on}}$ and $t_{\text{int,on}}$ values of these simulations equal the configuration of the experiments that will be shown in Section IV.

Based on the waveforms in Fig. 6 E_{on}, I_{rr}, di/dt and dv/dt were calculated in the same way as Fig. 4 and 5. These switching performance parameters can be seen in Fig. 7.

IV. Experimental Results

A. Description of the Test Setup and Measurement System

A prototype of the proposed AGD was built and tested with a Wolfspeed C3M0075120D Silicon Carbide Power MOSFET [22]. The DUT and FD were mounted on a low inductive test platform that is optimized for dynamic characterization of high switching speed wide-bandgap MOSFETs [19]. This platform has sockets for measuring the gate-source voltage (v_{GS}) and

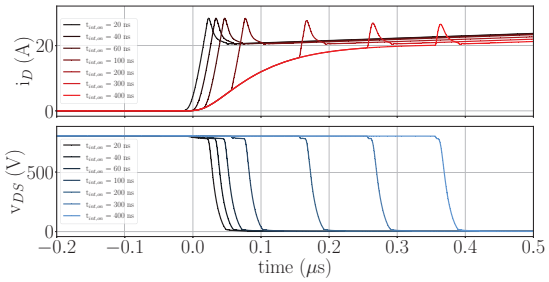
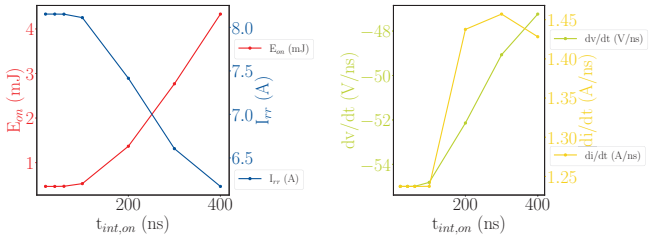


Fig. 6: Simulated drain current (i_{D}) and drain-source voltage (v_{DS}) waveforms under variation of $t_{\mathrm{int,on}}$



(a) (b)

Fig. 7: Simulation MOSFET switching performance parameters

v_{DS}. v_{GS} was measured using a Tektronix TPP1000 passive voltage probe [16], v_{DS}, using a Keysight 10076C passive voltage probe [17]. i_{D} was measured using a SDN-414-05 coaxial current viewing resistor from T&M Research Products Inc. [15]. The measurements were recorded with a Tektronix DPO5104B oscilloscope [18].

B. Gate-Source Voltage Measurement

To verify the functionality of the proposed gate driver, experiments were performed with a DC bus voltage of 0 V first. The gate source voltage measurements of these experiments are shown in Fig. 8. Despite the low-pass filtering effect of the MOSFET input capacitance and the external gate resistor, the AGD prototype is able to generate the proposed gate voltage pattern. $v_{\mathrm{int,on}}$ and $v_{\mathrm{int,off}}$ were varied from low to a high value. $t_{\mathrm{int,on}}$ and $t_{\mathrm{int,off}}$ were varied from a short to a long duration.

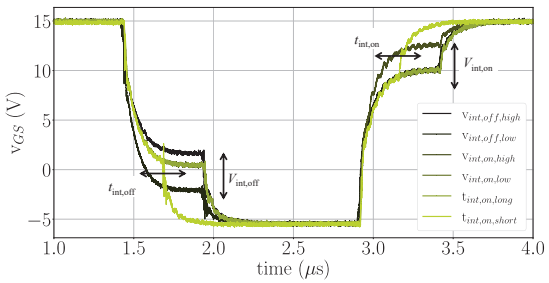


Fig. 8: v_{GS} measurements at $V_{\mathrm{DC}} = 0\,\mathrm{V}$ varying $v_{\mathrm{int,on}}$ and $t_{\mathrm{int,on}}$ with the proposed gate driver

TABLE II: $t_{\mathrm{int,on}}$ and $v_{\mathrm{int,on}}$ values used during experiments

$t_{\mathrm{int,on}}[ns]$	20	40	60	100	200	300	400
$v_{\mathrm{int,on}}[V]$	7.5						

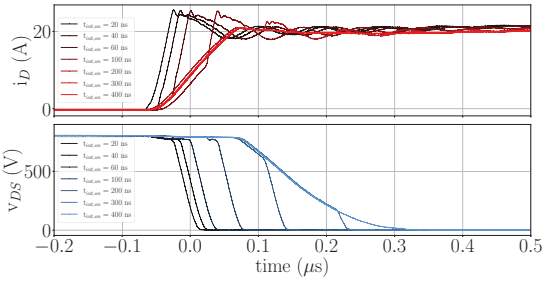


Fig. 9: Experimental turn-on i_{D} and v_{DS} waveforms showcasing impact of altering $t_{\mathrm{int,on}}$

C. High Power Experiments

An exemplary full series of $t_{\mathrm{int,on}}$ values and a single $v_{\mathrm{int,on}}$ value were used for the experiments. The experiment parameters are summarized in Table II.

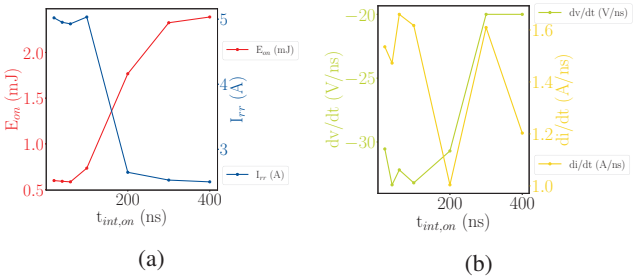
The experiments were performed at a load current of 20 A, a load inductance of 100 µH, a DC-link bus voltage of 800 V, and an external gate resistance of 25 Ω. Time domain measurements are presented in Fig. 9. The performance parameters presented in Fig. 10 are the same as those highlighted in Section III and were defined and calculated in the same way.

Figs. 8, 9 and 10 prove the ability of the proposed AGD to impact the turn-on switching transient of the DUT. The proposed AGD prototype operates as expected.

Increasing the duration of $t_{\mathrm{int,on}}$ has a clear impact on v_{GS} and i_{D}. Especially for higher values of $\mathrm{t}_{int,on}$ (300 ns and 400 ns), the proposed AGD significantly reduces voltage and current slopes.

D. Experiment and Simulation Results Comparison

Comparing Figs. 6 and 9, some differences become clear. In simulations (Fig. 6), the intermediate voltage level at $v_{\mathrm{int,on}} = 7.5\,\mathrm{V}$ has a purely delaying effect on the voltage commutation, dv/dt remains constant in good approximation. Meanwhile, in experiments (Fig. 9), v_{DS} has a delaying effect on the voltage commutation for small values of $\mathrm{t}_{int,on}$, but



(a) (b)

Fig. 10: Experimental MOSFET switching performance parameters

also reduces dv/dt for higher values of $t_{int,on}$. The drain current, i_D is relatively similar in Figs. 6 and 9 except from excessive oscillations in the experimental results and a higher I_{rr} in the simulations. This is caused by differences between the simplified circuit model and the real circuit, as well as the SPICE MOSFET and and switching device. The circuit parasitics are reduced to a single power loop inductance for the simulation, whereas in reality, multiple parasitic inductances and capacitances are distributed throughout the circuit and interact with each other. Previous work has shown that among other aspects, especially the quasi-saturation and saturation regions are not well represented in manufacturer SPICE models [20]. Simulated saturation currents are therefore lower than what can be found in experiments. This can explain the deviation between simulation and experiment.

V. Conclusion

This paper presents an active variable four-level voltage gate driver for SiC MOSFETs. Intermediate voltage pulses that are configurable in amplitude and duration, can be applied to the gate during switching and thereby control the switching transients. An extensive simulation study has demonstrated the potential of the proposed gate driver to decouple voltage and current slopes (dv/dt and di/dt) and the switching losses (E_{on} and E_{off}) to a certain degree, if the control variables ($v_{int,on}$, $v_{int,off}$, $t_{int,on}$ and $t_{int,off}$) are chosen accordingly.

A prototype of the proposed gate driver has been built and tested on a Wolfspeed C3M0075120D Silicon Carbide Power MOSFET. Sample measurements have been presented in this paper. Both simulation and experimental results show that the AGD is able to control E_{on}, I_{rr}, dv/dt and di/dt in the DUT during switching.

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