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An Adaptive Current-Source Gate Driver for High-Voltage SiC MOSFETs

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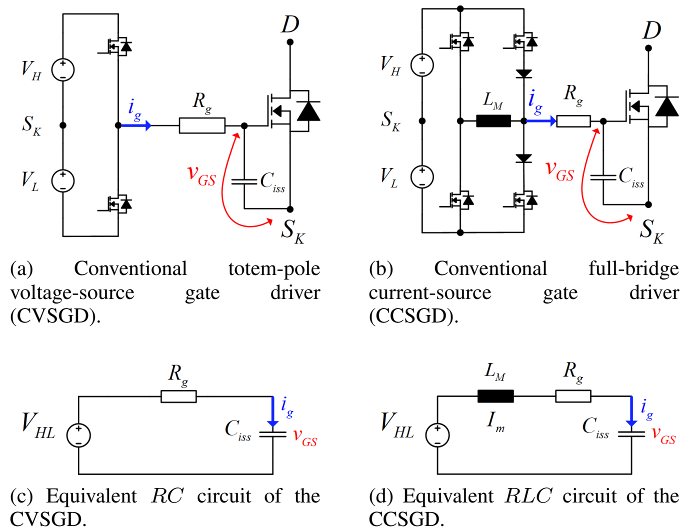
***Abstract*—This paper presents a novel current-source gate driver for Silicon Carbide (SiC) metal oxide semiconductor field-effect transistors (MOSFETs) with adaptive functionalities. The proposed driver aims to decouple and improve controllability of di/dt, dv/dt, as well as to decrease turn-on and turn-off delay times compared to conventional totem-pole voltage-source gate drivers and conventional current-source gate drivers. The circuit topology of the proposed gate driver and the working principle are analysed for the turn-on and turn-off processes. Furthermore, the driving requirements in terms of gate voltage and gate current for SiC MOSFETs that determine the design and tuning of gate drivers are presented. The performance of the proposed gate driver is validated experimentally on a 3.3 kV/750 A SiC MOSFET half-bridge power module. It is shown that, compared to conventional voltage-source gate drivers, the driver is capable of significantly reducing turn-on and turn-off delay times by approximately 57% and 33%, respectively. Moreover, the proposed gate driver enables 233% controllability of di/dt and 87% of dv/dt.**

***Index Terms*—Gate drivers, SiC MOSFETs adaptive driving.**



(a) Conventional totem-pole voltage-source gate driver (CVSGD).

(b) Conventional full-bridge current-source gate driver (CCSGD).

(c) Equivalent RC circuit of the CVSGD.

(d) Equivalent RLC circuit of the CCSGD.

Fig. 1: Circuit schematics and equivalent circuits of CVSGD and CCSGD.

I. INTRODUCTION

SILICON Carbide (SiC) metal oxide semiconductor field-effect transistors (MOSFETs) exhibit several advantages in high-voltage and high-power applications, due to the lower power losses and faster switching transients, higher blocking voltage, and higher maximum operating temperatures, compared to Silicon-based counterparts [1]. SiC MOSFETs allow for improved electrical and thermal performance of power converters for medium-voltage direct current (MVDC) and [2]–[4], high-voltage DC (HVDC) grids [5], [6], as well as, MV drives [7]–[9]. With significant trends leading towards increasing switching speeds in power electronic applications, very short rise and fall times during switching transients are desirable to reduce the anticipated hard-switching losses. The key to reach very fast switching transients is to utilise powerful gate drivers. Gate driver topologies are classified as voltage-source gate drivers (VSGD) and current-source gate drivers (CSGD). The conventional totem-pole VSGD (CVSGD) and the conventional full-bridge CSGD (CCSGD) are shown in Fig. 1a and Fig. 1b with their equivalent RLC circuits shown in Fig. 1c and Fig. 1d. For the CVSGD, the driving energy is provided by the electric field in the driver DC-link with $V_{HL} = V_H + V_L$. For the CCSGD, the driving energy is provided by the magnetic field in the driver inductor L_M, which prior to the turn-on and turn-off instants is charged to I_m by applying V_{HL}.

The CVSGD utilise a totem-pole circuit and gate resistors for controlling the gate current. However, they pose limitations in switching speeds as the gate current is reduced with reducing voltage difference between the driving voltage source and gate-source voltage. On the other hand, CSGD seem to be more promising compared to CVSGD. In particular, CSGD can provide a more constant gate current during switching transients and hold the ability to variate the initial turn-on and turn-off gate currents, hence enabling adjustable switching speeds.

Current-source gate drivers can be designed either as inductor-less – typically current-mirror based – drivers [10]–[12] or inductor-based – typically continuous-current and discontinuous-current mode gate drivers [13], [14]. Inductor-based CSGD, i.e. gate drivers utilizing inductor in the driver circuit as an energy-storage component, have been widely presented in literature for power semiconductor switches [14]–[31]. Common gate driver circuit topologies ranges from half-bridge [20], [21], [25], [29] variations to full-bridge [14], [16]–[19], [22], [24], [26], [31], [32] variations, with other topologies using four- [27] and two- [28] switch circuits with coupled inductors. CSGD are capable of supplying a more constant gate current compared to CVSGD drivers, providing charge to the gate at a higher rate, hence increasing the semiconductor switching speed. The peak gate-drive current is

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configurable by adjusting the driver pre-charge current level of L_M, hence the overall switching speed is adaptive. However, none of these drivers has the ability to inject (i.e., during turn-on) or sink (i.e., during turn-off) a second current peak to the gate, and thus limiting their ability to independently control the device's di/dt and dv/dt. Aside from increased switching speed compared to CVSGD, the existing driver concepts in literature are thus limited to adaptively adjust the overall switching speed, that is di/dt and dv/dt *together*, rather than *independently*.

The proposed adaptive current source gate driver (ACSGD) aims to independently control the turn-on and turn-off voltage and current rise and fall rates, di/dt and dv/dt by supplying two separate gate current peaks. Besides, the proposed ACSGD is capable of adaptively adjusting the turn-on and turn-off delay times of the devices. The controllability of turn-on and turn-off delay times enable accurate dead-time control, and can significantly reduce dead-time requirements which may have impact on power electronic systems such as the dual active bridge (DAB) converter [33]. The adjustable di/dt and dv/dt allows for control of electromagnetic emissions, introducing electromagnetic compatibility (EMC) flexibility and reduced converter filter size. The di/dt and dv/dt control can limit both drain-current and drain-source voltage overshoots, allowing converter switches to operate closer to its maximum safe operating area (SOA), and hence facilitating a more optimal converter design. The controllable di/dt and dv/dt enable accurate switching loss manipulation. The driver can significantly reduce device switching losses compared to CCSGD and CVSGD or control di/dt and dv/dt for active thermal control (ATC) purposes, improving reliability and lifetime of power electronic converters [34].

The paper is organized as follows. Section II gives an overview of gate driver design considerations for SiC MOSFETs. Section III introduces the proposed adaptive current source gate driver, its circuit topology, working principles and mathematical analysis, while Section IV presents experimental validation of the proposed driver with comparisons to CVSGD. System-level benefits using the proposed ACSGD are discussed in V. Lastly, conclusions are shown in Section VI.

II. Gate Driver Design Considerations for SiC MOSFETs

Driving SiC MOSFETs, (i.e. turning the MOSFET on and off), is in essence the process of manipulating charge in the physical structure of the device. For turn-on, the goal is to move sufficient charge from the the driver energy buffer (i.e., V_{HL}) to the gate in order to create an inversion layer between source and drain such that current may flow. For turn-off, the opposite process applies, where the gate charge is removed such that the inversion layer collapses and current can no longer flow through the MOSFET's channel. The movement of the gate charge can be captured by considering the equivalent device capacitances, that is the input capacitance $C_{iss} = C_{gs} + C_{gd}$, the output capacitance $C_{oss} = C_{ds} + C_{gd}$ and reverse transfer capacitance $C_{rss} = C_{gd}$, as illustrated in

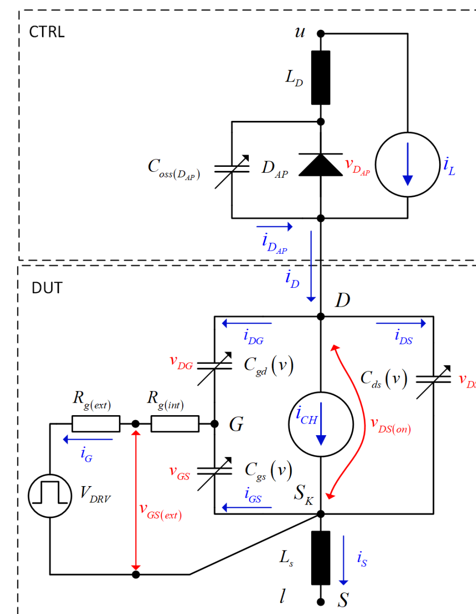

Fig. 2: Equivalent SiC MOSFET circuit during switching transients.

Fig. 2. These capacitances are integral to the evolution of the gate-source voltage, v_{GS}, drain current, i_D and drain-source voltage, v_{DS}. Accurate models of SiC MOSFET transient evolution of v_{GS}, i_D and v_{DS} and the significance of the equivalent device capacitances have been analysed in literature [35]–[38].

The gate-drain capacitance C_{gd} is dependent on v_{DS} and v_{GS} [39], as seen in Fig. 3, thus the input capacitance C_{iss} depends on both v_{GS} and v_{DS}. The gate-drain capacitance $C_{gd}(v_{DS}, v_{GS})$ of the device under test (DUT) Mitsubishi FMF750DC-66A SiC MOSFET half-bridge power module (3.3 kV/750 A) used in this paper was measured using the Keysight B1505A Power Device Analyzer and it is shown in Fig. 3a, while C_{gd}, C_{gs} and C_{iss} v_{GS} dependencies are shown in Fig. 3b. Their dependency on both v_{GS} and v_{DS} is clear, hence, the values of both v_{GS} and v_{DS} at the switching instant determine the response of v_{GS} and consequently constrain the driver design and operating parameters. The evolution of v_{GS} is impacted by the transients of i_D and v_{DS}, however, the impact of v_{DS} on the gate charge is minimal for high-voltage SiC MOSFETs due to the generally lower value of C_{oss} compared to C_{iss}. The total SiC MOSFET gate charge Q_g, that is the total amount of charge to be moved to and from the gate to charge v_{GS} from V_L to V_H and vice versa during switching transients, is given by

$$Q_g = \int C_{iss}(v)dV \tag{1}$$

The gate charge of the DUT is measured for low values of i_D ($i_D < 10mA$) using the Keysight B1505A Power Device Analyzer and visualised in Fig. 4a. The impact of v_{DS} on Q_g is low, as the gate charge difference $\Delta Q_{g(f)} = Q_{g(f_2)} - Q_{g(f_1)}$ between the required gate charge $Q_{g(f_1)}$ at $v_{DS} \approx 1V$ and the required gate charge $Q_{g(f_2)}$ at $v_{DS} \approx 1000V$ being 3.5% of

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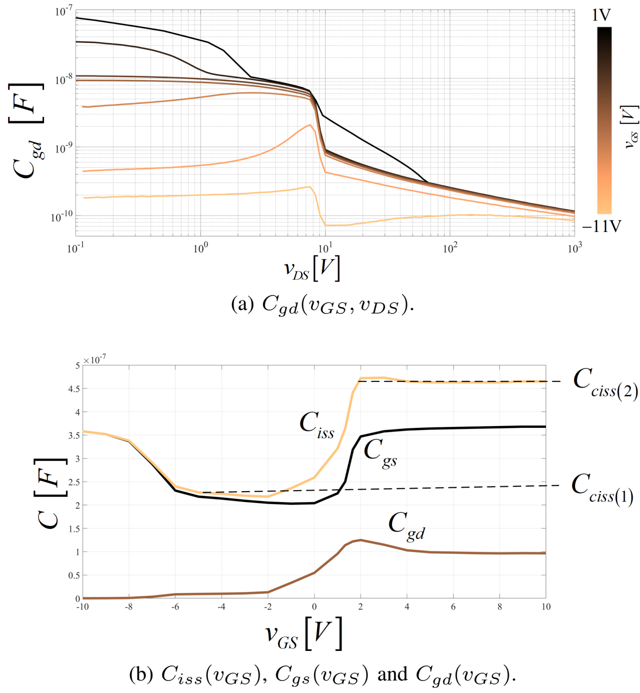
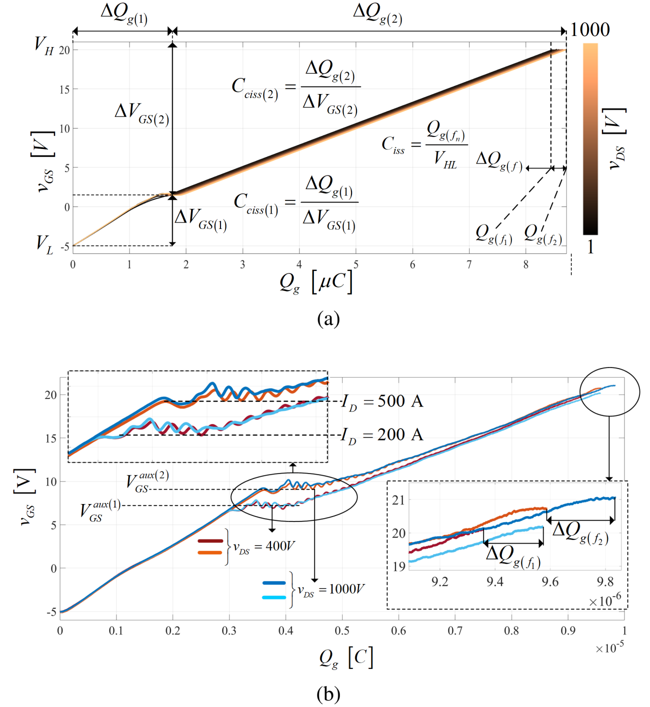


(a) $C_{gd}(v_{GS}, v_{DS})$.

(b) $C_{iss}(v_{GS})$, $C_{gs}(v_{GS})$ and $C_{gd}(v_{GS})$.

Fig. 3: Measured device capacitances of the Mitsubishi FMF750DC-66A SiC MOSFET half-bridge power module used as DUT.



(a)

(b)

Fig. 4: (a) $Q_g(v_{GS})$ measurements of device gate charge using the power device analyzer at low i_D of the Mitsubishi FMF750DC-66A SiC MOSFET half-bridge power module used as DUT and (b) $Q_g(v_{GS})$ measurements of DUT device gate charge using double pulse test with varying load values I_D and blocking voltages V_{DS}.

$Q_{g(f_2)}$. The resulting average capacitance

$$C_{iss} = \frac{\Delta Q_g}{\Delta v_{GS}} = \frac{Q_{g(f_n)}}{V_{HL}} \tag{2}$$

at $v_{DS} \approx 1V$ is $C_{iss(f_1)} \approx 336nF$ and at $v_{DS} \approx 1000V$ is $C_{iss(f_2)} = 348nF$. To visualise the impact of varying values of i_D on Q_g, Q_g is measured during double-pulse testing of the DUT as seen in Fig. 4b. With the i_D dependency on v_{GS} in the saturation region, a higher value of v_{GS} is required to obtain a higher value of i_D. The red (light and dark) measurements are performed at $400V$, while the blue (light and dark) measurements are performed at $1000V$. Two drain current I_D values (i.e. the value of i_D determined by the double-pulse duration) are compared. The value of v_{DS} impacts Q_g primarily after the Miller region (after v_{DS} rise and fall, as C_{oss} is being charged and discharged) as seen from the zoomed-in areas in Fig. 4b. Hence, gate driver design procedures can be assumed independent on v_{DS} with good accuracy, and the capacitance value for $v_{DS} \approx 1V$ is used during design process to keep a safety margin for v_{GS} overshoot and consequently possible gate oxide destruction. The drain current load value I_D is more critical for determining the Miller region ($V_{GS}^{aux(n)}(I_D)$) used for the *variable* dv/dt operation (see section IV-C) than the value of the blocking voltage V_{DS}.

A. Voltage and Current Source Gate Drivers

CVSGD are limited in providing fast driving capabilities due to the total gate resistance consisting of an internal, $R_{g(int)}$, and an external, $R_{g(ext)}$, resistive component $R_g = R_{g(int)} + R_{g(ext)}$, and the maximum allowed upper V_H and lower V_L drive voltage limit of V_{DRV} (Fig. 2). Most of the discrete SiC MOSFETs and SiC MOSFET power modules have a fixed $R_{g(int)}$ incorporated by the manufacturers. Moreover, the gates can only withstand certain maximum and minimum voltage stress values $\left(V_{GS}^{max}/V_{GS}^{min}\right)$, which eventually limit the maximum utilised V_H and V_L values. Considering these limitations, the CVSGD driver current is limited to

$$i_g = \frac{(V_{HL} - v_{GS})}{R_g} = \frac{V_{HL}}{R_g} e^{-t/\tau_{iss}} \tag{3}$$

with $\tau_{iss} = R_g C_{iss}$. The time duration $T_{V(1)}$ of which a CVSGD can move the arbitrarly amount of charge $Q_{g(1)}$ is given by

$$T_{V(1)} = -\tau_{iss} \ln\left(\frac{Q_{g(1)}}{\underbrace{C_{iss} V_{HL}}_{Q_{g(f_n)}}}\right) \tag{4}$$

and the switching speed obtainable by CVSGD is thus theoretically limited by R_g for maximum values of V_{HL} set by manufacturer limits $\left(V_{GS}^{max}/V_{GS}^{min}\right)$.

In case of CCSGD, the additional energy storing element, L_M, yields significant benefits in terms of switching speed flexibility. Considering the equivalent RLC circuit of the CCSGD given in Fig. 1d, the differential equation describing the evolution of v_{GS} is given by

$$\frac{d^2 v_{GS}}{dt^2} + \frac{R_g}{L_M} \frac{dv_{GS}}{dt} + \frac{v_{GS}}{C_{iss} L_M} = \frac{V_{HL}}{C_{iss} L_M} \tag{5}$$

Equation "(5)" is written in the Laplace domain as

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$$v_{GS}(s)\underbrace{\left(s^2+2\alpha_s s+\omega_{0_s}^2\right)}_{d(s)}=$$
$$\underbrace{\frac{V_H\omega_{0_s}^2}{s}+sV_L+\frac{I_m}{C_{iss}}+\frac{R_g}{L_M}V_L}_{n(s)} \tag{6}$$
$$\alpha_s=\frac{R_g}{2L_M},\ \omega_{0_s}^2=\frac{1}{C_{iss}L_M}$$

To obtain the fastest response of v_{GS} without oscillatory behaviour, v_{GS} should have a critically damped response, requiring a damping $\zeta_s=\alpha_s/\omega_{0_s}=1$. For a given C_{iss} and R_g, L_M should then be chosen as

$$L_M=C_{iss}\left(\frac{R_g}{2}\right)^2 \tag{7}$$

to preserve a damping of 1. For a critically damped response, v_{GS} have a single pole $s_s=-\alpha_s$, with its time-domain response described by

$$v_{GS}(t)=V_H+\underbrace{e^{-\alpha_s t}}_{e(t)}\cdot\underbrace{(k_{s_1}^v t+k_{s_2}^v)}_{l(t)}$$
$$k_{s_1}^v=\frac{I_m}{C_{iss}}+\alpha_s k_{s_2}^v,\ k_{s_2}^v=-V_{HL} \tag{8}$$

and the gate current i_g given by

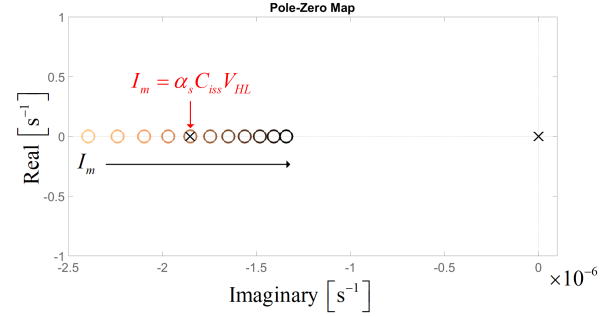
$$i_g(t)=C_{iss}\frac{dv_{GS}}{dt}=C_{iss}e^{-\alpha_s t}\cdot(k_{s_1}^i t+k_{s_2}^i)$$
$$k_{s_1}^i=-\alpha_s k_{s_1}^v,\ k_{s_2}^i=k_{s_1}^v-\alpha_s k_{s_2}^v \tag{9}$$

For a set of chosen values of R_g and L_M, the response of v_{GS} is determined by the charged value of I_m. Even though the response of v_{GS} is critically damped, the response may still exhibit an overshoot depending on the value of I_m. For a certain value of $I_m=I_m^{os}$, the zeroes of $v_{GS}(s)=n(s)/d(s)$ traverse into the dominant pole region of $v_{GS}(s)$ as seen in Fig. 5a, which will lead v_{GS} to be susceptible to overshoot as seen in Fig. 5b/5c. The point of which $I_m=I_m^{os}$ equates to the point of which the slope of $l(t)$ in "(8)" becomes positive, changing sign once for $t>0$. With the decaying term $e(t)$ being positive for $t>0$, $l(t)$ might push v_{GS} above V_H. A lower boundary for which an overshoot will not happen is thus given by

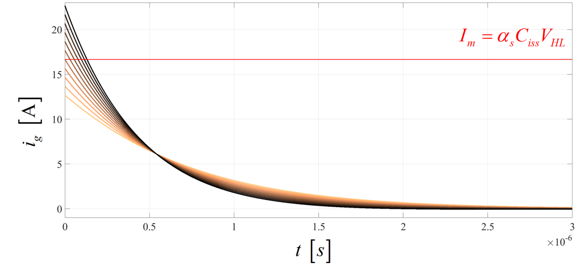
$$k_{s_1}\leq 0\rightarrow I_m\leq I_m^{os}=\alpha_s C_{iss}V_{HL}=\frac{R_g}{2L_M}C_{iss}V_{HL} \tag{10}$$

hence the peak pre-charge value I_m of i_m should not exceed I_m^{os}.

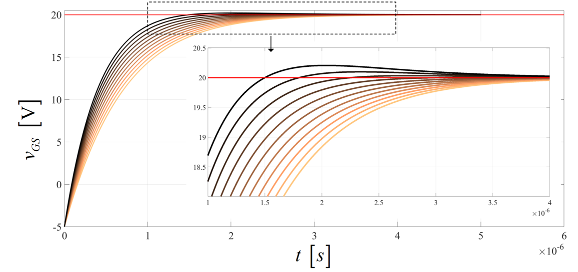
A comparison of v_{GS} rise times T_r between CVSGD and CCSGD for v_{GS} traversing from V_L to the voltage level V_{GS}^r with circuit values given in Table I are shown in Fig. 6. The CCSGD is capable of obtaining flexible T_r by adjusting I_m, while the T_r of CVSGD is constant at a certain value of R_g, hence T_r directly determined by R_g. As seen from Fig. 6, for $I_m>I_m^{os}$, the CCSGD enters the overshoot region (OSR) marked by blue circles and dotted lines in Fig. 6.



(a) Pole-zero map of $v_{GS}(s)$.



(b) Gate current, i_g, response for varying values of I_m.



(c) Gate-source voltage, v_{GS}, response for varying values of I_m.

Fig. 5

The maximum energy dissipation of the gate drivers is given by

$$E_D=\int_0^\infty R_g i_g^2 dt \tag{11}$$

The energy dissipation of the CVSGD is constant and given by

$$E_D^V=0.5C_{iss}V_{HL}^2 \tag{12}$$

with "(3)" used in "(11)". The energy dissipation of the CCSGD depends on the value of I_m as given in "(9)". Similarly, by using "(9)" in "(11)" with the condition $I_m=I_m^{os}$ yielding $k_{s_1}^1=0$ and $\alpha_s=2/(R_gC_{iss})$ for $\zeta_s=1$, the energy dissipation of the CCSGD is given by

$$E_D^{C(max)}=\frac{\alpha_s R_g(V_{HL}C_{iss})^2}{2}=C_{iss}V_{HL}^2=2E_D^V \tag{13}$$

Therefore, obtaining the maximum v_{GS} rise-time confined by "(10)" using the CCSGD, results in twice the energy dissipation compared to the CVSGD. For I_m values greater than the points marked by red circles in Fig. 6, yields lower

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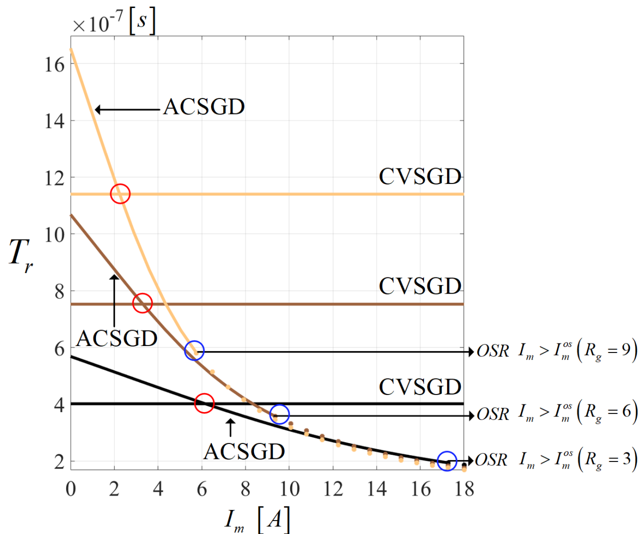

Fig. 6: Rise-time values, T_r, comparison between the CVSGD and CCSGD. Beyond the red line, v_{GS} goes into the overshoot region (OSR), causing v_{GS} to exceed V_H.

TABLE I: Circuit Parameters for Rise-time Estimation

$V_L[V]$	$V_{GS}^r[V]$	$C_{iss}[nF]$	$R_g[\Omega]$	$[I_m^{\min}, I_m^{\max}][A]$
-5	$V_{GS}^{aux(2)} = 9$	350	$[3, 6, 9]$	$[0, 18]$

T_r values of v_{GS} for CCSGD than CVSGD and, thus, results in faster switching time for CCSGD than CVSGD, albeit at the cost of higher gate driver energy consumption.

III. Proposed Adaptive Current-source Gate Driver

Fig. 7 shows the circuit schematic of the proposed ACSGD with typical driver waveforms for a double current injection operation mode shown in Fig. 8. The driver expands the CCSGD circuit capabilities by adding two additional energy storing inductors, L_H and L_L, and an auxiliary circuit branch controlled by Q_{aux}, allowing for a second gate current injection and sinking. The driver specifically exhibits three main characteristics as follows:

- Variable di_D/dt and dv_{DS}/dt by varying I_m.
- Independent control of di_D/dt and dv_{DS}/dt by varying the peak value I_{aux} of the auxiliary current and timing of i_{aux} injection or sinking.
- Reduction of the turn-on and turn-off delay times by pre-charging or pre-discharging v_{GS} prior to the switching instant.

The working principle of the ACSGD is analysed in the following subsections. The turn-on procedure is described in Sections III-A–III-D, while the turn-off procedure is described in III-E–III-H.

A. Turn-on Pre-charge Interval

The turn-on pre-charge interval is initiated at t_0 by turning Q_1 and Q_4 on as illustrated in Fig. 9a. During this interval the

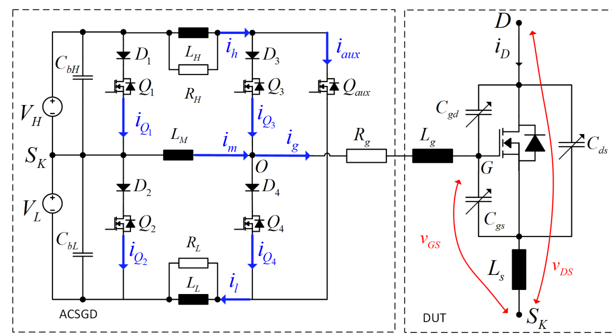

Fig. 7: Circuit schematic of the proposed adaptive current source gate driver.

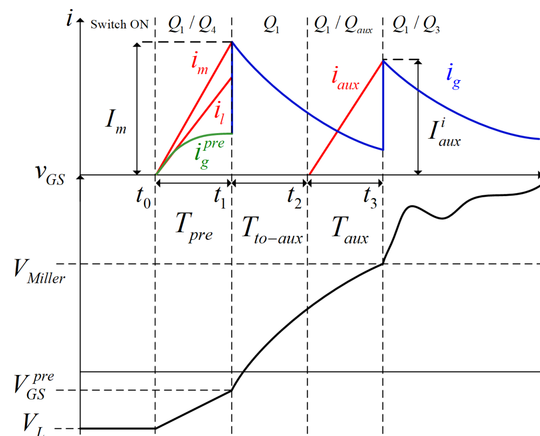

Fig. 8: Illustrative driver current and voltage waveforms during turn-on.

inductor L_M is charged to a pre-defined value I_m as illustrated in Fig. 9b. The interval causes a current, i_g^{pre}, to flow into the gate prior to the turn-on instant that is initiated at t_1 due to the current divider imposed by Z_L and Z_S. The pre-charge current i_g^{pre} charges the gate-source junction by increasing v_{GS} to the pre-charge value V_{GS}^{pre}. Pre-charging v_{GS} enables shorter turn-on delay times in half-bridge circuits, and thus, impacting the choice of dead-time intervals. In particular, decreasing the turn-on delay time, necessitates a shorter dead-time and, hence, higher switching frequencies can be utilised.

The evolution of v_{GS} during the pre-charge interval can be described by considering the equivalent RLC circuit shown in Fig. 9c. The discharge resistor R_l is used to provide a current path for the current i_l flowing in the lower L_L-branch when turning Q_4 off, and is chosen high enough so that it has negligible impact on i_l during the pre-charge interval. Using Kirchhoff's voltage law (KVL) on Fig. 9c yields the equations

$$V_H + V_L = L_M \frac{di_m}{dt} + L_L \frac{di_l}{dt} \tag{14}$$

and

$$L_L \frac{di_l}{dt} = i_g R_g + v_{GS} + V_L \tag{15}$$

of which the following differential equation for v_{GS}

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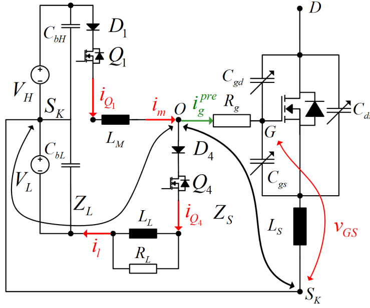
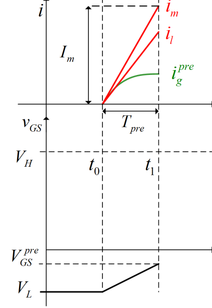
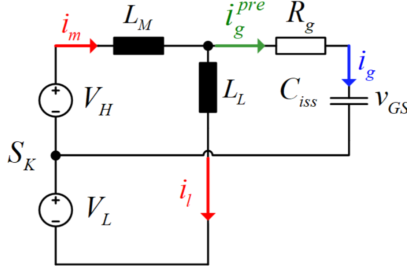


(a) Equivalent circuit during turn-on pre-charge interval.



(b) Illustrative waveforms during turn-on pre-charge interval.



(c) Equivalent RLC circuit during turn-on pre-charge interval.

Fig. 9: Pre-charge interval.

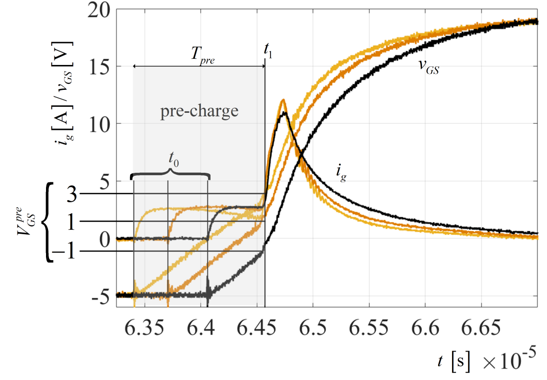


Fig. 10: Gate-source voltage, v_{GS}, and gate current, i_g, responses to varying pre-charge interval lengths T_{pre} for $L_M = L_H = L_L = 700nH$, $R_{g(ext)} = 1.5\Omega$ and $C_{iss} = 200nF$.

$$\frac{d^2 v_{GS}}{dt^2} + R_g\left(\frac{L_M + L_L}{L_M L_L}\right)\frac{dv_{GS}}{dt} + \left(\frac{L_M + L_L}{C_{iss(1)} L_M L_L}\right) v_{GS} = \frac{V_H L_L - V_L L_M}{C_{iss(1)} L_M L_L} \tag{16}$$

can be derived, with the characteristic equation written as

$$s^2 + 2\alpha_p s + \omega_{0_p}^2 = 0$$
$$\alpha_p = R_g\left(\frac{L_M + L_L}{2 L_M L_L}\right),\ \omega_{0_p}^2 = \left(\frac{L_M + L_L}{C_{iss(1)} L_M L_L}\right) \tag{17}$$

Since the pre-charge interval starts from $v_{GS} = V_L$, the input capacitance value is $C_{iss} = C_{iss(1)}$ (Fig. 3b). The solution of "(17)" is obtained for the over-damped and under-damped cases as

$$v_{GS} = \begin{cases} k_{p_1}^v e^{(s_{p_1} t)} + k_{p_2}^v e^{(s_{p_2} t)} + V_P, & \zeta_p > 1 \\ e^{-\alpha_p t}(k_{p_3}^v \cos(w_{d_p} t) + k_{p_4}^v \sin(w_{d_p} t) + V_P, & \zeta_p < 1 \end{cases} \tag{18}$$

where the damping ζ_p is $\zeta_p = \alpha_p / \omega_{0_p}$, V_P is the Thévenin voltage of the equivalent circuit (Fig. 9c) given by

$$V_P = \frac{V_H L_L - V_L L_M}{L_M + L_L} \tag{19}$$

and the poles $s_{1,2}$ given by

$$s_{1,2} = -\alpha_p \pm \sqrt{\alpha_p^2 - \omega_{0_p}^2} \tag{20}$$

The current i_m charging the inductor L_M is found by solving

$$i_m = \int \frac{V_{HL}}{L_M + L_L} dt + D + \frac{C_{iss(1)} L_L}{L_M + L_L}\frac{dv_{GS}}{dt} \tag{21}$$

D being the integration constant. For the over-damped case with the pre-charge interval time duration T_{pre}, the solution to "(21)" is

$$i_m = T_{pre}\frac{V_{HL}}{L_M + L_L} + \frac{C_{iss(1)} L_L}{L_M + L_L} \cdot \ldots \left(k_{p_0}^i + k_{p_1}^i e^{(s_{p_1} t)} + k_{p_2}^i e^{(s_{p_2} t)}\right),\ \zeta_p > 1 \tag{22}$$

and the under-damped case

$$i_m = T_{pre}\frac{V_{HL}}{L_M + L_L} + \frac{C_{iss(1)} L_L}{L_M + L_L} e^{(-\alpha_p t)} \cdot \ldots \left(k_{p_3}^i \cos(\omega_{d_p} t) + k_{p_3}^i \sin(\omega_{d_p} t)\right),\ \zeta_p < 1 \tag{23}$$

with the damped oscillation frequency ω_{d_p} given by

$$\omega_{d_p} = \sqrt{\omega_{0_p}^2 - \alpha_p^2} \tag{24}$$

The values of $k_{p_n}^v$ and $k_{p_n}^i$ are given in Table II. By adjusting I_m within the interval $[0, I_m^{os}]$, the overall switching speed of the device under test (DUT) can be controlled. For a set of designed driver parameters L_M, L_H, L_L, R_g and C_{iss}, varying T_{pre} results in varying values of V_{GS}^{pre} and I_m. This is shown in Fig. 10, where T_{pre} is varied for the driver parameters $L_M = L_H = L_L = 700nH$, $R_{g(ext)} = 1.5\Omega$ using a passive load at $C_{iss} = 200nF$. The T_{pre} length should thus not be chosen too long as to charge v_{GS} to a value exceeding the threshold voltage V_{th} (i.e. $V_{GS}^{pre} \leq V_{th}$) to avoid premature turn-on.

B. Turn-on

The turn-on process is initiated at the time instant t_1 by turning Q_4 off while keeping Q_1 on, injecting the current i_m charged with an amplitude I_m during the pre-charge interval, into the gate, yielding $i_g = i_m$ as shown in Fig. 11. The

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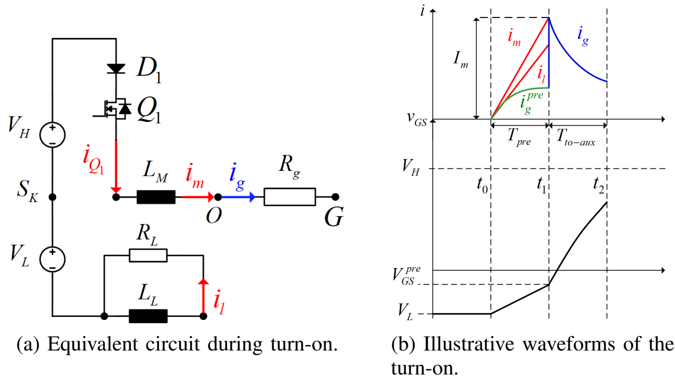
TABLE II: Pre-charge Interval Coefficient Expressions

k^v_{p1}	k^v_{p2}	k^v_{p3}	k^v_{p4}	k^i_{p0}	k^i_{p1}	k^i_{p2}	k^i_{p3}	k^i_{p4}
$s_2\frac{(V_L+V_P)}{s_1-s_2}$	$k^v_{p1}+V_L+V_P$	$-(V_L+V_P)$	$k^v_{p3}\frac{\alpha_p}{\omega_{dp}}$	$-(k^v_{p1}s_1+k^v_{p2}s_2)$	$s_1k^v_{p1}$	$s_2k^v_{p2}$	$(k^v_{p4}\omega_{d_p}-\alpha_pk^v_{p3})$	-$(k^v_{p4}\omega_{d_p}+\alpha_pk^v_{p3})$



(a) Equivalent circuit during turn-on. (b) Illustrative waveforms of the turn-on.

Fig. 11: First turn-on.

resulting equivalent circuit can be defined by the equivalent RLC circuit of Fig. 1d, hence the analysis described in Section II-A is also applicable for this interval with $V_L = V_{GS}^{pre}$ and $C_{iss} = C_{iss(2)}$. The value of I_m should thus not exceed

$$I_m \leq \alpha_s C_{iss}\left(V_H + |V_{GS}^{pre}|\right) \tag{25}$$

to avoid an overshoot in v_{GS} (Fig. 5). The value of I_m together with the driver design parameters determines the overall switching speed of the DUT.

C. Turn-on Auxiliary Charge Interval

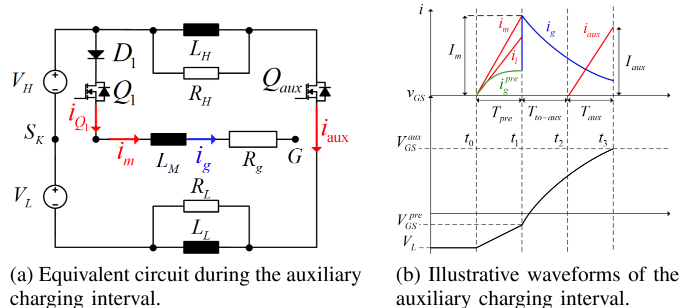
At the time instant t_2 after turn-on, the auxiliary charging interval is initiated. During this time interval the inductors L_H and L_L are charged with i_{aux} by turning Q_{aux} on while keeping Q_1 on as illustrated in Fig. 12. Again, it is assumed that the discharge resistors R_h and R_l have sufficiently high values, so their impact on i_{aux} is negligible. Thus, the amplitude of i_{aux} is calculated as

$$I_{aux} = T_{aux}\frac{V_{HL}}{(L_H + L_L)} \tag{26}$$

D. Auxiliary Turn-on

The working principle of the auxiliary turn-on is dependent on whether a current injection or a current sinking is desired at the auxiliary turn-on instant t_3.

1) Auxiliary Injection: At the time instant t_3 after the charging of i_{aux} has reached its desired amplitude I_{aux}^i, i_{aux} is injected into the gate G as $i_g = i_m + i_{aux}$, as illustrated in Fig. 13a, yielding the waveforms shown in Fig. 13c.



(a) Equivalent circuit during the auxiliary charging interval. (b) Illustrative waveforms of the auxiliary charging interval.

Fig. 12: Auxiliary charge interval.

2) Auxiliary Sinking: If sinking of i_g is desired at the second turn-on, the auxiliary current i_{aux} is charged to the value I_{aux}^s which should be lower than the gate current i_g at the time instant t_3. For this case, Q_1 should be turned off while Q_2 is turned on, to commutate i_m away from the gate G, as illustrated in Fig. 13b. After a short time period after Q_1 is turned off and Q_2 is turned on, the desired i_{aux} is sank from the gate as $i_g = i_{aux}$ by turning Q_3 on while turning Q_2 off, yielding the waveforms shown in Fig. 13c.

Injecting or sinking the auxiliary current at a specified time instant t_3 allows for control of either di/dt or dv/dt. For turn-on, setting t_3 before the Miller plateau (i.e., during i_D rise) allows for control of di/dt, while setting t_3 to the Miller plateau (i.e., during v_{DS} fall) allows for control of dv/dt. Similarly, at turn-off, setting t_3 at the Miller plateau before i_D fall allows for control of dv/dt, while setting t_3 after the v_{DS} rise allows for control of di/dt.

Determining the time instant t_3 can be done by estimating the time duration for v_{GS} to reach a certain voltage level, V_{GS}^{aux}. The time duration T_{aux-on} determining t_3 can be approximated by solving "(8)" numerically

$$f(t) = v_{GS}(t) - V_{GS}^{aux} = 0 \rightarrow T_{aux-on} \approx f^{-1} \tag{27}$$

The value of V_{GS}^{aux} depends on the operating mode of the driver. If manipulation of di/dt is desired at a specified drain current value I_D, V_{GS}^{aux} can be determined by solving the device drain current i_D saturation region transfer characteristics [39]

$$i_D \approx g_s(v_{GS} - V_{th})^x(1 + \lambda v_{DS}) \rightarrow \\ V_{GS}^{aux} = \sqrt[x]{\frac{I_D}{g_s\,(1 + \lambda v_{DS})}} \tag{28}$$

where g_s is the MOSFET transconductance, x is a fitting parameter to be adjusted to the specific device used and λ is the channel modulation index, with the value of v_{DS} being the device's blocking voltage. If manipulation of dv/dt is desired, V_{GS}^{aux} corresponds to the Miller plateau voltage, i.e., the value

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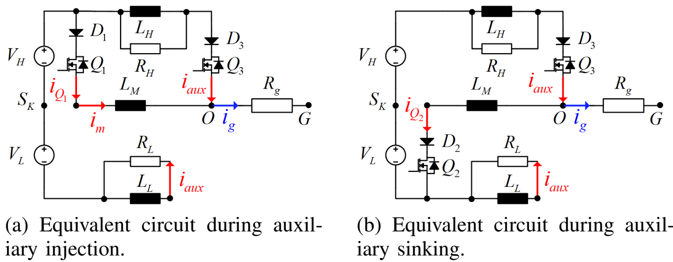
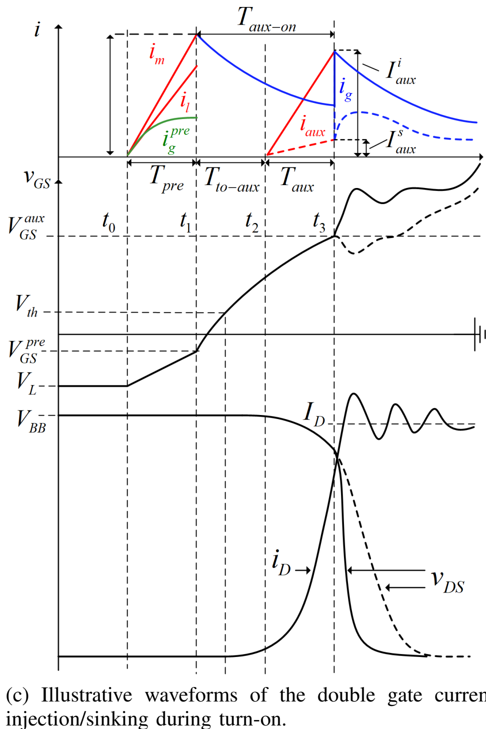


(a) Equivalent circuit during auxiliary injection.

(b) Equivalent circuit during auxiliary sinking.



(c) Illustrative waveforms of the double gate current injection/sinking during turn-on.

Fig. 13: Turn-on transition showing the impact of injecting (solid line) and sinking (dashed line) auxiliary gate current.

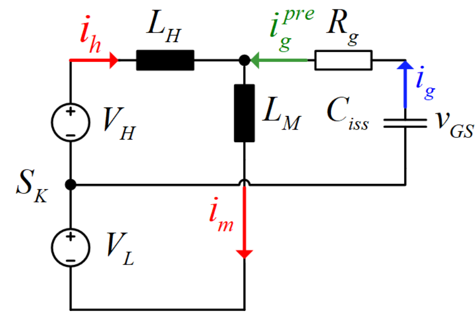


Fig. 14: Equivalent RLC circuit during turn-on pre-charge interval

TABLE III: Double Pulse Test Circuit Parameters

L_D	L_S	L_{up}	L_{low}	L_{LOAD}	C_f	C_{DS}
$7nH$	$7nH$	$20nH$	$20nH$	$80\mu H$	$10\mu F$	$800\mu F$

of v_{GS} during the v_{DS} fall-time. This value can similarly be determined with "(28)" by setting the drain-current value I_D equal to the system's load current.

The value of V_{GS}^{aux} can also be determined by using the $Q_g(v_{GS})$ measurements as seen in Fig. 4b. These measurements yields highly accurate values of V_{GS}^{aux} at a given load current value, I_D, and drain-source blocking voltage, V_{DS}. The $Q_g(v_{GS})$ can be obtained experimentally (e.g. through DPT) as seen in Fig. 4b) or by using a Power Device Analyser $Q_g(v_{GS})$ measurement method for both high V_{DS} and high I_D operation [40].

E. Turn-off Pre-charge Interval

The turn-off pre-charge interval is initiated by turning Q_2 and Q_3 on, charging the inductor L_M to the value I_m as illustrated in Fig. 15a. Similarly to the turn-on pre-charge interval, the equivalent current divider caused by the L_H, L_M, R_g and C_{iss} results in a current i_g^{pre} that flows out of the gate prior to turn-off, as illustrated in the pre-charge equivalent circuit in Fig. 14. Thus, the gate-source voltage will be at a lower value V_{GS}^{pre} than V_H at turn-off, as illustrated in Fig. 15e.

F. Turn-off

The turn-off process is initiated at time instant t_1 by turning Q_3 off while keeping Q_2 on, as illustrated in Fig. 15b. The same analysis as provided in Section III-B is valid for the turn-off process, with "(25)" changed as

$$I_m \leq \alpha_s C_{iss}\left(V_{GS}^{pre} + |V_L|\right) \tag{29}$$

to avoid undershoot in v_{GS} below V_L. The value of I_m together with the other driver design parameters determines the speed of the turn-off transition.

G. Turn-off Auxiliary Charge Interval

At time instant t_2 after the turn-off, the auxiliary charging is initiated. The inductors L_H and L_L are charged with i_{aux} by turning Q_{aux} on, as illustrated in Fig. 15c. The amplitude of i_{aux} is determined by "(26)", similarly as for turn-on transition.

H. Auxiliary Turn-off

As for the auxiliary turn-on (Section III-D), the specific driver switches that need to turn on and off depend on whether the auxiliary current is to be sinked or injected. If injection (as i_g is negative during turn-off as defined in Fig. 7, "injection" is here current injected from the gate to the driver power supply) is desired , i.e., a higher negative value if I_{aux} than i_g at time instant t_3, Q_4 is turned on while Q_{aux} is turned off, yielding $i_g = i_m + i_{aux}$. If sinking is required, Q_4 is turned on, while Q_{aux} and Q_2 are turned off, yielding $i_g = i_{aux}$. To commutate i_m, Q_1 is turned on for a short period as explained in section III-D.

IV. Experimental Results

The proposed ACSGD was experimentally tested on a double-pulse test circuit (DPT) as illustrated in Fig. 16a with a photo of the setup shown in Fig. 16b. The setup consists of a

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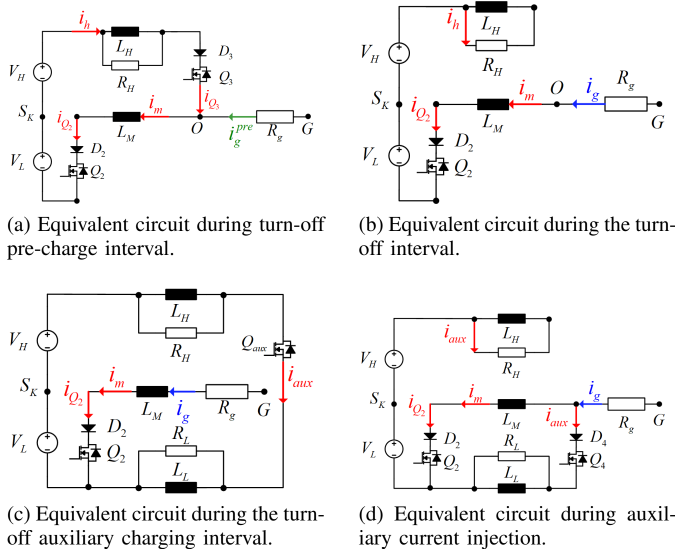
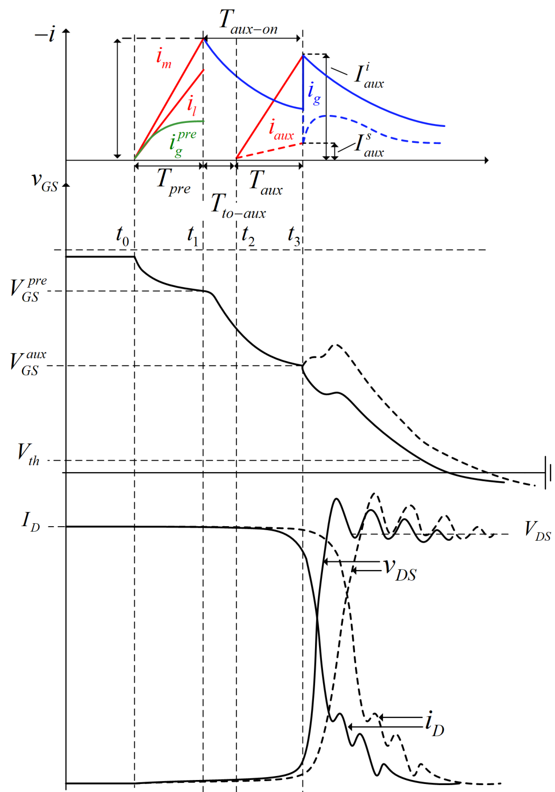


(a) Equivalent circuit during turn-off pre-charge interval.

(b) Equivalent circuit during the turn-off interval.

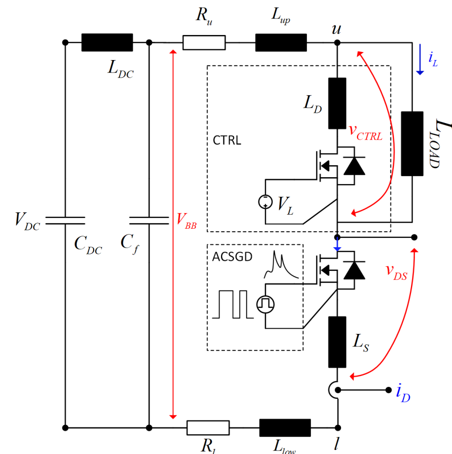
(c) Equivalent circuit during the turn-off auxiliary charging interval.

(d) Equivalent circuit during auxiliary current injection.

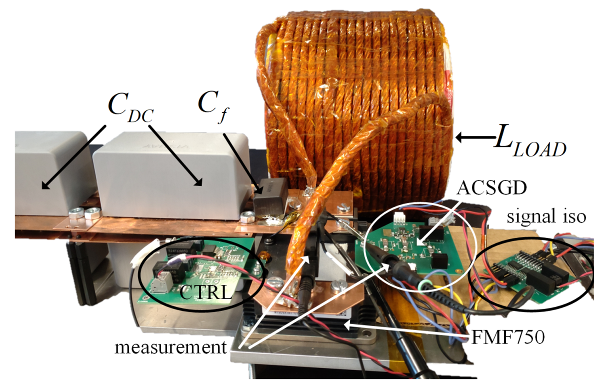


(e) Illustrative waveforms of the double gate current injection/sinking during turn-off.

Fig. 15: Illustrative waveforms for the turn-off transition showing the impact of injecting or sinking auxiliary gate current.



(a) Double pulse test equivalent circuit schematic.



(b) Photo of the experimental lab setup.

Fig. 16: Double pulse test setup.

TABLE IV: DUT Parameters

Device Name	FMF750DC-66A
Rated Blocking Voltage	$V_{BB} = 3.3kV$
Rated DC Drain Current	$I_D = 750A$
Internal Gate Resistance	$R_{g(int)} = 2.5\Omega$
Maximum v_{GS} Voltage Stress	$[V_{GS}^{max}/V_{GS}^{min}] = [20V/-20V]$

high-voltage SiC MOSFET half-bridge power module and an inductive load. The electrical parameters for the DPT are given in Table III, while Table IV summarizes the device parameters for the SiC MOSFET power module and Table V summarizing the measurement equipment used during testing.

The following subsection shows experimental results verifying the working principle of the ACSGD for different driver operation modes. These different modes are:

- *Single pulse* - Only i_m is varied with no additional second pulse.
- *Variable* di/dt - An additional current pulse is injected or sank at a specified time instant in order to vary the di/dt of the device.
- *Variable* dv/dt - An additional current pulse is injected or sank at a specified time instant in order to vary the dv/dt of the device.

A. Single pulse

By varying the pre-charge interval length $T_{pre} = t_1 - t_0$, the peak current I_m provided to the gate at turn-on and turn-off can be varied. This affects the speed at which the gate charge, Q_g, is provided to the gate, impacting the switching speed of the MOSFET. The variation of T_{pre} also affects the pre-charge value V_{GS}^{pre} of v_{GS} as described in Section III-A, affecting the turn-on and turn-off delay times. The effects of varying i_m are shown in Fig. 18 for the turn-on transition

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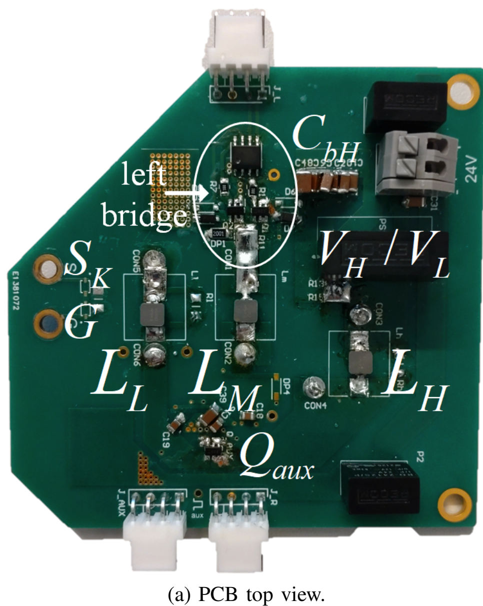
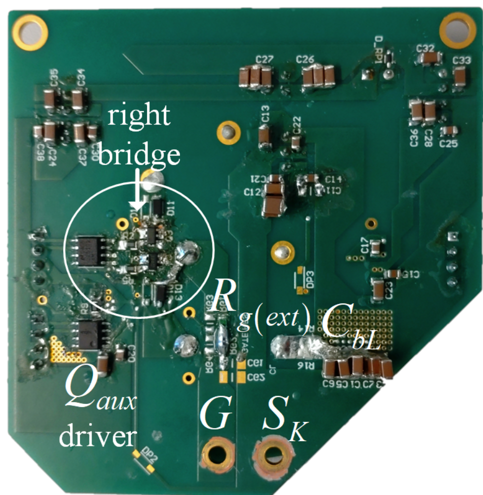


(a) PCB top view.



(b) PCB bottom view.

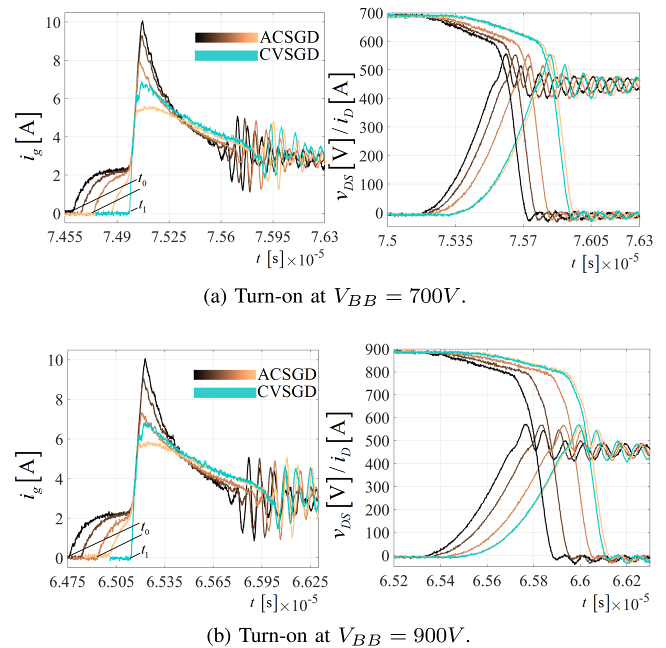
Fig. 17: ACSGD PCB photo.

TABLE V: Measurement Equipment

Scope	DPO4054B	$f_{bw} = 500MHz, 2.5GS/s.$
Voltage Probe v_{DS}	Tektronix P5100A	$f_{bw} = 500MHz$
Current Probe i_g	PEM CWTUM	$f_{bw} = 30MHz$
Current Probe i_D	PEM CWTUM	$f_{bw} = 30MHz$

with T_{pre} varied between $100 - 400ns$ and in Fig. 20 for the turn-off transition with T_{pre} varied between $100 - 500ns$. The value of I_m is varied and compared with a CVSGD having the same external gate resistance $R_{g(ext)} = 1.5\Omega$ for blocking voltages of $V_{BB} = 700V$ and $V_{BB} = 900V$ at a drain current level $i_D \approx 450A$.

Results containing turn-on and turn-off energy $E_{on/off}$, turn-on and turn-off delay $T_d^{on/off}$ and total turn-on and turn-off time $T_{on/off}$ for the CSVGD and ACSGD single pulse mode using maximum $I_m = I_m^{max}$ are summarized in Table VI. As shown from these tables, a 6.4% reduction at



(a) Turn-on at $V_{BB} = 700V$.

(b) Turn-on at $V_{BB} = 900V$.

Fig. 18: *Single pulse* turn-on operation of the ACSGD compared with the CVSGD (teal) with the same external gate resistance $R_{g(ext)} = 1.5\Omega$.

$700V$ and a 5.5% reduction at $900V$ is achieved for the turn-on energy E_{on}, and a 7.5% reduction at $700V$ and a 7.9% reduction at $900V$ is achieved for the turn-off energy E_{off}. An approximately 57% decrease in the turn-on delay time T_d^{on} and 32% decrease in the turn-off delay time T_d^{off} is achieved with the highest value of I_m compared to the CVSGD. An approximately 24% decrease in the total turn-on time T_{on} and 19.75% decrease in the turn-off time T_{off} is achieved with the highest value of I_m compared to the CVSGD.

TABLE VI: Single Pulse Results

	$E_{on}[J]$		$T_d^{on}[ns]$		$T_{on}[ns]$	
V_{BB}	$700V$	$900V$	$700V$	$900V$	$700V$	$900V$
CVSGD	0.0718	0.0996	350	350	960	980
ACSGD$^{I_m^{max}}$	0.0672	0.0941	150	160	730	750
Reduction [%]	6.4	5.5	57.2	54.3	24	23.5

	$E_{off}[J]$		$T_d^{off}[ns]$		$T_{off}[ns]$	
V_{BB}	$700V$	$900V$	$700V$	$900V$	$700V$	$900V$
CVSGD	0.0335	0.0406	900	900	1570	1590
ACSGD$^{I_m^{max}}$	0.0310	0.0374	610	610	1260	1290
Reduction [%]	7.5	7.9	32.2	32.2	19.75	18.9

The ACSGD energy use given by "(11)" is shown for the turn-on transition in Fig. 19 and for the turn-off transition in Fig. 21. The driver's energy use is calculated using experimental data from the time instant t_0 to the time point that v_{DS} reaches approximately the on-state drain-source voltage for turn-on, T_{on} and from t_0 to the time instant where i_D is approximately zero, T_{off}. As seen from Fig. 19, the energy use increases with increasing I_m (colorbar) and surpasses the

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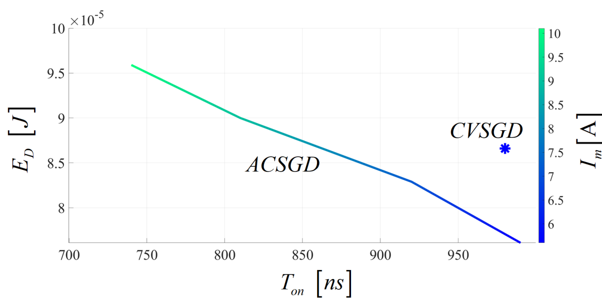


Fig. 19: ACSGD energy use $E_D[J]$ for the turn-on interval in single pulse mode.

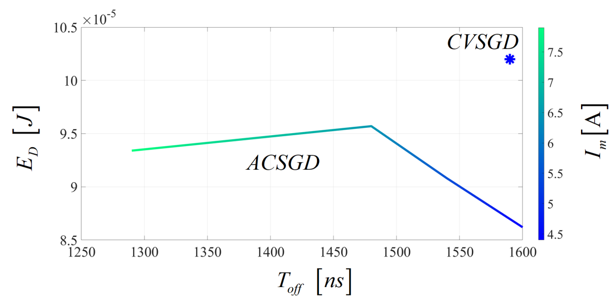
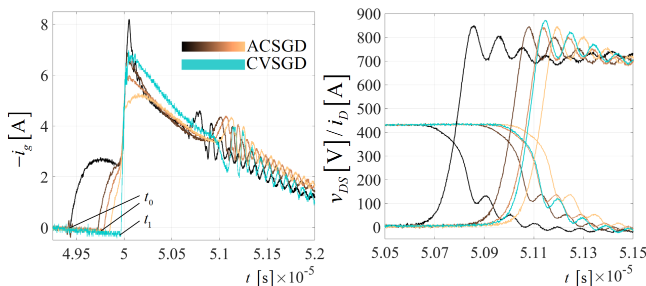
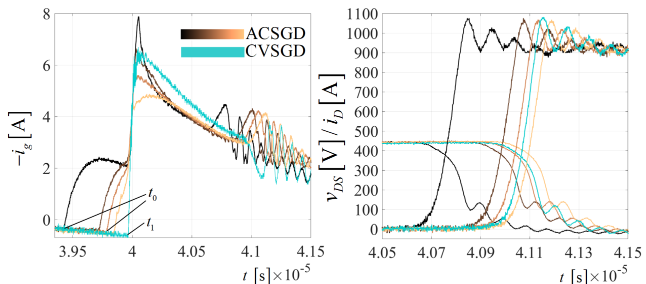


Fig. 21: ACSGD energy use $E_D[J]$ for the turn-off interval in single pulse mode.



(a) Turn-off at $V_{BB} = 700V$.



(b) Turn-off at $V_{BB} = 900V$.

Fig. 20: *Single pulse* turn-off operation of the ACSGD compared with the CVSGD (teal) with the same external gate resistance $R_{g(ext)} = 1.5\Omega$.

associated CVSGD energy use for a certain value of I_m. The turn-off transition has an similar E_D trend, although after a certain value of I_m the E_D decreases. This is due to the shortened T_{off}, having a larger decreasing effect on the integral calculation than the increasing amplitude of I_m. The CVSGD energy use is larger than the ACSGD due to the larger T_{off} and lack of pre-charge interval.

B. Variable di/dt

By varying the time to the auxiliary turn-on T_{aux-on} and T_{aux}, the ACSGD can manipulate di/dt and dv/dt of the switched device. By injecting i_{aux} before (turn-on) and after (turn-off) the Miller plateau (v_{DS} fall and rise intervals) the i_D slew rate can be controlled. This is shown in Fig. 22, where varying values of i_{aux} are injected to the gate at t_3 for an external gate resistor of $R_{g(ext)} = 1.5\Omega$. In Fig. 23, i_{aux} is varied and injected at different time instants t_3 (i.e., varying length of T_{aux-on}) for an external gate resistor of $R_{g(ext)} = 1.5\Omega$.

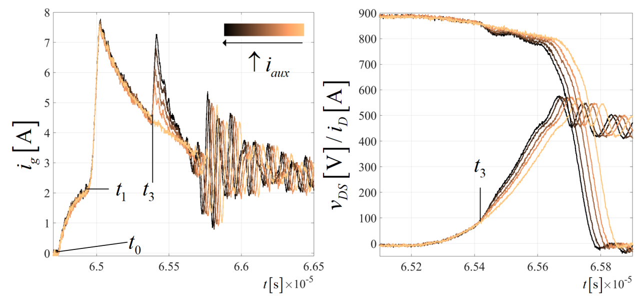


Fig. 22: Variable di/dt operation of the ACSGD with external gate resistance of $R_{g(ext)} = 1.5\Omega$ with $T_{aux-on} = 400ns$.

Results containing average and maximum di/dt, turn-on time T_{on} and turn-on energy E_{on} for different values of T_{aux-on} and I_{aux} are shown in Table VII. It is clear from this table and Fig. 23 that di/dt is controllable using the ACSGD. In particular, the maximum value of di/dt is highly controllable and can vary between $1.24A/ns$ to $4.5A/ns$ that is a maximum increase of 233% when the peak auxiliary current varies from $I_{aux} = 0$ to $I_{aux} = I_{aux}^{max}$. The greatest reduction of turn-on energy loss E_{on} is obtained for $T_{aux-on} = 750ns/I_{aux} = I_{aux}^{max}$ with a 33.5% decrease in E_{on} for the tested parameters.

TABLE VII: Results with variable di/dt

I_{aux}	T_{aux-on}	avg. di/dt	max. di/dt	$T_{on}[\mu s]$	$E_{on}[J]$
0	-	0.67 A/ns	1.24 A/ns	0.125	0.1189
I_{aux}^{max}	350 ns	0.87 A/ns	1.35 A/ns	0.110	0.1183
	500 ns	0.91 A/ns	1.46 A/ns	0.108	0.1060
	750 ns	0.91 A/ns	3.2 A/ns	0.107	0.0798
	900 ns	0.88 A/ns	4.5 A/ns	0.109	0.0818

C. Variable dv/dt

By injecting i_{aux} *during* the Miller plateau (v_{DS} fall and rise interval) the v_{DS} slew rate can be controlled. This is shown in Fig. 24, where varying values of i_{aux} are injected to the gate at t_3 when v_{DS} starts falling for an external gate resistor of $R_{g(ext)} = 1.5\Omega$. In Fig. 25, i_{aux} is varied and injected at different time instants t_3 (i.e., varying length of T_{aux-on}) for an external gate resistor of $R_{g(ext)} = 4\Omega$. Results containing average dv/dt, turn-on time T_{on} and turn-on energy E_{on} for different values of $R_{g(ext)}$ and I_{aux} are given in

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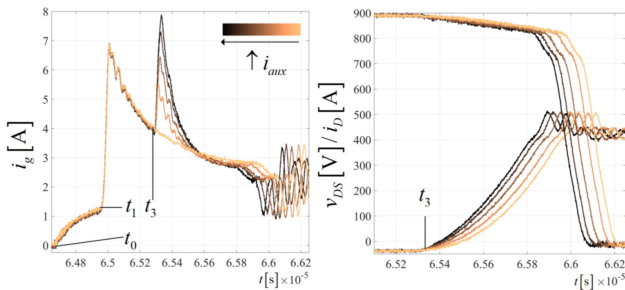
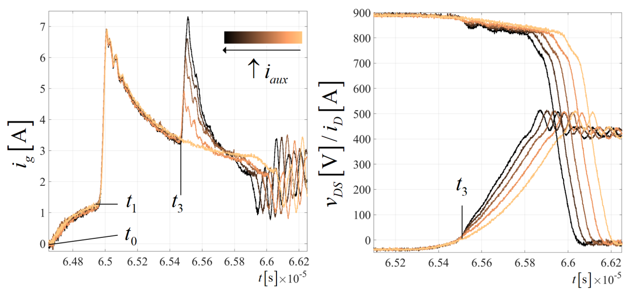
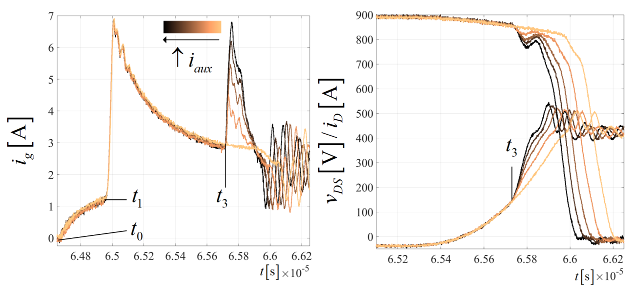


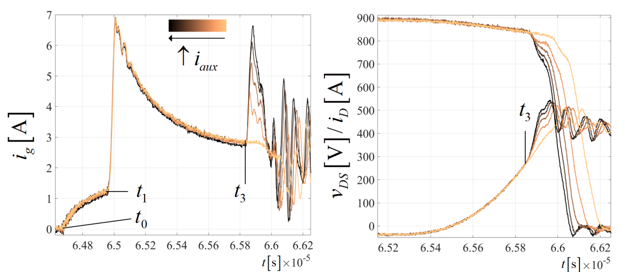
(a) Turn-on at $V_{BB} = 900V$ with $T_{aux-on} = 350ns$.



(b) Turn-on at $V_{BB} = 900V$ with $T_{aux-on} = 500ns$.



(c) Turn-on at $V_{BB} = 900V$ with $T_{aux-on} = 750ns$.

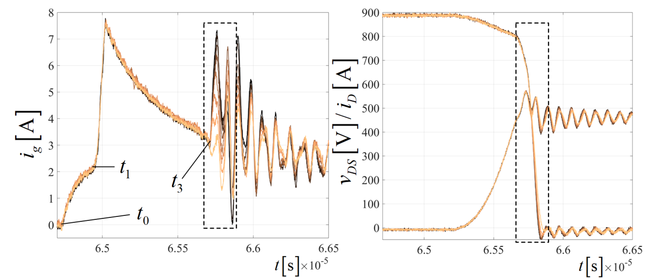


(d) Turn-on at $V_{BB} = 900V$ with $T_{aux-on} = 900ns$.

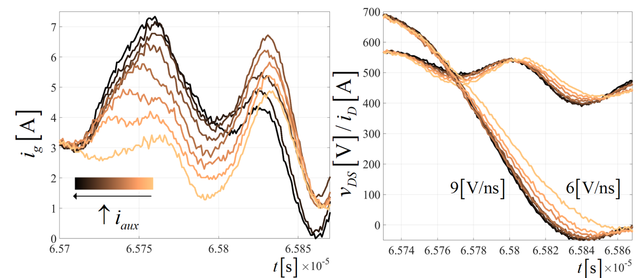
Fig. 23: Variable di/dt operation of the ACSGD with external gate resistance of $R_{g(ext)} = 4\Omega$

TABLE VIII: Results with variable dv/dt

$R_{g(ext)}$	I_{aux}	dv/dt	$T_{on}[\mu s]$	$E_{on}[J]$
1.5 [Ω]	0	$5.5\ V/ns$	0.890	0.1009
	I_{aux}^{max}	$9.5\ V/ns$	0.860	0.0987
4 [Ω]	0	$4\ V/ns$	1.350	0.1209
	I_{aux}^{max}	$7.5\ V/ns$	1.290	0.1121



(a) Turn-on at $V_{BB} = 900V$.



(b) Zoomed in view of turn-on at $V_{BB} = 900V$.

Fig. 24: *Variable* dv/dt operation of the ACSGD with external gate resistance of $R_{g(ext)} = 1.5\Omega$.

Table VIII. As can be seen from this table, a 73% increase in dv/dt is achieved for $R_{g(ext)} = 1.5\Omega$ and a 87% increase in dv/dt is achieved for $R_{g(ext)} = 4\Omega$ with the highest value of $I_{aux} = I_{aux}^{max}$ compared to no i_{aux} injection.

V. Discussion

The ACSGD is shown to be able to provide flexible turn-on and turn-off delay times, controllable turn-on and turn-off switching times, as well as adjustable di/dt and dv/dt values. Therefore, the ACSGD is a suitable driver concept for power electronic converters where such features are desired. In general, using CCSGD enable the possibility of reduced switching speeds and, hence, reduced switching loss compared to CVSGD, at the cost of increased gate driver energy use. This is beneficial in converter designs having strict efficiency requirements. The ACSGD in single mode operation provides flexibility in turn-on and turn-off delay times and switching speed control. The possibility of reduced turn-on and turn-off delay times is an advantage in dead-time sensitive converter applications such as the DAB converter. Considering the DAB converter operating in buck-mode, it is unable to transfer its rated power if the ratio of the dead-time to the switching period halved is larger than approximately 0.25 [33]. The dead-time can further impact the DAB operation with unwanted effects such as voltage reversal, phase drift, increased reflow power and voltage sag. However, the dead-time should be sufficiently long to discharge the output capacitance C_{oss} of the converter MOSFETs in order to achieve zero-voltage switching. The optimal dead-time length is thus depending on the converter operating point. The ACSGD's ability to dynamically adapt the dead-time to the converter operating point could thus be highly advantageous in such converters, allowing for a more optimal converter performance.

The adjustable switching speeds are not only desirable

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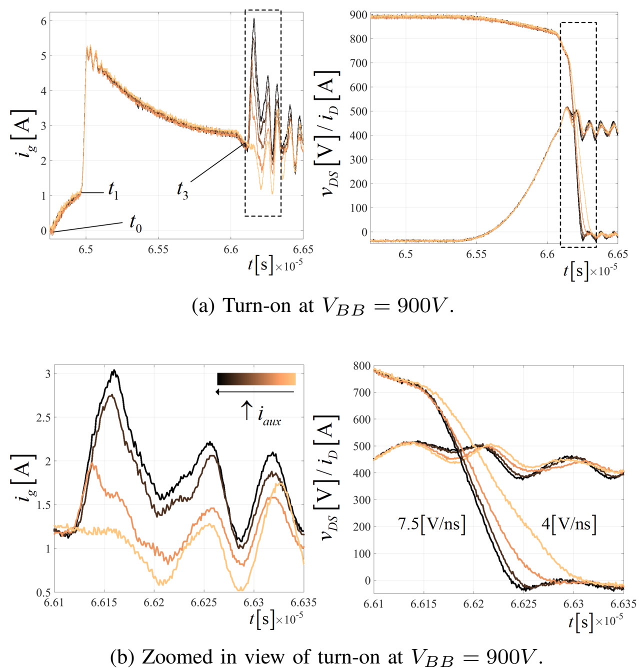
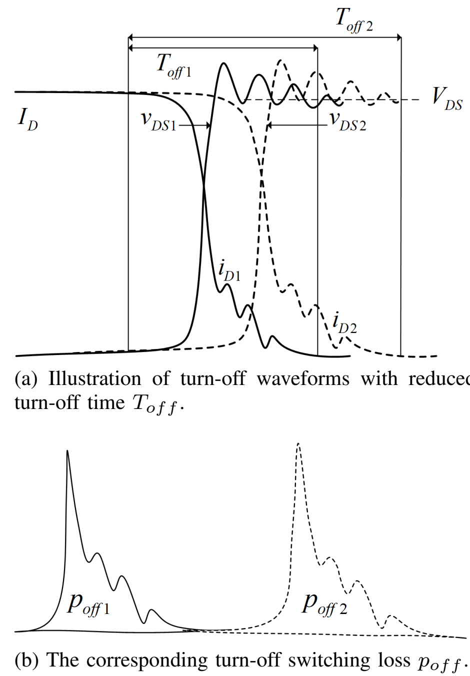


(a) Turn-on at $V_{BB} = 900V$.

(b) Zoomed in view of turn-on at $V_{BB} = 900V$.

Fig. 25: *Variable* dv/dt operation of the ACSGD with external gate resistance of $R_{g(ext)} = 4\Omega$.



(a) Illustration of turn-off waveforms with reduced turn-off time T_{off}.

(b) The corresponding turn-off switching loss p_{off}.

(c) Illustration of relative reduction in turn-off time compared to turn-off switching energy E_{off}

Fig. 26: Illustration of the turn-off procedure showcasing the switching losses variations.

for reduced switching loss possibility resulting in increased converter efficiency, but also for active thermal control (ACT). By actively controlling the switching loss, the junction temperature of the SiC MOSFETs can be controlled. In particular, by increasing the switching losses, the junction temperature increases and vice versa. Thus, the anticipated temperature cycles under load variations can also be controlled. Operating the power devices under load variations for improved reliability, necessitates the junction temperature variations to be kept as low as possible. Thus, the amount of lifetime consumed is minimised, since lifetime is inversely proportional to the temperature variations. The variable di/dt and dv/dt modes can also enable electromagnetic emission control, suitable for application where strict electromagnetic compatibility constraints are of essence.

As seen in Table VI, there is a lower reduction in the turn-on and turn-off energies (E_{on}/E_{off}) than in the turn-on and turn-off times (T_{on}/T_{off}). The reason for this is that the drain current i_D in the saturation region evolves according to "(28)", hence a reduction in (T_{on}/T_{off}) is not linearly reflected on a reduction in (E_{on}/E_{off}). For example, a 20% reduction, calculated as

$$\%\text{reduction} = 100 \cdot \frac{\text{val}_2 - \text{val}_1}{\text{val}_2} \tag{30}$$

in T_{off} does not correspond to a 20% reduction in E_{off} due to the drain current transfer characteristics and evolution of i_D, as illustrated in Fig. 26.

The oscillations in the waveforms in the experimental measurements are caused by the energy exchange between the power loop inductance $L_{low} + L_D + L_S$ and the equivalent device capacitance of the DUT approximated by C_{oss} [41]. These circuit and device parameters constitute a resonant circuit and consequently cause oscillations in i_g (and v_{GS}) through C_{gs} feedback.

VI. Conclusion

This paper proposes a novel adaptive current source gate driver capable of adaptively control the gate current of high-voltage SiC MOSFETs. The gate current manipulation is achieved by the proposed ACSGD enables independent control of turn-on and turn-off delay times, di/dt and dv/dt. The driver can provide reduced switching loss, shorter turn-on and turn-off delay times and shorter total turn-on and turn-off times compared to conventional voltage and current source gate drivers. Furthermore, the ACSGD ability to independently control di/dt and dv/dt is advantageous with respect to electromagnetic compatibility, the adaptive switching loss capability is advantageous for active thermal control and the adaptive turn-on and turn-off delay times is advantageous for dead-time critical power electronic systems, amongst others. From experiments on a 3.3kV/750A SiC MOSFET half-bridge power module, it has been shown that di/dt can be controlled

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in a range between $1.24A/ns$ to $4.5A/ns$ allowing switching energy reduction from $0.1183J$ to $0.0818J$, respectively. In addition, dv/dt has been shown to be controllable in a range of 87%, while turn-on and turn-off delay times are reduced by 57% and 33%, respectively. These results prove the applicability of the proposed ACSGD to power semiconductor devices requiring adaptive functionalities for improving electrical and thermal performance.

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