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High precision scalable power converter for accelerator magnets

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ABSTRACT: The lower conduction power losses and the positive temperature coefficient that favours parallel connections, make Silicon Carbide (SiC) metal oxide semiconductor field-effect transistors (MOSFETS) to be an excellent replacement of existing Silicon insulated gate bipolar transistors (IGBTs) technology. These characteristics combined with high switching frequency operation, enables the design of high-accuracy DC-DC converters with minimised filtering requirements. This paper investigates the design for a converter with high-accuracy current (0.9 ppm) supplying a 0.05 H electromagnetic load, aiming to achieve the accuracy without the use of active filters, by using SiC MOSFETs and a scalable module-based converter design.

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Contents

1 Introduction

A primary objective of the powering in particle accelerator is the precision and reproducibility of the experiments. Scalable converters enable sub-ppm current precision with minimal filtering requirements by using multiple modules in interleaved operation [1]. In order to reach the <1 ppm level which is required for some applications, active filters are often used [2]. However, they require relatively large reactors, contribute to power losses and their control is not trivial. With the introduction of Silicon Carbide (SiC) metal oxide semiconductor field-effect transistors (MOSFETs) as a commercial alternative to silicon insulated gate bipolar transistors (IGBTs) for switch-mode converters, it is now feasible to utilise SiC semiconductor technology in the world of high-energy particle physics as well. This paper demonstrates a case study for a 0.05 H electromagnet with high accuracy requirement of 0.9 ppm and investigates the performance improvements to the design and operation of such converters when using SiC MOSFETs compared to IGBTs. The benefits of the SiC MOSFET are two-fold. Firstly, the reduced conduction on-state losses and positive on-state temperature coefficient and secondly, the reduced switching losses, enabling operation at higher switching frequencies. And since the SiC based technology is emerging with lower current ratings than the IGBTs, parallel connection is necessary to take advantage of the SiC MOSFETS.

The reduced on-state losses of SiC MOSFETs enables high-efficiency operation. Besides, their positive temperature coefficient facilitates a robust and more reliable parallel connection, as the positive temperature coefficient leads to natural balance of the current. If the parallelisation required to handle the current is achieved by parallel connecting H-bridges, introducing a number of parallel connected DC-DC converter enables the use of interleaving to achieve a lower current ripple.

The current these power converters are designed to supply, will often be a series of trapezoid current pulses. These are supplied by power converters with built in energy recovery to reduce the overall energy consumption of the experiments [3, 4]. An example of such a current train is shown in figure 1(a). Since the ramping and energy recovery often will require negative voltage

to be applied across the magnet during ramp-down, such as in figure 1(b), the power converters are required to have 4-quadrant operation and a energy storage facility. Taking into account the advantages of SiC based MOSFETs, and taking the need for parallelisation as an opportunity, some interesting possibilities emerge with regards to reducing the ripple of the current supplied to magnets.
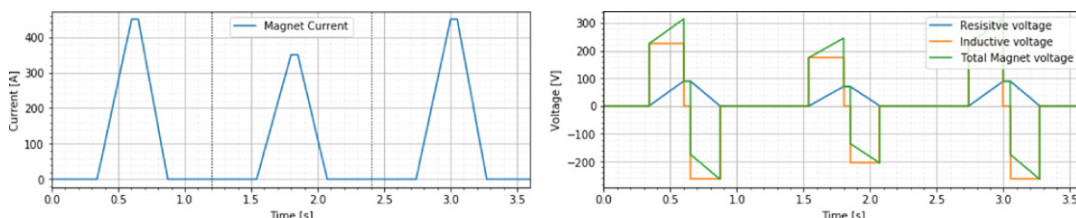
(a) Typical current cycle sequence, dotted lines indicate division between cycles.

(b) Typical voltage requirement for the cycles.

**Figure 1.** Examples of load which the DC-DC converters have to be designed for.

2 The modular power converter

Considering the constraints mentioned in the introduction, the magnets are normally supplied by an H-bridge with an electrolytic capacitor bank as energy storage [4]. The converter is such that often one converter is sufficient, perhaps combining 2 or 4 in series, parallel or series-parallel combination to achieve the required outputs, depending on the specific magnet. By opting for a parallel connection of power converters, the size and power ratings of each power converter can be reduced. The converter is now consisting of smaller identical modules, which will be named bricks, and for this paper the brick size has been chosen as 100 V and 100 A. This choice is based on previous work relating to the sizing system and operating cost of such modular power converters [5].

The proposed topology employs several bricks and assumes different functionality for them; some of them are connected to energy storage for the recovery of the magnet *B*-field energy while other bricks are connected to a power source (i.e. the grid) and supply the power losses due to the magnet resistance and the circuit self-consumption and the option to reduce the front-end peak-load and greater utilisation of the storage [6]. More specifically in the example of figure 2, four of the bricks are connected to storage while just one brick is connected to the power grid via a 3-phase diode rectifier.

This paper ends up with the topology shown in figure 2, with each brick able to supply 100 V and 100 A. Four of the bricks are connected to storage, and supply the reactive power to the magnet, and the 5th brick is connected to the grid via a 3-phase diode rectifier. Normally the power converter would be connected to the magnet via an active filter, which ensures the requirement for current accuracy. However, this filter is omitted in this paper in an effort to achieve the same accuracy by simply interleaving several bricks and operate them at higher switching frequencies. In this converter configuration and also in the modelling and simulations the arm inductance and

the intrinsic inductances were considered small compared to the inductance of the load, meaning they don't need to be compensated for by the converter control.
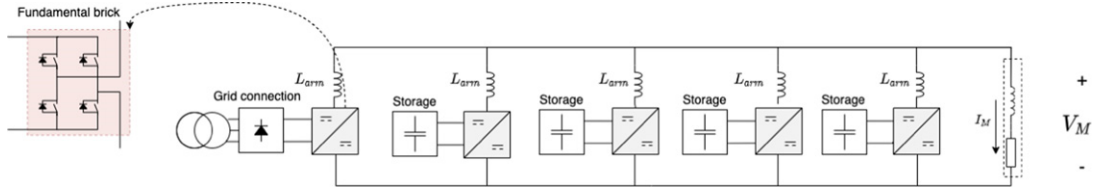

Figure 2. A possible configuration of the parallel connected bricks.

3 Simulating the interleaving

To investigate the performance of the parallel connected bricks, a PLECS model based of the topology in figure 2 was developed and simulated, where the number of parallel connected bricks was varied from 1 up to 25, to investigate the effect of using SiC MOSFETs with relatively small current rating to supply a large current with interleaving. The single brick compares to the conventional case where the current is supplied by a single power converter. This was done to understand how the interleaving would influence the current ripple to the inductive load of a magnet. All simulations were performed without considering power losses, apart from the resistance in the magnet, or relevant limits in dv/dt for the power semiconductor devices and the magnets. The interleaving was achieved by phase-shifting each of the bricks evenly, i.e., the phase-shift of brick N_i is $N_i = 360\frac{1}{N_{\text{bricks}}}$. Where N_{bricks} is the total number of bricks, and N_i is one of the bricks.

4 Effect of parallelisation and frequency on the current ripple

Using the voltage and current results shown in figure 3, it is possible to estimate the ripple of the current through the magnet. If the number of interleaved bricks is larger than one ($N_{\text{bricks}} > 1$), the voltage switches between zero and a positive value V_{M}, which is different to the bus voltage V_{bus}. And as the number of parallel connections increases, the number of pulses increases proportionally and the magnitude of the voltage is inversely proportional. The current in the magnet is ramped up when the voltage is positive, and slowly discharges through the resistor when the voltage is zero. This voltage is determined by $V_{\text{M}} = \frac{V_{\text{arm}}}{N_{\text{arms}}}$, and the duration of the applied voltage is controlled by the duty cycle of the bricks. The current is in the flat-top phase, so the average current over one cycle is equal to the DC-current applied, where the duty cycle m gives the following average voltage: $\widehat{V}_{\text{M}} = V_{\text{M}}m$. This is the voltage driving the ramp-up of the current. The voltage $\widehat{V}_{\text{M}}$ is also equal to the average DC-voltage required to sustain the current in the resistor component of the magnet, thus $\widehat{V}_{\text{M}} = I_{\text{flat}}R_{\text{M}}$.
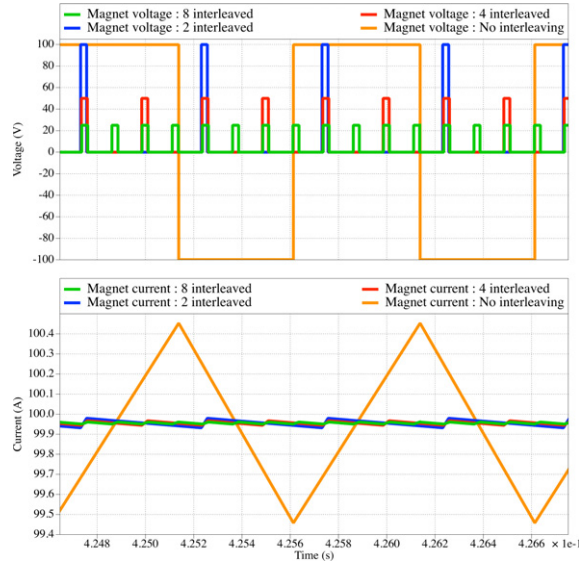
Figure 3. A plot showing the wave-forms of the interleaved voltage and current supplied to the magnet.
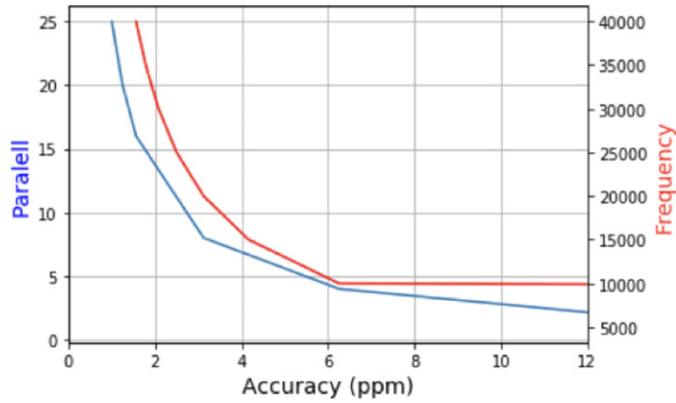
Figure 4. Effect of interleaving on magnet voltage (and current) precision (blue line: varying number of bricks with a fixed frequency of 40 kHz. Red line: varying the frequency with a fixed number of 16 interleaved bricks).

Using the fundamental relationship of an inductor in (4.1), and considering the delta current during the increasing of the ripple, the increasing current $di_M = \Delta I_{ripple}$ can be expressed in terms of the voltage V_M, inductance L_M and time $dt = m\frac{1}{f_{sw}}$.

$$V_M = L_M \frac{di_M}{dt}. \tag{4.1}$$

Using (4.1) and expressing for the ΔI_{ripple} the ripple can be expressed as in eq. (4.2). This finding closely matches the observed results from the simulations as shown in figure 4 for the case where $N_{arms} > 1$. Using the results obtained in eq. (4.2), the estimate is that 4.44 parallel strains should give the required accuracy at 50 kHz. This result has been achieved with only a

moderate increase of the switching frequency that becomes possible with a SiC technology device. In practice, 5 parallel interleaved bricks are sufficient to achieve the ripple accuracy of 0.9 ppm. This topology is shown in figure 2.

$$\Delta I_{\text{ripple}} = \frac{V_M \, dt}{L_M} = \frac{\frac{\widehat{V}_M}{mN_{\text{arms}}} \frac{m}{f_{\text{sw}}}}{L_M} = \frac{I_{\text{flat}} R_M}{L_M f_{\text{sw}} N_{\text{arms}}} \implies \Delta I_{\text{ppm}} \approx \frac{R_M}{L_M f_{\text{sw}} N_{\text{arms}}}. \tag{4.2}$$

5   Summary

The current ripple form a single converter can be approximated by (5.1), where the ripple is inversely proportional to the switching frequency of the DC-DC converter. By using SiC MOSFETs it becomes possible to increase the switching frequency from 5 kHz that is currently used, up to 60 kHz and beyond. This gives an increase in accuracy by an order of magnitude or more. In addition, higher switching frequency results in a higher frequency on the ripple, reducing the size of any filters if they are still required. Thus, the anticipated cost and losses of filters are reduced. It is also possible to consider 3-level modulation (unipolar switching), reducing the ripple even further.

$$\Delta I_{\text{ppm}} \approx \frac{R_M}{L_M f_{\text{sw}} N_{\text{arms}}}. \tag{5.1}$$

Introducing parallel connected devices leads to an increased investment cost for the devices, but it can reduce the device losses, cooling requirements, filter requirements and filter losses. In addition to being a more scalable topology, which enables it to cover a large range of loads with minimal overcapacity and the possibility to have redundancy in the converter. It also introduces more segmentation for the storage in the case of pulsed loads with storage requirements for the DC-DC converter. By taking a complete view and considering lifetime costs, SiC MOSFETs seem to be very suitable technology for this application [5]. Using the topology in figure 2 with interleaving, it is possible to achieve the sub ppm filter requirement without using active filters for this particular load. The results in figure 4 shows the effect of interleaving and switching frequency on the current ripple. At relative small number of parallel connected bricks, the sub-ppm accuracy seems achievable. Combining with SiC MOSFETs this solution compares well to a conventional converter with IGBTs and active filters.

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