Tobias Kristensen

Distributed Topology for Improved Thermal Performance in RFPA Design

Master's thesis in Electronics Systems Design and Innovation
Supervisor: Morten Olavsbråten
Co-supervisor: Arne Øistein Olsen
June 2022

Master's thesis

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Abstract

This work considers how a distributed topology can be used to reduce thermal challenges in power amplifiers. This is a relevant topic for modern radio systems where thermal considerations are a limiting factor due to highly modulated signals, large bandwidth and increasingly integrated systems. Combining multiple transistors in a distributed topology reduces the thermal stress on the individual transistors and simplifies cooling. This increases the reliability or allows increased output power.

A method for analysing a distributed topology is presented, where the thermal coupling for multiple transistors mounted on the same baseplate is considered. The gain of a distributed topology is discussed through an example, where the result shows that the distributed topology has a considerably reduced junction temperature. The method is also used to discuss different topologies and design parameters.

The design of a 100W PA with a distributed topology is also presented. The thermal behaviour of the amplifier is measured and fits well with the results from the presented model. However, the measurement uncertainty is too significant that it can be stated that the model gives a precise estimate. The amplifier has a measured $P_{del} > 50dBm$, PAE of 57-63% and G_T of $11 - 12dB$ in the 1.75-2.25 GHz frequency range. The amplifier has premature gain compression and is shown to only be conditionally stable. However, the design shows that a distributed topology is suitable for high power PA design.

The conclusion is that distributed topology is a good method for reducing the thermal stress in a PA. However, it is costly due to an increased number of components, larger area and increased complexity. Consequently, it should only be considered where it is necessary.

Sammendrag

Denne oppgaven tar for seg hvordan en distribuert topologi kan benyttes for å redusere den termiske belastningen i effektforsterkere. Dette er en høyaktuell problemstilling i moderne radiosystem med redusert effektivitet grunnet avanserte modulasjonsteknikker og høy båndbredde, kombinert med stadig mer kompakte system. Ved å kombinere flere transistorer i en distribuert topologi reduseres den termiske belastningen på de individuelle transistorene og kjølingen forenkles. Dette gir en økt pålitelighet for systemene, eller tillater at utgangseffekten kan økes.

En metode er presentert der man ser på varmefordelingen når flere transistorer er montert på samme bakplate. Denne metoden er benyttet i et eksempel for å belyse gevinsten med en distribuert topologi. Resultatet viser at en distribuert topologi gir en betydelig lavere driftstemperatur. Med bakgrunn i metoden er også ulike konfigurasjoner og betydningene av design parameterne diskutert.

Designet av en 100W PA med distribuert topologi er også presentert. Den termiske oppførselen til forsterkeren er målt, og stemmer godt overens med resultatet fra den presenterte metoden. Likevel er det for stor måleusikkerhet til å si med sikkerhet at metoden gir et presist estimat. Forsterkeren har en målt $P_{del} > 50dBm$, PAE mellom 57-63% and G_T på $11 - 12dB$ i frekvensområdet 1.75-2.25 GHz. Forsterkeren har et prematurt vinningstap og er kun stabil under gitte forhold. Likevel, viser designet at en distribuert topologi er egnet for design av effektforsterkere med høy utgangseffekt.

Konklusjonen er at distribuert topologi er en velegnet metode for å redusere den termiske belastningen. Det er likevel en svært kostbar metode, med tanke på økt antall komponenter, økt areal og økt kompleksitet. Det er derfor viktig at det gjøres en avveining om det er nødvendig for applikasjonen.

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First, I would like to thank my supervisors, Morten Olavsbråten and Arne Øistein Olsen, for their valuable help and motivation this last year. I have been lucky to have you as supervisors.

I would like to acknowledge Anders Ivar Haugen for his valuable help while measuring and Mattias Thorsell for valuable input on thermal considerations for GaN transistors.

In the end, I would also like to thank friends and classmates for five great years in Trondheim. And, of course, thank my family for their support.

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Abbreviations

PA - Power Amplifier

RF - Radio Frequency

RFPA - Radio Frequency Power Amplifier

OFDM - Orthogonal Frequency-Division Multiplexing

QAM - Quadrature Amplitude Modulation

SDR - Software Defined Radio

ECCM - Electronic Counter-Counter Measure

MIMO - Multiple Input, Multiple Output

Tx/Rx - Transmitter and Receiver

P1dB - 1 dB compression point

P2dB - 2 dB compression point

P3dB - 3 dB compression point

PAE - Power Added Efficency

PAPR - Peak-to-Average Power Ratio

IPBO - Input Power Back-Off

DC - Direct Current

ADS - PathWay Advanced Design System, Keysight

IR - Infrared

GaN - Gallium Nitride

TOSM - Trough, Open, Short, Match (Calibration method)

VNA - Vector Network Analyzer

DUT - Device under test

PCB - Printed Circuit Board

LMBA - Load Modulated Balanced Amplifier.

EER - Envelope Elimination Restoration

EM - Electromagnetic

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Chapter 1

Introduction

1.1 Motivation

The power amplifier (PA) is a central component used in transmitters to boost output power. It is commonly placed at the end of the output stage to drive an antenna. It operates at radio-frequency (RF) and has the highest power in the transmitter. Therefore it plays a dominant role for the overall efficiency and signal distortion.

The PA is a significant heat source due to the high output power combined with imperfect efficiency. In the case of insufficient cooling, this dissipated power results in an increased operating temperature due to thermal resistances. Thermal considerations must be kept in mind, as components have a maximum operating temperature they can handle before they fail. In addition, performance and reliability are generally lowered by higher operating temperatures.

Today, thermal management is an increasingly important topic in RFPA design. Three reasons stand out in this regard:

1. Advanced modulation schemes are commonly used to boost data rates in modern communication systems. One case is OFDM, where multiple carriers are combined to get superior robustness for radio transmission while maintaining a high data rate. Unfortunately, the combination of multiple carriers gives a high peak-to-average ratio. Consequently, the amplifier needs to operate in back-off to avoid clipping, which gives a considerable drop in average efficiency. Another case is high order QAM modulations, where a high number of bits are transmitted per symbol, giving a high data rate. However, short distance between the symbols gives a low margin of error for non-linearities in the amplifier. The amplifier then needs to operate in back-off to reduce signal compression at the cost of reduced efficiency.

2. The use of large bandwidths is highly desirable when implementing software-defined radios (SDR). First of all, a large bandwidth gives a flexible radio platform capable of communicating with multiple other radio systems operating at different frequencies. Secondly, a large bandwidth allows the system to adapt to the radio environment to avoid interference. For instance, this can be used by a cognitive

radio to utilise the radio spectrum more efficiently. Additionally, it is essential for defence communication as an electronic counter-countermeasure (ECCM) to be able to change band if disturbed, either by jamming or unintended interference. However, in practice, large bandwidth comes at the cost of reduced efficiency. This is seen through the Bode-Fano criterium, which shows that the theoretical limit for how well a load can be matched is reduced for increasing bandwidth [1]. Efficiency boosting techniques are also generally hard to implement for multi-octave bandwidths.

3. Advances in technology have opened the doors for making more compact and highly integrated systems. Massive MIMO base stations are an example of a highly integrated system central to the new 5G networks. Here, a high number of Tx/Rx modules and advanced beamforming can be used to increase spectral efficiency. From a thermal perspective, this results in an increased density of heat sources per area, increasing the effects of thermal coupling and likely increasing the case temperature when the cooling capabilities are limited. The same can also be seen within radars, where many Tx/Rx modules are used to control active phase steered arrays.

This project is done in cooperation with Kongsberg Defence & Aerospace, a leading supplier of advanced defence communications systems. Defence communication systems have strict demands for large bandwidths and high linearity, preferably in a compact case. Consequently, they experience challenges with thermal considerations and describe it as a limiting factor for what output power they can deliver. Thermal management is, therefore, a highly relevant issue to study.

1.2 Scope and contribution

This work considers how a distributed topology can be used to reduce thermal challenges. Here, distributed topology is used to describe the case where a large transistor is replaced by power combining multiple smaller transistors. The hypothesis is that spreading the power over multiple transistors reduces the thermal stress on the individual transistors. Spreading the heat dissipation over a larger area also helps ease the system's cooling. This can help increase the system's reliability or further increase output power.

The scope is limited to considering the method from a circuit designer's point of view. Aspects such as the cooling, circuit environment or transistor implementation will only be considered where it impacts the circuit design.

The main contribution is a method that can be used to consider if a distributed topology is practical and evaluate design parameters. The method is verified by measuring a realised amplifier.

1.3 Outline

Chapter 1: The first chapter introduces the motivation for thermal management and a distributed topology. The scope, main contribution and outline of the work are also presented.

Chapter 2: Here, the theoretical background for the work is presented. The measures and techniques used to design and measure a PA is presented here. In addition, an equivalent thermal circuit is introduced for the transistor, which is used to describe thermal considerations.

Chapter 3: A method for estimating the junction temperature of transistors mounted on the same baseplate is presented. The significance of a distributed topology is investigated through an example using this method. In addition, the design parameters and different topologies are investigated.

Chapter 4: The design of a power amplifier is presented, where four 25W transistors are combined for 100W delivered power. Simulated results and stability analysis are also presented here.

Chapter 5: The thermal performance of the amplifier from chapter 4 is measured, together with small- and large-signal performance. The method and results are presented for each measurement.

Chapter 6: Results from chapter 6 are discussed and used as a base for discussion of the method from chapter 3. The advantages and disadvantages of a distributed topology are additionally discussed from a general viewpoint, and alternative methods are introduced. Suggestions for future work are presented at the end.

Chapter 7: The results of the work are shortly summarised and concluded.

Chapter 2

Background theory

Parts of section 2.1, 2.2, 2.3 and 2.7 are repeated from previous work in [2] and extended here.

2.1 Amplifier measures

2.1.1 S-parameters

Scattering parameters (S-parameters) describe the behaviour of a linear network by considering the relationship between the incident waves a_n and reflected waves b_m at the different ports in the system. It is commonly used to describe the small-signal response of a linear system, as they are easy to measure using a Vector Network Analyzer.

$$\begin{bmatrix} b_1 \\ b_2 \end{bmatrix} = \begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} \cdot \begin{bmatrix} a_1 \\ a_2 \end{bmatrix} \tag{2.1}$$

A two-port device is shown in figure 2.1 with it incident waves a_1, a_2 and reflected waves b_1, b_2. This device can be described using the S-parameter matrix shown in 2.1. These individual S-parameters will then be:

$S_{11} = \frac{b_1}{a_1}\big|_{a_2=0}$ - The reflection coefficient for port1, Γ_{in}.

$S_{21} = \frac{b_2}{a_1}\big|_{a_2=0}$ - The forward gain.

$S_{12} = \frac{b_1}{a_2}\big|_{a_1=0}$ - The reverse gain.

$S_{22} = \frac{b_2}{a_2}\big|_{a_1=0}$ - The reflection coefficient for port 2, Γ_{out}.

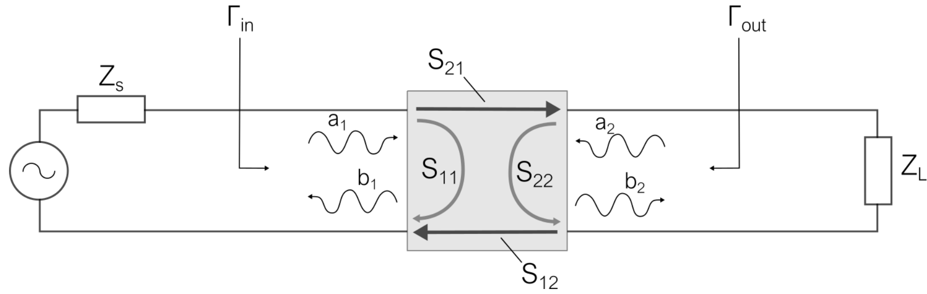


Figure 2.1: Two port device with incident waves a_1, a_2 and reflected waves b_1, b_2. The corresponding S-parameters are also marked. [2].

2.1.2 Gain

The Power Gain is the ratio between the average power delivered to the load and the average power delivered from the source, shown in equation 2.2. An alternative is the Transducer Gain which considers the average power available from the source instead, as shown in equation 2.3.

$$G_P = \frac{P_L}{P_S} \tag{2.2}$$

$$G_T = \frac{P_L}{P_{avs}} \tag{2.3}$$

The advantage of G_T is that it depends on the source and load impedances and, consequently, accounts for a mismatch. Considering the general amplifier shown in figure 2.2, G_T can be seen as a combination of the intrinsic transistor gain ($G_0 = \left|S_{21}\right|^2$), and the matching circuit gains (G_S, G_L). This is shown in equation 2.4 [3, p.563]. It can be seen that G_T will be maximised when the matching circuits are conjugate matched, meaning $\Gamma_S = S_{11}^*$ and $\Gamma_L = S_{22}^*$.

$$G_T = G_S \cdot G_0 \cdot G_L = \frac{1 - |\Gamma_S|^2}{|1 - \Gamma_{in}\Gamma_S|^2} \cdot |S_{21}|^2 \cdot \frac{1 - |\Gamma_L|^2}{|1 - \Gamma_{out}\Gamma_L|^2} \tag{2.4}$$

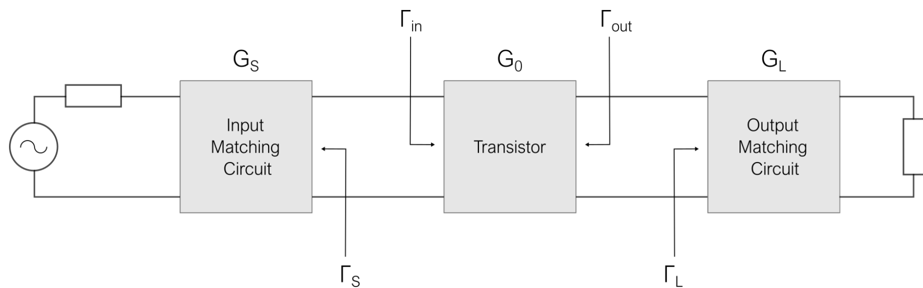


Figure 2.2: General amplifier with a transistor and in-/output matching circuits [2].

2.1.3 Gain compression

The power gain of an amplifier will gradually decrease as it leaves the linear region and enters saturation. This is known as compression, and as different power levels are amplified differently, it is a source of signal distortion. The point where the output power falls 1 dB below what is expected by an ideal linear amplifier is denoted as the 1 dB compression point or P1dB. Similarly, P3dB is where the output power falls 3 dB below the ideal response. This is illustrated in figure 2.3.

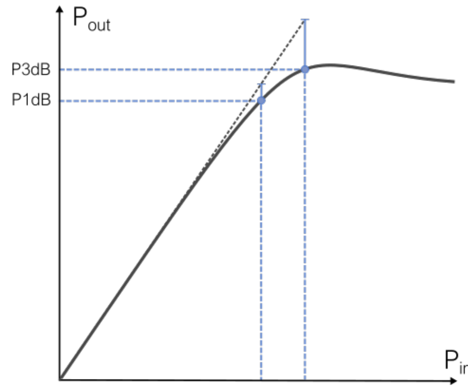


Figure 2.3: Sketch of P_{out} as P_{in} increases, compered with an ideal linear response. P1dB and P3dB is also marked.

2.1.4 Efficiency

Efficiency measures how well an amplifier utilises DC power when driving a load. The drain efficiency is a standard measure, which is the ratio between the delivered power and DC-power as shown in 2.5.

$$\eta = \frac{P_{out}^{RF}}{P^{DC}} \tag{2.5}$$

The power added efficiency is an alternative efficiency measure which accounts for the RF drive (P_{in}) as shown in equation 2.6. The same equation shows how it can be seen as the drain efficiency scaled with the power gain.

$$PAE = \frac{P_{out}^{RF} - P_{in}^{RF}}{P^{DC}} = \left(1 - \frac{1}{G}\right)\eta \tag{2.6}$$

The power dissipated to heat will depend on efficiency. The sum of P^{DC}, P_{in}^{RF}, P_{out}^{RF} and P_{diss} must be zero as consequence of the law of energy conservation. Consequently, the dissipated power can be found using equation 2.7.

$$P_{diss} = P^{DC} + P_{in}^{RF} - P_{out}^{RF} = P_{out}\left(1 - \frac{1}{G}\right)\left(\frac{1}{PAE} - 1\right) \tag{2.7}$$

The amplifier efficiency will vary as a function of the input power as sketched in figure 2.4, where the peak value is as it enters saturation. Consequently, the

overall efficiency of the amplifier depends on what the input signal looks like. If the signal has a high peak-to-average power ratio (PAPR), the input power must be reduced to avoid clipping the peak values. This results in reduced average efficiency, as shown in blue in figure 2.4. In addition, the signal might be reduced to minimise the gain compression of the signal due to high linearity demands. This is called an input power back off (IPBO) and results in a further decrease in efficiency as shown in red in figure 2.4.

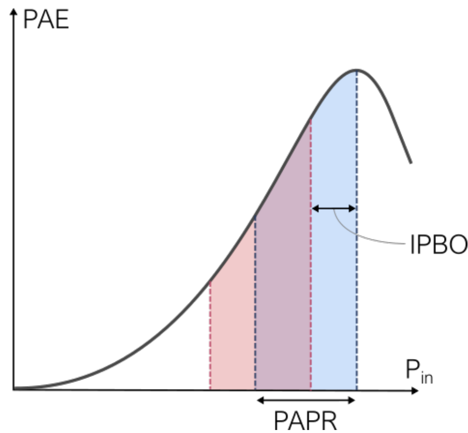


Figure 2.4: Sketch of how PAE changes with increasing P_{in}. The effect of PAPR and IPBO is also marked.

2.1.5 Amplifier classes

Amplifiers are divided into classes based on their operation. Class A, B and C are used for linear amplifiers where the conducting angle is altered for a trade-off between efficiency and distortion. Class D and E are cases of switching amplifiers, where the transistor switches between on and off to give high efficiency. Additionally, class F is used for amplifiers using harmonic tuning to increase efficiency. The following discussion will be limited to the linear amplifier classes A, B and C.

The class A amplifier has its operating point placed in the centre of the load-line as shown in figure 2.5. It will then conduct the entire signal period. A class B amplifier is instead placed at the cut-off point and only conducts for half of the period. This gives a drain efficiency of 78% compared to 50% for a class A amplifier [3, p.598]. However, this comes at the cost of reduced linearity. Class AB is a compromise between classes A and B, as it is biased to conduct between half and full signal period. Finally, class C is biased below cut-off, conducting for less than half period. The output power of class C is limited but has a potential high efficiency. The corresponding conducting angle and efficiency are summarised in table 2.1.

Table 2.1: Conduction angle and efficiency for class A, AB, B and C [3, p.598][2].

Class	Conduction angle	Theoretic efficiency
A	$\alpha = 2\pi$	50%
AB	$\pi < \alpha < 2\pi$	50-78%
B	$\alpha = \pi$	78%
C	$\alpha < \pi$	78-100%

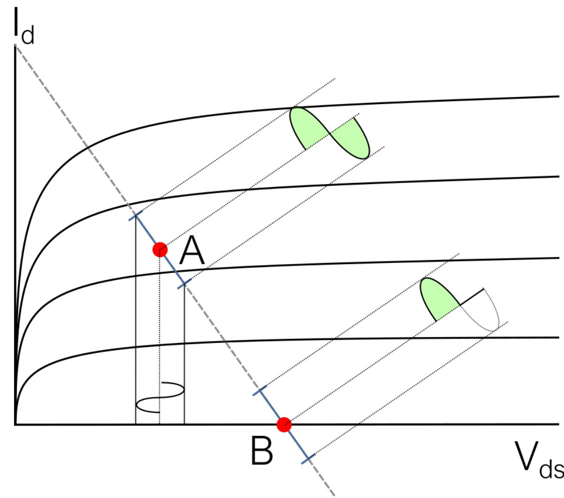


Figure 2.5: Load-line placement of class A and class B with corresponding conduction angle illustrated.

2.2 Amplifier stability

Stability analysis is a critical part of power amplifier design. The topic is complex and comprehensive and, therefore, only shortly introduced here to motivate the μ stability parameter and Admittance Analysis Method used later in section 4.4. [4] and [5] are recommended for a more comprehensive introduction.

In simple terms, an amplifier is said to be unstable if it is susceptible to oscillations. These oscillations are undesirable as they disturb the output spectrum and operation of the amplifier. In the worst case, they can also damage the system.

Feedback loop

An oscillation can occur as a consequence of a feedback loop, which can be found in power amplifiers due to, for instance, finite S_{12}, cross-talk between microstrip lines, or finite isolation between transistors in parallel. An ideal model of a feedback loop is shown in 2.6 and the corresponding transfer function in equation 2.8. This system will be unstable if the denominator of T(s) equals zero, as a non-zero output voltage can be achieved for a zero input voltage [3, p.606]. This analysis of a feedback loop is the base for more comprehensive analyses, such as the Nyquist Stability criterion and pole-zero analysis.

$$V_o(s) = T(s)V_i(s) = \frac{A}{1 + AH(s)} V_i(s) \tag{2.8}$$

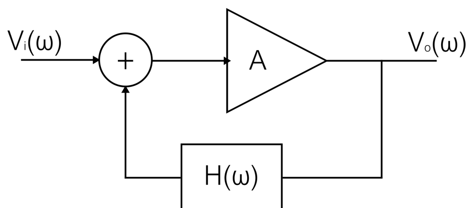


Figure 2.6: Block diagram illustration an feedback loop for an amplifier with gain A.

Negative resistance

An alternative way of viewing instabilities is to say that it occurs due to negative resistance in an active device. If a current runs through a negative resistance, it will deliver energy to the system, allowing an oscillation. This can be analysed by considering the simplified figure in 2.7, with an active device with impedance Z_{in} and a load Z_L. Kirchoff's voltage law implies that the sum of voltages around the closed-loop must equal zero, giving $(Z_L + Z_{in})I = 0$ [3, p.613]. In the case of an oscillation, $I \neq 0$, this demands that $R_L + R_{in} = 0$ and $X_L + X_{in} = 0$. A negative resistance will therefore be necessary if an oscillation were to occur. Consequently, the common practice in PA design is to design the system to avoid negative resistances and, by doing so, ensure stability.

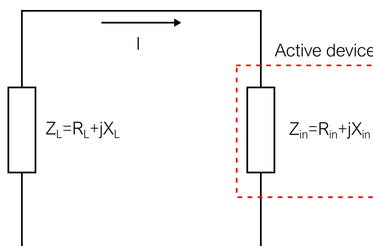


Figure 2.7: Example circuit to illustrate the negative resistance criteria.

2.2.1 μ stability parameter

Small signal analysis can analyse potential instabilities in the linear regime for different source- and load impedances. A amplifier can be susceptible for self-oscillation if $|\Gamma_{in}| > 1$ or $|\Gamma_{out}| > 1$. This would imply a negative resistance looking into the device, resulting in potential conditions for oscillation. Therefore, a goal of $|\Gamma_{in}| < 1$ or $|\Gamma_{out}| < 1$ ensure that the system is stable. An amplifier where this is fulfilled for all passive source and load impedances is said to be unconditionally stable. Alternatively, conditionally stable is used if it holds only for some source and load impedances.

The requirement for unconditional stability can be rewritten using S-parameters as shown in equation 2.9 and 2.10 [3, p.565], considering a circuit as in figure

2.2. These equations can be used to find find the potentially unstable regions in a smith chart.

$$\left|\Gamma_{in}\right| = \left|S_{11} + \frac{S_{12}S_{21}\Gamma_L}{1 - S_{22}\Gamma_L}\right| < 1 \tag{2.9}$$

$$\left|\Gamma_{out}\right| = \left|S_{22} + \frac{S_{12}S_{21}\Gamma_S}{1 - S_{11}\Gamma_S}\right| < 1 \tag{2.10}$$

The stability parameter μ shown in 2.11 can be used as a test to decide if a linear 2-port circuit is unconditionally stable [6]. It is a geometrically derived parameter that finds the minimum distance between the origo of the smith chart and the unstable region given by equation 2.10. The circuit will, as a consequence, be unconditionally stable if $\mu > 1$. A companion parameter μ^* is defined similarly for the source. The advantage of using μ over alternatives such as the Rollet criteria [7] is that μ also gives a measure of how stable a device is, not only if it is unconditionally stable or not.

$$\begin{aligned} \mu &= \frac{1 - \left|S_{11}\right|^2}{\left|S_{22} - \Delta S_{11}^*\right| + \left|S_{12}S_{21}\right|} \\ \Delta &= S_{11}S_{22} - S_{12}S_{21} \end{aligned} \tag{2.11}$$

2.2.2 Admittance Analysis Method

Power amplifiers that are stable in the small-signal regime can potentially still be unstable in the presence of an RF drive, especially when multiple transistors are placed in parallel. The presence of an RF drive can, for instance, provoke instabilities due to mismatch between transistors characteristics and finite isolation between transistors in parallel, giving a feedback loop. A method for analysing stability in the non-linear regime is therefore necessary.

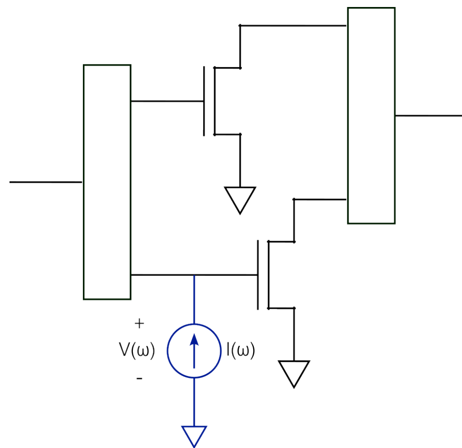


Figure 2.8: Illustration of a small-signal source used to measure the addmitance at the gate.

The Admittance Analysis Method utilises a ideal small-signal current source, as shown in figure 2.8, to measure the admittance in a node, $Y(f) = \frac{I(f)}{V(f)}$. The admittance can then be analysed to examine if a negative resistance is present and if the condition for oscillations, shown in equation 2.12, are fulfilled. The demand for a positive derivative of $Img\Big(Y(\omega_c)\Big)$ is necessary for a stable oscillation, which is further explained in [5].

The analysis should be performed on a wide range of different power levels and frequencies to ensure stability. It should also be performed at different nodes to consider different loops and sources of negative resistance. However, the nodes closest to the active device are most influential as the negative resistance is most likely to be found here.

$$\begin{aligned} Re\big\{Y(\omega_c)\big\} &< 0 \\ Img\big\{Y(\omega_c)\big\} &= 0 \\ \frac{\delta}{\delta\omega_c} Img\big\{Y(\omega_c)\big\} &> 0 \end{aligned} \tag{2.12}$$

2.3 Transmission Line Theory

Transmission line effects have to be considered at radio frequencies (RF). Figure 2.9 shows a general model for a transmission line with length Δz. The Telegraphers equation shown in equation 2.13 is a differential equation that describes the voltage and current on this line [8, p.439]. Here γ is the propagation constant given in equation 2.14.

$$\frac{\delta^2 V(x)}{\delta^2} = \gamma^2 V(x) \qquad \frac{\delta^2 I(x)}{\delta^2} = \gamma^2 I(x) \tag{2.13}$$

$$\gamma = \alpha + j\beta = \sqrt{(R + j\omega L)(G + j\omega C)} \tag{2.14}$$

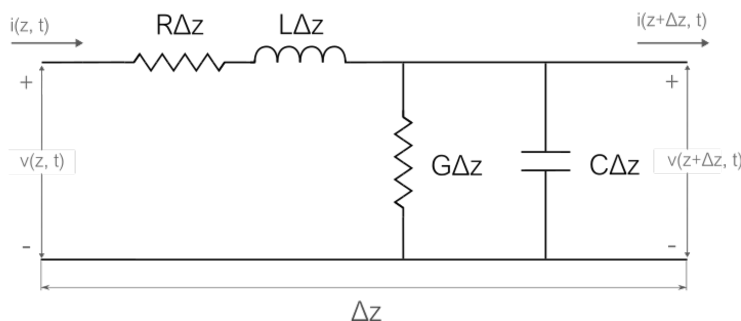


Figure 2.9: General model for transmission line with length Δz used as basis for the Telegraphers equation [2].

Equation 2.15 shows the general solution to the telegraphers equation [8, p.439]. Here Z_0 is the line's characteristic impedance, given in 2.16. The solution will

be the sum of an incident and a reflected wave, which is a motivation behind the setup of the S-parameters in section 2.1.1.

$$\begin{aligned} V(x) &= V^+ e^{-\gamma x} + V^- e^{\gamma x} \\ I(x) = \frac{V(x)}{Z_0} &= \frac{1}{Z_0} V^+ e^{-\gamma x} + V^- e^{\gamma x} \end{aligned} \tag{2.15}$$

$$Z_0 = \sqrt{\frac{R + j\omega L}{G + j\omega C}} \tag{2.16}$$

The reflection coefficient is the ratio between the incident and reflected wave, as shown in equation 2.17.

$$\Gamma = \frac{V^-}{V^+} \tag{2.17}$$

Impedance matching using transmission lines

The input impedance seen from a transmission line will be given by equation 2.18 [8, p.451]. Rewriting for Γ_L one get equation 2.19. Here, it is seen that impedance seen at the input of the line can be changed by adjusting the characteristic impedance Z_0 and transmission line length, l. In this way, a transmission line can be used in impedance matching.

$$Z_{in}(l) = \frac{V(l)}{I(l)} = Z_0 \frac{1 + \Gamma_L e^{-2\gamma l}}{1 - \Gamma_L e^{-2\gamma l}} \tag{2.18}$$

$$Z_{in}(l) = Z_0 \frac{Z_L + Z_0 \tanh \gamma l}{Z_0 + Z_L \tanh \gamma l} \tag{2.19}$$

Microstrip lines

The microstrip is a simple transmission line where a conductor is placed over a ground plane, separated by a substrate. This line is convenient as it easily can be produced on a printed circuit board. A cross-section of a microstrip is shown in figure 2.10.

Table 2.2 summarises the parameters used to characterise the microstrip transmission line. The substrate is mainly characterised by ϵ_r, $tan\delta$ and h. The relative dielectric constant, ϵ_r, describes the permittivity of the substrate. An electric field will polarise a substrate with high permittivity more easily than a substrate with low permittivity [8, p.110]. The dissipation factor, $tan\delta$, describes the loss seen by the electric field in the substrate. In practice, the substrate height is a scaling factor for these parameters. The permeability of the substrate is generally not of interest and therefore ignored.

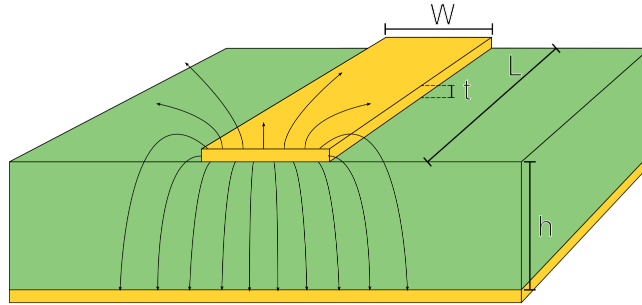


Figure 2.10: Microstrip line with dimension parameters. The fringing fields are also sketched.

Table 2.2: Summary of substrate parameters

Parameter	Unit	Description
ϵ_r	-	*Relative dielectric constant*
$tan\delta$	-	*Loss tangent*
h	m	*Substrate height*
W	m	*Transmission line width*
L	m	*Transmission line length*
t	m	*Transmission line thickness*
C	$W/(m \cdot K)$	*Conductor conductivity*

The transmission line width and substrate height are the most critical design parameters for setting the transmission line's characteristic impedance. The conductor thickness and conductivity describe the loss of the line.

A microstrip line will have fringing fields around the edges and at discontinuities in the line. This is sketched in figure 2.10. These fringing fields lead to some important effects : First, these fringing fields must be kept in mind when realising the circuit to reduce unwanted cross-talk. Secondly, the fringing fields at discontinuities give an effect similar to capacitance to ground. This *fringing capacitance* will give a slight deviation from the ideal transmission line behaviour [3, p.226]. Finally, the field will stretch outside the transmission line width as sketched in figure 2.10. This can be modelled as if the conductor is surrounded by a homogeneous substrate with a new effective dielectric constant. This new effective dielectric constant results in a new effective width of the line and a corresponding change in the characteristic impedance [3, p.148]. It is possible to use this model as the microstrip line in practice will have quasi-TEM fields. The three effects discussed above are considered in transmission line models, such as the Kirchning model used in ADS microstrip simulations [9].

2.4 Thermal analysis

2.4.1 Thermal conduction and - resistance

Fourier's law of heat conduction, shown in equation 2.20 describes the condition of heat through a medium[10]. Here, k is the thermal conductivity which describes how well the heat is transported. Assuming an isotropic medium allows rewriting the well-known heat equation shown in equation 2.21. α is the thermal diffusivity, which is the thermal conductivity divided by the medium's density and specific heat capacity.

$$\mathbf{q} = -\mathbf{k}\nabla\mathbf{T} \tag{2.20}$$

$$\frac{\delta T}{\delta t} = \alpha \nabla^2 T \tag{2.21}$$

Thermal resistance is the reciprocal of thermal conductance and describes the heat transfer in a steady-state. Looking at equation 2.20, the thermal resistance can be written as $R_\theta = \frac{\Delta T}{q}$. Considering the heat transfer through a cross-section, the specific thermal resistance can be calculated using equation 2.22[10]. Hera A is the cross-section area, and t is the thickness. The absolute thermal resistance is used to describe a component's steady-state thermal performance using measurements. Here R describes the ratio of temperature increase as a function of power as shown in equation 2.23. The thermal resistance additionally depends on the temperature. The thermal conductivity of a good conductor will decrease with increasing temperature [11]. The thermal resistance will then increase.

$$R_\theta = \frac{t}{kA} \tag{2.22}$$

$$\Delta T = R_\theta P \tag{2.23}$$

2.4.2 Thermal capacitance

Heat capacity describes how well heat is stored in a material, as shown in equation 2.24 [12]. Similarly, the specific heat capacity is defined as the heat capacity divided by mass. The capacitance is essential to describe a system's dynamic thermal behaviour and is accounted for in the thermal diffusivity in equation 2.21.

$$C = \lim_{\Delta T \to 0} \frac{\Delta Q}{\Delta T} \tag{2.24}$$

2.4.3 Thermal equivalent circuit models

The heat flow can be analysed using an equivalent electrical circuit using the definitions of thermal resistance and - capacitance from section 2.4.1 and 2.4.2. An equivalent circuit is driven by a current, which is the power flow, or a voltage which is the temperature. This is possible as Fourier's law in 2.20 is analogous to Ohm's law used as a basis for electronic circuit theory. This results in an analogy between thermal and electrical parameters as shown in table 2.3. The advantage of an equivalent thermal circuit is that it allows the use of known methods of analysis from electrical engineering. There is, however, not a perfect analogy due to differences in boundary conditions which is further discussed in [13].

Table 2.3: Overview of parameters used in this section and their electrical counterparts[14].

Parameter	Variable	Unit	Electrical analogy
Heat	Q	J	Charge, q
Temperature	T	K	Potential, V
Heat transfer rate / power	$\dot{Q}$ /P	W	Current, I
Heat flux density	q	W/m^2	Current density, j
Thermal resistance	R	K/W	Electrical resistance, R
Thermal conductance	G	W/K	Electrical conductance, G
Thermal resistivity	-	$(m \cdot K)/W$	Electrical resistivity , ρ
Thermal conductivity	k	$W/(m \cdot K)$	Electrical conductivity, σ

2.5 Thermal considerations for PA Transistors

2.5.1 Self heating effects

Heat is generated in a transistor due to channel resistance, ohmic contacts and more. Self-heating is an effect occurring when this dissipated heat/power, P_{diss}, exceeds what can be dissipated through the substrate. Then the junction temperature increases as a function of the dissipated power, resulting in a change in electrical performance.

The temperature due to self-heating can be estimated using an equivalent thermal circuit, as shown in figure 2.13. The thermal resistance, R_θ, and thermal capacitance, C_θ, are described using ideal circuit elements. The current that drives the circuit is the dissipated power from the transistor, P_{diss}. The implications of this model will be discussed further in the following subsections.

Thermal resistance and derating

The thermal resistance in the self-heating model describes how well the heat is conducted away from the junction in a steady state. It is measured as the temperature difference against a global reference temperature, T_0. T_0 can, for instance, be the temperature at the transistor case. It can be used to estimate the junction temperature using equation 2.25.

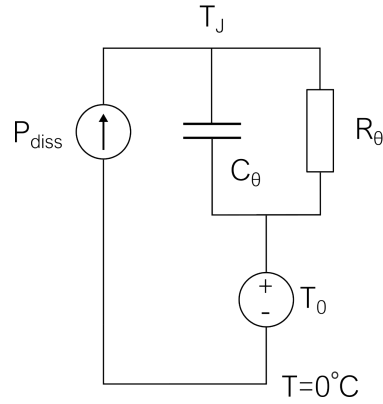


Figure 2.11: Equivalent thermal circuit used to model self heating.

$$T_j = T_0 + R_\theta \cdot P_{diss} \tag{2.25}$$

Assuming a maximum junction temperature, T_{jmax}, equation 2.26 gives the maximum allowable power dissipation as a function of T_0. Based on equation 2.7, this is also a limit of the maximum allowable output power or minimum efficiency. The reference temperature, T_0, can be set by the transistor mounting, as discussed later in section 2.5.2.

$$P_{diss} = \frac{T_{jmax} - T_0}{R_\theta} \tag{2.26}$$

Equation 2.26 can be used to define a derating curve, as shown in 2.12. Here, we have three cases:

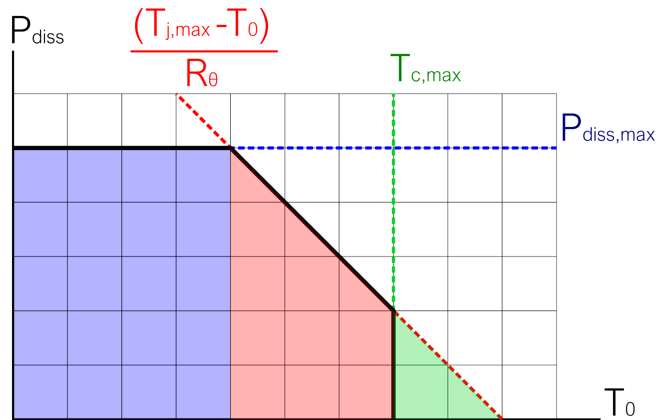


Figure 2.12: Example of a derating curve.

Case 1: No thermal limitations

The first case, marked in blue, is where T_0 is sufficiently low so that the dissipated power is only limited by the maximum delivered power by the transistor.

Case 2: Derating of P_{diss}

The dissipated power must be reduced if reference temperature T_0 is too high to avoid exceeding the maximum junction temperature. This is known as power derating and is seen in the red case in figure 2.12.

Case 3: Outside safe operation

The third case, marked in green, is where T_0 is outside the safe operating temperature of the circuit. This is a limit set due to reliability concerns for the transistor package.

Thermal capacitance and dynamic thermal effects

The thermal capacitance forms an RC-circuit together with R_θ. The equivalent circuit will consequently have a rise-time and frequency response which can be analysed using known equations from electronic RC-circuit analysis. For instance, the step-response can be found by 2.27, where $\tau = R_\theta C_\theta$. The RC circuit will also operate as a low-pass filter with cut-off frequency $\omega_c = \frac{1}{R_\theta C_\theta}$. Consequently, the circuit will behave differently for pulsed and constant waveform signals, where constant waveform will provide the worst case.

$$T = T_0\left(1 - e^{-\frac{t}{\tau}}\right) \tag{2.27}$$

2.5.2 Package and mounting

We will consider a backplate-cooled transistor package mounted on a metal baseplate with a heatsink underneath. The transistor package is designed so that the majority of the heat goes to the baseplate through the case. The heat through the baseplate can be estimated using a proportional constant, , as shown in equation 2.28. Here $P_{ambient}$ is used for the heat going other ways as, for instance, to the air, substrate and microstrip line.

$$P_{baseplate} = \left(\frac{P_{diss} - P_{ambient}}{P_{diss}}\right) \cdot P_{diss} = \kappa \cdot P_{diss} \tag{2.28}$$

It is necessary to consider the environment around the transistor package to estimate the case temperature. Figure 3.3 shows a typical configuration with the PA transistor mounted on a baseplate with a heatsink underneath. An equivalent circuit for the heat transfer through the baseplate and heatsink to the ambient is shown in figure 2.13. The thermal interface resistances, R_i, are added in the interface above and under the baseplate. This resistance is used to model the imperfect connection between the materials. As it is a series resistance, it is desirable that it is as low as possible to reduce temperature increase. Consequently, low-resistance thermal interface materials are typically used.

The baseplate serves two primary purposes; (1) to give mechanical support to the circuit board and (2) to spread the heat, making it easier to dissipate in the heatsink. The baseplate thickness will compromise these purposes and increased cost and weight. Typically a mechanical engineer will be responsible for designing

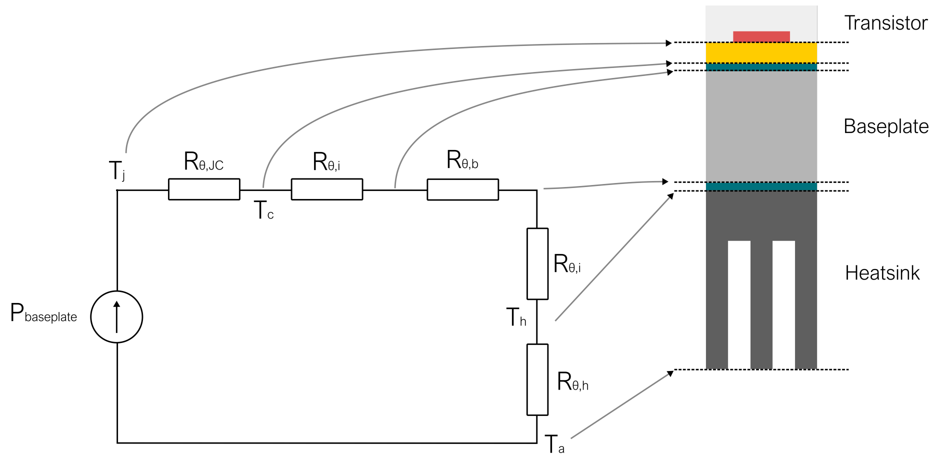


Figure 2.13: Equivalent circuit for the transistor package mounted on a baseplate.

the heatsink and ambient environment of the circuit. So for an electrical engineer, it will be interesting to design the circuit to handle a maximum temperature at the bottom of the baseplate, $T_{B\ max}$. Then the mechanical engineer has to design the environment such that the cooling is sufficient to maintain a maximum of $T_{B\ max}$. Given a $T_{B\ max}$, this allows us to estimate the junction temperature using equation 2.29. This can again be rewritten to find the maximum dissipated power possible, shown in equation 2.30. This equation shows the key design parameters, which will be discussed further in section 3.

$$T_j = \kappa(R_{\theta,i} + R_{\theta,B} + R_{\theta,JC}) \cdot P_{diss} + T_{Bb} \tag{2.29}$$

$$P_{max\ diss} = \frac{T_{jmax} - T_{Bbmax}}{\kappa(R_{\theta,i} + R_{\theta,B} + R_{\theta,JC})} \tag{2.30}$$

2.6 Power combining

Power combination is central in the realisation of a distributed topology. A simple configuration is shown in figure 2.14, where a divider is used to split the signal into two branches and a combiner that combines them at the output. A phase difference ϕ can be used between the branches, as will be discussed in section 2.6.3 and 2.6.4.

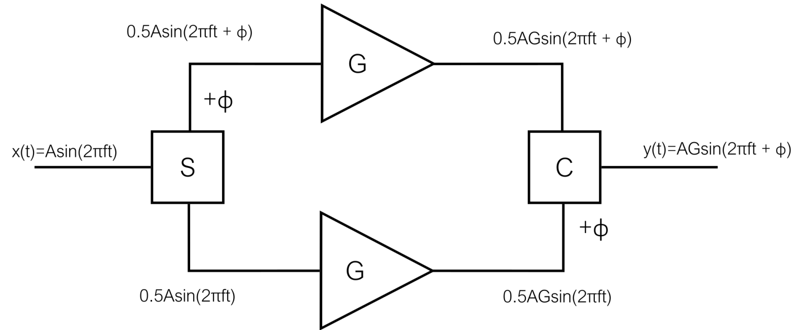


Figure 2.14: Example of a configuration where power combining is used for two branches, with equal power division and a phase difference, ϕ, between.

2.6.1 T-junction

It can be shown that a passive coupler cannot be reciprocal, lossless and matched at all ports [3, p.318]. Consequently, a division is done between lossless and resistive dividers. A lossless divider can be realised by combining three transmission lines, as shown by figure 2.15. A T-junction is the simplest case of such a divider/combiner. Assuming an ideal lossless case, input can be matched if equation 2.31 is fulfilled [3, p.325]. For an equal power split, it is then necessary that $Z_1 = Z_2 = 2Z_0$, giving a two-time increase in impedance. When using a lossless divider, there is no isolation or match for the output ports. Matching for all ports can be achieved using a resistive divider, where loss is used [3, p.326].

$$Y_{in} = \frac{1}{Z_1} + \frac{1}{Z_2} = \frac{1}{Z_0} \tag{2.31}$$

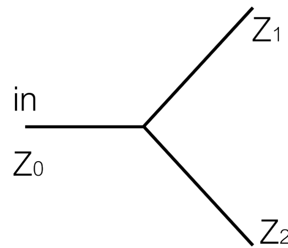


Figure 2.15: Three port lossless divider, where three transmission lines with characteristic impedance Z_0, Z_1 and Z_2 are combined.

2.6.2 Wilkinson couplers

The Wilkinson Power Divider is a common restive divider, which provides matching at all ports and isolation between the output ports. In addition, it will appear lossless if it is matched at the output and, in that case, only dissipate reflections from the output ports [3, p. 328].

A sketch of a Wilkinson divider is shown in figure 2.16. Here, two branches with length $\lambda/2$ and characteristic impedance $\sqrt{2}Z_0$ are used to split the signal with

a $2Z_0$ resistor placed between the branches. [3, p. 328] is recommended for a more in-depth analysis.

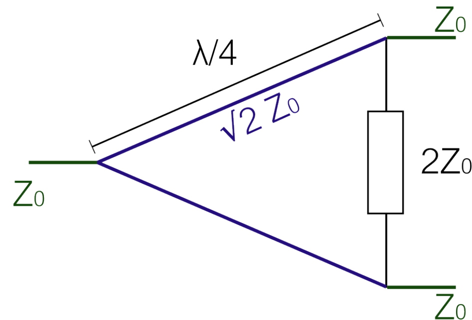


Figure 2.16: Wilkinson Power Divider.

2.6.3 Balanced amplifier

A balanced amplifier is an amplifier that combines two amplifiers with a 90° phase difference using a quadrature splitter/combiner. The significant advantage of the quadrature combination is that it cancels the output reflection coefficients from the device [3]. Consequently, the amplifier will seem well-matched from the input ports, even though the internal amplifiers are mismatched for maximum power. The isolation given by a quadrature combiner is in addition advantageous for stability. This configuration is commonly used in millimetre wave designs [15].

2.6.4 Push-pull amplifier

A push-pull amplifier is an amplifier where two amplifiers are combined with a 180° phase difference using a hybrid splitter/combiner. The 180° difference is advantageous as the two branches' differential operation helps cancel distortion from the amplifiers. This configuration is commonly used for amplifiers operating below 500 MHz [15].

2.7 Circuit simulation

2.7.1 Harmonic balance

Harmonic balance is a frequency-domain technique for simulating distortion in non-linear systems [16]. It assumes a steady-state solution that can be approximated using a finite Fourier series. The method essentially adjusts the current- and voltage sinusoidal of fundamental and harmonics until Kirchhoff's laws are fulfilled.

2.7.2 Optimisation

Parameter optimisation is an algorithmic method to find the optimal parameter values to reach a set goal. Here a residual is defined as the difference between the simulated result and the goal. An error function is defined as the sum of

residuals, as shown in equation 2.32, and optimisation aims to minimise this. The weight, W_i, can be adjusted to prioritise specific goals.

$$EF = \sum_{i=0}^{N_{goals}} W_i \cdot \left|simulation_i - goal_i\right|^P \tag{2.32}$$

The Least-Squares Error Function is a popular case where the residual power, P, is set to 2. ADS provides a series of optimisation algorithms, where the two most common are random search and gradient descent.

Random search

Algorithm that uses a random number generator to find new parameter values and calculates the error function for these new values. The new parameters are kept as the initial value for the next iteration if the error function is lower than the initial value. If not, the values are discarded.

Gradient descent

Algorithm that calculates the gradient of the error function and uses this to find which direction it should change the parameters to find an optimum. Parameters are then changed in this direction for the next iteration.

A gradient descent demands more computing time to find new parameters than a random search. It does, however, often need fewer iterations in order to find an optimum. A gradient descent only guarantees that we find an optimum, not necessarily the global optimum. However, a random search is more likely to hit close to the global optimum if run at an appropriate amount of time but does not guarantee to hit precisely. It is, therefore, common to combine the two using the random search algorithm to get close to the global optimum and then the gradient descent to find the optimum. This is unnecessary, assuming that the initial values are close to the optimal.

Chapter 3

Heat conduction through baseplate

This chapter introduces a simple method for estimating the junction temperature for multiple transistors mounted on the same baseplate. The method is based on work done by Associate Professor Morten Olavsbråten on estimating the thermal resistance in a GaAs HBT transistor [17] [18]. A similar analysis is performed in [19], [20]. The advantage of this method is that it allows for quick design assessments without setting up complex and time-consuming simulations. The goal here is not to give a highly accurate estimation of the junction temperature but to show the implication of heat conduction through the baseplate and discuss if a distributed topology is beneficial as a thermal management technique.

3.1 Simplified model

3.1.1 Theoretical background

The heat equation in 3.1 can be used to describe the temperature distribution in the baseplate. Here T is the temperature at a point in space represented by $\vec{s}$ and P is the power dissipated to the plate. α is the thermal diffusivity, and k is the thermal conduction of the metal plate. Assuming steady-state, that is $\frac{\delta T}{\delta t} = 0$, allows us to rewrite the equation to Poisson's equation in 3.2.

$$\frac{\delta T(\vec{s},t)}{\delta t} = \alpha \nabla^2 T(\vec{s},t) + \frac{\alpha}{k} P(\vec{s},t) \tag{3.1}$$

$$\nabla^2 T(\vec{s}) = -\frac{P(\vec{s})}{k} \tag{3.2}$$

The thermal conduction is here assumed to be independent of temperature. Metals generally has a linear dependence, as discussed in 2.4.1. However, coefficients are low for the alternative baseplate materials. Ignoring the temperature dependence is therefore assumed to give little error.

Equation 3.3 shows a solution for 3.2 giving the temperature in $\vec{s_p} = (x, y, z)$ given a point source in $\vec{s_s} = (x_0, y_0, z_0)$. This solution assumes a infinite plate.

$$T_{point}(x, y, z, x_0, y_0, z_0) = \frac{P}{2\pi k\sqrt{(x-x_0)^2 + (y-y_0)^2 + (z-z_0)^2}} \tag{3.3}$$

The transistor is simplified to an ideal rectangular heat source dissipating a power P, which is placed on the top of the baseplate as shown in figure 3.1.

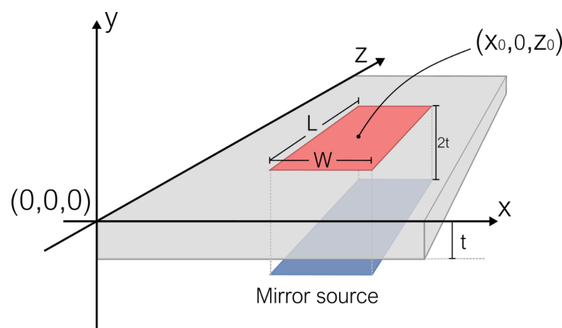


Figure 3.1: The coordinate system with model parameters.

The temperature increase due to the heat dissipated by a transistor, T_Q, at a point (x,0,z) on the top of the plate can be found by the integral in equation 3.4.

$$T_Q(x, z) = \frac{1}{LW}\int_L\int_W T_{point}(x, z, x_0', z_0')dx_0'dz_0' \tag{3.4}$$

The baseplate is assumed to be connected to an ideal heat sink giving a uniform temperature of $0°C$ at the bottom of the plate. This boundary condition is modelled by adding a mirror source at $y = -2 \times t$ with equal but negative power. The sum of the transistor and the mirror source will then be zero at $y = -t$.

The final temperature distribution on the top of the plate is found by summarising the contribution of the N transistor mounted to the plate. The contribution is the sum of the rectangle, T_Q, and mirror source T_M as shown in equation 3.5. The ambient temperature, T_a, is added to correct the simplification of $T = 0°C$ at the bottom of the baseplate.

$$T_{top}(x, z) = T_a + \sum_{n=0}^{N}\left(T_{Q,n}(x, z) + T_{M,n}(x, z)\right) \tag{3.5}$$

Finally, the case temperature can be estimated using two approaches: (a) Integrating over the area of the transistors to find the average temperature as shown in 3.6, or (b) taking the maximum temperature within the rectangle. The choice of method depends on how $R_{\theta JC}$ is measured. (b) is used in later simulations as it is a standard measure [21]. It will also give the worst-case solution.

$$T_c = \frac{1}{LW} \int_L \int_W T_{top}(x', z') dx' dz' \tag{3.6}$$

The junction temperature T_j can at the end be estimated using the thermal resistance between the junction and case, $R_{\theta JC}$, as shown in 3.7.

$$T_j = T_c + R_{\theta JC} \cdot P_{diss} \tag{3.7}$$

3.1.2 Implementation

Simulations are performed numerically using a python script [1]. The calculation of T_Q is accelerated using an analytical solution from [18]. This expression gives T_Q, not T_J, as stated in the thesis. Analytical expressions are more difficult for the mirror sources, as $y \neq 0$. Numerical integration is therefore implemented for mirror sources.

$$\begin{aligned} T_Q = \frac{P}{2\pi k LW} \Bigg\{ & A_2 \left[\sinh^{-1}\left(\frac{B_2}{|A_2|}\right) - \sinh^{-1}\left(\frac{B_1}{|A_2|}\right) \right] \\ & -A_1 \left[\sinh^{-1}\left(\frac{B_2}{|A_1|}\right) - \sinh^{-1}\left(\frac{B_1}{|A_1|}\right) \right] \\ & +B_2 \left[\sinh^{-1}\left(\frac{A_2}{|B_2|}\right) - \sinh^{-1}\left(\frac{A_1}{|B_2|}\right) \right] \\ & -B_1 \left[\sinh^{-1}\left(\frac{A_2}{|B_1|}\right) - \sinh^{-1}\left(\frac{A_1}{|B_1|}\right) \right] \Bigg\} \end{aligned} \tag{3.8}$$

Simulations are performed for a set view area, where the temperature is found for a number of points per millimetre. The number of points defines the resolution. Figure 3.2 shows the simulated average case temperature for different values of points per millimetre. It shows that the temperature converges for an increased number of points. Simulations in this chapter are done using 5 points per millimetre, which is a good compromise between accuracy and time consumption. The maximum case temperature is consistent for different point values, as it depends less on the exact position.

[1] The implemented code is published on GitHub: https://github.com/Tobiaskri/heat-distribution-baseplate

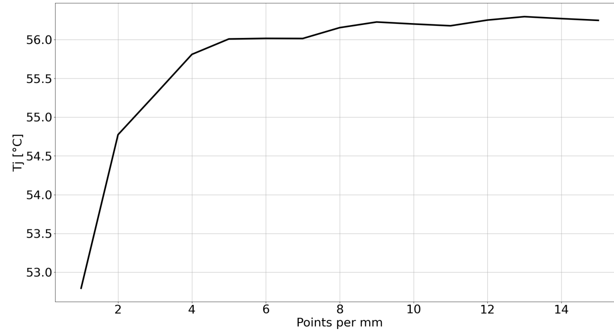


Figure 3.2: Simulated junction temperature for different number of points per mm.

The numerical integration of the mirror sources can be time-consuming, especially for a high number of points per millimetre. The mirror source can be simplified to a point source, for some loss in accuracy but a drastic reduction in time consumption. Simulations show that these simplifications lead to xx-yy % change in results. The accurate integration is used in later simulations. However, simplification can be helpful for quick design assessments.

3.2 Design parameters

This section concerns the impact of the design parameters for transistors placed on a baseplate. The discussion will be based on parameter-sweeps using the simulation case in table 3.1.

Table 3.1: Simulations parameters used in this section.

Parameter	Value	Unit
Transistors	2	-
Dissipated power	50	W
Plate thickness	10	mm
Thermal conductivity	238	$W/°C$
Ambient temperature	25	$°C$

Transistor distance

The distance between the two transistors is an important parameter. Temperature increases with the distance between the transistor as a consequence of equation 3.3. It implies that the junction temperature in the transistor will be a function of the distance to the other transistors on the baseplate. Figure 3.3 shows that the junction temperature decreases similar to $1/d$ with increasing distance between the two-transistor, as expected. As the distance increases, the thermal coupling between the transistors becomes neglectable compared to the baseplate thermal resistance. There is, therefore, no gain from increasing the distance further in that case.

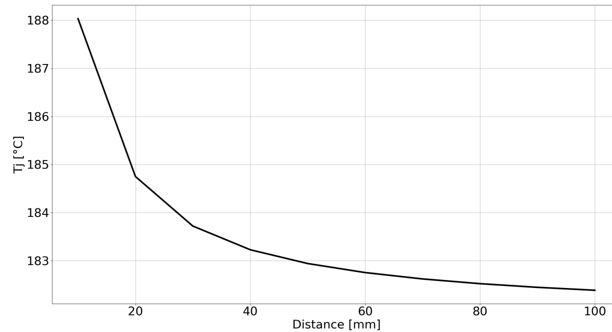


Figure 3.3: Simulated T_J for two transistors for different distances between the centre of the transistors.

Plate thickness

The baseplate thickness is another design parameter impacting the temperature increase. The thermal resistance of the baseplate increases as a function of the thickness, as seen by equation 2.22, resulting in increased temperature. A sweep of the thickness shown in figure 3.4 shows that the temperature increases with thickness like $C(1-1/t)$. Therefore, a thin baseplate is preferably due to the low thermal resistance. However, as an impact of equation 3.3, we see that increasing thickness will spread the heat to a larger area at the bottom of the baseplate, which is beneficial when considering the cooling of the system. The thickness will therefore be a trade-off.

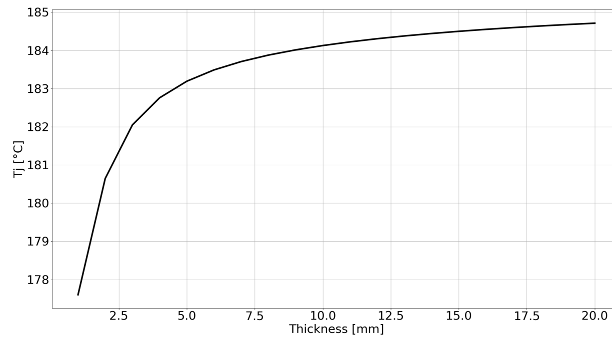


Figure 3.4: Simulated T_J for swept thickness.

Thermal conductivity

The thermal conductivity of the baseplate can be seen in the denominator of equation 2.22 and 3.3. Therefore, it is beneficial with a material with high thermal conductivity to reduce the temperature increase. The sweep of k in figure 3.5 shows that thermal conductivity above 200 $W/°C$ is preferable. Aluminium is commonly used due to it is good conductivity and reasonable price. However,

for instance, copper can be used to get higher conductivity.

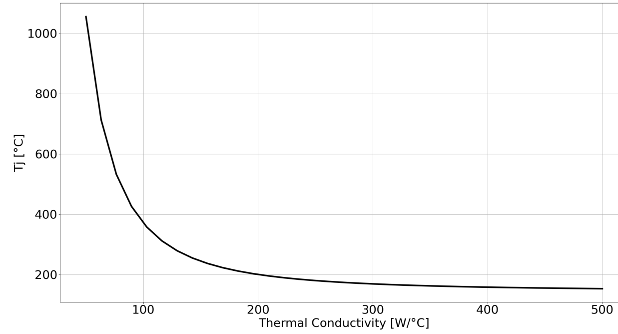


Figure 3.5: Simulated T_J for different values of thermal conductivity.

Transistor angle

Since the transistor is rectangular, the constellations will slightly depend on the angle between the transistors. There will be a larger contribution towards the axis along the broadside. A 180° sweep of the angle is performed in figure 3.7 using the setup in figure 3.6. Here a transistor is turned around in a circle around the other transistor with a given radius d, for a sweep of α. The result shows that the lowest temperature is when transistors are placed with the broadside towards each other as expected. However, there is only a 0.04°C difference between the top and bottom. The angle can therefore be assumed to have a limited impact. In practice, the screw used to mount the transistor might limit the difference even further.

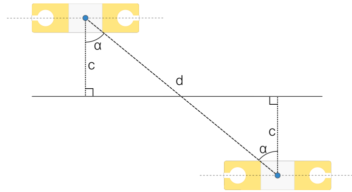


Figure 3.6: Illustration of the angular sweep setup.

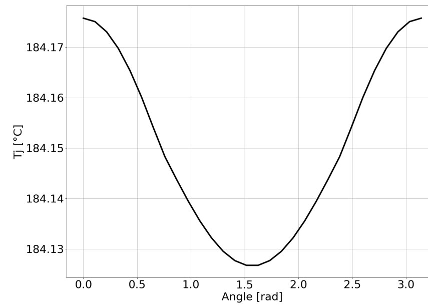


Figure 3.7: Simulated T_J for two transistors for different angles between them.

3.3 Evaluation of different topologies

This section will introduce an example to discuss the advantages of a distributed topology. The realisation of a 100W amplifier will be considered by using four 25W transistors, two 50W transistors or a single 100W transistor. Parameters from the Wolfspeed transistors given in table 3.2 are considered. The thermal resistance between the transistor junction and case, $R_{\theta JC}$, decreases as the transistor size increases. This decrease is simply due to the increased area of the transistor, which eases heat conduction as seen by equation 2.22. All transistors have a maximum operating junction temperature of $225°C$ [22]–[24].

Table 3.2: The Wolfspeed transistors which the simulations are based on, and their corresponding parameters [22]–[24].

P_{del}	Name	$R_{\theta JC}$ $[°C/W]$	L [mm]	W [mm]
100W	CG2H40120F	1.39	14.3	5.8
50W	CG2H40045F	2.8	14.3	5.8
25W	CG2H40025F	4.8	9.5	4.1

The junction temperature is found for five different efficiency values in table 3.3. The corresponding dissipated power is found using equation 2.7 for an output power of 100W and 14 dB gain. The transistors are placed on a line with a 25 mm distance between the centres, as shown in figure 3.8 (a).

The results in table 3.3 show that the estimated junction temperature decreases as the number of transistors increases. This effect is more noticeable as the dissipated power increases. The cases with two and four transistors can operate with an efficiency of 50% PAE in table 3.3 (a), something that is not possible with one transistor. The case with four transistors has a $30.4°C$ decrease in junction temperature compared to the case with two transistors in the 50% case in table 3.3 (a). This decrease in junction temperature benefits the transistor's performance and general reliability.

The table 3.3 (b) also show that the increased thermal conductivity of copper leads to a decreased case temperature. It is also an apparent decrease in the temperature difference between the centre and edge transistors for four transistors. Therefore, the thermal coupling of the transistors is lower or more equal in the case of higher thermal conductivity.

Table 3.3: Simulated temperatures for a 100W amplifier realised by one, two or four transistors on 10 mm thick aluminium and cooper plates. Transistors from table 3.2 are used and are placed on a horizontal line with 25 mm distance between the centres. The dissipated power is estimated for five levels of PAE using equation 2.7 for 100W delivered power and 14 dB gain. The ambient temperature is $T_a = 25°C$. "-" is used to mark the difference between centre and edge transistors in case 3.

(a) Aluminium plate

PAE	Pdiss [W]	Case 1: 1x100W		Case 2: 2x50W		Case 3: 4x25W	
		TC [°C]	TJ [°C]	TC [°C]	TJ [°C]	TC [°C]	TJ [°C]
70%	41.00	65.70	122.60	47.30	104.70	41.8-42.5	91.0-91.6
60%	63.80	88.20	176.70	59.70	148.90	51.1-52.1	127.7-128.7
50%	95.60	119.70	252.80	77.00	210.90	64.2-65.7	179.0-180.5
40%	143.50	167.30	366.70	103.00	303.90	83.8-86.1	256.0-258.2
30%	223.20	246.30	556.50	146.40	458.80	116.5-120.0	384.3-387.8

(b) Copper plate

PAE	Pdiss [W]	Case 1: 1x100W		Case 2: 2x50W		Case 3: 4x25W	
		TC [°C]	TJ [°C]	TC [°C]	TJ [°C]	TC [°C]	TJ [°C]
70%	41	39,0	96,0	32,6	90,0	30,7-30,9	79,9-80,1
60%	63,8	46,8	135,4	36,8	126,1	33,9-34,2	110,4-110,7
50%	95,6	57,6	190,6	42,3	176,2	38,4-38,8	153,1-153,6
40%	143,5	74,0	273,4	51,5	252,4	45,1-45,8	217,2-217,9
30%	223,2	101,2	411,3	66,3	378,7	56,2-57,3	324,0-325,1

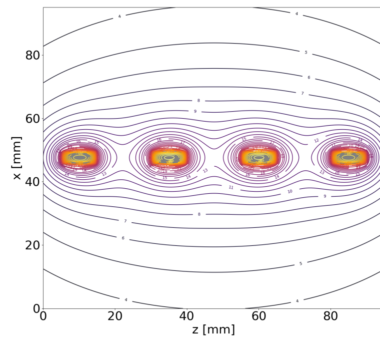
3.4 Alternative constellations for reducing thermal crosstalk

Temperature differences between transistors can be a challenge when assessing constellations of three or more transistors. This is visible for the transistors placed at a line in figure 3.8 (a). Here the centre transistors operate one contour higher due to the thermal coupling. The simulations in table 3.3 show that this can give a $1 - 2°C$ temperature difference, resulting in a potential mismatch in the coupler and stability issues.

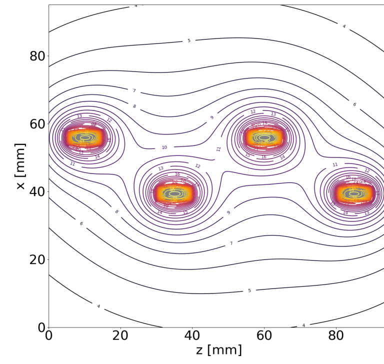
The temperature difference can be reduced by changing the constellation. An equal temperature can, for instance, be achieved if the distance between all transistors is equal, giving equal thermal coupling. This is achieved in the square

constellation shown in figure 3.8 (d). However, a slight temperature difference can be seen here due to the rectangular shape of the transistor. Alternatively, it can be fixed by turning the transistors 45° or slightly changing the distance in the z-direction.

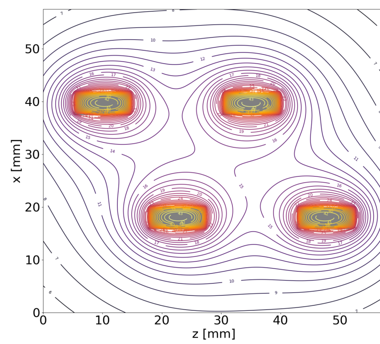
A downside of the squared constellation is that it increases the complexity of the matching network, as it has to be crammed between the transistors. A compromise can be achieved by using the constellations in figure 3.8 (b) and (c). Alternatively, the distance between the centre transistor can be changed to reduce the thermal coupling, or they can be isolated by introducing a division in the baseplate.



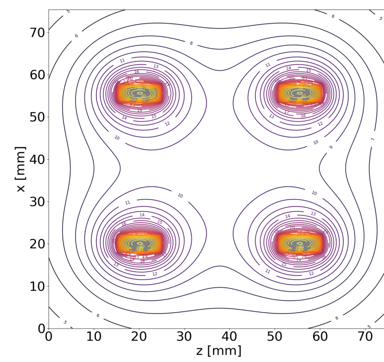
(a) Line constellation



(b) Line constellation with offset



(c) Z constellation



(d) Square constellation

Figure 3.8: Contour plot showing the temperature distribution on the top of the baseplate for four different constellations.

Chapter 4

Test amplifier design

4.1 Specification and technology

An amplifier is realised with a distributed topology to evaluate the method. Here, four 25W transistors are combined for 100W output power. The targeted specifications are shown in table 4.1. The frequency range is chosen as it is convenient for realisation using microstrip lines. It is also an interesting frequency range where the capacity bands in 3G and 4G systems operate [25].

Table 4.1: Specifications for test amplifier.

Parameter	Value	Unit	Comment
f_c	2000	MHz	Centre frequency
BW	500	MHz	RF bandwidth
P3dB	>100	W	Power delivered to load at 3 dB compression
PAE	>50	%	Power Added Efficiency at P3dB
G_T	14	dB	Transducer gain at P3dB
Z_S, Z_L	50	Ω	Source- and load impedance
S_{11}, S_{22}	<-10	dB	Input- and output return loss
μ, μ^*	>1	-	Unconditionally stable

4.1.1 Transistor and bias point

The design is based around a CG2H40025 transistor from Wolfspeed. It is a 25W general use GaN HEMT transistor with good gain and efficiency. A GaN HEMT transistor is a wide bandgap technology suitable for RF application, especially for high-temperature operation. [26] is recommended for an in-depth description.

4.1.2 Substrate and conductor

The design is done on a RO4003 substrate from Rogers. It is a substrate with low loss, low dielectric tolerances and stable electric properties vs frequency and temperature [27]. Critical parameters of the substrate are shown in table 4.2.

The glass transition temperature, T_g, is higher than the maximum transistor temperature, so the operating temperature will not be an issue for the substrate.

35 μm thick copper plates are used as conductors. A conductivity of $59.6 \times 10^6 S/m$ is used in the simulations [28]. Effects due to copper roughness and case height are ignored. Copper has a thermal expansion of 16.5 ppm [28]. This corresponds well with the thermal expansion of RO4003, so this is not assumed to be an issue.

Table 4.2: Substrate properties [27].

Parameter	Value	Unit
Dielectric Constant (ϵ_r)	3.38 ± 0.05	-
Thermal Coefficient of ϵ_r	+40	ppm/°C
Dissipation Factor ($\tan\delta$)	0.0021	-
Thickness	1.524	mm
Thermal Conductivity	0.71	W/m/°K
Glass Transition Temperature (T_g)	>280	°C TMA
Coefficient of Thermal Expansion	x: 11 y: 14 z: 46	ppm/°C

4.1.3 Passive components

Several passive lumped capacitors and resistors are used in stability circuits, DC feeds and DC blocks. The larger $100nF$ and $10\mu F$ capacitors in the DC feed are realised with Murata multi-layer ceramic capacitors. The rest is multi-layer ceramic High-Q capacitors from Johanson in the E12 range. All have models used to describe their non-ideal behaviour in the simulations. A standard pair of SMD resistors in the E12 range is also used. An ideal model is used for them as parasitic effects are less problematic for resistors.

4.2 Circuit design

4.2.1 Overall design

The overall design of the amplifier is shown in 4.1. The transistors are combined in a 2-to-1 approach with equal phases between the branches. This is done in order to reduce the complicity as much as possible. The 2-to-1 approach does in addition make the stability considerations easier to handle. The 2-to-1 approach also gives three symmetric levels, shown in figure 4.1, which are used to ease the design.

Individual bias points are added to each transistor gate to be able to compensate for different threshold voltages. Two bias points are used at the drain to reduce the currents running through the DC feeds.

The S_1 splitters are realised as Wilkinson Splitters to improve the isolation between the transistors. This is done to reduce potential instability. S_2 is for simplicity realised as a simple lossless T-junction. The combiners C_1 and C_2 are

also realised as lossless T-junction, as adding loss to the output is undesirable due to the high power. Matching circuits are added to match the transistor's target impedance and the ports to 50Ω. The matching is done in multiple steps to compensate for the increased impedance in the T-junctions.

4.2.2 Bias point

Figure 4.2 shows the simulated DC characteristics. The typical threshold voltage is stated to be -3 V in the datasheet, which is also seen in the simulation [22]. The amplifier is biased in class B due to its increase in efficiency compared to class A. A deep class AB is used as an ideal class B is not realisable in practice. A gate voltage of $V_{gs} = -2.85V$ is initially considered a suitable bias point. An alternative, $V_{gs} = -2.6V$ is also shown, which will be discussed further in section 4.4.

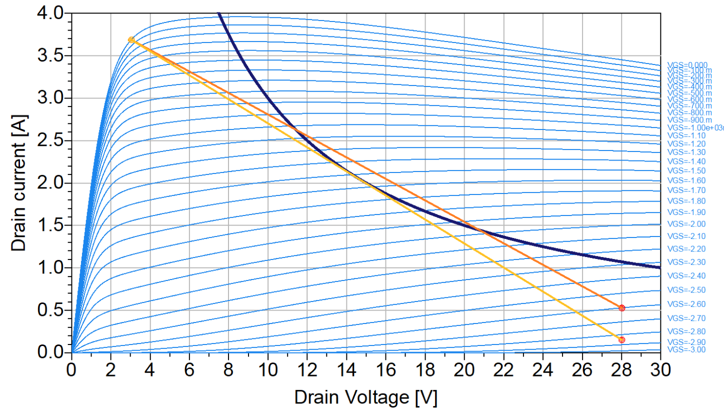


Figure 4.2: Simulated DC-characteristics for CG2H40025. The dark blue line marks $P_{DC} = 30W$.

4.2.3 Choice of target impedance

The gain, delivered power and efficiency of the transistor depend on the impedance seen by the transistor, Z_S and Z_L. Matching circuits are used to match the transistor to a suitable target impedance chosen here. The simulations are done in ADS, where the simulation setups are shown in appendix C.

Transistor impedance and Load-pull

The reflection coefficient looking into the gate and drain is shown in 4.3. Additionally, a load-pull is shown in figure 4.4 for 2 GHz with 30 dBm input power. The gain is maximised for $\Gamma_L = \Gamma_{in}^*$, as seen by the delivered power in 4.4 and expected from equation 2.4. However, the efficiency can be improved by moving slightly up in the inductive region.

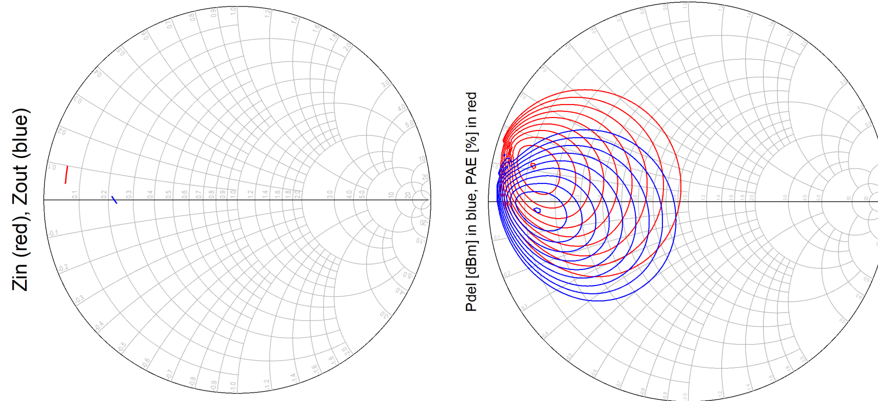


Figure 4.3: Impedance seen looking into the transistor.

Figure 4.4: Load-pull at 2 GHz with P_{in} = 30 dBm.

Optimised impedance

The optimal target impedance is found by performing load-pull using the setup in figure 4.5. The load- and source-pull sub-circuits are implemented as shown in figure 4.6. Here the S2P-block is used to control the reflection coefficient seen by the transistor at the operating frequency. These blocks are provided by Associate Professor Morten Olavsbråten. The source-pull is performed before a subcircuit which contains the transistor pad and stability circuit from subsection 4.4. This is done as this subcircuit is fixed and therefore not interesting for the source-pull. Harmonic tuning is not implemented to reduce complexity. The harmonic termination is therefore not considered here.

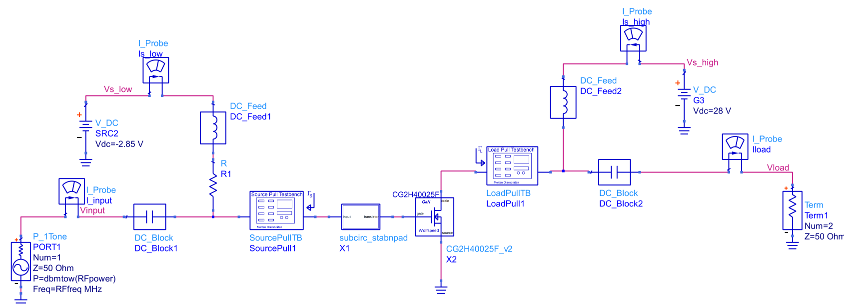


Figure 4.5: Test-bench used to find optimal transistor impedance.

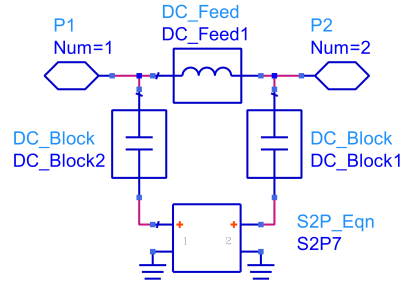


Figure 4.6: Implementation of load-pull block.

The ideal impedance will change slightly with frequency. A linear expression, shown in equation 4.1, is used to approximate this change. Parameter optimisation is used to find the constants using harmonic balance simulations. The optimisation goals are shown in table 4.3.

$$\Gamma = (A_m + B_m \cdot f)e^{j\omega(A_p + B_p \cdot f)} \tag{4.1}$$

Table 4.3: Optimisation goals for load-pull.

Paramter	Goal	Unit	Weight
Pdel	>45	dBm	1000
PAE	>60	%	1
GT	>16	dB	1

4.2.4 Bias circuit

A DC feed is realised as a part of the bias circuit to isolate the DC source from the RF path. An ideal DC feed should be a short circuit at DC and an open circuit at RF. In practice, it is often realised like a low-pass filter using an inductor or several decoupling capacitors. The latter is used here as shown in figure 4.7. The full implementation is shown in figure B.1 in the appendix. Ideally, a quarter wavelength line should be used for TL_{in} in combination with a quarter wavelength stub. This would give an open circuit looking into the bias. However, a stub is not used here due to limited area.

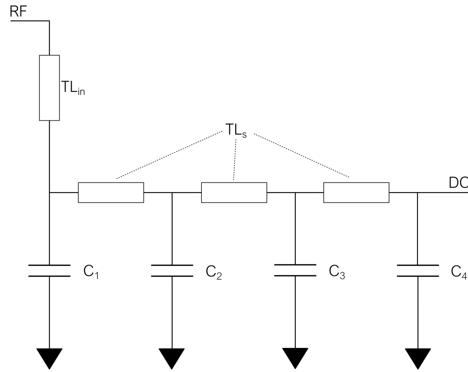


Figure 4.7: Schematic of DC-feed. $C_1 = 12pF$, $C_2 = 10\mu F$, $C_3 = 8.2pF$ and $C_4 = 100nF$.

The S-parameter dampening from the RF-port to the DC is shown in figure 4.8 when connected to a 50Ω termination. A dampening of $\approx -20dB$ is seen within the bandwidth. However slightly worse for harmonics. This is seen as good enough.

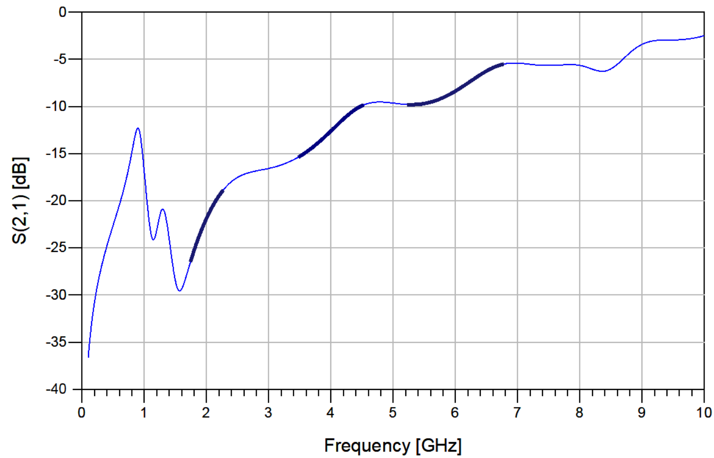


Figure 4.8: Transmission coefficient for realised DC-feed from RF to DC.

4.2.5 Matching circuits

The matching circuits are implemented using a stepped impedance approach to get a wideband matching. Three lines are used in the first place in each subcircuit in figure 4.1 and the parameter optimiser is used to find suitable length and width. The matching circuits are then simplified where this is suitable using an iterative process. The matching circuit is integrated into the power combining to reduce area.

4.2.6 Splitters and combiners

The T-junctions are realised using a MTEE-components in ADS. The junction dimensions are determined by the ideal width of the input and output lines used for matching. Tapers are used when there is a significant difference between the widths.

The Wilkinson couplers used on the input are realised as shown in figure 4.9. The full ADS implementation is shown in figure B.6 in appendix B. The resistor is implemented using two 220Ω resistors in parallel to handle higher power in case of a mismatch. This gives a slight deviation from the ideal 100Ω. However, this seems to have a limited impact. The simulated results shown in figure 4.10 shows a low loss, as the transfer ratio (S_{21}) is very close to - 3 dB. Good isolation of -20 dB is shown between the ports (S_{32}), and a good match to 50Ω is also seen (S_{11}).

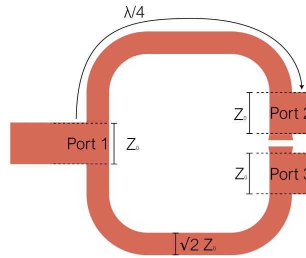


Figure 4.9: Implementation of the Wilkinson power divider.

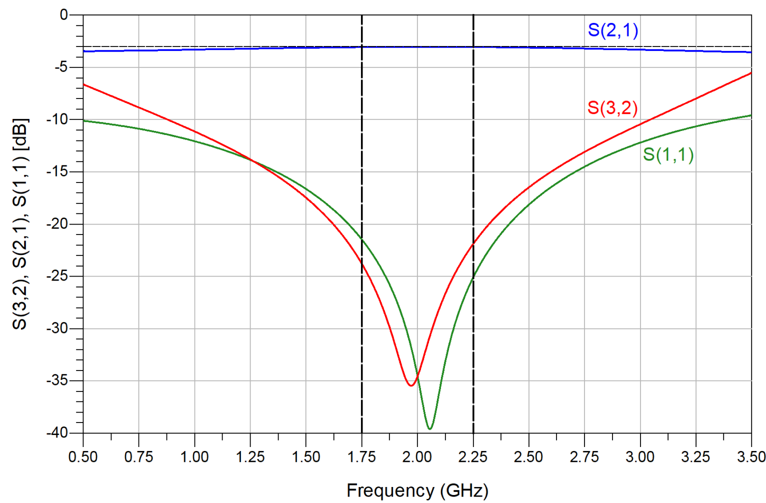


Figure 4.10: Simulated S-parameters fr the Wilkinson power divider. S_{21} (blue) is the transmission coefficient, S_{32} (red) is the isolation between the output ports, S_{11} is the input reflection coefficient.

4.2.7 Stability circuit

Resistance is added to the gate to compensate for the negative resistance of the amplifier and, by doing so, ensure stability. The main issue is the stability in the lower frequency range. A capacitor is therefore added in parallel with the resistor to form a high-pass filter. The value of the capacitor is then chosen so that loss is limited to the potentially unstable region. The introduction of the resistor results in a decrease in gain. Another resistor is therefore added to the gate bias to reduce the gate Resistance necessary.

The stability circuit is placed at the input as the high powers at the output make loss there disadvantageous. It is placed as close to the gate as possible as this is found to be the most sensitive node for stability. However, a large transistor pad is placed first, as this is necessary to hit the target impedance.

4.2.8 Optimisation

Small signal optimisation

The design is first optimised in the small-signal regime to find suitable lengths and widths for the transmission lines. This is done for each level in figure 4.1, where the transistor ports are matched to the target impedance found in section 4.2.3. The other port is (a) matched to 50Ω if it is connected to an in-/output or a Wilkinson splitter, or (b) 80Ω if it is connected to a T-junction. An impedance over 50Ω is used for the T-junctions to reduce the challenges with the impedance drop. The optimisation goal is here to minimise the reflection coefficients, S_{11} and S_{22}, as much as possible over the bandwidth.

The advantage of using a small signal optimisation is that it is considerably less time-consuming than a large signal simulation. This allows testing a more extensive set of possible combinations of transmission lines, and one is likely to get closer to the global optimum. The optimisation was done randomly before gradient descent was used to find an optimum combination.

Large signal optimisation

A large signal optimisation was performed using gradient descent at the end to compensate for the simplifications when finding the target impedances and optimising the coupler/splitters. The goals in table 4.4 are used. The small-signal same time to maintain the matching at the ports.

Table 4.4: Goals used in large signal optimisation.

Paramter	Goal	Unit	Weight
Pdel	>50	dBm	1000
PAE	>50	%	1
GT	>14	dB	1
S21	>15	dB	1
S11	<-10	dB	1
S21	<-10	dB	0.1

4.3 Realised amplifier

The finalised layout is shown in figure 4.11, while the implementations are found in appendix B. An effort is made to make the design as compact as possible by twisting lines while maintaining the correct spacing and symmetry. The output lines have a minimum width of 2 mm to limit heat increase due to losses. This corresponds to a maximum allowed temperature increase of 10°C for a 2 A current. This is calculated using a calculator based on the IPC-2221 standard [29]. The outline of the baseplate and corresponding screwing holes are also shown in figure 4.11. Figure 4.12 shows the realised amplifier with all the soldered components.

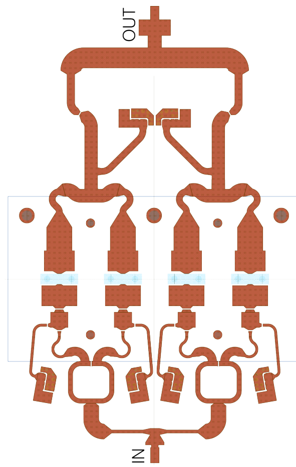


Figure 4.11: Final layout

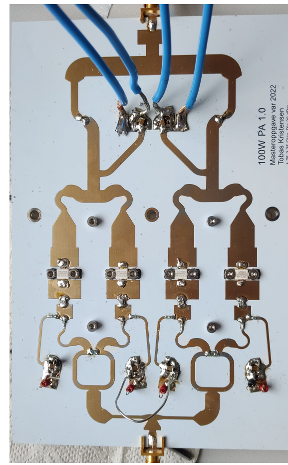


Figure 4.12: Realised amplifier.

4.4 Stability analysis

4.4.1 Small-signal stability

Small signal stability is ensured by checking the μ-stability parameter from section 2.2.1. This is done for the individual levels shown in figure 4.1, where the result is shown in figure 4.13. The test benches are shown in appendix C. It is seen that $\mu > 1$ and $\mu^* > 1$ for all frequencies. Therefore, the amplifier can be assumed to be unconditional stable in the small-signal regime.

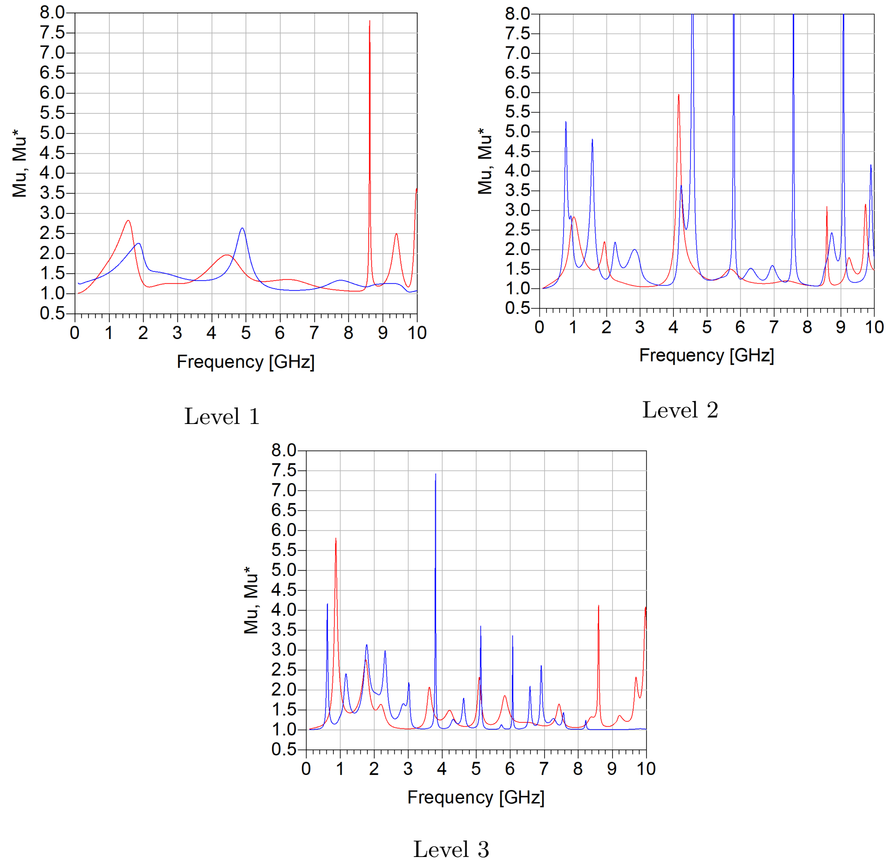
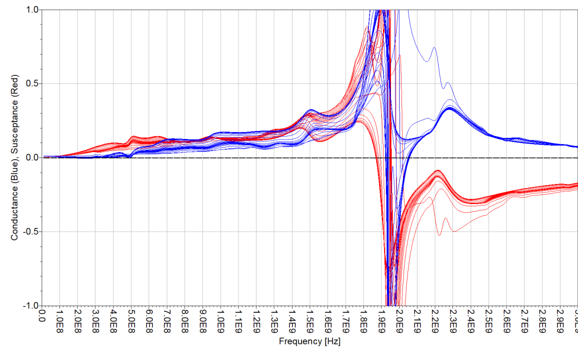


Figure 4.13: Simulated μ (blue) and μ^* (red) for the three levels from figure 4.1.

4.4.2 Large-signal stability

The conductance and susceptance are measured on different nodes using the admittance analysis method described in section 2.2.2. The gate node, shown in figure 4.15, was problematic. Here there are a considerable negative resistance for a P_{in} between 16 and 38 dBm in the frequency range of 1950-2050 MHz as shown in figure 4.14. This issue is most problematic for an RF drive in the upper part of the frequency band. There is also a slight negative resistance for P_{in} between 0-14 dBm between 150 MHz and 300 MHz. However, the oscillation criteria from 2.12 is never seen to be fulfilled as the susceptance never crosses 0 with a positive derivative. No signs of these instabilities were seen at the drain node.



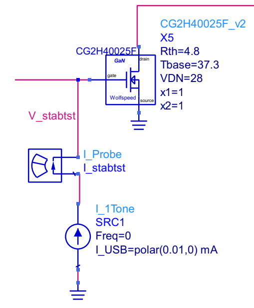


Figure 4.14: Simulated conductance and susceptance at the gate node for 2.25 GHz RF drive.

Figure 4.15: Simulation setup for the admittance analysis.

After some investigation, it was seen that the negative resistance could be reduced by increasing the gate bias from -2.85V to -2.6V and increasing the stability capacitance from 1.5 pF to 2.7 pF. However, the negative resistance could not be removed entirely without substantially affecting the amplifier's performance. The result is shown in figure 4.16. The criteria for oscillation are still not fulfilled for any frequency. Therefore, the amplifier can only be said to be conditionally stable as there are negative resistances.

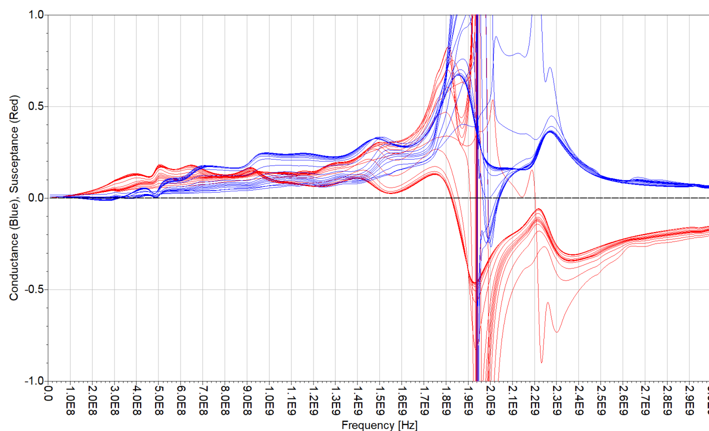


Figure 4.16: Simulated conductance and susceptance at the gate node for 2.25 GHz RF drive after the gate bias is increased from -2.85V to -2.6V and the stability capacitance from 1.5 pF to 2.7 pF.

4.5 Simulated results

4.5.1 Small signal simulations

The simulated small-signal response of the amplifier is shown in figure 4.17. The simulations show a small signal gain of 17-18 dB over the bandwidth. The gain

is relatively flat but decreases for higher frequency as the intrinsic gain decreases. The input reflection coefficient of $S_{11} < -10dB$ is not achieved over the entire bandwidth. However, it is decided to be good enough. The output reflection coefficient is well within the specification.

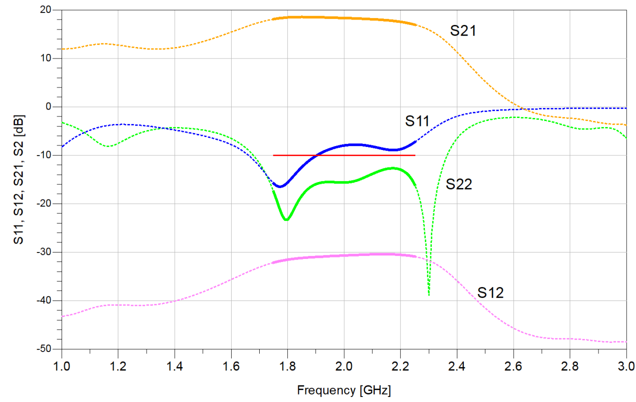


Figure 4.17: Simulated S-parameters.

Figure 4.18 and 4.19 shows the reflection coefficients seen by the transistor. It is seen that the matching circuit provides a reflection coefficient close to the target impedance, especially considering the bandwidth. The input reflection coefficient is shown before and after the stabpad subcircuit, as the target impedance is found before in section 4.2.3.

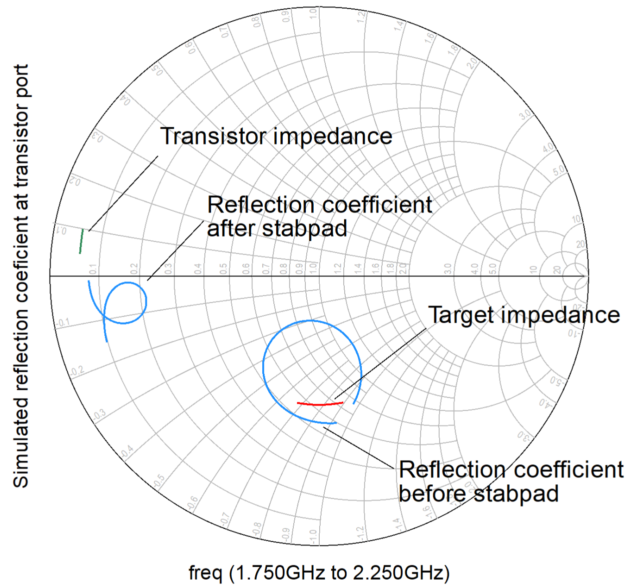


Figure 4.18: Simulated input reflection coefficient compared to target impedance and transistor impedance.

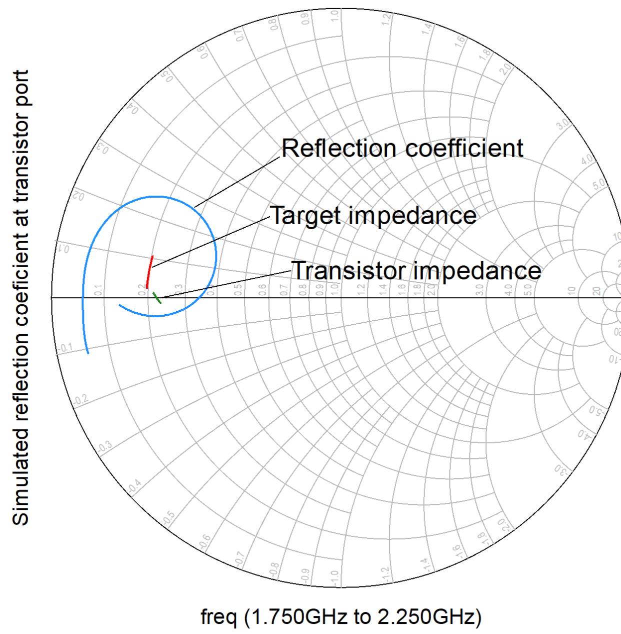


Figure 4.19: Simulated output reflection coefficient compared to target impedance and transistor impedance.

4.5.2 Large signal simulation

The simulated output power and transducer gain are shown for a swept input power in figure 4.20 for the centre and edges of the frequency band. It is seen that the gain at 2250 MHz is $\approx 1dB$ lower, as also seen in figure 4.17. A delivered power of $\approx$ 50.5 dBm is seen at the optimised input power of 36 dBm and a peak output power of 52 dBm. The gain is seen to have a premature gain compression.

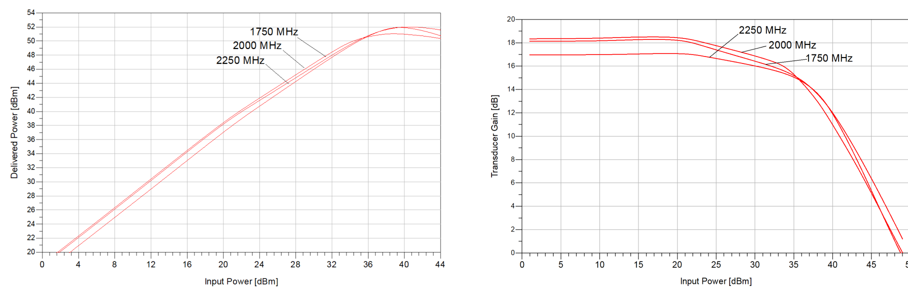


Figure 4.20: Delivered power and transducer gain for a swept P_{in}

P_{del}, PAE and G_T is shown for different frequencies and compression levels in figure 4.21, 4.22 and 4.23. The specifications at P3dB are fulfilled for the bandwidth, outside a small deviation at around 1915 MHz.

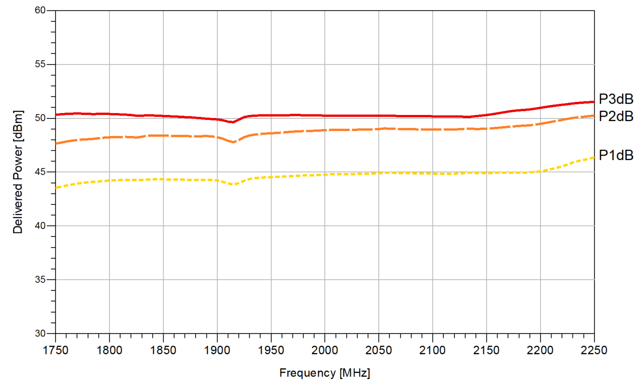


Figure 4.21: Delivered power for P1dB, P2dB and P3dB over the bandwidth.

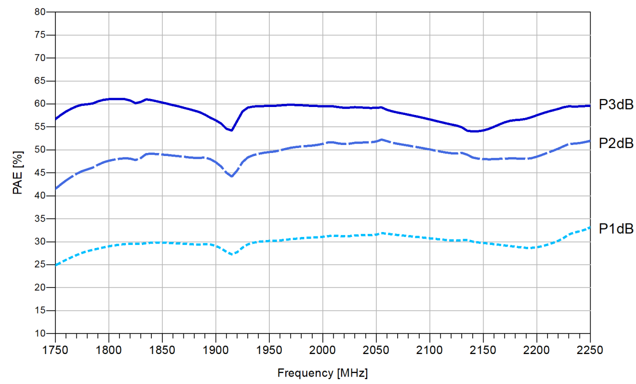


Figure 4.22: PAE for P1dB, P2dB and P3dB over the bandwidth.

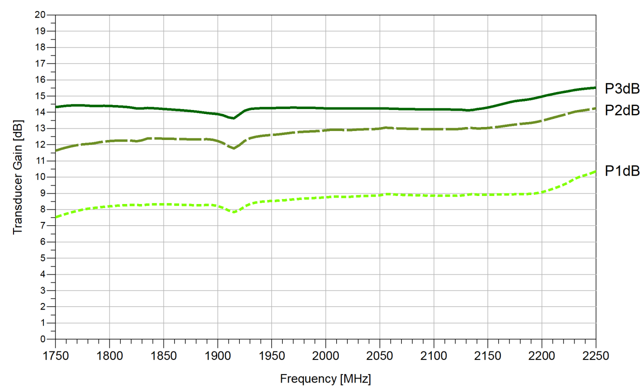


Figure 4.23: Transducer gain for P1dB, P2dB and P3dB over the bandwidth.

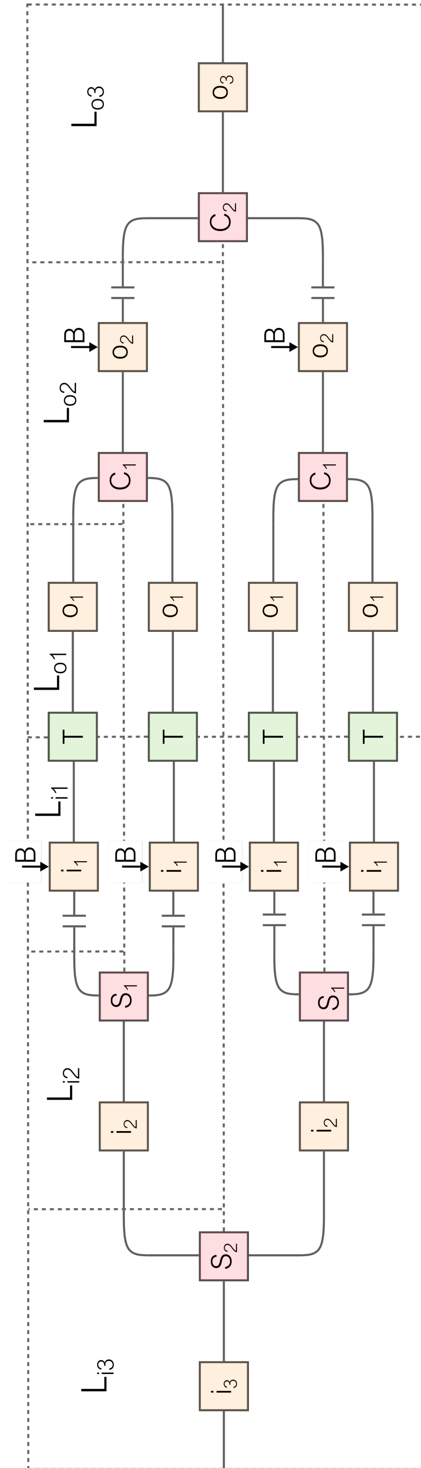


Figure 4.1: Block diagram of the test amplifier. The yellow blocks (i_n,o_n is matching networks. Red blocks are splitters (s_n) and combiners (c_n). The green blocks are transistors. The insertion of biasing is denoted with a black arrow and **B**. The blocks are indexes based on the symmetry levels L_1, L_2, L_3 which is marked by the grey lines.

Chapter 5

Measurements

Thermal DC measurements are done to evaluate the thermal performance of the test amplifier. Small- and large-signal measurements are also performed to verify the amplifier operation. The particular methods and results of the measurements are discussed in the following sections. The equipment used is listed in appendix A.

5.1 DC measurements

DC measurements are performed to measure the thermal response of the amplifier. The dissipated power from equation 2.7 simplifies to $P_{diss} = P_{DC} = V_{ds}I_{ds}$ with no RF-drive. So, it is possible to control the dissipated power by setting the operating point, V_{ds}, I_{ds}. This is used to measure the steady-state operating temperature for a series of power levels. In addition, the threshold voltages and the thermal step response are measured.

5.1.1 Method

Laboratory setup

The test amplifier from section 4.3 is mounted to a 12 mm thick, 25 cm x 40 cm aluminium plate with a heat sink clamped on beneath to improve the heat dissipation. Thermal paste is used between the metals to ensure good thermal contact. Two 2" x 4" wooden boards are used to lift the aluminium plate above the table and form a channel to control the heat flow. This is shown in figure 5.2. Two fans are placed at the channel entrance to push cold air towards the heat sink. This should be capable of cooling the system sufficiently.

The DC measurements are performed with 50Ω termination on the input and the output, as shown in figure 5.1. Termination is used to protect in case of oscillations.

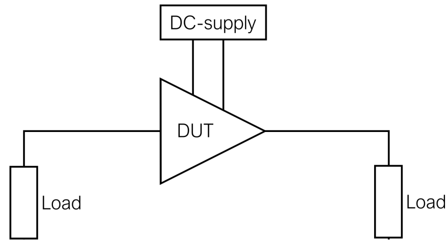


Figure 5.1: DC measurement setup.

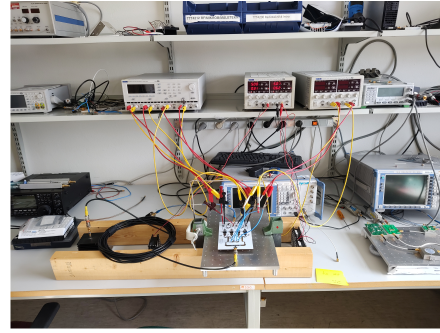


Figure 5.2: Laboratory setup.

Thermal measurements

Five measurement points are defined as shown in figure 5.3. The screws used to mount the transistors, M1 and M3, are considered the best points to measure the case temperature of the transistor, as it is not possible to measure directly on the baseplate. The difference between M1 and M3 are used to measure temperature differences between the centre and edge transistors. M2 are used to consider heat dissipation outside the baseplate. M4 are at the narrowest line at the output and is used to measure the temperature increase due to high currents in the microstrip lines. M5 is at the PCB in between the centre transistors. In addition, a point at the edge of the aluminium plate is measured for comparison.

A Fluke Ti10 IR camera is used for temperature measurements. It has an accuracy of $\pm 2°C$ or 2%, depending on which is the largest. Measurements are done on the aluminium plates, microstrip lines and screws made of non-ferrous metals with low emissivity. The low emissivity makes IR measurements challenging. As little heat is emitted as thermal radiation, the metal looks colder in the IR photo. The available IR camera could not compensate for this low emissivity. Therefore, small pieces of paper are glued to the measurement points to overcome this issue. These paper pieces have higher emissivity, allowing more precise measurements. The paper is so thin that it is assumed to have the same temperature as the metal.

Biasing

The following procedure is used for biasing the amplifier. The GaN transistor demands negative gate voltage, so it is applied first to ensure safe operation. Individual gate voltages are found to account for differences between the transistors.

1. Turn on a gate voltage of -4V on all transistors.
2. Turn on a drain voltage of 5V on all transistors and increase drain voltages up to 28V.
3. Increase the gate voltage on a transistor until $I_D/4$ is achieved, while the other transistors are biased at -4V. Repeat for all transistors.

4. The found gate voltages are applied to the corresponding transistors, and I_D is checked.

The gate voltage is adjusted after some time to account for the effects of increased temperature. The drain voltage is also measured at the circuit and adjusted to account for the voltage drop in the cable when using high currents.

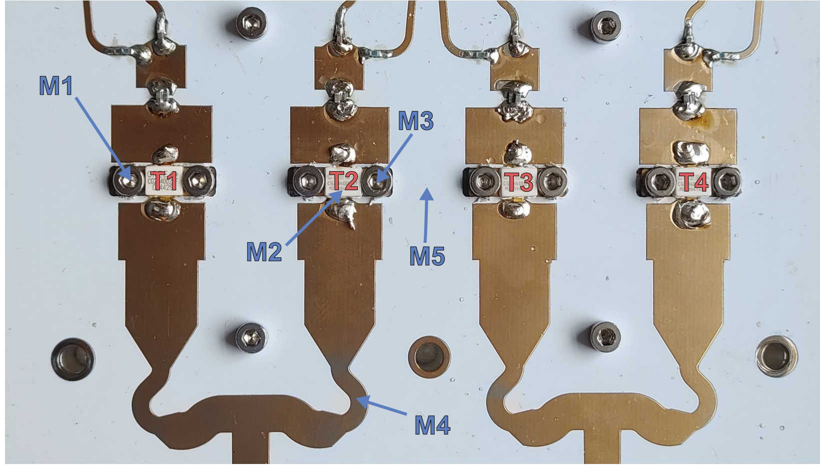


Figure 5.3: Image of the realised amplifier with the five measurement points: M1, M2, M3, M4, M5. The image also shows the transistor numbers used throughout the text.

5.1.2 Results

Measurement of threshold voltages

The different transistors' threshold voltages are measured to unveil possible differences. The differences are measured by finding the V_{gate} necessary to achieve a I_D of 20 mA, 50 mA and 80 mA. The transistors are measured individually, where the gate voltage of one transistor is increased while the rest is biased off with $V_{gate} = -4.0V$. The result is shown in table 5.1. It can be seen that the transistors at the edge are roughly 200 mV different from the centre transistor.

Table 5.1: Gate voltages necessary to achieve $I_D = 20mA$, $I_D = 50mA$ and $I_D = 80mA$.

	I_D = 20mA	I_D = 50mA	I_D = 80mA
T1	2.80V	2.74V	2.70V
T2	3.01V	2.94V	2.91V
T3	3.03V	2.97V	2.93V
T4	2.86V	2.80V	2.77V

Thermal step response

The thermal step response is measured to find the time needed for the system to achieve a steady-state. The measurement is done by applying a DC bias to achieve $P_{diss} = 50W$. The temperature is then measured using an IR camera at points M1, M2 and M3 from figure 5.3. As it is done by hand, it can be assumed there are inaccuracies in both time and temperature.

The measurements are shown in figure 5.4. A steady-state seems to be achieved in around 60 minutes. Using the assumption that a steady-state condition is achieved after 6τ, this corresponds to a time constant of 10. $\tau = 10$ is plotted in the figure using equation 2.27 and seems to fit well. Based on these measurements, it is decided that at least 60 minutes should be waited to ensure a thermal steady state at later measurements.

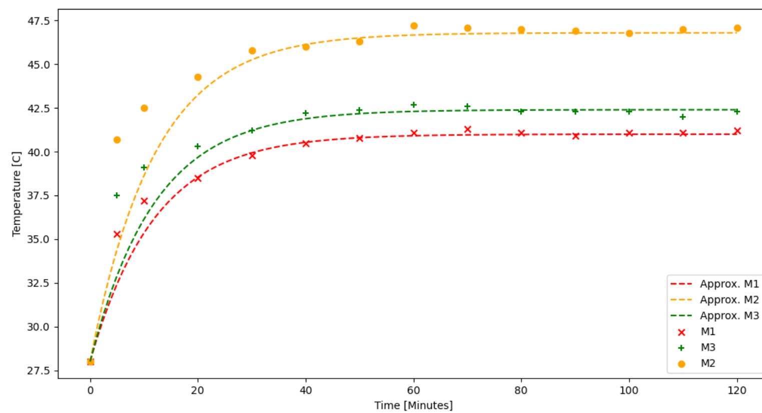


Figure 5.4: Measured temperature at point M1, M2 and M3 when $P_{diss} = 50W$ is applied as a step response. The dotted lines shows the ideal response for $\tau = 10$ using equation 2.27.

DC power dissipation

The DC-measurement setup is used to measure the steady-state temperature for three cases of dissipated power. The dissipated power are corresponding to 70%, 60% and 50% PAE, using equation 2.7 for 14 dB Gain and 100W P_{out}. The temperature is measured at the measurement points in figure 5.3 after waiting 60 minutes for steady-state. The results is shown in table 5.2.

The measurements are compared to the simulated temperatures at M1 and M3 in table 5.3. The simulations are performed for a 22 mm thick aluminium plate to account for the test rig. An ambient temperature of $T_a = 25°C$ is used, accounting for a slight temperature increase through the heatsink.

Table 5.2: Measured temperature at the measurement points from figure 5.3 for ideal PAE of 70%, 60% and 50%. The corresponding P_{diss} is found using equation 2.7 for 14 dB gain and $P_{out} = 100W$.

PAE P_{diss}	70% 41.0W	60% 63.3W	50% 95.6W
M1	38.1	44.7	53.1
M2	42.1	52.8	66.0
M3	39.3	46.3	56.3
M4	35.5	40.2	48.4
M5	38.5	42.7	57.1
Baseplate	33.3	37.7	44

Table 5.3: Measured and simulated temperature at M1 and M3.

PAE P_{diss}	70% 41.0W	60% 63.3W	50% 95.6W
Measured M1	38.1	44.7	53.1
Sumulated M1	37	43	50
Difference	1.1	1.7	3.1
Measured M3	39.3	46.3	56.3
Simulated M3	37.8	44.5	52
Difference	1.5	1.8	4.3

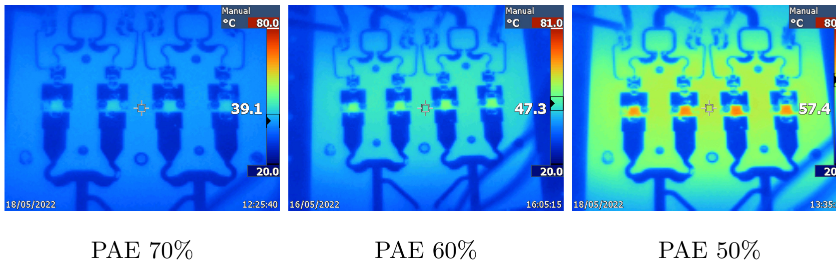


Figure 5.5: IR image for the three measured cases.

5.2 Small-signal measurements

5.2.1 Method

Laboratory setup

A VNA is used to measure the small-signal performance as shown in figure 5.6. A 3 dB (20W) attenuator is placed at the output, and a 30 dB (500W) attenuator is placed at the output. The measurements are performed with 0 dBm power and 1 kHz bandwidth. 64 times averaging was used to reduce noise.

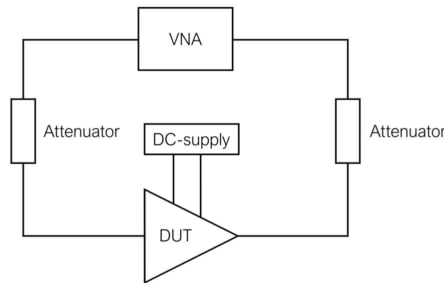


Figure 5.6: Small-signal measurement setup.

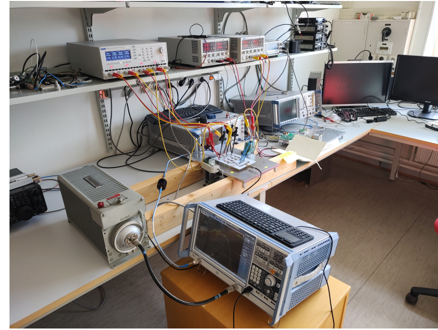


Figure 5.7: Image of laboratory setup.

Calibration

The VNA is calibrated using a conventional TOSM-method, which is further explained in [30]. This is generally assumed to have high accuracy. The calibration is performed with the attenuators.

5.2.2 Results

The measured forward gain, S_{21}, is shown in figure 5.8 plotted against the simulated results from 4.5. The measurements show a gain of $S_{21} = 15dB$, which is relatively constant within the frequency band. The gain is 2-3 dB lower than expected from the simulations. The measurements are also slightly shifted upwards in frequency compared to the simulations.

The measured input return loss, S_{11}, is shown in figure 5.9 plotted against the simulated results from 4.5. The measurements are mostly beneath $-15dB$ in the frequency band, which is distinctively better than expected from the simulations.

The measured S_{12} is shown in figure 5.10 plotted against the simulated results from 4.5. The measurements fit well with the simulated results but show the same tendency as the forward gain in that it is slightly lower and shifted upwards in frequency. The S_{22} measurement is unreliable due to the 30 dB attenuator, as the reflected wave is then damped with a total of 60 dB and hard to disguise from the noise floor.

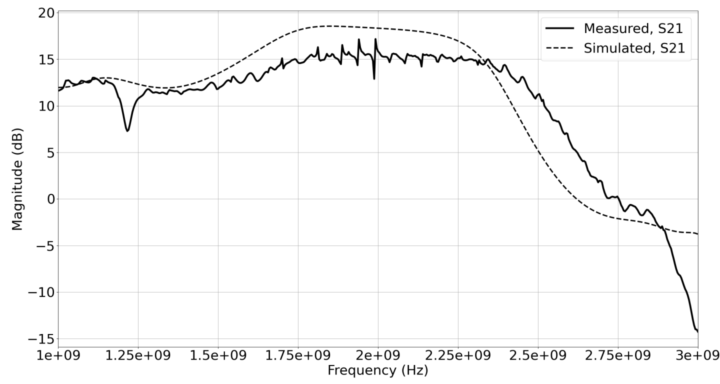


Figure 5.8: Measured and simulated S_{21}.

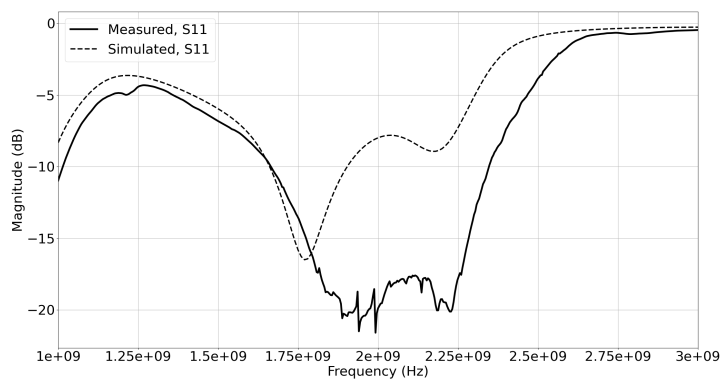


Figure 5.9: Measured and simulated S_{11}.

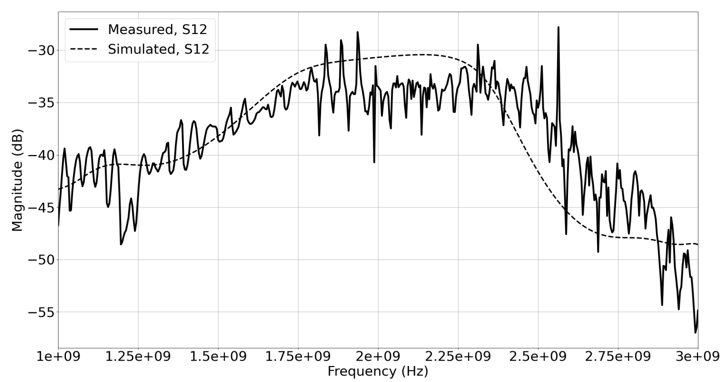


Figure 5.10: Measured and simulated S_{12}.

5.3 Large-signal measurements

5.3.1 Method

Laboratory setup

The large-signal measurements are performed using the setup shown in figure 5.11. A drive amplifier ensures enough gain to drive the test amplifier into saturation, and a circulator is used to isolate the test amplifier from the driver. Attenuators are used to avoid exceeding the maximum P_{in} of the spectrum analyzer.

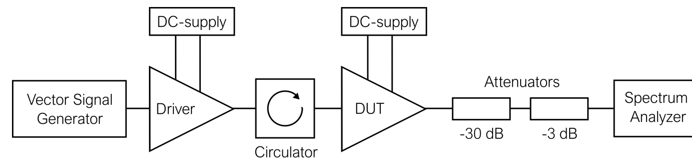


Figure 5.11: Measurement setup.

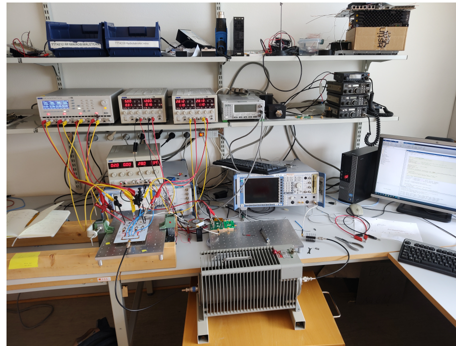


Figure 5.12: Image of laboratory setup.

Calibration

The power loss through the passive output network is measured during a power sweep to compensate for the loss in the final measurements. Noise makes a noticeable contribution at low power levels, so the attenuation is manually set to an average value to ensure that the noise does not give poor calibration. Then the drive amplifier and circulator were placed in front of the passive output network, and the output power was measured to find the correct input power. The measurements make it possible to find the correct input- and output power for the DUT. The non-linear behaviour of the drive amplifier is also corrected using these measurements. After calibration, the setup was tested with a through connection. A maximum of 0.05-0.09 dB deviation from the 0 dB gain expected through the connector is found. The measurements are done over a short time, so effects due to drifts in the drive amplifiers are ignored. The drive amplifier is also given time to heat up to a thermal steady state, so effects due to changing temperature are also ignored.

5.3.2 Results

The delivered power, transducer gain and power added efficiency are measured for the centre and endge of the frequency band. Figure 5.13, 5.14 and 5.15 shows the result for a swept input power. The measurements shows roughly 3 dB less gain than expected from the simulations in figure 5.14. P_{del} and PAE is corresponded shifted roughly 3 dB to the right in figure 5.13 and 5.15 correspondingly. The maximum values for P_{del} and PAE is also slightly lower than simulated. This applies especially to PAE at 2 GHz.

Table 5.4 shows the measured values at 1-,2- and 3 dB compression. A delivered power above 50 dBm and 50-60 % PAE is achieved at 3 dB compression at the three measured frequencies. The amplifier has a premature gain compression resulting in poor results for 1- and 2-dB compression.

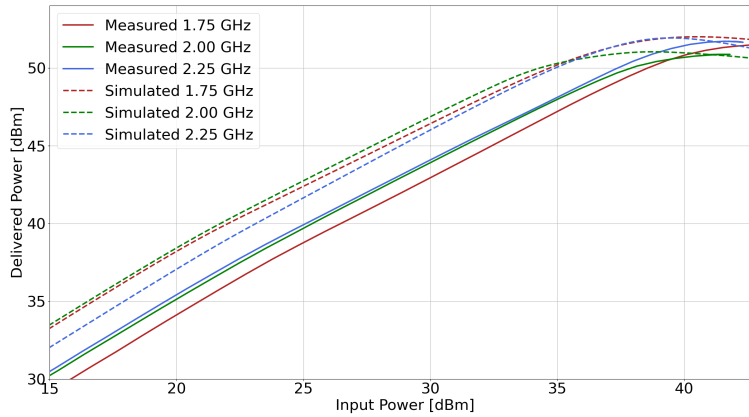


Figure 5.13: Measured and simulated P_{del} for a swept P_{in} at 1.75, 2.0 and 2.25 GHz.

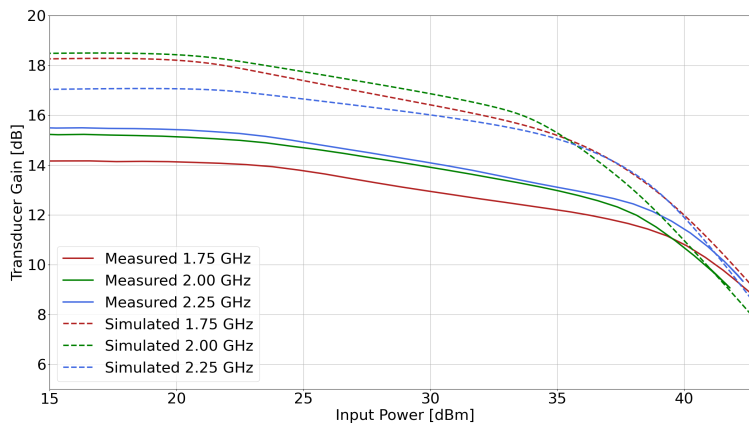


Figure 5.14: Measured and simulated G_T for a swept P_{in} at 1.75, 2.0 and 2.25 GHz.

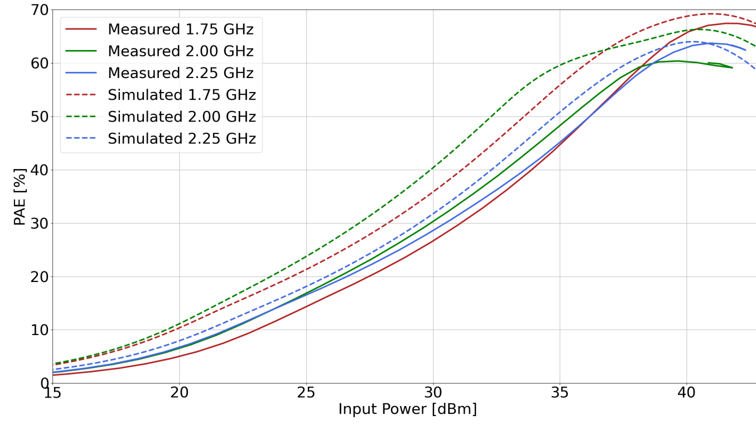


Figure 5.15: Measured and simulated PAE for a swept P_{in} at 1.75, 2.0 and 2.25 GHz.

Table 5.4: Large signal measurement at 1-, 2- and 3- dB compression.

Frequency	Compression level	Pin [dBm]	Pout [dBm]	Gt [dB]	PAE [%]
1750 MHz	1 dB	28,9	42,02	13,11	23,6
	2 dB	35,51	47,63	12,12	46,96
	3 dB	39,32	50,48	11,16	63,87
2000 MHz	1 dB	28,60	42,75	14,15	26,13
	2 dB	34,28	47,41	13,13	45,43
	3 dB	38,13	50,11	11,98	59,24
2250 MHz	1 dB	27,63	42,12	14,49	22,39
	2 dB	33,46	46,87	13,42	39,42
	3 dB	37,99	50,43	12,44	57,62

Chapter 6

Discussion

6.1 Measurements

6.1.1 Amplifier performance

The measured result is compared to the specification and the simulated result in table 6.1. The main deviation is a lower gain than anticipated from simulations, and it is also below specification. This is seen both for the small- and large-signal measurements. Besides this, the measurements fulfil the specifications. However, the stability factor μ and μ^* are not measured due to the poor S22 measurements. Still, no signs of oscillations were seen during the measurements.

Table 6.1: Measurements compared to specification and simulations.

	Spec.	1.75 GHz		2.00 GHz		2.25 GHz		Unit
		Sim.	Meas.	Sim.	Meas.	Sim.	Meas.	
P3dB	>50	51.65	50.48	50.36	50.11	51.65	50.43	dBm
Gt	>14	15.06	11.16	14.37	11.98	15.65	12.44	dB
PAE	>50	62.65	63.87	62.27	59.24	61.41	57.62	%
S11	<-10	-15.82	-13.64	-7.99	-19.88	-7.27	-17.92	dB
S22	<-10	-11.63	-	-12.89	-	-12.98	-	dB

Three observations differ between the measured and simulated small-signal response: Loss in gain, shift towards higher frequency and lower input reflection. This implies that the realised network response is moved slightly compared to the simulated network. This can be due to EM crosstalk from a close distance between lines or discontinuities, which is not sufficiently modelled using a lumped model approach. The pad at the transistor input is also slightly wider than the ADS model recommends, which can be another reason for the difference. Alternatively, it can be the effective dielectric constant which is lower than expected. The difference could also be due to errors in the transistor model. However, the models from Wolfspeed are assumed to be too good to give the error measured here.

The difference between simulated and measured P_{del} and PAE is not higher than expected due to variations. However, there is an interesting difference between the frequency response of the large-signal measurement. It can seem like the response of 1.75 and 2.25 GHz have shifted place. This can be due to the frequency shift seen for the measured S_{21}. The premature gain compression seen in figure 5.14 is possibly a result of the trapping effects in GaN [26].

A periodic error can be seen in the small-signal measurements. This may be due to delayed reflections from the attenuator that are not correctly calibrated away using TOSM. The error is repeated roughly every 50 MHz, corresponding to an electrical length of $e \approx 4m$ for a coaxial cable with a velocity factor of $\kappa = 0.66$ [31]. This imply a reflection after a cable with length $e/2 \approx 2m$. This corresponds well with the length of the cable between the amplifier and attenuator output.

Table 5.1 shows that the centre and edge transistors have different threshold voltages. It is likely that these transistors are from two different batches and therefore operate slightly different. As the transistors are individually biased for a given drain current, it is not assumed to be an issue. However, it should be noted as a challenge when using multiple transistors and that individually biasing is recommended for future designs.

6.1.2 Thermal measurements

IR camera

An IR camera was used to measure temperature as this was the best equipment available. It is, however, not reliable for accurate measurements. When measuring by hand, variations are seen as a result of small movements. It is then hard to find the correct temperature. In addition, the camera has a considerable uncertainty of 2% or $2°C$ depending on which largest. The camera also automatically recalibrated between measurements. This leads to additional uncertainty. On top of this is the uncertainty due to emissivity discussed in section 5.1.1. Therefore, the measurements cannot be assumed to be accurate enough for a precise evaluation of the model.

Thermocouples could be a better alternative to the IR camera. Of course, this method would also have uncertainties, but they could be fixed to the measurement points to reduce some uncertainty.

Performing the measurements on the screws gives additional uncertainty. The screw will have thermal resistance and be affected by ambient temperature on the top and through the heatsink at the bottom. Improved measurements could be performed by adding holes or pads on different spots in the PCB boards where thermocouples could be mounted. Then the simulated model could be investigated more thoroughly for more points than just the screws close to the transistor.

The issues with emissivity are seen in figure 5.5. Here the matching circuit and screws are all colder than the substrate. However, the points where paper is glued on showing a higher temperature.

Step response

The thermal step response in figure 5.4 fits roughly with the ideal model. However, there is a consistent deviation at the beginning. First of all, it must be assumed to be some inaccuracy in the measurements in both time and temperature as the measurements are done by hand. The measurements could take 30-60s and are done in the order of M1, M2, and M3. This time deviation could explain some of the misses, as the timing is most important in the beginning when the temperature increases rapidly. There is also an uncertainty in temperature, as discussed. This can be seen in the practice of the variations in steady-state.

The system showed slight signs of overshooting as the temperature started to decrease a little after 60 minutes. It could be the uncertainties in measurements, but as it is consistent for all points, it could also indicate multiple poles. This is quite likely, as a complex system is considered, with multiple plates and complexity in the transistor.

6.2 Baseplate model

The measured temperature shows a deviation of a couple of degrees compared to the simulated values in table 5.3. However, the result is considered suitable for the models intention of being used for design assessments and evaluating issues related to thermal coupling. The deviations are also well explained by the boundary conditions and choice of ambient temperature discussed in the following subsections.

Boundary conditions

The assumption of an infinite baseplate might introduce an error in the result. Introducing the boundary condition at the baseplate edge, $T_{edge} = T_a$, should intuitively give a slight decrease in temperature close to the edge of the baseplate. This can be why the measured temperature difference between M1 and M3 exceeds the simulated difference. The boundary condition could be implemented using mirror sources at the top of the baseplate, similarly to what is done for the bottom of the baseplate. A similar implementation is mention in [19].

Choice of ambient temperature

The arbitrary assumption of $T_a = 25°C$ beneath the baseplate is used in table 3.3. It is chosen with the assumption of a $\approx 2°C$ temperature increase compared to room temperature due to the thermal resistance of the heat sink. The result in table 5.3 would have fitted better for a temperature of $T_a \approx 26 - 27°C$. A similar heat sink is said to have a thermal resistance of $\approx 0.2°C/W$ under forced convection [32]. Considering table 5.3 this corresponds a $\approx 2°C$ increase for PAE of 70%, $\approx 3,2°C$ for 60% and $\approx 4,8°C$ for 50%. Here thermal coupling is ignored for simplicity. Compared with table 5.3, this fits well with how the error increases with dissipated power. The thermal resistance of the heat sink can therefore be included for better accuracy. It is worth noting that the heat sink will not be able to deliver a perfect uniform temperature equal to T_a in practice. Therefore, an error must be expected.

When discussing the ambient temperature, it is also worth noting that design specifications often demand higher ambient temperature than room temperature. For instance, the military standard MILSTD810 demands that an operating temperature up to $+55°C$ is tolerated. This limitation is for equipment that will coexist with humans. The operation temperature specifications can be even higher in the case of autonomous or more isolated systems. The margin for T_J will decrease when stricter demands for T_a, making the advantage of multiple transistors more critical.

Use of thermal resistances

It is essential to discuss the limitations of thermal resistances, which place an essential role in the model. The thermal resistance is not an intrinsic property of a component but depends on the environment and dissipated power, as further discussed in [21] [33]. It can, therefore, not be relied on entirely if the manufacturer does not provide additional information. However, it should be accurate enough for the discussion considered here.

It should also be noted that the exact P_{diss} dissipated through the baseplate is hard to find accurately. Therefore, the model will only give the worst case, assuming that all P_{diss} goes through the baseplate. Heat dissipation in other directions can have higher thermal resistance and therefore result in increased temperature.

6.3 Distributed topology

A distributed topology is shown to considerably reduce the thermal stress in section 3. However, this gain in thermal performance comes with an expense of an increased cost, area and complexity. PA transistors are often costly, so increasing the number of transistors will considerably increase the final price. However, it is not a linear increase in cost. An additional cost must also be considered if more sophisticated couplers are used.

The increased area is also an issue when considering mobile applications, as it corresponds to the increased weight and size of the product. This could be less concerning for fixed applications. Again the area does not scale linearly with the number of transistors, as the transistor size is also reduced for smaller power. The increased complexity in realizing the matching networks for multiple transistors is an additional issue. Careful design is necessary to ensure that each path has the correct length to avoid phase differences. Additionally, parallel transistor demands careful designs to maintain stability.

The cases in 3.3 indicate that the main limitation is not the thermal resistance in the baseplate or thermal coupling but the high $R_{\theta JC}$ of the transistor. The main advantage of a distributed topology must therefore be said to be the reduction of the dissipated power in the individual transistors. However, the baseplate design will be critical due to the $1/x$ proportionality, seen for many design parameters in section 3.2. A bad design choice can consequently have a significant impact.

Another advantage of the distributed topology is that it can be a balanced- or push-pull configuration can be used, as introduced in section 2.6. This allows

for improved matching and redundancy in the case of a balanced configuration. Alternatively, it reduced distortion for a push-pull configuration. However, implementing the necessary couplers is difficult, especially for bandwidth and power handling. These alternatives should, however, be considered for practical designs.

6.4 Alternative methods

First and foremost, the thermal issues can reduce by reducing the dissipated power. Increasing efficiency is the key method here. For instance, harmonic tuning can be a suitable method for increasing efficiency. Alternatively, efficiency enhancement techniques can be used to handle signals with high PAPR. Techniques such as envelope-tracking and Kahn/EER increase efficiency by adjusting the drain voltage of the transistor such that it always operates in saturation. Other alternatives are Doherty or Load-Modulated Balanced Amplifier (LMBA), which utilize load modulation to increase efficiency. These efficiency enhancement techniques can improve efficiency considerably. However, they come at an increased cost, complexity and challenges with high bandwidth. Also, nonlinear distortion due to the techniques often makes additional linearization techniques necessary, increasing the complexity further.

Interestingly, these techniques can be seen as distributed typologies, as the heat dissipation is spread over multiple transistors. The method discussed in this work could, consequently, also be applied to these cases. However, the motivation is different, as the efficiency enhancement techniques target the PAPR. Preferably, PAPR could also be reduced for increased efficiency. However, this is typically defined by standards and consequently not possible to change for circuit designers.

The thermal challenges can also be reduced by improving the cooling and consequently reducing the case temperature. Water cooling, or similarly, is preferable where this is possible to implement. Alternatively, improved heat sinks or increased air throughput could be used to boost the thermal convection. Heat pipes can also be neatly integrated into a baseplate to spread the heat more efficiently and reduce the implications of thermal hot spots.

6.5 Future work

Comparison with more advanced thermal simulations

The thermal measurements in 5 contain many uncertainties and, therefore, cannot give an accurate evaluation of the method from section 3. A thermal simulation software should be used to investigate the method's validity and limitations further. Especially the implications of boundary conditions should be considered.

EM simulations

The deviations between the amplifier's simulated and measured small-signal response could be explained by EM crosstalk or discontinuities, which are not accounted for in the lumped microstrip models. A set of EM simulations on the

realized circuit should be performed to check for these effects, as the design has many close lines and discontinuities. Integration of EM simulations can be found in the most common RF circuit simulation software.

Test alternative constellations

A square constellation was proposed in section 3.4 to reduce the temperature difference between the transistors. It could be interesting to do a similar design using this constellation and compare it with the one presented here.

Linearity and Intermodulation Distortion

The amplifier linearity and intermodulation distortion were not prioritised in this work. It is, however, an essential property for the operation of the amplifier and something that can be increasingly difficult to achieve for a distributed topology. Therefore, future work should also look into linearity and intermodulation distortion performance.

Chapter 7

Conclusion

A distributed topology is advantageous for reducing thermal challenges in RFPA design. A method for evaluating a distributed topology is presented, considering the thermal coupling between multiple transistors placed on the same baseplate. The results show that high $R_{\theta JC}$ in the transistor is the leading thermal challenge. The main advantage of the distributed topology is, therefore, that the dissipated heat is reduced for the individual transistors, reducing the temperature increase. It is also shown that materials with high thermal conductivity, such as copper, help considerably.

Thermal measurements on the realised 100W PA fit well with the result expected from the model. However, measurements are too inaccurate to conclude on the models accuracy. However, it is seen that the fit can be improved by accounting for the thermal resistance of the heatsink and the boundary conditions at the sides of the baseplate. Further investigations using advanced thermal simulation software and more specific measurements are recommended.

The presented amplifier proves that the distributed topology can be used to design an amplifier with high output power. The amplifier has a lower gain than expected, likely due to different behaviour off the realised matching circuit that the simulated. This can be explained by EM crosstalk or other effects not sufficiently modelled in the lumped component approach used in the simulations. In addition, the amplifiers suffer from premature gain compression and are only conditionally stable in the large-signal regime. The design shows the complexity associated with a distributed topology. Which, in addition, is more costly and vulnerable to stability issues. Consequently, a distributed topology should not be used if it is not strictly necessary.

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Appendix A

Measurement equipment

The following equipment is used for the measurements:

- ZNB8 Network analyzer
- 85052D calibration kit
- SMU200A Signal Generator
- FSQ40 Signal Analyzer
- MX100QP 420W DC source
- EL302TV DC source
- CPX200DP DC source
- MCL BW-S3W20+ 3dB attenuator
- TENULINE 8325 30 dB attenuator
- AFB08054 fan
- R127025DC fan
- MCL TERM-50W-1835+ 50W termination
- PNR T2516 ATM termination
- OiYBC15049B 15T35F Circulator

Appendix B

Schematics of realised amplifier

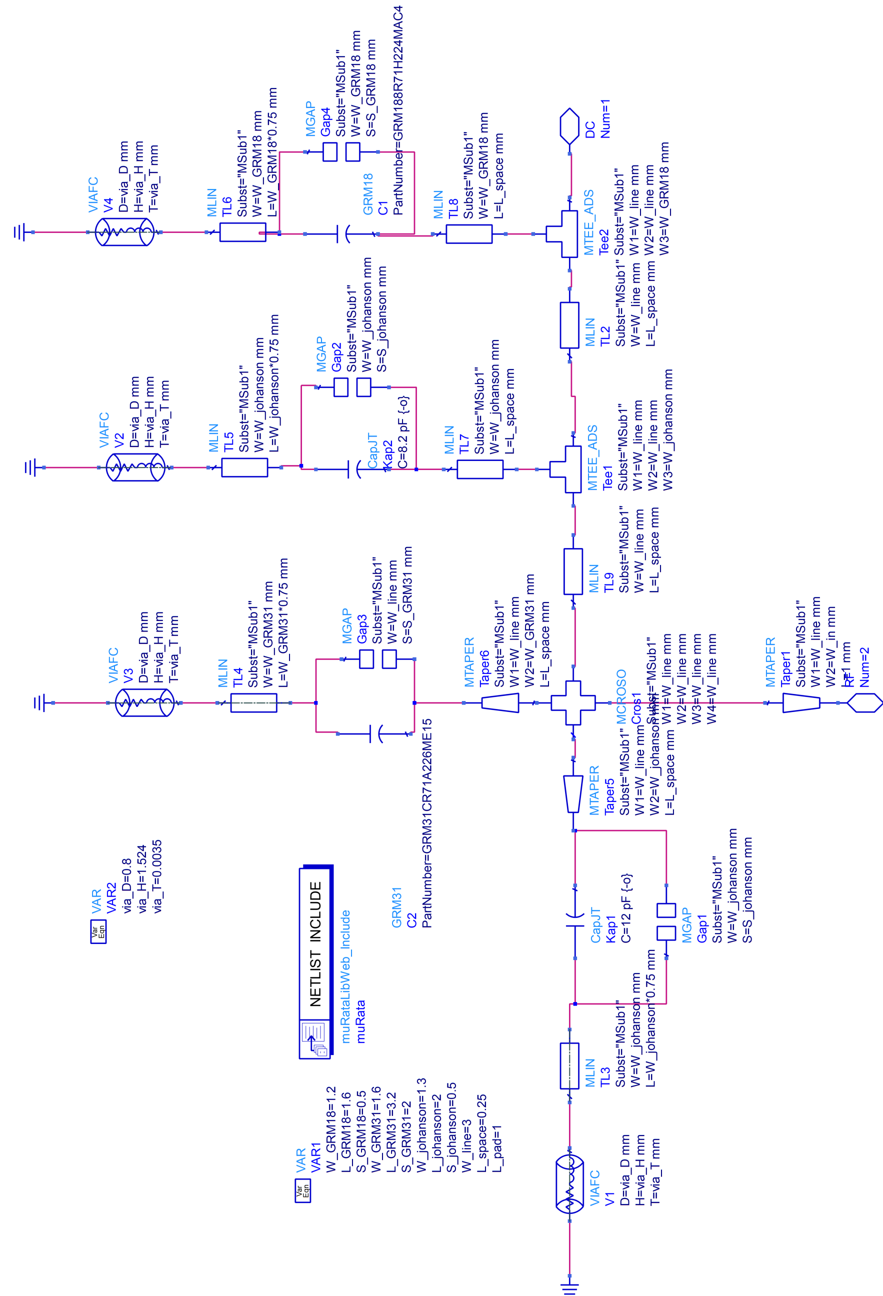


Figure B.1: ADS schematics of bias circuit.

Figure B.2: ADS schematics of input level 1.

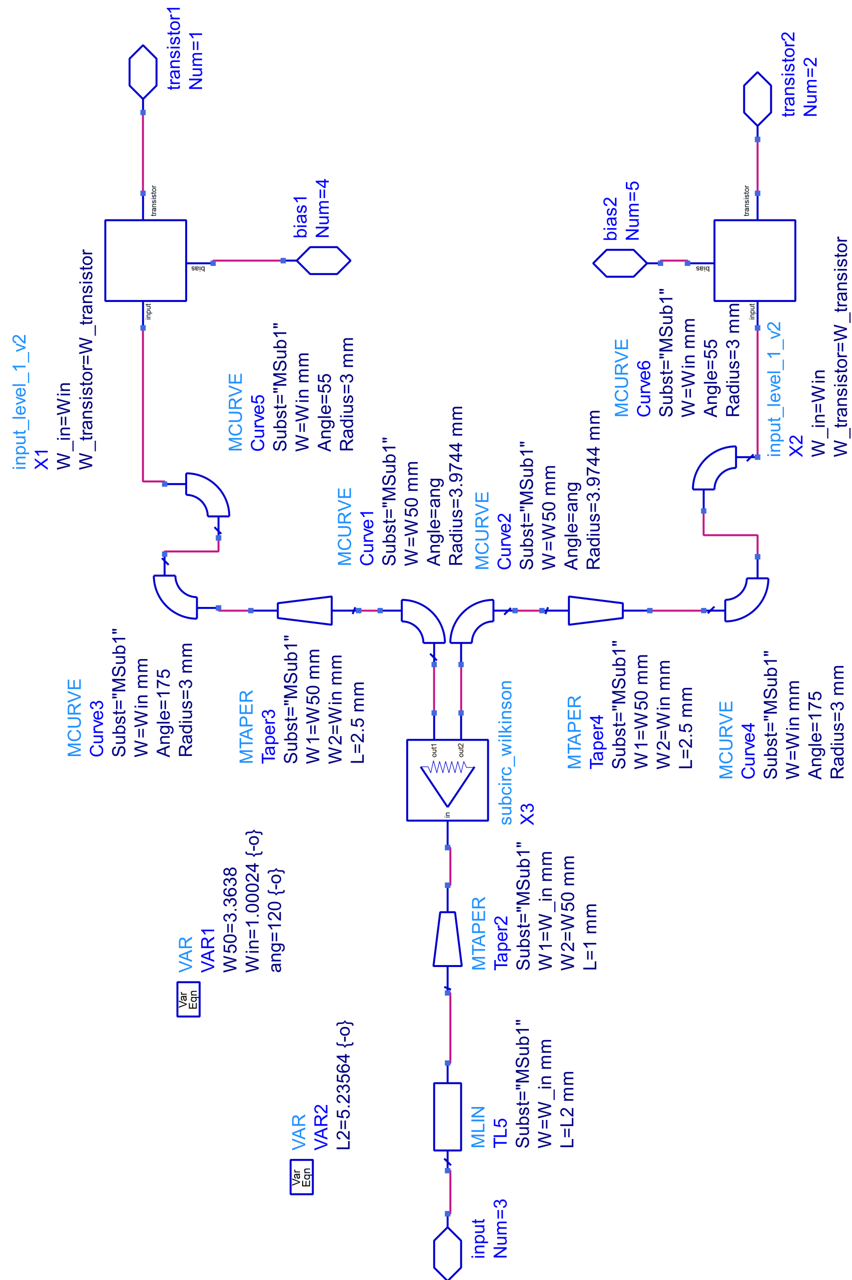


Figure B.3: ADS schematics of input level 2.

Figure B.4: ADS schematics of input level 3.

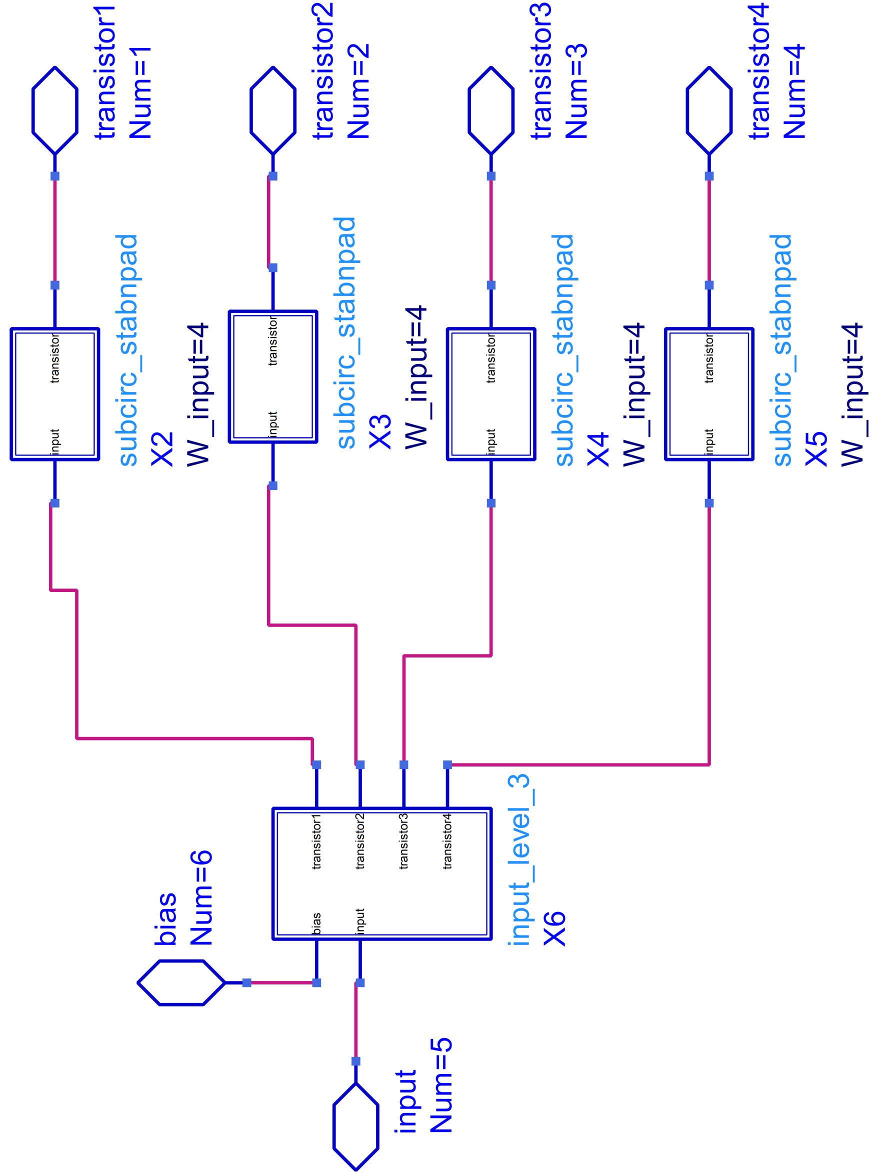


Figure B.5: ADS schematics of input level 4.

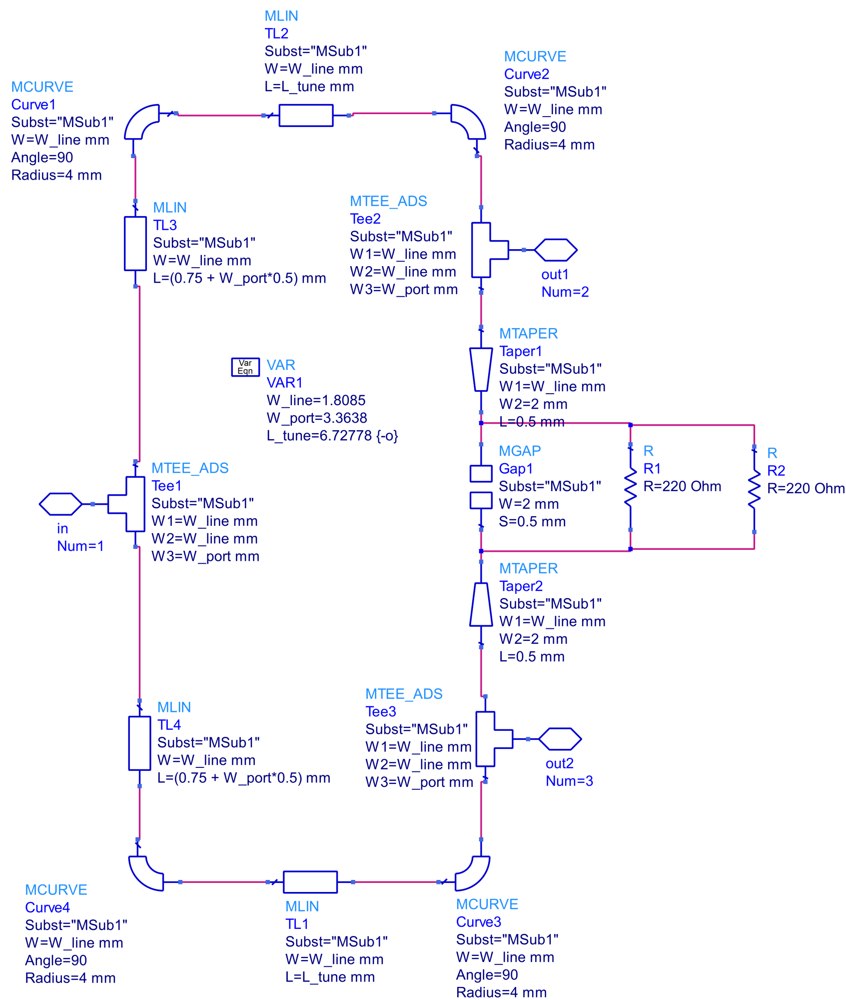


Figure B.6: ADS schematics of Wilkinson Power Divider.

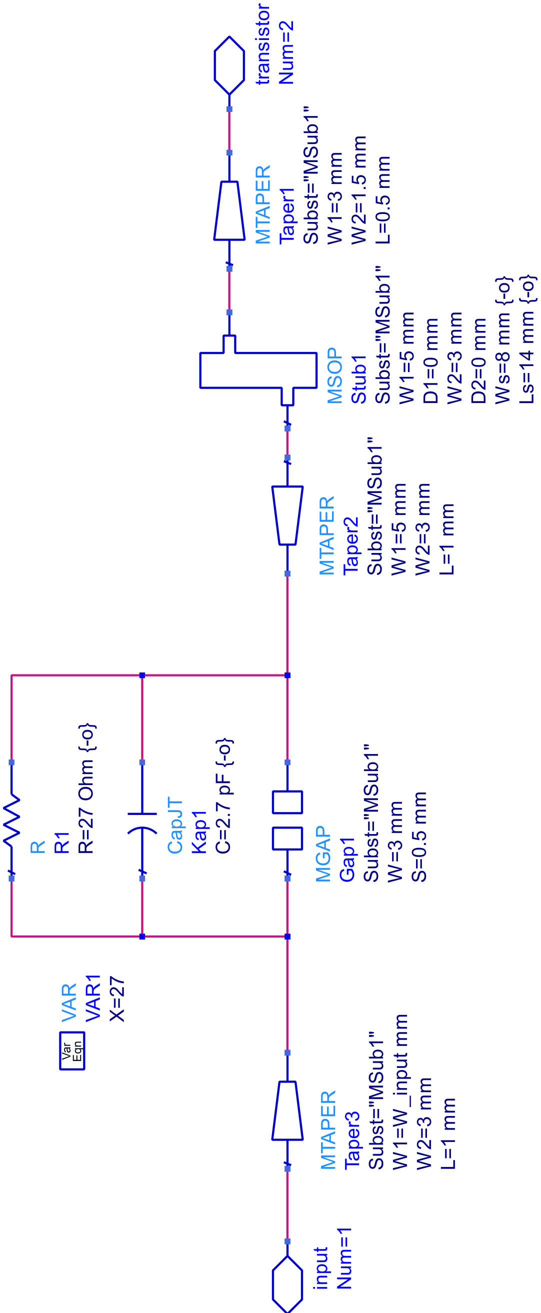


Figure B.7: ADS schematics of stability circuit and transistor pad.

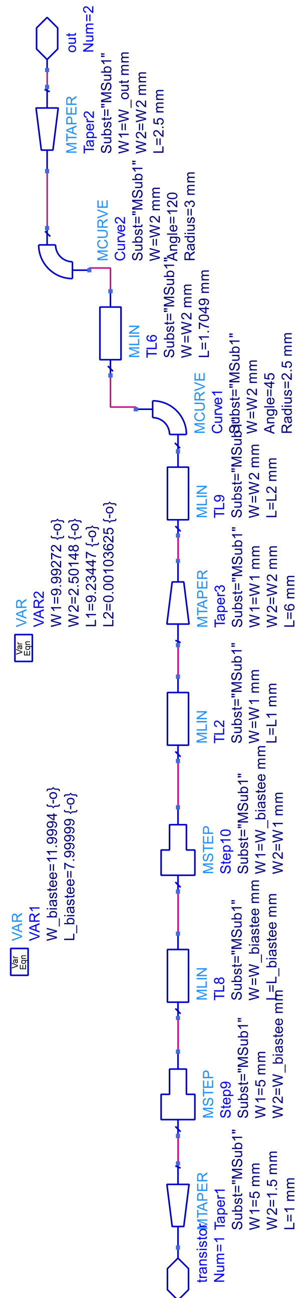


Figure B.8: ADS schematics of output level 1.

Figure B.9: ADS schematics of output level 2.

Figure B.10: ADS schematics of output level 3.

Appendix C

ADS testbenches

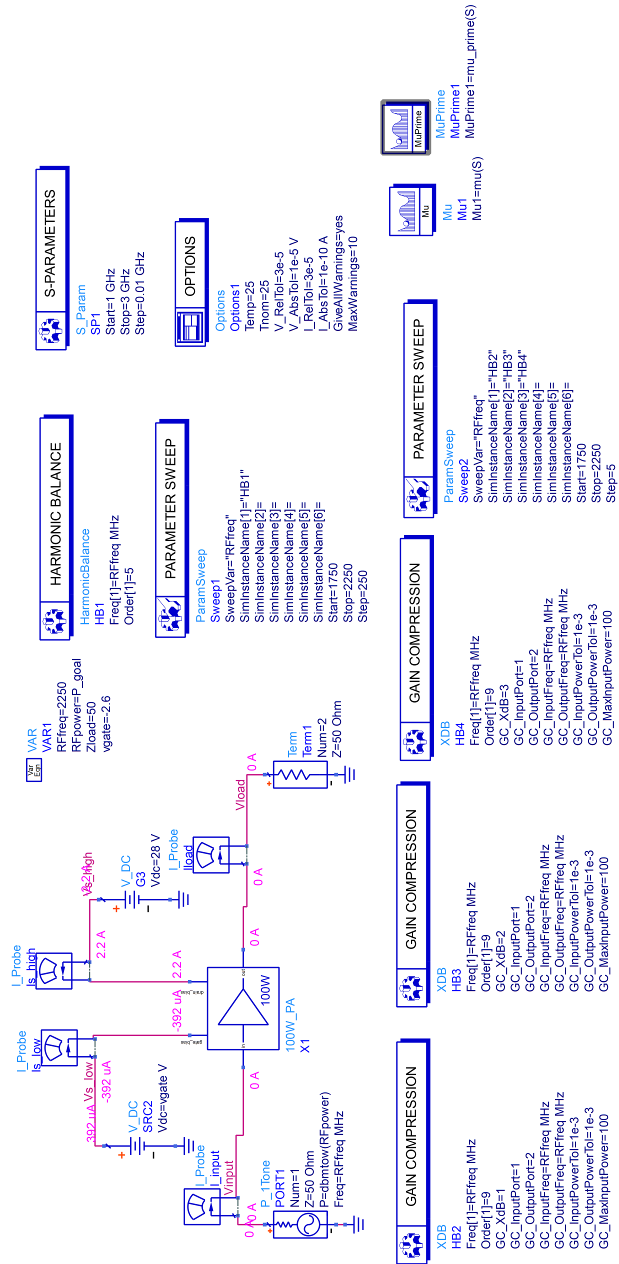


Figure C.1: Testbench for compression simulations.

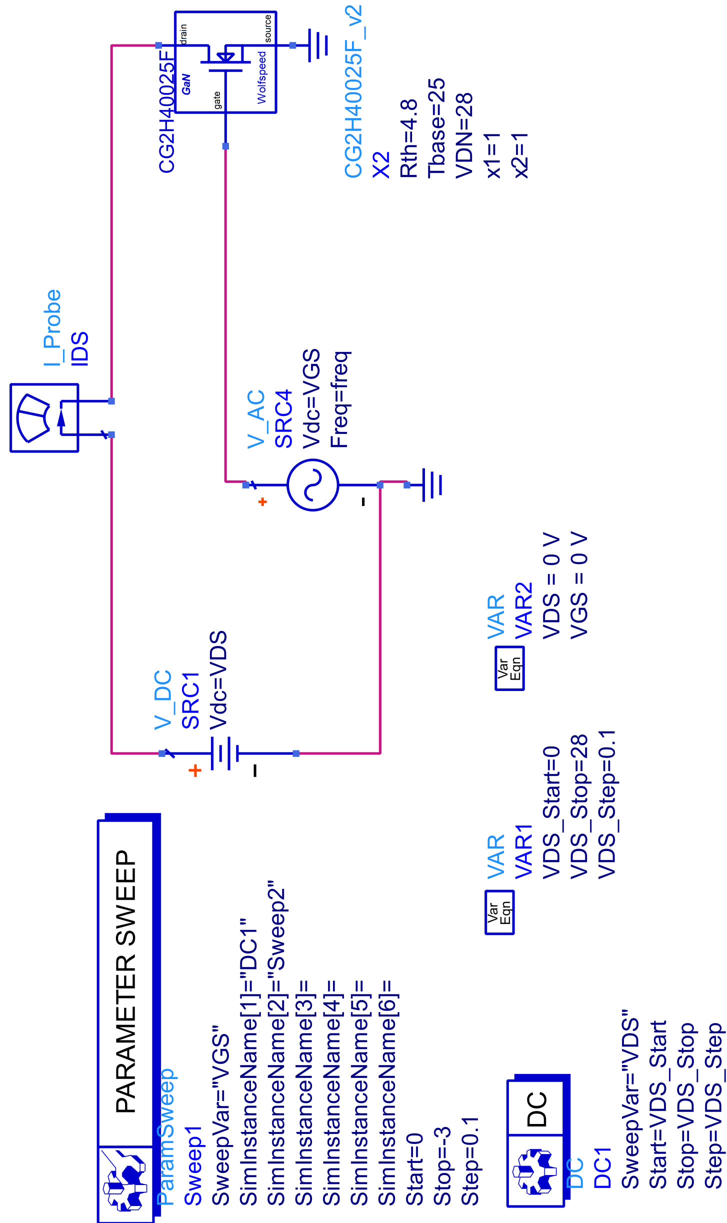


Figure C.2: Testbench for simulating DC characteristics.

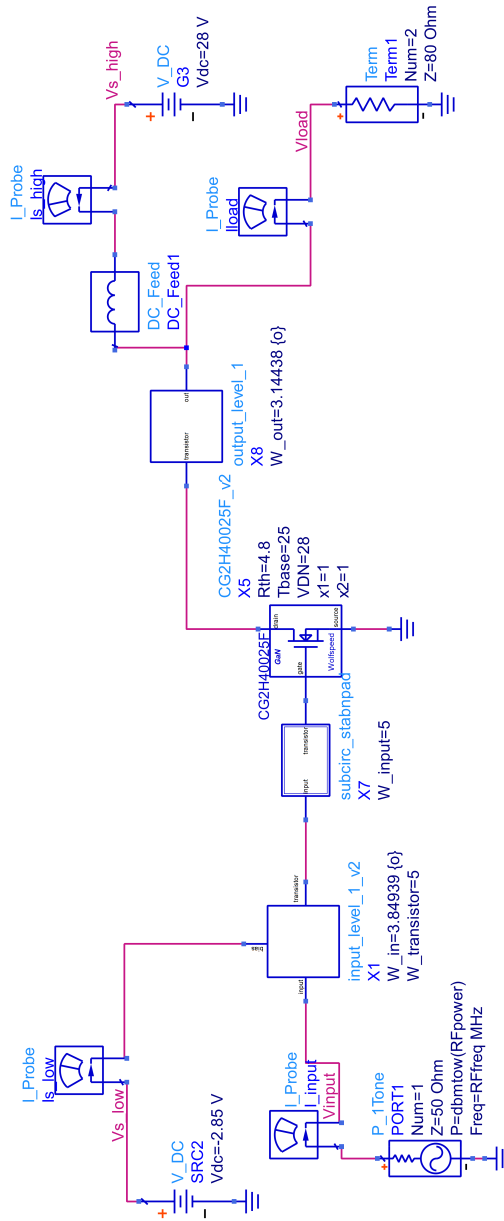


Figure C.3: Testbench for level 1.

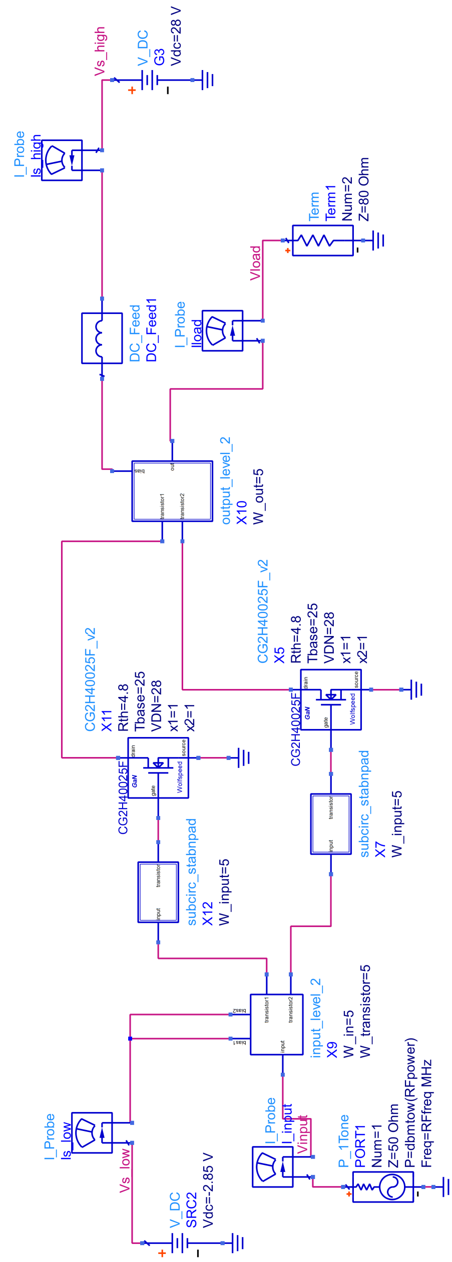


Figure C.4: Testbench for level 2.

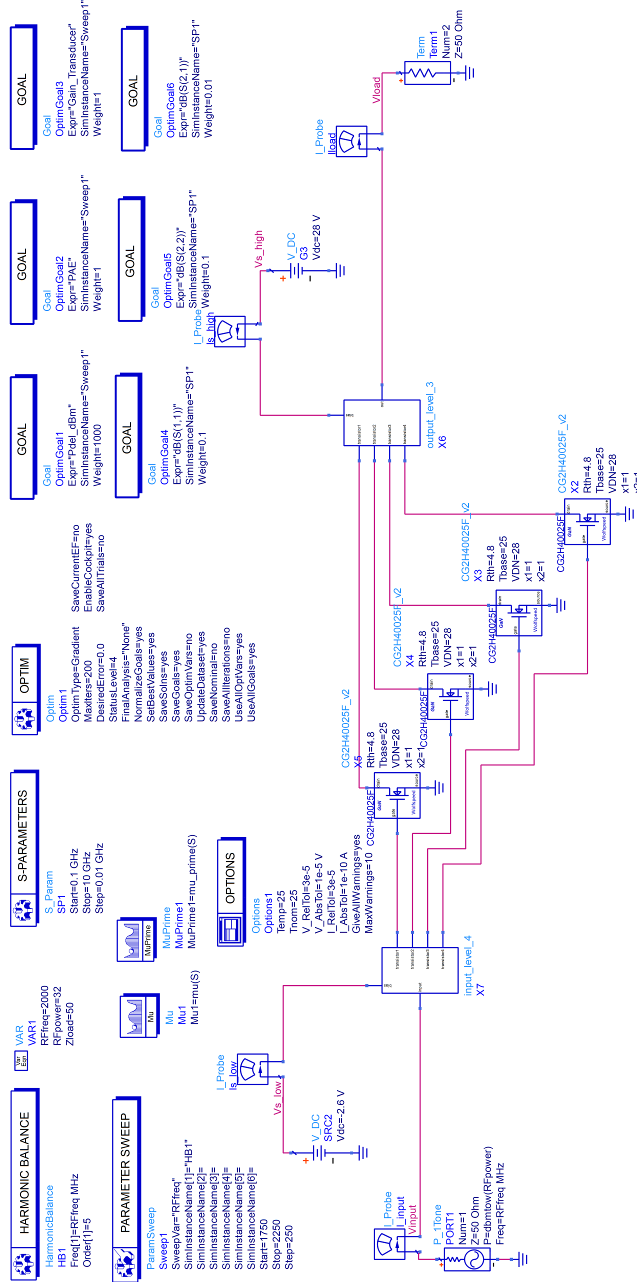


Figure C.5: Testbench for level 3/4.

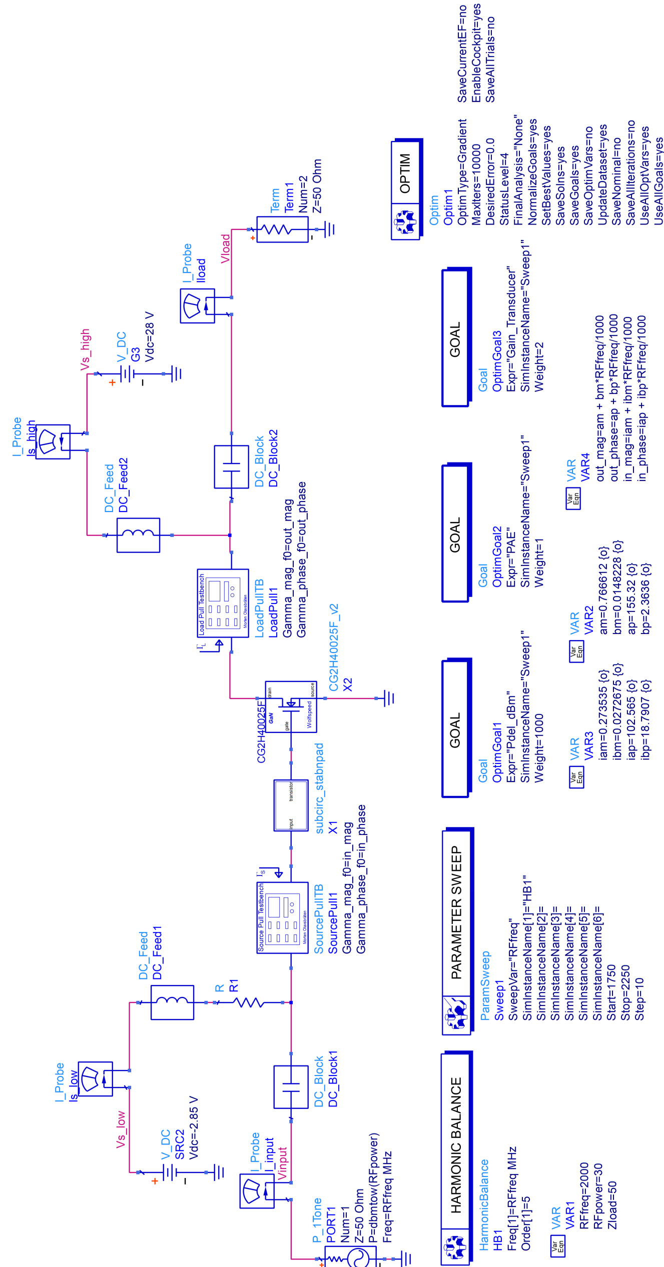


Figure C.6: Testbench for load-pull.

Figure C.7: Testbench for large signal stability.

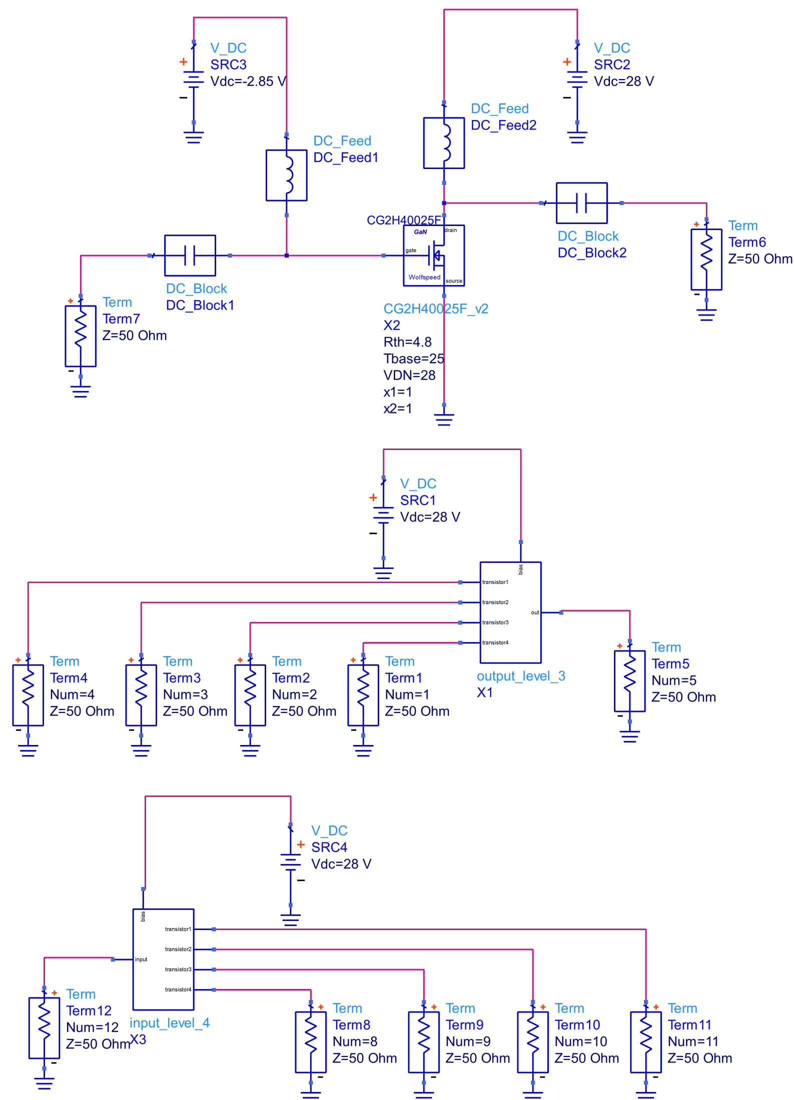
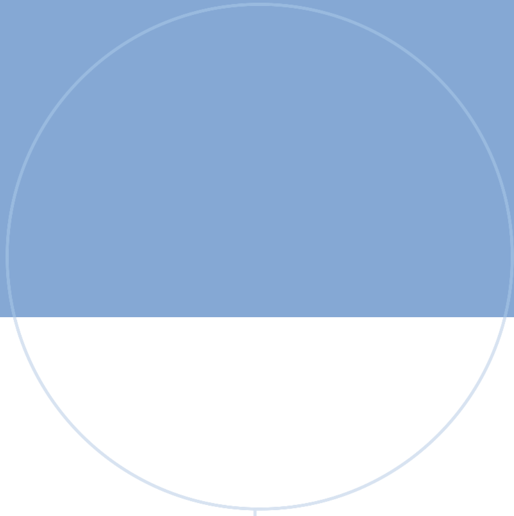
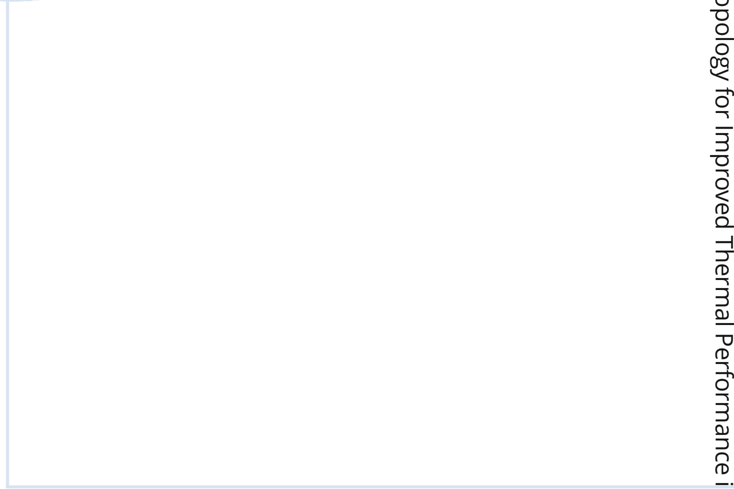


Figure C.8: Testbench for reflection coefficients.





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