Master's thesis

NTNU
Norwegian University of Science and Technology
Faculty of Information Technology and Electrical Engineering
Department of Electronic Systems

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Design of an RF Supply Modulator for use in Envelope Tracking

Master's thesis in MTELSYS
Supervisor: Morten Olavsbråten
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Abstract

Tomorrow's communication systems face the challenges to be both energy-efficient and able to send large amounts of information. A critical factor in achieving this is to find new ways of improving the systems.

This thesis explores a new design methodology for implementing a supply modulator for Envelope Tracking (ET), using Radio Frequency (RF) transistors. The idea behind the RF transistor is to be able to use a higher frequency for modulation, resulting in greater bandwidth. All designs are tested over three loads ranging from 50Ω to 150Ω.

Firstly, the rectifier module is designed and tested. The first design is self-injected and achieves an average efficiency of 75%. The system is produced on an FR4 substrate with a measured peak efficiency of 4%. The method is believed to be too sensitive, resulting in a mismatch in the realized circuit and causing the efficiency to disappear.

The rectifier is redesigned to allow for power injection. By injecting power, the goal is to reduce sensitivity. The circuit is designed on a higher performance substrate, RO4003. Simulations show the efficiency drops despite using a better substrate. A poorer matching circuit design for the rectifier with active injection seems to cause the efficiency to drop. Measurements find the system is able to rectify a signal, reaching efficiencies over 50% at peak.

The full RF supply modulator is implemented using an ideal class B amplifier to drive the rectifying element with active injection. The bandwidth is determined to be 90MHz on average for the three loads. The system reaches an average efficiency of 78%, delivering a minimum of 9.9W of power

Finally, the supply modulator is reoptimized to drive a single 30Ωload. This design reaches a peak efficiency of 80%, with an average efficiency of 78% in a 200MHz band. Despite being optimized for peak efficiency, the system performs incredibly well in a wideband test case.

The thesis proves that the system can be used as a supply modulator, but more testing is needed to verify the system's performance in an ET design.

Sammendrag

Fremtidens kommunikasjonssystemer må kunne sende store mengder informasjon, samtidig som de er enerigeffektive. For å lage slike system må nye måter å designe systemene på utvikles.

Denne masteroppgaven utforsker bruken av RF transistorer for å lage spenningsforsyningen i et ET system. Målet er å oppnå bedre båndbredde i et slikt design sammenliknet med design som allerede eksisterer. Alle design i denne oppgaven har en senterfrekvens på 2.9GHz, og er testet over tre laster i området 50Ω til 150Ω.

Først testes likerettingsmodulen i designet. Den første likerettingsmodulen er ikke injesert med et eksternt signal, og oppnår en simulert effekt på 75%. Systemet produseres på et FR4 substrat, og gir en målt effektivitet på 4%. Grunnen til det store avviket mellom simuleringer og målinger mistenkes å være på grunn av høy sensitivitet, kombinert med lav nøyaktighet i produksjon.

Likerettingsmodulen endres for å tillate injeksjon av effekt. Dette gjøres for å redusere sensitiviteten til designet. Substratet RO4003 brukes i dette designet, som skal ha bedre ytelse enn FR4. Simuleringer viser at de to designene har relativt lik effektivitet. Målingene viser at systemet virker bedre enn det uten injisert effekt, med en maks effektivitet på over 50%.

Spenningsforsyningen implementeres ved å kombinere likeretteren med injeksjon med en klasse B forsterker. Båndbredden for designet simuleres til 90MHz i gjennomsnitt. Systemet oppnår en gjennomsnittlig effektivitet på 78% for senterfrekvens, og leverer minst 9.9W effekt til lasten.

Spenningsforsyningen optimeres på nytt for å drive en 30Ω last. Ved å kun fokusere på en last oppnår systemet en effekt på 80% for senterfrekvensen, og har en gjennomsnittlig effektivitet på 78% over et 200MHz bånd.

Oppgaven viser at systemet kan brukes som en spenningsforsyning i ET, og utkonkurrerer andre spenningsforsyninger på båndbredde. Flere tester bør gjennomføres for å utforske ytelsen i mer realistiske testområder.

Contents

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Acronyms

λ wavelength. 7, 8, 14

AC Alternating Current. 7–9, 16, 28

ADS Advanced Design System. 15, 23

DC Direct Current. 7, 8, 11, 23, 30

DUT Device Under Test. 12, 27, 33, 34

ET Envelope Tracking. iii, v, 2, 8–11, 15

$\mathbf{f_0}$ center frequency. 8, 17, 23, 25, 34, 36, 51, 55

GaN HEMT Gallium Nitride High Electron Mobility Transistor. 2, 11, 17, 28, 53

MMIC Monolithic Microwave Integrated Circuit. 56

PA Power Amplifier. 1, 3, 4, 17

PCB Printed Circuit Board. 2, 21, 25, 31, 48, 55

PWM Pulse Width Modulation. 10

RF Radio Frequency. iii, 2–5, 7, 9–12, 21, 28, 33, 35, 36, 50, 51, 55

Chapter 1

Introduction

1.1 Motivation

It is hard to imagine a world without wireless communication. Today, over 60% of the world's population is online [1]. Keeping all these people connected poses some challenges regarding available power. Vodafone, for example, is reported to consume over 1 million gallons of diesel every day to keep their networks online in places where a power grid is unavailable [2].

One way to reduce the environmental harm caused by cellular networks is improving the networks' efficiency. It is estimated that the base station consumes 80% of the power in a cellular network, with 50-80% of this power being consumed by the Power Amplifier (PA) [3]. Improving PAs could therefore have an enormous impact on the environment. Reducing the power consumption of the network would also lower the cost of operation.

The efficiency, however, should not hinder the PAs ability to send information. System performance and efficiency often oppose each other as design goals, and the challenges of designing the wireless systems of tomorrow become apparent when both are equally important. Exploring new design techniques is crucial to finding a solution to this conundrum.

1.2 Scope of thesis

The goal of this thesis is to explore the possibility of designing a supply modulator using an RF transistor as the rectifying element. Conceptually, the design methodology for the RF supply modulator is initially proposed by A. Alt [4]. Transistor characteristics for reverse bias found in the project thesis are used in the design process [5].

A popular approach to supply modulation in envelope tracking is to use buck converters. The widespread use comes from their high efficiency, which makes them appealing in an efficiency-boosting technique such as Envelope Tracking (ET) [6]. The main drawback of the buck converter is the relatively low bandwidth the design can achieve. While the high efficiencies of the buck converter are not feasible with an RF supply modulator, the RF supply modulator has the potential to significantly outperform the buck converter on bandwidth.

The designs proposed in this thesis uses the Wolfspeed CG2H40010F GaN HEMT, which has its simulation model enhanced to behave according to measured IV-curves in sub-threshold operation [5].

The thesis proposes two approaches for the rectifying element: A self-injected rectifier and an active injection rectifier. Definitions of efficiency and bandwidth are presented to determine the system performance. The design characteristics are determined using computer simulations before producing and testing them in a laboratory. Each rectifier's efficiency is simulated and measured to determine which design is better over a range of load impedances. Different PCB substrates are also considered and tested.

Finally, an ideal RF supply modulator is created by combining a rectifying element with a class B amplifier design. The system is simulated for peak efficiency and swept over a frequency range to explore the design's wideband performance. A comparison is made with a buck converter design to gauge the performance of the RF supply modulator [6]. The RF supply modulator is reoptimized to match the Buck converter's parameters closely.

Chapter 2

Theoretical background

As this thesis is a continuation of the work presented in the project thesis, parts of the theoretical background are taken from there [5]. However, the parts reused are modified, with some additions to ensure the theoretical background covers the more extensive work presented in this thesis.

2.1 Amplifier classes

Power Amplifiers (PA) are a key component in RF systems. Their main goal is to increase the magnitude of an incoming signal. There are several different ways of designing PAs, each one having different strengths and weaknesses. Two groups of PAs exist; linear and non-linear amplifiers. For each group, classes exist that further determine the characteristics of the amplifier.

There are four different classes defined as linear: A, AB, B, and C. The linear PAs tries to preserve the waveform of the input signal. Thus, the output of such an amplifier is ideally just the input signal with increased amplitude.

The main differentiator between the linear amplifier classes is the operating point used by each class. The operating point will determine how much of the amplifier's signal cycle will remain in the active region.

Suppose a bias point ensures the amplifier is active 100% of the time. Conduction 100% of the time is equal to a conduction angle of 360°. An amplifier with a 360° conduction angle is known as a class A amplifier [7].

The class A amplifier achieves low distortion at the cost of low efficiency. Lowering the conduction angle makes it possible to increase the efficiency, although the distortion will increase. By using a conduction angle of 180°, which equals conduction 50% of the signal cycle, a class B PA is made [8].

It is also possible to bias the amplifier between these conduction angles, which is called a class AB PA. This configuration will have a conduction angle between 180° and 360°. It is also possible to reduce the conduction angle further from B, which will result in a class C PA.

Figure 2.1 displays the different linear amplifier classes, with their conduction angles and ideal peak efficiency.

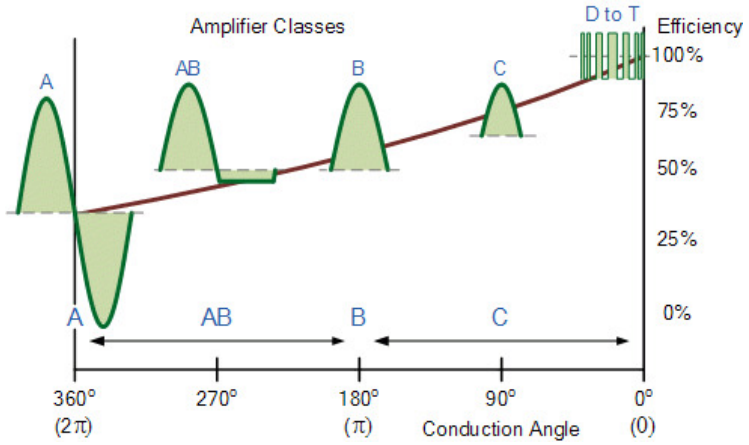


Figure 2.1: Conduction angle and efficiency for amplifier classes [7].

The non-linear amplifiers implement different forms of switching to increase efficiency further. Some frequently used non-linear classes are D, E, and F. Ideally, they can reach an efficiency of 100% [8].

2.2 S-parameters

S-parameters are one way of describing the small-signal characteristics of an RF system. The parameters determine how an incident wave is reflected on a system port for a given frequency [9]. The method of analyzing systems does not rely on open- and short-circuit states but instead uses matched loads to characterize the system [10]. An example of the S-parameters for a two-port system is shown in Figure 2.2.

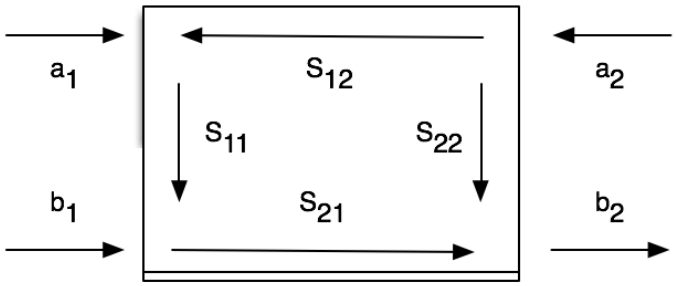


Figure 2.2: Definition of S-parameters for 2-port system [11].

The S-parameters for a circuit are denoted by a large S, including two subscript numbers. The first number denotes the reflected port, and the second number gives the incident port. For example, S_{11} describes the reflection at port one from an incident wave at the same port.

2.3 Impedance Matching

In RF systems, different modules are combined to create a system with the desired specifications. The impedance of each module is rarely the same, which is known as a mismatch. Mismatch in a system will lead to reflections, causing power loss and may add noise. It is possible to mitigate this loss of power through impedance matching. Usually, an impedance network connects the source and load. The impedance network ensures the impedance seen from the generator is equal to the system's characteristic impedance, maximizing the power transferred to the load [9].

The source and load impedances will have positive resistance in almost all cases. However, the complex value can be either positive or negative. When matching, different components will tune the impedance from a complex impedance to a given reference load, known as the characteristic impedance. The characteristic impedance is generally 50Ω or 75Ω. Different circuit components alter the network to ensure a perfect match between source and load. Impedance matching is either done with lumped components or transmission lines.

It is possible to visualize how the impedance of a system will change by using a Smith chart, shown in Figure 2.3. The chart is created by wrapping the y-axis containing the imaginary values around the positive x-axis, denoting the real values. Real negative loads are impossible to realize with passive components, so they are omitted from the chart. The center of the Smith chart is the characteristic impedance of the system, with the far left being a short circuit and the far right

being an open circuit. The top half contains inductive loads, with the bottom half containing capacitive loads [12].

Adding impedance and admittance lines to the chart makes it easier to visualize how different components will affect the system's performance. Reactive components in series will follow the impedance lines and shunted reactive elements follows admittance lines.

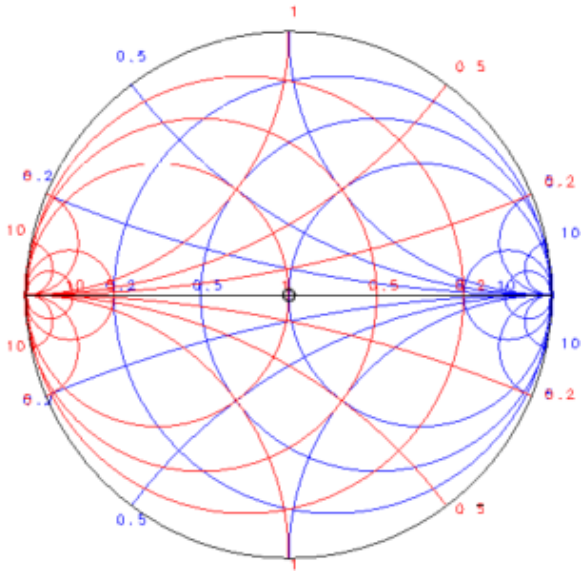


Figure 2.3: The Smith Chart, obtained using ADS.

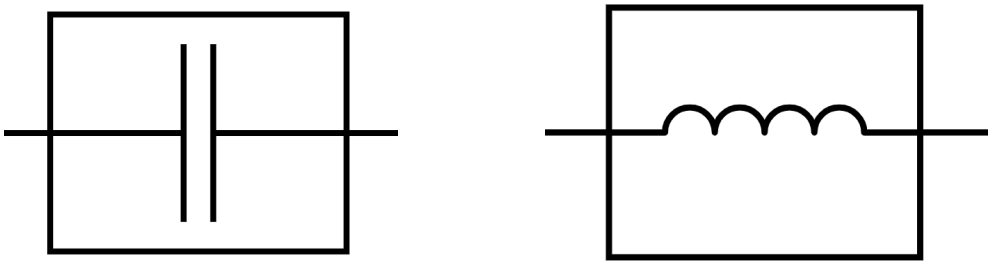
A lumped component may pose design challenges for high-speed systems, as their frequency response is far from ideal for higher frequencies. Frequency dependency is especially challenging with coils, as high frequency will accentuate the capacitive effect between each coil turn, changing the frequency response from inductive to capacitive.

Transmission lines omit some of the design challenges posed by lumped components. While a transmission line also is frequency-dependent, it has less prominent parasitic effects than lumped components. Thus, it is possible to use them to match at higher frequencies.

A transmission line connected in series with the load will result in a phase change. In the Smith chart, this corresponds to moving radially around the center of the chart. Lines can also be connected as stubs, being either open circuits or connected to ground. These stubs will behave as capacitive and inductive elements, respectively, and will transfer the impedance along the admittance lines of the Smith chart.

2.4 DC blocks and DC feeds

When designing RF circuits, it is important to remove the possibility of interference between the RF signals and the DC voltages in the system. Ideally, no AC signal should be present at DC sources, and no DC should be available at the AC input. The circuit components that enable the separation of AC and DC are known as DC blocks and DC feeds The schematic symbols used for the two designs are shown in Figure 2.4.



(a) Schematic symbol for a DC block.

(b) Schematic symbol for a DC feed.

Figure 2.4: Schematic symbols for DC block and feed.

The DC block is the simplest of the two to implement. By connecting a capacitor in series with the signal line, the DC voltages are unable to enter the AC lines. The impedance of a capacitor is given by:

$$Z_C = \frac{1}{j\omega C} \tag{2.1}$$

Since the AC frequencies of the system generally are in the GHz range for RF systems, the load of the capacitor used as a DC block becomes negligible. I.e., no observable attenuation of the signal is experienced from the capacitor. However, it is crucial to be aware of parasitic capacitances and inductances of lumped components. As the frequency increase, the parasitic impedance can dominate, completely changing the frequency response of the component.

A more complex topology is needed to realize the DC feed. One way of designing a DC feed is using two quarter-wave ($\lambda/4$) transmission lines, configured as shown in Figure 2.5. To further attenuate AC signals, shunted capacitors and coils in series can be implemented. Generally, it is beneficial to use different types of capacitors with capacitances of different orders of magnitude to attenuate a range of frequencies better.

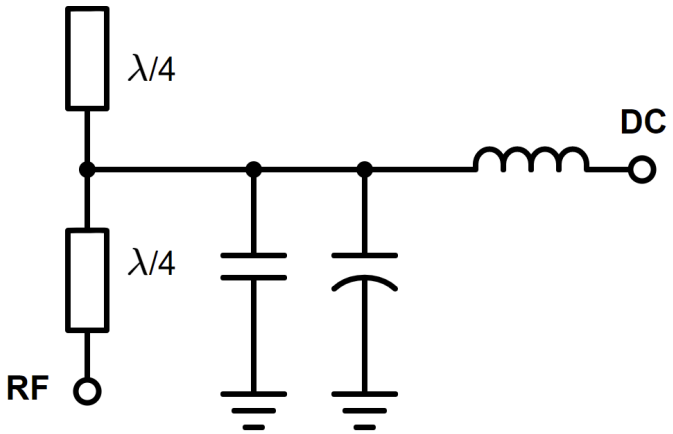


Figure 2.5: DC feed circuit.

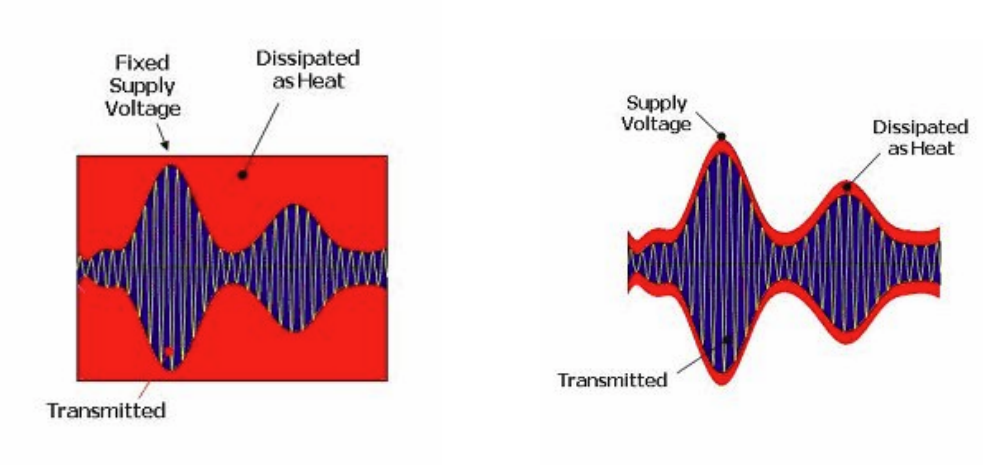
This design will ensure the center frequency (f_0) behaves as if the load is an open circuit, which will prohibit the signal from reaching the DC line. Plotting this in the Smith chart will show that the $\lambda/4$ lines will move the impedance of the line from short circuit to open circuit, ensuring a high impedance. The stub will further attenuate the AC in the DC node, as it will phase shift the signal back to open circuit. As λ is frequency dependent, this will only work perfectly for f_0 in the circuit.

2.5 Envelope tracking

In its simplest mode of operation, an amplifier will receive a single tone signal at its input. The signal will be amplified as efficiently as possible by driving the amplifier close to compression.

Unfortunately, modern modulation schemes ensure that the signal varies greatly in amplitude throughout a signal cycle. If a fixed power supply drives the amplifier, as shown in Figure 2.6a, the excess power is lost as heat. A way to mitigate this is to implement a variable power supply. By allowing the supply voltage to swing following the input signal, the amplifier is always driven close to compression. Figure 2.6b show how a lot less power is lost in heat dissipation, thus increasing the efficiency of the system.

Envelope Tracking (ET) is an efficiency-boosting technique implementing a variable supply voltage. ET uses the envelope of the signal to determine the amount of voltage needed to drive the system. As the envelope will change continuously throughout the signal cycle, the timing constraints on an envelope-tracked system are strict.



(a) PA with fixed supply voltage. **(b)** PA with ET architecture.

Figure 2.6: Reduction of heat dissipation using ET [13].

A suggested architecture for an envelope-tracked system is shown in Figure 2.7. The RF input is read by the supply modulator, either by digitally generating the envelope or extracting it directly from the AC signal. The supply modulator then rectifies the signal and generates an output value used to drive the amplifier.

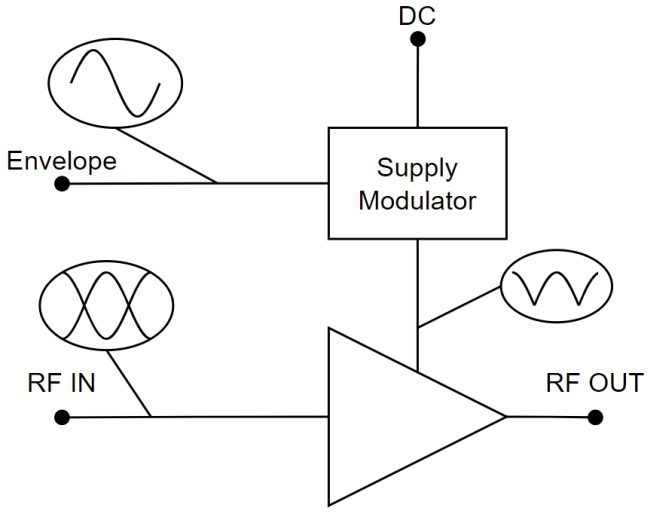


Figure 2.7: Block diagram of an Envelope Tracking system.

Ideally, this method of efficiency-boosting will not add any distortion to the signal. As the efficiency is handled externally from the signal amplifier, the main focus of the amplifier design is linearity. Thus, classes A, AB, B, or F are common in ET systems.

2.6 Supply modulation

As the concept of ET is dependent on being able to modulate the supply voltage to increase system efficiency, the supply modulator in Figure 2.7 is a crucial component of the architecture.

Precise timing is essential for envelope tracking. Efficiency is not increased if the modulation is high when the signal is low. On the other hand, if the signal is high and the modulation is low, the signal will be distorted. Thus, the timing of modulation is an essential factor. In modern systems, a digital signal processor handles the timing.

The efficiency of the supply modulator is also essential. If the supply modulator is inefficient, nothing will be gained from implementing it.

Finally, the modulator should have a large bandwidth. The bandwidth will determine how closely the supply modulator can follow the signal amplitude. A larger bandwidth enables the supply modulator to change its output more rapidly, which allows for a more efficient system overall.

As described in section 2.5, the supply modulator uses the magnitude of the input signal to determine the output power delivered to the amplifier. As the signal is a complex value, the magnitude can be found as shown in Equation 2.2.

$$|z| = \sqrt{a^2 + b^2} \tag{2.2}$$

By taking the square root of the complex signal, the bandwidth is infinitely large [14]. If the supply modulator has to track this perfectly, it would need an infinite bandwidth. In a physical system, this is not possible but emphasizes the importance of the supply modulators' bandwidth.

One way of implementing the supply modulator is to use buck converter designs. The main reason is that these designs have the best efficiency of the known supply modulation techniques. Their main drawback has historically been their limitations in bandwidth, which reduces their compatibility with high-speed systems.

2.7 RF supply modulation

This paper explores a different way of implementing the supply modulator than the buck converter. Instead of using a PWM signal and switching the transistors quickly on and off, RF supply modulation relies on using an RF transistor as a rectifying element. The expectation is for the supply modulator to outperform the buck converter on bandwidth at the cost of some efficiency.

2.7.1 RF transistor as rectifying element

For an ideal half-bridge rectifier, the rectifying element would ensure complete power transmission for one polarity while completely negating the power of the opposite polarity to flow to the load. In non-RF designs, this can be implemented simply by using a diode.

In ET designs, however, using a single diode may prove to be complicated. RF diodes are often limited in maximum current rating, which makes them unable to rectify the power needed in an ET system. However, RF transistors are also able to rectify the signal. As RF transistors can withstand higher power consumption by design, readily available components may be used to realize an RF supply modulator [4].

Figure 2.8 compares the IV curves of a diode to a GaN HEMT. When designing the system, using a transistor to rectify the signal introduces an additional degree of freedom. While the diode's breakdown is constant, the gate voltage of the transistor can be changed to enable the transistor to work more ideally as a rectifier. By decreasing the gate voltage for positive input voltage, the transistor will not conduct, thus not transferring any power. In the opposite case, an increase in gate voltage will let more current go through the transistor, thus letting more power flow to the drain of the transistor.

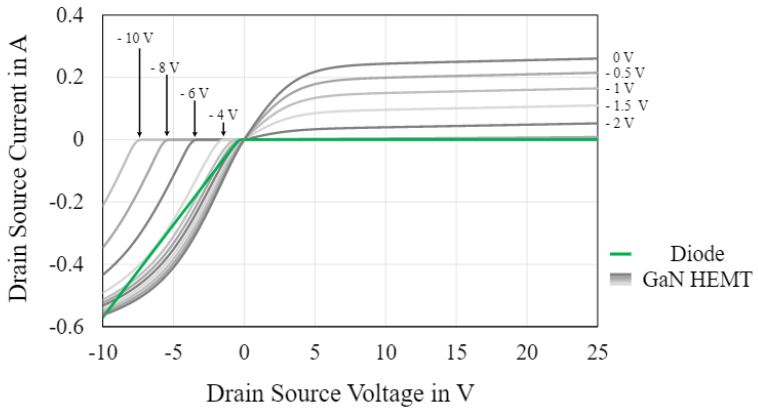


Figure 2.8: IV-curves for a GaN HEMT compared to a schottky diode [4].

2.7.2 System design

The setup of the supply modulator consists of two RF transistors, which mirror each other. The first transistor works as the amplifier, whose input is the envelope signal of the transmitted signal in the system. The second transistor rectifies the amplified signal by driving the amplifier in reverse. It can have a purely DC gate

bias, or an RF signal can be applied to accentuate the rectifying behavior.

The rectified signal is transmitted to the load from the drain of the second transistor. For a real implementation of a supply modulator, this would be the signal amplifier in the system. A suggested RF supply modulator design is shown in Figure 2.9.

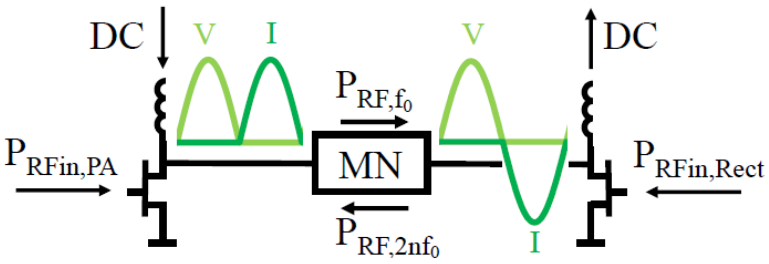


Figure 2.9: RF supply modulator [4].

The operation frequency of the supply modulator does not necessarily need to coincide with the transmitted signal in the amplifier. By choosing a different frequency, it is easier to filter out the frequencies from the supply modulator to reduce the noise on the transmitted signal [4]. This way of implementing a supply modulator aims to improve the bandwidth of the supply modulator compared to a buck converter design.

2.8 Lab equipment

Some extra components are needed to do measurements and drive the Device Under Test (DUT) without risk of harming other equipment. Some of these components are described below.

2.8.1 Circulators

An RF circulator is a component designed to only allow power to flow in one direction. Circulators often consist of three directional ports. A general schematic symbol for a circulator is shown in Figure 2.10.

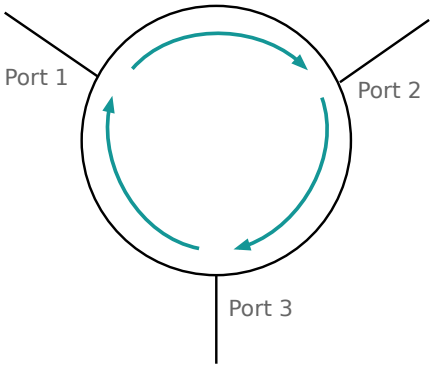


Figure 2.10: Schematic symbol of a circulator [15].

Power entering port one will be transmitted to port two with low loss. If the wave is reflected and returned to port two, the power returned will be isolated from port one and instead be transferred to port three. This is useful as the components connected to port one now are isolated from port two, reducing the risk of harming them.

A special case of the circulator is an isolator, where port three is terminated to a load. The reflected power from port two is in this case automatically burnt up in the resistor.

2.8.2 Directional coupler

A directional coupler is a component that only allows transmitted signals to travel in one direction. A schematic symbol for a directional coupler is shown in Figure 2.11.

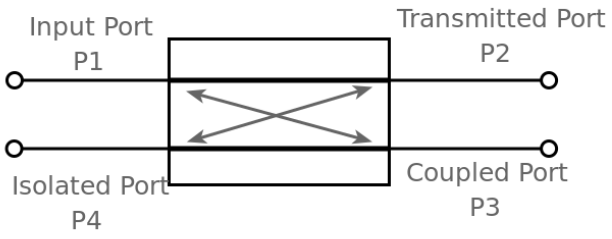


Figure 2.11: Schematic symbol of an RF coupler [16].

The coupler has four ports. The input is transmitted to the coupled port, which functions as the output for the coupler. The signal is also found on the transmitted port, although attenuation is experienced from the input. The isolated port is

coupled to the transmitted port but isolated from the input. The relation between the coupled port and the isolated port is the same as the input and transmitted port.

2.8.3 Wilkinson power divider

A Wilkinson power divider is a circuit element that splits the input power into two ports that are isolated from one another. Usually, the signal in a Wilkinson power divider is split evenly, which means each output port has the input level reduced by -3dB. The power divider has all its ports matched as well.

The design of the Wilkinson power divider is made up of two $\lambda/4$ transmission lines, with a characteristic impedance corresponding to $\sqrt{2} \cdot Z_0$. The lines are terminated to one another using a resistor with $R_L = 2 \cdot Z_0$ [9].

Chapter 3

Method

The electronic design software Advanced Design System (ADS) is used throughout this work. Circuit design, simulations, and layout are all made with ADS.

3.1 Efficiency

As ET is an efficiency-boosting technique, the modules needed to implement the design technique have to enhance the overall efficiency of the system. If no efficiency is gained, there is no benefit to implementing ET. In this thesis, a few different definitions of efficiency is used to determine the usefulness of the designs. The definitions are determined from a physical point of view, calculating the efficiency from what power is applied against the power returned.

The power over a load with a given value can be found by measuring the voltage. From the voltage and impedance value, the power can be found as shown below:

$$P_L = \frac{V^2}{Z_L} \tag{3.1}$$

If the power over the load is known, efficiency can be determined. The simplest case is the self biased rectifier. As the only non-negligible power applied to the system is the input signal, the efficiency is defined as follows:

$$\eta_{rect} = 100\% \cdot \frac{P_L}{P_{in}} \tag{3.2}$$

Where P_{in} is the input power and P_L is the power measured over the load.

If AC power is injected on the gate of the rectifying element, it has to be taken into account when calculating the efficiency of the system. Let P_{inj} denote the injected power applied to the rectifier. The formula for calculating the efficiency then becomes:

$$\eta_{rect,inj} = 100\% \cdot \frac{P_L}{P_{in} + P_{inj}} \tag{3.3}$$

Figure 3.1 displays the input- and output power in the rectifying element. In the first case with self-injection, it is assumed that $P_{inj} = 0$. The power not measured on the output, P_{diss} is dissipated as heat.

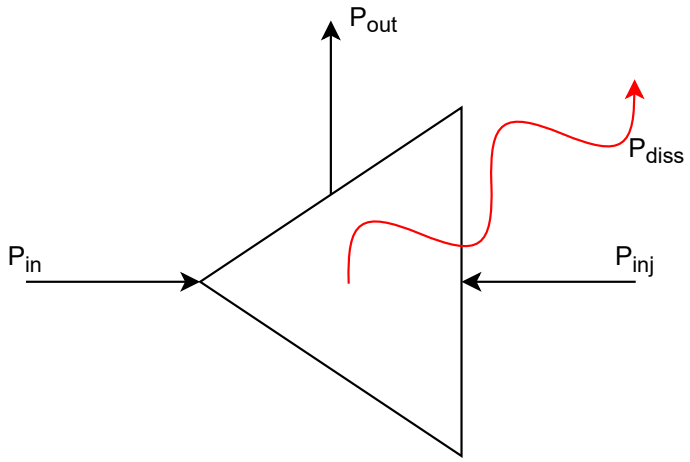


Figure 3.1: Input- and output power in the rectifier.

Finally, if the complete supply modulator efficiency is to be determined, the power consumption of the amplifying stage also has to be considered. To drive the amplifier, an additional source P_{DC} is needed. The overall efficiency of the supply modulator is found by including the power consumption generated from driving the amplifying stage to Equation 3.3:

$$\eta_{PAE} = 100\% \cdot \frac{P_L}{P_{DC} + P_{in} + P_{inj}} \tag{3.4}$$

3.2 Bandwidth of efficiency

As stated in subsection 2.7.2, a relative -3dB bandwidth of 5-10% of the center frequency is considered narrowband for an RF amplifier.

A rule of thumb used for narrowband PAs states the -3dB bandwidth generally is 5-10% of the systems center frequency (f_0). Intuitively, using the same components and design techniques in the supply modulator, it is reasonable to assume it would result in a bandwidth performance similar to the one achieved for an amplifier. However, it makes little sense to determine bandwidth this way when the critical parameter of the system is efficiency instead of output power. As a crude way to determine the system's bandwidth, this thesis defines it as the frequency range in which the loss of efficiency is less than 10%.

3.3 Operation frequency

Choosing center frequency (f_0) is crucial to designing the supply modulator. As stated in subsection 2.7.2, the frequency does not have to coincide with the transmitted signal. By choosing a different frequency, filtering out noise from the supply modulator becomes easier if chosen carefully. By considering this, a frequency of 2.9GHz is chosen. For a 5G design, this frequency is not used, which makes it ideal for the supply modulator [4]. For $f_0 = 2.9$GHz, the rule of thumb would yield an approximate bandwidth of 100-200MHz.

The frequency is also previously used to design the RF rectifying element for a supply modulator [5], making a comparison of results easier.

3.4 Transistor choice

The transistor used in this thesis is the Wolfspeed CG2H40010F GaN HEMT. Computer analysis of the system's behavior is essential before measuring its performance in a laboratory. For such an analysis to be valuable, the transistor characteristics must be correct for the region of operation. Computer analysis has previously proved challenging, as this transistor is not modeled for sub-threshold operation initially. Using previously measured characteristics for the transistor using below threshold gate voltages makes it possible to create a model that correctly describes transistor behavior in this range of operation [5].

3.4.1 Improved transistor models

Morten Olavsbråten designed the improved transistor models used in this thesis.

Reverse bias functionality

The new transistor model is shown in Figure 3.2. The model is usable in reverse bias by adding a diode between gate and drain, which emulates the breakdown

measured on the device. The diode parameters are optimized to equal the measured IV curves from the project thesis [5].

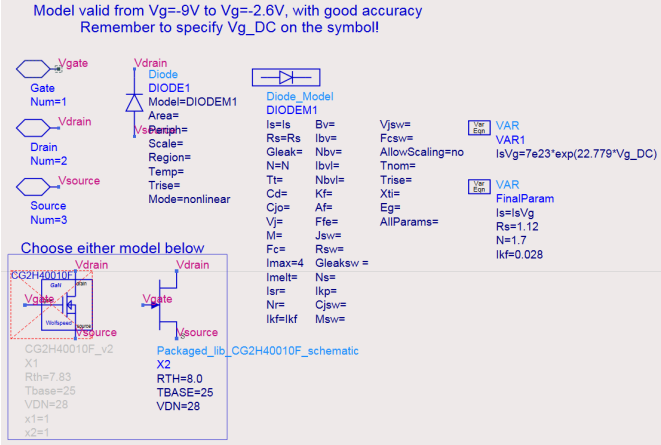


Figure 3.2: Modified transistor design to enable reverse bias.

Internal voltage accessibility

Iterating on the first transistor model allows for accessibility of the internal voltages and currents in the model. By adding parasitic components with simulated negative values compared to the actual parasitics in the transistor, it is possible to find internal values without altering the characteristics of the model. Figure 3.3 shows the new transistor model. Allowing for the internal values to be measured also places the diode more correctly relative to the parasitics of the transistor package.

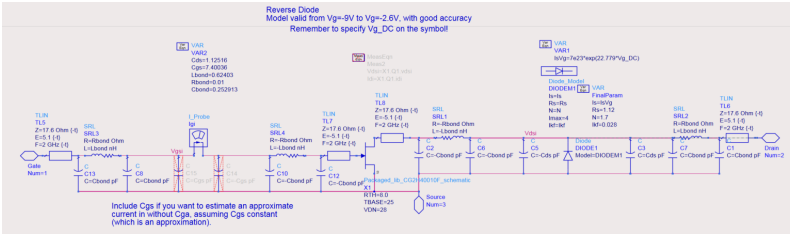
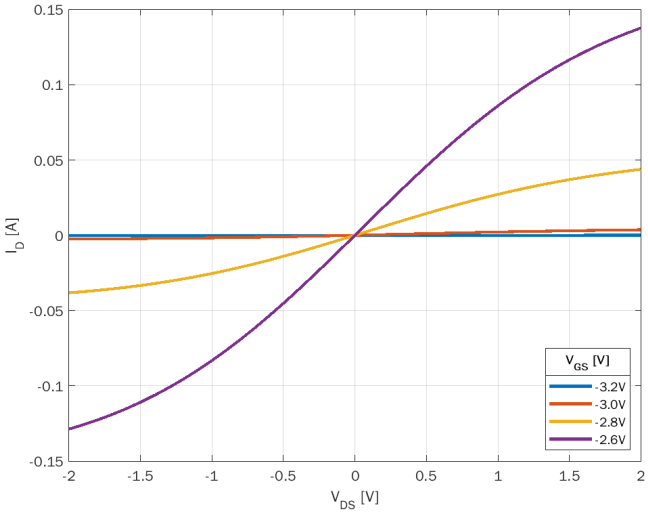
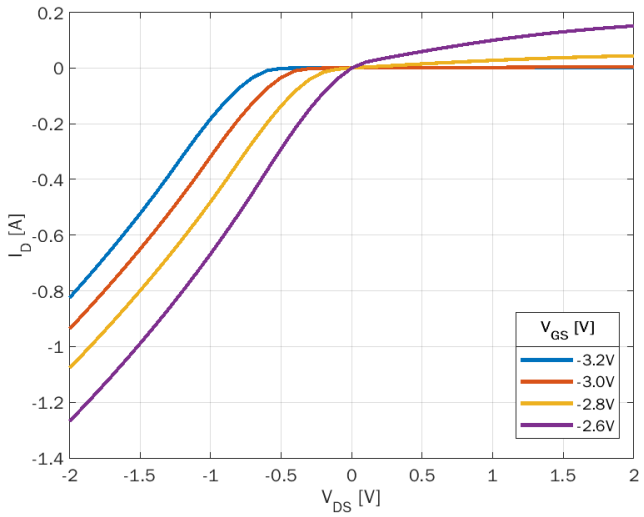


Figure 3.3: Modified transistor design to enable probing of internal parameters.

Finally, Figure 3.4 display the simulated IV curves of the unmodified model from Wolfspeed compared to the one with reverse bias compatibility. For the unmodified model in Figure 3.4a, the IV curves seems to be mirrored at the x-axis. For V_{GS} below threshold the model also simulates zero I_D for all values of V_{DS}. Figure 3.4b Shows a breakdown for negative I_D which more closely resembles the behaviour shown in Figure 2.8. The modified transistor is valid for -9V $< V_{GS} <$ -2.6V.



(a) IV curves of unmodified transistor model.



(b) IV curves of modified transistor model.

Figure 3.4: Unmodified and modified transistor model IV curves.

3.5 Source- and load-pull modules

Knowing how well a design may perform with the chosen transistor when creating the system is valuable. By simulating the system using ideal matching circuits, it is possible to determine a benchmark of how well the system could work when implementing transmission lines.

Source- and load-pull modules designed by Morten Olavsbråten help realize the ideal designs. The modules are two-port systems that can simulate the parameters of a matching circuit. Each module emulates matching circuits by determining the signal's reflection factor and phase change for the fundamental tone, second and third harmonics.

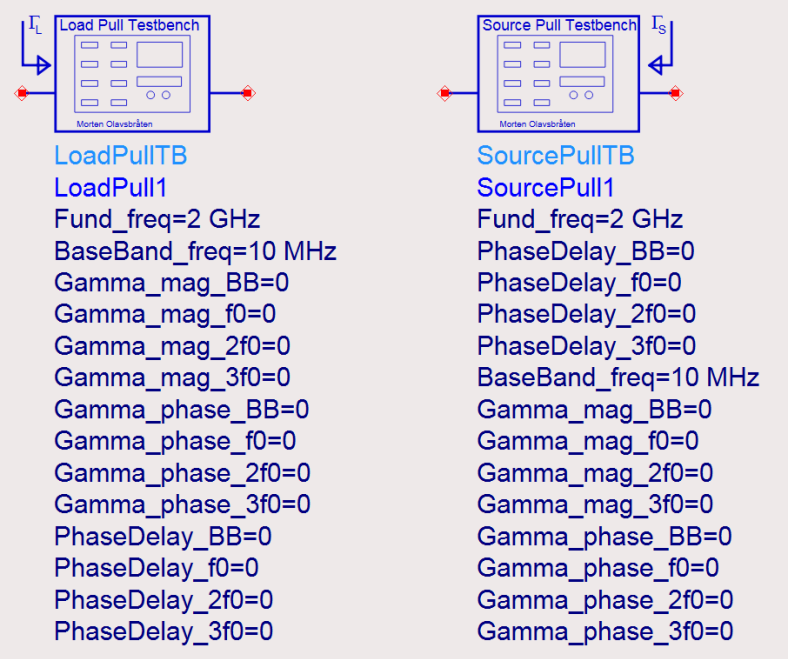


Figure 3.5: Source- and load pull design modules.

The source- and load-pull modules are revised during the thesis to include the possibility of calculating the phase delay through the module. Figure 3.5 show the second revision, which includes the extra variables for phase delay.

3.6 Sensitivity analysis

An optimal value is found for the circuit parameters when designing a circuit. While the highest efficiency is desirable, it may not be the best choice for the design in question. In some cases, a manufacturer may not be able to create the system to the specifications set during simulations. Inaccuracies in production, and variance in substrate parameters can alter the system performance.

The sensitivity analysis aims to find how large the room for error is before the performance suffers greatly. This thesis determines the sensitivity after optimizing the source- and load-pull modules to what is assumed to be the best performance the system can achieve. When optimizations are complete, each parameter is changed

individually to check how significant alterations can be without losing too much performance. The output power is chosen as the critical parameter for the sensitivity analyses presented in this thesis. Values 3%, 5%, and 10% down from the highest achieved output power are set as limits.

3.7 PCB substrate

This thesis uses two different substrates when realizing different designs. Firstly, FR4 is used, which is a commonly used substrate for PCB design. FR4 is beneficial for a prototype as it is cheap to produce and widely available.

The other substrate considered in this thesis is RO4003 [17]. This substrate is better suited for RF designs, as the lower dielectric constant of the substrate gives lower loss compared to FR4. Substrate parameters for both substrates are shown in Table 3.1.

Table 3.1: Substrate parameters for FR4 and RO4003.

Parameter	**Value**	
Substrate	FR4	RO4003
ε_r	4.4	3.55
μ_r	1	
H	1.52 mm	
T	35e-3 mm	
Cond	5.96e7 mm	
TanD	0.02	0.0022

3.8 DC feed

For this thesis, the DC feed network is designed as shown in Figure 3.6. As stated in section 2.4, the DC feed is needed to isolate AC power from the DC bias nodes. The designed DC feed differs slightly from the one in Figure 2.5, omitting the inductor. The laboratory at NTNU has a limited set of inductors available. All available inductors are limited in max power, making them unsuitable for the designs considered in this thesis. By omitting them, more of the RF signal will probably bleed through to the load. Noise and ripple could be problems in an actual application, but they should not change the ability to measure efficiency for this thesis.

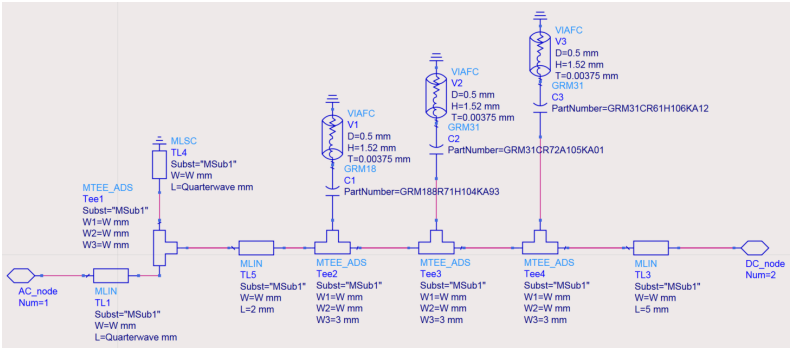


Figure 3.6: Schematic design of DC feed.

DC feed designs are frequency-dependent, as the signal's wavelength will determine the length of the quarter-wave transmission line. As the systems designed in this thesis are made on two different substrates, the wavelength will differ on each substrate. The length and width of the quarter-wave lines are calculated using the substrate parameters shown in Table 3.1, with a characteristic impedance of 50 Ω and a length of 90°. Table 3.2 shows the line dimensions. The values of the decoupling capacitors used are shown in Table 3.3.

Table 3.2: Quarter wave lines in each substrate used

	Length [mm]	Width [mm]
FR4	14.174	2.899
RO4003	15.432	3.371

Table 3.3: Decoupling capacitors for DC feed.

Capacitor	Value
C_1	12 nF
C_2	1 µF
C_3	10 µF

3.9 Measurements

In an application where the supply modulator drives an amplifier, the system's impedance will generally not be a single value. As the supply modulator drives an amplifier, its impedance will change depending on the input signal of the system.

Thus, the system is tested for three different loads Z_L: 50Ω, 100Ω and 150Ω. The range of impedances seems reasonable as an approximation for an amplifier and will give some insight into how the system adapts to driving a varying load.

For the simulations, the efficiency is obtained by using a harmonic balance module and measuring the power over the loads. The measurements are done by calculating the power from the voltage over the loads. For the measurements done at the lab, the input power is generated by a vector signal generator.

3.10 Self injection rectifier

The general architecture for the rectifying element in the supply modulator is shown in Figure 3.7.

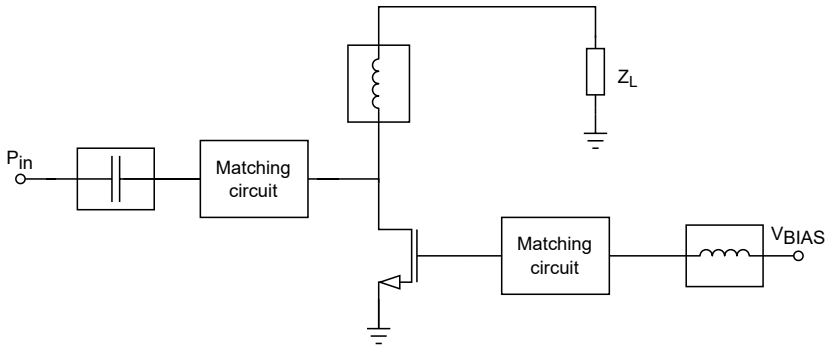


Figure 3.7: Circuit schematic of self biased rectifier.

This design relies on self-injection through leakage from drain to gate, which means the DC voltage is the only one applied to the gate. As opposed to the designs presented in [5], the gate is connected to a matching circuit, which aims to control the leakage and use it to increase the performance of the rectifier.

3.10.1 Circuit design

The first iteration of the design uses source- and load-pull components to emulate drain and gate matching circuits. This is shown in Figure 3.8.

The system is optimized to achieve peak efficiency for f_0, defined by Equation 3.2. By allowing the optimizer in ADS to tune the parameters of the source- and load-pull modules, it is possible to find the peak efficiency of the matching circuit.

The self-injected design analysis is done with the first revision of the source- and load-pull modules. The first revision cannot calculate phase delay, which is excluded in this design.

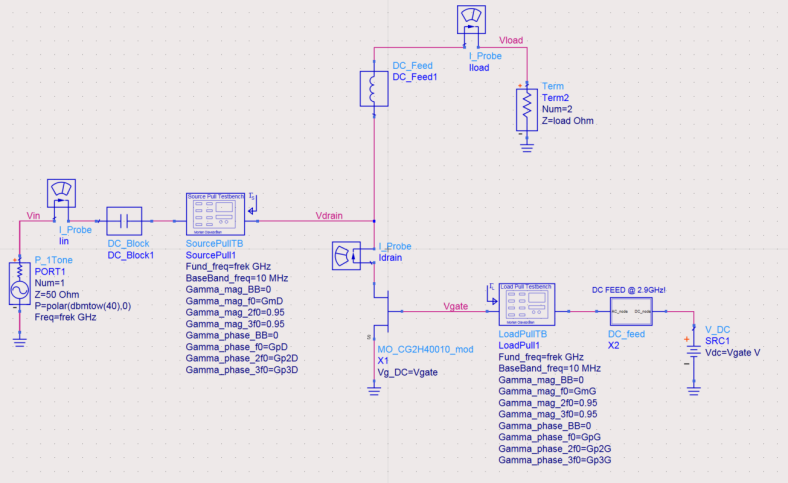


Figure 3.8: Schematic with non-ideal matching circuits.

Different bias voltages are tested to see which value results in the highest output power. The parameters for the matching circuits are optimized for each configuration. For the realization, a gate voltage of -3V is chosen. The voltage equals the threshold voltage of the transistor [18].

A sensitivity analysis is done as described in section 3.6. The variables from the load- and source pull modules are all swept for each load. Finally, the analysis determines a parameter that seems to be a good compromise between the three loads. Appendix A displays the sensitivity analysis.

3.10.2 Rectifying element matching circuits

A transmission line circuit is optimized to resemble the parameters from the sensitivity analysis as closely as possible. The source/load-pull and the transmission line circuits are terminated separately, and an optimizer is set up to equal the S-parameters of both circuits. Finally, the transmission line circuits are connected to the transistor design, and the system is optimized towards max power output.

Simulations for the self-injected rectifier are done on the FR4 substrate and the RO4003 substrate.

Gate match network

The topology of the gate network is shown in Figure 3.9. The left side is directly connected to the gate of the transistor. To the right, the gate match is connected to the DC feed, as shown in section 2.4.

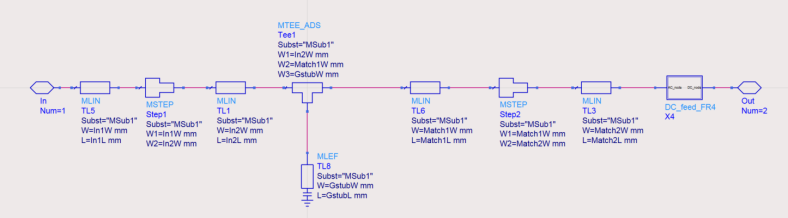


Figure 3.9: Gate matching circuit.

Drain match network

Figure 3.10 depicts the design of the drain network. As more harmonics are expected on this side of the system, a different DC-feed design is considered. The lines of this DC feed are allowed to be optimized as opposed to the gate network DC feed. By allowing for the DC feed to be optimized, the system is better at removing harmonics as well as f_0.

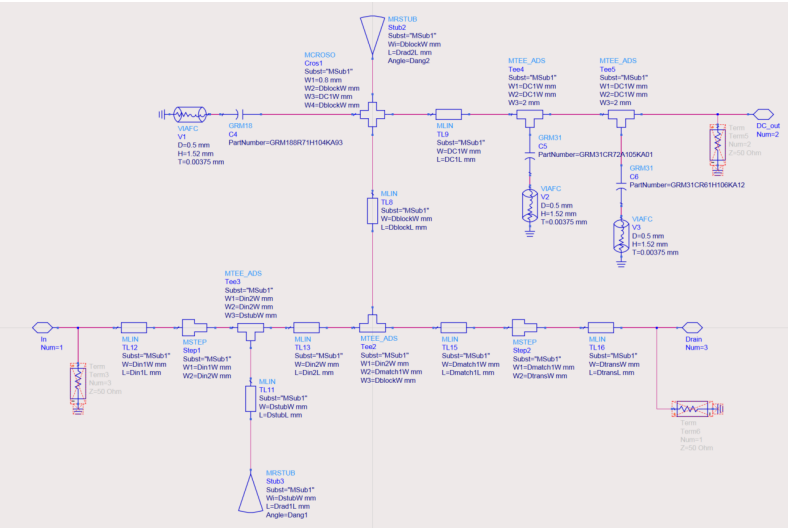


Figure 3.10: Drain matching circuit.

3.10.3 Layout

The layout for the circuit is shown in Figure 3.11. The PCB is only made using the FR4 substrate. The finalized PCB with components soldered to it is shown in Figure 3.12. While designing the layout for the self-biased rectifier, the length of the stub on the gate matching circuit is increased. The elongation of the gate stub is done to see how different stub lengths will alter the circuit's performance. A ruler is added to the stub to shorten the line precisely.

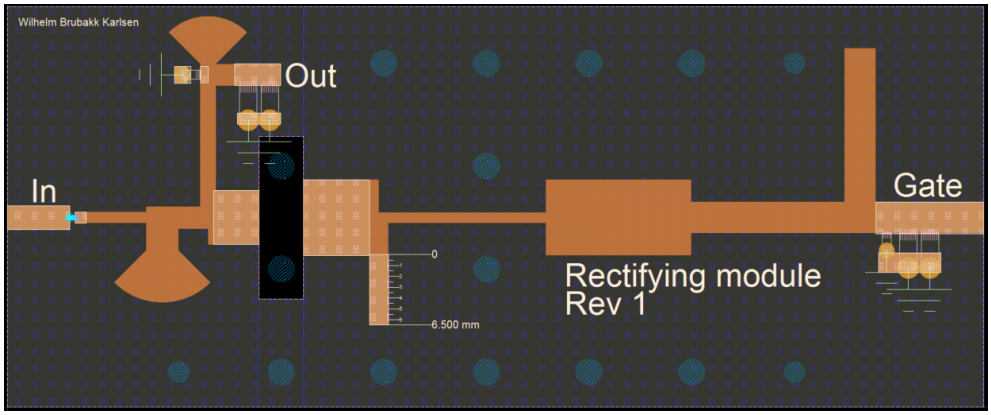


Figure 3.11: Layout for the self biased rectifier.

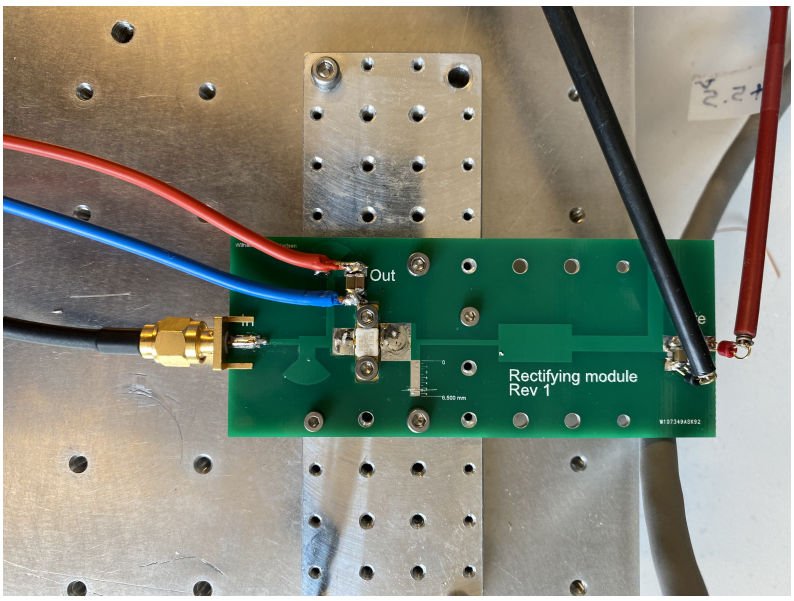


Figure 3.12: Soldered PCB of the self biased rectifier.

3.10.4 Measurements

The measurement setup for efficiency of the self-injected design is identical to the setup used in [5]. Thus, the description of the setup made in the laboratory is reused with some modifications.

A block diagram describing the test bench for measurement of efficiency is shown in Figure 3.13.

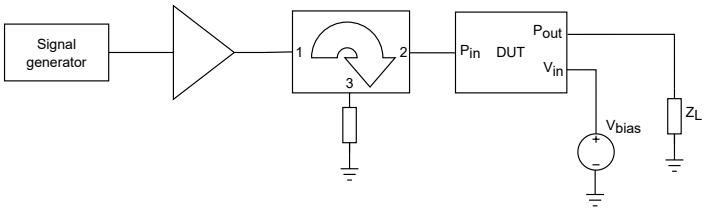


Figure 3.13: Block diagram for power measurement of self biased rectifier.

A vector signal generator is used to drive an amplifier. The amplifier increases the total output of the vector signal generator to ensure the rectifier is fed the correct amount of power during measurements.

The output of the amplifier is connected to an isolator. By configuring it this way, reflections that may occur when experimenting with different matching circuits will be dissipated in the load connected to the isolator instead of being reflected directly to the output of the amplifier.

To be able to measure the input power on the DUT, an RF port is connected to the isolator. The "FWD" is connected to a power meter to read the incident power. The rectifier is connected to the "OUT" port. Lastly, the rectifier sends DC power to a load with a known resistance. A voltmeter is used to measure the voltage over the load. Equation 3.1 is used to determine the system's total output power. The setup from the laboratory is shown in Figure 3.14.

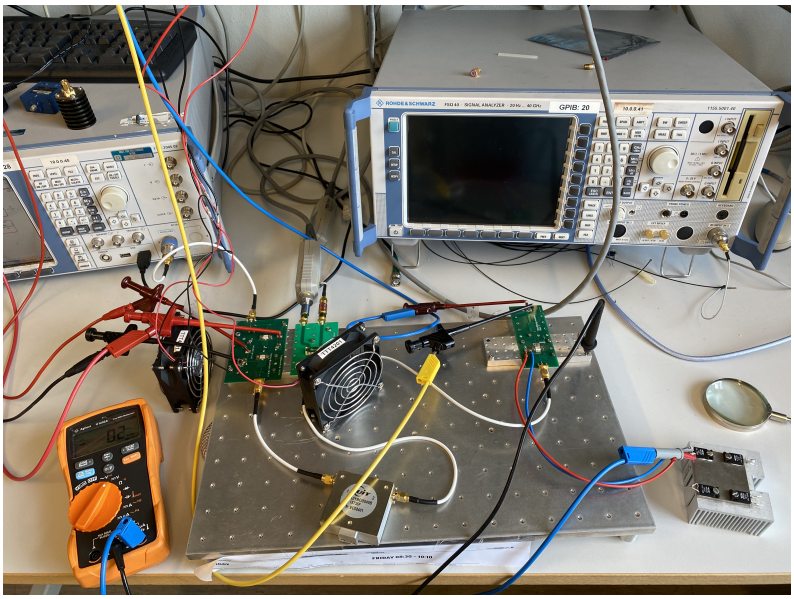


Figure 3.14: Output power measurement setup for self biased rectifier.

A Rohde & Schwarz SMU200A generates the input signal. The signal is amplified

with an in-house designed driver buffer, designed around a Wolfspeed CG2H40025F 25W GaN HEMT. Next to the amplifier, a cooling fan is placed to ensure the amplifier does not overheat. The gate voltage is applied using a CPX200DP lab power supply. The isolator used is a UIYBCI5049B15T3SF. It has an operational range from 1.5GHz to 3GHz. Port three is terminated using a 50Ω resistor.

The RF port is a Mini Circuit SCBD-01. When setting up the system, the port is measured to have an FWD loss of -18dB. The loss from the input to the output is measured to be -0.5dB. The loss measured from In to REW is -40dB, which is assumed to be negligible.

For the FWD line, an Anritsu power sensor is used. The sensor has a maximum power rating of 20dBm. Requiring 40dBm at the input of the rectifier means the loss in the directional coupler is not enough to keep the power level low enough for the power meter. Thus, an attenuator is needed between the port and power sensor. The attenuator will further decrease the signal at FWD with -6dB.

The rectifier is connected to the lab setup using a cable with a measured loss of 1.2dB. The losses between the power sensor and rectifier input are summed up to determine the power level applied to the rectifier. E.g., if 40dBm is expected at the rectifier, the power sensor has to display:

$$\begin{aligned} P_{FWD} &= 40dBm - P_{att} - P_{Port} + P_{loss} + P_{cable} \\ P_{FWD} &= 40dBM - 6dB - 18dB + 0.5dB + 1.2dB = 17.7dBm \end{aligned} \tag{3.5}$$

By varying the input signal from the vector signal generator, the FWD power meter continuously shows 17.7dBm, ensuring that the rectifier is fed 40dBm.

3.11 Active injection rectifier

A second iteration of the rectifier design is created to compare the performance of the two circuits.

The self-injected rectifier design is modified to be able to actively inject AC power into the gate of the transistor. The goal is to improve its ability to rectify the incident wave from the input. For positive signal, the transistor should not conduct any current, and opposite for negative signal, as described in section 2.7. The transistor should operate more ideally than the self-injected rectifier by applying a sine wave and the nominal DC bias voltage to the gate.

3.11.1 Circuit design

The schematic design for the self-biased rectifier, shown in subsection 3.10.1, is modified to be able to bias the gate of the rectifier with a sine wave. The new design is shown in Figure 3.15.

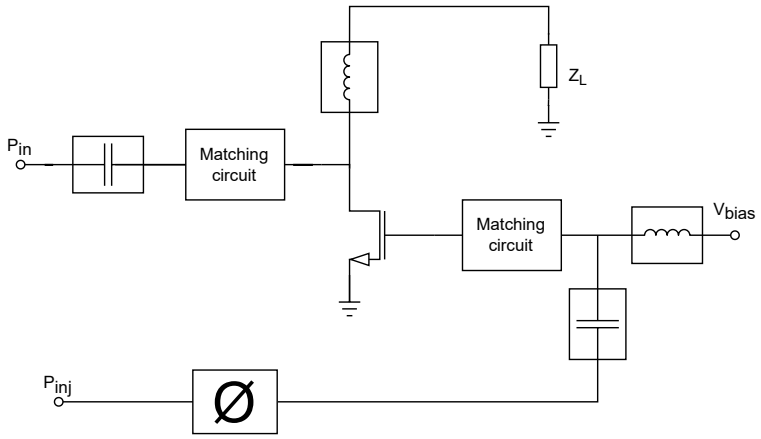


Figure 3.15: Circuit schematic of rectifier with injection.

The sine wave applied to the gate must be precisely out of phase with the incident wave on the drain. Correcting the phase on the injected signal is done with a phase shifter. The phase delay value is optimized with the circuit parameters to ensure the two signals are out of phase. The power added to the gate has to be calculated when determining the efficiency of the actively injected design, which is done by using Equation 3.3.

The design process from subsection 3.10.1 is followed for this design as well, which starts by implementing the matching circuits with source- and load-pull modules, shown in Figure 3.16. The design iteration of the load- and source-pull modules happens between the two designs. The new design allows for the inclusion of phase delay in the blocks.

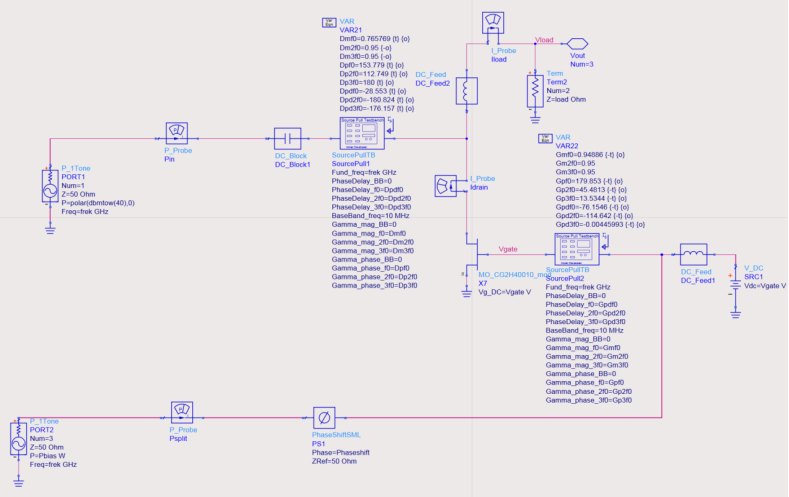


Figure 3.16: Rectifier with injection using load- and source pull modules.

A sensitivity analysis is also done with the active biased circuit. As opposed to the sensitivity analysis done for the self-biased design, the overall sensitivity of the injected design is done by analyzing the average power over all three loads. Finding one parameter that fits all loads well makes it easier to determine the parameters needed to optimize the transmission lines for the final design with transmission lines.

As the source pull modules are updated between the design of the self-biased and actively biased rectifier, the sensitivity analysis of the actively biased rectifier also contains the phase delay through the source pull module. The sensitivity analysis for the rectifier with injection is shown in Appendix B.

3.11.2 Rectifying element matching circuits

The matching circuits for the active biased rectifier are designed using a similar approach to the one described in subsection 3.10.2. The architecture for the active bias rectifier is only simulated on the RO4003 substrate.

Gate match network

The gate matching network for the rectifier with injection is shown in Figure 3.17. The most significant change from the self-injected gate match is the addition of a port for active injection. The DC feed has the same architecture, but with the line lengths for RO4003 shown in Table 4.2.

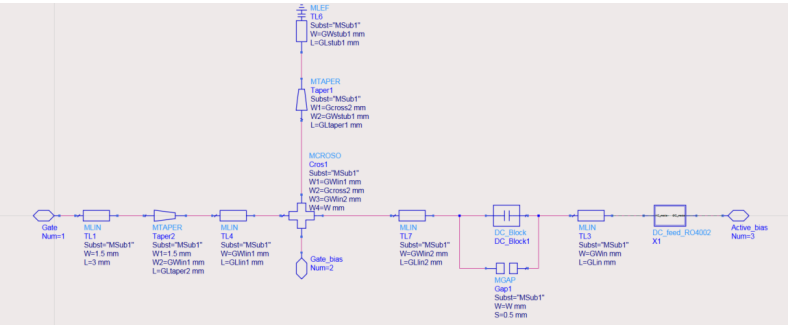


Figure 3.17: Gate match network for the rectifier with active injection.

Drain match network

Figure 3.18 displays the drain match network. The design is comparable with the design for the self-injected circuit, with the most notable design change being the addition of a capacitor on the output line. Transmission lines are also tweaked slightly to ensure the system behavior is close when comparing simulations and measurements.

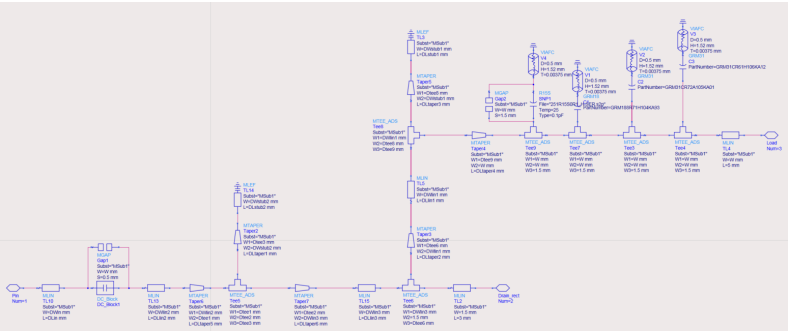


Figure 3.18: Layout for the rectifying element with injection.

3.11.3 Layout

The layout for the rectifier is shown in Figure 3.19. The system is realized on the RO4003 substrate. Figure 3.20 displays the finalized PCB for the system with active injection.

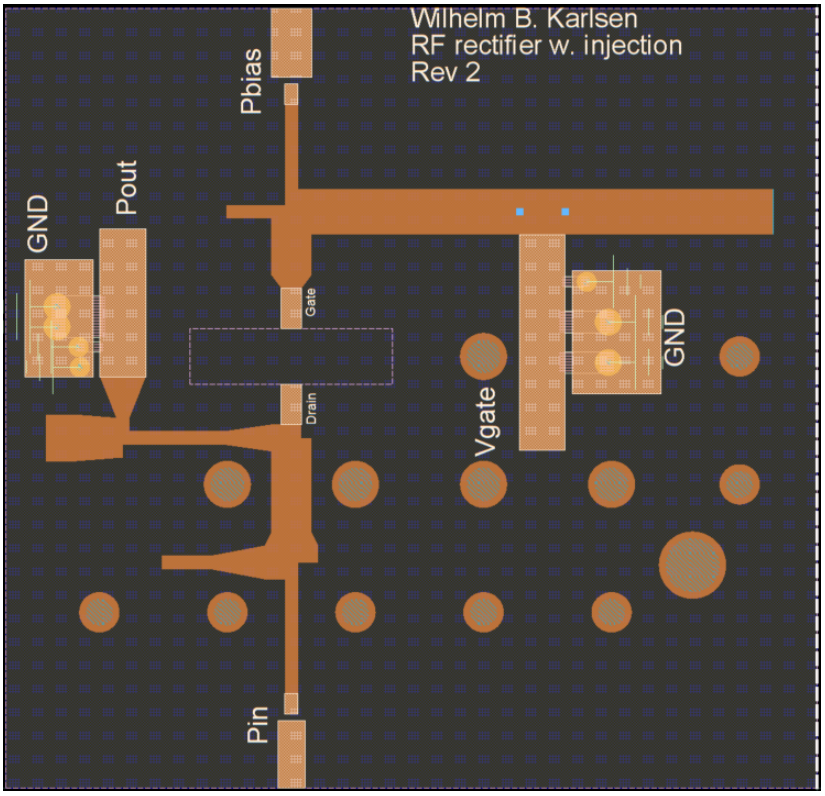


Figure 3.19: Layout for the rectifying element with injection.

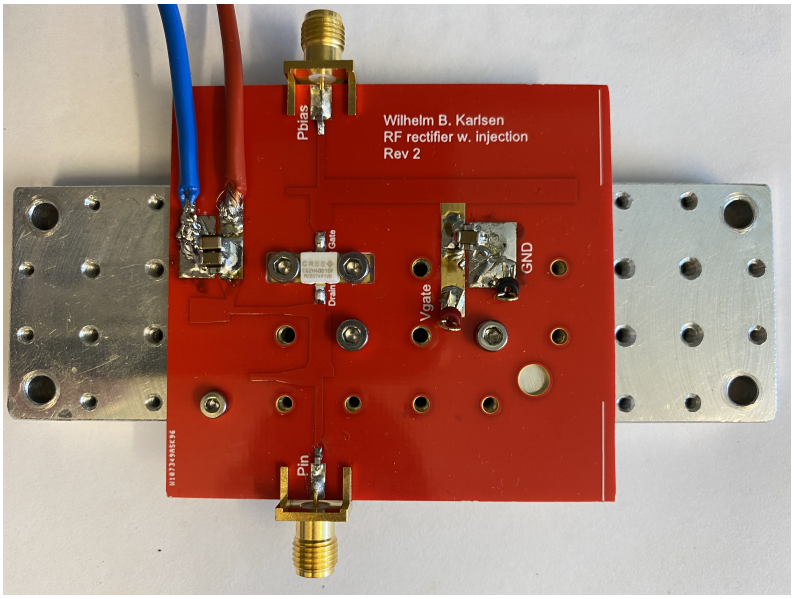


Figure 3.20: PCB for the rectifying element with injection.

3.11.4 Measurements

Schematics for the test bench used to measure the design with active injection is shown in Figure 3.21

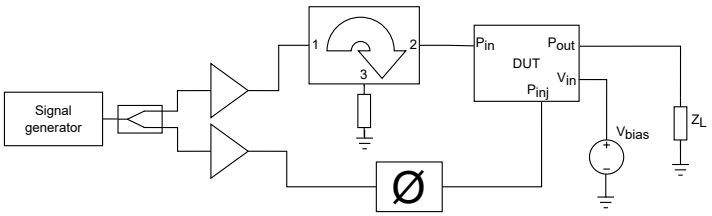


Figure 3.21: Active injection test bench schematic.

The testbench can be designed with a single signal generator by splitting the signal. The split signal is amplified to the desired gain in each branch, with one signal being phase-shifted from the other one. Efficiency is calculated over the load by measuring the voltage using a multimeter.

Realizing the test bench follows the procedure from subsection 3.10.4, using the same signal generator and amplifying circuit. The second amplifier is an older revision of the same circuit, meaning the amplifiers have similar specifications.

A Pasternack PE2014 10W Wilkinson power divider is used to split the signal to each amplifier. The injected power on the gate is supposed to be lower than the input power applied to the drain. Attenuators decrease the signal on both the input and output of the amplifier supplying the injected power. A -6dB attenuator on the input and a -3dB attenuator on the output of the amplifying stage ensures the correct power is applied to the gate.

In this configuration, the RF isolator and power meters are omitted from the testbench. The correct power levels are dialed in before the DUT is connected to the testbench, meaning there is no longer a need for continuous power measurements. A Rohde & Schwarz FSQ 40 signal analyzer measures the power level before the DUT is connected. The testbench for efficiency measurements is shown in Figure 3.22

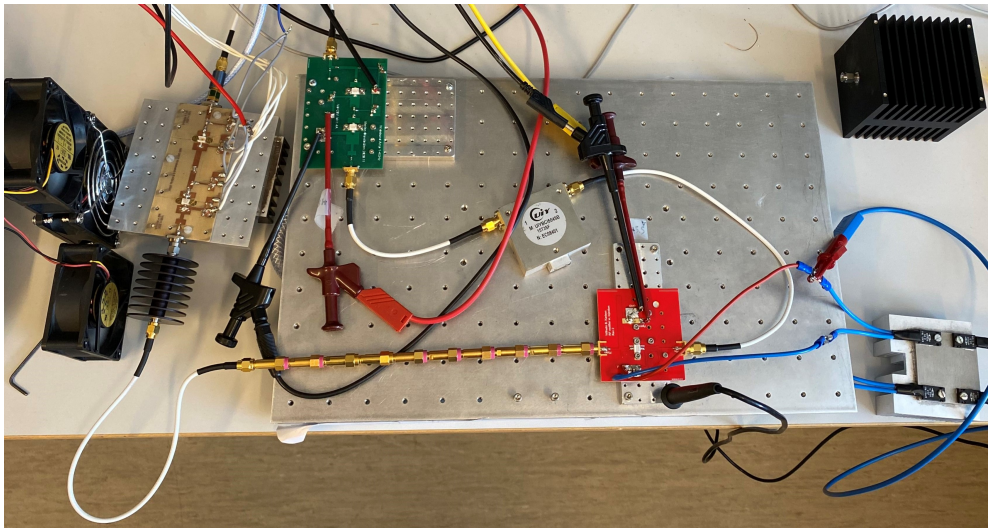


Figure 3.22: Realized testbench for rectifier with active injection.

Phase changes on the injected line come from adding a varying amount of male- to female connectors between the DUT and cable. Figure 3.23 show the connectors and how they are coupled. A single connector has a phase change of 112.5° for f_0. Connecting them in series enables testing of different phases.

Figure 3.23: Male- to female connectors for phase change.

Table 3.4 show the total phase change for zero to ten connectors coupled in series, with the corresponding relative phase change.

Table 3.4: Phase change with different amounts of connectors.

No. of connectors	Absolute phase	Relative phase
0	0	0
1	112.5	112.5
2	225	225
3	337.5	337.5
4	450	90
5	562.5	202.5
6	675	315
8	900	180
9	1012.5	292.5
10	1125	45

3.12 Supply modulator

A class B amplifier design drives the rectifying element, as suggested in [4]. The amplifier is designed around the same transistor as the rectifier. The threshold voltage of the CG2H40010F is -3V. Thus, a gate bias of -3V is set for the amplifier design.

The amplifier is combined with a rectifying module to create a full RF supply modulator design. Load- and source pull modules are added to the gate of each transistor. Both transistors share a load module on their drain. The complete schematic for the system is shown in Figure 3.24.

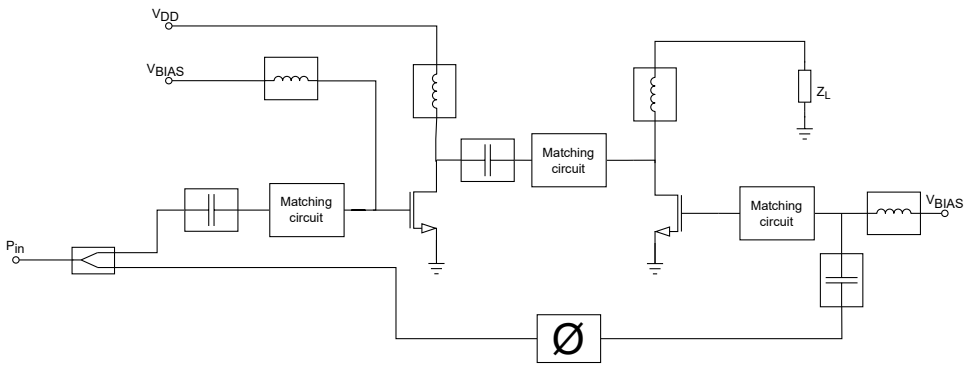


Figure 3.24: Circuit schematic for supply modulator.

The input power is split 50/50 between the gate of the amplifier and the active injection. A phase change is applied to the injected signal to ensure it is out of phase with the signal rectified.

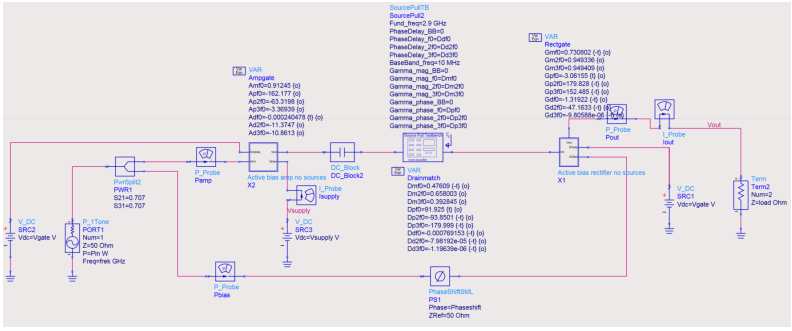


Figure 3.25: Circuit schematic for ideal supply modulator.

Due to time constraints, the implementation of supply modulators is ideal, with source- and load-pull modules. This design is shown in Figure 3.25.

3.12.1 Bandwidth

The bandwidth analysis of the system is performed by modifying the efficiency measurements to be swept over a frequency range. The bandwidth performance can then be analyzed by having the efficiency swept in a 100MHz band around f_0 for each load.

3.12.2 Single load analysis

The buck converter presented in [6] is tested using a 30Ωload to emulate the performance of the system. To make a fairer comparison to the performance of the buck converter, the RF supply modulator is reoptimized for a 30Ωload. Finally, a bandwidth analysis is done to compare the bandwidth performance of the RF supply modulator to the buck converter.

Chapter 4

Results

While efficiency is shown for all loads in the tables presented in this chapter, the figures depicting the internal voltages in the rectifying element only display the graph for the 100Ω load. The other loads are omitted from the graphs to make them easier to read and compare. The main reason for including the figures is to compare the trends displayed in them instead of the exact values for each load.

4.1 Self injection rectifier

For simulations and measurements of efficiency done on the self-injection design, Equation 3.2 is used to determine the efficiency.

4.1.1 Ideal matching circuits

Output efficiency for different loads and gate bias voltages are shown in Table 4.1. The system has $P_{in} = 10W$ for this analysis. The 100Ω efficiency measurement for a gate bias of -2.9V ran into a simulation error, resulting in no efficiency calculation.

Table 4.1: Efficiency for ideal match at different bias values.

	Z_L [Ω]		
V_g [V]	**50**	**100**	**150**
-2.9	86%	-	84%
-3	89%	87%	88%
-3.5	86%	79%	84%
-4	85%	85%	84%
-7	72%	81%	75%

Appendix A displays the sensitivity analysis for the self injected design. In some cases, a phase change of 2° from the ideal value results in a 10% drop in efficiency. At 2.9GHz in FR4, 2° equals a transmission line length of 0.3mm.

4.1.2 FR4 simulations

Table 4.2 displays the simulated efficiency for the system with transmission lines on the FR4 substrate. The average power for the three loads is 75%.

Table 4.2: Simulated efficiency for the self biased rectifier on FR4 substrate

$\mathbf{Z_L}$ [Ω]	**50**	**100**	**150**
η [%]	75	78	71

The internal IV-curve of the transistor is displayed in Figure 4.1. Figure 4.2 shows the internal gate-source voltage compared to the drain-source voltage over time. The bias voltage V_{GS} = -3V in both cases.

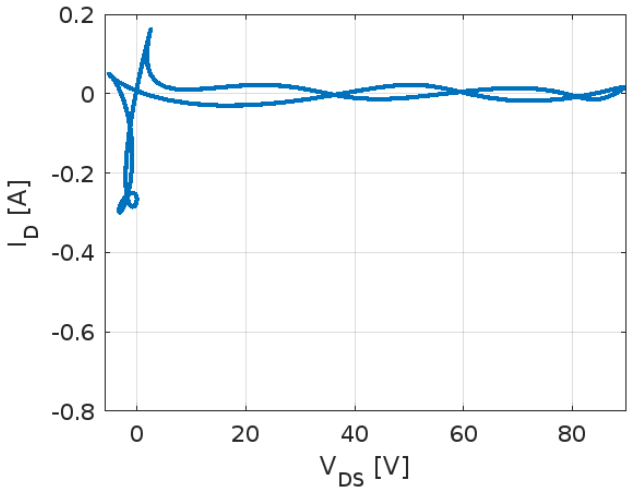


Figure 4.1: Time domain IV curve for self biased rectifier.

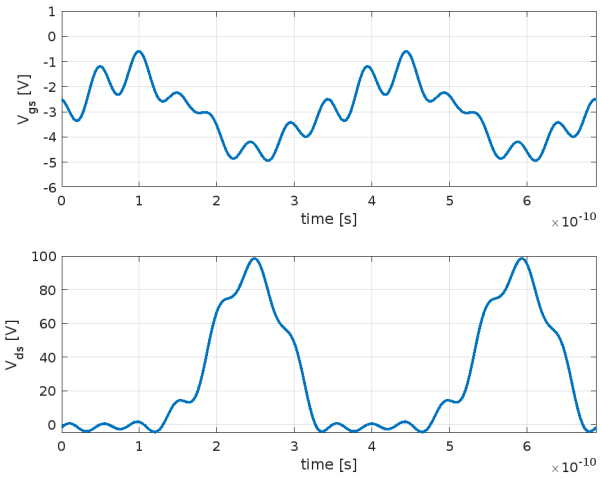


Figure 4.2: Internal V_{gs} and V_{ds} over time.

4.1.3 RO4003 simulations

The output efficiency for the system designed on the RO4003 substrate is shown in Table 4.3. The efficiency is calculated for $P_{in} = 10$W, yielding an average power of 83%.

Table 4.3: Simulated output power for self biased rectifier on RO4003 substrate.

Z_L [Ω]	50	100	150
η [%]	81	87	81

4.1.4 Measurements

Power output for the realized system on FR4 for different gate stub lengths is shown in Table 4.4.

Table 4.4: Measured output efficiency for self biased rectifier with 10W input.

	Z_L [Ω]		
Stub length [mm]	**50**	**100**	**150**
6.5	1%	0.4%	0.3%
5.5	4.6%	2.7%	1.9%
4.5	3.7%	3.6%	2.9%
3.5	2.9%	3.3%	2.2%

4.2 Active injection rectifier

The efficiency of the active injection rectifier design is determined using Equation 3.2.

4.2.1 Ideal matching circuits

For these measurements, input power $P_{in} = 10W$. The highest efficiency is gained with an injection power of $P_{inj} = 321mW$ and a phase change of Φ_{inj} = -134°. The efficiency for the system is shown in Table 4.5. Average power for the rectifier with active injection is calculated to be 85% ideally.

Table 4.5: Efficiency for ideal matching active bias rectifier.

Z_L [Ω]	50	100	150
η [%]	81	90	84

Figure 4.3 and Figure 4.4 display the internal IV-curves and the internal gate-source and drain-source voltages respectively. The bias voltage for all curves are V_{GS} = -3V.

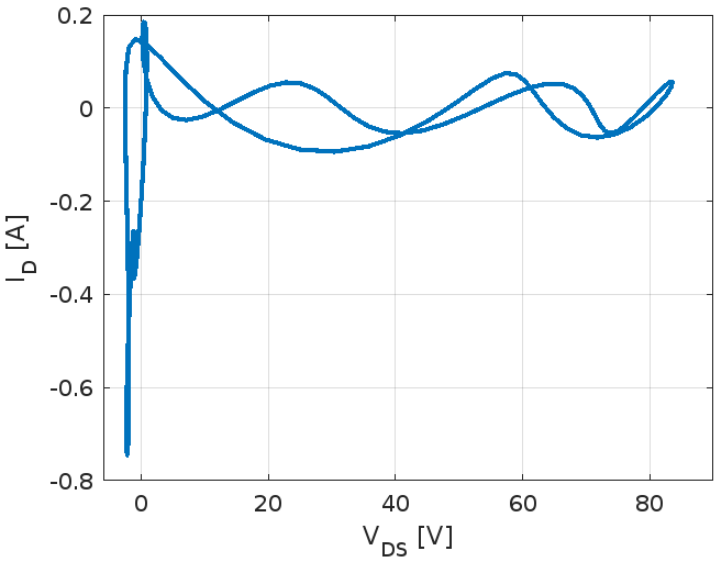


Figure 4.3: Time domain IV curve for self biased rectifier.

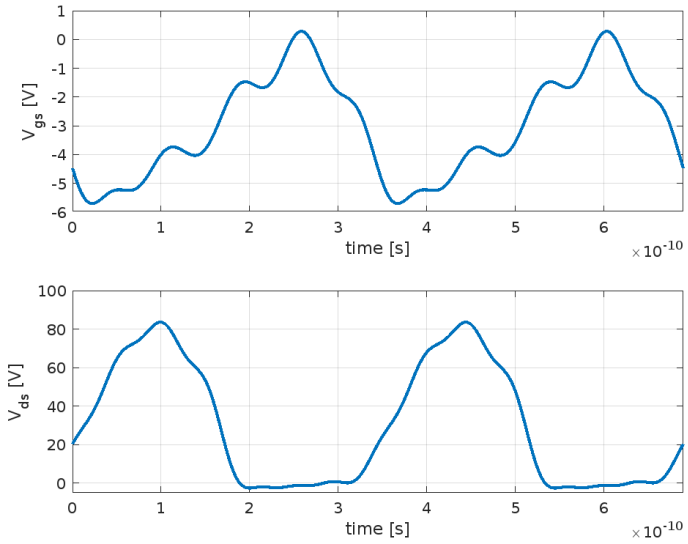


Figure 4.4: Internal V_{gs} and internal V_{ds} over time.

4.2.2 RO4003 matching circuits

$P_{in} = 10W$. Highest efficiency is gained with an injection power of $P_{inj} = 470mW$ and a phase change of $\Phi_{inj} = -173°$. Efficiency for each load is shown in Table 4.6. The average efficiency for the system is 71%.

Table 4.6: Simulated efficiency for non-ideal matching circuits.

Z_L	50	100	150
η [%]	73	73	66

The circuit performance is also measured with the injected power 20° out of phase from the ideal phase shift, as shown in Table 4.7.

Table 4.7: Efficiency for each load with injection 20° out of phase from the ideal value

Load [Ω]	+20°	-20°
50	61%	63%
100	59%	60%
150	53%	52%

The IV characteristics of the rectifier design with active injection and transmission line matching circuits are shown in Figure 4.5. Note the different scale of the y-axis compared to Figure 4.1 and Figure 4.3. Figure 4.6 displays the internal gate-source and drain-source voltages. The gate bias in both Figure 4.5 and Figure 4.6 is set to V_{GS} = -4.7V

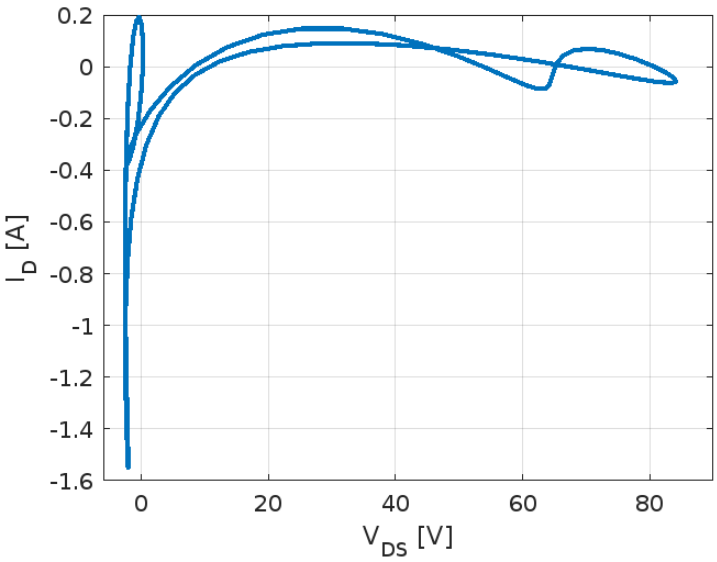


Figure 4.5: Time domain IV curve for self biased rectifier.

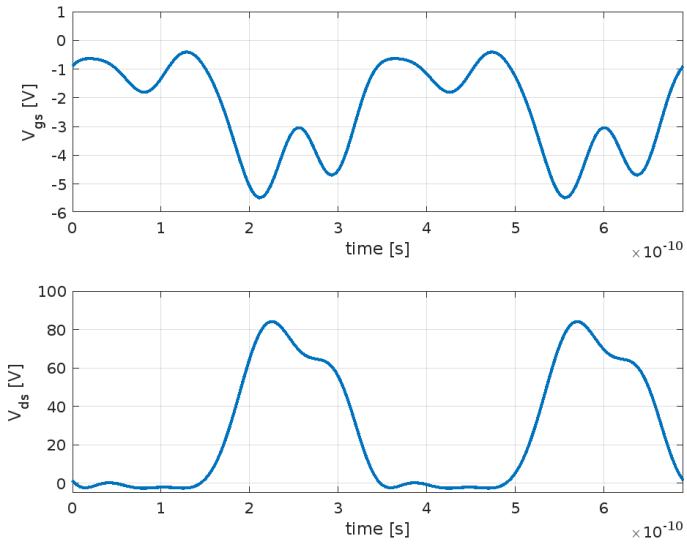


Figure 4.6: Internal V_{gs} and V_{ds} over time.

4.2.3 Measurements

Measurements of the rectifier with active injection follow the procedure described in subsection 3.11.4. Power delivery is tuned such that P_{in} = 10W and P_{inj} = 470mW. The applied gate voltage V_{gs} = -4.0V. Figure 4.7 show efficiency measurements for different phase changes. The plot is rearranged to display values after the relative phase change applied instead of the number of connectors used. Efficiency is calculated using Equation 3.3.

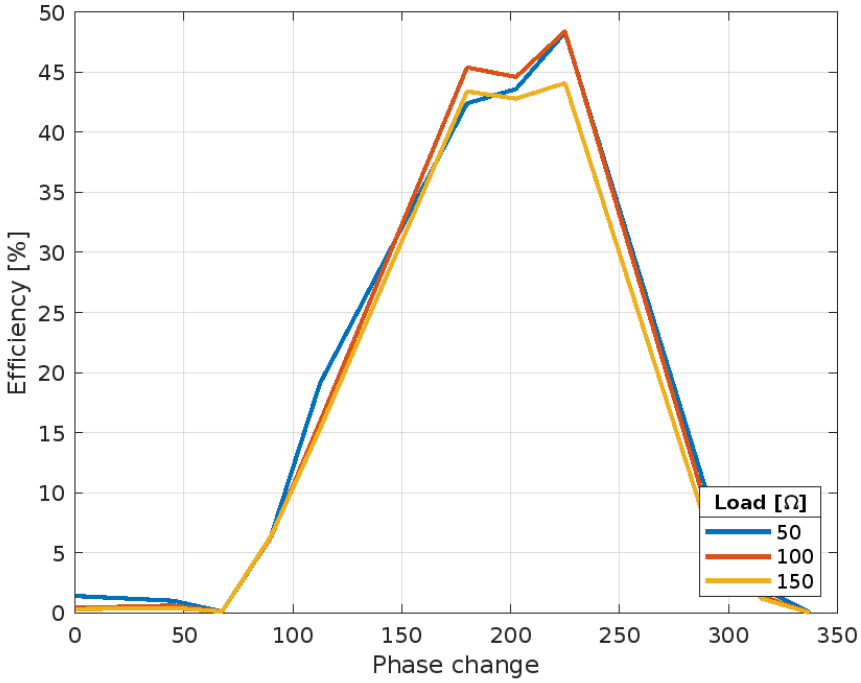


Figure 4.7: Measured efficiency for different phase changes.

The peak efficiencies of 48.3%, 48.4%, and 44.1% for each load, respectively, are obtained using two connectors in series resulting in a relative phase change of 225°.

The measurements using two connectors are repeated to find what V_{GS} gives the highest efficiency. The voltage is swept in a range from -3V to -6V. Table 4.8 displays the best efficiency achieved with the corresponding gate voltage.

Table 4.8: Highest efficiency achieved with the corresponding gate voltage for each load.

Load [Ω]	**V_{gs} [V]**	**η [%]**
50	-4.2	48.9
100	-4.3	50.6
150	-4.7	48.6

4.3 Supply modulator

Supply modulator efficiency is calculated using Equation 3.4.

4.3.1 Ideal gain and efficiency

The system is fed an input signal P_{in} = 600mW. The phase change on the active injection is Φ = -82°. Table 4.9 displays the output power and efficiency measured over each load.

Table 4.9: Output power and efficiency for the ideal supply modulator at f_0.

Load [Ω]	P_{out} [W]	η [%]
50	9.9	77
100	11.9	80
150	12.6	76

4.3.2 Ideal bandwidth

Figure 4.8 shows the efficiency and output power for each load from 2.85GHz to 2.95GHz, respectively. Using the definition of bandwidth presented in section 3.2 results in a bandwidth for each load as shown in Table 4.10.

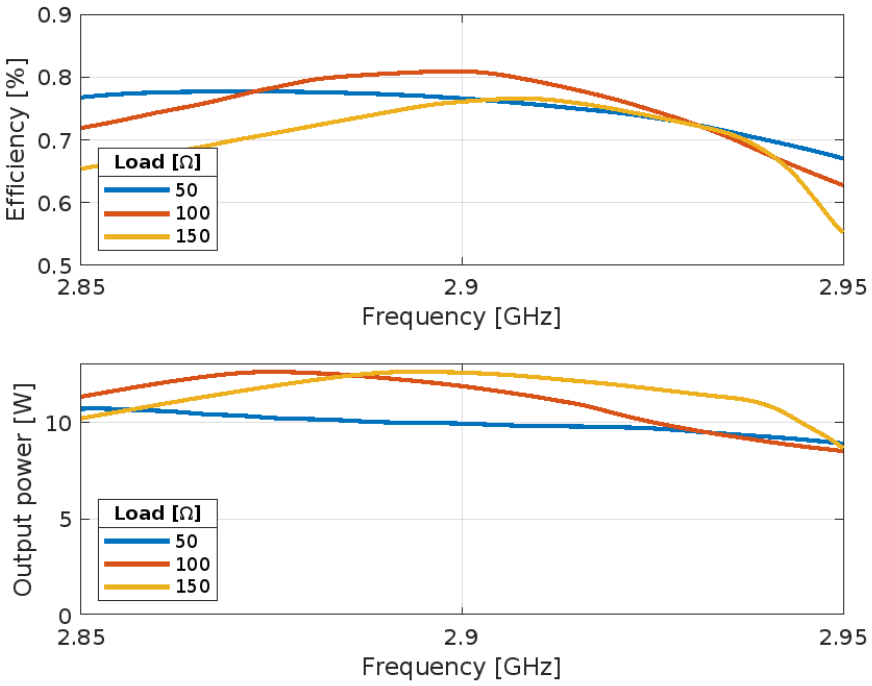


Figure 4.8: Efficiency and output power for the ideal supply modulator.

Table 4.10: Ideal bandwidth for each load.

Load [Ω]	Lower limit	Upper limit	Total bandwidth
50	2.85GHz	2.95GHz	100MHz
100	2.85GHz	2.93GHz	80MHz
150	2.85GHz	2.94GHz	90MHz

4.3.3 Single load analysis

Figure 4.9 displays the efficiency and output power from the analysis of the system optimized for a 30Ω load.

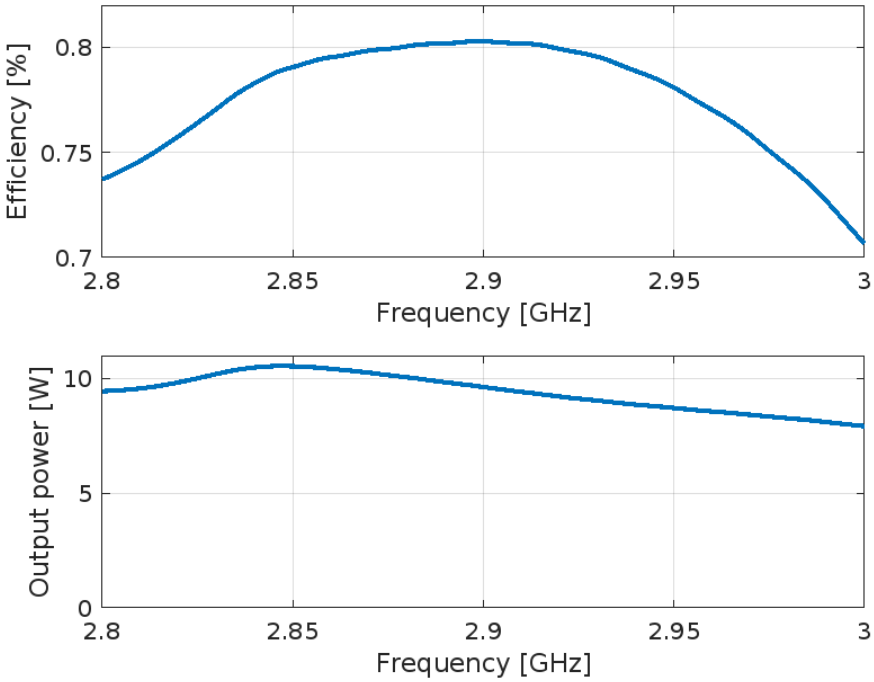


Figure 4.9: Efficiency and output power when supplying a 30Ω load.

The calculated mean efficiency over a 200MHz band is determined to be 78%, assuming the modulated signal is uniformly distributed. For the entire band, the output power is greater than or equal to 8W.

Chapter 5

Discussion

Overall, the simulations show the designs proposed in this thesis are able to rectify the signal and maintain an efficiency greater than 70% in most cases. In addition, the bandwidth seems to be comparable to that of a narrowband amplifier, which is an improvement over buck converter designs.

Designing the system posed some difficulties due to the choice of frequency. While higher frequency gave a more realistic view of the performance of an RF supply modulator, it also made the sensitivity of the system harder to control. A lower frequency equals a longer wavelength, which would have lowered the sensitivity to deviations in production.

In general, as the design is a proof of concept, it would have been easier to focus on a single load instead of trying to design for three different load values. While it may be more realistic to have a varying load, it complicates the design process and increases simulation times significantly.

The decoupling capacitors on the system's output would remove the modulation from the output signal, making the modulator unusable. As the system is only designed for testing, they are added for system stability. A new output circuit must be designed should the system be used for supply modulation.

5.1 Self injection rectifier

The simulations done with the self-injected rectifier show that the design can achieve relatively high efficiency. The gate bias impacts how efficiently the system can rectify the input signal, with the threshold voltage generating the highest efficiency for all loads.

From simulations, the choice of the substrate has a significant impact on the system's efficiency. The increased efficiency is probably gained from the far lower dielectric loss in the RO4003 substrate compared to FR4, which can be seen in Table 3.1.

When looking at the internal voltages and currents in the transistor shown in Figure 4.2, the rectifying functionality is clearly seen. Despite only applying a DC voltage at the gate, V_{gs} swings around the threshold voltage. The gate network is also tuned to get out of phase from the drain voltage. This behavior increases the effect of the transistor as a rectifier. In comparison, the output power previously achieved was measured at 22.5% [5]. The design created in that paper omitted a gate match for simplicity, as the transistor at that point did not have reverse bias compatibility. The gate match has a massive impact on system performance from the simulation data presented.

5.1.1 Measurements

Measurements of the realized system show a considerable deviation from the simulated performance. While the simulated efficiency is high, the sensitivity analysis also predicted that the system was susceptible to variations. Tiny deviations in substrate parameters or low precision in production could ensure a poor match for the system.

As shown in Table 4.4, the line does alter the performance of the system, but the measured efficiency still lacks compared to the simulated results. The measured efficiency averages 3% for the three loads, a 72% drop from the simulated efficiency.

Cutting the gate stub during measurements confirmed the system performance is affected by the line length, which may be part of the explanation as to why the system performed so poorly. During optimizations, the stub is determined to be a specific length. As the stub is shortened by hand during measurements, it is impossible to cut with the accuracy needed to find the exact length optimized.

When realizing the design, the lines connecting the transistor to the PCB are discovered to be wider than the pins of the transistor itself. The broader lines may have generated parasitic capacitance from gate and drain to source, altering the match. The lines are cut closest to the transistor to remove the parasitic capacitance. The alteration of the lines proved to have little effect on the efficiency, suggesting the previous two issues were a lot more significant.

During measurements, the gate voltage is always set to -3V. While this is the nominal threshold voltage for the transistor, individual differences in transistors may cause this to vary. From Table 4.1, it is seen that the threshold voltage will alter the circuit performance. While it may not have given a tremendous increase in

performance, some efficiency could be lost due to the sub-optimal gate voltage being applied to the transistor.

5.2 Active injection rectifier

In the simulation using ideal components, the efficiency is similar to the self-injected design. The system is assumed to be more efficient than the self-injected design, but the injected power holds back overall efficiency. The systems' performance is explained by comparing the internal IV curves of the two designs shown in Figure 4.1 and Figure 4.3. The curves for the design with active injection seem to go deeper in reverse bias, ensuring the transistor acts more like an ideal rectifier than the self-injected one.

Comparing Figure 4.2 and Figure 4.4, it is evident that both designs enhance the transistors ability to rectify the signal by ensuring V_{gs} is out of phase with V_{ds}. If only V_{gs} is considered, the self-injected design has a lower voltage swing on the gate, with more ripple. Despite having some extra power consumption due to the active injection, Figure 4.3 gains more efficiency from the greater output swing with less ripple on its gate.

The efficiency for each load could potentially be even better than the self-injected design, as a single matching network is used for all loads. Had they been designed individually, greater efficiency is expected for each load. The advantage of finding a single set of design parameters is that it makes it easier to produce the transmission lines for the system. In addition to the higher gain achieved, the sensitivity analysis suggests the system with active injection is more robust than the self-injected one.

When the injected design is implemented using transmission lines, the efficiency achieved is lower than expected. Being even lower than the self-injected design's efficiency on the lower performance FR4 substrate suggests the design itself is poor. While the systems are similar in design, some changes are made to the matching circuits when the system is remade to allow active injection. The redesign may have resulted in a matching circuit with poorer impedance matching, resulting in a lower output efficiency.

The IV curves disclose that the system deviates from the ideal design. While positive V_{gs} results in close to no I_d in Figure 4.1 and Figure 4.3, a non-negligible current is observed in Figure 4.5. The threshold voltage is lowered to reduce the current drawn for positive gate voltage, resulting in a slight increase in efficiency. The transistor seems to operate at its highest efficiency when the DC bias for the gate is at the threshold voltage. If a matching circuit could be made that generates a lower current draw for positive V_{ds}, V_{gs} could be increased back to the threshold voltage, achieving higher efficiency.

5.2.1 Measurements

Measurements show the system is capable of rectifying an RF signal if an injected power is applied. The system performance seems to vary little when driving different loads, suggesting the system could be capable of driving an amplifier with a varying load without too much deviation in efficiency.

0° relative phase change in measurements does not equal the phase-shifted value from simulations. It describes the change in phase from directly connecting the gate with a cable. It is difficult to know what phase change corresponds to the peak measurements.

The way phase measurements are done results in very little ability to tune in between the phase changes for a single connector. Thus, it is not guaranteed that the optimal phase value is reached during measurements. It is probable that the optimal phase change is not obtained, meaning more power could be achieved if a better way of tuning the circuit is found. Comparing the simulated values for the circuit shown in Table 4.6 and Table 4.7 shows that missing the optimal phase change with 20°in either direction results in approximately 13% of efficiency lost.

For the measurements, the system has a bias voltage of -4V applied to the gate of the transistor. The voltage is chosen as a compromise between the simulated optimal value and the theoretical ideal bias voltage being the threshold voltage. In retrospect, choosing a compromise may not have been the best choice of bias. However, different gate biases are tested for the most optimal phase shift to find the highest performance possible. Table 4.8 shows gate biases closer to the simulated ideal bias of -4.7V as opposed to the threshold voltage. The efficiency did not see a considerable jump when altering the bias voltage. However, a few percent are gained.

There is a small deviation in efficiency for the different loads. This is promising, hinting at the rectifier being able to supply a varying load with some consistency. For driving an amplifier which will vary depending on the incident signal, it is key that the efficiency is somewhat similar for different loads.

Due to the device heating up significantly during measurements, the system is not tested running continuously. More cooling is likely needed to run the system over a more extended period. Therefore, it is uncertain how the system behaves when running continuously.

5.3 Supply modulator

The supply modulator is designed with ideal modules, which gives an idea of the absolute max performance that can be achieved with the design and topology of

the system. If the system is realized, lower efficiency is expected from this design. Stability is not tested for the amplifier, which could be an issue if the system is produced. Stability circuits would also lower performance slightly.

Testing the bandwidth by sweeping the efficiency in a 100MHz range around f_0 shows the system's ability to operate at a wide frequency range. The design is optimized for peak efficiency alone, so it is reasonable to believe that a greater efficiency for the frequency band could be achieved by optimizing for the whole frequency range as shown in Figure 4.8. Buck converters with peak efficiency of 91% and driver efficiency of approximately 84% for a 20MHz signal have been reported [6]. In this case, 7% efficiency is lost by driving the signal with a 20MHz signal. The system is tested by driving a 30Ω load with a peak output of 7W. For the RF supply modulator driving a 50Ω load, the system has experienced approximately 10% loss in efficiency over a 100MHz band for the same output power. The peak output power is lower than the buck converter, but the bandwidth is significantly greater in comparison.

5.3.1 Single load analysis

When the system is optimized for a single 30Ω load, the performance improves compared to the system designed for three loads. Some gain may come from driving a load with lower impedance, but the ability to focus the matching on a single element is probably the leading cause for improvement.

Despite analyzing the system in a 200MHz band around f_0, the optimization is purely done for the center frequency at 2.9GHz. As the output power never falls below 8W in the range of operation, the supply modulator is quite capable of driving a 30Ω load in this region. The peak efficiency is comparable to the efficiency achieved for the 100Ω simulation performed previously. The bandwidth, however, is significantly increased in the 30Ω design.

The previously mentioned buck converter design achieved a measured peak efficiency of more than 91%, approximately 10% greater than reported for the RF supply modulator presented in this thesis [6]. In their paper, the buck converter can track a modulated signal of 20MHz, dropping 7% from peak efficiency. Suppose the modulated signal is assumed uniform in frequency. In that case, the RF supply modulator drops 3% in efficiency for a bandwidth of 200MHz, one order of magnitude greater than the buck converter reports. As the design presented in this thesis is not optimized for bandwidth, it is not unreasonable to assume the efficiency could be further improved over the entire band if this had been the main design focus.

Chapter 6

Conclusion

In this thesis, a proof-of-concept for an RF supply modulator is designed. Firstly, the rectifying element of the modulator is analyzed. Two architectures of the rectifying element are created, one with self-injection and one with active injection using a CG2H40010F GaN HEMT. Both circuits are analyzed with computer simulations and measurements done at a lab. Computer simulations are done in two stages, first with ideal matching circuits before transmission line matching circuits are made. The analysis is done for a center frequency of 2.9GHz, over three loads of 50Ω, 100Ω and 150Ω, respectively.

The rectifier with self-injection is biased at -3V, with an input power of 10W. This setup returns an average efficiency of 88% over the three loads when implemented ideally. Implementing transmission lines on an FR4 substrate yields an average efficiency of 75%. The loss when going from ideal matching networks to transmission lines is explained by losses in the substrate and a poorer match from the transmission lines than the ideal network. Simulations on the RO4003 substrate show an improvement in the efficiency of 8% compared to FR4. The system is produced on the FR4 substrate. When measured, the system only achieves a peak efficiency of 4.6%. It is believed that some inaccuracies during production cause the matching network to be slightly different from simulations. As the system design seems to be highly sensitive, the inaccuracies in the production phase are believed to work poorly.

The system is redesigned to allow for active power injection to reduce sensitivity. Ideally, the efficiency fell to 85%, although a higher peak efficiency of 90% is obtained. Simulations on RO4003 show an average efficiency of 71%. Measurements show that the realized system can output a peak efficiency of 50%. It is not sure whether or not this is the peak value, as the phase shift module in the testbench is limited.

Finally, a supply modulator is simulated using ideal matching networks. The aver-

age efficiency over the three loads is analyzed to be 78%. The output power varies for each load, but the system can output close to 10W. A sweep from 2.85GHz to 2.95GHz is done to find the wideband performance. Using the definition from section 3.2 yields a bandwidth of 100MHz, 80MHz and 90MHz for the different loads.

If the system is reoptimized to drive a single load, the system has a significant increase in bandwidth. For a 30Ω load, the system has an average efficiency of 78% over a 200MHz band centered at 2.9GHz.

From the initial test done in this thesis, the RF supply modulator shows promise for increased bandwidth compared to buck converters. As expected, the trade-off is lower efficiency.

Chapter 7

Future Work

Using an RF supply modulator architecture is supposed to increase the bandwidth performance compared to a buck converter. A further drop in efficiency is expected compared to the buck converter, but the bandwidth performance could be even better. Thus, it could be beneficial to optimize the system over a bandwidth instead of optimizing purely at f_0.

A significant efficiency indicates that the transistor model works as intended for the rectifier with active injection. However, as the transistors' reverse compatibility is added to the model, it is questionable how accurate it is. Using a transistor where the model is more accurately analyzed in reverse bias, it is not unthinkable that the measured performance will correspond better to the analyzed one. Regardless, it could be interesting to compare the results from this thesis with an RF supply modulator using a transistor made with reverse bias compatibility. In previously presented RF supply modulation designs, a Qorvo transistor is explicitly used for its capability of operation in reverse bias [4].

For an analysis where the RF supply modulator is used to drive an amplifier, the DC feed should be redesigned to allow transmission of the modulation signal. As stated in chapter 5, the current DC-feed would not be able to transmit a modulated DC signal. The capacitors used as decoupling will eradicate the modulation. However, removing the capacitors would create new noise challenges to the signal.

Little attention is given to the amplifying stage of the supply modulator, as this stage is only designed with ideal components. Transmission line matching circuits are needed to implement a supply modulator and create a PCB for the design. Transmission lines would be required for the amplifier and the matching circuit connecting the amplifier to the rectifying element. Considering stability would also be necessary for such a design.

Transmission line matching circuits must be designed for the amplifier and a net-

work connecting the amplifying and rectifying elements. Stability should also be considered for such a design.

A better system could probably be designed by creating the system in a Monolithic Microwave Integrated Circuit (MMIC). Creating the design integrated would reduce the issues caused by the susceptible system. As MMIC allows for more control of the transmission lines, the matching circuit would be produced more precisely.

Bibliography

[1] S. Kemp. 'Digital 2021 april global statshot report.' (), [Online]. Available: https://datareportal.com/reports/digital-2021-april-global-statshot (visited on 01/06/2022).

[2] C. Han, T. Harrold, S. Armour, I. Krikidis, S. Videv, P. M. Grant, H. Haas, J. S. Thompson, I. Ku, C.-X. Wang, T. A. Le, M. R. Nakhai, J. Zhang and L. Hanzo, 'Green radio: Radio techniques to enable energy-efficient wireless networks,' *IEEE Communications Magazine*, vol. 49, no. 6, pp. 46–54, 2011. DOI: 10.1109/MCOM.2011.5783984.

[3] K. Davaslioglu and E. Ayanoglu, 'Quantifying potential energy efficiency gain in green cellular wireless networks,' *IEEE Communications Surveys Tutorials*, vol. 16, no. 4, pp. 2065–2091, 2014. DOI: 10.1109/COMST.2014.2322951.

[4] A. Alt, 'Supply modulated gan hemt power amplifiers - from transistor to system,' Ph.D. dissertation, Dec. 2020, pp. 75–108, 160–186.

[5] W. B. Karlsen, 'Rf supply modulation rectifier architecture, for use in envelope tracking.,' 2021.

[6] Y. Zhang, M. Rodríguez and D. Maksimović, '100 mhz, 20 v, 90% efficient synchronous buck converter with integrated gate driver,' in *2014 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2014, pp. 3664–3671. DOI: 10.1109/ECCE.2014.6953899.

[7] E. Tutorials. 'Amplifier classes.' (), [Online]. Available: https://www.electronics-tutorials.ws/amplifier/amplifier-classes.html (visited on 15/12/2021).

[8] P. B. Kenington, *High Linearity RF Amplifier Design*, 1st ed. Norwood, MA: Artech House, 2000, pp. 94–102.

[9] D. M. Pozar, *Microwave Engineering*, 4th ed. Norwood, MA: Wiley, 2011, p. 178.

[10] Wikipedia. 'Scattering parameters.' (), [Online]. Available: https://en.wikipedia.org/wiki/Scattering_parameters (visited on 10/03/2022).

[11] Testips. 'S-parameters.' (), [Online]. Available: http://www.testips.com/sparams.php (visited on 15/12/2021).

[12] P. H. Smith, 'An improved transmission line calculator,' *Electronics*, vol. 17, p. 130, 2017.

[13] N. team - Nujira. 'Envelope tracking waveform.' (), [Online]. Available: https://commons.wikimedia.org/w/index.php?curid=16119096 (visited on 25/10/2021).

[14] M. Olavsbråten and D. Gecan, 'Bandwidth reduction for supply modulated rf pas using power envelope tracking,' *IEEE Microwave and Wireless Components Letters*, vol. 27, pp. 374–376, 2017.

[15] Electronicsnotes. 'Rf / microwave circulator / isolator basics.' (), [Online]. Available: https://www.electronics-notes.com/articles/radio/rf-microwave-circulator-isolator/what-is-an-rf-circulator-isolator.php (visited on 05/06/2022).

[16] P. Microwave. 'Rf directional coupler basics tutorial.' (), [Online]. Available: https://pandamw.com/rf-directional-coupler-basics-tutorial/ (visited on 16/12/2021).

[17] R. corporation. 'Ro4000® series high frequency circuit materials.' (), [Online]. Available: https://rogerscorp.com/-/media/project/rogerscorp/documents/advanced-electronics-solutions/english/data-sheets/ro4000-laminates-ro4003c-and-ro4350b---data-sheet.pdf (visited on 01/03/2022).

[18] Wolfspeed. 'Cg2h40010 datasheet.' (), [Online]. Available: https://assets.wolfspeed.com/uploads/2020/12/CG2H40010.pdf (visited on 07/12/2021).

Appendix A

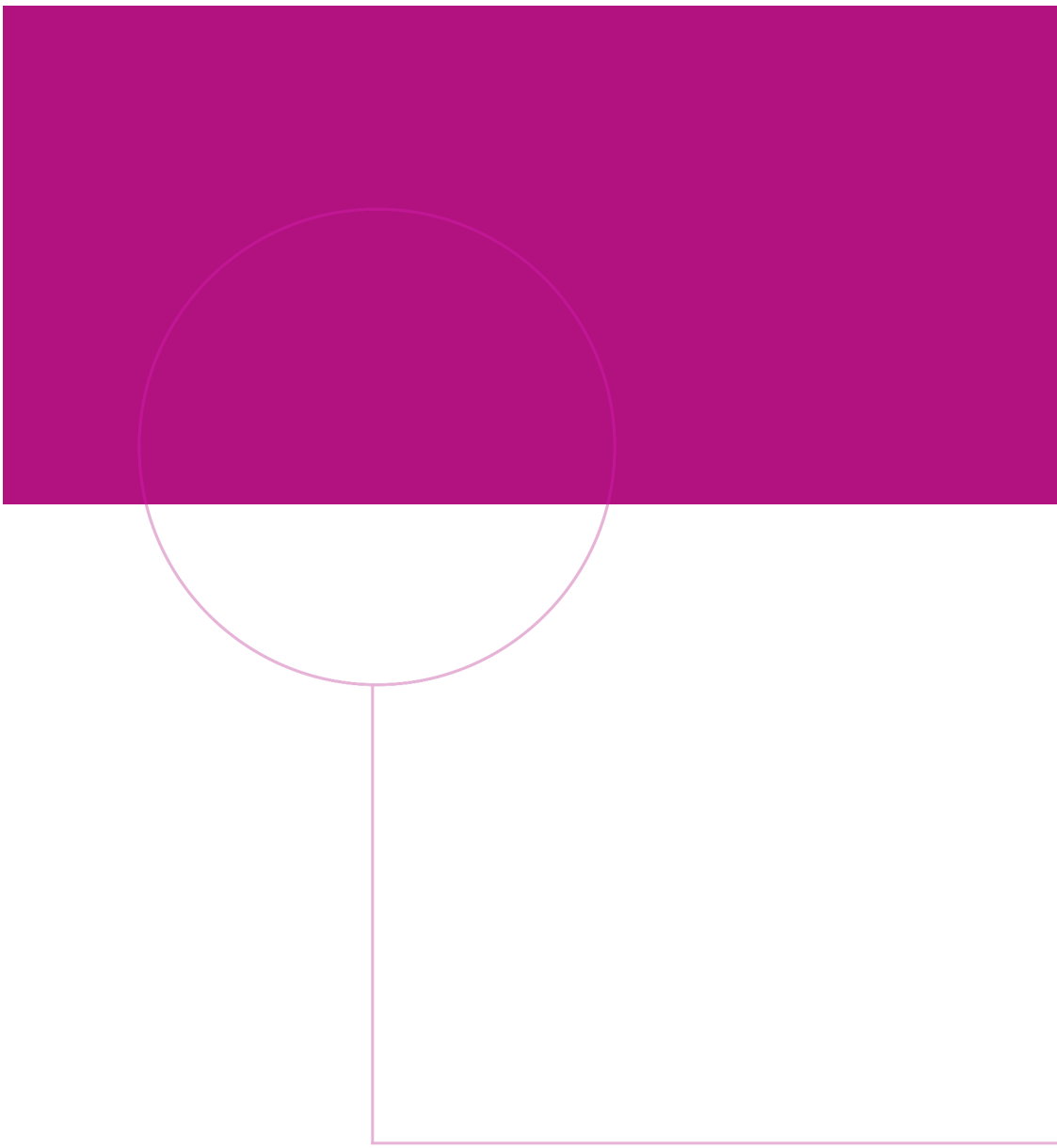
Sensitivity analysis - self bias rectifier

				GmG			
	10%	**5%**	**3%**		**3%**	**5%**	**10%**
50R	0,60	0,68	0,73	**0,95**	-	-	-
100R	0,76	0,83	0,86	**0,95**	-	-	-
150R	0,77	0,84	0,86	**0,95**	-	-	-
				GpG			
	10%	**5%**	**3%**		**3%**	**5%**	**10%**
50R	−163	−162	−162	−161	**−159**	−159	−158
100R	−162	−161	−160	**−159**	−158	−157	−157
150R	−160	−159	**−159**	−158	−158	−157	−157
				Gp2G			
	10%	**5%**	**3%**		**3%**	**5%**	**10%**
50R	−86	−84	**−84**	−77	−56	−38	158
100R	−89	−86	**−85**	−80	−67	−62	−28
150R	−87	−86	−85	**−83**	−82	−81	−80
				Gp3G			
	10%	**5%**	**3%**		**3%**	**5%**	**10%**
50R	-	-	19,00	121,00	-	-	-
100R	19	27	31	119	-	-	-
150R	-	-	-	−156	−55	−39	−21
				GmD			
	10%	**5%**	**3%**		**3%**	**5%**	**10%**
50R	0,44	0,52	0,55	0,66	**0,74**	0,76	0,80
100R	0,54	0,6	0,63	**0,72**	0,79	0,81	0,84
150R	0,64	0,69	**0,72**	0,79	0,84	0,86	0,88
				GpD			
	10%	**5%**	**3%**		**3%**	**5%**	**10%**
50R	139	144	147	157	164	166	171
100R	130	134	136	142	148	150	154
150R	133	135	137	140	145	147	149
				Gp2D			
	10%	**5%**	**3%**		**3%**	**5%**	**10%**
50R	−165	−156	**−152**	−129	−93	−82	−48
100R	−171	−167	−165	−157	**−144**	−141	−133
150R	−163	−159	−157	**−151**	−136	−129	−113
				Gp3D			
	10%	**5%**	**3%**		**3%**	**5%**	**10%**
50R	**42**	56	65	85	98	103	150
100R	**1**	108	110	145	177	-	-
150R	−21	−6	−2	10	40	**48**	60

Appendix B

Sensitivity analysis - active bias rectifier

	Decreased val		**Param**		**Increased val**	
10%	**5%**	**3%**		**3%**	**5%**	**10%**
			Pout			
7,68	**8,10**	**8,27**	**8,53**	**8,27**	**8,10**	**7,68**
			Gmf0			
0,73	0,82	0,86	0,95	0,98	0,99	0,99
			Gpf0			
175	177	178	180	185	186	188
			Gp2f0			
19	33	37	45	48	48	49
			Gp3f0			
-	-	-	14	152	156	-
			Gpdf0			
−81	−80	−78	−76	−76	−75	−75
			Gpd2f0			
			−115	−110	−109	−102
			Gpd3f0			
-	-	-	0	-	-	-
			Dmf0			
0,61	0,66	0,69	0,77	0,83	0,84	0,87
			Dpf0			
146	149	150	154	158	161	164
			Dp2f0			
−70	−6	28	113	168	176	-
			Dp3f0			
1	21	35	180	-	-	-
			Dpdf0			
−45	−40	−35	−29	-	-	-
			Dpd2f0			
-	-	-	−181	-	-	-
			Dpd3f0			
-	-	-	−176	-	-	-
	Decreased val		**Param**		**Increased val**	
10%	**5%**	**3%**		**3%**	**5%**	**10%**
			Pout			
7,68	**8,10**	**8,27**	**8,53**	**8,27**	**8,10**	**7,68**



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