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Impact of digital time delay on the stable grid-hosting capacity of large-scale centralised PV plant

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Abstract

Digital control system has been widely used for the inverters in PV plant. However, the effects of digital time delay of digital control system on grid-connected PV plants have not been fully studied. Therefore, in view of the stable grid-hosting capacity is a key parameter in the process of designing and operating of a grid-connected PV plant, this paper investigates in detail the influence of digital time delay on the stable grid-hosting capacity of large-scale centralised PV plant. Considering the practical situation of large-scale centralised PV plants, the stable grid-hosting capacity of plant is discussed with the conditions of inverters in PV plant have the same and different digital time delays. The analysis results revealed that stable grid-hosting capacity is varied with the digital time delay of inverter and the combination of the inverter with different digital time delays. Meanwhile, in order to realize a stable grid-connected PV plant in particular delay case, a procedure on how to determine the exact inverter number that can be used in a specific PV plant is provided. The theoretical analysis is verified by simulation and equivalent experiment results.

1 | INTRODUCTION

With the rapid development of the renewable energy, the advance in photovoltaic technology and growth in demand for power enable a wide deployment of large-scale centralized PV (LSCPV) plants due to their unique advantages over small-scale PV applications [1]. However, because the inverters in PV plant are coupled through the grid impedance and the degree of coupling is increased with the increase of grid-connected inverter number, the stability of grid-connected LSCPV system becomes more complicated with increasing of its gird-hosting capacity [2, 3].

Generally, considering the inverters in LSCPV plant are coupled with grid and other inverters through grid impedance, the effects of grid impedance on grid-connected LSCPV system has attracted broad attention. Agorreta et al. [3] built the Norton equivalent model of grid-connected LSCPV system and found that equivalent grid-side impedance of single inverter is increased with the number of grid-connected inverter in plant. The increasing of equivalent grid impedance lead to decrease of system stability margin, which may cause harmonics amplification problem and further decrease the system stability [4–6]. In order to analysis the stability of grid-connected LSCPV system more accurately, Zhou et al. [7] modelled the grid-connected LSCPV system with considering the influence of double split winding transformers in plant, and analysed the influence of equivalent grid impedance on the stability range of grid-connected PV inverters.

In addition to the equivalent grid impedance, the effects of control structure [8], control parameters [9], sampling mode [10], and other inverter parameters on system stability and harmonic characteristics are also explored in many literatures. Meanwhile, other factors also has an impact on system, for example the type of load will influence the power sharing of multi-inverter system [11]; the circulating current of the system with different types inverter becomes more complicated and hard to suppress [12]. For the grid-voltage harmonic, Zhou et al. [13] found that power quality and stability of system are seriously deteriorated by the harmonic voltage distortions. Although the effects of various factors on grid-connected multi-inverter system have been investigated in existing literatures, the impacts of digital time delay on system have not been fully studied yet.

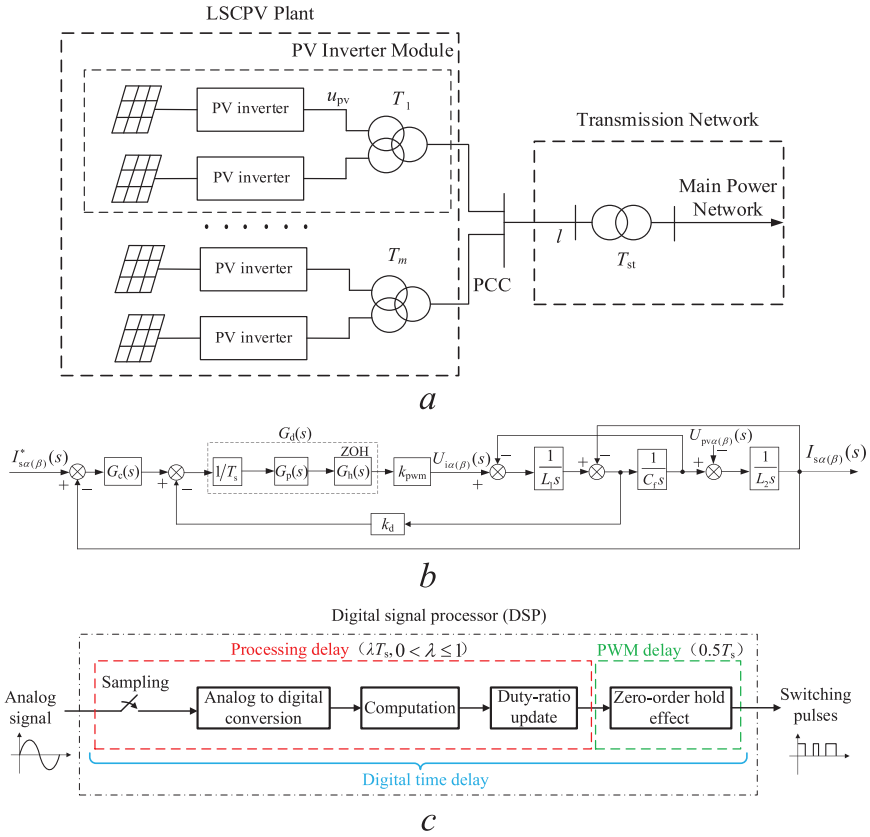


FIGURE 1 Grid-connected LSCPV system (a) main topology, (b) inner loop control model of inverter and (c) digital time delay of digital control system

Along with the popularization of digitally controlled inverter in LSPV plant, the effects of digital time delay on system have become inevitable. For the digital time delay of inverter, [14–16] found that stability of grid-connected inverters is deteriorated by the digital time, which embodies in a reduction of system stability margin. Meanwhile, the system steady-state error is increased with the digital time delay increases [17], and the design of inverter control parameters will become stricter since the system damping region is reduced with the digital time delay [18, 19]. Furthermore, the performance of traditional control structures are also weaken by the digital time delay of inverter, for example, the sliding mode control structure [20], deadbeat control structure [21], active damping structure [22], grid-voltage feedforward structure [23] and so on. However, it can be found from above that current literatures about effects of digital time delay mainly focus on the single inverter. There are few research carried on the impact of digital time delay on grid-connected multi-inverter system, especially the grid-connected LSCPV system.

For the specific effects of digital time delay on grid-connected LSCPV systems, [24–26] modelled the PV plant with considering the digital time delay of inverter and described the effects of digital time delay on harmonics damping performance. In addition, in order to simplify the process of modelling and analysis, most of related research on the effects of digital time delay are mainly focused on the multi-inverter system in PV plant, for example, the bandwidth [27], operating model [28], etc. Moreover, [29] and [30] have shown that an increase of digital time delay of inverter also has a negative influence on reactive power sharing performance in parallel operation inverters.

From the above analysis of existing research, it can be found that many studies have been carried out that analysis the grid-connected multi-inverter system, but only a few have addressed the effects of the digital time delay of inverter on grid-connected multi-inverter system. For stable grid-hosting capacity of grid-connected multi-inverter system, which is important to the design and capacity expansion of grid-connected LSCPV plants [7], the influence of the digital time delay of inverter on it remained unclear. This paper is concerned with precisely that aspect, the study of grid-hosting capacity of LSCPV plants taking into account the effects of digital time delay on grid-connected LSCPV system. In Section 2, a Norton equivalent model of the grid-connected LSCPV system is built based on a typical topology of a grid-connected LSCPV system. The effects of digital time delay on the stable grid-hosting capacity of LSCPV plants are studied for two LSCPV plant scenarios that are described in Sections 3 and 4, respectively. The simulation and experimental results are presented in Section 5 to validate the analysis. Finally, conclusions are drawn in Section 6.

2 | GRID-CONNECTED LSCPV SYSTEM

2.1 | System description

Figure 1a shows a typical topology of a grid-connected LSCPV system, which mainly consists of LSCPV plant and

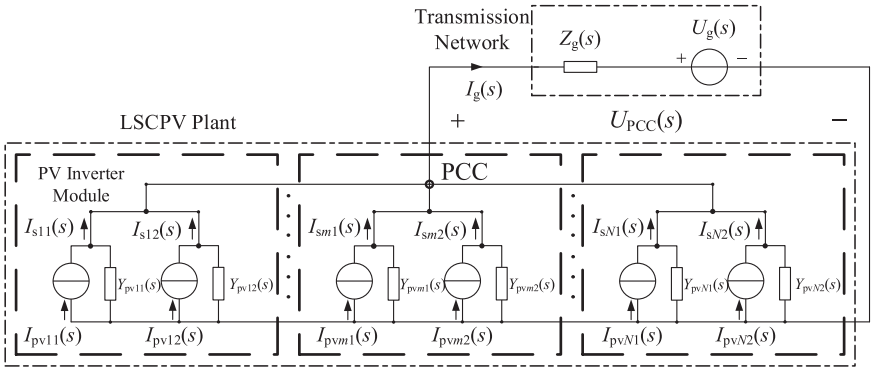


FIGURE 2 Equivalent model of grid-connected LSCPV system

transmission network. T_m is the mth double split-winding transformers in LSCPV plant and two PV inverters constitute a PV inverter module. T_{st} represents the large-capacity step-up transformer.

Generally, a cascade control strategy, which contains an inner loop and an outer loop, is used in PV inverters [3]. The inner loop and outer loop control the grid-side current and the dc-side voltage, respectively. Therefore, considering the inner loop and outer loop control is decoupled, in order to avoid the influence caused by the dc-side voltage fluctuation, the outer loop is not considered here and thus the dc-bus of inverter can be assumed as a constant voltage source [15]. Moreover, the effects of the phase locked loop unit are also ignored in the modelling and analysis, since the instantaneous power control is used to generate the reference signal [2].

2.2 | Modelling of the system

To acquire an independent control of two-phase current without any decoupling modules, a current control loop in stationary $\alpha\beta$-frame is adopted and the control model of digitally controlled inverter is given in Figure 1b. G_c(s) is the current controller and a proportional-resonant controller is adopted. Meanwhile, as shown in Figure 1c, the digital time delay is the time duration from the sampling of analog signal to the obtaining of switching pulses. Normally, the digital time delay of digital control system mainly includes the processing delay and the PWM delay [18]. The processing delay and PWM delay is represented as G_p(s) and G_h(s) in Figure 1b, respectively. Moreover, $1/T_s$ represents the sampler and T_s is the system sampling period.

For the synchronous sampling scheme, the delay coefficient λ shown in Figure 1c is 1 and then the total digital time delay of control loop is 1.5 T_s. To obtain a rational transfer function, a second-order Padé approximation is used to describe the delay in s-domain, which can be given by

$$G_d(s) \approx \frac{(1.5sT_s)^2 - 9T_s s + 12}{(1.5sT_s)^2 + 9T_s s + 12}. \tag{1}$$

According to Figure 1b, an equivalent model of grid-connected LSCPV system with N inverter modules can be derived and shown Figure 2, where the output current $I_{pvmn}(s)$ and equivalent output admittance $Y_{pvmn}(s)$ of nth inverter in mth inverter module are expressed as

$$I_{pvmn}(s) = \frac{G_{mn}(s)I^*_{smn}(s)}{Y_{eqmn}(s)L_{Tmn}s + 1} \tag{2}$$

$$Y_{pvmn}(s) = \frac{Y_{eqmn}(s)}{Y_{eqmn}(s)L_{Tmn}s + 1} \tag{3}$$

where $G_{smn}(s) = k_{pwm}G_{dmn}(s)$, $\omega_{rmn} = \sqrt{1/(L_{2mn}C_{fmn})}$, $\omega_{resmn} = \sqrt{(L_{1mn} + L_{2mn})/(L_{1mn}L_{2mn}C_{fmn})}$, $n = 1, 2$.

$$G_{mn}(s) = \frac{G_{smn}(s)\omega^2_{rmn}G_{cmn}(s)}{L_{1mn}s^3 + k_{dmn}G_{smn}(s)s^2 + L_{1mn}\omega^2_{resmn}s + G_{smn}(s)G_{cmn}(s)\omega^2_{rmn}} \tag{4}$$

$$Y_{eqmn}(s) = \frac{(L_{1mn}/L_{2mn})s^2 + (k_{dmn}G_{smn}(s)/L_{2mn})s + \omega^2_{rmn}}{L_{1mn}s^3 + k_{dmn}G_{smn}(s)s^2 + L_{1mn}\omega^2_{resmn}s + G_{smn}(s)G_{cmn}(s)\omega^2_{rmn}} \tag{5}$$

$G_{mn}(s)$ and $Y_{eqmn}(s)$ represent the control coefficient and equivalent admittance of the nth inverter in mth inverter module, respectively.

Based on Figure 2, the transfer function of grid-side current of the nth inverter in mth inverter module can be derived as

$$\begin{aligned} I_{smn}(s) = &\left(1 - \frac{Y_{pvmn}(s)}{\sum_{m=1}^{N}\sum_{n=1}^{2} Y_{pvmn}(s) + Y_g(s)}\right) I_{pvmn}(s) \\ &- \frac{Y_{pvmn}(s)Y_g(s)}{\sum_{m=1}^{N}\sum_{n=1}^{2} Y_{pvmn}(s) + Y_g(s)} U_g(s) \\ &- \sum_{t=1}^{N}\sum_{h=1,h\neq n}^{2} \frac{Y_{pvmn}(s)}{\sum_{m=1}^{N}\sum_{n=1}^{2} Y_{pvmn}(s) + Y_g(s)} I_{pvth}(s). \end{aligned} \tag{6}$$

3 | STABLE GRID-HOSTING CAPACITY OF THE LSCPV PLANT CONTAINS SAME DIGITAL TIME DELAY

In most LSCPV plants, the PV inverters are installed by the same firm and are of the same type [4]. Hence, the equivalent output admittance $Y_{\mathrm{pvmn}}(s)$ of the inverter contained in Equation (6) can be considered the same, and thus Equation (6) can be simplified as

$$\begin{aligned} I_{smn}(s) = & \left(1 - \frac{Y_{\mathrm{pv}}(s)}{2NY_{\mathrm{pv}}(s) + Y_{\mathrm{g}}(s)}\right) I_{\mathrm{pv}mn}(s) \\ & - \frac{Y_{\mathrm{pv}}(s)Y_{\mathrm{g}}(s)}{2NY_{\mathrm{pv}}(s) + Y_{\mathrm{g}}(s)} U_{\mathrm{g}}(s) \\ & - \sum_{t=1}^{N} \sum_{b=1, b\neq n}^{2} \frac{Y_{\mathrm{pv}}(s)}{2NY_{\mathrm{pv}}(s) + Y_{\mathrm{g}}(s)} I_{\mathrm{pv}tb}(s). \end{aligned} \tag{7}$$

Substituting Equations (2) and (3) into Equation (7), the closed-loop transfer function of the grid-side current of inverter can be derived as

$$\begin{aligned} I_{smn}(s) = & \left[1 - \frac{Y_{\mathrm{eq}}(s)}{2NY_{\mathrm{eq}}(s) + Y_{\mathrm{g}}(s)\left(Y_{\mathrm{eq}}(s)L_{\mathrm{T}}s + 1\right)}\right] \\ & \times \frac{G(s)}{Y_{\mathrm{eq}}(s)L_{\mathrm{T}}s + 1} I^{*}_{smn}(s) \\ & - \frac{Y_{\mathrm{eq}}(s)Y_{\mathrm{g}}(s)}{2NY_{\mathrm{eq}}(s) + Y_{\mathrm{g}}(s)\left(Y_{\mathrm{eq}}(s)L_{\mathrm{T}}s + 1\right)} U_{\mathrm{g}}(s) \\ & - \frac{Y_{\mathrm{eq}}(s)}{2NY_{\mathrm{eq}}(s) + Y_{\mathrm{g}}(s)\left(Y_{\mathrm{eq}}(s)L_{\mathrm{T}}s + 1\right)} \\ & \times \frac{G(s)}{Y_{\mathrm{eq}}(s)L_{\mathrm{T}}s + 1} \sum_{t=1}^{N} \sum_{b=1, b\neq n}^{2} I^{*}_{stb}(s). \end{aligned} \tag{8}$$

Table 1 shows the parameters of the 500 kW inverter, which the system sampling frequency f_{s} is twice the switching frequency f_{sw} since the inverter adopts a synchronous sampling scheme. According to Equation (2) and the parameters listed in Table 1, Figure 3 shows the root locus of grid-side current as the digital time delay varies from 1 to 600 μs. As seen, the stability of inverter is decreased with the increase of digital time delay. The intersection of root locus and imaginary axis is the marginal delay that the inverter can remain stable. Then, the delay range that the inverter is stable can be derived as Equation (9), by solving the characteristic equation of Equation (2).

TABLE 1 Main parameters of 500 kW inverter

Parameters	Values	Parameters	Values
k_{p}	0.001	L_1	0.15 mH
k_{r}	0.2	L_2	0.12 mH
k_{d}	0.00035	C_{f}	218 μF
ω_0	100 π rad/s	ω_{i}	π rad/s
V_{dc}	800 V	u_{pv} (rms)	156 V
f_{sw}	2.5 kHz	f_{s}	5 kHz

$$0\mu s < T_{\mathrm{d}} < 510\mu s. \tag{9}$$

Considering the switching frequency of large-capacity PV inverter which is usually in the range of 2–3 kHz, which corresponds to the digital time delay range of 250–375 μs when the synchronous sampling scheme is adopted. Therefore, it can be found from Equation (9) that, the parameters listed in Table 1 are applicable to the system that switching frequency is within the range of 2–3 kHz. In such a situation, the parameters of the inverter can remain the same in spite of the change of switching frequency.

Table 2 shows the main parameters of double split winding transformer and transmission network, which are chosen from a practical grid-connected LSCPV system in China's Inner Mongolia. According to the parameters listed in Table 2, the values of equivalent inductance of double split winding transformer and equivalent resistance of transmission network can be obtained as

$$\begin{cases} L_{\mathrm{T}} = 10.4\mu H \\ L_{\mathrm{g}} = (0.54 + 15.78)\,\mu H = 16.32\mu\mathrm{H} \\ R_{\mathrm{g}} = 3.06\mathrm{m}\Omega \end{cases}. \tag{10}$$

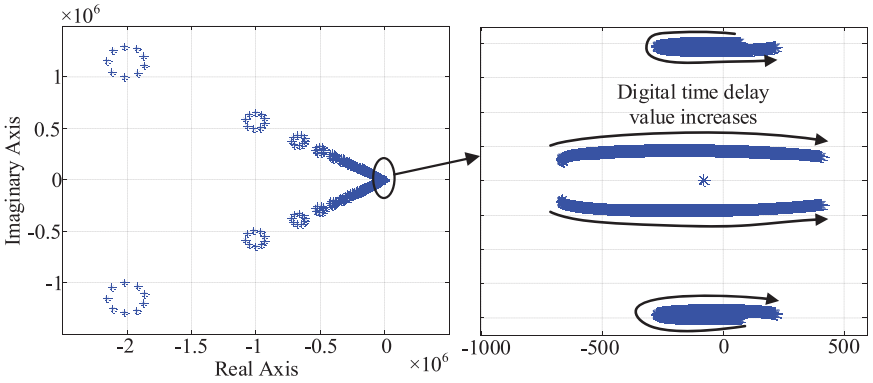


FIGURE 3 Root locus of i_{pv} as digital time delay varies

TABLE 2 Main parameters of the double split winding transformer and transmission network

Component	Description	Notation	Value
Double split winding transformer	Rated voltage ratio (High voltage/low voltage 1/low voltage 2)	$U_h/U_{l1}/U_{l2}$	$10 \pm 2 \times 2.5\%/0.27/0.27$ kV
	Impedance voltage	U_z	4.5%
	Rated capacity	S_s	1000/500/500 kV
Large-capacity Step-up transformer	Short circuit voltage ratio (%)	$U_s\%$	10.5
	Rated voltage of high voltage side	U_H	$110 \pm 8 \times 1.25\%$kV
	Rated voltage of low voltage side	U_L	10.5 kV
	Rated capacity	S	50,000 kVA
Transmission line	Unit resistance	r	0.21 Ω/km
	Unit reactance	x	0.34 Ω/km
	Line length	l	20 km

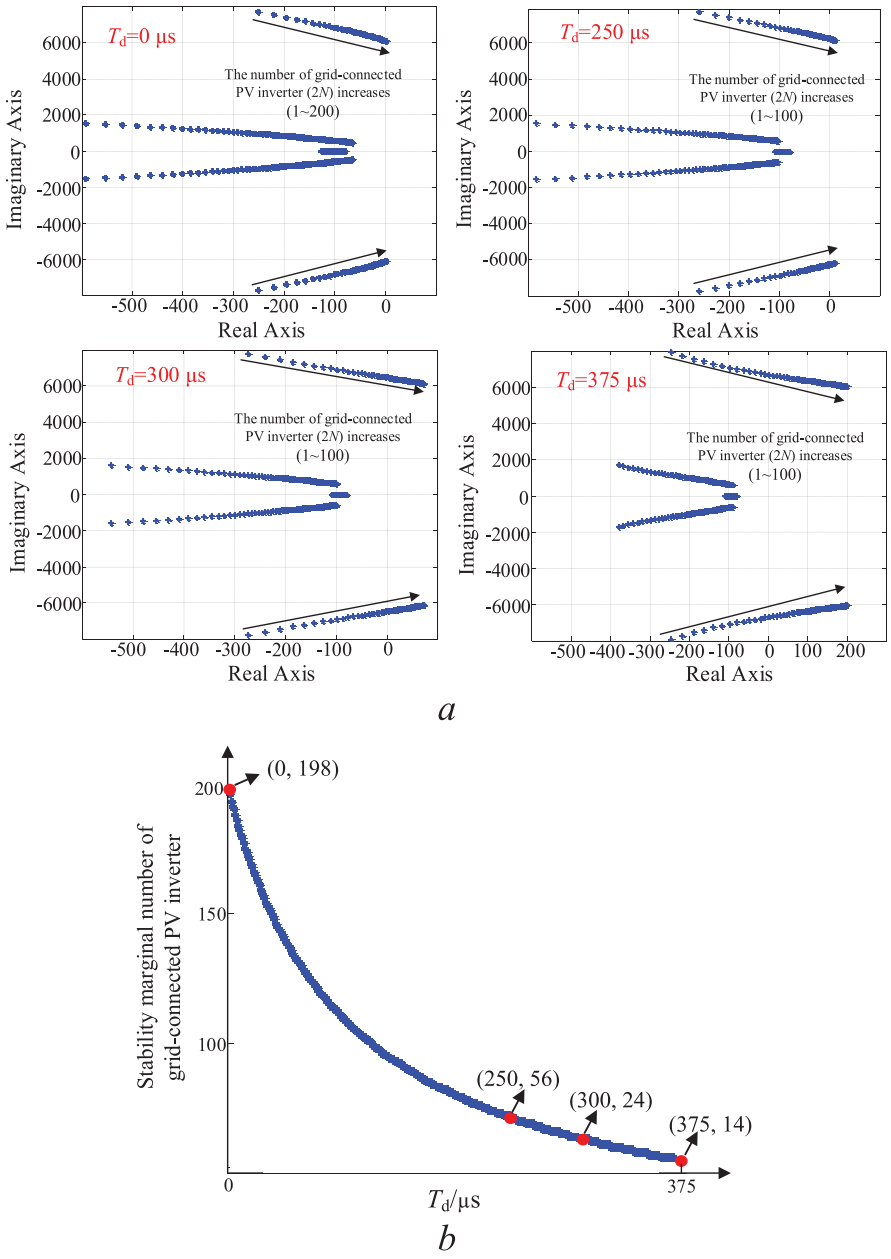
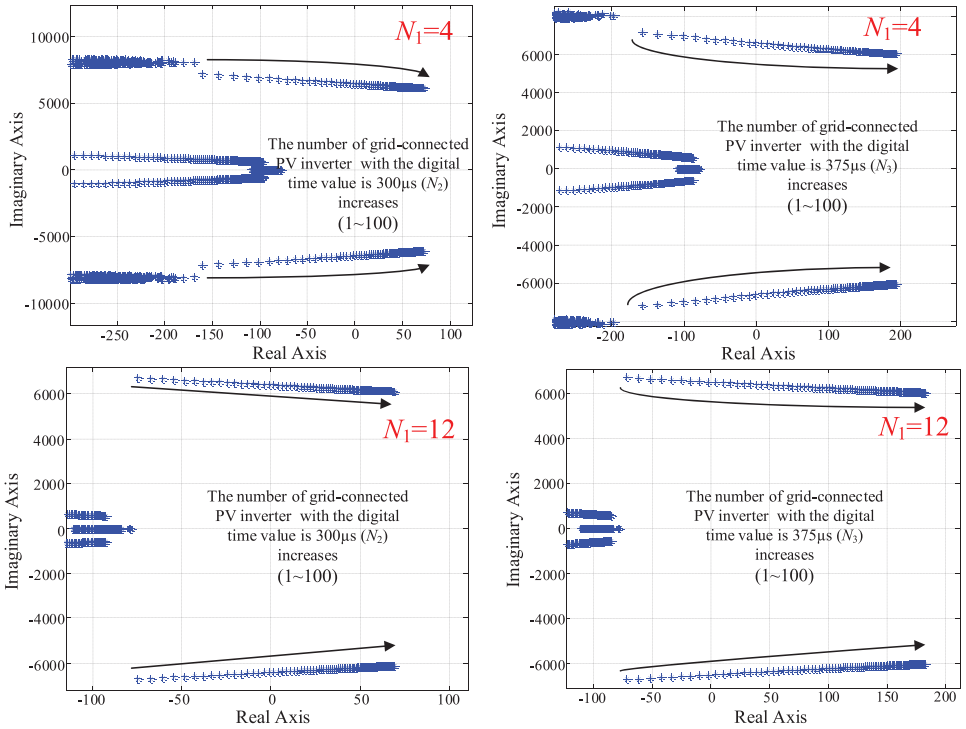


FIGURE 4 Root locus and stability marginal number diagram. (a) Root locus of the grid-side current i_s for different digital time delays. (b) Stability marginal number of grid-connected inverter as digital time delay varies



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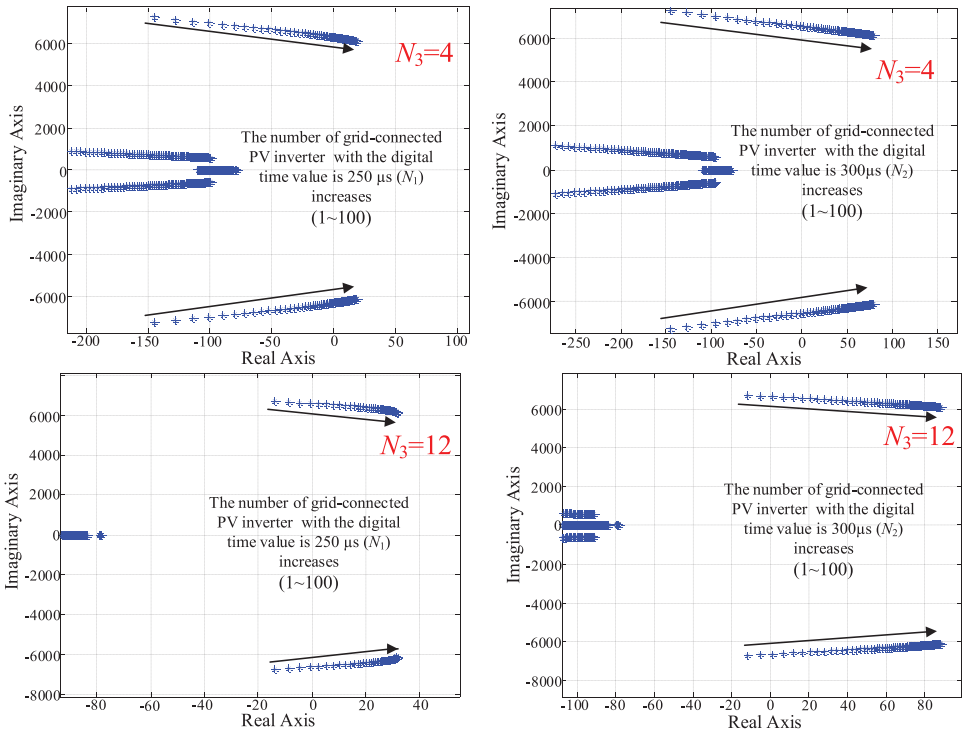

b

FIGURE 5 Root locus and stability marginal number diagrams. (a) Root locus of i_s for Case I (b) Root locus of i_s for Case II. (c) Stability marginal number of grid-connected inverter as digital time delay varies

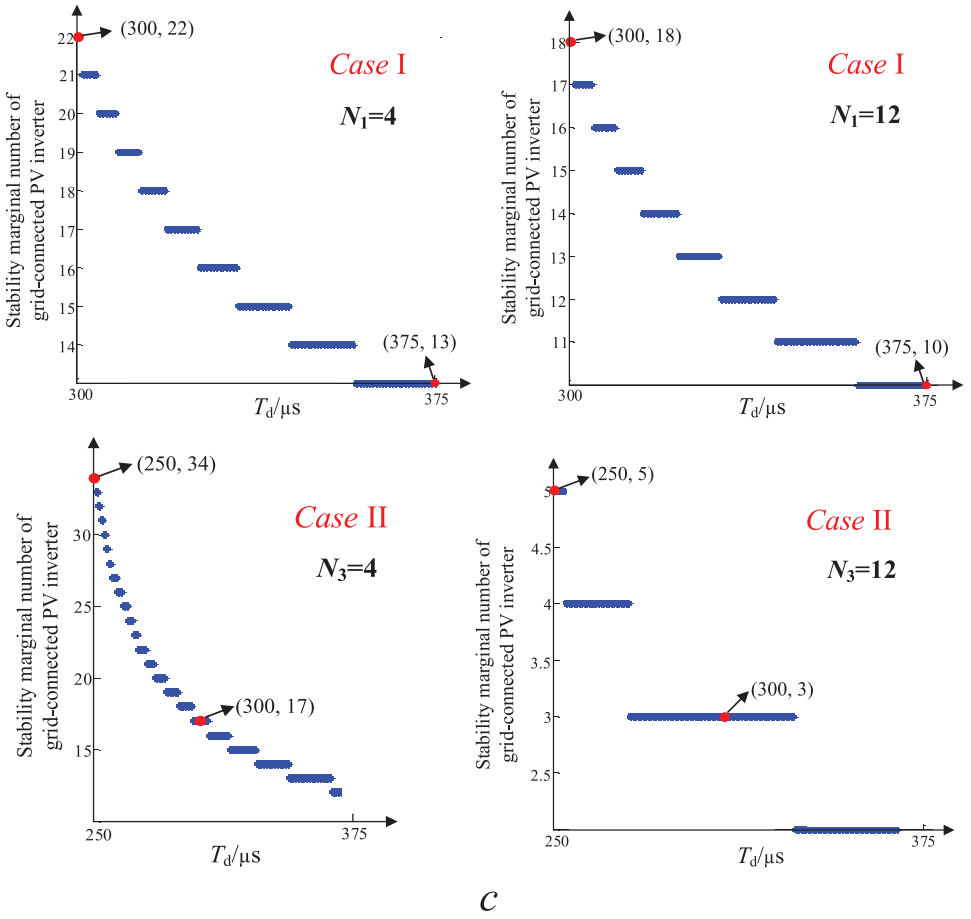

FIGURE 5 Continued

According to Equation (8), Figure 4a shows the root locus of grid-side current as the number of grid-connected inverters (2*N*) varies. In Figure 4, the digital time delay 250, 300 and 375 μs corresponding to the commonly used large-capacity inverter switching frequency 3, 2.5 and 2 kHz. As seen, the closed-loop poles gradually approach and finally across the imaginary axis as the number of grid-connected inverter increases. Moreover, the increase in digital time delay enables poles to get closer to the imaginary axis when the grid-connected inverter number is the same. These indicate that both of digital time delay and inverter number have negative effects on the stability of system, and this effects become stronger with the increase of digital time delay and grid-connected inverter number.

According to the stability criterion, the intersection of root locus and imaginary axis determines the stability marginal number of grid-connected inverter. Figure 4b shows the stability marginal number of grid-connected inverters as the digital time delay varies from 0 to 375 μs, which are derived from the characteristic equation of Equation (8). It can be seen that, the stability marginal number of grid-connected inverter is decreased significantly with the increase of digital time delay. In other words, the impact of digital time delay on stable grid-hosting capacity of LSCPV plant will become more apparent with the digital time delay of inverter increases.

4 | STABLE GRID-HOSTING CAPACITY OF THE LSCPV PLANT CONTAINS DIFFERENT DIGITAL TIME DELAYS

In practical LSCPV plant, different types of inverter may be adopted in the expansion of plant, and thus may result in the inverters in the LSCPV plant have different digital time delays. Assuming the inverters in LSCPV plant contain h ($h > 1$) different digital time delay, the number of the inverter with same digital time delay is denoted as N_i ($i = \sim 1$–h). According to Equation (6), the transfer function of grid-side current of jth ($0 < j < N_i$) inverter can be derived as

$$I_{sij}(s) = \left(1 - \frac{Y_{\mathrm{pv}ij}(s)}{\sum_{k=1}^{h}\sum_{l=1}^{N_i} Y_{\mathrm{pv}kl}(s) + Y_{\mathrm{g}}(s)}\right) I_{\mathrm{pv}ij}(s) - \frac{Y_{\mathrm{pv}ij}(s)Y_{\mathrm{g}}(s)}{\sum_{k=1}^{h}\sum_{l=1}^{N_i} Y_{\mathrm{pv}kl}(s) + Y_{\mathrm{g}}(s)} U_{\mathrm{g}}(s) - \sum_{q=1,q\neq j}^{N_i} \frac{Y_{\mathrm{pv}ij}(s)}{\sum_{k=1}^{h}\sum_{l=1}^{N_i} Y_{\mathrm{pv}kl}(s) + Y_{\mathrm{g}}(s)} I_{\mathrm{pv}iq}(s)$$

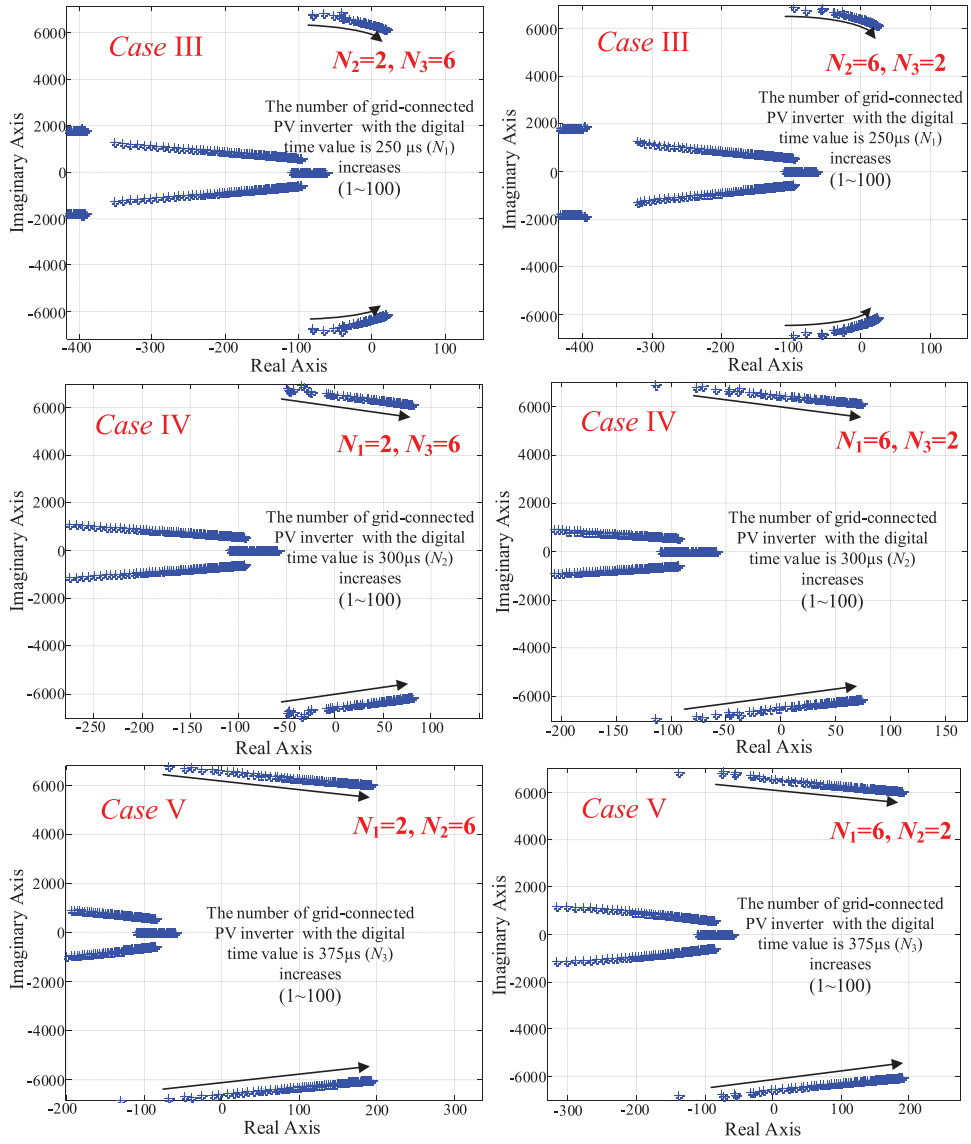

FIGURE 6 Root locus and stability marginal number diagram. (a) Root locus of i_s as the number of added inverters varies. (b) Stability marginal number of grid-connected inverters as digital time delay varies

$$-\sum_{p=1,p\neq i}^{b}\sum_{q=1}^{N_p}\frac{Y_{\mathrm{pv}ij}(s)}{\sum_{k=1}^{b}\sum_{l=1}^{N_i}Y_{\mathrm{pv}kl}(s)+Y_{\mathrm{g}}(s)}I_{\mathrm{pv}pq}(s). \tag{11}$$

The transfer function of equivalent current source (I_{pv}) and equivalent admittance (Y_{pv}) are the same for the inverter with the same digital time delay. Thus, the grid-side current of the inverters with same digital time delay are the same and then Equation (11) can be simplified as

$$I_{si}(s)=\left(1-\frac{N_iY_{\mathrm{pv}i}(s)}{\sum_{k=1}^{b}N_kY_{\mathrm{pv}k}(s)+Y_{\mathrm{g}}(s)}\right)I_{\mathrm{pv}i}(s)$$

$$-\frac{Y_{\mathrm{pv}i}(s)Y_{\mathrm{g}}(s)}{\sum_{k=1}^{b}N_kY_{\mathrm{pv}k}(s)+Y_{\mathrm{g}}(s)}U_{\mathrm{g}}(s)$$

$$-\sum_{p=1,p\neq i}^{b}\frac{N_pY_{\mathrm{pv}i}(s)}{\sum_{k=1}^{b}N_kY_{\mathrm{pv}k}(s)+Y_{\mathrm{g}}(s)}I_{\mathrm{pv}p}(s). \tag{12}$$

In order to facilitate the process of analysis, the number of inverters with the digital time delay of 250, 300 and 375 μs, are denoted as N_1, N_2 and N_3, respectively. Assuming that inverters in original LSCPV plant have the same digital time delay, two different delay cases are defined as follows:

Case I: When the digital time delay of inverters in original LSCPV plant is 250 μs and the number of inverters is

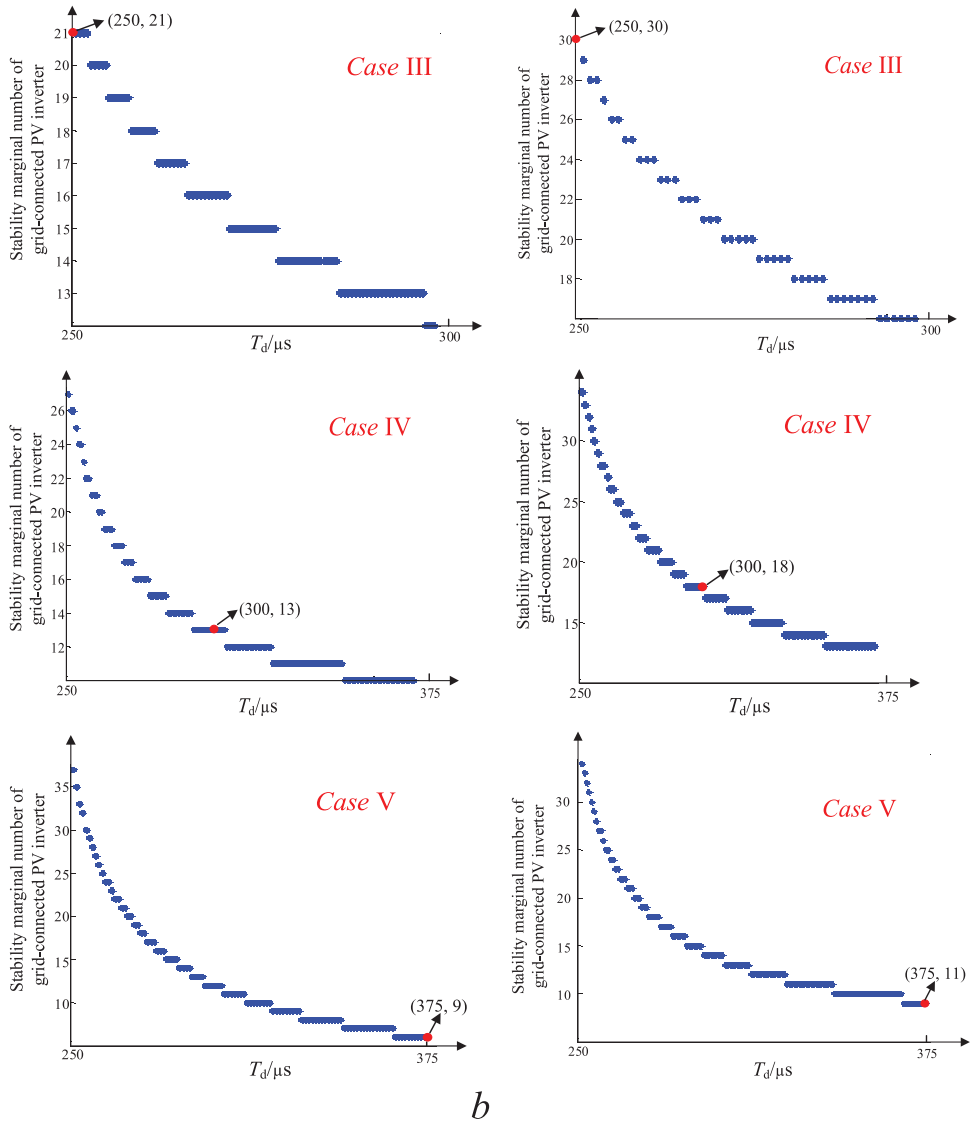

FIGURE 6 Continued

4 and 12, respectively, the inverters with a larger digital time delay are added to the original LSCPV plant.

Case II: When the digital time delay of inverters in original LSCPV plant is 375 μs and the number of inverters is 4 and 12, respectively, the inverters with a smaller digital time delay are added to the original LSCPV plant.

According to Equation (12), the root locus of the grid-side current for Cases I and II as number of grid-connected inverter number increases from 1 to 100, are shown in Figure 5a,b, respectively. As shown in Figure 5a,b, a pair of poles gradually approaches the imaginary axis as grid-connected inverter number and digital time delay of added inverters increases. It proves once again that digital time delay and grid-connected inverter number have a negative effect on the stability of the system. Moreover, it is obvious that stability marginal number of inverter is decreased as the digital time delay of added inverter increases.

Figure 5c shows the stability marginal number of grid-connected inverter for Cases I and II, as the digital time delay of added inverter varies. As seen, the stability marginal number of grid-connected inverter is decreased with the increase of the digital time delay of added inverter. By comparing the stability marginal numbers of the grid-connected inverter shown in Figures 4b and 5c, it can be found that the addition of the inverters with a larger digital time delay will reduce the stability range of grid-connected inverter number, and the stability range of grid-connected inverter number will be extended as the inverter with a smaller digital time delay is added. Moreover, with considering the number of inverters in original LSCPV plant and added inverters, the stability ranges of total grid-connected inverter number is increased in Case I and decreased in Case II as the number of inverters in original LSCPV plant increases.

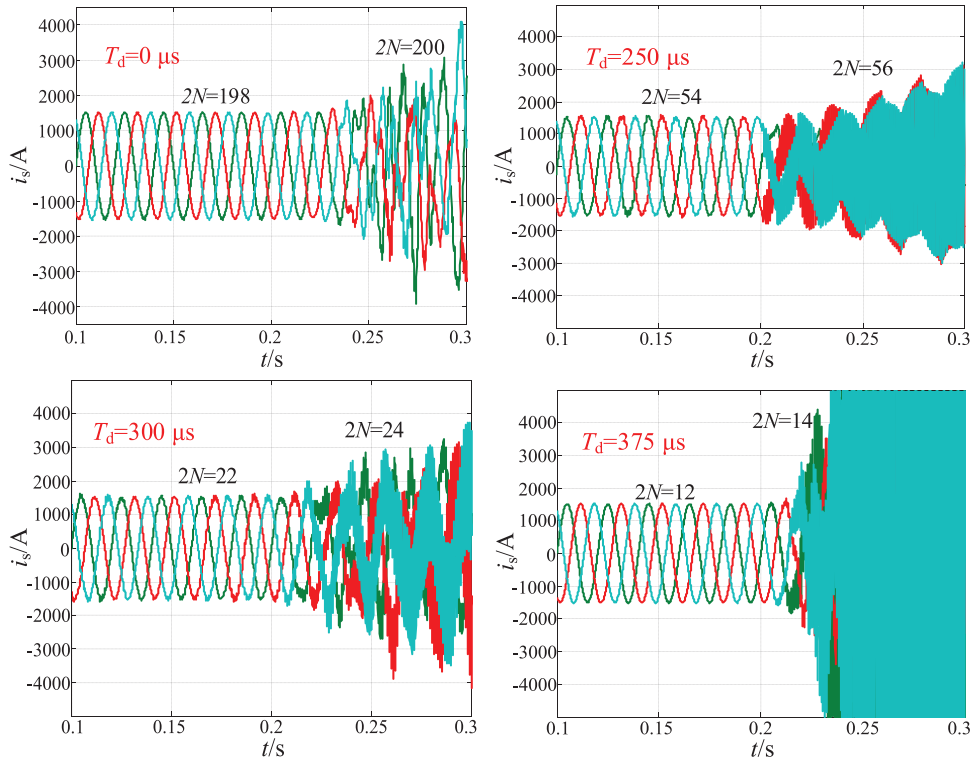

FIGURE 7 Simulation waveforms of i_s under different digital time delay T_d with larger digital time delay and the decline of the upper limit of stable grid-hosting capacity will be more significant as the digital time delay of added inverter increases

In addition to the scenario of inverters original LSCPV plant have the same digital time delay, the scenario of inverters in original LSCPV plant have different digital time delays is also discussed based on the three different delay cases given below:

Case III: The inverters in original LSCPV plant have two different digital time delays: 300 and 375 μs. When the number of inverters in original LSCPV plant is $N_2 = 2$, $N_3 = 6$ and $N_2 = 6$, $N_3 = 2$, respectively, inverters that have a smaller digital time delay are added.

Case IV: The inverters in original LSCPV plant have two different digital time delays: 250 and 375 μs. When the number of inverters in original LSCPV plant is $N_1 = 2$, $N_3 = 6$ and $N_1 = 6$, $N_3 = 2$, respectively, the added PV inverters have a digital time delay that is midway between the two digital time delays of the inverters in original LSCPV plant.

Case V: The inverters in original LSCPV plant have two different values of digital time delay: 250 and 300 μs. When the number of inverters in original LSCPV plant is $N_1 = 2$, $N_2 = 6$ and $N_1 = 6$, $N_2 = 2$, respectively, the inverters that have a larger digital time delays are added.

Figure 6a shows the root locus of grid-side current i_s for Cases III, IV and V as the number of added inverter varies. As seen, the poles are closer to imaginary axis as the number of grid-connected inverter and proportion of the inverter with larger digital time delay in original LSCPV plant increases. The position changes of poles indicate that added inverter and the increase of inverter number with a larger digital time delay will reduce system stability.

According to Equation (12), Figure 6b shows the stability marginal number of grid-connected inverter for Cases III, IV and V, as the digital time delay of added inverter varies. The stability marginal number of grid-connected inverter shown in Figure 6b further illustrates that stability ranges of grid-connected inverter number is decreased with the increase of digital time delays of added inverters. If the original LSCPV plant has a higher proportion of the inverters with smaller digital time delay, it will exhibit a greater stability range of grid-connected inverter number.

Therefore, according to the analysis above, the effects of digital time delay on stable grid-hosting capacity of the LSCPV plant have different digital time delays can be concluded as follows:

1. The addition of the inverter with smaller digital time delay will increase the stability of the original system and thus make the system able to break through the maximum stability marginal value of grid-hosting capacity, and the upper limit of stable grid-hosting capacity will increase as the digital time delay of added inverter decreases. The stability of original system will decrease with the addition of inverter.
2. The impact of the added inverter on system stability will decrease with the increase of the number of inverters with smaller digital time delay in original system. In short, a higher proportion of inverters with smaller digital time delays will lead to higher stability which enables the system to have a larger expansible grid-hosting capacity.

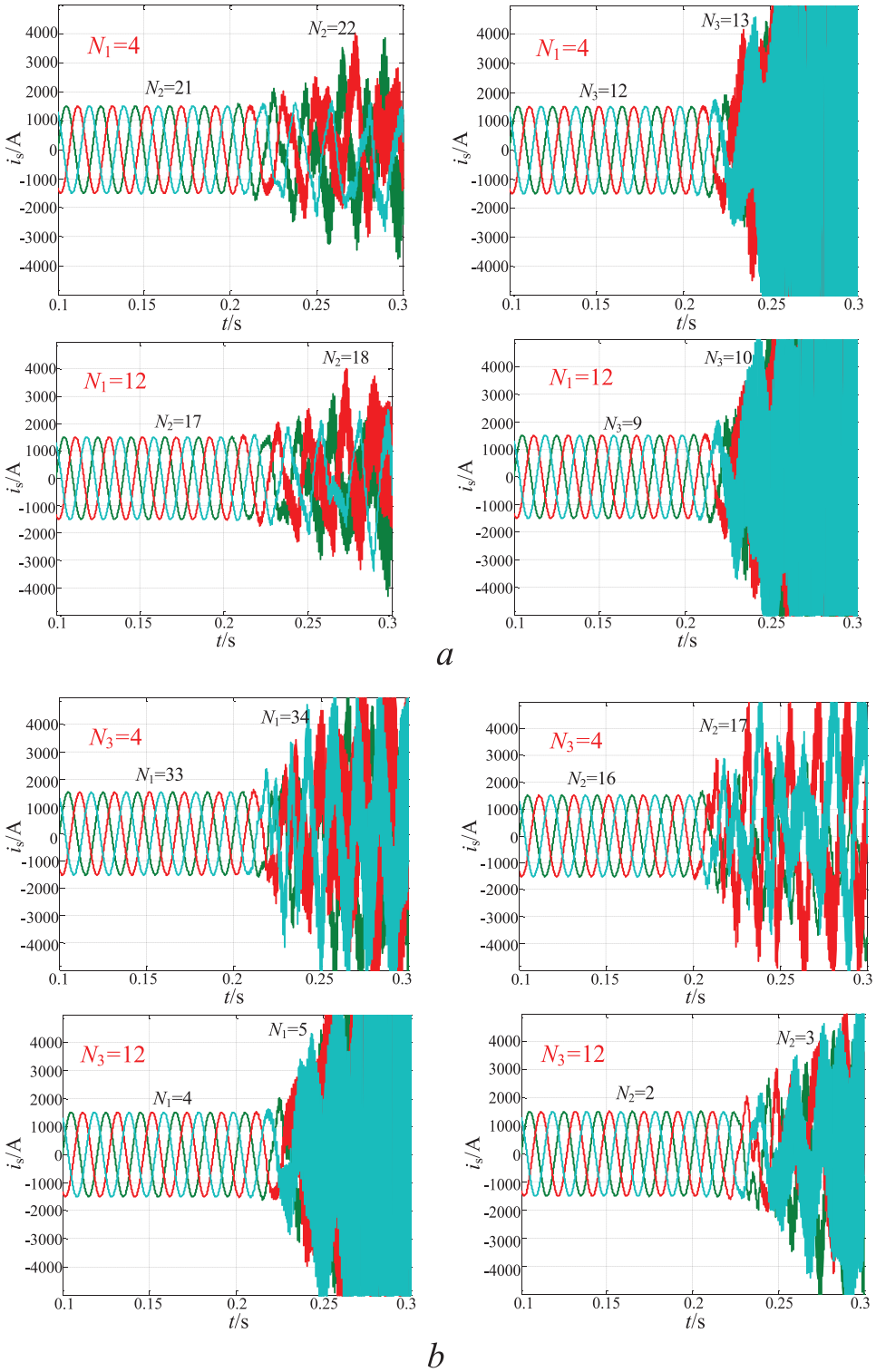

FIGURE 8 Simulation waveforms of i_s. (a) Simulation waveforms of i_s for Case I. (b) Simulation waveforms of i_s for Case II

5 | SIMULATION AND EXPERIMENTAL RESULTS

Since the building of a grid-connected LSCPV system is difficult to achieve in lab conditions, a high-fidelity simulation model of the grid-connected LSCPV system was built in MATLAB/SIMULINK to validate the theoretical analysis in the above sections. The main parameters of inverters and other main components are shown in Tables 1 and 2, respectively.

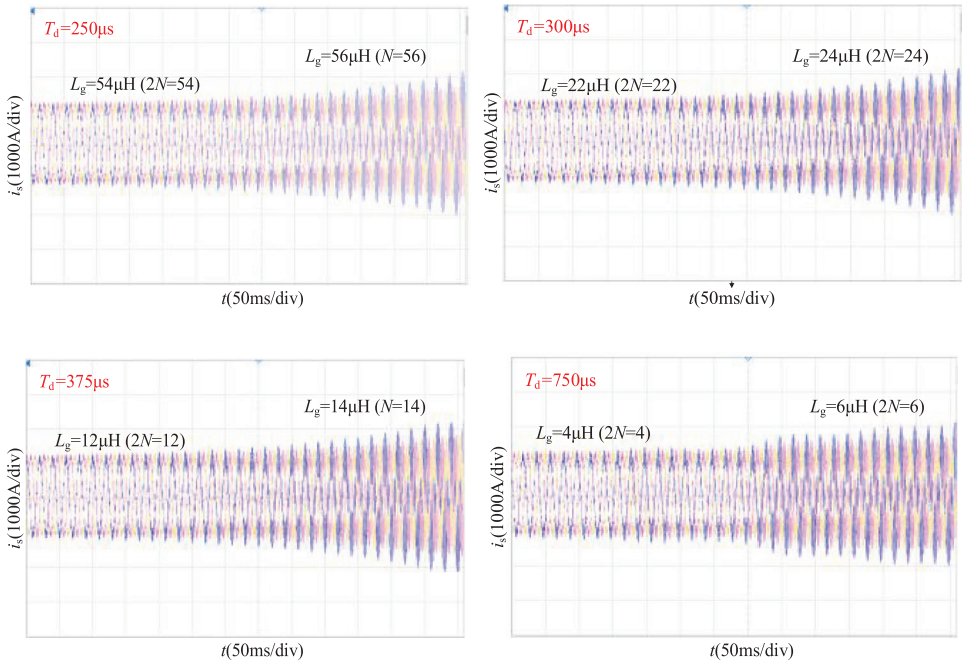

FIGURE 9 Experimental waveforms of i_s under different digital time delay T_d

Figure 7 shows the grid-side current of grid-connected inverter when the number of grid-connected inverter increases. As seen, the grid-side current of inverter is stable only if the number of grid-connected inverter within the stability ranges shown in Figure 4b. Meanwhile, the number of inverter that can be connected to grid stable is decreased as the digital time delay of inverter increases, which are matched with the theoretical analysis results in Section 3.

Figures 8 and 10 show the grid-side current of inverter for five delay cases. It can be found that grid-side current of system will become unstable when the grid-connected inverter number is outside the stability ranges shown in Figures 5c and 6b.

Figure 8 shows the simulation waveforms of the grid-side current of inverter for Cases I and II, respectively. As seen, the stability ranges of grid-connected inverter number are decreased as the digital time delay of added inverter increases. On the contrary, when the digital time delay of inverter is smaller that of inverters in original LSCPV plant, the stability ranges of grid-connected inverter number will be extended. Meanwhile, the stability range of grid-connected inverter number is increased with the proportion of inverter with smaller delay in original system.

When the parameters of inverters are the same, N paralleled grid-connected inverter in system can be represented by a single inverter whose grid impedance is N times bigger [3]. Therefore, the theoretical analysis of stable grid-hosting capacity of LSCPV plant contains same digital time delay can be further verified by a single inverter experiment platform. Figure 9 shows the experimental waveforms of grid-side current of a 500 kW grid-connected inverter system, where the fundamental impedance 1 μH and $T_d = 0$ μs in Figure 7 is replaced by $T_d = 750$ μs (corresponding to $f_{sw} = 1$ kHz) since it cannot be reproduced in a practical digital control system. As seen, the stability range of grid-connected inverter number is decreased with the digital time delay of inverter, and the stability ranges are in line with the results obtained by the method discussed in Section 3.

The simulation waveforms of the grid-side current of inverter for Cases III, IV, and V are shown in Figure 10. It can be found that stability ranges of grid-connected inverter number become larger, when the original LSCPV has a larger proportion of inverters with smaller digital time delay. Meanwhile, when the grid-connected inverter numbers in original LSCPV plant are the same, the scenario of the added inverters has smaller digital time delay will allow the LSPV plant has a much larger stability ranges of grid-connected inverter numbers.

6 | CONCLUSION

The effects of digital time delay of inverter is introduced to the research of stable grid-hosting capacity of LSCPV plant in this paper. In addition to the widely used single-delay case, the multi-delay case corresponding to the complicated delay case of LSCPV plant is proposed to make the research more precise and comprehensive. The research results show that digital time delay of inverters has a negative effect on the stable grid-hosting capacity of LSCPV plants and the maximum marginal value of the stable grid-hosting capacity of LSCPV plant will be expanded with the addition of inverters with smaller digital time delay. Meanwhile, the degree of expansion is also increased as the number of grid-connected inverters in original LSCPV plant decreases or the digital time delay of inverters in original LSCPV plant increases. Moreover, the grid-connected LSCPV plant will have a greater expansible capacity when the

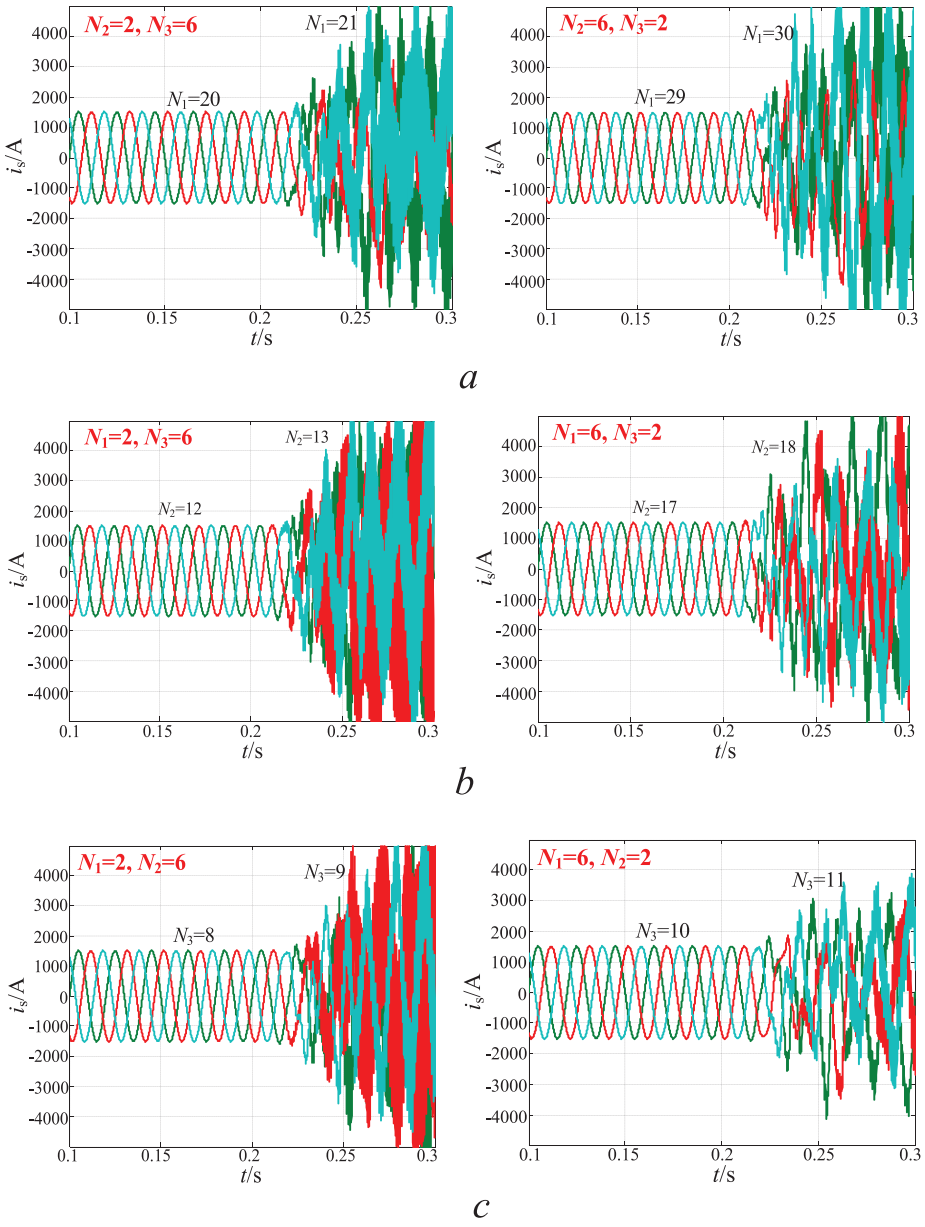

FIGURE 10 Simulation waveforms of i_s (a) Simulation waveforms of i_s for Case III (b) Simulation waveforms of i_s for Case IV (c) Simulation waveforms of i_s for Case V

inverters with smaller digital time delays have a larger share in LSCPV plant. The research about the stable grid-hosting capacity of LSCPV plant provides a solid reference for the practical determination of hosting capacity in the design and expansion phase of multi-inverter system, and for the selection of inverters with different digital time delays when the capacity of a multi-inverter system is determined, which is beneficial to the promotion of the economic efficiency of multi-inverter system. The theoretical analysis results presented in this paper were positively validated through simulation results on a high fidelity model of the LSCPV plant and experimental results on an equivalent experimental platform. It can also be used as a guideline for the research of grid-connected renewable energy systems.

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REFERENCES

1. Renewables 2020 global status report, REN21 Secretariat, Paris (2020)
2. Liu, J.H., et al.: Modeling and analysis of a digitally controlled grid-connected large-scale centralized PV system. IEEE Trans. Power Electron. 33(5), 4000–4014 (2018)
3. Agorreta, J.L., et al.: Modeling and control of *N*-paralleled inverters with *LCL* filter coupled due to grid impedance in PV plants. IEEE Trans. Power Electron. 26(3), 770–785 (2011)
4. Qin, C.W., Zhang, C.H., Chen, A., Circulating current suppression for parallel three-level inverters under unbalanced operating conditions. IEEE J. Emerg. Sel. Top. Power Electron. 7(1), 480–492 (2019)

5. Hong, L.C., et al.: Harmonic resonance investigation of a multi-inverter grid-connected system using resonance modal analysis. IEEE Trans. Power Deliv. 34(1), 63–72 (2019)
6. Yu, J.R., et al.: New perspectives on stability analysis of three-phase grid-connected inverter considering system coupling. IEEE Trans. Power Syst. 35(3), 1967–1978 (2020)
7. Zhou, L., Zhang, M., Modeling and stability of large-scale PV plants due to grid impedance. In: IECON 2013–39th Annual Conference of the IEEE Industrial Electronics Society, Vienna, Austria, pp. 1025–1030, (2013),
8. Wen, B., et al.: Impedance-based analysis of grid-synchronization stability for three-phase paralleled converters. IEEE Trans. Power Electron. 31(1), 26–38 (2016)
9. Hong, L.C., et al.: Harmonic resonance investigation of a multi-inverter grid-connected system using resonance modal analysis. IEEE Trans. Power Deliv. 34(1), 63–72 (2019)
10. Yu, C.Z., et al.: Modeling and resonance analysis of multiparallel inverters system under asynchronous carrier conditions. IEEE Trans. Power Electron. 32(4), 3192–3205 (2017)
11. Ketabi, A., Rajamand, S., Shahidehpour, M., Power sharing in parallel inverters with different types of loads. IET Gener. Transm. Distrib. 11(10), 2438–2447 (2017)
12. Zhang, Q.H., Xing, X.Y., Sun, K., Space vector modulation method for simultaneous common mode voltage and circulating current reduction in parallel three-level inverters. IEEE Trans. Power Electron. 34(4), 3053–3066 (2019)
13. Zhou, L.M., et al.: Harmonic voltage distortion damping method for parallel-connected LCL-type inverters in islanded operation. IEEE Trans. Ind. Electron. 66(11), 9032–9044 (2019)
14. Zou, C.Y., et al.: Influence of delay on system stability and delay optimization of grid-connected inverters with LCL filter. IEEE Trans. Ind. Inform. 10(3), 1775–1784 (2014)
15. Wang, J.G., et al.: Delay-dependent stability of single-loop controlled grid-connected inverters with LCL filters. IEEE Trans. Power Electron. 31(1), 743–757 (2016)
16. Tu, Y.M., et al.: Impedance-based analysis of digital control delay in grid-tied voltage source inverters. IEEE Trans. Power Electron. 35(11), 11666–11681 (2020)
17. Ashtiani, N.A., Azizi, S.M., Khajehoddin, S.A., Impedance-based analysis of digital control delay in grid-tied voltage source inverters. IEEE Trans. Control Syst. Technol. 27(6), 2361–2373 (2019)
18. Pan, D.H., et al.: Capacitor-current-feedback active damping with reduced computation delay for improving robustness of LCL-type grid-connected inverter. IEEE Trans. Power Electron. 29(7), 3414–3427 (2014)
19. Liu, J.H., Zhou, L., Marta, M., Damping region extension for digitally controlled LCL-type grid-connected inverter with capacitor-current feedback. IET Power Electron. 11(12), 1974–1982 (2018)
20. Zheng, L.J., Jiang, F.Y., Song, J.C., A discrete-time repetitive sliding mode control for voltage source inverters. IEEE J. Emerg. Sel. Top. Power Electron. 6(3), 1553–1566 (2018)
21. Yang, Y., Wen, H.Q., Li, D.P., A fast and fixed switching frequency model predictive control with delay compensation for three-phase inverters. IEEE Access. 5, 17904–17913 (2017)
22. Lin, Z.H., et al.: Multi resonant component-based grid-voltage-weighted feedforward scheme for grid-connected inverter to suppress the injected grid current harmonics under weak grid. IEEE Trans. Power Electron. 35(9), 9784–9793 (2020)
23. Zhu, K.L., et al.: Frequency-division virtual impedance shaping control method for grid-connected inverters in a weak and distorted grid. IEEE Trans. Power Electron. 35(8), 8116–8129 (2020)
24. Eduard, B.-M., Ricard, F.-D.-J., Mònica, A.-P., Power plant control in large-scale photovoltaic plants: Design implementation and validation in a 9.4 MW photovoltaic plant. IET Renew. Power Gener. 10(1), 50–62 (2016)
25. Nada, A.A., Mohamed, S.E.M., A novel centralized PV power plant controller for reducing the voltage unbalance factor at transmission level interconnection. IEEE Trans. Energy Convers. 32(1), 233–243 (2017)
26. Liu, Q.Y., et al.: Power quality management of PV plant with transformer integrated filtering method. IEEE Trans. Power Deliv. 34(3), 941–949 (2019)
27. Qin, C.W., et al.: Circulating current suppression for parallel three-level inverters under unbalanced operating conditions. IEEE J. Emerg. Sel. Top. Power Electron. 7(1), 480–492 (2019)
28. Meng, X., et al.: A universal controller under different operating states for parallel inverters with seamless transfer capability. IEEE Trans. Power Electron. 35(9), 9794–9812 (2020)
29. Farshad, Z., et al.: Adaptive complex virtual impedance control scheme for accurate reactive power sharing of inverter interfaced autonomous microgrids. IEEE Trans. Power Deliv. 12(22), 6021–6032 (2018)
30. Mi, Y., et al.: Reactive power sharing control for islanded AC microgrid based on fuzzy adaptive compensation method. IET Gener. Transm. Distrib. 14(4), 585–593 (2020)

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