Master's thesis

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Norwegian University of Science and Technology
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Reference generator for a sub-nW 9-bit 1kSample/s asynchronous SAR-ADC in 22nm UTBB FDSOI

Master's thesis in MTELSYS
Supervisor: Trond Ytterdal
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TFE4940 - Electronic Systems Design and Innovation, Master's Thesis

Reference generator for a sub-nW 9-bit 1kSample/s asynchronous SAR-ADC in 22nm UTBB FDSOI

By:
Isak Hannisdal

June, 2022

Abstract

This thesis presents the implementation and simulation results of a reference generator circuit for a sub-nW 9-bit 1kSample/s asynchronous SAR-ADC in 22nm UTBB FDSOI. The work in this thesis is a continuation of the work presented in the specialization project, where a sub-nW bandgap reference was designed and tested using the same design kit [1]. Two reference voltages of 0.2 V and 0.4 V are generated, and they inherit a temperature coefficient (TC) of 24.1 ppm/°C and 11.8 ppm/°C respectively, in nominal corner conditions during schematic simulations. The SAR-ADC achieves an Effective Number Of Bits (ENOB) of 8.91 bits when utilizing ideal voltage sources as reference voltages for the capacitive DACs. Simulations of the SAR-ADC with the reference generator implemented in this thesis achieve an ENOB of 8.73 bits in nominal corner conditions, including parasitic capacitances, extracted from a manually created layout. The design struggles in certain process corners as well as in mismatch simulations, resulting in a severe degradation in the ENOB at the output signal of the SAR-ADC. Output-referred noise at the reference generator outputs, integrated over an interval of 1 Hz to 20 kHz (two times the internal clock frequency of the SAR-ADC), is kept low at around 100 μV, in both reference voltages. The power supply rejection at the clock frequency is kept below -40 dB across process corners in layout simulations, in both reference voltages, however, the supply rejection at DC is only -20 dB in worst-case conditions, due to gain-degradation in the OTAs used in the output buffers. The total power consumption of the reference generator in nominal corner conditions is 241 nW (schematic simulations).

Sammendrag

Denne rapporten presenterer implementasjonen samt simuleringsresultater til en referansegenerator for en sub-nW 9-bit 1kSample/s asynkron SAR-ADC i 22nm UTBB FDSOI. Rapporten bygger på arbeidet i spesialiseringsprosjektet, hvor en sub-nW båndgapsreferanse ble designet og testet i den samme prosessteknologien [1]. To referansespenninger på 0.2 V og 0.4 V er generert, og de innehar en temperaturkoeffisient på henholdsvis 24.1 ppm/°C og 11.8 ppm/°C, hvor disse resultatene gjelder i det nominelle prosesshjørnet i skjemasimuleringer. SAR-ADC'en oppnår en *Effective Number Of Bits* (ENOB) på 8.91 bits, ved bruk av ideelle spenningskilder som referansespenninger til de kapasitive DAC'ene. Simuleringer av SAR-ADC'en i kombinasjon med referansegeneratoren som er implementert i denne rapporten, viser en ENOB på 8.73 bits i det nominelle prosesshjørnet, hvor utleggsparasitter, ekstrahert fra et manuelt opprettet utlegg er inkludert. Designet sliter i visse prosesshjørner, så vel som i mismatch simuleringer, noe som resulterer i en alvorlig degradering i ENOB på utgangssignalet til SAR-ADC'en. Utgangsreferert støy på utgangene til referansegeneratoren, integrert over et område fra 1 Hz til 20 kHz (to ganger den interne klokkefrekvensen til SAR-ADC'en), holdes lavt til rundt 100 μV i begge referansespenningene. Attenueringen av variasjoner i forsyningsspenningene ved klokkefrekvensen på 20 kHz (målt i PSRR), holdes lavt til under -40 dB over alle prosesshjørnene i utleggssimuleringer, men denne attenueringen er kun -20 dB ved DC i verste tilfelle. Dette er på grunn av degradering i forsterkningen i forsterkerne som blir anvendt i utgangsbufferne. Det totale effektforbruket til referansegeneratoren er 241 nW i det nominelle prosesshjørnet (skjemasimuleringer).

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Chapter 1

Introduction

Energy efficiency is a major concern in the design of integrated analog circuits and has become even more relevant in recent years, where keywords such as *green* and *sustainable* can be frequently observed in both daily life and research papers concerning integrated circuit design. The quest for low power and high-resolution Analog-To-Digital Converters (ADCs) introduces difficult and interesting design challenges, however, some aspects of the design are often neglected in scientific publications, namely the generation of stable and accurate reference voltages. Research papers about ultra-low-power ADCs do seldom mention the power consumption needed to generate the required reference voltages. Often these publications use the supply voltage as the main reference voltage. This is a problem in many applications where the noise at the supply voltage is too high to achieve a good enough resolution at the output of the ADC. In order to develop a realistic model of the total power consumption of an ultra low power ADC, the generation of reference voltages should be of major concern. This thesis presents the implementation and simulation results of a reference generator for a sub-nW 9-bit 1 kSample/s asynchronous SAR-ADC in 22nm UTBB FDSOI. The SAR-ADC is designed as the master project of a fellow student, where further information can be found in [2].

A reference generator delivers accurate, process-independent, voltages and currents that are needed in several aspects of modern VLSIC design. Extreme operating conditions including large variations in both temperature and supply voltages are some of the challenges to overcome, especially in industrial applications. The work in this thesis is a continuation of the work presented in the specialization project with subject code TFE4580, where a sub-nW bandgap reference is designed and tested utilizing the same design kit [1].

1.1 Thesis outline

The thesis is organized as follows:

Chapter 2 - SAR-ADC overview General concepts including the operation of a SAR-ADC and performance metrics e.g. ENOB are presented and discussed. This chapter also presents nonlinear mechanisms in SAR-ADCs that affects the design and performance of reference generators.

Chapter 3 - Reference generator overview Here, the general concepts regarding reference generation are presented, including a description of the different circuit blocks including; bandgap reference circuit, constant-transconductance circuit, and operational transconductance amplifier (OTA). Different key performance metrics of these types of circuits are also introduced.

Chapter 4 - Implementation of the reference generator An extensive description of the reference generator is presented, where several key design choices are examined.

Chapter 5 - Results and discussions Results, including data from several corner simulations and Monte Carlo runs, are presented and discussed.

Chapter 6 - Conclusion and future work The thesis is concluded and future work is commented.

Chapter 2

SAR-ADC overview

This chapter presents an overview of the SAR-ADC used in this thesis and describes the specific switching scheme in the capacitive DACs, as it affects the requirements of the reference generator. The chapter also discusses how the reference generator can cause nonlinear effects at the output of the ADC and defines ENOB as the most essential performance metric for measuring this non-linearity.

2.1 SAR-ADC

The Successive-Approximation Register Analog-to-Digital Converter (SAR-ADC) is a popular approach for converting analog signals to the digital domain. A known reference voltage is compared with the analog input signal in an algorithm that resembles binary search. The SAR-ADC used in this thesis has a 10-bit topology, however, it only attains a 9-bit resolution (ENOB). A thorough explanation of the SAR-ADC used in this thesis can be found in [2], however, this particular ADC topology utilizes a noteworthy switching scheme during the charge-redistribution phase, based on the work found in [3]. This affects the design choices in the implementation of the reference generator and is therefore further elaborated in the following sub-chapter.

2.1.1 Common Mode-based Charge Recovery

To allow for a sub-nW SAR-ADC a common mode-based monotonic charge recovery (CMMC) technique is utilized in the capacitive DACs in the ADC. This technique introduces an extra voltage reference $\mathbf{V_{CM}}$ to reduce the switching power compared to conventional switching schemes, as well as reduce the total amount of unit capacitors from 2^n to $2^{(n-1)}$ for an n-bit ADC [3]. The SAR-ADC used in this thesis, found in [2], utilizes a fully differential implementation of the topology found in [3]. This ensures a much greater common-mode noise rejection as well as a suppression of substrate and supply noise. A 3-bit example of the CMMC switching technique

is illustrated in Fig. 2.1.

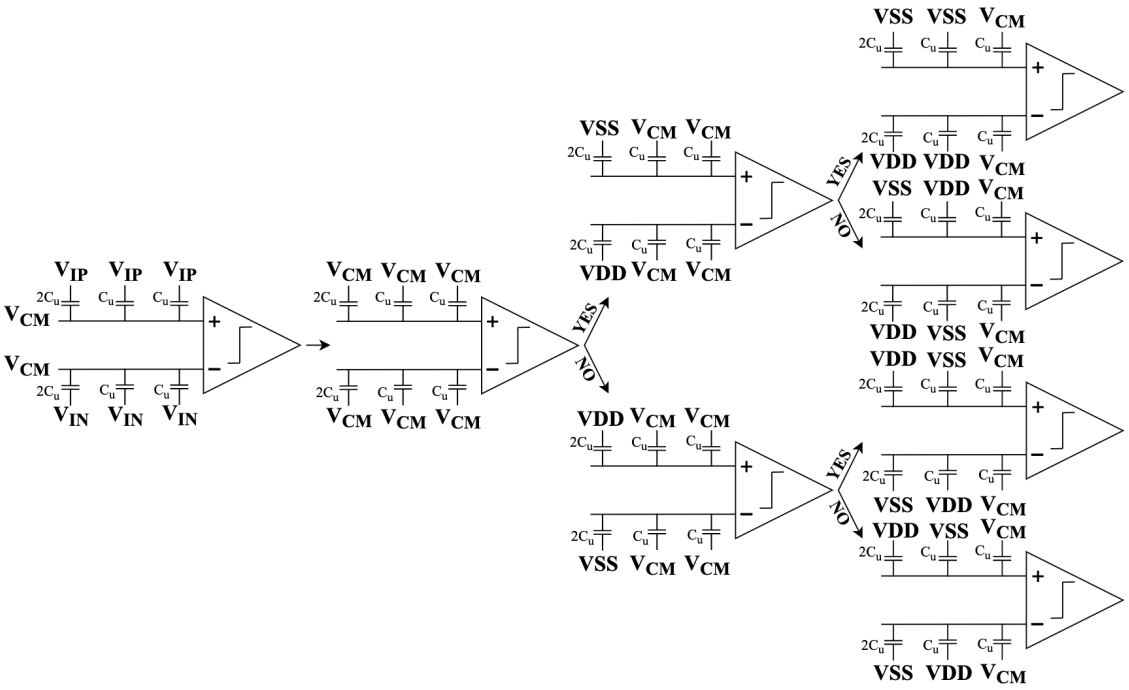


Figure 2.1: 3-bit example of the CMMC switching technique [2].

During the first step the input signal $\mathbf{V_{IP}}$ and $\mathbf{V_{IN}}$ are sampled while the common-mode voltage $\mathbf{V_{CM}}$ is connected to the bottom plate of the capacitors. This allows the most significant bit (MSB) to be determined without consuming any energy from the CDAC and as mentioned above, reduces the total amount of unit capacitors from 2^n to $2^{(n-1)}$ for the n-bit ADC. During the next step the largest capacitor is charged from $\mathbf{V_{CM}}$ to **VDD** or discharged from $\mathbf{V_{CM}}$ to **VSS** depending on the previous step. The CMMC technique halves the maximum voltage difference over the capacitors compared to traditional switching schemes, reducing the required current drawn from the reference generator, however, introduces a common-mode voltage $\mathbf{V_{CM}}$, which in this differential implementation is loaded with a maximum of $2(2^{(n-1)})$ unit capacitors. The implications of this switching technique are further investigated in Ch. 3.1, where expressions for maximum reference current and reference load capacitance are presented.

2.2 ENOB

ENOB is an abbreviation referring to the Effective Number of Bits and is used as one of the main performance metrics when describing the dynamic range of an ADC. The most common relationship for describing ENOB is given by Eq. 2.1 [4],

$$ENOB = \frac{SINAD_{DB} - 1.76}{6.02} \tag{2.1}$$

where SINAD is the signal-to-noise and distortion ratio, given by Eq. 2.2 [4].

$$SINAD = \frac{P_{signal}}{\sum P_{Harmonics} + \sum P_{Noise}} \tag{2.2}$$

The numbers 1.76 and 6.02 in Eq. 2.1, come from the famous theoretical signal-to-quantization noise model that assumes a sinusoidal input signal. The degradation in the ENOB is used as the main performance metric when analyzing how the reference generator design affects the SAR-ADC later in this thesis. Some usual causes of such degradations are discussed in the following sub-chapter.

2.3 Non-linearities

The discussions about non-linearities are based on the chapter concerning charge-redistribution SAR-DACs in [5]. One of the main limitations of the charge redistribution DAC used in the SAR-ADC is the accuracy of the reference voltages. During the SAR phase of the ADC, the reference voltages are connected to the comparator inputs through switches and capacitors. The transfer function from the input of the comparator to the reference voltage is not linearly code-dependent. This can cause errors in the conversions and produce distortion at the output of the ADC if the ripples on the reference voltage during the SAR phase are greater than 1 LSB.

Another effect that is not linearly code-dependent is the absorbed charge at the output of the reference generator. Due to the finite impedance of the reference generator and the switching of the DAC capacitors, a low-frequency code-dependant voltage ripple is produced. In differential topologies, this produces a considerable spectral component at the second harmonic of the ADC input signal, resulting in a large third harmonic at the output of the ADC.

These non-linearities make reference generator design for high-resolution SAR-ADCs particularly difficult, however, there exist two main techniques for mitigating these effects. In order to deal with the non-linear transfer function between the input of the comparator and the reference generator, large decoupling capacitors at the reference generator outputs are usually required. This will remove some of the high-frequency ripples at these nodes. The second non-linear effect can be attenuated by designing the reference generator in such a way that its peak output impedance is low. This will in turn lessen the low-frequency voltage ripple caused by the absorbed charge in the reference generator, resulting in an attenuation of the third harmonic in the output of the ADC.

Chapter 3

Reference Generator Overview

This chapter presents the main building blocks of the reference generator as well as some key design equations in order to achieve the desired resolution at the output of the ADC. It also presents the main performance metrics for the reference generator, as well as discusses some of the main limitations in the design. Background theory describing the FDSOI technology, as well as concepts such as body-biasing can be found in [1].

3.1 Design Equations

The SAR-ADC utilizes a supply voltage **VDD** of 0.4 V, a common-mode voltage $\mathbf{V_{CM}}$ of 0.2 V and ground **VSS** (0 V), in order to implement the CMMC technique illustrated in Fig. 2.1. The reference generator therefore needs to deliver two voltages of 0.4 V and 0.2 V, hereby called $VREFP$ and $VREFCM$ respectively. In order to calculate the required decoupling capacitances at these nodes to avoid the non-linear effects discussed in Ch. 2.3, one can construct simple equations based on the worst-case switching in the SAR-ADC's capacitive DACs. The equations are based on the work found in [4].

The maximum charge supplied by the reference voltages can be expressed by Eq. 3.1,

$$Q_{max} = \sum C_{LOAD} \cdot \Delta V_{max} \tag{3.1}$$

where $\sum C_{LOAD}$ is the sum of the total load capacitance seen by the reference voltages and ΔV_{max} the maximum voltage difference over the given load capacitance. In order to avoid conversion errors in ADC, the maximum instantaneous voltage error $V_{error_{max}}$ should be kept below LSB/2. This gives the following expression for an arbitrary reference decoupling capacitor C_{REF}:

$$C_{REF} = \frac{Q_{max}}{V_{error_{max}}} = \frac{Q_{max}}{\frac{LSB}{2}} \tag{3.2}$$

where Q_{max} is the maximum charge supplied by the reference voltage from Eq. 3.1, and the Least Significant Bit (LSB) = $V_{REF}/2^N$.

To calculate the specific decoupling capacitance for the reference voltages $VREFP$ and $VREFCM$ based on Eq. 3.2, one can assume a unit capacitance of C_u in the capacitive DACs and a resolution of 9-bit [2]. This gives the following expressions for the two reference decoupling capacitors:

$$C_{VREFP} = \frac{\sum C_{LOAD_{VREFP}} \cdot (VREFP - VREFCM)}{\frac{LSB}{2}} = \frac{256 \cdot C_u \cdot 0.2\ V}{(\frac{0.4V}{2^9})/2} \tag{3.3}$$

$$C_{VREFCM} = \frac{\sum C_{LOAD_{VREFCM}} \cdot |VREFCM - V_{IN}|_{max}}{\frac{LSB}{2}} = \frac{2 \cdot 512 \cdot C_u \cdot 0.2\ V}{(\frac{0.4V}{2^9})/2} \tag{3.4}$$

where the maximum load capacitance seen by the reference $VREFP$ and $VREFCM$ is $256C_u$ and $2(512)C_u$ respectively. As mentioned in Ch. 2.1, the SAR-ADC is implemented with a 10-bit topology, however, the resolution is only 9-bits. Therefore the maximum load capacitances used in Eq. 3.3 and Eq. 3.4 are based on a 10-bit resolution, and not 9-bits as for the LSB. The maximum voltage difference at the reference nodes is the same (0.2V), where the reference $VREFP$ experiences a maximum change of voltage as the difference between $VREFP$ and $VREFCM$. The other reference voltage experiences a maximum voltage change based on the input signal, which has its extremal points at 0.4V and 0V. This makes the common-mode reference voltage $VREFCM$ more affected by the input signal as well as having the same maximum voltage change as the other reference voltage $VREFP$.

One can observe that the large load capacitance seen by the reference voltage $VREFCM$, makes the decouple capacitance at this node C_{VREFCM} four times as large as C_{VREFP}, in order to achieve a 9-bit resolution. A closer look at the equations also reveals that these decouple capacitors become very large and requires a lot of area, even if the unit capacitors in the SAR-ADC DAC are minimized. This is one of the major limitations with high-resolution SAR-ADCs, and for resolutions over 9/10-bit ENOB, the decoupling capacitors in the reference generators become the most area dominant part in ADC designs [5].

In order to calculate the required output current of the references as well as the necessary unity gain frequencies of the buffer amplifiers in the design, certain assumptions need to be made. The following models are based on the work found in [6], where design equations regarding reference voltage buffer design for a SAR-ADC are presented. The SAR-ADC has a sample rate of 1kSample/s and operates with an internal clock frequency of 10 kHz, which gives a period T = 100 μs. Assuming that 50 % of the period is utilized for comparator evaluation and that 10 % of the

period is used for the delay in the digital logic, 40 μs is available for DAC-settling. However when accounting for layout parasitics and other interconnect effects a more robust settling time requirement of 35 μs can be exercised for the reference voltages. The models in [6] allocate 10 % of the total available settling time for slewing and 90 % for linear settling, however, mentions that it is problematic to accurately distinguish between these two regions. With these assumptions one can calculate the required output current, using Eq. 3.5.

$$\frac{\Delta V_{max}}{t_{slew}} = \frac{I_{out}}{C_{Lmax}} \tag{3.5}$$

Solving this equation for the current I_{out} leads to the following expression for the output current in the $VREFP$ reference:

$$I_{VREFP} = \sum C_{LOAD_{VREFP}} \frac{\Delta V_{max}}{t_{slew}} = 256 \cdot C_u \cdot \frac{0.2\ V}{0.1 \cdot 35\ \mu s} \tag{3.6}$$

where $\sum C_{LOAD_{VREFP}}$ and ΔV_{max} are the same as in Eq. 3.3. Similarly for the other reference $VREFCM$:

$$I_{VREFCM} = \sum C_{LOAD_{VREFCM}} \frac{\Delta V_{max}}{t_{slew}} = 2 \cdot 512 \cdot C_u \cdot \frac{0.2\ V}{0.1 \cdot 35\ \mu s} \tag{3.7}$$

where $\sum C_{LOAD_{VREFCM}}$ and ΔV_{max} are the same as in Eq. 3.4. It is important to note that Eq. 3.6 and Eq. 3.7 represent the worst-case settling at their respective output nodes, and are based on several assumptions. However, the model serves as a good design origin, as a lack of good mathematical models for reference generators concerning SAR-ADCs are observed in literature.

When calculating the necessary unity gain frequencies of the output buffer amplifiers in the design, one can simplify the models by assuming single-pole amplifiers. The step response of such a system is given by Eq. 3.8

$$V_{out}(t) = V_{step}(1 - e^{\frac{-t}{\tau}}) \tag{3.8}$$

where τ is given by Eq. 3.9.

$$\tau = \frac{1}{\beta \cdot \omega_{ug}} \tag{3.9}$$

Here, β represents the feedback factor, which in a unity gain feedback system equals 1, and the unity gain frequency is represented with the symbol ω_{ug}. Defining the settling error $\epsilon = e^{\frac{t}{\tau}}$ and taking the logarithm on both sides of this expression, lead to the following equation for the settling error:

$$\ln(\epsilon) = \frac{-t}{\tau} = -t \cdot \omega_{ug} \tag{3.10}$$

solving Eq. 3.10 for ω_{ug}, which equals $2\pi f_{ug}$, one can express the minimum unity gain frequency by Eq. 3.11,

$$f_{ug} = \frac{-\ln(\epsilon)}{2\pi \cdot t} \tag{3.11}$$

where t equals the time allocated for linear settling. Solving the equation using one extra bit for redundancy (10-bit instead of 9-bit), gives the following value for the minimum unity gain frequency:

$$f_{ug} = \frac{-\ln \frac{1}{2^{10}}}{2\pi \cdot 0.9 \cdot 35\ \mu s} = 35\ kHz \tag{3.12}$$

the relatively slow internal clock frequency of 10 kHz in the SAR-ADC allows for slow amplifiers in the output buffers of the reference generator. The implications of this are further discussed in Ch. 3.3, concerning the design of the OTAs in the reference generator design.

3.2 Bandgap Reference

A bandgap reference is a circuit that produces a temperature-independent reference voltage. This voltage is derived from the bandgap voltage in intrinsic silicon, hence this reference voltage is referred to as the bandgap reference. The bandgap reference used in this thesis is the same as the circuit presented in [1], where a detailed description of the concepts regarding temperature-independent voltage generation can be found. It utilizes a novel topology combining BJT-based and MOS-threshold-based design, without the need for a high-gain OTA.

3.3 Symmetrical OTA

An example of a symmetrical (or current mirror) OTA is illustrated in Fig. 3.1. This OTA features a PMOS input stage as well as cascoded transistors in order to increase the output impedance and therefore the gain of the amplifier.

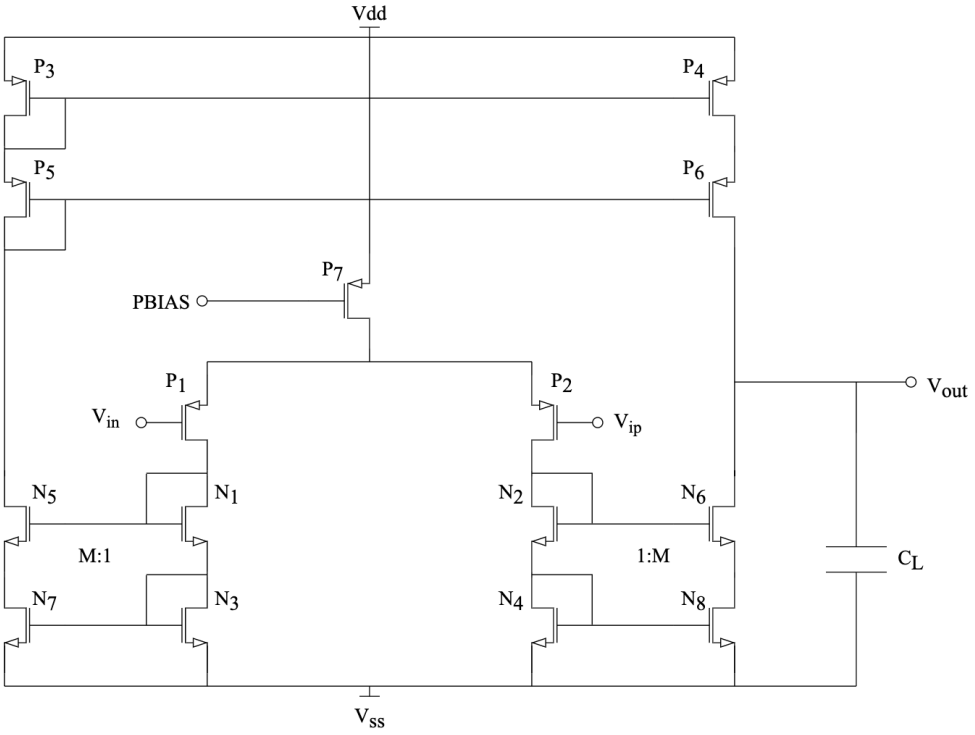


Figure 3.1: Symmetrical OTA with cascoded transistors and PMOS input stage

The chapter on current mirror opamps in [7], provides the following expression when describing the gain of such an amplifier:

$$A_V = \frac{V_{out}(s)}{V_{in}(s)} = Mg_{m1}Z_L(s) = \frac{Mg_{m1}r_{out}}{1 + sr_{out}C_L} = \frac{Mg_{m1}}{sC_L} \tag{3.13}$$

where M is the multiplication factor between the input and output transistors illustrated in Fig. 3.1. Eq. 3.13 ignores the high-frequency poles and zeroes and approximates the system in dominant pole operation. The output impedance of such an amplifier can be quite high when cascoded transistors are used and is in the order of $g_m r_{ds}^2$ /2 (from the chapter regarding folded-cascode opamps in [7]). The current gain factor can be increased in order to increase the gain of the OTA further, however, this will increase the impedance of internal nodes, and the impact of other poles makes it difficult to maintain stability.

These types of OTAs are favorable in a reference biasing design because they present less systematic offset compared to other OTA topologies, given that both of the input transistors see the same load, a diode-connected transistor [8].

A PMOS input stage is favorable as it provides a larger unity gain frequency and lower flicker noise [7], however, it is important to note that this is technology dependant and that wideband thermal noise can be improved by choosing an NMOS input stage. The Symmetrical OTA in Fig. 3.1 is biased by a PMOS current source P_7, where the gate voltage of this device $PBIAS$, determines the current in the OTA. How the $PBIAS$ reference is created, is covered in the following sub-chapter.

3.4 Constant-transconductance circuits

A constant-transconductance circuit produces a process-, temperature- and supply-independent small-signal transconductance referenced to a resistor value. An example of a constant transconductance circuit is illustrated in 3.2.

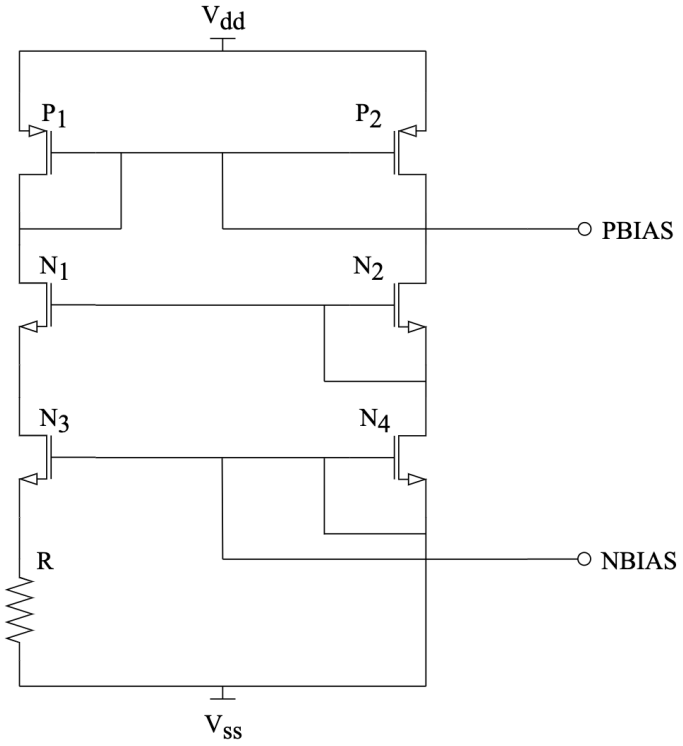


Figure 3.2: Constant-transconductance bias circuit.

As mentioned in the previous sub-chapter, these circuits can be used to provide bias currents for OTAs. These currents will inherit a PTAT relation and only have a weak dependence on variations in the power supply. In order to accurately describe how the constant transconductance is attained, some mathematical models are needed. These models are based on the chapter about establishing constant transconductance in [7].

First, one assumes that the current in the two branches is equal, namely that $(W/L)_{P1} = (W/L)_{P2}$. Then one can describe the gate-to-source voltage of the transistor N_4 by Eq. 3.14.

$$V_{GS_{N4}} = V_{GS_{N3}} + I_{D_{N3}} R \tag{3.14}$$

Substituting the gate-to-source voltages with $V_{eff} + V_T$, the threshold voltages V_T cancels and one ends up with Eq. 3.15.

$$V_{eff_{N4}} = V_{eff_{N3}} + I_{D_{N3}} R \tag{3.15}$$

Recalling that $I_{D_{N4}} = I_{D_{N3}}$, one can rewrite the expression in Eq. 3.15 as:

$$\sqrt{\frac{2I_{D_{N4}}}{\mu_n C_{ox}(W/L)_{N4}}} = \sqrt{\frac{2I_{D_{N4}}}{\mu_n C_{ox}(W/L)_{N3}}} + I_{D_{N4}}R \tag{3.16}$$

when rearranging Eq. 3.16, one can obtain the following expression for the resistance R:

$$R = \frac{2}{\sqrt{2\mu_n C_{ox}(W/L)_{N4}}}(1 - \sqrt{\frac{(W/L)_{N4}}{(W/L)_{N3}}}) \tag{3.17}$$

Eq. 3.17 can be simplified as $g_{m_{N4}} = \sqrt{2\mu_n C_{ox}(W/L)_{N4}}$, and the transcontuctance of $N4$ can now be expressed by Eq. 3.18.

$$g_{m_{N4}} = \frac{2(1 - \sqrt{\frac{(W/L)_{N4}}{(W/L)_{N3}}})}{R} \tag{3.18}$$

Here, it is made obvious that the transconductance only depends on the geometric ratios of the transistors and the resistance R. If the transistors in Eq. 3.18 have the same (W/L) and a multiplication factor of 4 is used for the transistor N_3, one ends up with Eq. 3.19.

$$g_{m_{N4}} = \frac{1}{R} \tag{3.19}$$

Since all currents are derived from the same bias network, all of the transconductances in the circuit in Fig. 3.2 are stabilized. It is important to note that the transconductance of the PMOS transistors will depend on $\sqrt{\mu_p/\mu_n}$ and that this can lead to large variations from chip to chip. As mentioned above, this circuit can be used as a PTAT current source to bias different circuits where power supply variation is a concern. The current is proportional to the threshold voltage V_T, which is the reason for the PTAT relation.

3.5 Performance Metrics and Limitations

A good reference generator provides temperature, mismatch, and process independent reference voltages and currents. As mentioned in Ch. 2.2, the main performance metric for evaluating how the reference generator design affects the sub-nW SAR-ADC is the ENOB at the output of the ADC. In order to thoroughly evaluate the performance of the reference generator, one can also utilize other commonly used performance metrics. In literature, a temperature dependence is often expressed in terms of the Temperature Coefficient (TC). This performance metric has the unit of ppm/°C and can be expressed by Eq. 3.20.

$$TC = \frac{V_{max} - V_{min}}{V_{nominal}(T_{max} - T_{min})} \cdot 10^6 \tag{3.20}$$

It is important to note that the TC does not include any DC-offset, meaning that a reference voltage generator can provide excellent results regarding temperature dependence across process corners, however with a large offset between the nominal voltages $V_{nominal}$ in the different corners. This voltage is often set to the room temperature, in this thesis at 27 °C. A temperature range from -40 to 125 °C is often utilized, as this is the standard industrial temperature range.

Another key performance metric of the reference generator is the capability to withstand variations in the supply voltages, often referred to as the power supply rejection of the circuit. This is measured in dB and referred to as the Power Supply Rejection Ratio (PSRR). The PSRR at DC is in this reference generator design determined by the gain of the OTAs in the output buffers in Fig. 4.3. The PSRR degrades at higher frequencies where the gain of the OTAs starts to decrease [9], however when using large decouple capacitors at the outputs, this degradation does not cause a problem, as the high-frequency components are shorted by the large load capacitances.

Total noise power at the output reference voltages affects the performance of the SAR-ADC and is therefore of interest. It is important that the noise at the reference voltages, containing both thermal and flicker noise components, is kept below the ADC noise. A noise budget containing the maximum allowed noise integrated over the band of interest is needed to optimize the noise performance of the reference generator. The noise in the SAR-ADC is dominated by kT/C-noise where the unit capacitance C_u determines a trade-off between the total noise power and the area of the ADC.

The total power consumption of the reference generator system is limited by the required output current at the reference voltage nodes. Therefore the power efficiency of the system needs to be evaluated based on the amount of extra power used in the rest of the circuits. Ideally, all of the current drawn from the supplies should be exploited in the output stage, however, some current is needed to obtain a stable bandgap reference, high gain OTAs and constant-transconductance bias circuits. Another key aspect of the current drawn by the output stage is the trade-off between output impedance and power consumption. As mentioned in Ch. 2.3, the output impedance of the reference generator should be minimized to avoid non-linear effects. This can be achieved by increasing the current in the output stage, however, this will lead to a large increase in the total power consumption, as most of the current in the reference generator is utilized by the output stage.

Chapter 4

Implementation of The Reference Generator System

This chapter covers the implementation of the reference generator system. A block diagram of the entire system is illustrated in Fig. 4.1, where bias circuits and the bandgap reference [1] from are included.

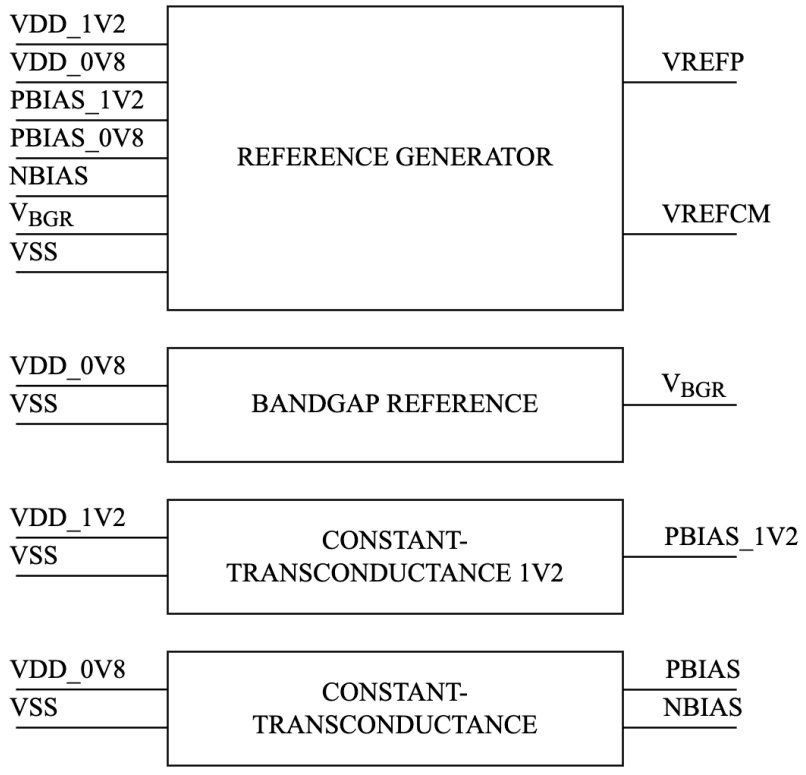


Figure 4.1: Block diagram of the entire reference generator system including bias circuits.

The entire system is designed and simulated in the *Cadence Virtuoso Environment*,

utilizing a commercially available 22nm FDSOI process. Supply voltages in this technology can be increased from the nominal supply voltage of 0.8V with the use of thick-oxide devices (IO-transistors). Due to the minimum V_{DS} of certain devices in the design, two different supply voltages of 1.2V and 0.8V are used. The following sub-chapters explain the implementation of the different circuit blocks in Fig. 4.1 and detailed schematics including device sizes can be found in appendix A.

4.1 Reference Generator

The implementation of the reference generator is based on the work presented in [4], and the schematic of the circuit is illustrated in Fig. 4.2.

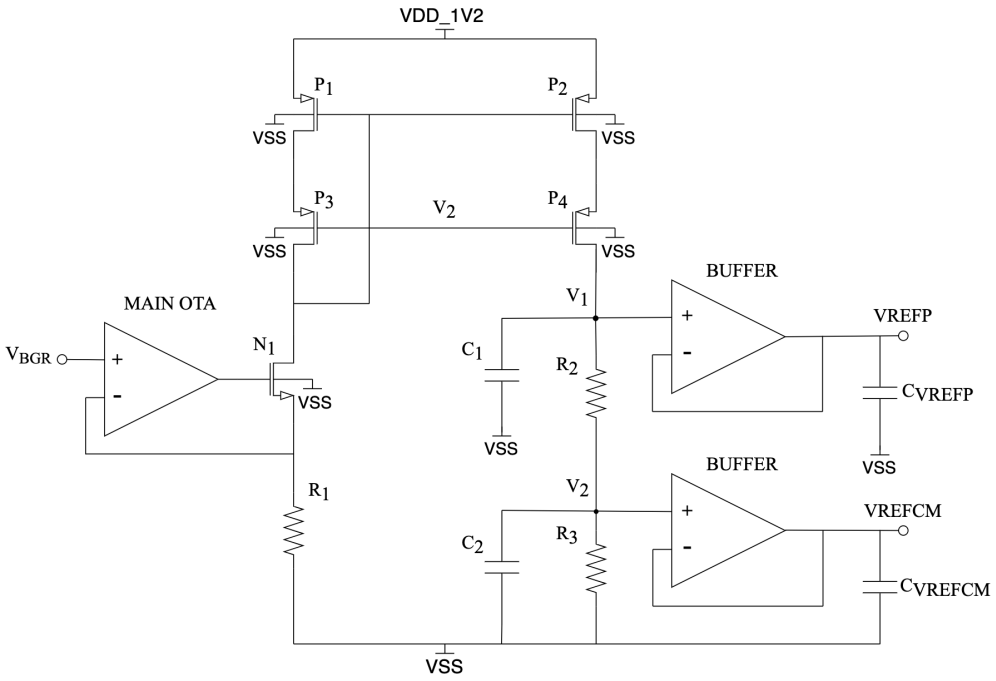


Figure 4.2: Schematic of the reference generator.

The bandgap voltage V_{BGR} is used to generate two reference output voltages; $VREFP$ and $VREFCM$. The values of these voltages are 0.4V and 0.2V respectively. The bandgap voltage V_{BGR}, $MAIN\ OTA$ and the resistor R_1 are used to generate a current $I_{D_{N_1}}$, proportional to the resistance of R_1. If the gain of the $MAIN\ OTA$ is high, the voltage drop across the resistor R_1 equals the bandgap voltage V_{BGR} due to the feedback loop, and the drain current of the transistor N_1 can be expressed by Eq. 4.1.

$$I_{D_{N_1}} = \frac{V_{BGR}}{R_1} \tag{4.1}$$

This current is then mirrored by the high-swing current mirror consisting of the transistors P_1-P_4 (flipped-well devices). The output from the current mirror flows

into a resistor string which consists of the resistors R_2 and R_3. This converts the reference current into reference voltages at the nodes V_1 and V_2. The voltages at these nodes can be expressed by Eq. 4.2 and Eq. 4.3.

$$V_1 = \frac{I_{D_{N_1}}}{R_2 + R_3} = V_{BGR}\frac{R_1}{R_2 + R_3} \tag{4.2}$$

$$V_2 = \frac{I_{D_{N_1}}}{R_3} = V_{BGR}\frac{R_1}{R_3} \tag{4.3}$$

From these equations, one can observe that the voltages depend on the ratio of the resistors, such that variations in the resistance values cancel out, given that the resistors match well. Another advantage of this implementation is that almost any reference voltage can be created by scaling the resistors R_2 and R_3. Bypass capacitors C_1 and C_2 are added to reduce the voltage variation at these nodes, improving the power supply rejection at the output.

In order to optimize the power efficiency, one would ideally operate the circuit with a supply voltage of 0.8 V, allowing a drain-to-source voltage of 0.2 V over each transistor, however, the bandgap reference in this design delivers a fractional bandgap voltage $V_{BGR} = 566$ mV. In order to maintain the desired operating region of the transistors, the supply voltage is increased to 1.2 V, and thick-oxide devices are therefore used. A further increase in the supply voltage would be necessary in the original topology from [4], however, this implementation utilizes a high-swing current mirror in order to minimize power consumption and keep the circuit operative at a more common supply voltage of 1.2 V.

The voltages at V_1 and V_2 are buffered in order to supply the currents drawn from the $VREFP$ and $VREFCM$ references. A schematic of the buffers is illustrated in Fig. 4.3, and the circuit is operated at a supply voltage of 0.8 V.

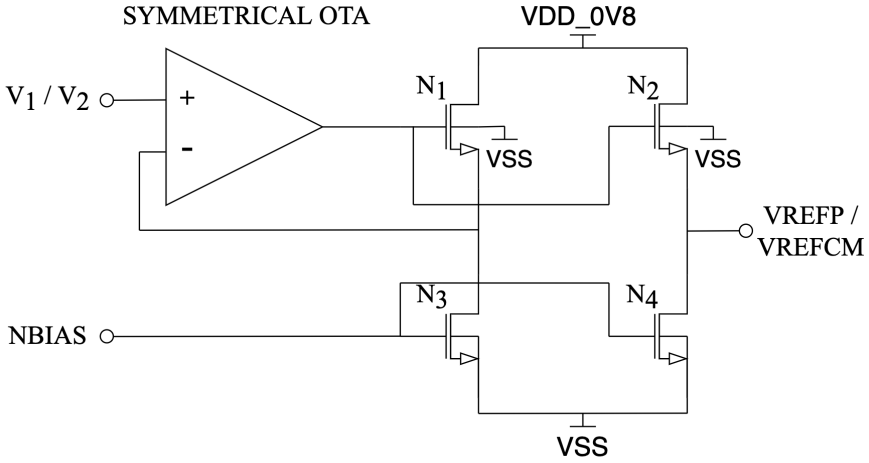


Figure 4.3: Reference generator buffer circuit.

The symmetrical OTA in the buffer is used in a similar way as the $MAIN\ OTA$

in Fig. 4.2 to set the voltage at the source of N_1 equal to the input signal V_1/V_2. High gain in the symmetrical OTA is needed to equate these voltages, as well as to maintain a good Power Supply Rejection (PSR) at DC in the output voltage reference. If good matching between the transistors N_1 and N_2, and N_3 and N_4 is obtained, the source voltage of N_2 ($VREFP/VREFCM$) equals the source voltage of N_1 (V_1/V_2). This technique of copying the reference voltage to another current branch isolates the buffer OTA from the large load capacitance at the output node, which can cause instability. Another advantage of this implementation is that the transistors in the output branch N_2 and N_4, can be scaled up to obtain low output impedance, needed to reduce the non-linear effects discussed in Ch. 2.3.

Both the $MAIN\ OTA$ and the amplifiers in the output buffers are implemented as cascoded symmetrical OTAs. This amplifier topology is used because of the reduced systematic offset at the input compared to other topologies, as well as the high gain that such an amplifier can achieve, as described in Ch. 3.3. The bandwidth constraints given by Eq. 3.12, make it possible to bias the OTAs with very little current. This is because the bandwidth of the amplifiers is proportional to the branch current in the OTAs, resulting in lower total power consumption. All of the OTAs are implemented as in Fig. 3.1 with a PMOS input stage because of the advantages mentioned in the same chapter, as well as constraints on the common-mode input signal. The $MAIN\ OTA$ is driven by a supply voltage of 1.2 V and the buffer amplifiers are operated at a 0.8 V supply. A current gain multiplication factor $M = 1$ is used for the $MAIN\ OTA$ to maintain stability and low current consumption, and a multiplication factor of 4 is used for the OTAs in the output buffers to provide enough gain and bandwidth to achieve accurate output reference voltages. The implementation utilizes the g_m/I_D design methodology described in [10] and targets a gain >60 dB.

The unit capacitance $C_u = 3$ fF in the sub-nW SAR-ADC[3]. Using Eq. 3.6 and Eq. 3.7, the theoretically required output currents can be calculated.

$$I_{VREFP} = 256 \cdot 3fF \cdot \frac{0.2V}{0.1 \cdot 35\mu s} = 43.9nA \tag{4.4}$$

$$I_{VREFCM} = 2 \cdot 512 \cdot 3fF \cdot \frac{0.2V}{0.1 \cdot 35\mu s} = 176nA \tag{4.5}$$

In order to minimize the total current consumption of the reference generator, large multiplication factors in the output branch are desirable. However, if the gate area of the transistors N_1 and N_3 in Fig 4.3 is too low, flicker noise in these devices will dominate, resulting in large output-referred noise in the reference voltages. The implemented circuit utilizes high-threshold devices for the transistors N_1-N_4. This allows for a small gate length, reducing the output impedance while retaining low power consumption. Another advantage is that large aspect ratios can be used, maximizing the transconductance g_m of these devices, and therefore further lowering the output impedance, which is inversely proportional to g_m.

The decoupling capacitors at the outputs of the reference generator can be calculated using Eq. 3.3 and Eq. 3.4.

$$C_{VREFP} = \frac{256 \cdot 3fF \cdot 0.2V}{(\frac{0.4V}{2^9})/2} = 393pF \tag{4.6}$$

$$C_{VREFCM} = \frac{2 \cdot 512 \cdot 3fF \cdot 0.2V}{(\frac{0.4V}{2^9})/2} = 1.57nF \tag{4.7}$$

The capacitance values in Eq. 4.6 and Eq. 4.7 are considerable, as mentioned in Ch. 3.1, the decoupling capacitors become the main area contributor for high-resolution SAR-ADCs. However, due to the low sample frequency of the sub-nW SAR-ADC, these capacitors can be placed off-chip. This is not a viable option for high-frequency ADCs, as the effective inductance in the bond wires will resonate with these capacitors [11].

4.2 Bandgap Reference

The implementation of the bandgap reference is based on the work presented in the specialization project [1], and the schematic of the bandgap reference is illustrated in Fig. 4.4.

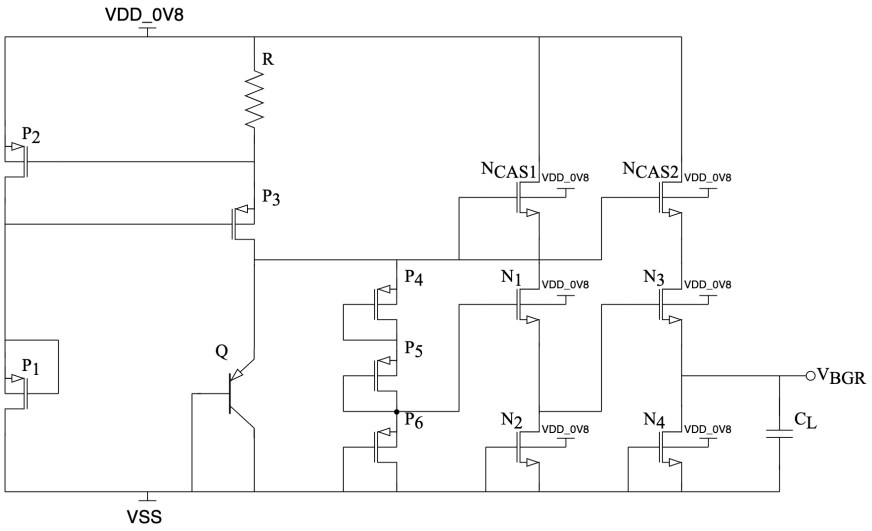


Figure 4.4: Schematic of the bandgap reference [1].

The main goal in the original bandgap reference design was to achieve sub-nW operation, however, this lead to a degradation in the temperature coefficient at the output. The bandgap reference used in this thesis is modified to improve the process corner variation, at the cost of power consumption, where a target of 3 nW operation is used. More specifically increasing the sizes of some of the transistors in the output stage of the bandgap reference. The increased power consumption of the bandgap reference does not affect the total power consumption of the reference generator system to a high degree, as this circuit only contributes ≈ 1 % to the total power

consumption. Another modification made to the bandgap reference in this thesis is the use of a larger load capacitance to improve the noise suppression at the output, as well as improving the high-frequency power supply rejection.

A detailed description of the operation of the bandgap reference circuit can be found in [1]. The circuit utilizes flipped-well devices in order to enable the use of body-bias in the output stage.

4.3 Constant-transconductance circuits

The reference generator is biased with three different current references; $PBIAS\_1V2$, $PBIAS$ and $NBIAS$. These references originate from constant-transconductance circuits, described in Ch. 3.4. $NBIAS$ is used to bias the output buffers, while $PBIAS$ is utilized as a PTAT current source for the symmetrical OTAs in the same output buffers. The $MAIN\ OTA$ operates with a supply voltage of 1.2V, and a separate constant-transconductance circuit operating at the same supply voltage is used to provide a PTAT current source in the form of $PBIAS\_1V2$ to this OTA. The nets $PBIAS$ and $NBIAS$ are loaded with bypass capacitors in order to improve the supply rejection in these references.

4.4 Layout

A layout of the entire reference generator system is manually created in order to examine the effects of layout parasitics. Design Rule Check (DRC) and Layout Vs. Schematic (LVS) is utilized to validate the completed layout, such that no errors from these tests are generated. The parasitic extraction is performed using Calibre PEX, which is configured to only include capacitive parasitics. The extracted netlist containing these parasitics is simulated in the same testbenches used for the schematic simulations. Tab. 4.1 presents the total rectangular area of the different circuit blocks in the reference generator system and includes a reference to illustrations of the specific circuits included in the appendix.

Table 4.1: Area of different circuit blocks in the reference generator system.

	Area[kμm^2]	Ref.
Reference generator system incl. decoupling caps	293	Fig. B.15
Reference generator system excl. decoupling caps	10.7	Fig. B.16
Bandgap reference	2.31	Fig. B.17
Constant-transconductance	3.75	Fig. B.18
Constant-transconductance 1V2	.264	Fig. B.19
$MAIN\ OTA$	.060	Fig. B.20
Symmetrical OTA in the $VREFP$-buffer	.114	Fig. B.21
Symmetrical OTA in the $VREFCM$-buffer	.088	Fig. B.22

The main layout of the entire reference generator system used in layout simulations includes the decouple capacitances. This is done in order to illustrate the large area savings of placing this capacitance off-chip (282 kμm^2), as well as being able to simulate how the extracted netlist containing these capacitances behaves. The total rectangular area of the entire reference generator system including bias circuits is 10.7 kμm^2, where it is assumed that the decoupling capacitors are placed off-chip.

Chapter 5

Results and Discussions

This chapter presents several different simulation results in multiple sub-chapters. Different analyses and testbenches are used to obtain these results and a thorough explanation of the analyses is included in the associated sub-chapter. The *Cadence Virtuoso Environment*, which utilizes the *Spectre Circuit Simulator*, is used to obtain the simulation results. Illustrations of the different testbenches can be found in appendix C.

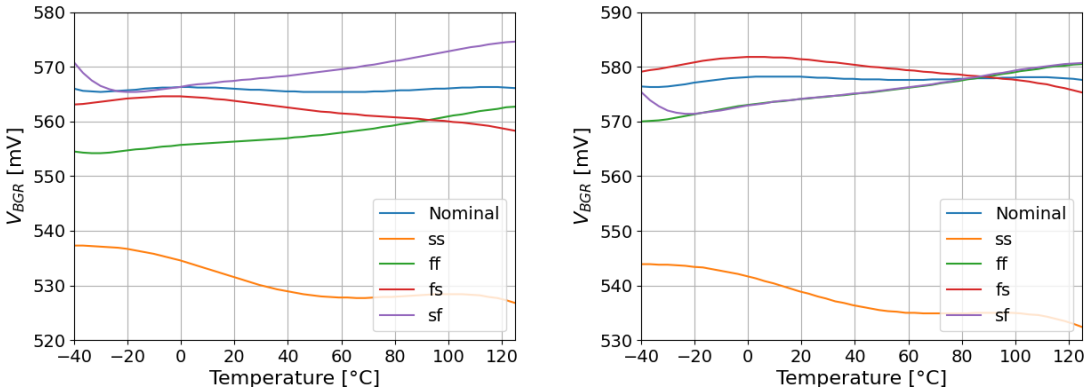
As mentioned in Ch. 3.5, the performance metrics of the reference generator include; the Temperature Coefficient (TC), the DC value of the references at room temperature (27°C), the Power Supply Rejection Ratio (PSRR), the total integrated output noise (from 1 to 20 kHz), the total power consumption of the entire reference generator system, as well as the ENOB at the output of the ADC. The presentation of the results includes a continuous discussion, however other key aspects of the design are further discussed in Ch. 5.8. The layout simulations utilize a netlist containing parasitic capacitances, extracted from the manually created layout, including on-chip decoupling capacitors. Knowledge regarding Monte Carlo mismatch simulations and process variation is considered well-known to the reader, and not further elaborated on in this thesis.

5.1 DC-simulations

The DC-simulation results are presented in this sub-chapter and are obtained by using the *DC-analysis*, sweeping the temperature from -40 to 125 °C, while keeping the supply voltages VDD_1V2 and VDD_0V8 fixed at their respective voltage levels. The power consumption of the entire reference generator system is obtained in DC-simulations, however, included as a separate sub-chapter, Ch. 5.7.

5.1.1 Bandgap reference voltage V_{BGR}

Both schematic and layout DC-simulations of the bandgap voltage V_{BGR} are illustrated in Fig. 5.1.



(a) Schematic simulation of V_{BGR}.

(b) Layout simulation of V_{BGR}.

Figure 5.1: Simulations of V_{BGR} across different process corners.

From the figure, one can observe a DC-offset between the different process corners, especially when it comes to the ss-corner. It is also clear that there is a small DC-offset between the schematic and layout simulations, indicating a deviation in current between the schematic and the netlist containing parasitic capacitances. Even though the layout simulation shows slightly larger voltage values across all corners, the high-temperature behavior is superior as compared to the schematic simulation where a larger spread between the corners can be observed. The complex curvature of the voltages comes from the higher-order curvature correction in the bandgap reference, explained in [1]. The key results from Fig. 5.1 are summarized in Tab. 5.1 and Tab. 5.2.

Table 5.1: Schematic simulation of V_{BGR} across different process corners.

	nominal	ss	ff	fs	sf
TC(V_{BGR}) [ppm/°C]	9.71	120	92.9	67.9	98.5
Power consumption [nW]	3.29	1.28	7.23	5.96	2.06
V_{BGR} at room temperature (27 °C) [mV]	566	531	556	563	568

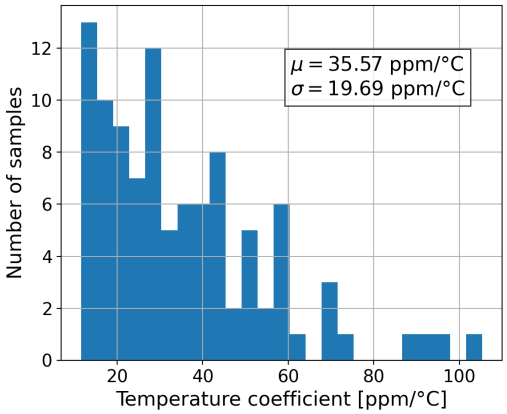
Table 5.2: Layout simulation of V_{BGR} across different process corners.

	nominal	ss	ff	fs	sf
TC(V_{BGR}) [ppm/°C]	20.7	130	111	68.2	97.5
Power consumption [nW]	3.09	1.19	6.79	5.59	1.94
V_{BGR} at room temperature (27 °C) [mV]	578	538	574	581	574

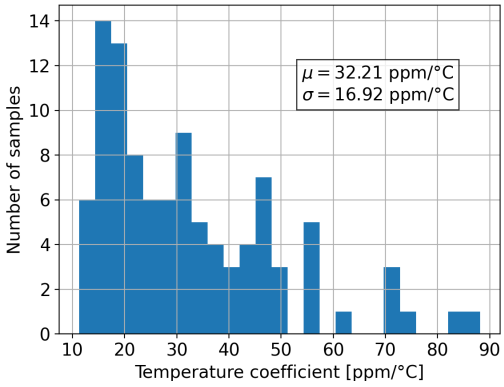
From the tables, one can observe that the DC-offset at room temperature between the nominal- and ss-corner is 35 mV and 40 mV for the schematic and layout simula-

tion respectively, but because of the higher-order curvature correction, the TC of the bandgap voltage V_{BGR} is kept $\leq$130 ppm/°C across all process corners, where the temperature coefficient in the nominal corner in the schematic simulation achieves an impressive value of $\leq$10 ppm/°C, indicating a very weak temperature dependence. As compared to the work in [1], the TC is improved across all process corners, however, the nominal power consumption is increased from .983 nW to 3.29 nW in the schematic simulation. The DC-offset at room temperature between the nominal corner and all other corners, except the ss-corner, is small and at maximum only 4 mV.

A mismatch simulation of V_{BGR} containing 100 Monte Carlo runs is included in appendix D and histograms of the different key performance metrics are illustrated in Fig. 5.2 and Fig. 5.3.

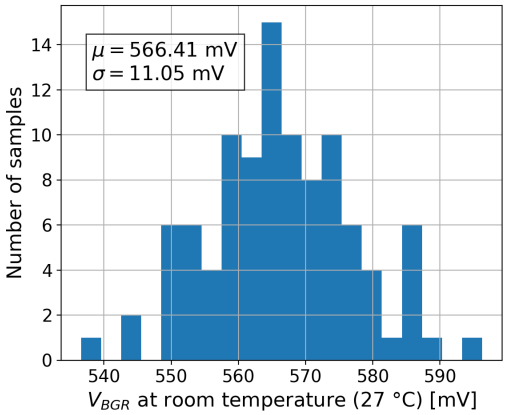


(a) Schematic simulation of V_{BGR}.

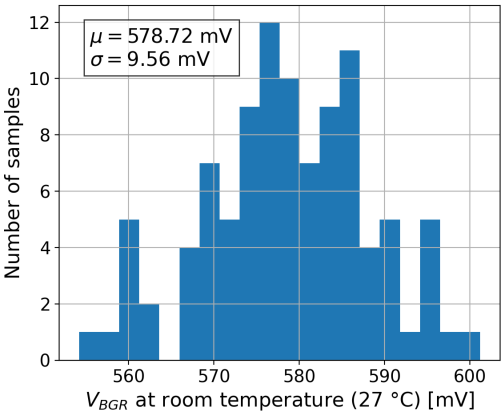


(b) Layout simulation of V_{BGR}.

Figure 5.2: 100 run Monte Carlo simulation of the TC of V_{BGR}.



(a) Schematic simulation of V_{BGR}.



(b) Layout simulation of V_{BGR}.

Figure 5.3: 100 run Monte Carlo simulation of V_{BGR} at 27°.

From the histograms, one can observe that the layout containing the parasitic capac-

itances achieves a better mean TC = 32.21 ppm/°C as compared to the schematic simulation where the mean TC equals 35.57 ppm/°C. It is also clear from the same figure that the standard deviation is smaller in the layout simulation and a stronger grouping around 20 ppm/°C can be observed in Fig. 5.2b, as compared to Fig. 5.2a. The same relation between the schematic and layout simulations can be found in Fig. 5.3, where the bandgap voltage V_{BGR} in a 100 run Monte Carlo simulation is illustrated. There is not a large difference in the standard deviation in the different simulations, however the same DC-offset as the process corner simulations can be observed, where the mean value of the bandgap voltage containing parasitic capacitance equals 578.7 mV at room temperature, while the schematic simulation results in a mean V_{BGR} of 566.4 mV at room temperature. The results from the Monte Carlo mismatch simulations are summarized in Tab. 5.3 and Tab. 5.4.

Table 5.3: 100 run schematic Monte Carlo simulation of V_{BGR}.

	Min	Max	Mean (μ)	Std Dev (σ)
TC(V_{BGR}) [ppm/°C]	11.6	105	35.6	19.7
Power consumption [nW]	2.57	4.71	3.33	.385
V_{BGR} at room temperature (27 °C) [mV]	537	596	566	11.1

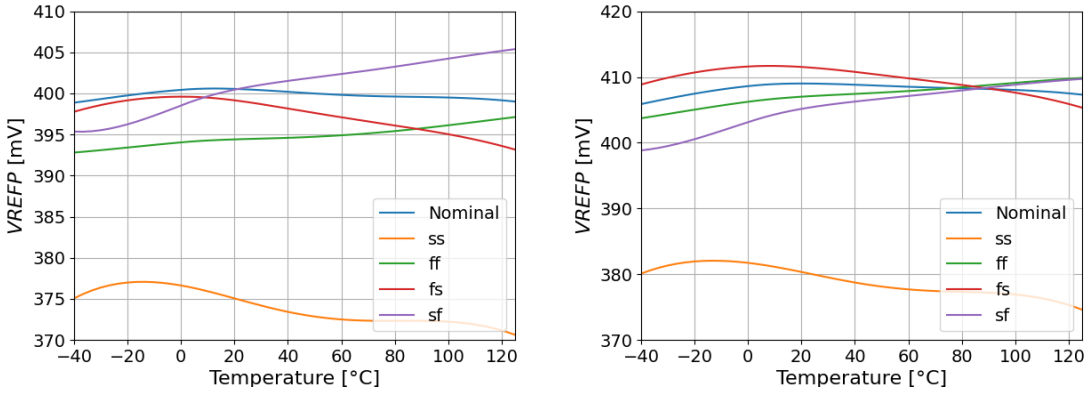
Table 5.4: 100 run layout Monte Carlo simulation of V_{BGR}.

	Min	Max	Mean (μ)	Std Dev (σ)
TC(V_{BGR}) [ppm/°C]	11.3	88.2	32.2	16.9
Power consumption [nW]	2.73	4.23	3.34	.365
V_{BGR} at room temperature (27 °C) [mV]	554	601	579	9.56

An interesting observation is that even though the mean V_{BGR} at room temperature differs by 13 mV between the schematic and layout simulations, the mean power consumption only varies by 0.01 nW between the same simulations. The mismatch performance in terms of the TC is improved, compared to the original design in [1], however, the standard deviation of the bandgap voltage V_{BGR} at room temperature is worse when the same comparison is made. How the bandgap voltage affects the reference voltages is discussed in the following sub-chapters.

5.1.2 VREFP

Both schematic and layout DC-simulations of the reference voltage $VREFP$ are illustrated in Fig. 5.4.



(a) Schematic simulation of $VREFP$. (b) Layout simulation of $VREFP$.

Figure 5.4: Simulations of $VREFP$ across different process corners.

The curvature and corner variation of the reference voltage $VREFP$ resembles the bandgap voltage in Fig. 5.1. This is not surprising, as this reference voltage is a scaled version of V_{BGR} given by Eq. 4.2. The key results from Fig. 5.4 are summarized in Tab. 5.5 and Tab. 5.6.

Table 5.5: Schematic simulation of $VREFP$ across different process corners.

	nominal	ss	ff	fs	sf
TC($VREFP$) [ppm/°C]	24.1	105	64.2	99.5	154
Output current [nA]	47.9	34.7	67.8	37.5	61.5
$VREFP$ at room temperature (27 °C) [mV]	400	374	395	399	401

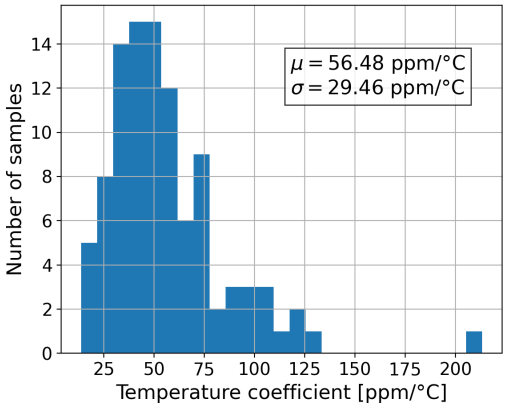
Table 5.6: Layout simulation of $VREFP$ across different process corners.

	nominal	ss	ff	fs	sf
TC($VREFP$) [ppm/°C]	42.8	120	88.5	94.6	159
Output current [nA]	62.5	39.9	102	57.5	69
$VREFP$ at room temperature (27 °C) [mV]	409	380	407	411	406

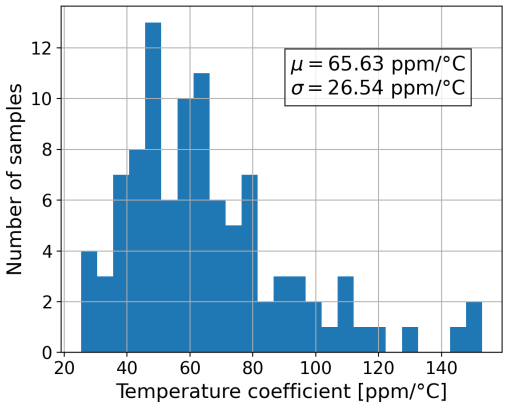
Comparing these tables with the tables summarizing the bandgap reference performance reveals that the temperature coefficient is improved at the output of the reference generator in the ss- and ff-corner. The large degradation in the TC in the sf-corner is due to degradation in the DC-gain of the symmetrical OTA in the $VREFP$ buffer. This is further discussed, as well as illustrated in Ch. 5.3.

Key results from the tables include the output current, as the required output current calculated in Eq. 4.4, is crucial for delivering enough current to the capacitive DACs

in the SAR-ADC. Both the ss- and fs-corner in the schematic simulation have a lower output current than the calculated value in Eq. 4.4. This is because the design is optimized in nominal corner conditions. How this affects the SAR-ADC performance is discussed in Ch. 5.5. A mismatch simulation of $VREFP$ containing 100 Monte Carlo runs is included in appendix D and histograms of the different key performance metrics are illustrated in Fig. 5.5 and Fig. 5.6.

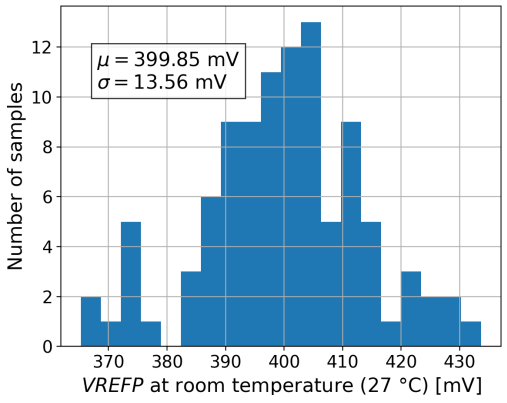


(a) Schematic simulation $VREFP$.

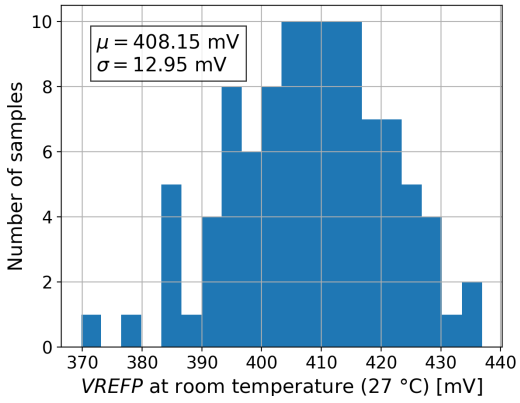


(b) Layout simulation of $VREFP$.

Figure 5.5: 100 run Monte Carlo simulation of the TC of $VREFP$.



(a) Schematic simulation of $VREFP$.



(b) Layout simulation of $VREFP$.

Figure 5.6: 100 run Monte Carlo simulation of $VREFP$ at 27 °C.

The Monte Carlo simulation of $VREFP$ reveals a higher TC as compared to the TC of the bandgap voltage V_{BGR} in Fig 5.2. This is mainly due to mismatch in the output buffer. The devices used in the output stage of the buffer are high threshold devices and the devices used in the symmetrical OTA are low threshold devices with better mismatch performance. Simulation shows that using the same types of devices in both sub-circuits improves the matching at the output, meaning that low threshold devices need to be used in both the symmetrical OTA and in the output buffer stage to improve mismatch. There exists several advantages with

high threshold devices in the output stage, discussed in Ch. 4.1, hence this type of mismatch optimization is not utilized. The results from the Monte Carlo mismatch simulations are summarized in Tab. 5.7 and Tab. 5.8.

Table 5.7: 100 run schematic Monte Carlo simulation of $VREFP$.

	Min	Max	Mean (μ)	Std Dev (σ)
TC($VREFP$) [ppm/°C]	13.8	213	56.5	29.6
Output current [nA]	18.8	101	49.3	15.7
$VREFP$ at room temperature (27 °C) [mV]	365	434	400	13.6

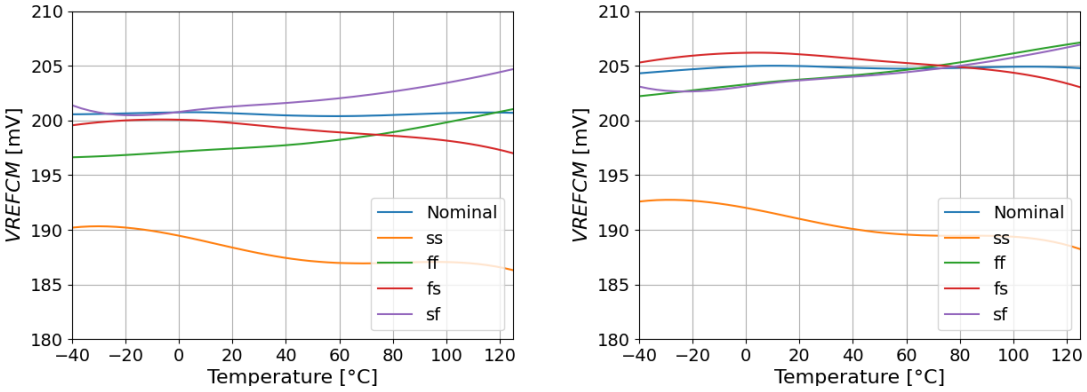
Table 5.8: 100 run layout Monte Carlo simulation of $VREFP$.

	Min	Max	Mean (μ)	Std Dev (σ)
TC($VREFP$) [ppm/°C]	25.4	153	65.6	26.7
Output current [nA]	31.4	156	67.4	21.3
$VREFP$ at room temperature (27 °C) [mV]	370	437	408	13.0

From the tables, one can observe that the mean TC of $VREFP$ in the layout Monte Carlo simulation is higher than the schematic simulation, however, the standard deviation is lower, mainly because of the outlier at 213 ppm/°C, observed in Fig 5.5a. One can also observe a higher mean output current as well as a higher voltage value of $VREFP$ at room temperature in the layout simulation. How the mismatch in the reference voltage $VREFP$ affects the SAR-ADC performance is discussed in Ch. 5.5.

5.1.3 VRECM

Both schematic and layout DC-simulations of the reference voltage $VREFCM$ are illustrated in Fig. 5.7.



(a) Schematic simulation of $VREFCM$. (b) Layout simulation of $VREFCM$.

Figure 5.7: Simulations of $VREFCM$ across different process corners.

The temperature dependence of $VREFCM$ resembles the DC-simulation of $VREFP$. This reference voltage is also a scaled version of the bandgap voltage given by Eq. 4.3. The key results from Fig. 5.7 are summarized in Tab. 5.9 and Tab. 5.10.

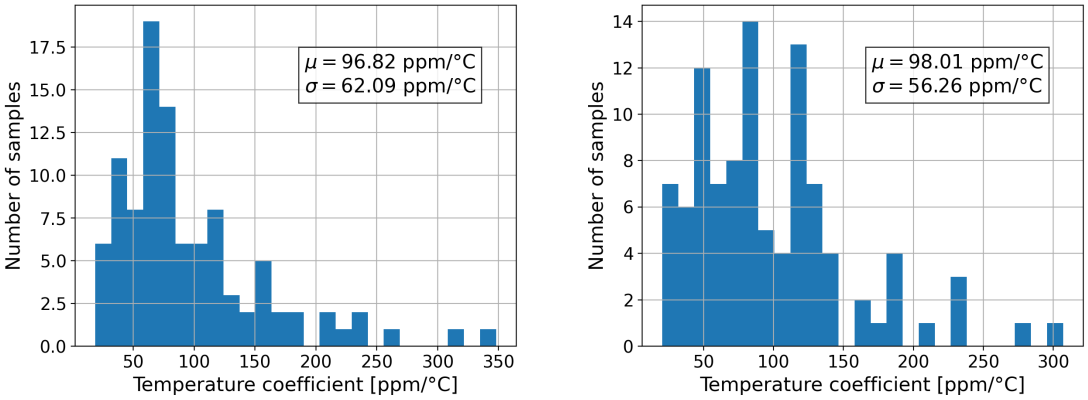
Table 5.9: Schematic simulation of $VREFCM$ at different process corners.

	nominal	ss	ff	fs	sf
TC($VREFCM$) [ppm/°C]	11.8	130	134	94.9	129
Output current [nA]	183	139	252	141	239
$VREFCM$ at room temperature (27 °C) [mV]	201	188	198	200	201

Table 5.10: Layout simulation of $VREFCM$ at different process corners.

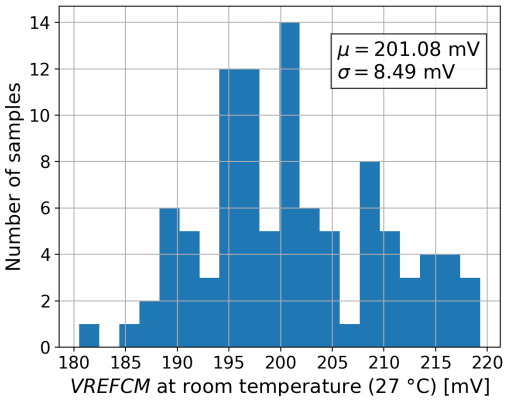
	nominal	ss	ff	fs	sf
TC($VREFCM$) [ppm/°C]	19.4	142	144	95.3	131
Output current [nA]	346	220	577	332	368
$VREFCM$ at room temperature (27 °C) [mV]	205	191	204	206	204

It is clear from the tables that the TC of the reference voltage $VREFCM$ is optimized in nominal corner conditions, where a particularly low-temperature coefficient of 11.8 ppm/°C is achieved in the schematic simulation. The corner performance resembles the results from the $VREFP$ reference voltage, however, a noticeable deviation in the output current between the schematic and layout simulation can be observed. The nominal output current in the schematic simulation is based on Eq. 4.5, including a small margin to handle process variations. The output current in the layout simulation is almost two times as large as the output current in the schematic simulation. The parasitic extraction of the layout only includes capacitive effects, however, it is apparent that these effects result in a deviation in the current in the output buffer. A mismatch simulation of $VREFCM$ containing 100 Monte Carlo runs is included in appendix D and histograms of the different key performance metrics are illustrated in Fig. 5.8 and Fig. 5.9.

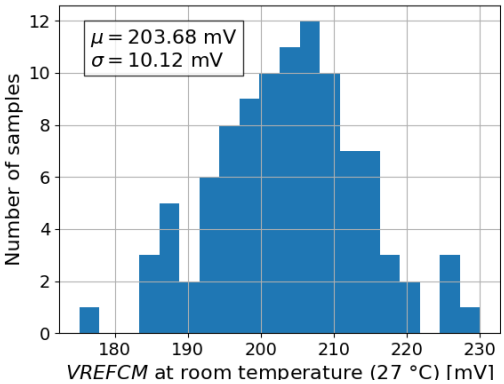


(a) Schematic simulation $VREFCM$. (b) Layout simulation of $VREFCM$.

Figure 5.8: 100 run Monte Carlo simulation of the TC of $VREFCM$.



(a) Schematic simulation of $VREFCM$.



(b) Layout simulation of $VREFCM$.

Figure 5.9: 100 run Monte Carlo simulation of $VREFCM$ at 27 °C.

The histograms indicate a worse mismatch performance in the $VREFCM$ reference voltage when a comparison with the $VREFP$ reference is made. The mean voltage level of $VREFCM$ at room temperature is close to the desired voltage of 200 mV, however, the standard deviation is almost 10 % of the mean value, due to some outliers, clearly illustrated in Tab. 5.11 and Tab. 5.12, where min and max values are included.

Table 5.11: 100 run schematic Monte Carlo simulation of $VREFCM$.

	Min	Max	Mean (μ)	Std Dev (σ)
TC($VREFCM$) [ppm/°C]	18.8	348	96.8	62.4
Output current [nA]	74.7	415	188	60.3
$VREFCM$ at room temperature (27 °C) [mV]	181	219	201	8.53

Table 5.12: 100 run layout Monte Carlo simulation of $VREFCM$.

	Min	Max	Mean (μ)	Std Dev (σ)
TC($VREFCM$) [ppm/°C]	20.3	307	98.0	56.5
Output current [nA]	168	873	371	116
$VREFCM$ at room temperature (27 °C) [mV]	175	230	204	10.2

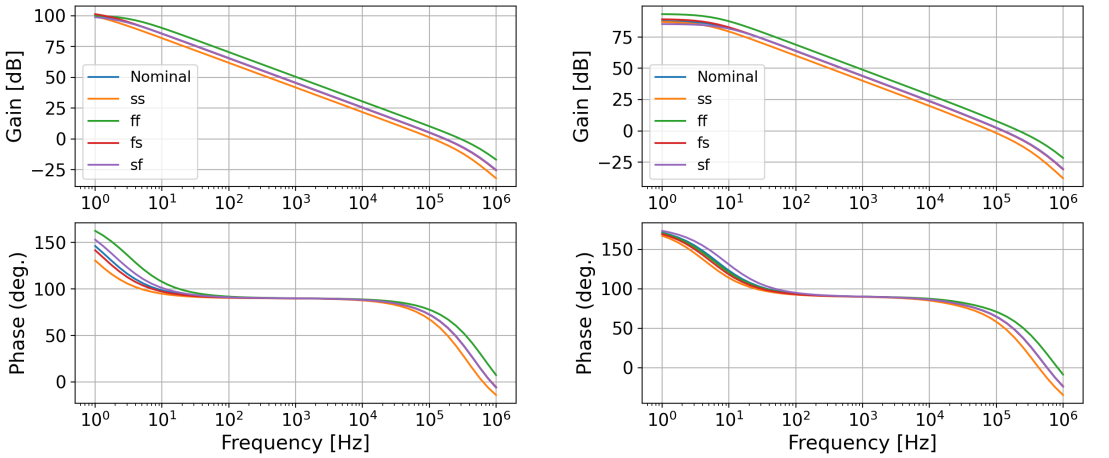
Even though the nominal temperature coefficient in the $VREFCM$ reference is superior, compared to the $VREFP$ reference, the mismatch performance is notably worse. It is clear that the effect of using high threshold devices in the output stage affects the $VREFCM$-buffer in a more significant way. When running another mismatch simulation, where mismatch in the $VREFCM$-buffer is ignored, the performance drastically improves and it is clear that techniques for optimizing the mismatch in this buffer need to be implemented in future work.

5.2 AC-simulations

5.3 OTAs

The simulation results of the different OTAs used in the reference generator design are included in this thesis, as they affect the temperature coefficient of the reference voltages, as well as the power supply rejection at the output nodes. The OTAs are implemented based on the bandwidth requirement in Eq. 3.12, as well as a targeted DC-gain of >60 dB from Ch. 4.1. The results are obtained using *STB-analysis* and breaking the feedback-loop with an *iprobe* (current probe) such that the open-loop response, including gain and phase, can be measured.

The gain- and phase-response of the $MAIN\ OTA$ in different circuit configurations are illustrated in Fig 5.10.

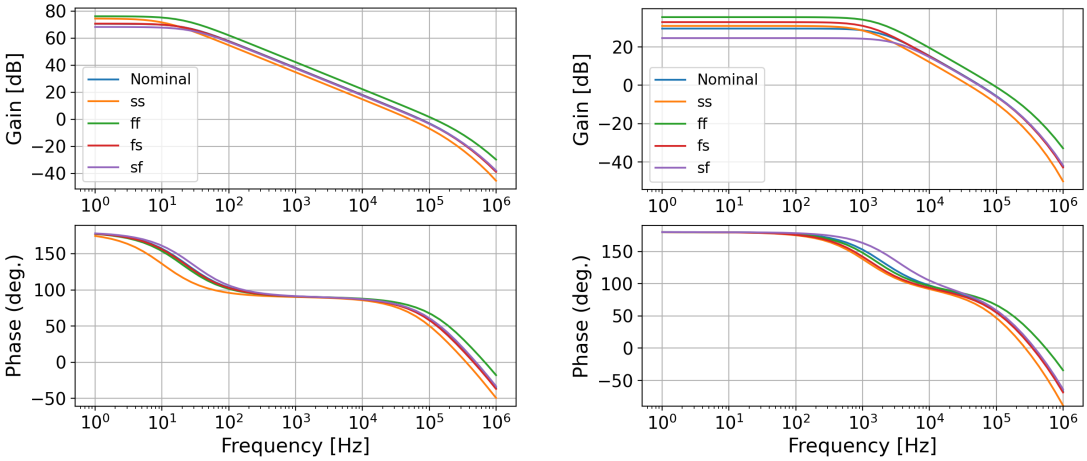


(a) $MAIN\ OTA$ only.

(b) $MAIN\ OTA$ incl. output network.

Figure 5.10: Gain and phase of $MAIN\ OTA$ in different configurations.

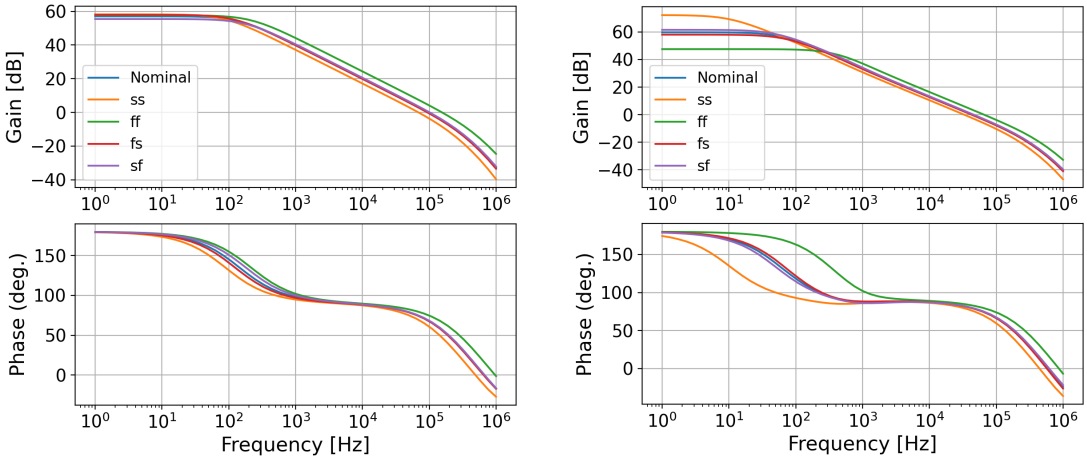
The results in Fig. 5.10a are utilizing a testbench where only the $MAIN\ OTA$ is included, and the results in Fig. 5.10b includes the entire reference generator circuit from Fig. 4.2, such that the effect of the transistor N_1 in the feedback-loop can be investigated. Simulation results show a large DC-gain of >100 dB in the isolated testbench and a DC-gain of >80 dB when the effect of the transistor N_1 in Fig. 4.2 is included. This large DC-gain ensures that the voltage across the resistor R_1 equals the bandgap voltage V_{BGR}. The bandwidth of the OTA is above the required 35 kHz from Eq. 3.12 and the phase margin is kept above 60° across all process corners to ensure stable operation in both circuit configurations. An interesting observation is that the OTA is biased with a very little current to improve the total power consumption, such that the phase response does not start at 180°, and the gain response immediately starts to decrease in the configuration in Fig. 5.10a. The low bandwidth requirement of only 35 kHz makes the low current biasing possible, as the gain of the OTA is well above the targeted value of 60 dB.



(a) $VREFP\ OTA$ only. (b) $VREFP\ OTA$ incl. output network.

Figure 5.11: Gain and phase of $VREFP\ OTA$ in different configurations.

Similar to the previous simulations, the results in Fig. 5.11a are utilizing a testbench where only the $VREFP\ OTA$ is included, and the results in Fig. 5.11b includes the entire buffer circuit from Fig. 4.3, such that the effect of the transistor N_1 in the feedback-loop can be investigated. One can observe large degradations across process corners in the gain of the OTA in the $VREFP$-buffer, as compared to the testbench that excludes the effect of the output network. The largest degradation in DC-gain takes place in the sf-corner and correlates with the results in Ch. 5.1.2, where the worst temperature coefficient can be observed in this exact process corner. Another implication of the degradation in gain is the effect this has on the power supply rejection at the output, covered in the next sub-chapter.



(a) $VREFCM\ OTA$ only. (b) $VREFCM\ OTA$ incl. output network.

Figure 5.12: Gain and phase of $VREFCM\ OTA$ in different configurations.

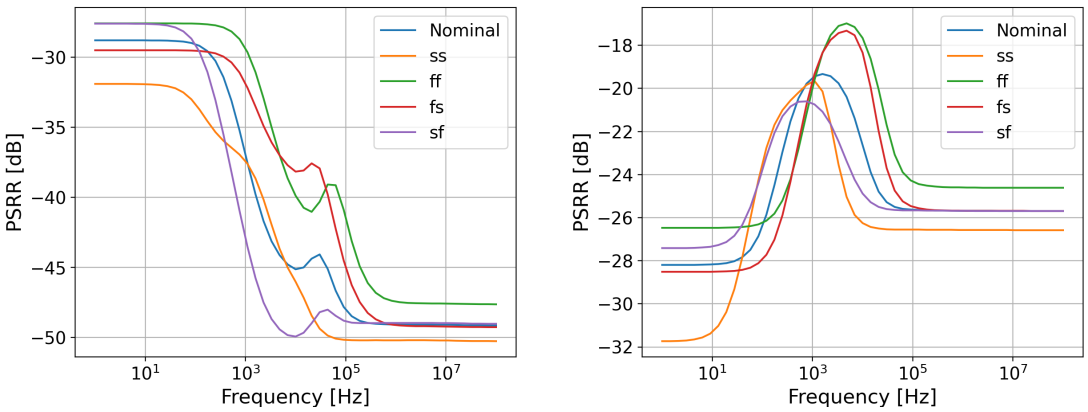
The same type of testbenches used for the $VREFP\ OTA$ are implemented for the

$VREFCM$ OTA, where the results of these are illustrated in Fig. 5.12. From the figures (a) and (b), one can observe a smaller degradation in gain as compared to the $VREFP$ OTA in Fig. 5.11, for the OTA including the effect of the output network. The ff-corner inherits the lowest DC-gain, therefore resulting in the largest temperature coefficient for $VREFCM$ in this corner, given in Tab. 5.9 and Tab. 5.10.

Simulations show that increasing the length of the transistors in the output buffers counteracts the degradation in gain that is taking place in both output buffers. This can lead to an improved temperature coefficient in the reference generator voltages $VREFP$ and $VREFCM$, as well as improved power supply rejection performance, however with one major consequence. By increasing the length of the transistors in the output buffers, the output impedance will be increased, resulting in non-linear effects at the output of the SAR-ADC and degradation in the achieved ENOB. How the gain of the amplifiers in the output buffers affects the PSRR in the reference voltages is covered in the following sub-chapter.

5.4 Power Supply Rejection

The results regarding the power supply rejection are obtained using *AC-analysis*, and the supply voltages VDD_1V2 and VDD_0V8 are set up as AC voltage sources. The square of the changes in the supply voltage is divided by the square of the changes in the reference voltages V_{BGR}, $VREFP$ and $VREFCM$, in order to calculate the PSRR. Results of both schematic and layout simulations of the PSRR in the bandgap voltage V_{BGR} are illustrated in Fig. 5.13.



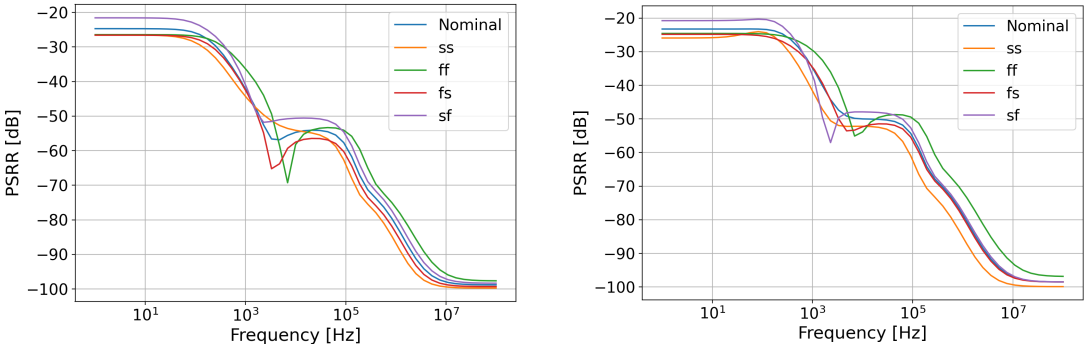
(a) Schematic simulation of V_{BGR}.

(b) Layout simulation of V_{BGR}.

Figure 5.13: Simulations of the PSRR in V_{BGR} across different process corners.

Comparing the results of the PSRR with the original implementation in [1], one can observe an improved suppression of the supply variation in the bandgap voltage. This can be explained by the increased load capacitance at the output node. There still exists a resonance in the layout simulation across all process corners, due to

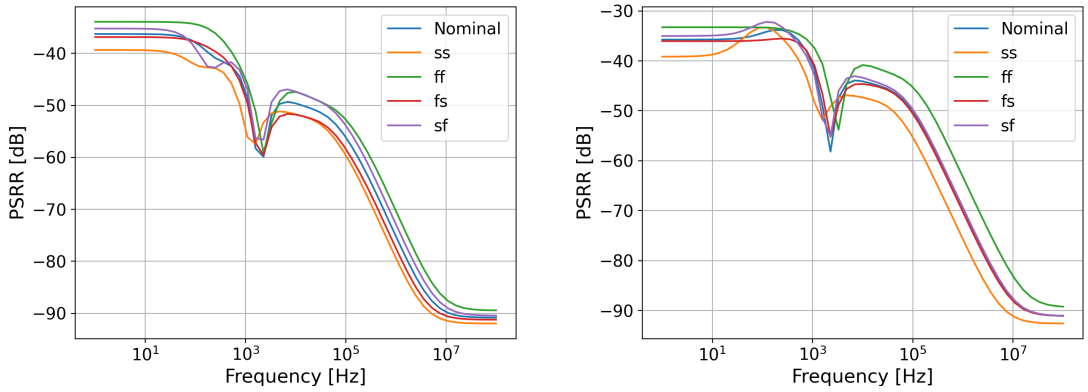
the use of body-bias in the output stage of the bandgap reference (supply voltage used to body-bias transistor N_3 in Fig. 4.4). The parasitic capacitance between the bulk and source of the output transistor couples the supply voltage directly to the bandgap voltage, however because of the increased load capacitance, this effect is attenuated. Other techniques of improving the PSRR of the bandgap reference such as using a separate voltage source for the body-bias or powering the entire bandgap reference with a large capacitor are mentioned in [1]. Simulation results including schematic and layout simulations of the PSRR in the reference voltage $VREFP$ are illustrated in Fig. 5.14.



(a) Schematic simulation of $VREFP$. (b) Layout simulation of $VREFP$.

Figure 5.14: Simulations of the PSRR in $VREFP$ across different process corners.

The power supply rejection at DC is limited by the gain of the symmetrical OTA in the $VREFP$-buffer, illustrated in Fig. 5.11b. When comparing the two figures, one can observe that the sf-corner, which has the worst PSRR at DC, also has the lowest gain in the $VREFP$ OTA. The gain of this OTA needs to be increased in order to achieve a better power supply rejection at the output reference node. Simulation results of the other reference voltage $VREFCM$ are illustrated in Fig. 5.15.



(a) Schematic simulation of $VREFCM$. (b) Layout simulation of $VREFCM$.

Figure 5.15: Simulations of the PSRR in $VREFCM$ across different process corners.

The same relation between the gain of the symmetrical OTA in the output buffer

and the PSRR can be observed in the reference voltage $VREFCM$. One can also observe that the PSRR at DC of this reference is greater than the simulation results of the PSRR of $VREFP$ in Fig. 5.14, as the $VREFCM$ OTA achieves greater gain across all process corners, compared to the $VREFP$ OTA. In OTA-based reference generator designs, the bandwidth of the OTAs limits the high-frequency suppression of the supply voltage variation at the output node. This is not the case for the reference voltages $VREFP$ and $VREFCM$, as large capacitive loading is utilized in these nodes. There is a resonance at 10^3-10^5 Hz in the PSRR of both reference voltages, however, the bypass capacitors C_1 and C_2 in Fig. 4.2 attenuate these resonances. The large decoupling capacitors C_{VREFP} and C_{VREFCM} improve the high-frequency response above 10^5 Hz. The results of the PSR-simulations are summarized in Tab. 5.13 and Tab. 5.14, where results at key frequencies are included.

Table 5.13: Schematic simulations of the PSRR at key frequencies across different process corners.

	nominal	ss	ff	fs	sf
$VREFP$ [dB] (DC)	-24.7	-26.6	-26.4	-26.6	-21.6
$VREFP$ [dB] (1 kHz)	-42.0	-44.2	-36.2	-42.4	-40.8
$VREFP$ [dB] (10 kHz)	-54.7	-54.1	-58.2	-57.5	-50.6
$VREFCM$ [dB] (DC)	-36.3	-39.3	-33.9	-36.9	-35.2
$VREFCM$ [dB] (1 kHz)	-47.3	-54.3	-44.8	-48.4	-45.9
$VREFCM$ [dB] (10 kHz)	-49.6	-51.7	-47.4	-51.8	-47.3

Table 5.14: Layout simulations of the PSRR at key frequencies across different process corners.

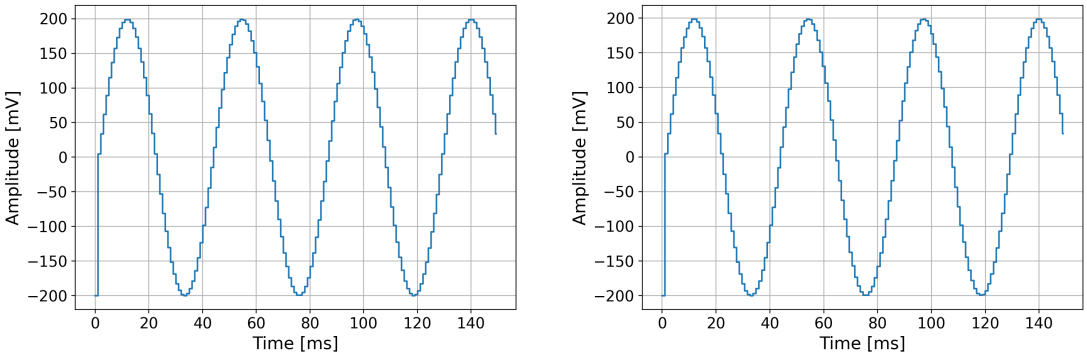
	nominal	ss	ff	fs	sf
$VREFP$ [dB] (DC)	-23.3	-24.1	-24.6	-24.9	-20.6
$VREFP$ [dB] (1 kHz)	-34.7	-41.5	-29.5	34.5	-36.9
$VREFP$ [dB] (10 kHz)	-50	-52.2	-53.9	-52.3	-47.9
$VREFCM$ [dB] (DC)	-33.8	-33.3	-33.3	-35.5	-32.2
$VREFCM$ [dB] (1 kHz)	-40.7	-46.9	-36.9	-40.0	-41.8
$VREFCM$ [dB] (10 kHz)	-44.1	-47.3	-40.8	-44.6	-43.4

The tables include results at DC, 1 kHz, and 10 kHz. This is because the sampling frequency of the SAR-ADC is 1 kHz and the internal clock frequency is 10 kHz, where supply variation at these frequencies is to be expected. The results in the tables are color-coded in terms of the achieved PSRR, to make it easier to compare the two tables. Values >-30 dB are colored red, values between -30 dB and -40 dB are colored black, and values <-40 dB are colored green. Coupling effects due to the parasitic capacitances in the layout result in a degradation in the PSRR for both reference voltages, when comparing the results to the schematic simulations. A PSRR of <-40 dB ensures an attenuation factor of 100, between the changes in the supply voltage and the output. This is achieved in the schematic simulation at the sampling frequency of 1 kHz, across all process corners, except for the ff-corner in the $VREFP$ reference voltage. Increasing the capacitance at the nodes

V_1 and V_2 in Fig. 4.2, can lead to a further improvement in the PSRR at this frequency, however, introduces a large area penalty. The best way of improving the power supply rejection is to increase the gain of the symmetrical OTAs in the output buffers. Interestingly the power supply rejection of V_{BGR} does not degrade the supply rejection at $VREFP$ and $VREFCM$. Using an ideal voltage source as the bandgap voltage results in the same PSRR-response at these nodes. A possible reason for this can be the high gain in the $MAIN\ OTA$.

5.5 Transient Simulations

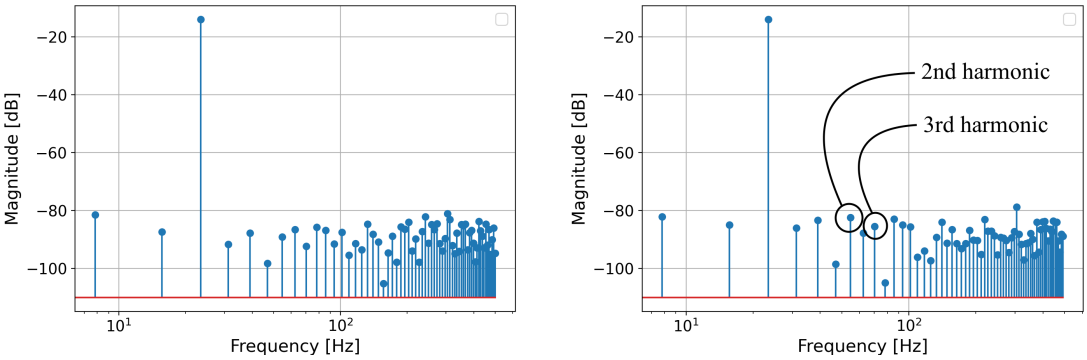
This sub-chapter presents simulations of the reference generator in combination with the sub-nW SAR-ADC. The results are obtained using *tran-analysis* and applying a full-scale sinusoidal signal as the input to the ADC. The reference generator provides the reference voltages for the capacitive DACs, while the comparator and other circuits including digital logic blocks in the SAR-ADC, are driven by a separate supply voltage. The process corner and mismatch simulations do not include variations in the ADC itself, only corner variation and mismatch in the reference generator are introduced. This is because the SAR-ADC is not optimized for corner variation and mismatch. The output signal of the SAR-ADC in nominal corner conditions is illustrated in Fig. 5.16, where both ideal voltage sources and the reference generator are used to supply the reference voltages for the capacitive DACs.



(a) Ideal voltage sources as references. (b) Reference generator as references.

Figure 5.16: Output signal of the ADC, using different voltage references.

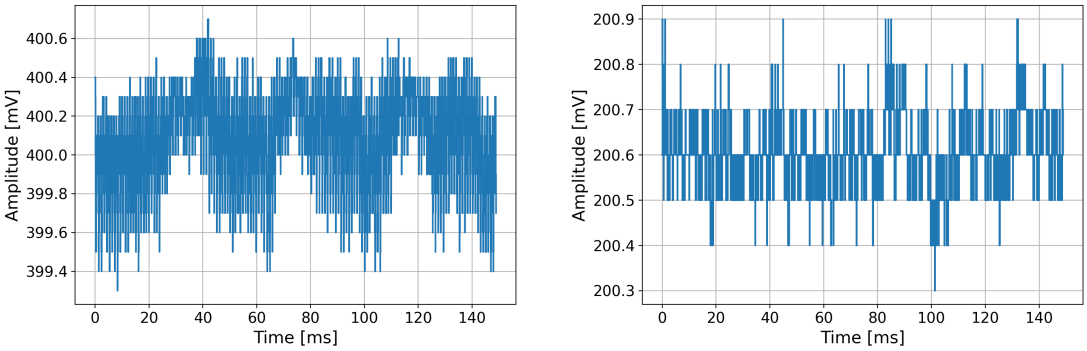
From the figure, it is difficult to observe the non-linear effects the reference generator introduces. The signal at the output of the ADC is shifted by 200 mV with an ideal Verilog-A module to remove the DC-component, and the voltage glitch at the start of the simulation is due to the testbench set-up and not included in the calculation of the ENOB, or the spectrum at the output, illustrated in Fig. 5.17.



(a) Ideal voltage sources as references. (b) Reference generator as references.

Figure 5.17: Output spectrum of the ADC, using different voltage references.

Comparing the output frequency spectrum of the different simulations, the non-linear effects caused by the reference generator is revealed. One can observe a higher noise floor in the simulation utilizing the reference generator, where the second and third harmonics are highlighted in the illustration to make it easier to compare the two results. The 2nd harmonic is slightly larger when compared to the simulation utilizing ideal voltage sources, meaning that the advantages of the differential implementation in the SAR-ADC are weakened. One can also observe a large increase in the third harmonic, which can be explained by the non-linear effects discussed in Ch. 2.3. This sub-chapter describes this non-linearity as a low-frequency code-dependant voltage ripple, due to the output impedance of the reference generator. The effect of this is made obvious in Fig. 5.18, where the transient behavior of the reference voltages in nominal corner conditions is illustrated.



(a) $VREFP$. (b) $VREFCM$.

Figure 5.18: Reference voltages during ADC operation in nominal corner conditions.

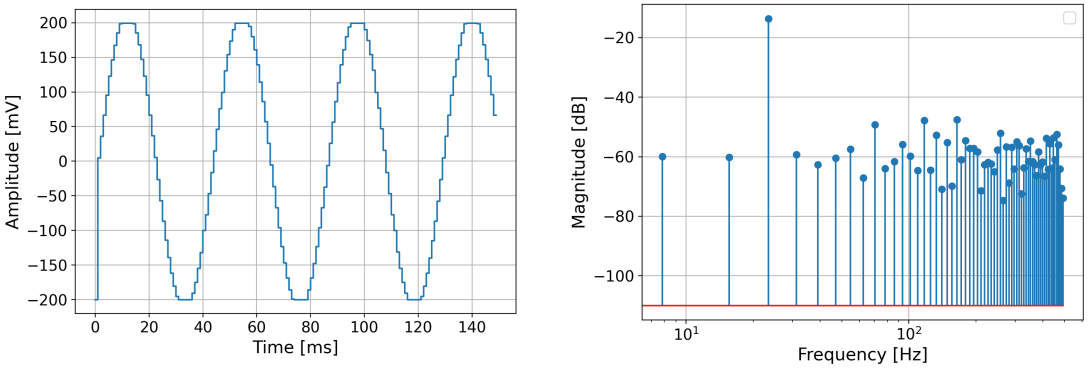
From Fig. 5.18a, illustrating the $VREFP$ reference voltage, periodic low-frequency behavior can be observed, resulting in a large third harmonic in the output spectrum of the SAR-ADC. One can also observe that the voltage ripples in the $VREFP$ reference are larger than LSB/2 = 391 mV, however, the $VREFCM$ voltage ripples are kept below this target value. The simple models used to calculate the decoupling

capacitors in Ch. 4.1 are proven inaccurate, and the capacitance of C_{VREFP} needs to be increased in order to attenuate the non-linear effects at the output of the ADC. Results from a schematic simulation of the ADC across different process corners are summarized in Tab. 5.15, where the achieved effective number of bits at the output of the ADC is included.

Table 5.15: Schematic simulation of the ADC across different process corners.

	nominal	ss	ff	fs	sf
ENOB [bit]	8.81	3.90	7.51	8.69	8.68
Average power consumption [pW]	986	673	899	994	960

The sub-nW SAR-ADC achieves an ENOB of 8.91 bit in nominal corner conditions when using ideal voltage sources as references for the capacitive DACs. With the reference generator, only a small degradation is observed, and an ENOB of 8.81 bit is achieved, however, the reference generator design struggles to maintain this performance across all process corners. The large DC-offset in the ss-corner, discussed in Ch. 5.1, results in a 5-bit loss in resolution at the output of the ADC, when compared with the simulation using ideal voltage sources in the nominal corner. The output signal, as well as the output spectrum of the SAR-ADC, when the reference generator is operating in the ss-corner, is illustrated in Fig. 5.19.

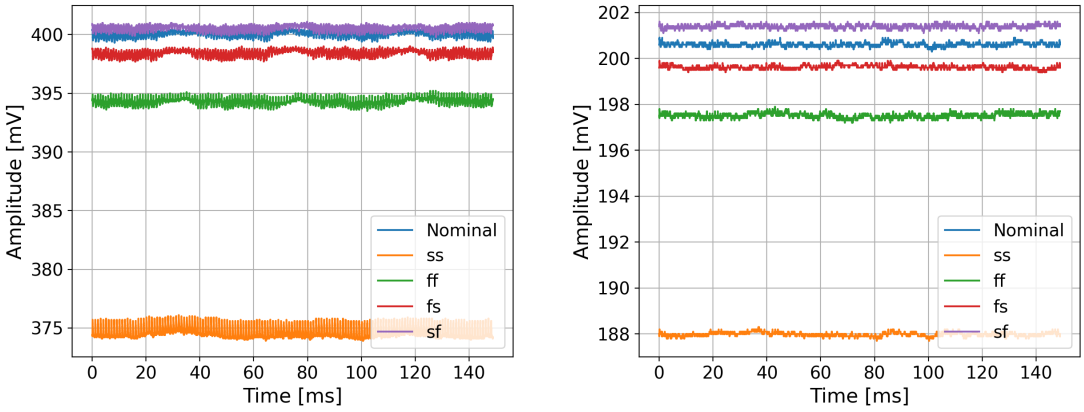


(a) Output signal of the SAR-ADC.

(b) Output spectrum of the SAR-ADC.

Figure 5.19: Output of the SAR-ADC with the reference generator operating in ss-corner.

The output signal experiences clipping effects at ±200 mV, leading to distortion in the output spectrum. The large negative DC-offset in the ss-corner, decreases the value of the LSB, lowering the dynamic range of the ADC. This affects the achieved resolution at the output of the SAR-ADC. The DC-offset in the different reference voltages across process corners during transient simulation is illustrated in Fig. 5.20.



(a) $VREFP$. (b) $VREFCM$.

Figure 5.20: Reference voltages during ADC operation across different process corners.

From the figure, one can observe that the process corner simulation with the second-largest DC-offset (ff-corner), results in the second-worst resolution (ENOB) at the output of the SAR-ADC, substantiating the relation between the DC-offset and the achieved ENOB at the output of the ADC. In order to examine the effect of the process corner variation in the bandgap reference circuit and the ENOB, a simulation using an ideal voltage source as the bandgap voltage V_{BGR} is made, where the results of this simulation are presented in Tab. 5.16.

Table 5.16: Schematic simulation of the ADC across different process corners, using an ideal voltage source as the bandgap voltage V_{BGR}.

	nominal	ss	ff	fs	sf
ENOB [bit]	8.62	8.78	8.74	8.87	8.58
Average power consumption [pW]	985	966	998	975	987

From the table, it is clear that the main degradation in the ENOB at the output of the SAR-ADC originates from the poor DC-performance of the bandgap reference circuit. In order to improve the corner performance of the reference generator, the bandgap reference needs to be re-designed, with a focus on minimizing the DC-offset between the different process corners in the bandgap voltage V_{BGR}.

Another way of improving the corner performance of the reference generator, without the need for a large re-design, is to implement the resistors in the design as trim-resistors. Given that the DC-offset is the cause of the degradation in the achieved ENOB, the resistors R_1, R_2, and R_3 from Fig. 4.2, can be implemented in such a way that makes post-fabrication trimming possible. After fabrication, the resistor values can be calibrated such that the effects of process corner variation on the DC-offset are canceled. It is important to note that only the DC-offset, and not the temperature coefficient of the reference voltages, can be calibrated in this post-fabrication process, however, the TC of the reference voltages is not the limiting factor in this reference generator design.

Results from a layout simulation of the ADC across different process corners are summarized in Tab. 5.17.

Table 5.17: Layout simulation of the ADC at different process corners.

	nominal	ss	ff	fs	sf
ENOB [bit]	8.73	4.30	8.75	8.66	2.17
Average power consumption [nW]	1.13	.724	1.10	1.07	1.18

From the table, one can observe an improved resolution at the output of the SAR-ADC in the ss-corner, compared to the schematic simulation. This is due to the increased reference voltage values in the netlist containing parasitic capacitances, discussed in Ch. 5.1. A large degradation in ENOB can be observed in the sf-corner. This result is not easily described by the DC-behaviour of the reference generator, however, can be caused by coupling effects between sensitive nodes in the output buffers due to parasitic capacitances. The average output current is increased, compared to the schematic simulation, mainly because of the increased current in the $VREFCM$-buffer. Key results from a 10 run schematic Monte Carlo mismatch simulation, are summarized in Tab. 5.18, while results for the same simulation utilizing the layout generated netlist is presented in Tab. 5.19.

Table 5.18: 10 run schematic Monte Carlo simulation of the ADC.

	Min	Max	Mean (μ)	Std Dev (σ)
ENOB [bit]	.254	8.85	4.92	3.33
Average power consumption [nW]	.707	1.41	.976	.227

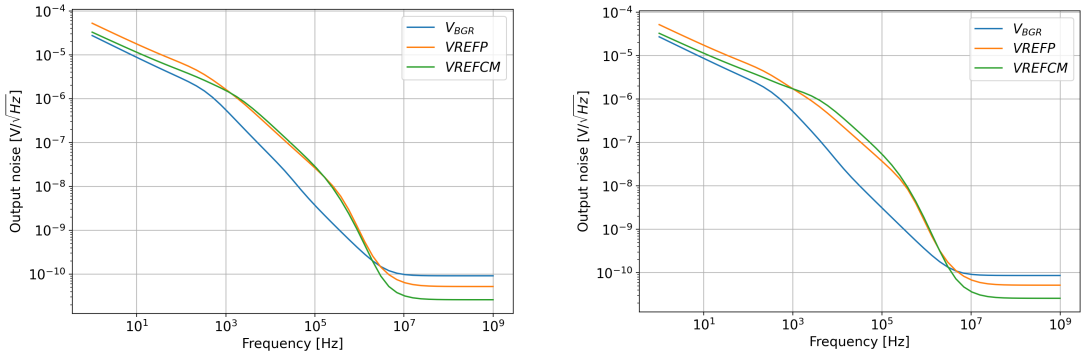
Table 5.19: 10 run layout Monte Carlo simulation of the ADC.

	Min	Max	Mean (μ)	Std Dev (σ)
ENOB [bit]	-.103	8.96	4.82	4.05
Average power consumption [nW]	.703	1.16	.999	.135

From the tables, one can observe that the reference generator design struggles when it comes to mismatch. The mean ENOB at the output of the SAR-ADC is far from the desired 9-bit resolution, and mismatch optimization techniques need to be implemented in the reference generator. The outliers in the mismatch simulation of the reference voltages in Ch. 5.1, result in a large degradation in the ENOB at the output of the ADC. This mismatch is mainly due to the mismatch performance of the bandgap reference as well as the output buffers in the reference generator. When taking a look at the mismatch simulations in App. D, it is clear that the DC-offset in the different runs is quite large, however, the temperature coefficient in each run is low. This means that the same resistor-trim technique, suggested to minimize the effect of process variation in the DC-offset, can be implemented to improve the mismatch performance of the reference generator.

5.6 Noise Simulations

Noise simulation results are presented in this sub-chapter and are obtained using *noise-analysis*, sweeping the frequency from 1 Hz to 1 GHz and analyzing the output-referred noise of the signals. The noise spectral density of the different reference voltages is illustrated in Fig. 5.21, where both schematic and layout simulations are included.



(a) Schematic simulation of output noise.

(b) Layout simulation of output noise.

Figure 5.21: Simulations of output noise for the different reference voltages.

The output noise of the different signals shows a small variation across process corners, therefore only the nominal corner is included in the simulation results. From the figure, one can observe that the reference voltage $VREFP$ inherits the largest noise power, this is because it has a much smaller load capacitance than the other reference voltage $VREFCM$. The total integrated output noise from 1 Hz to 20 kHz is summarized in Tab. 5.20.

Table 5.20: Total integrated output noise from 1 Hz to 20 kHz.

	Schematic	Layout
V_{BGR} [μV]	79.8	78.7
$VREFP$ [μV]	127	130
$VREFCM$ [μV]	91.8	103

From the table, one can observe a large increase in the total noise power of $VREFCM$, when comparing the schematic and layout simulation. This can be explained by the large current increase in the output stage of the $VREFCM$-buffer in the netlist containing parasitic capacitance, discussed in Ch. 5.1.3. Output noise is highly dependent on bias currents, and in order to improve the noise performance in the layout simulations, great care should be employed when preforming layout of bias circuitry.

The total noise power of the different reference voltages is mainly affected by flicker noise, as the band of interest only includes frequencies up to 20 kHz (two times the internal clock frequency of the SAR-ADC), and the thermal noise is filtered by

the large load capacitances in the design. The main limiting noise component in the bandgap reference is the flicker noise in transistor N_4 in Fig. 4.4. Increasing the gate area of this device leads to a large degradation in the TC of the bandgap voltage V_{BGR}, therefore there exists a large trade-off between the DC-performance and noise-performance in the bandgap reference. The total output noise in the reference voltages $VREFP$ and $VREFCM$ is dominated by the flicker-noise in the devices N_1 and N_3 in Fig. 4.3. Increasing the size of these devices leads to larger power consumption in the output buffers, affecting the total power consumption of the reference generator system to a high degree. These devices are implemented as high threshold devices to minimize the length and therefore output impedance of the buffers, however, the small gate length leads to a small gate area in these devices, resulting in poor flicker noise performance.

A noise budget for the SAR-ADC, containing the allowed noise power in the two reference voltages is not provided, however, the low achieved noise of around 100 μV in the two reference voltages, allows for a large margin in the design of the SAR-ADC.

5.7 Power Consumption

The total power consumption of the entire reference generator system in nominal corner conditions is 241 nW in schematic simulations. A pie chart illustrating the percentile power consumption of the different circuit blocks in the reference generator system can be seen in Fig. 5.22.

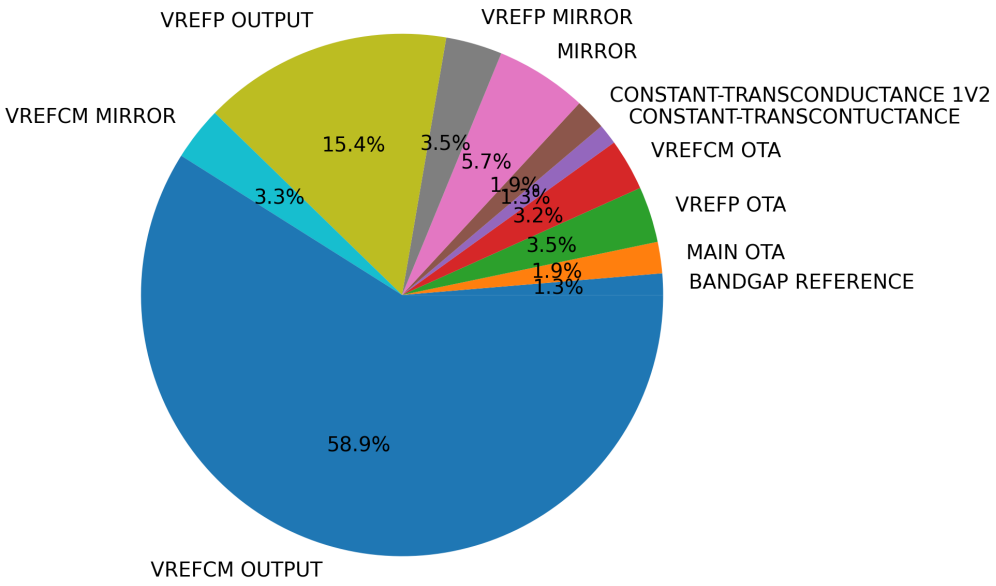


Figure 5.22: Power consumption of different parts of the reference generator system in a schematic simulation.

The pink region $MIRROR$, includes the power consumed by the high swing current mirror in the reference generator, while the $VREFCM\ MIRROR$ and the $VREFP\ MIRROR$ sections include the power consumed by the branch consisting of transistor N_1 and N_3 in Fig. 4.3. The other parts of the charts are self-explanatory, and one can observe that most of the power is consumed in the two output stages $VREFP\ OUTPUT$ and $VREFCM\ OUTPUT$ (branch consisting of transistors N_2 and N_4 in Fig. 4.3). A total of 187 nW (74% of the total power) is consumed in these output stages, where the current in these branches is based on Eq. 4.4 and Eq. 4.5 in Ch. 4. The remaining power consumption is only 54 nW (26% of the total power), used to generate the bandgap reference voltage, obtain constant transconductances, bias the OTAs and supply the other current branches in the reference generator design.

Layout simulations of the reference generator system result in total power consumption of 388 nW. This is due to an increase in current in the $VREFCM$-buffer, discussed in Ch. 5.1.3. A pie chart illustrating the percentile power consumption of the different circuit blocks, in a layout simulation of the reference generator, can be seen in Fig. 5.23.

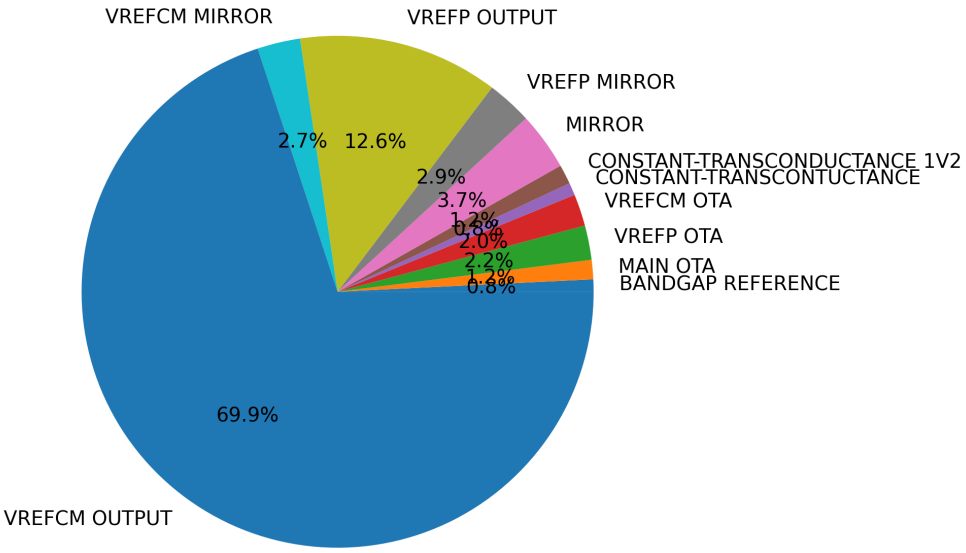


Figure 5.23: Power consumption of different parts of the reference generator system in a layout simulation.

Comparing the two figures, one can clearly see the effect of the increased current consumption in the $VREFCM$-buffer. Only minor deviations in the current consumption are observed when comparing the schematic and layout simulation of the other circuit blocks.

The design implemented in this thesis is based on a Class A output stage, meaning that all of the required current in the SAR-ADC is available at the output of the reference generator at all times. To minimize the power consumption in the reference generator system, the output stage could be configured in a different Class, such that the SAR-ADC sources the required current at the given time. This can however lead to non-linear effects and result in a degradation of the ENOB at the output of the ADC, nevertheless resulting in a severe improvement in the total power consumption of the reference generator system and should be investigated in future work.

Minimizing the power consumption in other parts of the circuit is proven difficult because of the bandwidth constraints on the OTAs and the minimum required current to obtain a stable bandgap reference voltage, however, these parts contribute to only 26% of the total power consumption in the schematic simulation. It is worth mentioning that the constant transconductance circuits can be shared with other circuit blocks that require bias voltages and currents, such that the contribution these have to the total power consumption can be neglected.

5.8 Further discussions

The simulation results in Ch. 5 do not include start-up simulations, as power-down functionality is not implemented in the reference generator. In order to save power when the reference generator is not utilized, this functionality should be implemented, and a fast start-up time to minimize the power consumption during start-up should be targeted. The bandgap reference from [1], includes simulations on start-up behavior across different process corners, where the supply voltage is abruptly switched from 0 V to the supply voltage of 0.8 V. These simulations show a fast start-up time of only 4.27 μs in nominal corner conditions in the bandgap reference voltage, however, the implementation in this thesis utilizes an increased load capacitance to improve the output noise, as well as the high-frequency power supply rejection. This increased capacitance can result in a severe degradation in the start-up time of the bandgap reference. The implementation of the reference generator includes several large capacitors, to reduce the voltage ripples on the reference voltages for the SAR-ADC. The large capacitive loading slows the circuit down and a start-up simulation of the entire reference generator system would reveal a substantial start-up time, compared to the start-up time of the bandgap reference in [1].

In order to improve the start-up behavior, one could implement a kick-start circuit, often used in commercial integrated CMOS designs, where sleep mode and other similar functionality are implemented to lower the average power consumption of the entire design. A kick-start circuit provides a large current in a short amount of time to lower the time it takes for the reference generator to become operational. It is important to note that these transient currents can lead to railing voltages and instabilities, therefore the design of such circuits is often non-trivial.

A method for improving the process corner variability was presented in Ch. 5.5. Implementing the resistors in the design as trim-resistors, enabling post-fabrication calibration. Another way of improving the DC-offset in the reference generator voltages, while taking advantage of the process technology, is to utilize dynamic body-biasing, where the basic concepts of body-biasing are described in the *Background Theory* chapter in [1]. Enabling dynamic body-biasing in the high swing current mirror in the reference generator can help to minimize the corner variation in the internal voltage nodes V_1 and V_2 in Fig. 4.2, thus improving the corner performance in the output reference voltages. An example is the ss-corner, where the output current of the high swing current mirror is too low to generate an adequate voltage in the output stage. Corner dependant dynamic body-biasing in the current mirror could allow for more current in this process corner, resulting in a higher output voltage and reduced DC-offset at the output.

Chapter 6

Conclusion and Future Work

In this thesis, a reference generator for a sub-nW 9-bit 1kSample/s asynchronous SAR-ADC in 22nm UTBB FDSOI has been implemented and simulated. The design was a continuation of the work presented in the specialization project, where a sub-nW bandgap reference was designed and tested using the same design kit. Two reference voltages of 0.2 V and 0.4 V were generated, using a 0.8 V and 1.2 V supply. The references inherit a temperature coefficient of 24.1 ppm/°C and 11.8 ppm/°C in nominal corner conditions during schematic simulations, for the 0.2 V and 0.4 V references respectively. The SAR-ADC achieves an ENOB of 8.91 bits when utilizing ideal voltage sources as reference voltages for the capacitive DACs. Simulations of the SAR-ADC in combination with the reference generator implemented in this thesis achieved an ENOB of 8.73 bits in nominal corner conditions, including parasitic capacitance, extracted from a manually created layout. Several different simulation results were presented and it was made clear that the design struggled with process corner variation as well as mismatch, resulting in a severe degradation in the ENOB at the output of the SAR-ADC. Several techniques for minimizing the process corner variation were suggested and are a part of the future work in this thesis.

The reference generator achieved low output-referred noise in the two reference voltages, measuring at around 100 μV (integrated over an interval of 1 Hz to 20 kHz), mainly because of the large decouple capacitances used in the design. The power supply rejection at the clock frequency of 10 kHz was kept below -40 dB across process corners in layout simulations, however, the PSRR at DC was found to be only -20 dB in worst-case conditions. This was due to gain-degradation in the OTAs used in the output buffers, where a redesign of these OTAs to improve the PSRR was suggested. The total power consumption of the reference generator was found to be 241 nW in nominal corner conditions during schematic DC-simulations, however, layout simulations showed a large increase in output current, in one of the reference branches, making the power consumption of the netlist including layout parasitics equal to 388 nW. Techniques for minimizing the total power consumption, such as substituting the Class A output stage with a different configuration, as well as implementing power-down functionality, were suggested.

Future work needs to contain improvements to the large DC-offset due to process variation, where both trim-resistors and dynamic body-biasing are mentioned as possible solutions to the problem, without the need of redesigning the bandgap reference. The mismatch performance is also a major concern and design techniques for minimizing the mismatch in the output buffers should be implemented. The power supply rejection at the outputs of the reference generator should also be considered as a key aspect in future work, where a redesign of the OTAs in the output buffers should target a very high gain to improve the PSRR at the sampling frequency of the SAR-ADC (1 kHz), as well as at DC. Power-down circuitry should be implemented in future work in order to minimize the average power consumption of the reference generator. Another important aspect of such an implementation is to investigate the achievable start-up time of the entire system, as large capacitive loading in the reference generator circuit, can make the settling time at the output reference nodes enormous. Despite the large performance degradation across different process corners, as well as the poor mismatch behavior, the reference generator circuit provides promising results in nominal corner conditions. This proves that ultra-low-power reference generation is possible, however that accurate methods and innovative design techniques are required, good news for future research in this interesting field.

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2004 47th Midwest Symposium on Circuits and Systems, 2004. MWSCAS '04., volume 1, pages I–5, 2004.

Appendix

A Schematics including device sizes

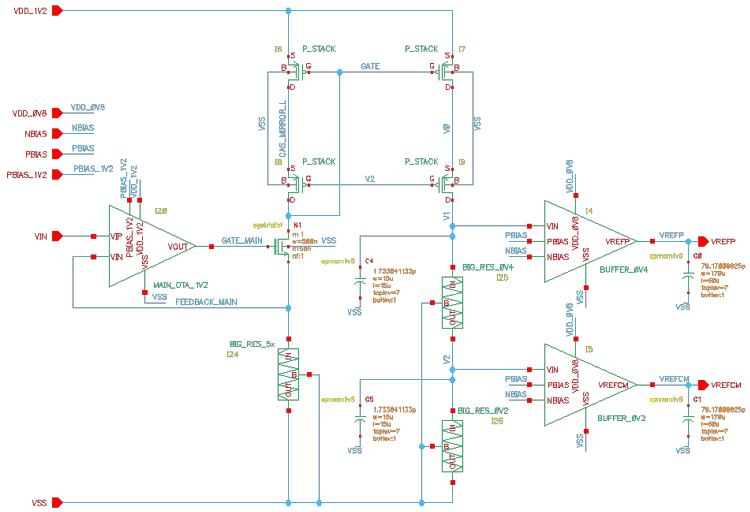


Figure A.1: Schematic of the reference generator from Fig. 4.1 including device sizes.

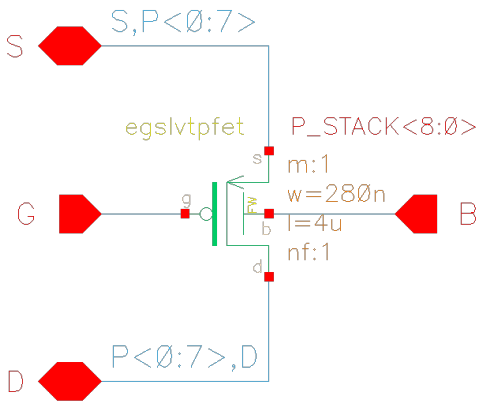


Figure A.2: Schematic of the P_STACK transistor from Fig. A.1 including device sizes.

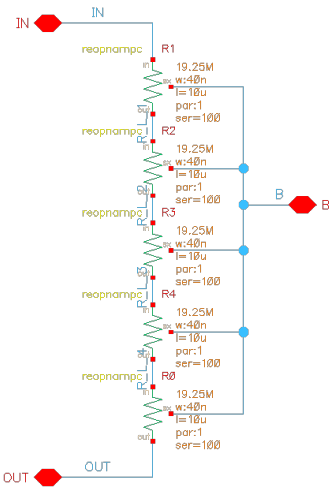


Figure A.3: Schematic of the BIG_RES_5x resistor from Fig. A.1 including device sizes.

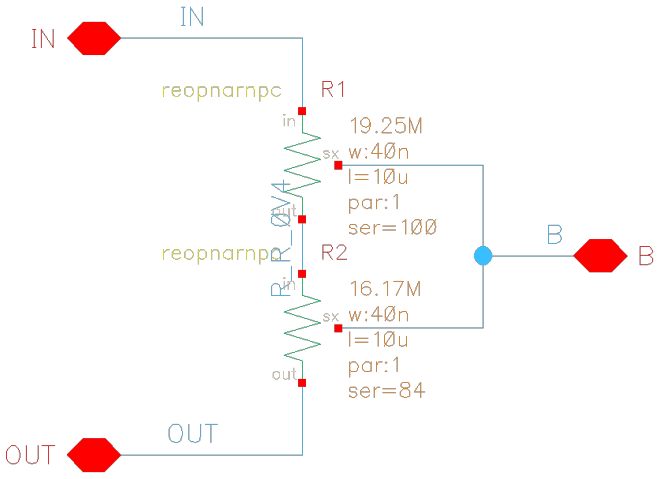


Figure A.4: Schematic of the BIG_RES_0V4 resistor from Fig. A.1 including device sizes.

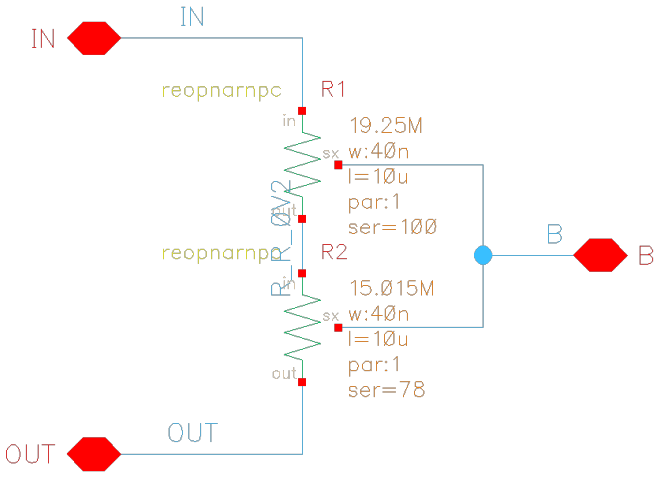


Figure A.5: Schematic of the BIG_RES_0V2 resistor from Fig. A.1 including device sizes.

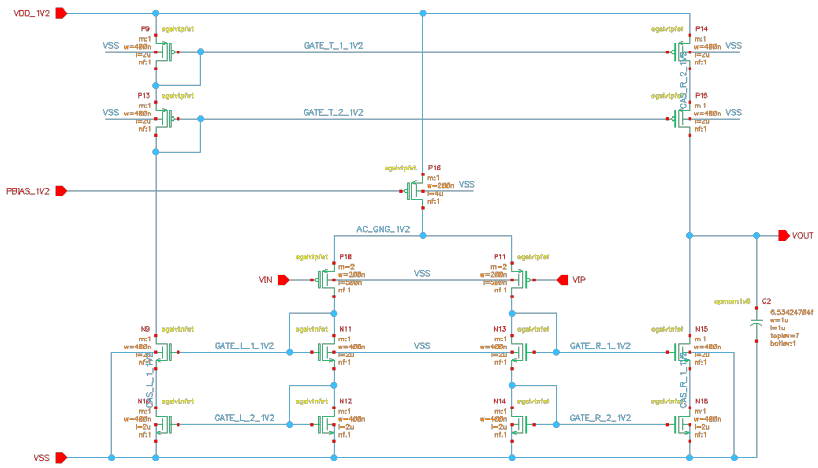


Figure A.6: Schematic of MAIN_OTA_1V2 from Fig. A.1 including device sizes.

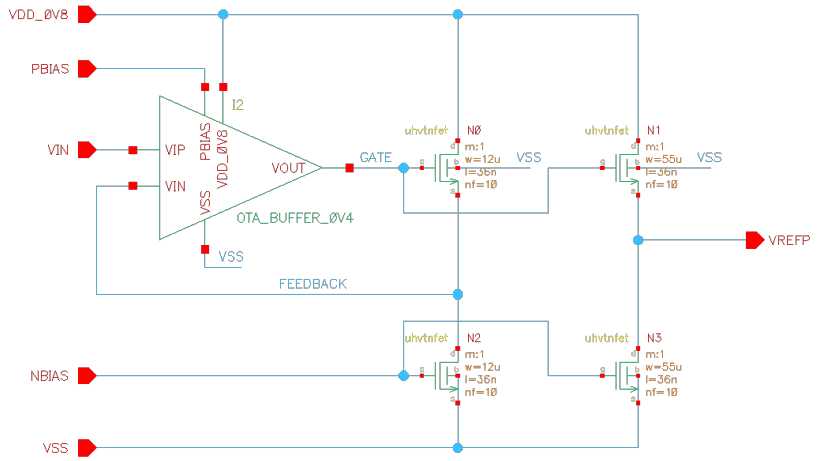


Figure A.7: Schematic of BUFFER_0V4 from Fig. A.1 including device sizes.

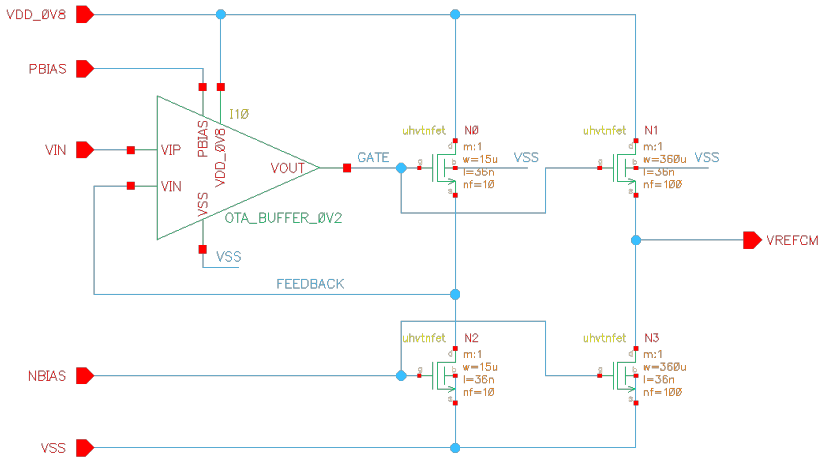


Figure A.8: Schematic of BUFFER_0V4 from Fig. A.1 including device sizes.

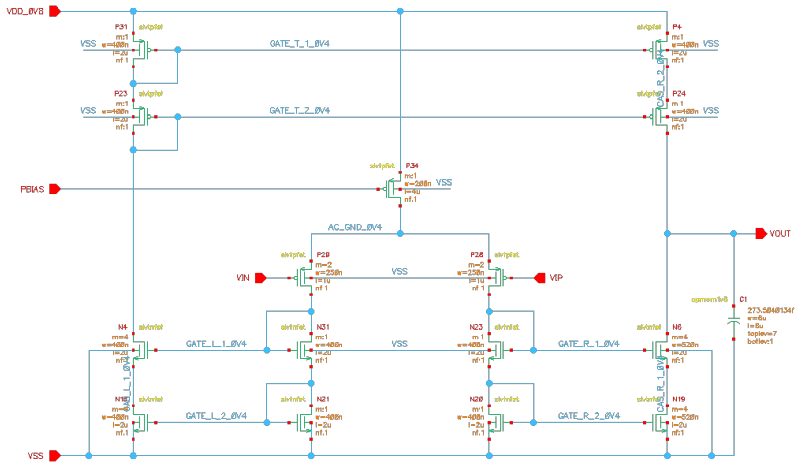


Figure A.9: Schematic of OTA_BUFFER_0V4 from Fig. A.7 including device sizes.

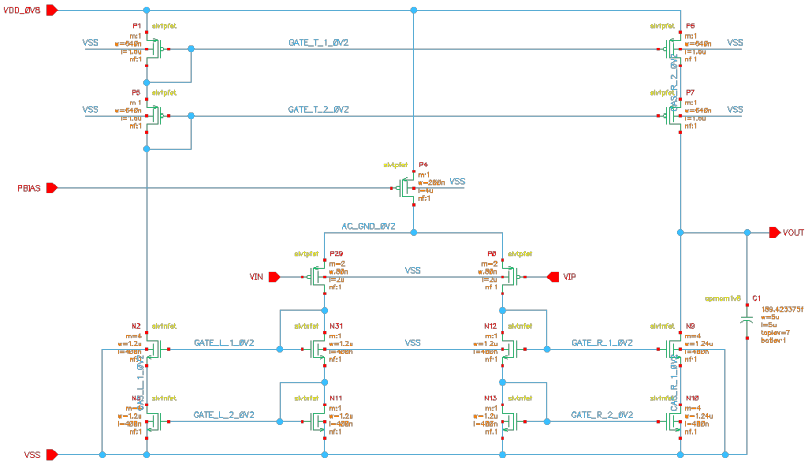


Figure A.10: Schematic of OTA_BUFFER_0V2 from Fig. A.8 including device sizes.

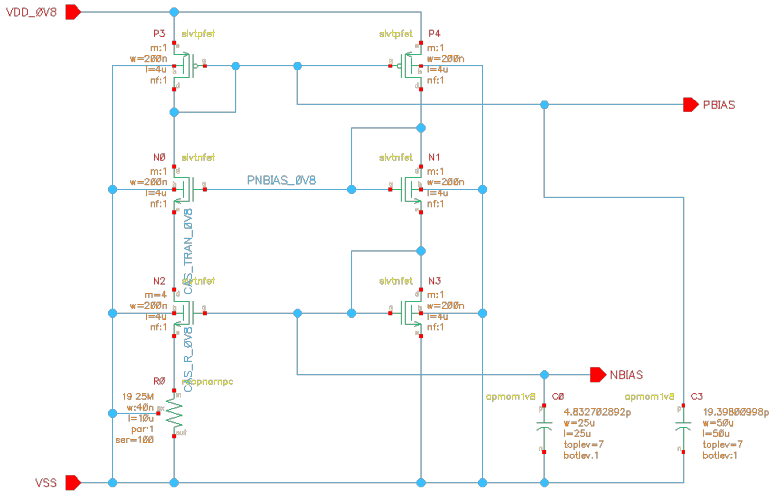


Figure A.11: Schematic of the $CONSTANT-TRANSCONDUCTANCE$ circuit from Fig. 4.1 including device sizes.

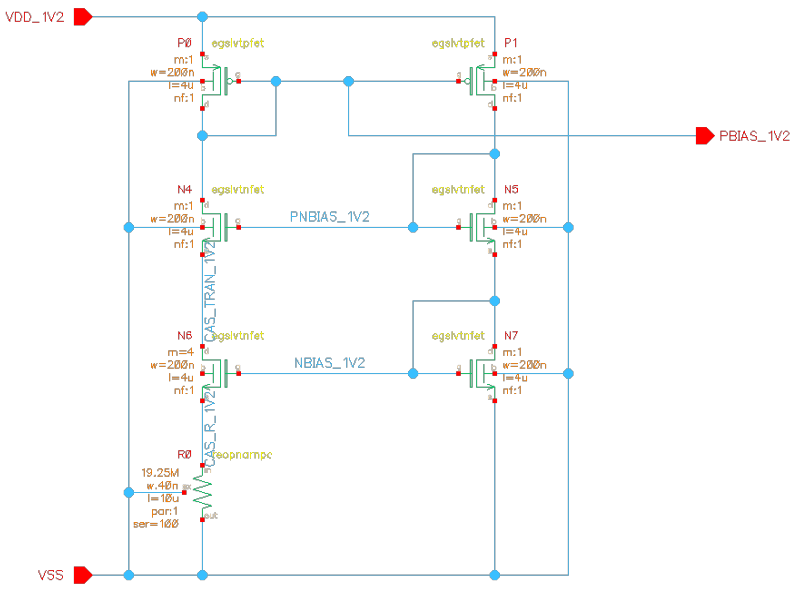


Figure A.12: Schematic of the $CONSTANT-TRANSCONDUCTANCE\_1V2$ circuit from Fig. 4.1 including device sizes.

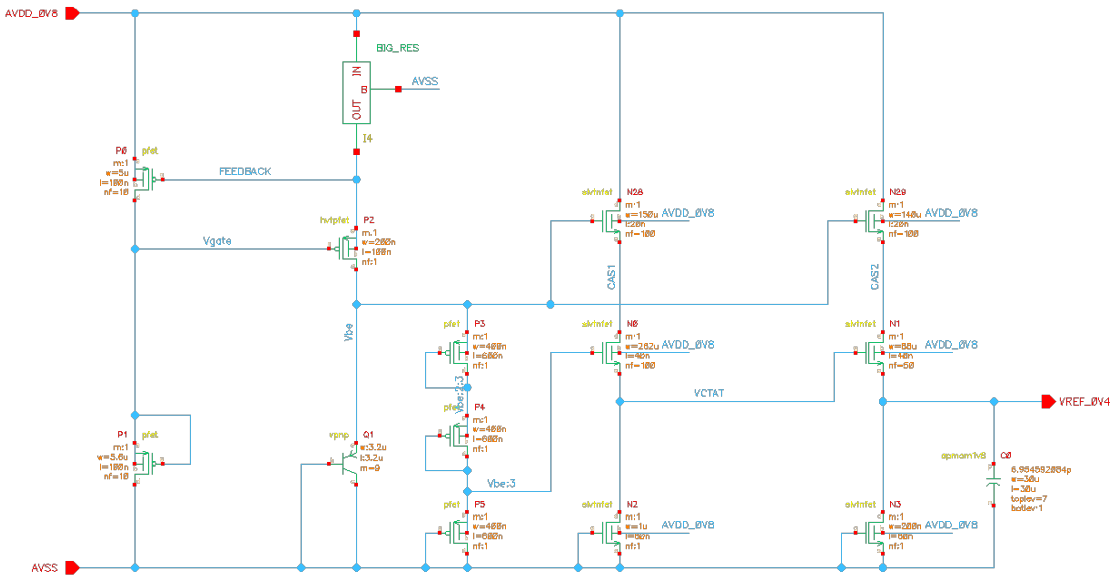


Figure A.13: Schematic of the *BANDGAP_REFERENCE* circuit from Fig. 4.1 including device sizes.

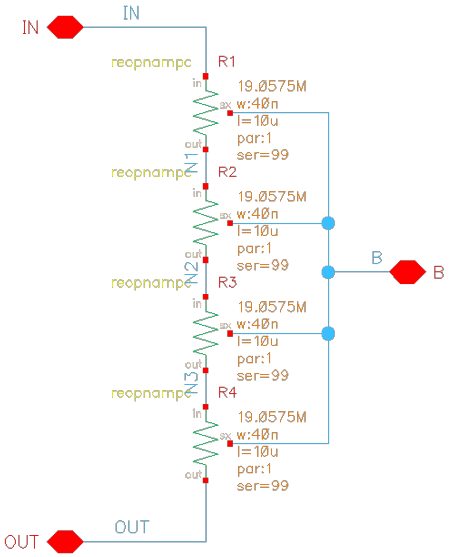


Figure A.14: Schematic of the BIG_RES resistor from Fig. A.13 including device sizes.

B Layout of different circuit components

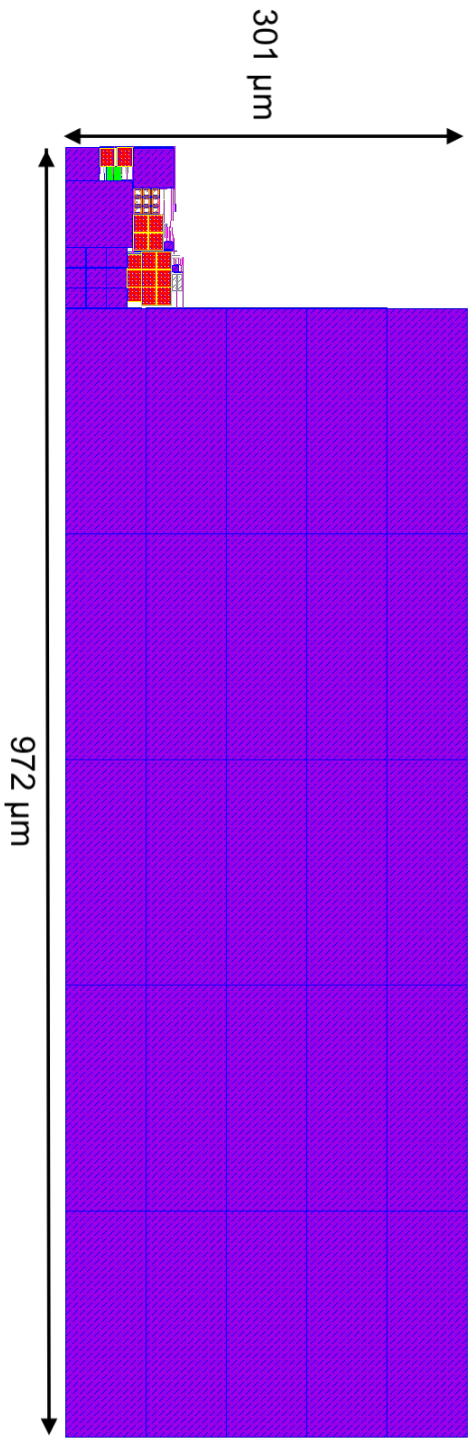


Figure B.15: Layout of the reference generator system including on-chip decoupling capacitors.

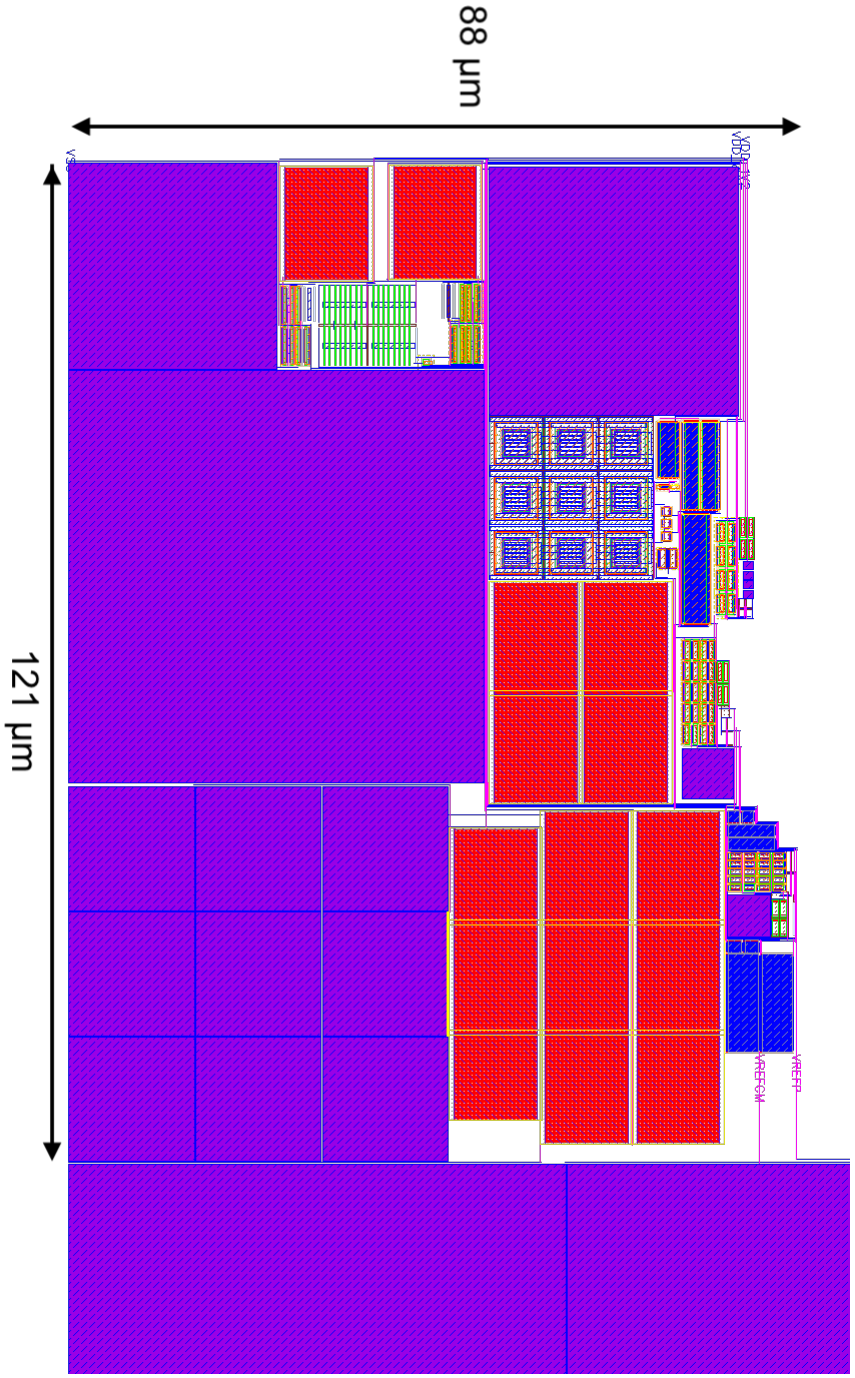


Figure B.16: Layout of the reference generator system excluding on-chip decoupling capacitors.

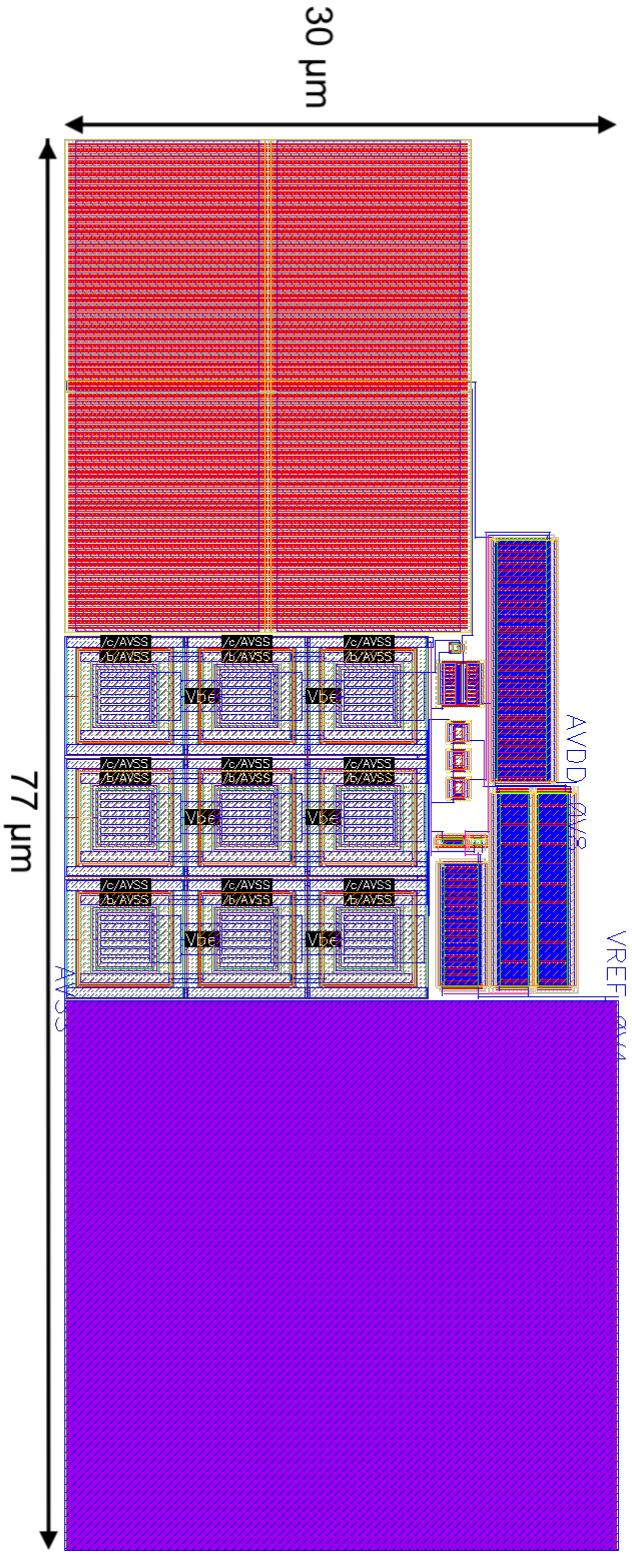


Figure B.17: Layout of the *BANDGAP REFERENCE*.

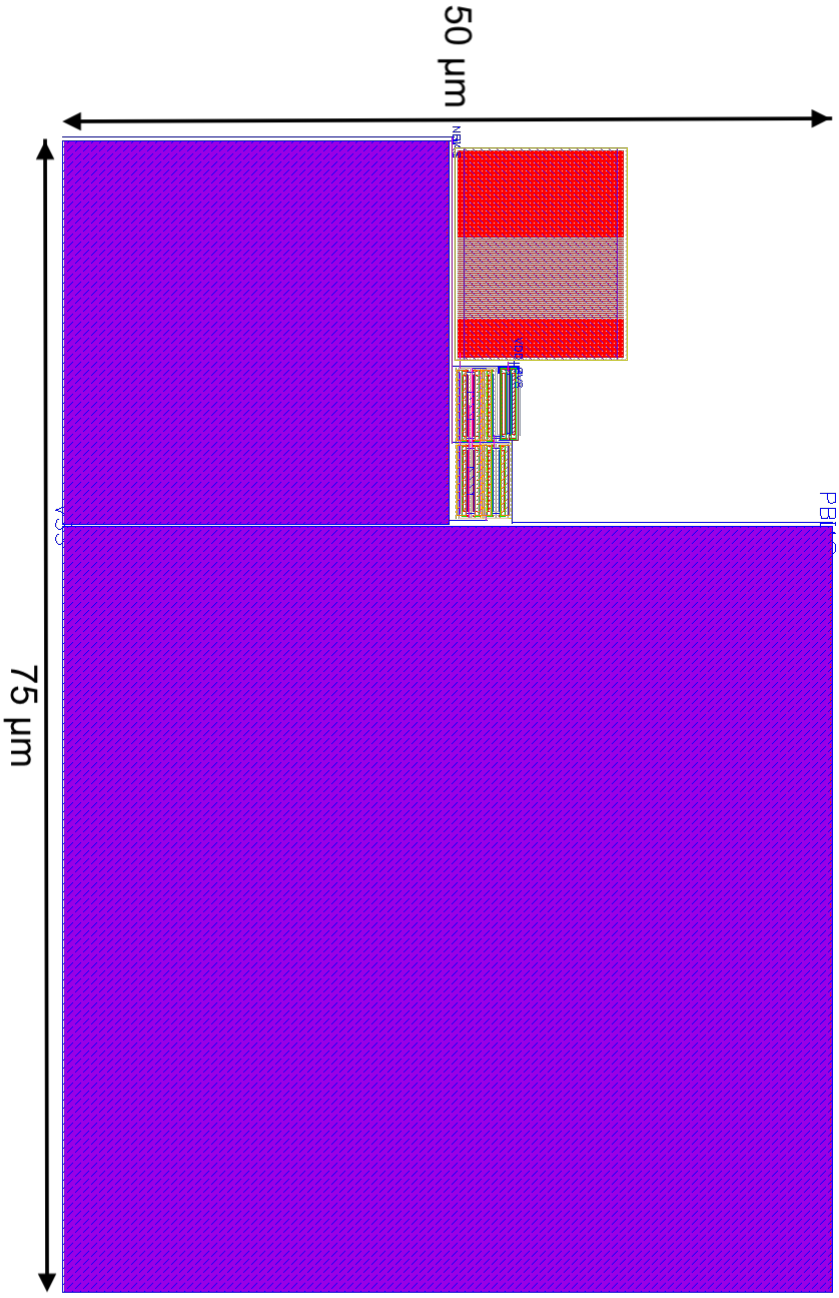


Figure B.18: Layout of the $CONSTANT - TRANSCONDUCTANCE$ circuit.

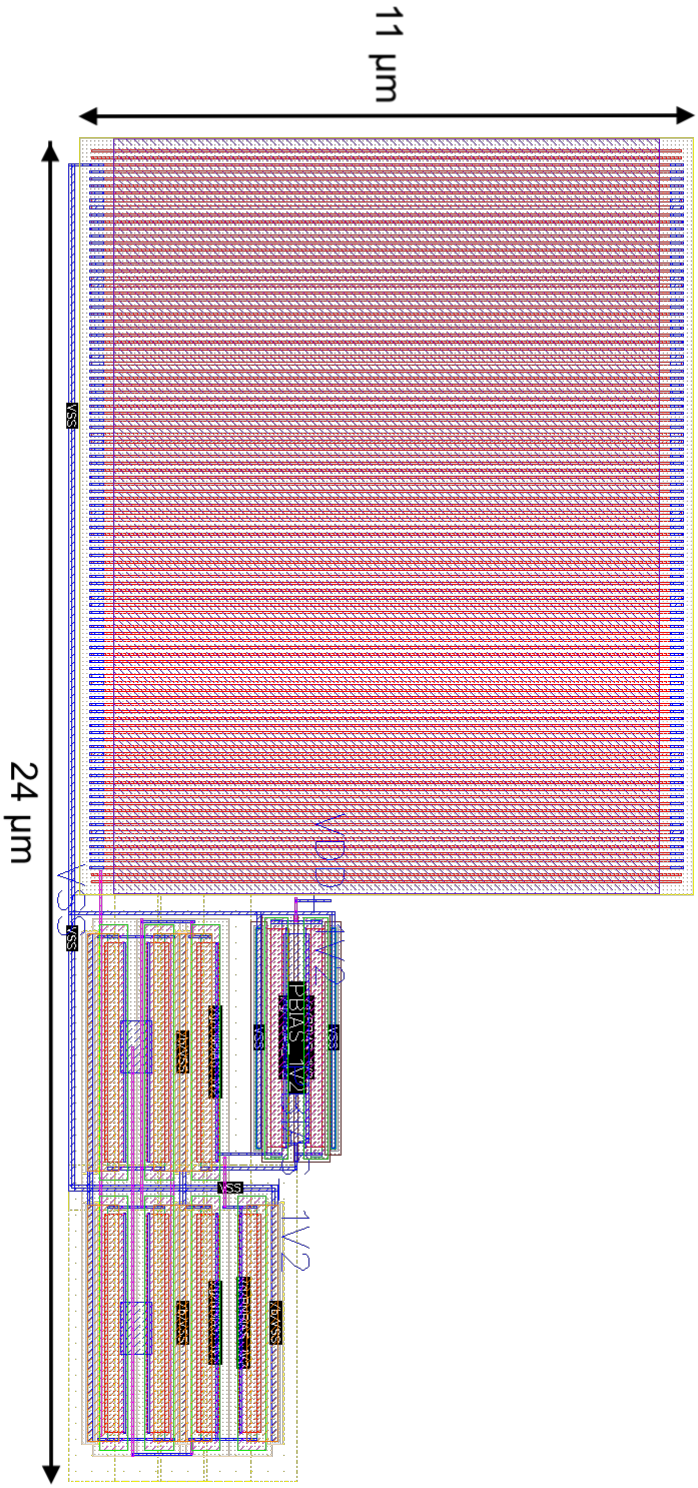


Figure B.19: Layout of the $CONSTANT - TRANSCONDUCTANCE$ $1V2$ circuit.

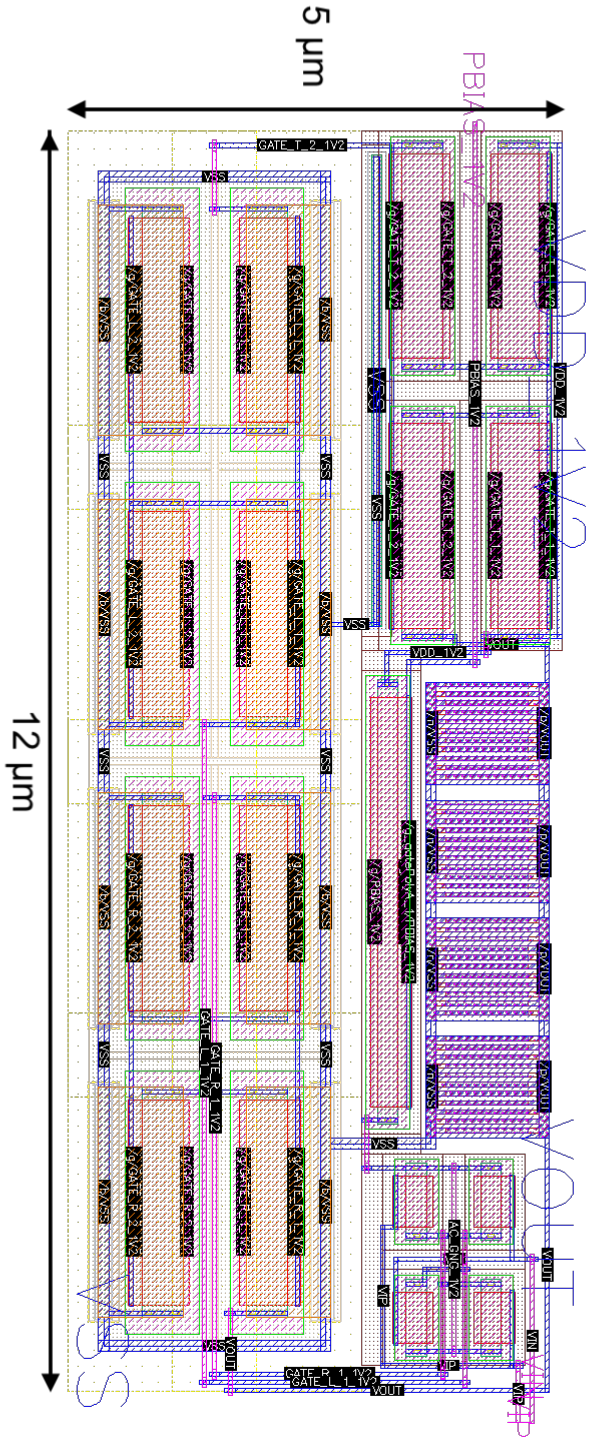


Figure B.20: Layout of the $MAIN\ OTA$.

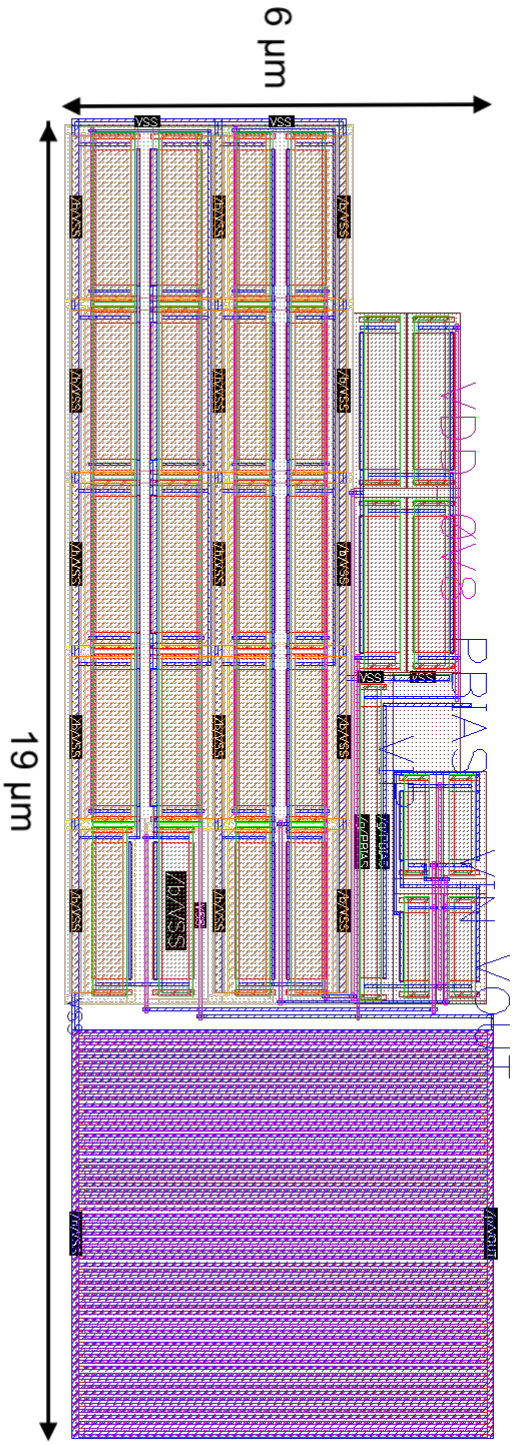


Figure B.21: Layout of the $VREFP\ OTA$.

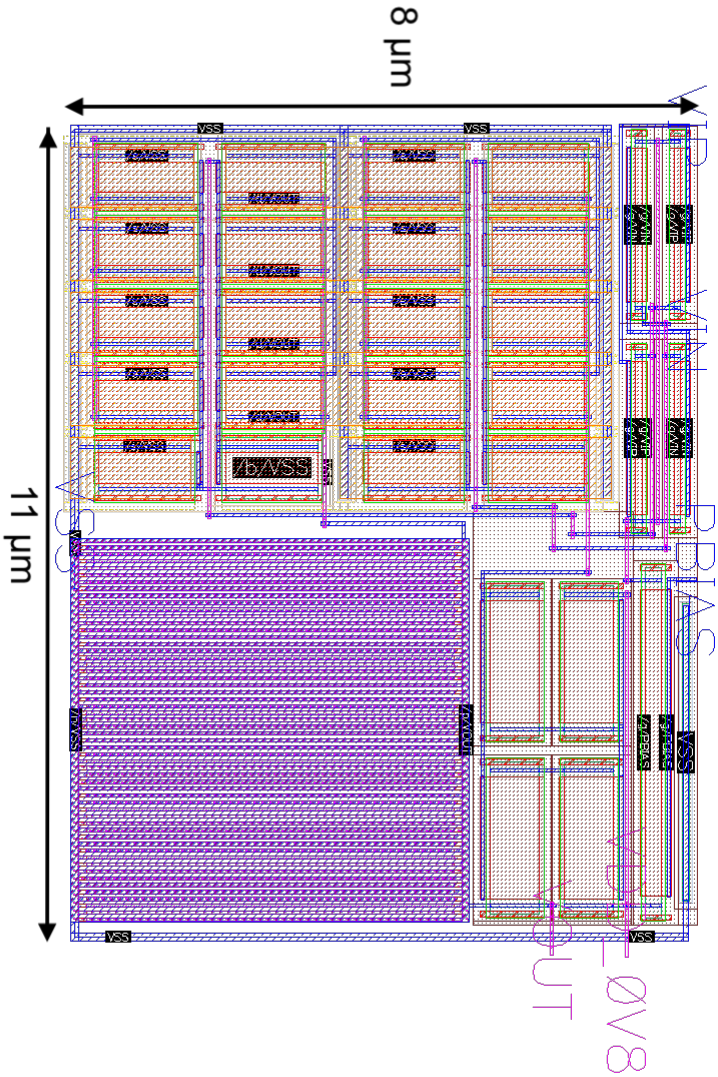


Figure B.22: Layout of the $VREFCM\ OTA$.

C Testbenches

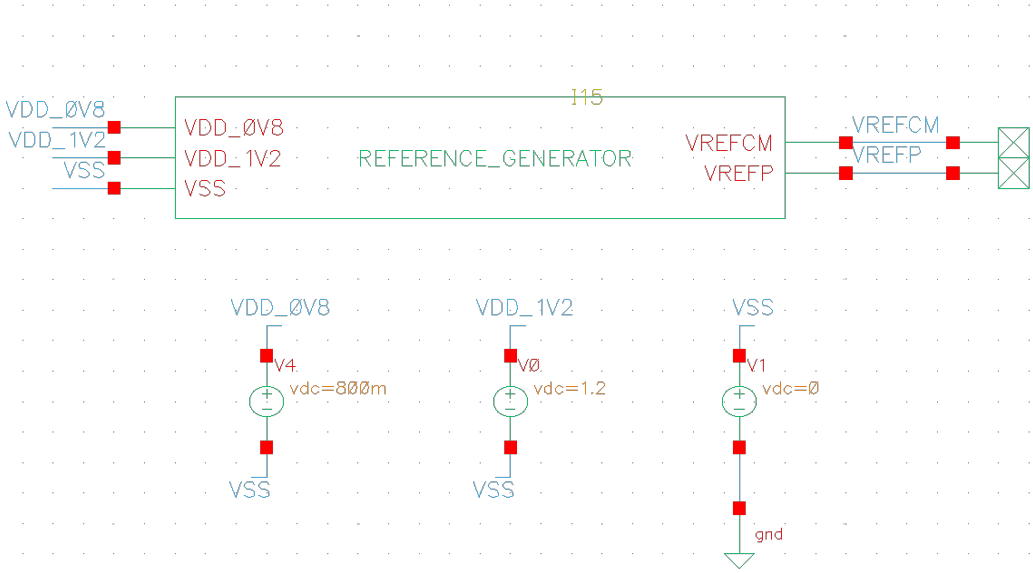


Figure C.23: Illustration of the testbench used to obtain both the DC and noise results of the reference generator.

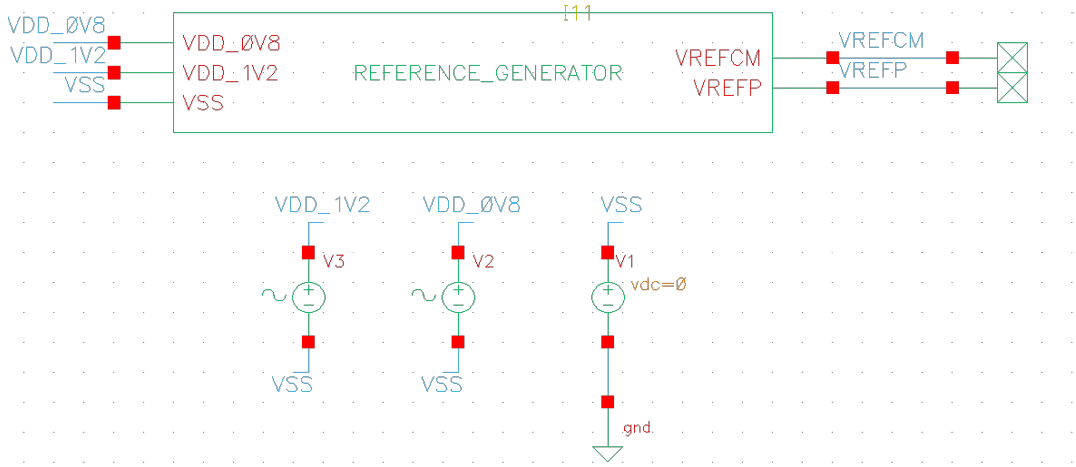


Figure C.24: Illustration of the testbench used to obtain the PSRR results of the reference generator.

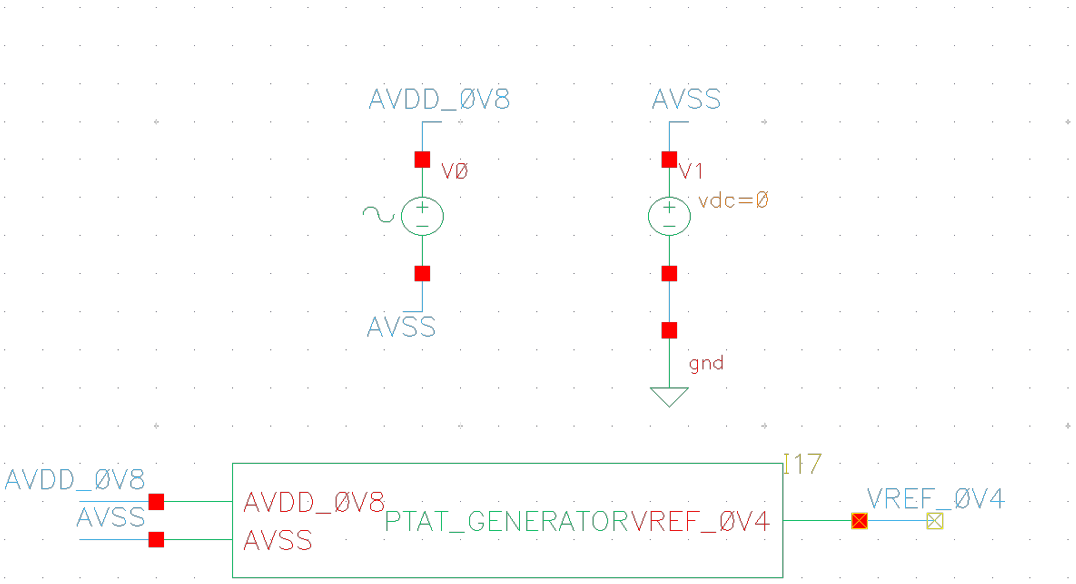


Figure C.25: Illustration of the testbench used to obtain the PSRR results of the bandgap reference.

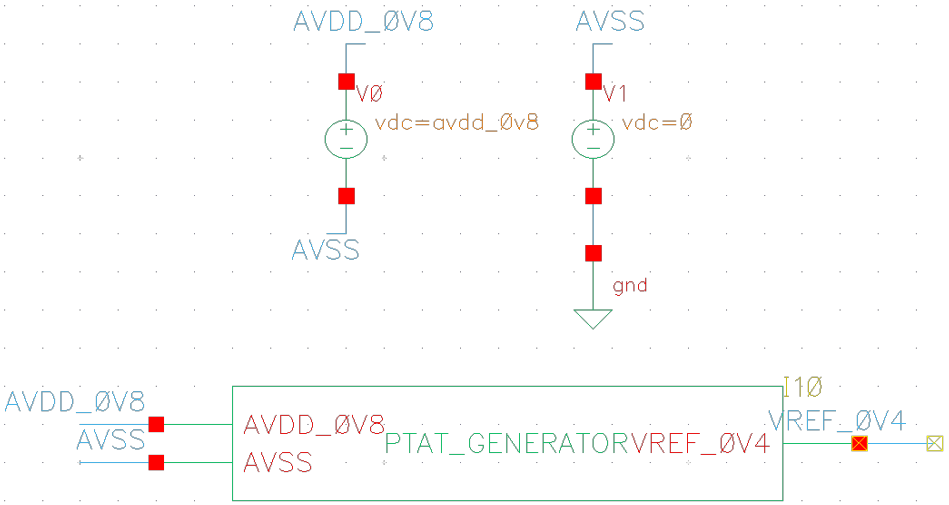


Figure C.26: Illustration of the testbench used to obtain both the DC and noise results of the bandgap reference.

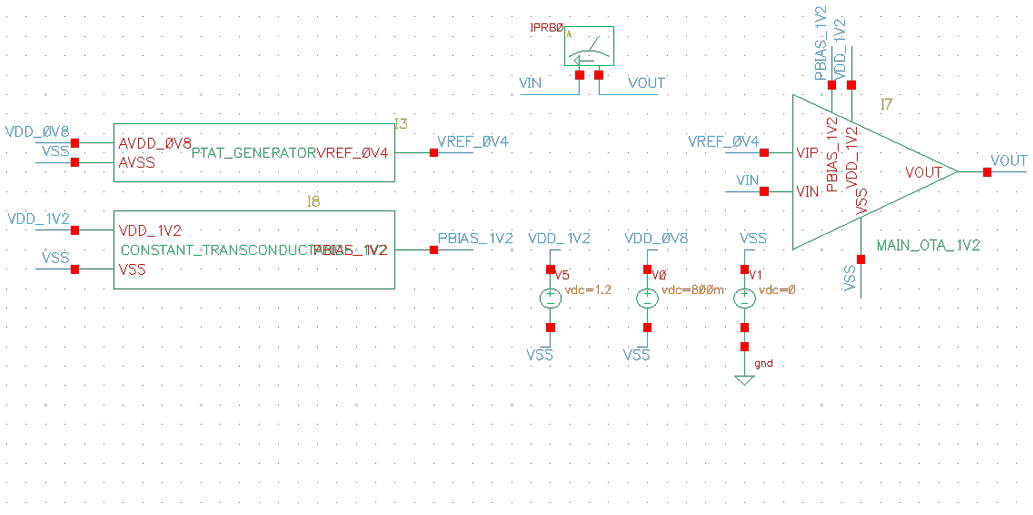


Figure C.27: Illustration of the testbench used to obtain the AC results of the *MAIN OTA*. For the test including the effect of the output network, the *IPROB0* is connected between the source of transistor N_1 and the negative input terminal of the *MAIN OTA* in Fig. 4.2.

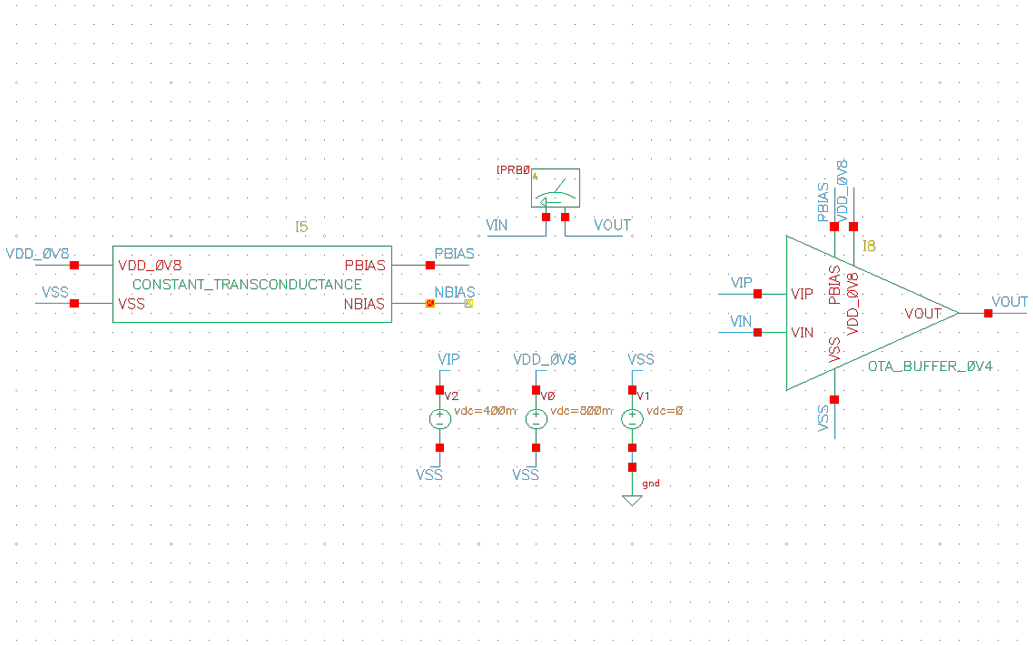


Figure C.28: Illustration of the testbench used to obtain the AC results of the *VREFP OTA*. For the test including the effect of the output network, the *IPROB0* is connected between the source of transistor N_1 and the negative input terminal of the *SYMMETRICAL OTA* in Fig. 4.3.

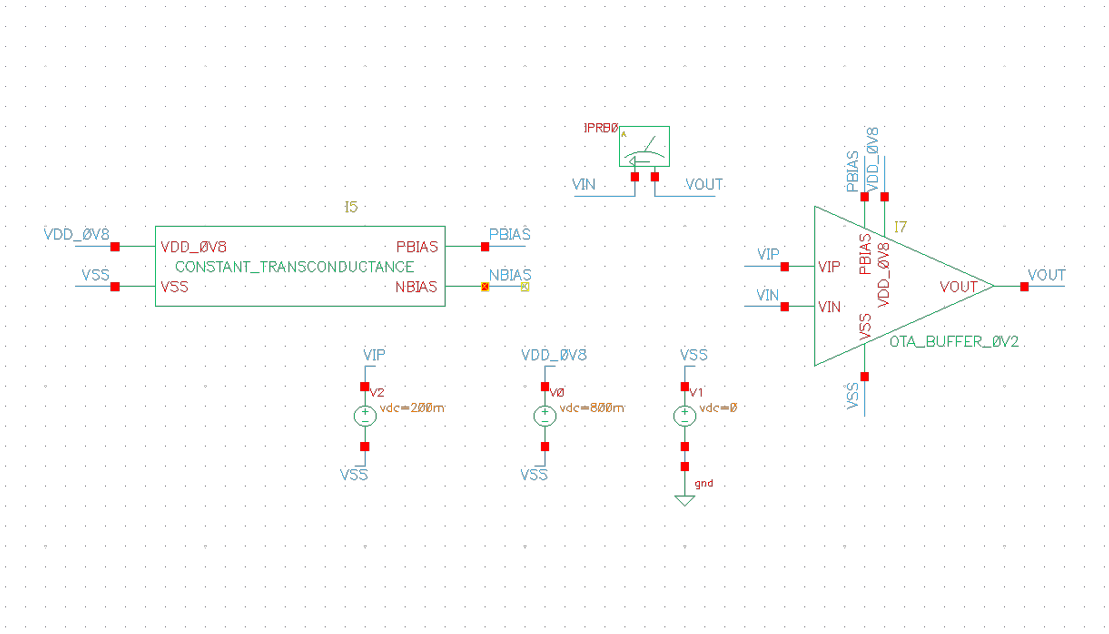


Figure C.29: Illustration of the testbench used to obtain the AC results of the $VREFCM\ OTA$. For the test including the effect of the output network, the $IPROB0$ is connected between the source of transistor N_1 and the negative input terminal of the $SYMMETRICAL\ OTA$ in Fig. 4.3.

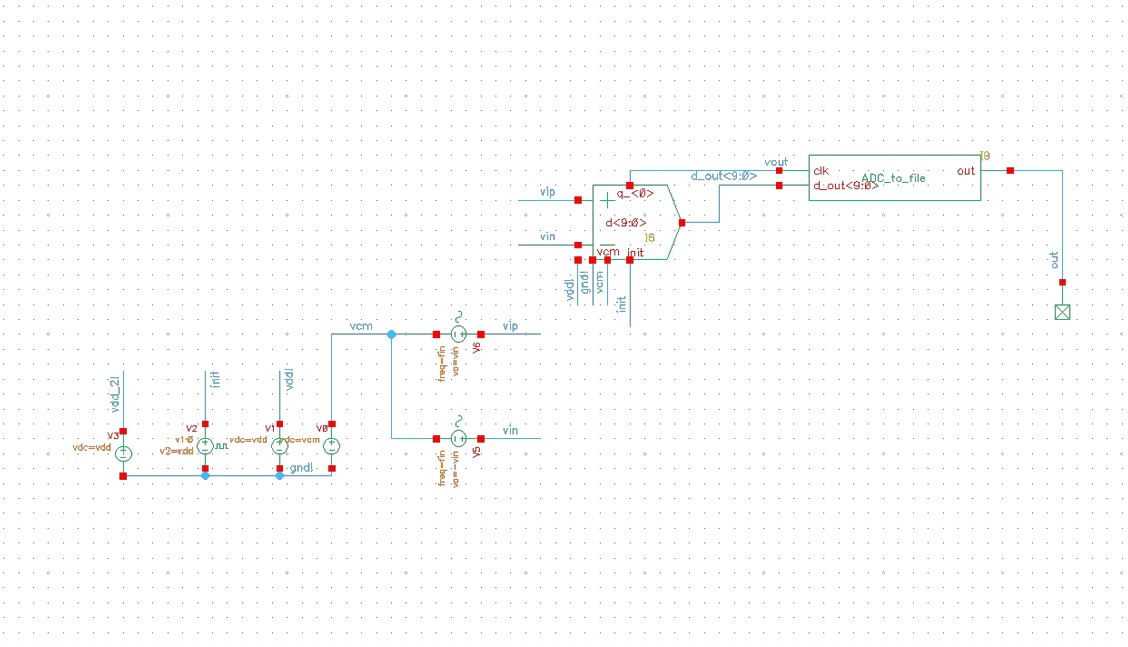


Figure C.30: Illustration of the testbench used to obtain the transient results of the SAR-ADC with ideal voltage sources as references.

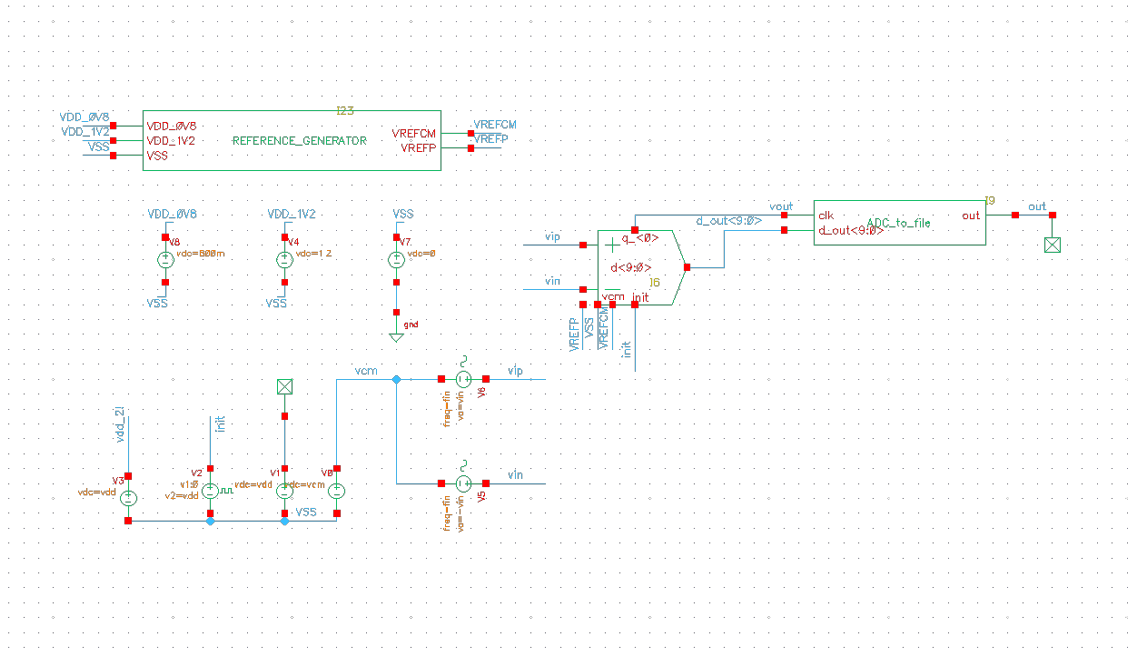
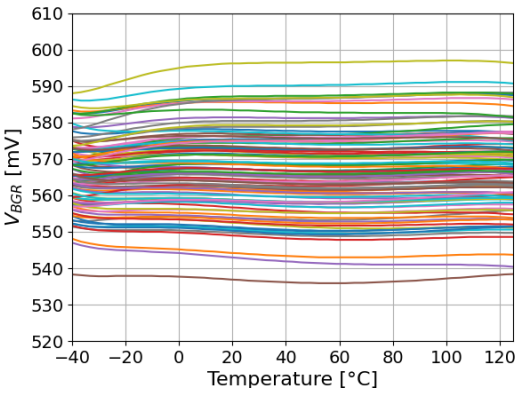
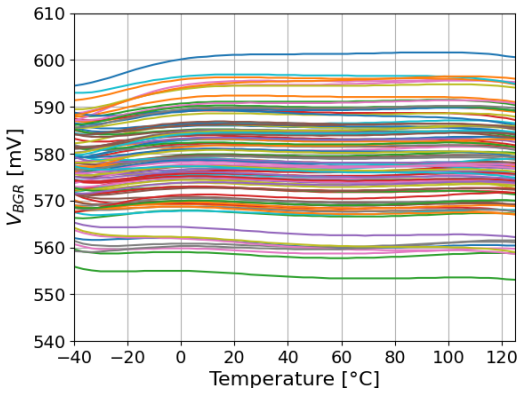


Figure C.31: Illustration of the testbench used to obtain the transient results of the SAR-ADC utilizing the reference generator.

D Monte Carlo simulation plots

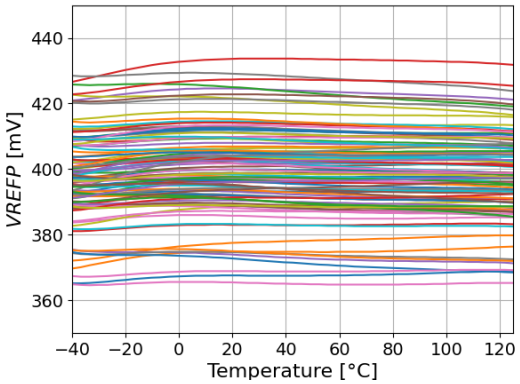


(a) Schematic simulation of V_{BGR}.

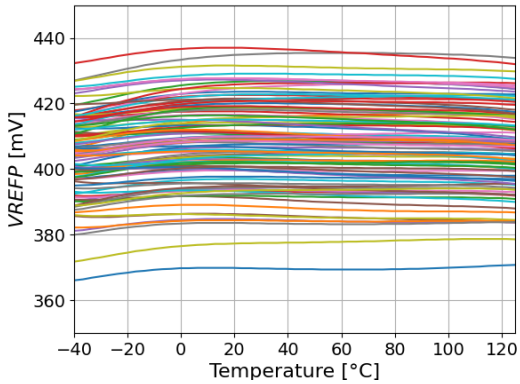


(b) Layout simulation of V_{BGR}.

Figure D.32: 100 run Monte Carlo simulation of V_{BGR}.

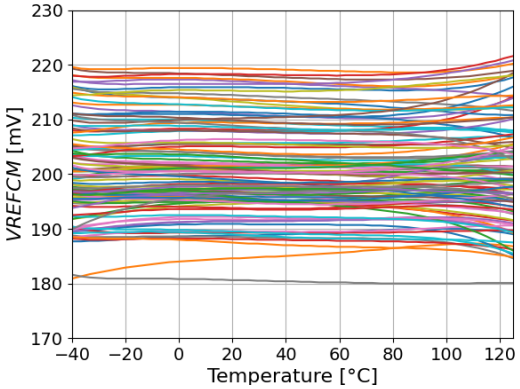


(a) Schematic simulation of $VREFP$.

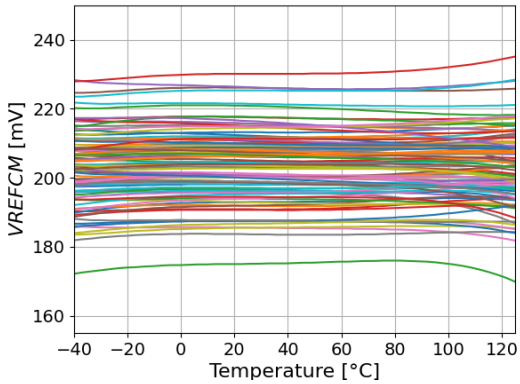


(b) Layout simulation of $VREFP$.

Figure D.33: 100 run Monte Carlo simulation of $VREFP$.

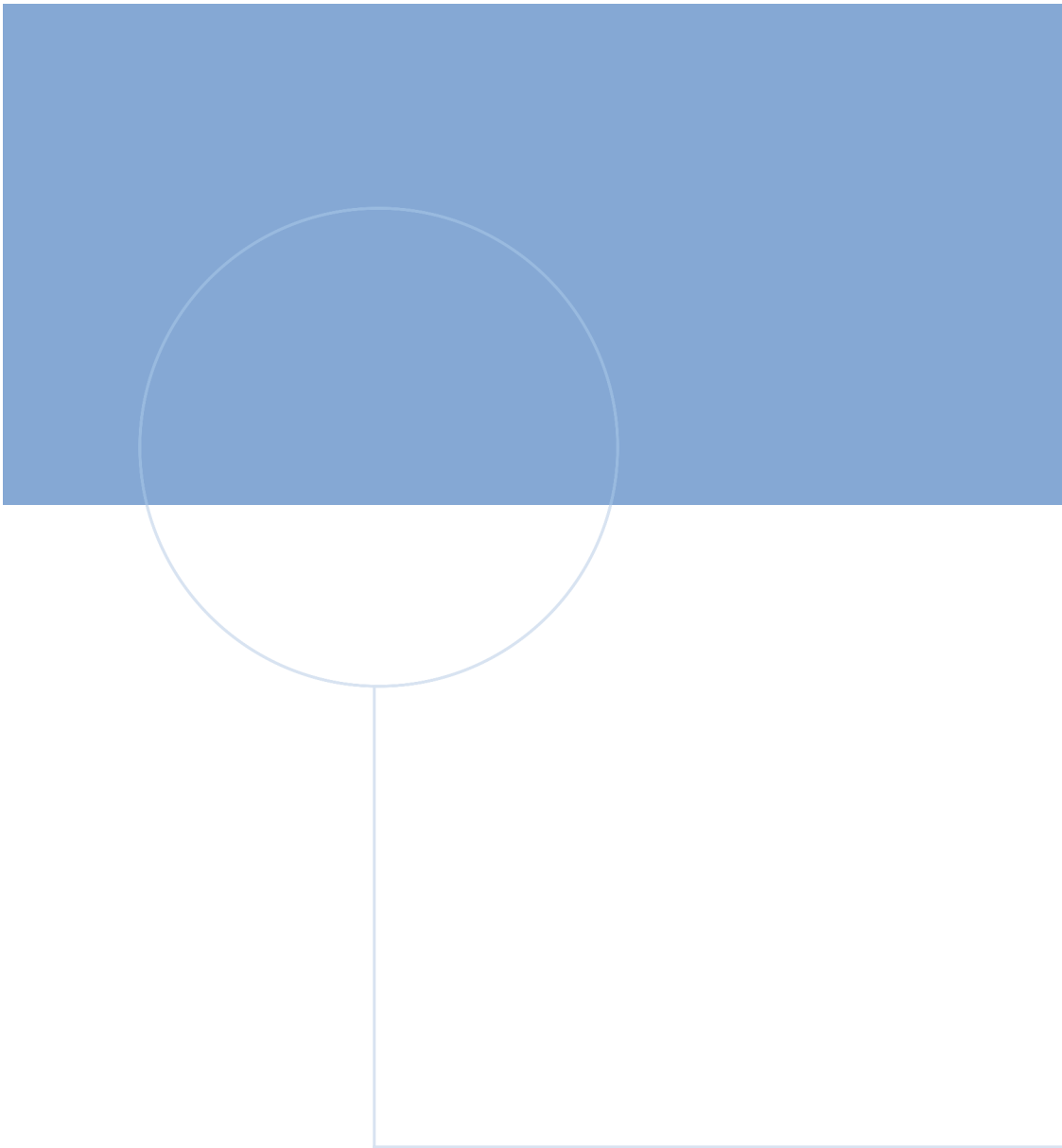


(a) Schematic simulation of $VREFCM$.



(b) Layout simulation of $VREFCM$.

Figure D.34: 100 run Monte Carlo simulation of $VREFCM$.



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