Master's thesis

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Norwegian University of Science and Technology
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Department of Electronic Systems

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Inverter-based OTA for a control-bounded ADC

Master's thesis in Electronics Systems Design and Innovation
Supervisor: Trond Ytterdal
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Abstract

This project covers the design of an operational transconductance amplifier (OTA) in 22nm FDSOI technology, for the purpose of using it in a Control-bounded Analog-to-Digital converter. Fully depleted silicon on insulator (FDSOI) is a transistor technology that makes it possible to scale down devices further than traditional bulk CMOS. The big issue with scaling down bulk CMOS is leakage current. FDSOI uses a buried oxide layer to reduce this. Control-bounded ADCs are made up of a chain of integrators with a digital controller connected in feedback. The aim of the ADC is to make analog to digital conversion of weak signals more power-efficient.

To address this, an inverter-based pseudo-differential OTA was designed. The simulated circuit implementation shows that the amplifier, in the nominal corner, has a DC gain of 70.47dB, a unity gain frequency of 720MHz, and an input-referred noise of 6.3nV/$\sqrt{\text{Hz}}$ at 1MHz. In some of the process corners, the amplifier does not meet the gain and bandwidth specifications, but it meets the noise requirement in all corners. To further test the circuit's performance, it was implemented in layout. It uses an area of 35.3μm^2, and post-layout simulations showed that it achieved a DC gain of 66.61dB, a unity gain frequency of 667.8MHz, and an input-referred noise of 6.3nV/$\sqrt{\text{Hz}}$ at 1MHz. Future research should try to implement a compensation circuit to reduce the effects of process variations, for example, by adding an adaptive body bias.

Sammendrag

Dette prosjektet tar for seg designet av en OTA i 22nm FDSOI teknologi. Hensikten er å lage en modul som skal brukes i en kontrolbegrenset analog-til-digital omformer. FDSOI er en transistor teknologi som gjør det mulig å skalere ned enheter i større grad enn det som er mulig med Bulk CMOS. Den store utfordringen med å skalere ned bulk CMOS er lekkasjestrømmer. FDSOI benytter et begravd oksidlag for å redusere dette. En kontrolbegrenset A/D omformer er bygd opp av en kjede av integratorer, med en digital kontroller koblet i en tilbakekoblingssløyfe. Hensikten er å kunne gjøre analog til digital omforming av svake signaler mer energi effektivt.

For å ta tak i dette ble en inverterer-basert pseudodifferensiell OTA laget. Fra de simulerte kretsimplementasjonene ble det funnet at forsterkeren hadde en DC forsterkning på 70.47dB, en frekvens for enhetsforsterkning på 720MHz, samt en inngangsreferert støy på 6.3nV/$\sqrt{\text{Hz}}$ ved 1MHz i nominelt hjørne. I noen av prosesshjørnene klarte ikke forsterkeren å nå spesifikasjonene for forsterkning og båndbredde, men den nådde støykravet i alle hjørner. For å videre teste forsterkeren ble den implementert som utlegg. Den bruker et areal på 35.3μm^2, og simuleringer av utlegget viste at den oppnådde en forsterkning på 66.61dB, en frekvens for enhetsforsterkning på 667.8MHz, samt en inngangsreferert støy på 6.3nV/$\sqrt{\text{Hz}}$ ved 1MHz. Fremtidig forskning burde prøve å implementere en form for kompensasjonskrets for å redusere påvirkning av prosess variasjoner, for eksempel en adaptiv body-bias krets.

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1 Introduction

1.1 Background

Engineers always try to make smaller, faster, and more energy-efficient circuits. One of the circuits that is always subject to improvement is the Analog-to-digital converter (ADC). For example, improvements can be made by using smaller transistors or implementing new design concepts. The precise goal of improvement varies from design to design, but a common goal is low power consumption and low noise.

The concept of control-bounded ADCs were recently proposed in [1], [2]. The architecture tries to combat the issue of high power consumption used in analog-to-digital conversion. It aims to be a good candidate for digitalizing weak signals, like a sensor output. The performance will depend on two main factors: the analog system's gain and how well the digital controller bounds the internal voltage and current signals [3].

Continuous-time integrators, such as active RC integrators, are needed to implement a control-bounded ADC. This integrator uses capacitive feedback to perform the integration of current upon a capacitor. They achieve higher linearity than their Gm-C counterparts. However, the RC integrator also has a higher current consumption since the internal operational transconductance amplifier (OTA) requires a unity gain bandwidth much higher than the integrator itself. Nevertheless, they are easy to implement and can be designed for single-ended and fully differential operations.

When implementing low-power designs, an inverter-based amplifier might be a good choice. They have high energy efficiency and can operate with low supply voltage. One of the main disadvantages is that they have a low tolerance to Process, Voltage, and Temperature (PVT) variations. They also have reduced common mode rejection ratio (CMRR), and power supply rejection ratio (PSRR) [4].

New fabrication methods like Fully depleted silicon on insulator (FDSOI) make it possible to reduce transistor size without inducing high leakage currents. FDSOI also allows a high degree of body biasing and includes several transistor classes for different threshold voltages. Compared to traditional CMOS bulk devices, the designer has a higher degree of control when designing low-power circuits.

1.2 Scope

This thesis aims to make an OTA that can be used in an active RC integrator in a control-bounded ADC. The OTA is designed to be used in a Leapfrog ADC, a version of a control-bounded ADC. The ADC is constructed by a chain of integrators. Since the ADC is an existing system, the values of the RC components and load resistance for the integrator were already defined. The input resistance of the integrator is $R_{\beta 1} = 5\text{K}\Omega$, the feedback capacitance is $C_1 = 1.7\text{pF}$, and the load resistance is $R_{\beta 2} = 50\text{K}\Omega$. In addition, the system is fully differential, and FDSOI technology is used. Given this background, the main focus is on the amplifier implementation and making it work under these conditions.

1.3 Specifications

The control-bounded ADC sets the specifications for this project. As mentioned above, the amplifier must operate in a chain of integrators. In addition, the amplifier should fulfill the specifications given in table 1. No specification was given for the power consumption, but it is desirable to minimize it.

Table 1: Specifications for the OTA

Parameter	**Symbol**	**Value**	**Comment**
DC Gain	A_0	500	
Input referred noise	$v_{ni}(f)$	$< 12\text{nV}/\sqrt{\text{Hz}}$	At 1MHz
Max output swing		V_{dd}	Differential, p2p
Unity gain frequency	f_{ug}	500MHz	

1.4 Previous work

Using active RC integrators in a control-bounded ADC has not been explored. However, they are common in continuous time Delta-Sigma modulators, and the use of inverter-based amplifiers in active RC integrators has been studied in [5]–[7]. That being said, these OTA implementations have a lower bandwidth than what is needed for this project. Because of this, an OTA made for a Gm-C integrator was studied as an alternative. The amplifier architecture used was proposed in [8] and [9]. In [8], it achieved a gain of 37.7dB and a unity gain bandwidth of 25GHz. In [9], the implemented design has a higher gain of 52dB but a lower unity gain bandwidth of 3.69GHz.

1.5 Thesis outline

The remainder of this thesis is structured as follows.

Chapter 2 (Theory) introduces control-bounded ADCs, active RC integrators, inverter-based amplifiers, and FDSOI technology. In addition, the design method g_m/I_D is described.

Chapter 3 (Design) covers the design of the integrator. A detailed explanation of the amplifier implementation and transistor sizing is covered, and a description of the layout design is included.

Chapter 4 (Simulation results) presents the results achieved by the amplifier for the nominal corner, process corners, and post-layout simulations.

Chapter 5 (Discussion) discusses the circuit's performance and gives some reasons why some things did not work and how they might be improved. It also includes some suggestions for future work.

Chapter 6 (Conclusion) gives the final conclusion of this thesis.

2 Theory

Some background knowledge is needed to understand the context of this thesis and the design choices. This chapter gives an overview of control-bounded ADCs, active RC integrators, inverter-based amplifiers, and FDSOI technology. In addition, the design method g_m/I_D is explained. It is assumed that the reader has a basic knowledge of analog circuit design.

2.1 Control-bounded ADC

The concept of the control-bounded ADC was proposed in [1], [2]. Illustrated in figure 1 is a Leapfrog ADC, an example of a control-bounded ADC. This thesis gives a simplified explanation of how the ADC operates to give some context for this project.

As illustrated, the ADC architecture is a chain of integrators. The figure only shows two integrators, but in practice, the structure can be repeated N number of times. Each integrator has a digital feedback loop, marked in red in the figure. The feedback will act as a digital controller for the integrator. In addition, a feedback resistor is added between neighbouring integrators, marked in blue. The resistor enables complex poles in the transfer function of the analog system.

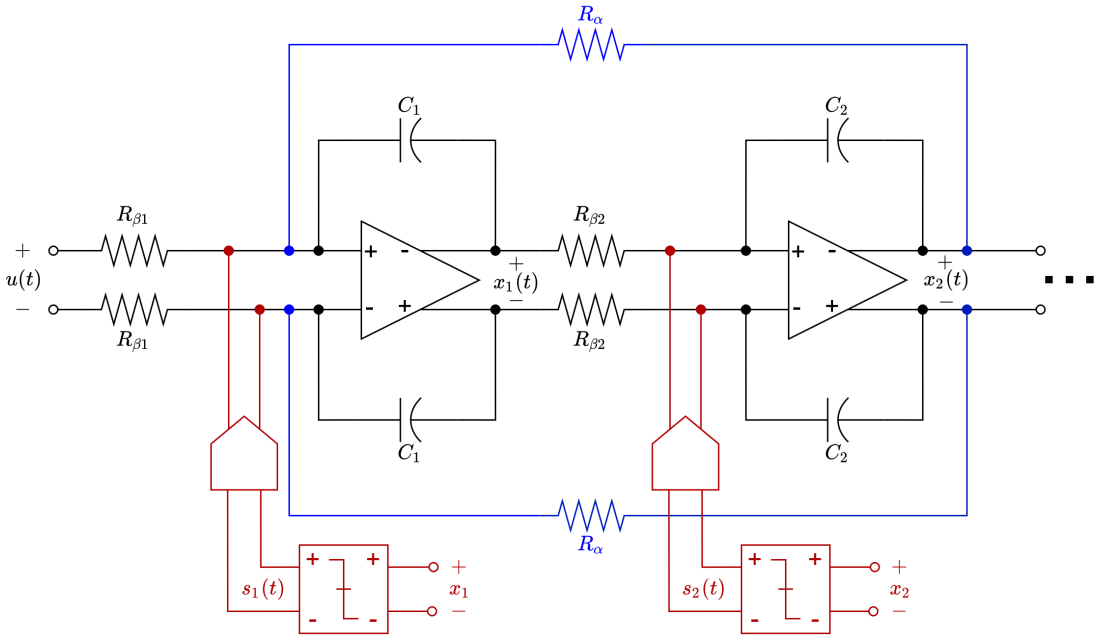


Figure 1: Illustration of a Leapfrog ADC

When a signal $u(t)$ is applied to the input, the digital controller will first observe the output of the integrator $x_i(t)$. The controller will then try to force the output $x_i(t)$ to zero by applying a control signal $s_i(t)$ to the input of the integrator. This is done for each of the N number of integrators in the chain. A digital output can then be found by observing what the controller did and applying a digital filter

that determines which input most likely triggered the observed sequence of control signals $s(t)$.

Because of the architecture of the ADC, the noise of the first integrator in the chain will heavily affect the total performance. Because of this, the noise in the first integrator is a crucial parameter when it is designed.

2.2 Active RC integrators

A type of integrator that can be used in control-bounded ADCs is the active RC integrator. Figure 2 shows a simple single-ended version of an RC integrator. Assuming an ideal opamp, node V_x will keep virtual ground during the operation. The integration works by having resistor R convert the input voltage V_{in} to current. This current is then summed up in the capacitor C_1, and the inverted output appears at V_{out} [10].

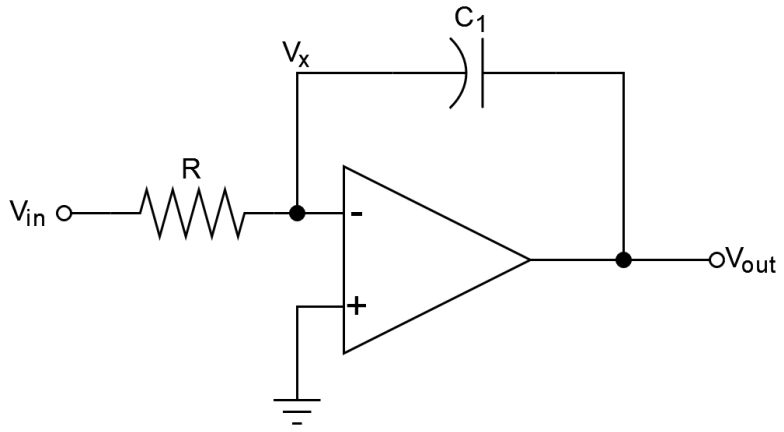


Figure 2: Active RC integrator

The resistor's size will determine the gain in the voltage to current conversion, and since this is a passive element, it will achieve good linearity. The size of the capacitor will, together with the resistor, determine the bandwidth of the integrator. Equation 1 defines the bandwidth of the RC integrator ω_0, given an amplifier with finite gain A_0.

$$\omega_0 = \frac{1}{A_0 RC} \tag{1}$$

2.3 Inverter based amplifiers

Inverter-based amplifiers are convenient building blocks when implementing energy-efficient amplifiers. They are easy to design, and given the figure of merit (FoM) in equation 2, they have a significantly higher energy efficiency compared to other common amplifier topologies [11]. Additionally, they can achieve a decent slew rate with a given power consumption since they can operate as dynamic amplifiers.

$$FoM = \frac{GBW \cdot C_L}{I_{Total}} \tag{2}$$

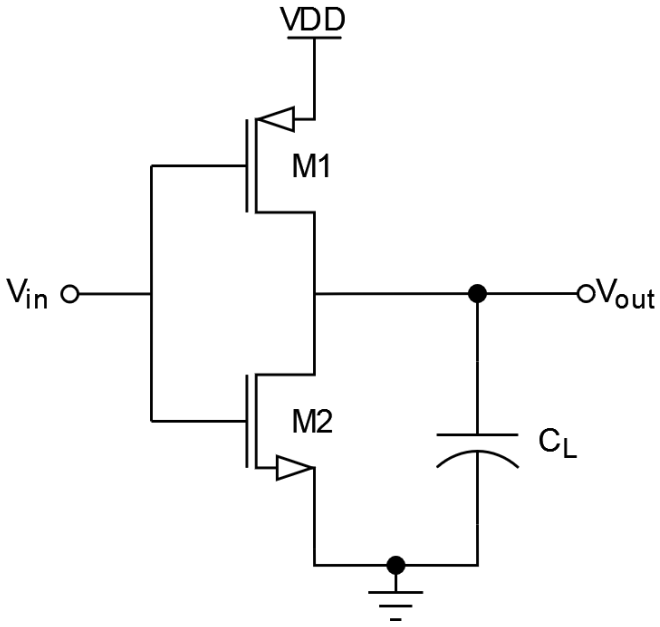


Figure 3: Inverter stage

Figure 3 shows a single inverter stage. The gain of the inverter can be found using small signal analysis. It is given in equation 3. Where g_{m1} and g_{m2} are the transconductance of the PMOS and the NMOS transistor, respectively. The output resistance R_o is given by the parallel combination of the output resistance r_{ds} in the transistors.

$$A_0 = -R_o(g_{m1} + g_{m2}) \tag{3}$$

The bandwidth of the inverter stage is found by analyzing the poles and zeros of the system's transfer function. They are given in equation 4 and 5. In the equations, C_{gd} and C_{bd} are the intrinsic capacitances between gate and drain, and body and drain in the two transistors. C_L refers to the load capacitance of the stage, and g_{ds} is the output conductance of the transistors.

$$p = \frac{-(g_{ds1} + g_{ds2})}{C_L + C_{gd1} + C_{gd2} + C_{bd1} + C_{bd2}} \tag{4}$$

$$z = \frac{g_{m1} + g_{m2}}{C_{gd1} + C_{gd2}} \tag{5}$$

Assuming $z >> p$, the inverter will have a first order response, where the pole defines the cutoff frequency. The unity gain frequency of the inverter can be found using the relationship in equation 6, where A_0 is the small signal gain defined above.

$$\omega_{ug} \cong A_0 \omega_p \tag{6}$$

Equation 7 gives the unity gain frequency of the inverter. It is assumed that the load capacitance value is much higher than the sum of the intrinsic capacitances $C_L >> C_{gd1} + C_{gd2} + C_{bd1} + C_{bd2}$.

$$\omega_{ug} = -R_o(g_{m1} + g_{m2}) \cdot \frac{g_{ds1} + g_{ds2}}{C_L + C_{gd1} + C_{gd2} + C_{bd1} + C_{bd2}} \approx \frac{g_{m1} + g_{m2}}{C_L} \tag{7}$$

The linearity of the V-I conversion in the inverter pair is determined by the matching of $\beta = \frac{\mu C_{ox} W}{L}$ in the PMOS and NMOS transistor [12]. The output current of the stage is defined in equation 8, given that both transistors are in saturation and strong inversion. V_{tp} and V_{tn} are the threshold voltage of the PMOS and NMOS, respectively. From this, it can be observed that the conversion will not be linear if $\beta_n \neq \beta_p$.

$$I_{out} = a(V_{in} - V_{tn})^2 + b \cdot V_{in} + c \tag{8}$$

$$a = \frac{1}{2}(\beta_n - \beta_p) \tag{8a}$$

$$b = \beta_p(V_{dd} - V_{tn} - V_{tp}) \tag{8b}$$

$$c = \frac{1}{2}\beta_p(V_{tn}^2 - (V_{dd} + V_{tp})^2) \tag{8c}$$

One of the limitations when using inverter stages is the low gain. The standard way to address this is by adding cascodes. If the design is for low-power applications, this is not ideal since it reduces headroom. With the inverter stage, there are other possible solutions to this issue. One example is adding a negative resistance to the inverter output [12]. This is done by adding auxiliary inverters, as shown in blue in figure 4. It should be mentioned that no internal nodes are added to the circuit, so the system's bandwidth does not suffer. Equation 9 gives the small signal gain of the modified inverter, where g_m and R_o is the transconductance and intrinsic output resistance of the inverter. R_{load} is the negative resistance added by the auxiliary inverters. The equation shows that the inverter gain will be boosted by the load R_{load}. It should be noted that the stability of the circuit might break down if $R_o = -R_{load}$. Consequently, R_o should always be smaller than R_{load} to maintain stability.

$$A_0 = g_m \cdot (R_o \| R_{load}) \tag{9}$$

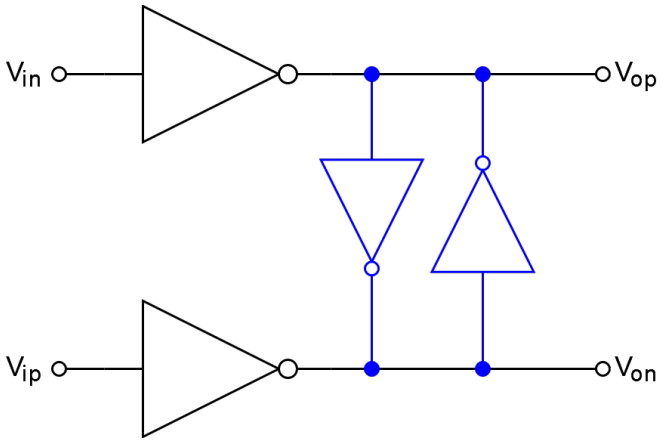


Figure 4: Inverter stage with added negative resistance

2.4 gm/ID method

The g_M/I_D method is a design methodology for determining transistor sizes in a circuit. It was proposed in [13]. It is a popular tool since it is better at modeling weak and moderate inversion than the square law model. It is also a more accurate method since it uses measurable values in the transistor.

As the name suggests, the g_m/I_D method uses the relationship between the ratio of the transconductance g_m, the dc drain current I_D, and the normalized drain current $I_D/(W/L)$ as a tool for sizing CMOS circuits. It is a good tool because g_m/I_D is closely related to the performance of analog circuits, for example, the DC gain and unity gain frequency in an intrinsic gain stage. Secondly, it can be proven that the g_m/I_D ratio is equal to the derivative of the logarithm of I_D with respect to V_G. This relation can indicate the operating region of the transistor. Additionally, both g_m/I_D and the normalized current are size-independent. The relationship between them is then also size-independent.

There are different approaches to using the g_m/I_D method to size transistors. One possible method is:

1. Estimate required g_m from a design specification.
2. Choose a g_m/I_D based on gain and speed requirements.
   - Small g_m/I_D gives high speed, large V_{dsat}.
   - Large g_m/I_D gives low power, low speed, small V_{dsat}.
3. Estimate required g_m/g_{ds} based on gain or output resistance requirements.
4. Calculate gate length and width and bias current based on the requirements.

2.5 FDSOI Technology

Fully Depleted Silicon On Insulator (FDSOI) technology is a planar device. Since the traditional CMOS devices are having trouble keeping up with Moore's law, the idea behind FDSOI is to provide a device that can be scaled even further down. Figure 5 shows an illustration of the FDSOI transistor. There are two main differences from traditional CMOS devices. Firstly, the device has a very thin silicon layer in the channel, so no doping is needed, making it fully depleted. Secondly, there is an ultra-thin buried insulator between the base silicon and the channel [14]. Compared to bulk CMOS devices, the FDSOI achieves less leakage current. Furthermore, the parasitics between the source and the drain are reduced because of the buried oxide.

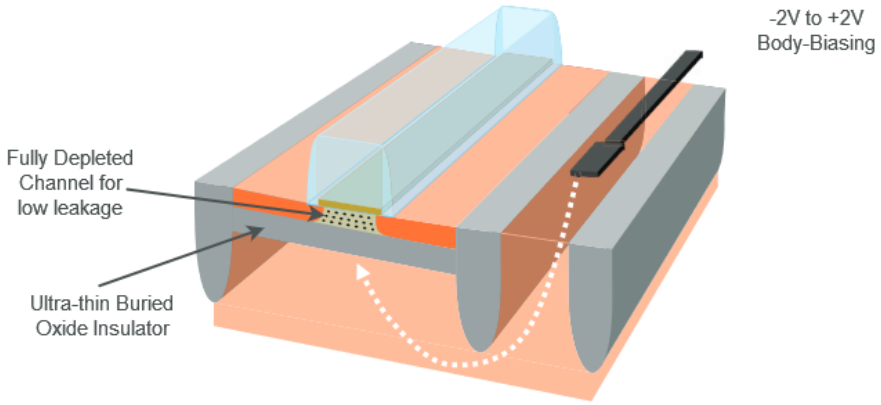


Figure 5: Illustration of the FDSOI device [14]

Another feature of the FDSOI is the high level of control the designer has on the threshold voltage in the device. Firstly, there are several transistor models with different intrinsic threshold voltages. Secondly, it is possible to use a high degree of body biasing on the devices. Traditional CMOS devices have limited body biasing because of parasitic leakage currents. In FDSOI, the buried oxide reduces this, making it possible to use both Reverse body bias (RBB) and Forward body bias (FBB) [14].

3 Design

This chapter covers the design of the OTA. First, the implementation of the amplifier circuit and its common mode circuits is covered. Then the layout design is explained. The full schematic implementation is shown in appendix A.

3.1 Amplifier design

The OTA implementation used in this thesis is shown in figure 6. The architecture can be defined by the amplifier and the common mode circuits. The amplifier is an inverter-based pseudo-differential OTA. Two common mode circuits, a common mode feedforward (CMFF) and common mode feedback (CMFB), are added to help set the amplifier's operating point. The circuit was proposed in [8] and [9]. Amplifier architecture was chosen based on a literature study because previous implementations had achieved a high bandwidth compared to the other amplifiers studied.

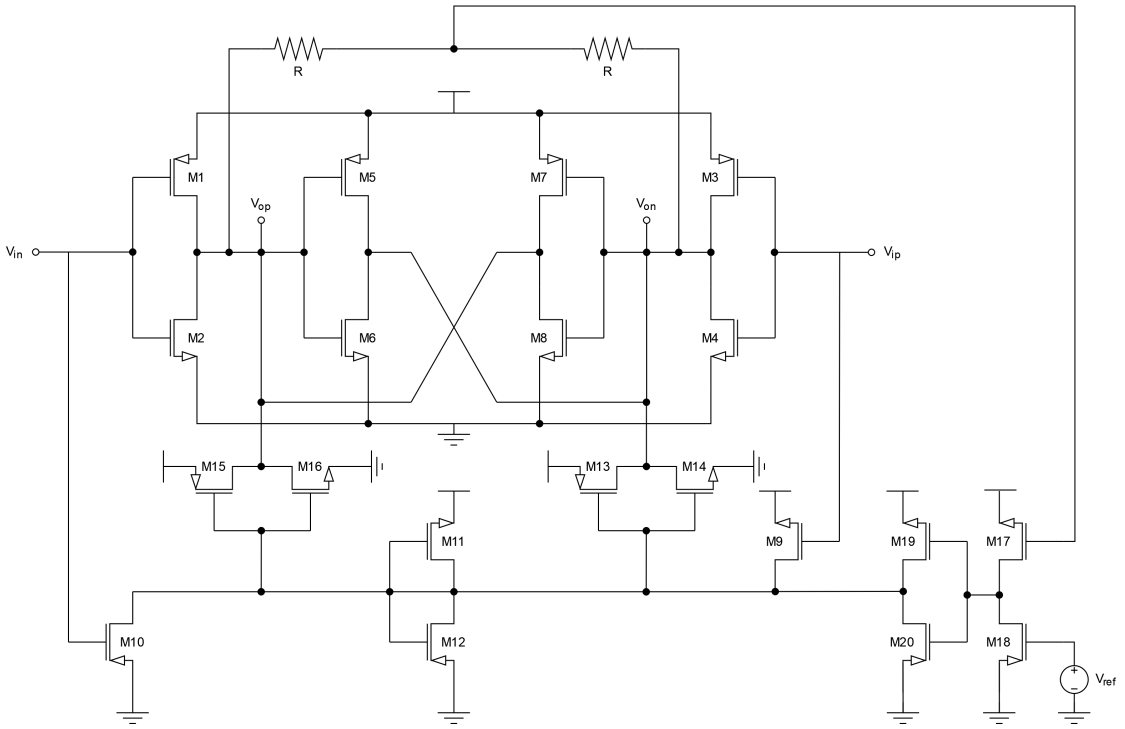


Figure 6: The implemented amplifier schematic

The amplification stage shown in figure 7. It uses an inverter stage as input and has an additional auxiliary inverter stage to boost gain with negative resistance. No tail-transistors are used to give the inverters more headroom, making it a pseudo-differential amplifier.

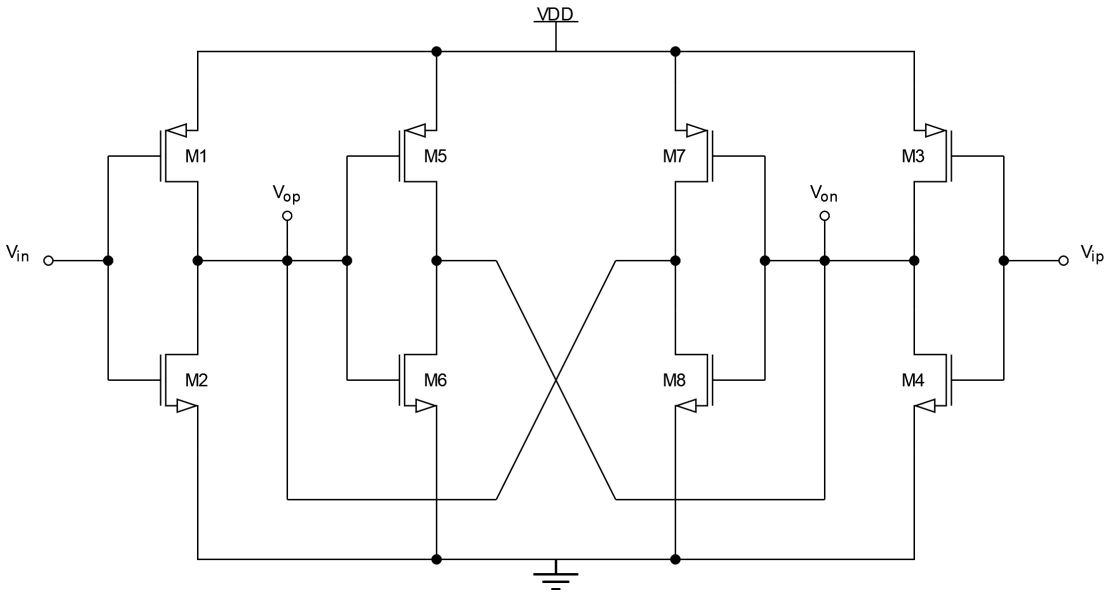


Figure 7: Inverter-based amplifier

The small signal amplification of the OTA is found by analyzing half the circuit, M1, M2, M7, and M8. The same analysis will hold for the other half-circuit by symmetry. As shown in section 2.3, equation 10 gives the gain of the input inverters. In the equation, g_m is the transconductance of the transistors, and r_{ds} is the output resistance.

$$A_{inv} = -(r_{ds1} \| r_{ds2})(g_{m1} + g_{m2}) \tag{10}$$

The auxiliary inverters M5-M8 are cross-coupled, creating positive feedback. This generates a negative resistance at the output node, which will boost the gain of the amplifier. Equation 11 gives the additional amplification with which the gain is boosted.

$$A_{aux} = \frac{1}{1 - R_o(g_{m7} + g_{m8})} \tag{11}$$

In the equation above, R_o is the output resistance of the output node V_{op}. It will be the parallel combination of the output resistance r_{ds} of all the transistors connected to the node. The definition of this resistance is shown in equation 12.

$$R_o = r_{ds1} \| r_{ds2} \| r_{rds7} \| r_{ds8} \approx r_{ds1} \| r_{ds2} \tag{12}$$

The total small signal gain of the OTA will be the product of the gain in the input stage A_{in} and the auxiliary stage A_{aux}, shown in equation 13. It is preferable to

have the output resistance of the input inverters smaller than the auxiliary inverters, because this makes the total output resistance R_o only dependent on M1 and M2, shown in 12, giving the designer more control. This simplification is helpful when stability is considered. To avoid instability the denominator $1-R_o(g_{m7}+g_{m8})$ should be positive at all times. Having R_o be independent of $g_{m7} + g_{m8}$ makes designing for high gain and good stability considerably easier.

$$A = -\frac{R_o(g_{m1} + g_{m2})}{1 - R_o(g_{m7} + g_{m8})} \tag{13}$$

3.2 Common mode circuits

In the OTA, two common mode circuits are added to set the operating point in the amplifier. Figure 8 shows the common mode feedforward circuit. In the circuit, transistors M9 and M10 will sense the input voltage and create a common mode current in node A. All differential currents will be canceled. The resistance R_A in node A is given in equation 14. Since M11 and M12 is diode-connected, this will be a low impedance node. The resistance and common mode current will create a common mode voltage at the input of the inverter-pairs M13-M14 and M15-M16. This voltage will then adjust the common mode voltage at the output node of the amplifier. The inverter pairs are necessary to stop common mode current flow to the output.

$$R_A = r_{ds9} \| r_{ds10} \| \frac{1}{g_{m11}} \| \frac{1}{g_{m12}} \approx \frac{1}{g_{m11}} \| \frac{1}{g_{m12}} \tag{14}$$

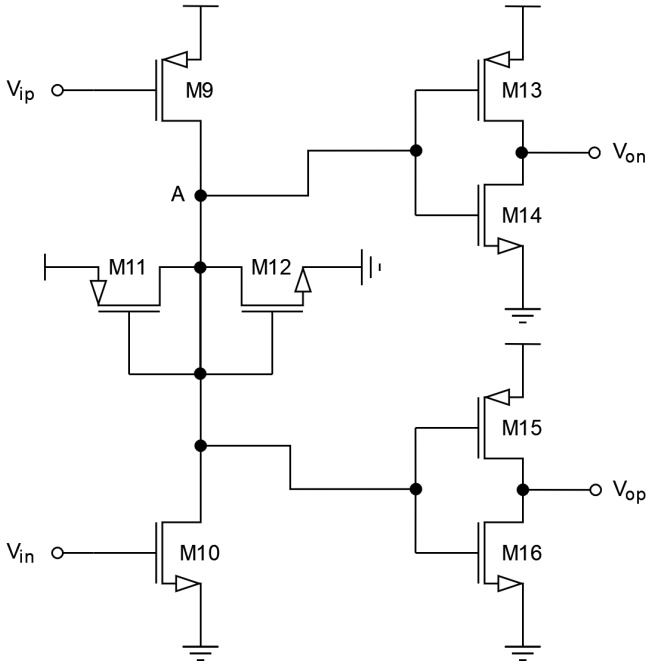


Figure 8: Common mode feedforward circuit

Figure 9 shows the common mode feedback circuit. It works by having transistor M17 sense the common mode voltage at the output of the amplifier. This voltage is then compared to the reference voltage V_{ref} at the input of M18. Using the inverter pair M19-M20, a feedback voltage V_{fb} will bias the voltage at node A in the CMFF circuit to counteract any deviation.

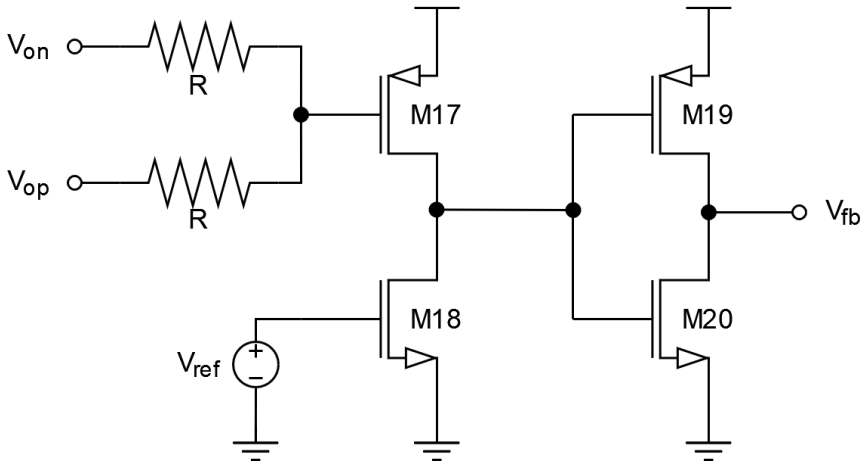


Figure 9: Common mode feedback circuit

3.3 Transistor sizing

The transistor dimensions used in the circuit implementation are shown in table 2. All the transistors are FDSOI devices, and the model with the lowest inherent threshold voltage is used. The resistor value in the common mode feedback circuit is 2.56MΩ. Since the amplifier layout is implemented, it is preferable not to have gate fingers wider than 500nm or longer than 500nm. This can be accomplished by using multiple gate fingers in the transistors. The number of gate fingers used is also presented in the table.

The g_m/I_D method is used to find the transistor sizes in the amplifier. For the input inverter pairs M1-M4, unity gain frequency specifications gives that $g_{m1} + g_{m2} >$ 5.3mS is needed. To add a design margin it is set to $g_{m1} + g_{m2} =$ 7.8mS. In addition, the transistors are biased in strong inversion to achieve fast devices. The input inverters provide most of the amplification in the system, so a high g_m/I_D is desired. g_m/I_D is therefore set to 15 for the input inverter pairs to get a high gain while also keeping the power consumption at a reasonable level,

For the auxiliary inverter pair, a high g_m/I_D is also desirable to boost the gain of the amplifier. In M5-M8, g_m/I_D is therefore set to 17. However, to keep the amplifier stable $1 - R_o(g_{m7} + g_{m8})$ has to be positive. Meaning g_m and consequently, I_D has to be small. The transistors are biased between moderate and strong inversion. They do not affect the unity gain bandwidth to a high degree, but somewhat fast devices are preferable.

The sizing of the transistors in the common mode circuits is done experimentally, with the aim of keeping common mode gain minimal.

Table 2: Transistor dimensions used in the implemented amplifier

Transistor	**Type**	Width [nm]	Length [nm]	Gate fingers
M1, M3	PMOS	9306	70	22
M2, M4	NMOS	9306	70	22
M5, M7	PMOS	510	270	2
M6, M8	NMOS	510	270	2
M9	PMOS	300	300	1
M10	NMOS	300	300	1
M11	PMOS	852	380	4
M12	NMOS	852	380	4
M13, M15	PMOS	1602	500	6
M14, M16	NMOS	1602	500	6
M17	PMOS	640	100	2
M18	NMOS	640	100	2
M19	PMOS	2400	390	10
M20	NMOS	2400	390	10

3.4 Layout

The layout of the amplifier is implemented to verify the performance further. This is done since parasitic effects are not included in the transistor model used in circuit simulations. Because of time constraints, the common mode circuits are not included in the layout, only the amplifier transistors M1-M8. The implementation is shown in figure 10. The total area if the amplifier was 35.5μm^2. It should be noted that transistor matching is not considered in the layout. This is again because of time constraints.

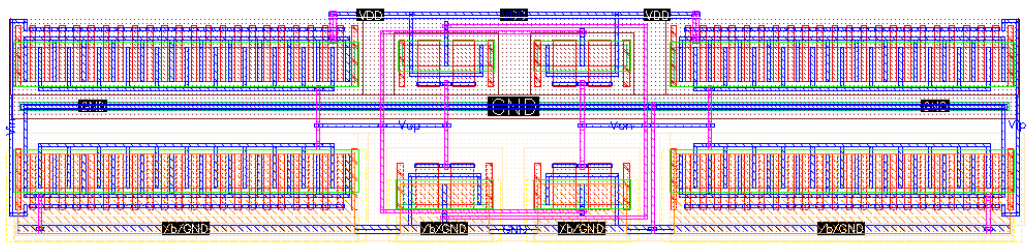


Figure 10: Amplifier layout

4 Simulations results

This chapter presents the simulation results achieved in this project. The results are only briefly discussed, as a more thorough discussion is done in section 5. All the circuits were simulated using Cadence Virtuoso. The full testbenches are shown in the appendices B, C and D. All the simulations use a supply voltage of 0.8V. As mentioned in the introduction, the ADC defines the integrator components. The components values are shown in table 3, and all component models used are ideal.

Table 3: Integrator component values

Component	**Value**
$R_{\beta 1}$	5KΩ
C_1	1.7pF
$R_{\beta 2}$	50KΩ

4.1 Open Loop simulations

The DC gain, unity gain frequency, and the input-referred noise of the amplifier are found using the testbench shown in figure 11. The signal applied to the amplifier V_{in} is a sine. It has a frequency of 1MHz with an AC magnitude of 1V and a common mode level of 400mV. The load resistors are connected to common mode voltage $V_{CM} = 400\text{mV}$, to eliminate DC currents.

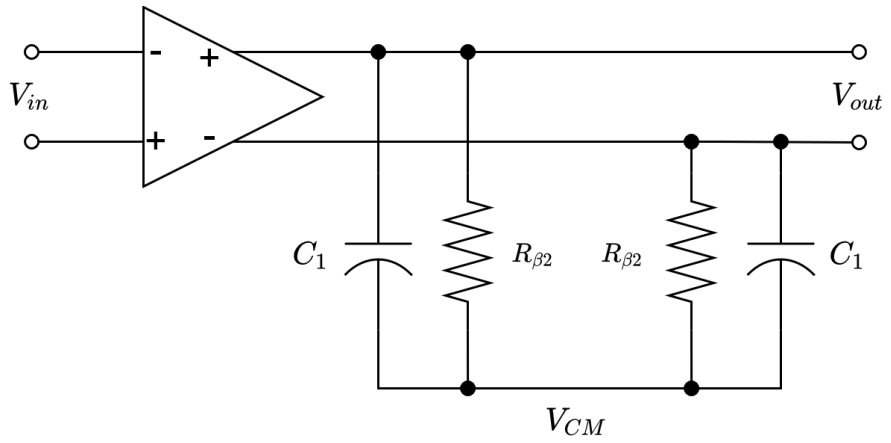


Figure 11: Open loop testbench

Figure 12 shows the frequency response of the open loop testbench. Both the gain and phase response is included. Simulations show that the amplifier achieves a DC gain of 70.47dB and a unity gain frequency of 720.1MHz. The current consumption of the OTA is 572.2μA.

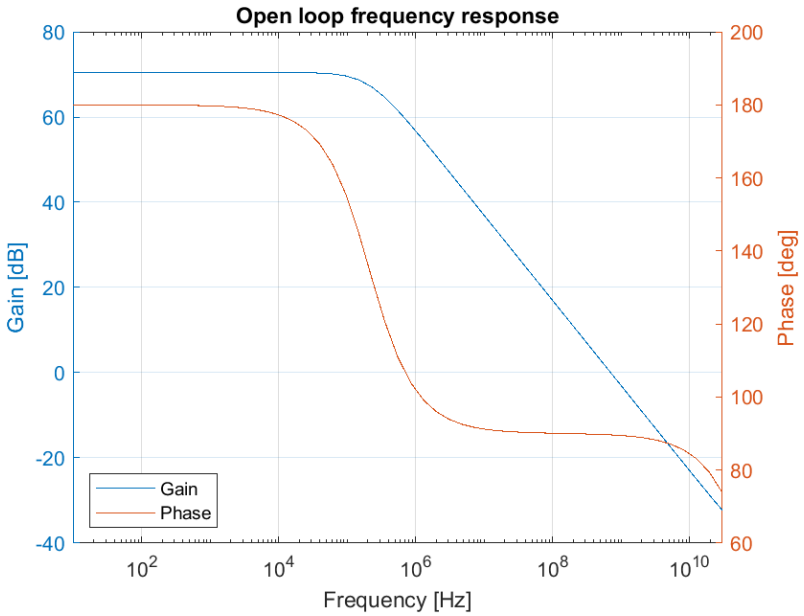


Figure 12: Open loop frequency response

The input-referred noise in the amplifier is shown in figure 13. At 1MHz the noise is 6.303 nV/$\sqrt{\text{Hz}}$. The thermal noise of the OTA is found at 1GHz, and it is 1.585nV/$\sqrt{\text{Hz}}$.

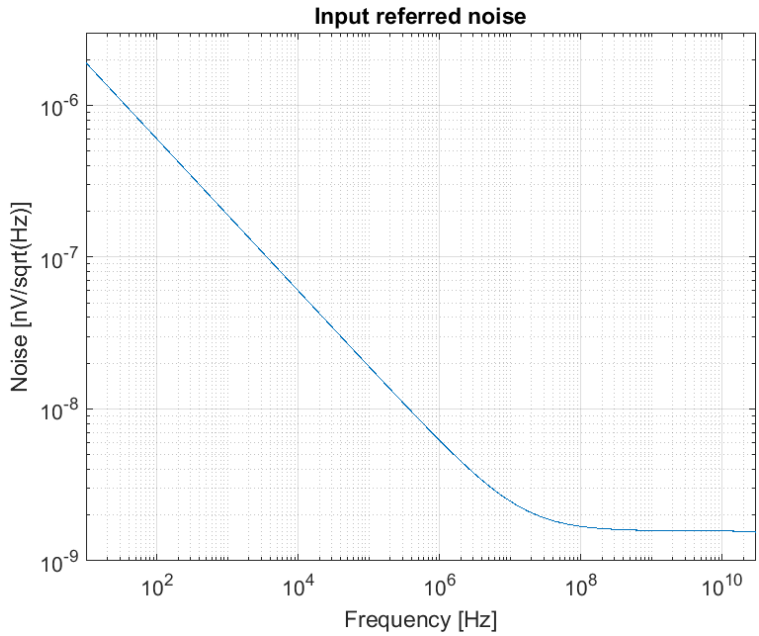


Figure 13: Input-referred noise

The same testbench is used for testing the amplifier in process corners (SS, FF, FS, SF). Figure 14 shows the frequency response for all the corners. The simulations show that the DC gain of the amplifier varies between 44dB (SF) and 70.14 dB (SS). The unity gain frequency varies between 492.8MHz (SS) and 978.5MHz (FF). The current consumption varies between 342.9μA (SS) and 891.3μA (FF). The input-referred noise varies between 5.8 nV/$\sqrt{\text{Hz}}$ (SS) and 6.7 nV/$\sqrt{\text{Hz}}$ (FF).

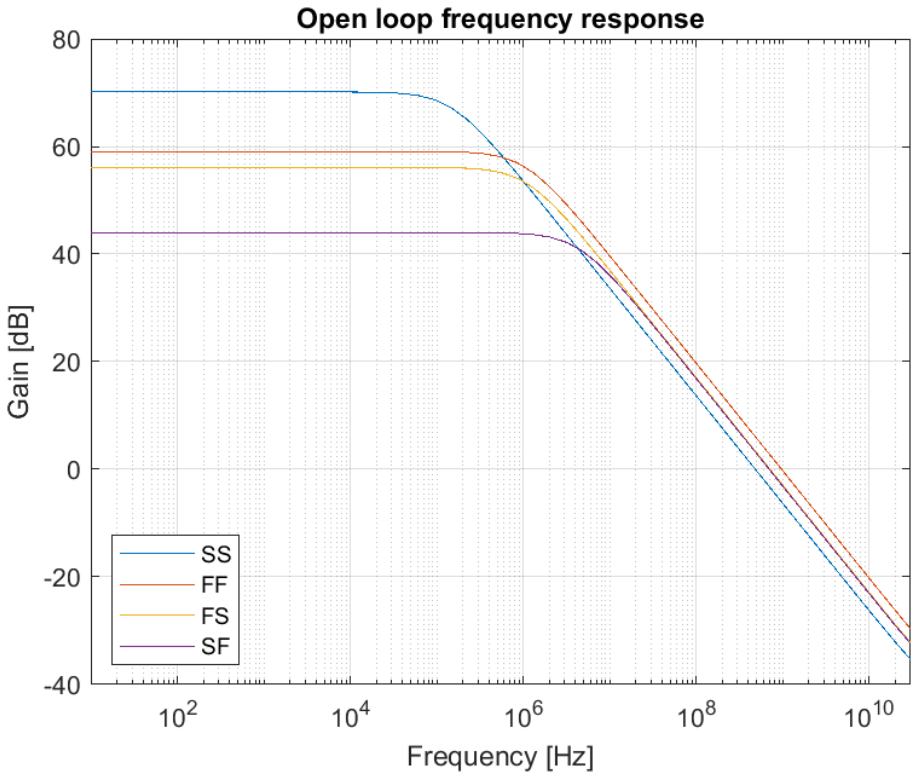


Figure 14: Open loop frequency response in process corner

4.2 Closed Loop simulations

The amplifier's closed loop response and phase margin are found using the testbench shown in figure 15. The signal applied to the amplifier V_{in} is a sine. It has a frequency of 1MHz with an amplitude of 50mV and a common mode level of 400mV. The load resistors are connected to common mode voltage $V_{CM} = 400\text{mV}$, to eliminate DC currents.

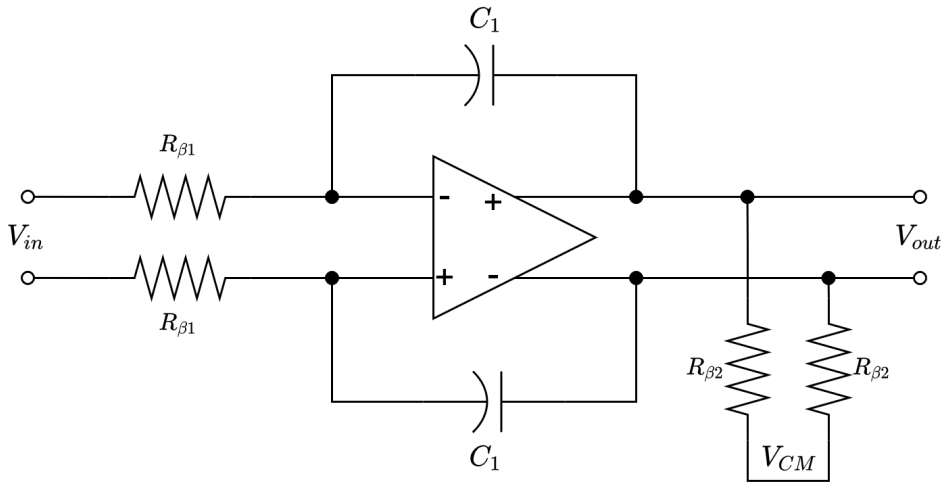


Figure 15: Closed loop testbench

The frequency response of the closed loop testbench is shown in figure 16. The phase margin of the amplifier is 69.39°. In corner simulations the phase margin varies between 69.46° (FS) and 70.21° (SS).

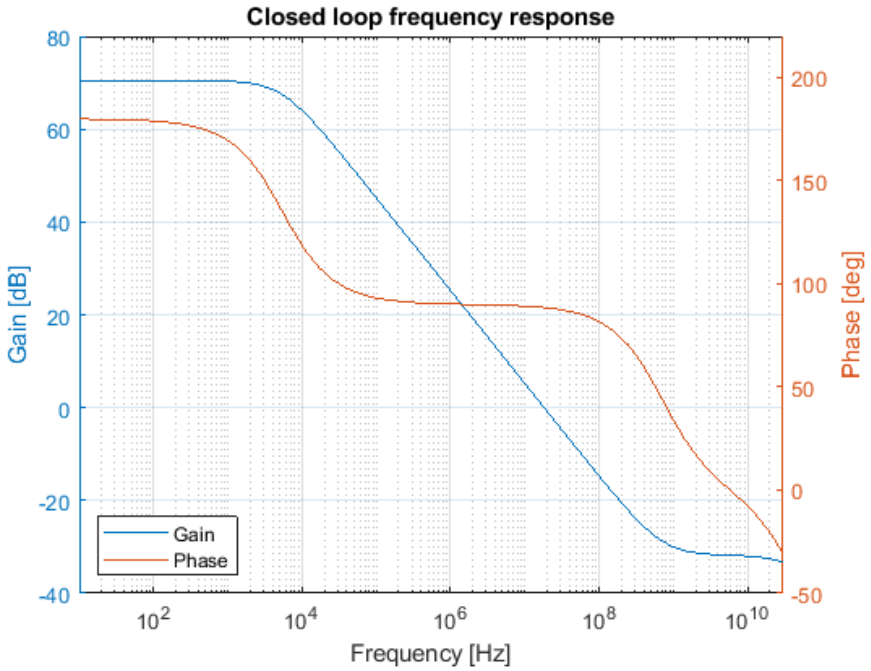


Figure 16: Closed loop frequency response

4.3 Linearity simulations

The second order harmonic distortion (HD2) in the amplifier is found using the testbench shown in figure 17. The size of the capacitors are $C_1 = 1.7$pF and $C_2 = 3.4$pF, achieving a feedback gain of 2. The feedback resistor value is $R_1 = 500\text{M}\Omega$, and the load resistor value is $R_{\beta 2} = 50\text{K}\Omega$. The signal applied to the amplifier V_{in} is a sine. It has a frequency of 1MHz with an amplitude of 100mV and a common mode level of 400mV. The load resistors are connected to common mode voltage $V_{CM} = 400$mV, to eliminate DC currents.

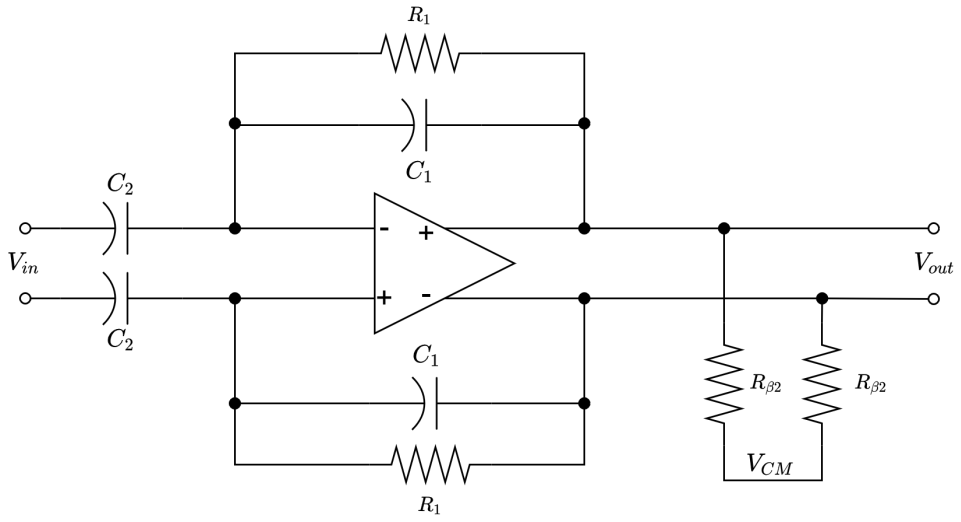


Figure 17: Linearity testbench

Virtuoso's spectrum feature is used to calculate the HD2. It is based on a transient analysis with stop time 20μs and added transient noise with Noise Fmax = 1GHz. The retol factor is set to 10μ. The spectrum setup uses start time 0, stop time 20μ, Sample Count 1024, Window type Hanning and harmonics 2.

Figure 18 shown the spectrum of the differential part of the output signal V_{out}. The HD2 is determined using a Monte Carlo simulation with 100 points and reporting the worst case. For this amplifier, that is -69dB.

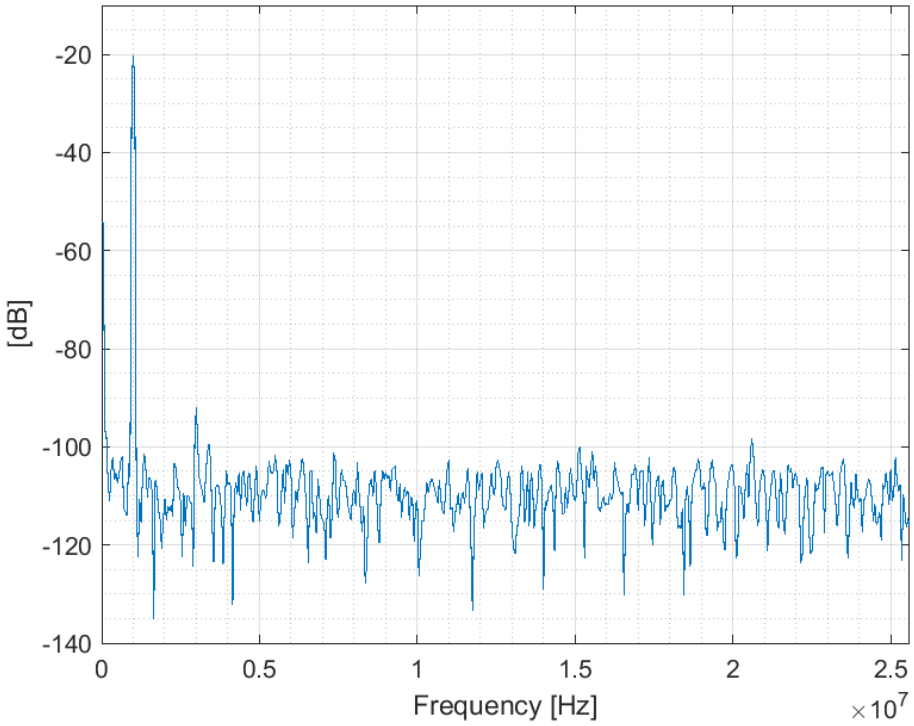
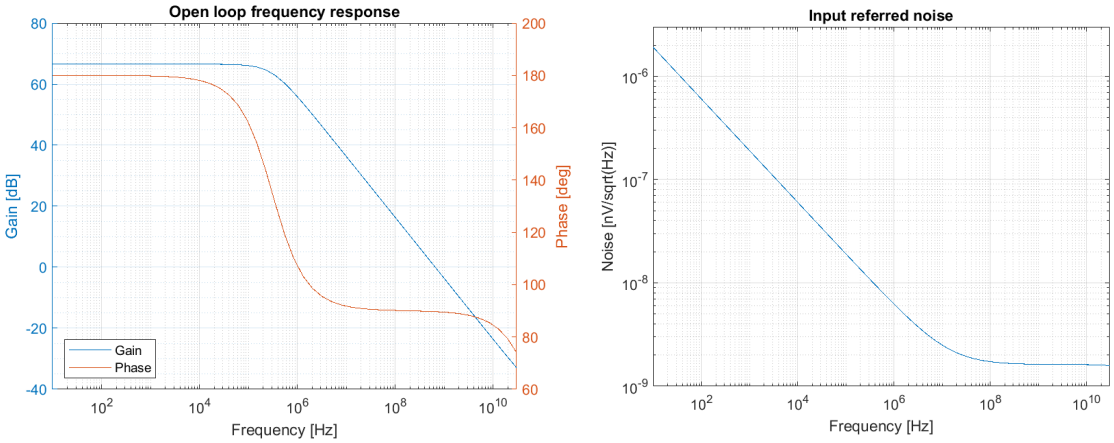


Figure 18: Simulated spectrum

4.4 Post layout simulations

Simulations of the amplifier post layout are also performed. The same testbenches are used for the post layout simulations. Since only parts of the OTA were implemented in layout, CMFF and CMFB are added back as schematics before simulations.



(a) Open loop frequency response

(b) Input-referred noise

Figure 19: Post layout simulations

Figure 19 shows the open loop simulations of the amplifier post layout. The simulations show that it achieves a DC-gain of 66.61dB and a unity gain frequency of

667.8MHz. The current consumption in the amplifier is now 595.9μA. The input-referred noise remains the same at 6.303 nV/$\sqrt{\text{Hz}}$ at 1MHz.
The linearity testbench shows that the post layout amplifier has an HD2 of -67.98dB.

4.5 Final results

An overview of all the simulation results is given in table 4.

Table 4: Final results

	Spec	**Nominal**	**Min**	**Max**	**Post layout**	**Unit**
DC gain	55	70.47	44	70.14	66.61	dB
Unity gain frequency	500	720.1	492.8	978.5	667.8	MHz
Noise voltage density @ 1MHz	<12	6.3	5.8	6.7	6.3	nV/$\sqrt{\text{Hz}}$
Current consumption	-	572.2	342.9	891.3	595.9	μA
HD2	-	-69			-67.98	dB

5 Discussion

The main issue with the implemented amplifier is the effects of process variations. It was shown in the simulations that the gain, bandwidth, and current consumption of the amplifier change a lot between corners. The gain varies by almost 30dB and the bandwidth with 500MHz. Even though corner simulations present the worst-case scenarios, this will severely limit the OTA's applicability if implemented in more extensive systems. In addition to these variations, another issue the amplifier has with process variations is common mode voltage. In skewed corners SF and FS, the common mode voltage at the output deviated from the expected $V_{DD}/2$. This deviation will also be an issue if the design is taken further.

One possible reason the amplifier is sensitive to process variations is the heavy use of inverters. As mentioned in section 2.3, it is crucial to match the factor β for the PMOS and the NMOS transistors in an inverter pair. Having $\beta_p = \beta_n$ will give the best linearity of the V-I conversion in the inverter [12]. When they are mismatched, the conversion becomes less linear. This might also be why corners FS and SF are most affected. The whole OTA uses nine inverter pairs. As mentioned with corner simulations, the mismatch in each inverter will be the worst-case scenario. If the design is taken to tape out, the β mismatch will differ between the inverters. Layout techniques can be used to reduce the mismatch in the most vital transistors. Regardless, some compensation or biasing should be added to reduce the effects of process variations.

A possible way of dealing with the corner variations is adding some adaptive body biasing. In the book Low-Power Analog Techniques, Sensors for Mobile Devices, and Energy Efficient Amplifiers [11], two possible methods of using body biasing on inverter-based amplifiers are presented. One method uses a sensing transistor and a resistor to provide a corner-dependent voltage. This voltage is then applied to the bulk of the device to regulate the threshold voltage. The other method applies a voltage to the bulk with diodes to keep the total overdrive voltage of the inverter constant. The second one is specifically designed to deal with supply variations but may also help with corner variations. Body biasing might be a good idea for this implementation because FDSOI transistors are used. As mentioned in section 2.5, a wide range of voltages can be applied to the bulk of FDSOI devices to adjust the threshold voltage. This means the designer has a high degree of control over the devices, making it easier to use adaptive body biasing than in traditional bulk CMOS.

The common mode voltage issue in some corners can be addressed by adding a tail-transistor. The amplifier uses a pseudo-differential input stage, contrary to the more typical fully differential input stage. In the paper where the amplifier is proposed, the supply is 0.6V. So, using a pseudo-differential structure saves headroom [9]. The issue is that pseudo-differential stages have a lower common mode rejection ratio and are more likely to have common mode gain. For this thesis, the supply voltage is 0.8V, and all the devices have an inherent low threshold voltage. It would be possible to add a tail-transistor above or below the input inverters to make it fully differential. This will reduce the headroom of the transistors, but that is a tradeoff

for better CMRR.

Two things are easily noticed when comparing the results of the implemented OTA to the papers that proposed the architecture. The OTA has a much higher gain, but on the other hand, it has a much lower unity gain bandwidth. It is discussed in [9] that the gain of the OTA is inversely proportional to the bandwidth. Since these papers implement Gm-C integrators, their OTA needs a much higher unity gain bandwidth. For this thesis, the bandwidth requirements are much lower, so this tradeoff can be taken advantage of to achieve a much higher gain.

In addition to the corner variations, there are some issues with the layout design. Because of time constraints, no effort was put into matching any transistors. One thing that could have improved the layout is placing the input transistors closer together and in the middle of the layout. Since they provide most of the amplification, minimizing the mismatch between them is crucial. Matching is done by placing them close together, reducing the possible doping variations in the silicon. Placing them in the middle will protect against things like over-etching. The effect of this issue has not been quantified since mismatch was not simulated for the post layout circuit. Nonetheless, it is good design practice to do this for transistors that need to be matched.

Another good design practice that was not considered is adding dummies to the transistors. During production, dummies protect the transistors from fabrication variations, especially over-etching. In addition, can they be used to achieve better symmetry in the layout, which helps against mismatch. Adding dummies will increase the area of the amplifier, but they are unavoidable, so it is good design practice to add them.

5.1 Future work

Some work should be considered before using this OTA as a building block for larger implementations. As mentioned above, some compensation techniques should be added to reduce corner variations in the circuit. This could be an adaptive body biasing or any other compensations circuit. However, it will be necessary to make the amplifier pass specifications in all corners if it is used for other implementations.

Another design consideration that might be useful for future work is matching β in the inverter pairs. As pointed out in [12], if β of the NMOS and PMOS are matched, the V-I conversion will achieve the best linearity possible. This design did not consider this technique, so its effects are unknown. Nevertheless, it would be interesting to apply this in future work to see if it improves the amplifier's performance.

To further test the amplifier's performance, future work should try to implement the whole OTA in layout. The post layout simulations showed a drop in DC gain and bandwidth. Implementing the whole system in layout might uncover if any parasitic effects will reduce the operation of the amplifier any further. If this is done, matching the transistors, like adding dummies and rearranging the transistors, should be considered.

6 Conclusion

In this project, an OTA has been designed using 22nm FDSOI technology. This implementation was done so that it could be used as a component in a control-bounded ADC. An inverter-based pseudo-differential OTA was designed to achieve the given specifications. The OTA was implemented as a schematic and simulated in Cadence Virtuoso. A layout of the amplifier, excluding the common mode circuits, was implemented and simulated to test the performance further and evaluate the effects of the circuit's parasitic components.

The simulations showed that the amplifier achieved a DC gain of 70.47dB, a unity gain bandwidth of 720.1MHz, and an input-referred noise of $6.3\text{nV}/\sqrt{(}\text{Hz})$ at 1MHz in the nominal corner. The results are well within the specifications given for the amplifier.

When simulating process corners, it was found that the amplifier gain and bandwidth varied a lot. For corner FS and SF, the amplifier showed signs of unwanted common mode gain at the output. This deviation is most likely because of the mismatch in the inverters. Some compensation should be implemented to reduce the effects of process corners, for example, adaptive body biasing. To reduce the unwanted common mode gain a tail-transistor could be added. Apart from this, no impactful variation in input-referred noise was observed, suggesting the amplifier is resilient against noise.

The post layout simulations showed a slight drop in DC gain and bandwidth but were overall not affected by the parasitic capacitances. The DC gain was 66.61dB, and the unity gain frequency was 667.8MHz. The input-referred noise stayed the same, again implying that the amplifier is resilient against noise.
The amplifier worked and showed promising results in the nominal corner, but some work is still needed to make it usable in process corners for further use in other implementations.

References

[1] H.-A. Loeliger, L. Bolliger, G. Wilckens, and J. Biveroni, "Analog-to-digital conversion using unstable filters," in *2011 Information Theory and Applications Workshop*, 2011, pp. 1–4. DOI: 10.1109/ITA.2011.5743620.

[2] H. Malmberg, G. Wilckens, and H.-A. Loeliger, "Control-bounded analog-to-digital conversion," *Circuits Syst. Signal Process.*, vol. 41, no. 3, pp. 1223–1254, Mar. 2022, ISSN: 0278-081X. DOI: 10.1007/s00034-021-01837-z. [Online]. Available: https://doi.org/10.1007/s00034-021-01837-z.

[3] F. E. Feyling, "Design considerations for a low-power control-bounded a/d converter," M.S. thesis, NTNU, 2021.

[4] R. Harjani and R. K. Palani, "Design of pvt tolerant inverter based circuits for low supply voltages," in *2015 IEEE Custom Integrated Circuits Conference (CICC)*, 2015, pp. 1–8. DOI: 10.1109/CICC.2015.7338424.

[5] A. Ismail and I. Mostafa, "A process-tolerant, low-voltage, inverter-based ota for continuous-time $\Sigma - \Delta$ adc," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 24, no. 9, pp. 2911–2917, 2016. DOI: 10.1109/TVLSI.2016.2525786.

[6] P. C. C. de Aguirre and A. A. Susin, "A 0.6-v, 74.2-db dr continuous-time sigma–delta modulator with inverter-based amplifiers," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 65, no. 10, pp. 1310–1314, 2018. DOI: 10.1109/TCSII.2018.2853088.

[7] L. Lv, X. Zhou, Z. Qiao, and Q. Li, "Inverter-based subthreshold amplifier techniques and their application in 0.3-v $\Delta\Sigma$ -modulators," *IEEE Journal of Solid-State Circuits*, vol. 54, no. 5, pp. 1436–1445, 2019. DOI: 10.1109/JSSC.2018.2889847.

[8] D. M. Abdolmaleki M. and T. M.B., "Design and simulation of tunable low-pass gm-c filter with 1 ghz cutoff frequency based on cmos inventers for high speed telecommunication applications," *Analog Integr Circ Sig Process*, vol. 100, no. 2, pp. 279–286, 2019. DOI: 10.1007/s10470-019-01484-0.

[9] N. Ramesh and J. S. Gaggatur, "A 0.6 v, 2nd order low-pass gm-c filter using cmos inverter-based tunable ota with 1.114 ghz cut-off frequency in 90nm cmos technology," in *2021 34th International Conference on VLSI Design and 2021 20th International Conference on Embedded Systems (VLSID)*, 2021, pp. 305–309. DOI: 10.1109/VLSID51830.2021.00057.

[10] T. Carusone, D. Johns, and K. Martin, *Analog Integrated Circuit Design*, ser. Analog Integrated Circuit Design. Wiley, 2011, ISBN: 9780470770108. [Online]. Available: https://books.google.no/books?id=1OIJZzLvVhcC.

[11] Y. Chae, "Energy-efficient inverter-based amplifiers," in *Low-Power Analog Techniques, Sensors for Mobile Devices, and Energy Efficient Amplifiers : Advances in Analog Circuit Design 2018*, K. A. A. Makinwa, A. Baschirotto, and P. Harpe, Eds. Cham: Springer International Publishing, 2019, pp. 297–314, ISBN: 978-3-319-97870-3. DOI: 10.1007/978-3-319-97870-3_14. [Online]. Available: https://doi.org/10.1007/978-3-319-97870-3_14.

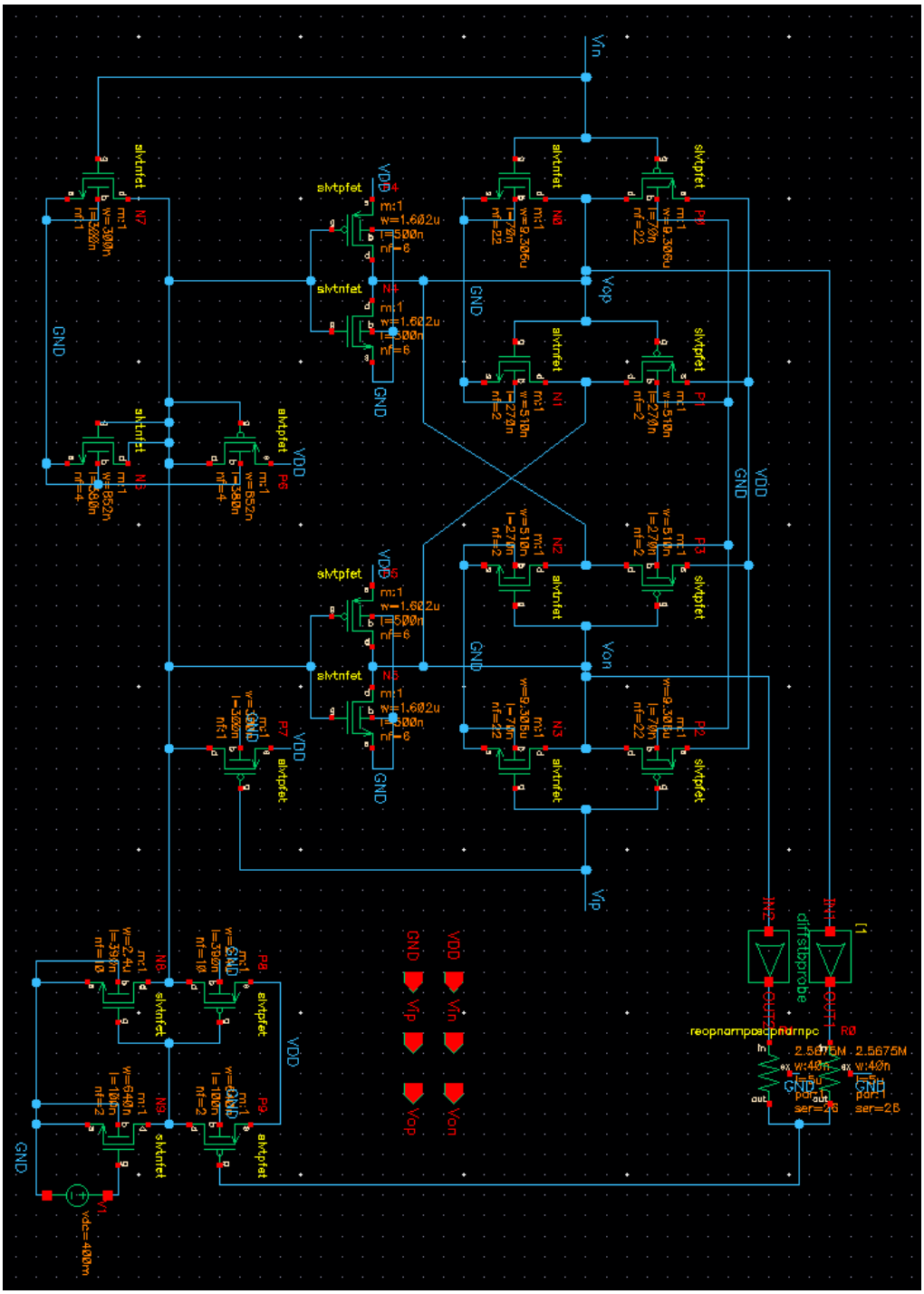
[12] B. Nauta, "A cmos transconductance-c filter technique for very high frequencies," *IEEE Journal of Solid-State Circuits*, vol. 27, no. 2, pp. 142–153, 1992. DOI: 10.1109/4.127337.

[13] F. Silveira, D. Flandre, and P. Jespers, "A g/sub m//i/sub d/ based methodology for the design of cmos analog circuits and its application to the synthesis of a silicon-on-insulator micropower ota," *IEEE Journal of Solid-State Circuits*, vol. 31, no. 9, pp. 1314–1319, 1996. DOI: 10.1109/4.535416.

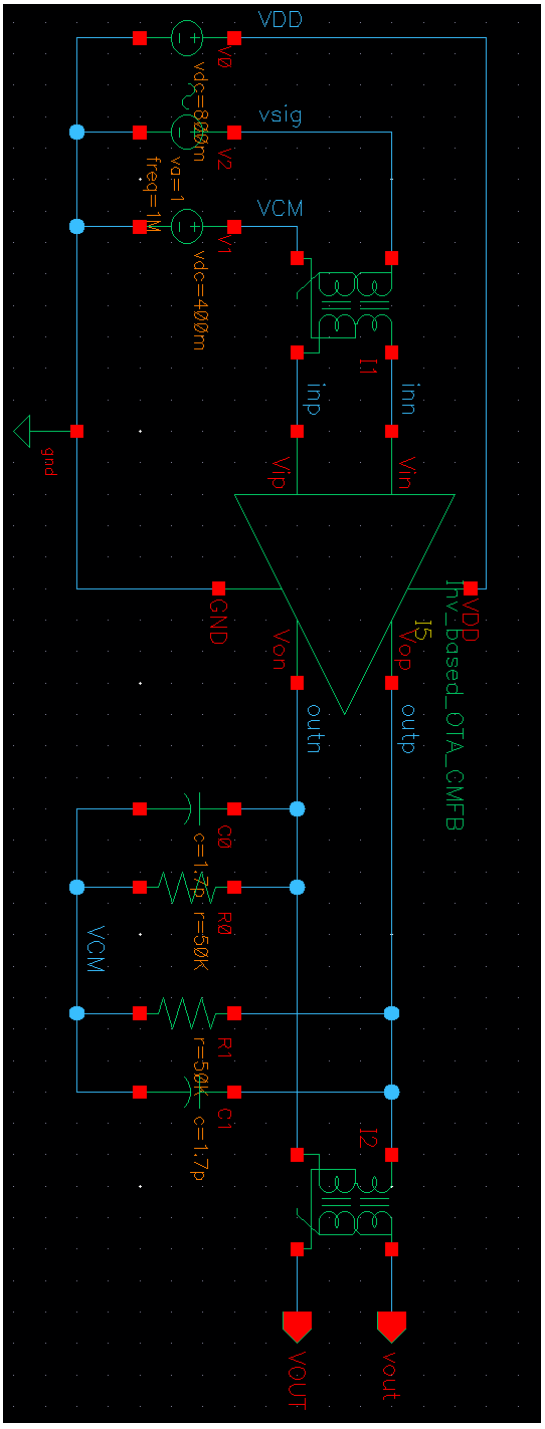
[14] Globalfoundries, *Fd-soi technology innovations extend moore's law*, Last accessed 14 Desember 2021, 2015. [Online]. Available: https://globalfoundries.com/sites/default/files/technicalpaper/fd-soi-technology-extend-moores-law.pdf.

Appendix

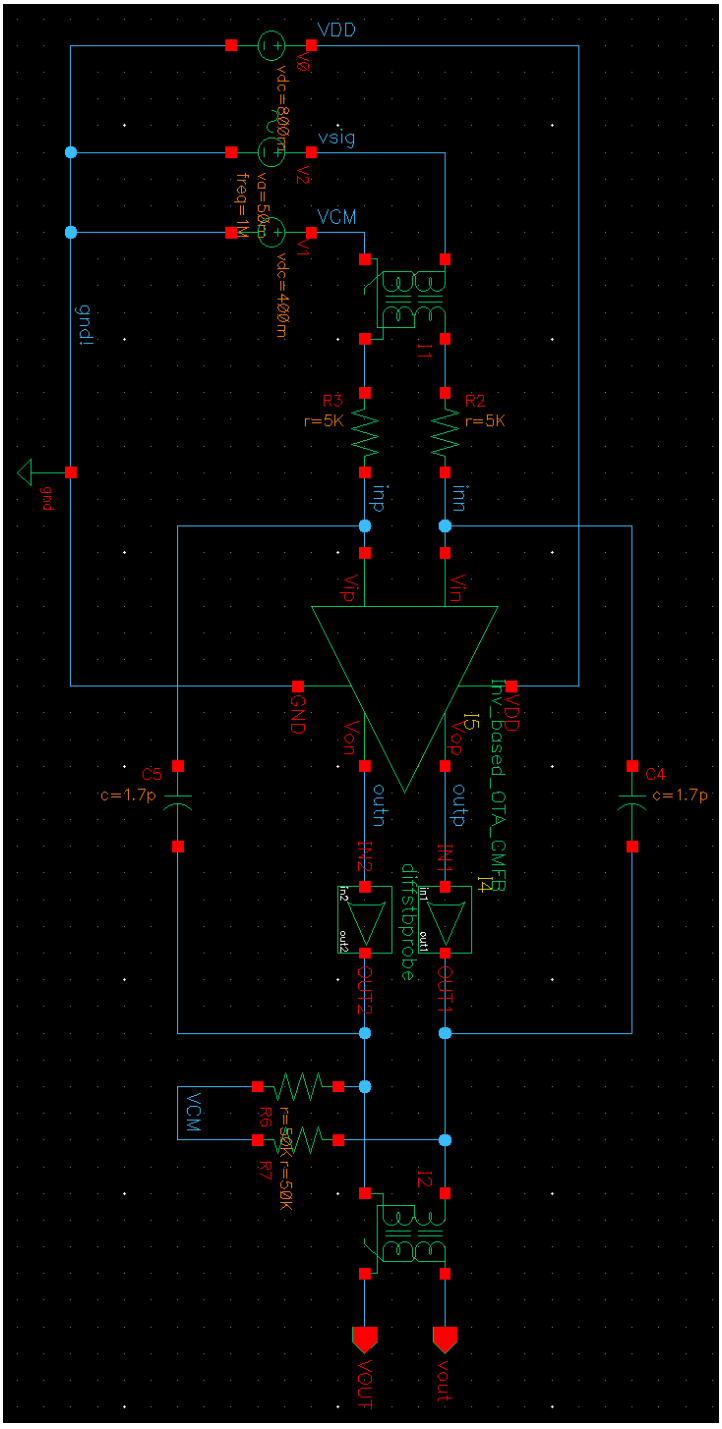
A Amplifier schematic



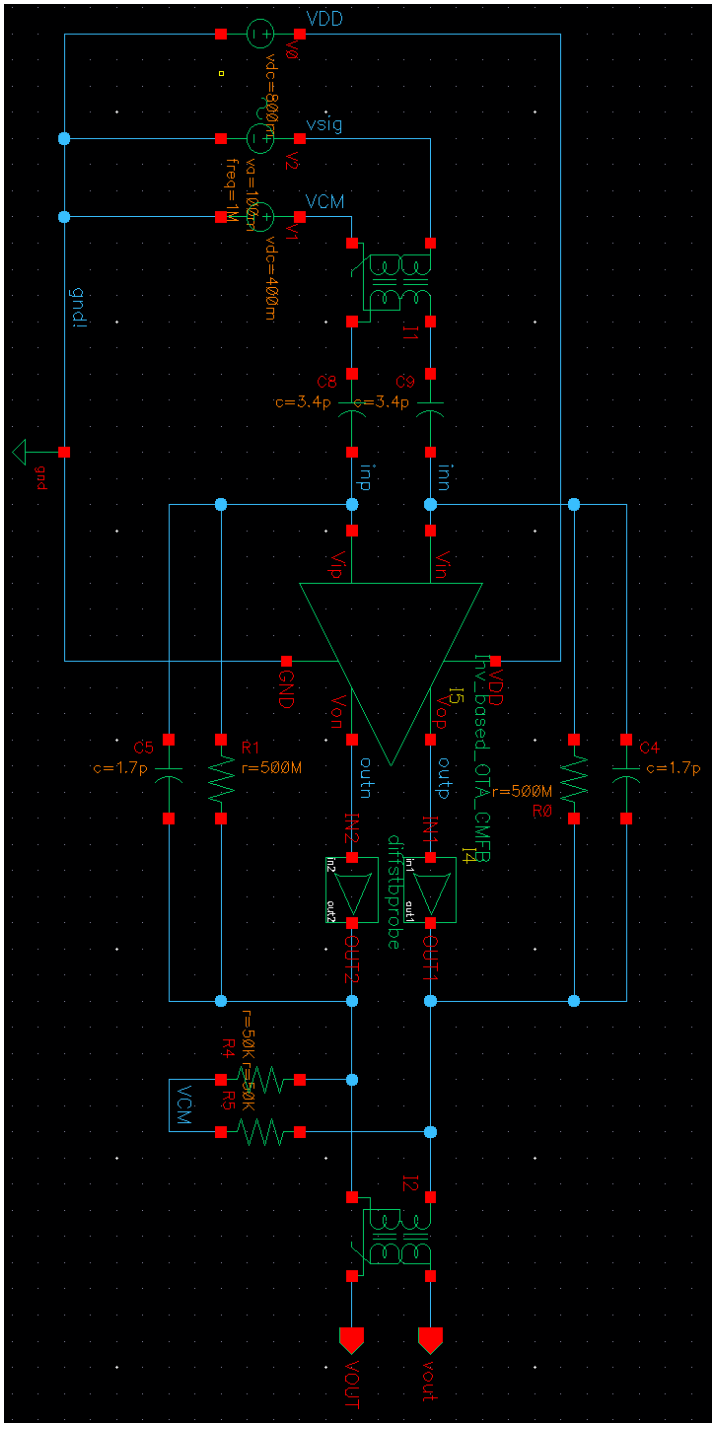
B Open Loop testbench

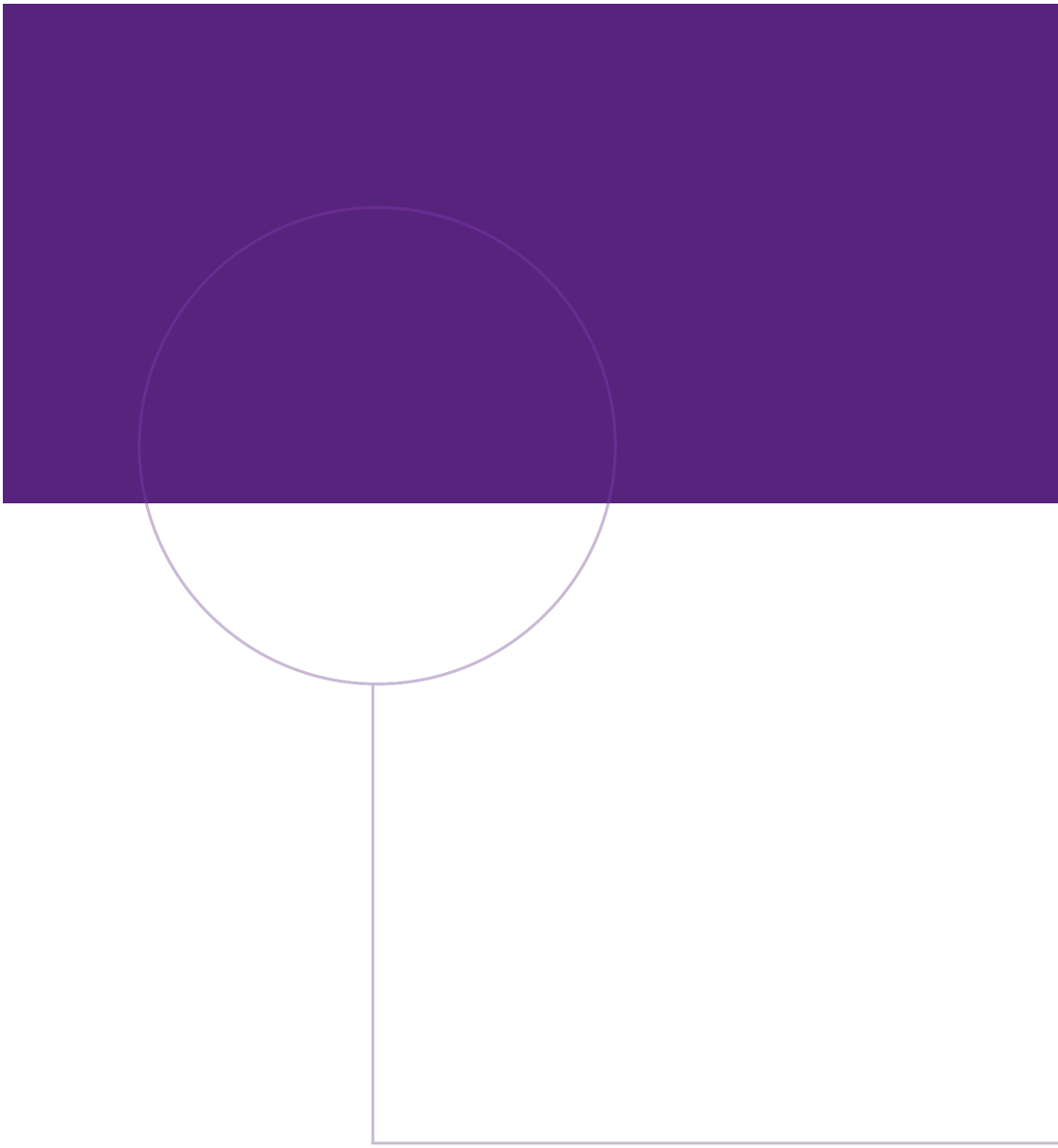


C Closed Loop testbench



D Linearity testbench





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