Master's thesis

NTNU
Norwegian University of Science and Technology
Faculty of Information Technology and Electrical Engineering
Department of Electronic Systems

Viktor Aase

Low Noise Variable Gain Amplifier for Time-Gain Compensation in Ultrasonic Imaging Front-End using 22nm FDSOI

Master's thesis in Electronics Systems Design and Innovation
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Abstract

As an ultrasound wave travels through the body, it is attenuated proportionally to the distance the wave needs to travel to return to the probe. With the fixed dynamic range of the ADC, the resolution of features further from the probe will be worse, as the reflected signal amplitude is more attenuated. A time-gain compensation circuit, like a variable gain amplifier (VGA), is therefore added between the transducer element and the ADC. The gain is increased with time so that the dynamic range of the signal reaching the ADC is reduced, thereby allowing greater resolution. This thesis proposes a current-based VGA based on a flipped voltage follower (FVF) current sensor (CS). The proposed VGA has a continuous gain range from $0dB$ to $20dB$ and a bandwidth of $20MHz$. Variable gain is achieved through dynamic back-gate biasing, a feature of the 22nm FDSOI technology, to change the relative transconductance of the reference and output transistors of the CS. Linearity is characterized by second harmonic distortion (HD2) and reaches a maximum value of $HD2 = -28.95dB$ without any additional linearization techniques. The amplifier contributes low noise to the signal, with a noise figure of $2.967dB$. A single-ended input stage and pseudo-differential output stage is utilized for driving a fully differential ADC. The power consumption of the VGA is $26\mu W$.

Sammendrag

Når en ultralyd puls propagerer gjennom kroppen blir den attenuert proporsjonalt til hvor langt bølgen propagerer før refleksjonen kan måles tilbake i proben. Ettersom en ADC har konstant dynamisk område, vil signaler som er reflektert lengre unna proben resultere i lavere oppløsning om transduseren er koblet direkte på ADCen. Tid-gain kompensering, i form av en variabel gain forsterker (VGA), er derfor lagt til mellom transduseren og ADCen. Forsterkningen økes med tiden etter en puls er sendt slik at amplituden på utgangssignalet skal være konstant og dermed øker den mulige oppløsningen i ADCen. Denne avhandlingen foreslår en strøm-basert VGA basert på en flipped voltage follower (FVF) strømsensor (CS). VGAen har kontinuerlig justerbar forsterkning fra $0dB$ til $20dB$ med en båndbredde på $20MHz$. Den variable forsterkningen oppnås ved dynamisk back-biasing, en egenskap ved 22nm FDSOI teknologien, for å endre den relative transkonduktansen mellom referanse og utgangstrinnet til strømsensoren. Linearitet er karakterisert av forvrengningen av den andre-harmoniske komponenten på utgangssignalet (HD2) og er simulert til en maksverdi på $HD2 = -28.95dB$ uten å bruke ekstra lineariseringsteknikker. Forsterkeren legger til lite støy på signalet og oppnår en støyfigur på $2.967dB$. Inngangstrinnet på forsterkeren er single-ended, mens utgangstrinnet er pseudo-differensielt for å drive en fult-differensiell ADC. Effektforbruket til VGAen er på $26\mu W$

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1 Introduction

Ultrasonic imaging is a proven technology for diagnosing a wide range of medical conditions and as the capabilities of the technology are further explored, more and more applications are discovered. However, the adoption of ultrasound imaging as a widespread diagnostic tool is limited by the current cost and bulk of the ultrasonic imaging systems. Advances in highly integrated ultrasound SoCs are bringing the complexity and cost of ultrasonic imaging down, making widespread adoption more feasible [2].

Miniaturized ultrasound probes can also be used in new ways due to their size. Miniaturization, therefore, unlocks new diagnostic practices, like ultrasonic imaging from within arteries where current probes are too big. Increasing the resolution of current small form factor probes can enable new and more reliable diagnostic techniques [3].

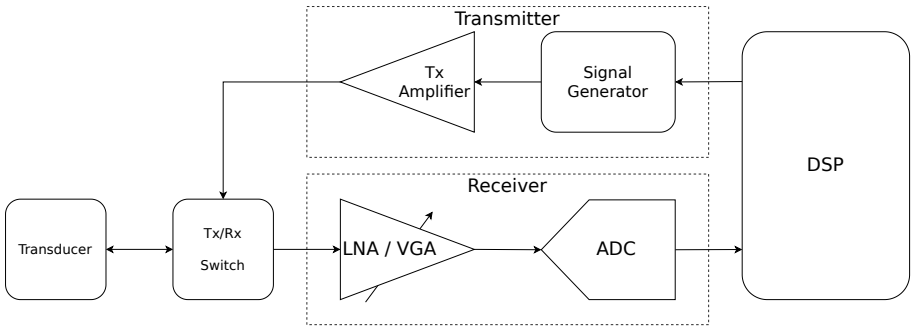
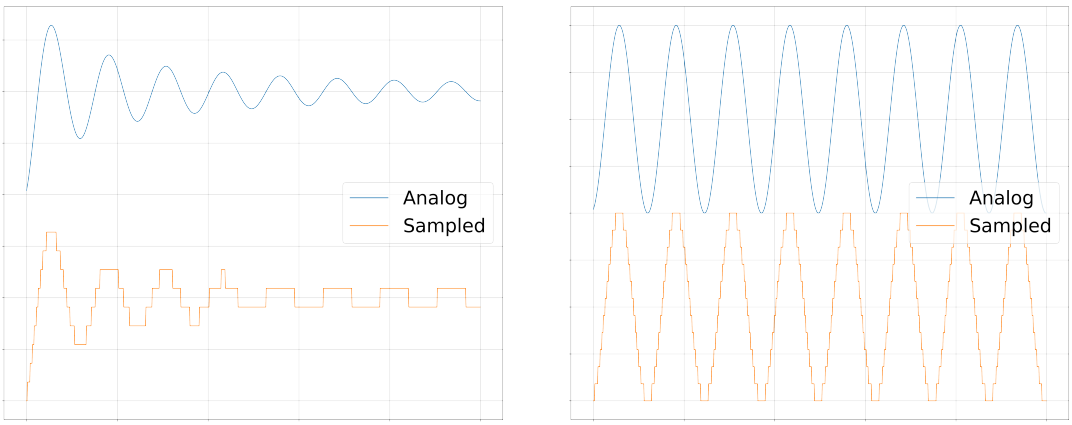


Figure 1.1: Typical analog front-end for ultrasonic imaging sensors

Figure 1.1 shows the typical building blocks of the front-end of an ultrasonic imaging sensor, consisting of the transducer, receiver, transmitter and digital signal processing unit (DSP). The receiver aims to provide a high-resolution digital signal for the DSP [4]. The ultrasound pulses are attenuated as they travel through tissue resulting in weaker signals from features further away from the probe. A variable gain amplifier (VGA) is added as a time-gain compensation circuit where the gain is increased with time to counteract the attenuation. This plays an important role in reducing the dynamic range of the input signal from the transducer. Limiting the dynamic range of the input signal of the ADC increases the bit resolution of the entirety of the signal compared to a high dynamic range signal, as illustrated in Figure 1.2

Traditionally the VGA is implemented using a transimpedance amplifier (TIA) with resistive feedback and programmable gain using resistor ladders and switch arrays to modify the feedback loop, as in [5, 6, 7, 8]. These resistor ladders can be area demanding and only stepwise gain-adjustment is achieved. The bandwidth is often limited using this technique without a significant increase in power consumption. Open-loop VGAs with analog gain control, like the one presented [9] based on transconductors and current steering, are viable options, however, they are not typically favored in the current ultrasonic SoCs.

This work aims to explore the possibility of using a current sensor (CS) topology as a



(a) Sampled dampend sine

(b) Sampled constant amplitude sine

Figure 1.2: Sampling of sine with and without time-gain compensation

current-based VGA with analog gain control. FDSOI offers techniques for dynamic adjustment of the transconductance, g_m, which can be utilized in current mirrors to achieve variable current-gain. Current amplifiers based on traditional current mirrors can struggle to meet noise figure $NF(f)$ requirements in ultrasound systems based on Capacitive Micro-machined Ultrasound Transducers (CMUTs), because of the input impedance inverse proportionability- and thermal noise proportionability-to g_m. Therefore, a low input impedance current mirror topology, where the input impedance is not as dependent on g_m, is utilized in the VGA presented in this thesis.

2 Theory

2.1 Ultra Thin Body and Box Fully-Depleted Semiconductor On Insulator

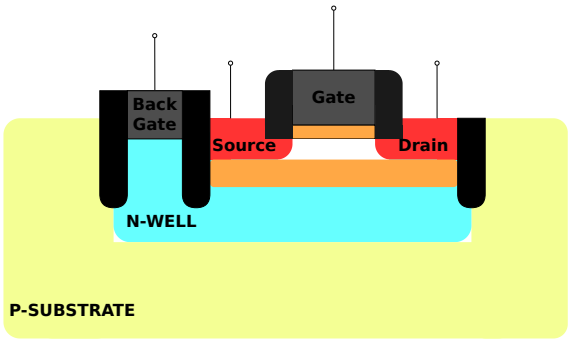


Figure 2.1: FDSOI PMOS

An illustration of a Ultra Thin Body and Box(UTBB) Fully-Depleted Semiconductor On Insulator(FDSOI) transistor can be seen in Figure 2.1. FDSOI uses a buried oxide (BOX) to isolate the channel from the well. A bias terminal, known as a back gate contact, can be connected to the well to control its potential. This is similar to bulk technologies, but the insulator increases the available bias range.

FDSOI enables several ways of modifying the threshold voltage, V_T, of the transistors. By isolating the well from the channel, both p- and n-type wells are available for both NMOS and PMOS. The technology also provides a method for controlling the doping of the channel. This provides a design kit with transistors with multiple V_T [10].

In addition to the composition of the transistors themself, applying a voltage to the back-gate, V_B, adjusts V_T of the device, as illustrated in Figure 2.2. Forward-body biasing (FBB) lowers $|V_T|$ and is used for low-V_T devices, while Reverse-body biasing (RBB) increases $|V_T|$ and is used for high-V_T devices. However, as seen in Figure 2.3, limited biasing outside this convention is possible as long as the inter-well diodes are not forward biased [11]. The actual body bias range is technology-specific and must be checked as applying V_B outside this range may result in issues with the entire SoC.

Body biasing can be applied both staticlly and dynamicly. An expression for V_T for a FDSOI transistor is shown in Equation 2.1;

$$V_{T_{sat}} = V_{T0} + r(V_{B0} - V_B) - SCE - DIBL \tag{2.1}$$

where V_{T0} is due to the front face, $r(V_{B0} - V_B)$ is the effects of the back gate biasing and SCE and DIBL is short channel effect and drain induced barrier lowering respectively. $r(V_{B0} - V_B)$ can be further broken down to the body factor (r), the effect on V_T based on static back-gate conditions (V_{B0}) and the back gate bias voltage (V_B). A detailed description of these can be found in [10].

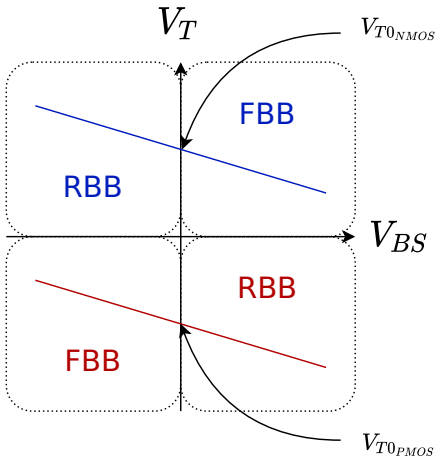


Figure 2.2: Forward and Reverse Back Bias, body-source voltage V_{BS}

The low thickness of the BOX in UTBB technologies increases these effects compared to technologies with thicker insulating layers.

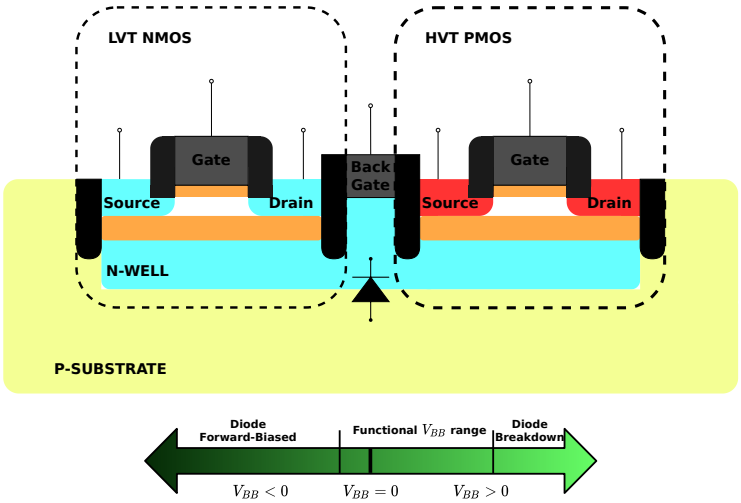


Figure 2.3: Back bias considerations

Back biasing can allow for variable MOS-capacitors. Adjusting V_B impacts the generation of the inversion layer or, in the case of FBB, generates a second inversion layer. Applying FBB, therefore, increases the MOS capacitance at a set V_{gs} while the opposite is true when applying RBB [11].

2.2 Capacitive Micro-machined Ultrasound Transducer

Advances in fabrication procedures of flexible components on silicon have made Capacitive Micro-machined Ultrasound Transducers (CMUTs) a viable alternative to the more traditional piezoelectric-based transducers in ultrasound probes [12]. Figure 2.4 shows the general construction of a CMUT, which is a parallel plate capacitor with the top electrode attached to a flexible layer [13]. The general

equation for a parallel plate capacitor, Equation 2.2, shows the relationship of the distance between the plates, d, and the charge, Q, and voltage, V, across the plates. In a receiver configuration, a change in d must either result in a change in V or Q, which in turn induces a current, I. This allows for either current- or voltage-mode receivers.

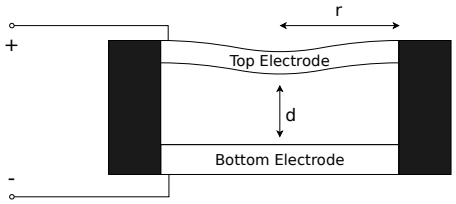


Figure 2.4: CMUT [1]

$$C = \frac{Q}{V} = \epsilon\frac{A}{d} = \epsilon\frac{2\pi r^2}{d} \tag{2.2}$$

A CMUT is a mechanical-electrical component and must be analyzed as such. A lumped circuit model, [14], models the mechanical properties of the CMUT with electrical components so that the equations can relate the electrical and mechanical properties of the transducer. Equation 2.3 relates the speed of the membrane, $\dot{u}$, to the output current, I, of the CMUT. A low impedance load minimizes the change in V_{out}, simplifying the equation to $I \approx \phi\dot{u}$.

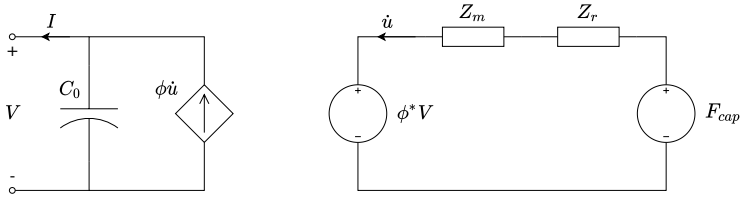


Figure 2.5: CMUT lumped component model

$$I = -j\omega C_0 V_{out} + \phi\dot{u} \tag{2.3}$$

2.3 Current Mirror

The current amplification in a current mirror is typically expressed as $A_{CM} = \frac{i_{out}}{i_{in}} = \frac{(W/L)_2}{(W/L)_1}$, but looking at the small signal model in Figure 2.6, the small signal gain is more accurately expressed as the transconductance ratio of the reference, M_1 and output, M_2, transistors, as seen in Equation 2.4.

$$A_{CM} = \frac{i_{out}}{i_{in}} = \frac{g_{m2}}{g_{m1}} \tag{2.4}$$

As seen from Equation 2.5, $g_m \propto \mu C_{ox}, \left(\frac{W}{L}\right), V_{eff}$ [15, Chapter 1.3.3]. As described in section 2.1, FDSOI enables adjusting V_{th} through back gate biasing. Using this

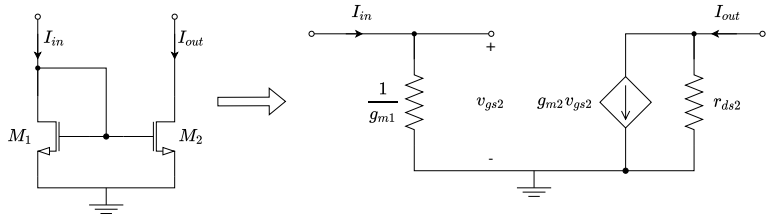


Figure 2.6: Current mirror small signal

technology, continuos variable gain can therefore be achieved through dynamic body biasing.

$$g_m = \mu C_{ox} \frac{W}{L} (V_{eff}) \tag{2.5}$$

The large signal gain, however, is derived from Equation 2.6. Therefore, adjusting V_T to control the gain of the current mirror consequently adjusts $I_{IN} \propto V_{eff}^2$ and $i_{in} \propto V_{eff}$.

$$\frac{I_2}{I_1} = \frac{\left(\frac{W}{L}\right)_2 (V_{eff_2})^2}{\left(\frac{W}{L}\right)_1 (V_{eff_1})^2} \tag{2.6}$$

2.4 Folded Voltage Follower

A folded voltage follower (FVF), is a variation of a common drain amplifier topology with reduced output resistance due to the shunt feedback of M2. A detailed analysis of the FVF topology is found in [16].

The output resistance, R_{out}, of the FVF is given by Equation 2.7. The source resistance, R_B, is decided by the current mirror topology used to generate the bias current, I_B. A simple current mirror results in $R_B = r_{ds}$ resulting in $R_{out} \approx \frac{2}{g_{m1} g_{m2} r_{ds1}}$, while very large values of R_B, such as the output resistance of a cascode current mirror, results in $R_{out} \approx \frac{1}{g_{m1} g_{m2} r_{ds1}}$ [16].

$$R_{out} = \frac{\frac{1}{g_{m1}} \left(1 + \frac{R_B}{r_{ds1}}\right) || r_{ds2}}{g_{m2} \left(R_B || g_{m1} r_{ds1} r_{ds2}\right)} \tag{2.7}$$

The FVF is a two-pole system with a dominant pole, ω_{p_2}, at node (2), and a high-frequency pole, $\omega_{p_{out}}$, at node (1). In a negative feedback system, such as the FVF, the dominant pole must limit the gain-bandwidth product, defined as $GB = \frac{g_{m_1}}{C_2}$ for FVF, so it is between one-half and one-third of the high-frequency pole of the open-loop to ensure stability [17]. The stability condition depends on R_B. A simple current mirror implementation has the stability condition given by Equation 2.8a, while for higher R_B implementations or large capacitive loads the expression is modified to Equation 2.8b [16].

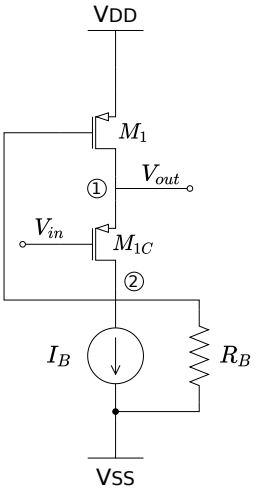


Figure 2.7: PMOS FVF Cell

$$\frac{C_{out}}{C_1} < \frac{g_{m1C}}{4g_{m1}} \tag{2.8a}$$

$$\frac{C_{out}}{C_1} < \frac{1}{g_{m1}r_{ds1}} \tag{2.8b}$$

Figure 2.8 shows a current mirror utilizing the FVF Cell. The input resistance, $R_{in_{FVFStandard}}$, of this current mirror is significantly lower than the standard current mirror topologies, and is equal to the standard FVF buffer output resistance [18], shown in Equation 2.7:

$$R_{in_{FVFStandard}} \approx \frac{1}{g_{m1}g_{m2}r_{ds1}} \tag{2.9}$$

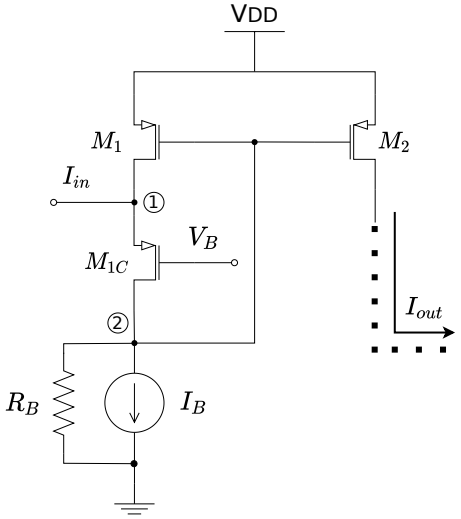


Figure 2.8: FVF Current Mirror

The input resistance can be further improved by using an amplifier to actively bias M_{1C}, as seen in Figure 2.9. Looking at the node resistance at node X of the improved

CCII in [16], the input resistance of the activly biased FVF current mirror is given by;

$$R_{in_{Active}} = \frac{R_{in_{FVFStandard}}}{|A|} \approx \frac{1}{g_{m1}g_{m2}\left(r_{ds3}||r_{ds1}\right)|A|} \tag{2.10}$$

assuming that A is negative and $|A| >> 1$.

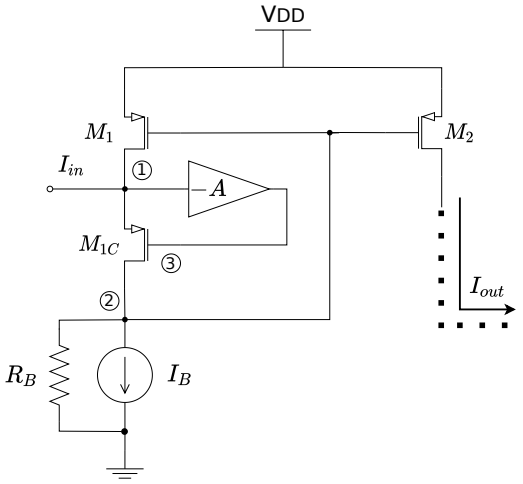


Figure 2.9: FVF Current Mirror with acive biasing circuit

The cascode transistor and active bias can be added to the output branch to force $V_{DS1} = V_{DS2}$. This increases the output resistance of the current mirror while increasing accuracy and linearity as the channel length modulation effect is minimized [19].

2.5 Folded Cascode Gain Stage

The gain of a cascode gain stage is derived in [15, Chapter 3.7]. A schematic of the folded voltage cascode gain stage is shown in Figure 2.10. Comparing the small-signal models of the telescopic- and folded-cascode gain stages in Figure 2.11, it is clear that the same expressions derived for the telescopic cascode gain stage holds for the folded cascode gain stage when substituting r_{ds1} with $r_{ds1}||r_{ds2}$. The expressions for gain and port-resistances are given by Equation 2.11 and Equation 2.12 respectively.

$$A_{V_{cas}} = \frac{v_{out}}{v_s}\frac{v_s}{v_{in}} = -g_{m1}g_{m3}\left(r_{ds1}||r_{ds2}||r_{cas}\right)\left(r_{ds3}||r_{ds4}\right) \tag{2.11}$$

$$R_{in} \approx \infty, R_{out} = \left(r_{ds3}g_{m3}\left(r_{ds1}||r_{ds2}\right)\right)||r_{ds4} \tag{2.12}$$

($r_{cas} = \frac{g_{m3}}{1+\frac{r_{ds4}}{r_{ds3}}}$ is derived in [15, Chapter 3.7] as r_{in2}.)

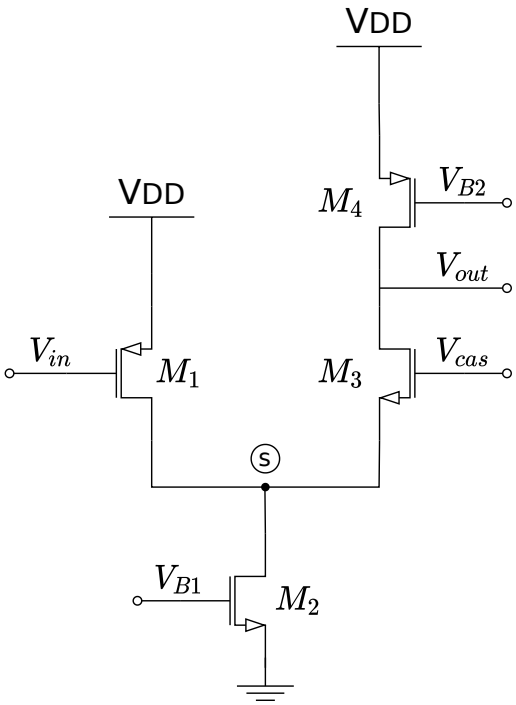
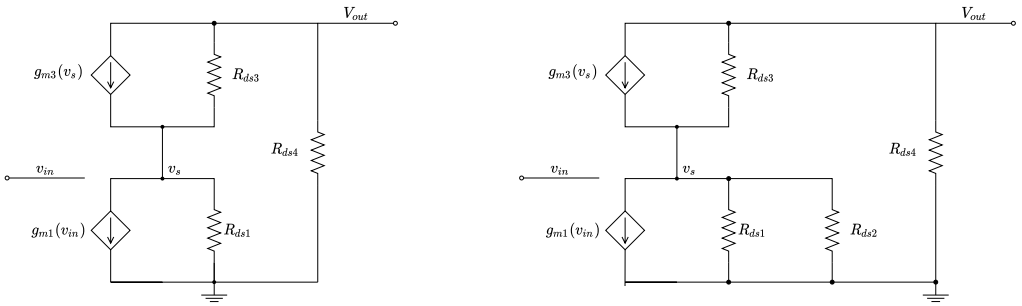


Figure 2.10: Folded Cascode Amplifier



(a) Small signal model for telescopic cascode gain stage

(b) Small signal model for folded cascode gain stage

Figure 2.11: Small signal model for cascode gain stages

The bandwidth of the cascode gain stage is estimated in [15, Chapter 4.3]. Substituting r_{ds1} with $r_{ds1}||r_{ds2}$ again, the high-frequency model of the telescopic cascode gain stage can be used for the folded cascode gain stage. Summarizing the time constants of all the nodes in the amplifier we get:

$$\begin{aligned}\tau_{total} = \tau_1 + \tau_2 + \tau_3 + \tau_4 \approx &\left(g_{m3}\left(r_{ds1}||r_{ds2}\right) r_{ds3}||r_{ds4}\right) C_{out} + \left(r_{ds1}||r_{ds2}||r_{cas}\right) C_s \\ &+ R_{in}\left[1 + g_{m1}\left(r_{ds1}||r_{ds2}||r_{cas}\right)\right] C_{gd1} + C_{gs1} R_{in}\end{aligned} \tag{2.13}$$

This can then be used to approximate ω_{-3dB} in Equation 2.14.

$$\omega_{-3dB} = 1/\tau_{total} \tag{2.14}$$

2.6 Feedback

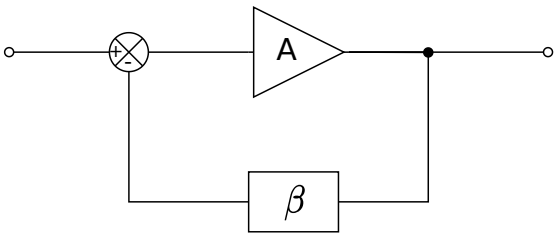


Figure 2.12: Ideal negative feedback loop

Figure 2.12 shows a general negative feedback system. The open-loop gain, L, of the system is defined in Equation 2.15, where A is the gain of the amplifier and β is the gain of the feedback. There are several benefits to a negative feedback system, such as better linearity, increased bandwidth and lower gain variability. However, feedback can lead to instability in the circuit [15, Chapter 5.1].

$$L = A\beta \tag{2.15}$$

From Equation 2.15, the magnitude (Equation 2.16) and phase (Equation 2.17) of L can be expressed. $\angle L(\omega_0)$, the phase of the loop-gain at unity gain frequency ($|L(\omega_0)| = 1$), is used to express the stability of the negative feedback system. For an unconditionally stable negative feedback system, the phase margin (Equation 2.18) must be greater than zero. However, oscillations may still occur at low phase margins, which is why phase margins between 45° and 90° degrees are often required [15, Chapter 5.2].

$$|L(\omega)| = |A(\omega)|\beta \tag{2.16}$$

$$\angle L(\omega) = \angle A(\omega) + \angle\beta \tag{2.17}$$

$$PM = \angle L(\omega_0) + 180^\circ \tag{2.18}$$

2.7 Pole-Zero Analysis

Pole-Zero analysis is useful for assessing the frequency response of a system. Several properties of the circuit can be explored, like stability, bandwidth and overshoot. This is especially useful for complex systems, where an analytical model of the transfer function is difficult or impractical to develop. Poles and zeros can be extracted by simulation and used to inform iterations until the desired frequency response is achieved.

All the poles of a stable circuit are in the left half-plane(negative real part). The poles of a system are either real or complex conjugate pairs. Complex conjugate pairs with $Q > 0.5$ give rise to oscillations, as seen in Figure 2.13 [15, Chapter 4.1].

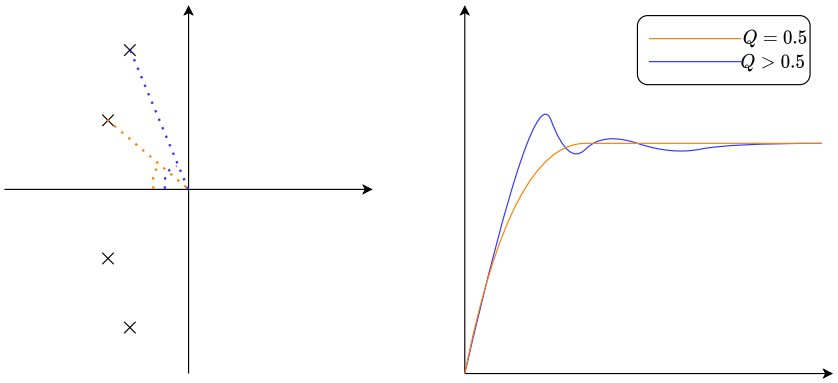


Figure 2.13: Complex conjugate poles with different Q-factors and corresponding step response

Left half-plane zeros typically improve the phase margin as phase lead is introduced. Right half-plane zeros, however, introduce phase lag, which typically negatively impacts the phase margin [15, Chapter 4.2].

2.8 Noise in CMOS

Noise models for each circuit component can be found in [15, Chapter 9]. Only the most significant subchapter for the VGA will be discussed in more detail in this report.

2.8.1 MOSFET

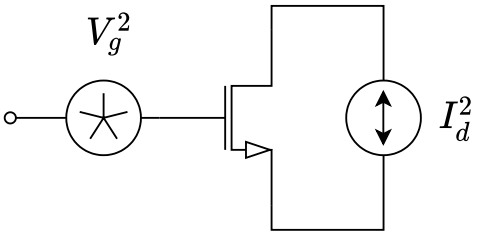


Figure 2.14: Noise model of MOSFET

A typical MOSFET is modeled with two separate noise sources, as seen in Figure 2.14. This is due to two distinct phenomena giving rise to two types of noise with different properties. Flicker noise, V_g^2, is frequency-dependent and is typically modeled as a voltage noise source connected to the gate of the transistor, and is expressed in Equation 2.19. The flicker noise is most significant at low frequencies, as seen in Figure 2.15 [15, Chapter 9.3.4].

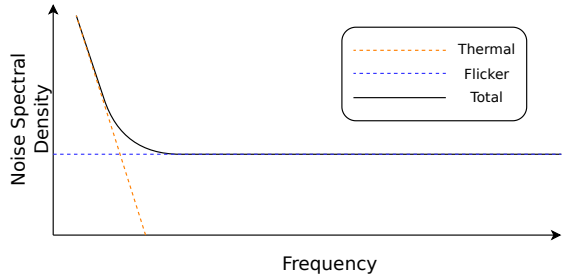


Figure 2.15: Noise spectral density of MOSFET

$$V_g^2(f) = \frac{K}{WLC_{ox}f} \tag{2.19}$$

Thermal noise, I_d^2, is noise that occurs because of the resistive effects of the channel and is modeled as a current noise source in parallel with the channel. As seen in Figure 2.15, the thermal noise is frequency-independent and dominates at higher frequencies, which is reflected in Equation 2.20 [15, Chapter 9.3.4]. g_m and γ are dependent on transistor parameters. γ is dependent on short channel properties and can be difficult to predict analytically, contrary to g_m, which is defined in Equation 2.5.

$$I_d^2(f) = 4kT\gamma g_m \tag{2.20}$$

2.8.2 Noise Figure

One metric for noise performance in amplifiers is how much output noise is contributed by the amplifier compared to the output noise contributed by the source. This metric is called noise factor, $F(f)$ [15, Chapter 9.3.8]. Figure 2.16 shows a setup for determining the noise factor. Equation 2.21 expresses the output noise power of the system with a noisy amplifier, while Equation 2.22 shows the output noise power of the system with a noiseless amplifier. I_{so}^2 is the source noise and I_{ao}^2 is the output noise of the amplifier.

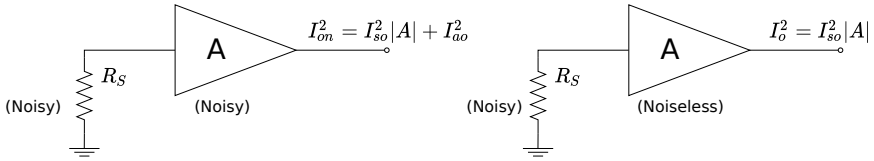


Figure 2.16: Setup for determining noise factor

$$I_{on}^2 = I_{so}^2|A| + I_{ao}^2 \tag{2.21}$$

$$I_o^2 = I_{so}^2|A| \tag{2.22}$$

$F(f)$ is then expressed as the ratio of these:

$$F(f) = \frac{I_{on}^2}{I_o^2} \tag{2.23}$$

It is often preferable to express the noise factor in decibels, which is the noise figure, $NF(f)$, of the system:

$$NF(f) = 10\log_{10}[F(f)]dB \tag{2.24}$$

2.9 Harmonic Distortion

Harmonic distortion occurs due to nonlinearities in a system where the harmonics of the input signal appear on the output signal. In CMOS circuits, the main drivers for harmonic distortion are the derivatives of I_d, ie. the second harmonic component of the output signal is generated by the second derivative of I_d. Therefore, minimizing the derivative components of I_d, which contributes to the most significant harmonic components, is important in single-ended circuits [20].

2.10 Layout

A silicon wafer will have variations in its electrical properties, both across different production batches and across each individual silicon wafer. The consistent repeatable variation seen across all chips in a production line is called systematic variation and can be minimized by proper layout techniques [15, Chapter 2.3]. Different techniques can be employed for both minimizing mismatch between critically matched transistors and reducing variation between pre- and post-layout simulations [21].

Interdigitated and common-centroid layout patterns both improve matching as they reduce the impact of doping gradients in the wafer. Both techniques split the devices, such that, in the case of interdigitated layout, the devices can be interleaved, while in common-centroid layout the devices are distributed equidistantly from a center point. Devices that are too small to be split into multiple devices can not be matched in this way, but will benefit from being close together as this minimizes the effects of the doping gradient [22].

Dummy elements help mitigate differences in devices due to uneven diffusion around the edges of a transistor. Additional unconnected devices are added around the active device so that the edges of the device have consistent diffusion on all sides [22]. This difference between a device with and without dummy elements is illustrated in Figure 2.17.

The distance from the device and the edge of the well impacts matching due to doping irregularities, which is known as well proximity effects (WPE). For this

reason, the distance from a device to the well-edge should be kept consistent on all sides [21]. Fully encircling the active region of the transistor with contacts, often called a guard ring, keeps the edge conditions consistent, reducing WPE, and provides a low resistance contact to the body of the transistor, ensuring a constant potential across the entire transistor [15, Chapter 2.4].

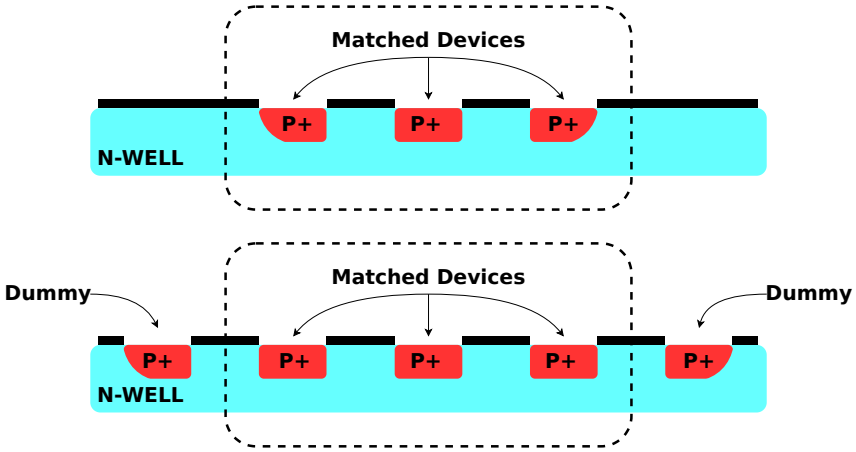


Figure 2.17: Impact of dummy devices

Table 3.1: Specifications for the VGA

Supply Voltage	VDD	0.8	V
Bandwidth	BW	20	MHz
Center Frequency	f_0	10	MHz
Settling Time ($\pm 5\%$)	t_{set}	15	ns
Gain	A_{VGA}	1 - 10	
Noise Figure	NF_{min}	3	dB
Second Harmonic Distortion	$HD2$	-40	dB
Power consumption	P_{VGA}	Minimize	μW
Area		Minimize	μm^2

3 Implimentation

A schematic of the VGA is shown in Figure 3.1. Schematics with all component sizes can be found in Appendix B.

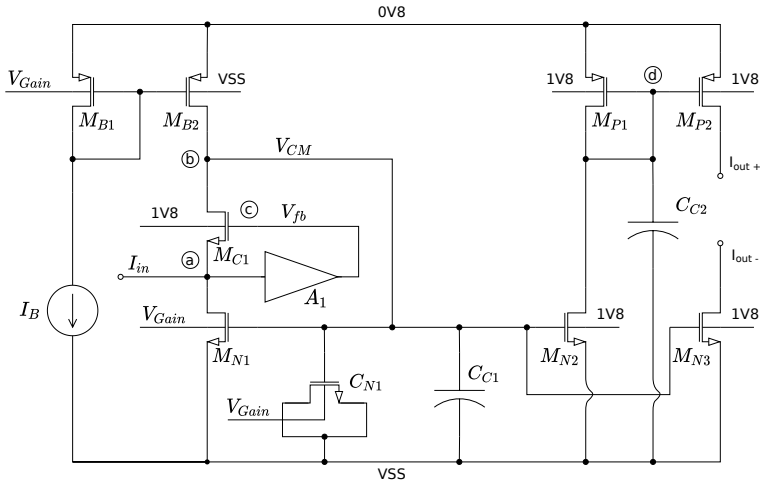


Figure 3.1: Schematic of the proposed VGA

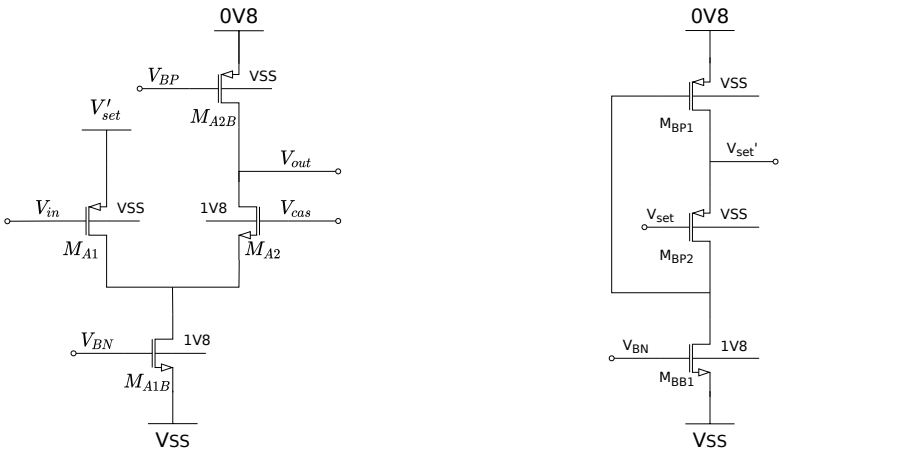
3.1 Specifications

Due to layout considerations of the CMUT transducers, the number of parallel CMUTs used to drive the VGA is limited to a quadratic number to maintain maximum area density. The number of CMUTs used in this implementation is nine, as this provides a large enough signal strength to meet noise requirements while keeping the capacitance at node (a).

The analog front-end requires that the VGA has a single-ended input stage and differential output stage. For ease of integration and reduced power consumption, a pseudo-differential output stage is chosen.

The specifications of the VGA are presented in Table 3.1. The gain range of the VGA must be continuous and is adjusted by an analog voltage.

3.2 Active Biasing Circuit



(a) Folded Cascode Amplifier (b) Folded Voltage Follower Buffer

Figure 3.2: Active Biasing Amplifier

The bias amplifier, A_1, is a single-ended folded cascode gain stage amplifier, depicted in Figure 3.2a. The cutoff frequency, $f_{-3dB_{A_1}}$, of A_1 must be higher than the desired cutoff frequency of the VGA, $f_{-3dB_{VGA}}$. As such, a cutoff frequency of $f_{-3dB_{A_1}} > 20MHz$ is chosen. To achieve this, high g_m transistors is required, but the input capacitance of A_1 must be kept low so the stability of the VGA at high bandwidth is compromised due to high input capacitance (see stability criteria in Equation 2.8). Given these restrictions, the amplifier is biased so that $I_{d_{A1}} = 20\mu A$, whereas $I_{d_{A2}} = 10\mu A$ as its gate capacitance is less of a consideration. Inserting the simulated values for g_m and r_{ds} in Equation 2.11 gives:

$$A_{Bias} \approx 15.6dB \tag{3.1}$$

Based on simulation data, however, the gain is significantly higher than this and thus, the dimensioning of A_1 has been largely based on an iterative design process where its impact on the VGA performance is most heavily weighted.

The resistive component of $\tau_{[1-4]}$ in Equation 2.13 is also calculated using the simulated values for g_m and r_{ds} to highlight the sensitivity to each of the capacitive component of $\tau_{[1-4]}$. This is useful in identifying the nodes that limit the bandwidth. These values are presented in Equation 3.2 and shows that the amplifier is most sensitive to C_{gd1} and C_s when compared to Equation 2.13.

$$\begin{aligned} R_{\tau_1} &\approx 18k\Omega \\ R_{\tau_2} &\approx 71k\Omega \\ R_{\tau_3} &\approx 34k\Omega \\ R_{\tau_4} &\approx 1.3k\Omega \end{aligned} \tag{3.2}$$

A_1 and the FVF stage formed by M_{N1}, M_{C1} and M_{B2} form a negative feedback system. Relating this to section 2.6, the feedforward component of the system is A_1

while the feedback consists of the FVF stage. As presented in section 2.4, the FVF cell is analyzed as a common drain topology with a gain $A_{FVF} \approx 1 = \beta$, resulting in a loop gain of $L = A\beta \approx A$. The stability of this loop is dependent on low phase shift in both A_1 and the FVF feedback.

The FVF buffer in Figure 3.2b, is used to generate V'_{set}, which supplies M_{A1}. M_{BP2} and M_{A1} are matched and biased with the same bias current, I_{Buffer}, and will therefore source the same current for the same V_{gs}. Any mismatch between V_{IN} and V_{set} is counteracted by the negative feedback system so that V_{IN} can be forced to a specific bias voltage, without using a more traditional differential amplifier structure which has a higher power consumption.

A benefit of this amplifier structure is that the FVF buffer can supply multiple amplifiers. This spreads the power consumption and area of the FVF buffer across multiple VGAs so that the total is divided across all circuits. As such, this topology is highly efficient in applications with multiple instances of the same circuit, like ultrasonic imaging probes. The stability criteria presented in Equation 2.8 is the limiting factor in the number of circuits that can be powered by the same buffer.

The ability to adjust V_{IN} can be useful in calibration and can even be adjusted with the gain so the operating region of M_{N1} is adjusted for stability and linearity.

3.3 VGA

The input stage of the VGA is based on the input stage of the FVF current mirror presented in [19]. This topology is selected because of the high gain of the folded cascode gain stage, A_1. Equation 2.10 shows that low R_{in} is achievable without high $g_{m_{N1}}$ as long as the gain $|A_{Bias}|$ of A_1 is large. Keeping $g_{m_{N1}}$ low generates low thermal noise in M_{N1}, as derived in Equation 2.20.

Figure 3.3 shows a simplified model where only the thermal noise sources of M_{N1} and M_{B2} are included. These are the dominant noise sources of the amplifier as these noise currents are introduced in parallel with the noise current from the CMUT and amplified through the VGA. The thermal noise of M_{C1} is neglected as cascode transistors typically generate low noise due to their feedback properties. The noise figure (NF_{min}) is evaluated at a VGA gain of $A_{VGA} = 10$ as this is the VGA configuration where the input signal power is close to the noise floor of the CMUT. $NF_{min} < 3dB$ is achieved if $I_{in}^2 > I_{N1}^2 + I_{B2}^2$ in this noise model. Factoring in the contribution of other noise sources, some margin must be added to this condition.

The output stage of the main current mirror consists of two simple current mirror transistors in M_{N1} and M_{N2}. The significant increase in power consumption caused by adding additional biasing amplifiers outweighs the increased linearity and accuracy associated with the cascode output stage. The single-ended output is mirrored through M_{N2} to M_{P1} and M_{P2} to achieve a pseudo-differential output current between M_{N3} and M_{P2}.

V_{Gain} is also connected to the back gate of M_{B1} to provide a gain-dependent bias current, I_B. I_B is scaled inversely proportional to the gain of the amplifier to increase

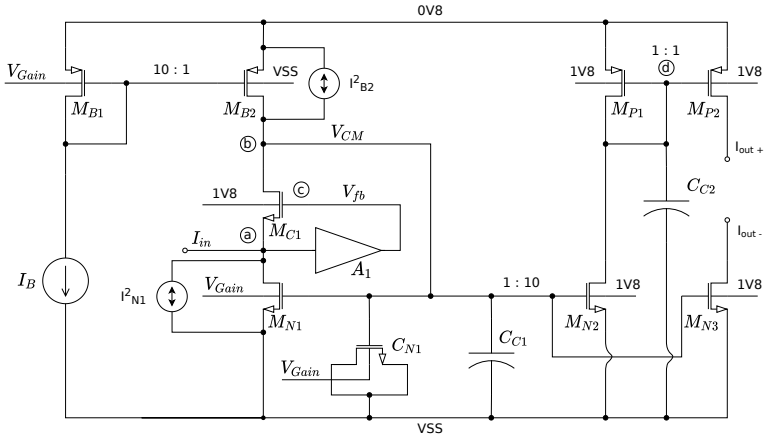


Figure 3.3: VGA Noise

the dynamic range of the amplifier at low gains, while maintaining low $g_{m_{N1}}$ and $g_{m_{B1}}$ at high gains. This also reduces the change in operating points in the VGA, as the voltage at node (b) can be kept more stable.

As the back gates of M_{N1} and M_{B1} are both driven by the same voltage, V_{Gain}, both transistors must be in the same well, based on the FBB and RBB conventions presented in section 2.1. For ease of process on a p-substrate, n-well devices are chosen for both N- and P-devices to avoid the need for deep N-wells. M_{N1}, M_{N2} and M_{N3} must therefore be low-V_T devices while M_{B1} and M_{B2} are high-V_T devices. Both M_{N1} and M_{B1} break the body bias convention presented in section 2.1 while $V_{Gain} < 0.8V$ and M_{B2} is always biased in FBB against the convention. However, this is within the specifications of the 22nm FDSOI process as the inter-well diode should not yet be reverse biased at these voltages.

A_{VGA}, is adjusted by applying dynamic body biasing to M_{N1} with V_{Gain}. V_{Gain} is an analog control voltage ranging from $0V$ to $1.8V$. The base transistors of the 22nm FDSOI technology can not operate at $VDD > 0.8$, meaning I/O transistors must be used to generate V_{Gain}.

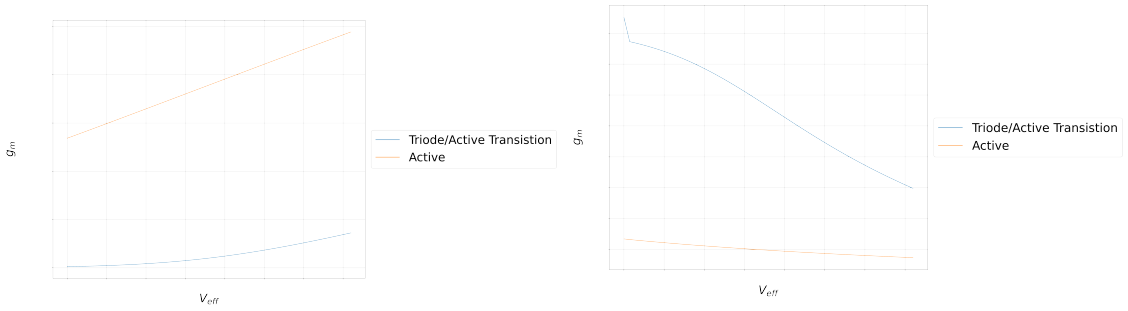
Applying FBB to NMOS transistors reduces V_T and therefore g_m. A back bias voltage of $1.8V$ is applied to M_{N2} and M_{N3} such that increasing $g_{m_{N1}}$ reduces A_{VGA}. This is based on a noise consideration so that $g_{m_{N1}}$ is lowest at $A_{VGA} = 10$. Unity gain is achieved by matching the back-bias voltage of M_{N1}, M_{N2} and M_{N3} ($V_{Gain} =$ 1.8V). The single-ended to differential conversion doubles the output amplitude compared to a single-ended to single-ended implementation. A current mirror gain of $A_{CM_N} = 1/2$ is needed which sets the following condition for the W/L-ratio of M_{N1}, M_{N2} and M_{N3}:

$$\frac{(W/L)_{M_{N2},M_{N3}}}{(W/L)_{M_{N1}}} = \frac{1}{2} \tag{3.3}$$

The transistor width of M_{N1}, M_{N2} and M_{N3} is set small to minimize g_m, but large enough to not be affected significantly by the narrow channel effect.

To reach a high gain range, the derivative of $g_{m_{N1}}$ must be large, while achieving a low NF_{min} requires $g_{m_{N1}}$ itself to be low. In the transition between triode- and active-region, g_m increases exponentially with V_{eff} and g_m is low, as shown in Figure 3.4a. Plotting $\frac{g'_m}{g_m}$ in Figure 3.4b also implies that biasing M_{N1} at the transition between the triode- and active-region is beneficial, as g_m will have a high rate of change compared to its magnitude. The derivative of g_m is also small in this region, which is beneficial for lowering the second harmonic distortion ($HD2$). The DC input voltage of $V_{IN} = V_{set} = 130mV$ is set so that M_{N1} is biased at the edge of the triode region. The length of M_{N1}, M_{N2} and M_{N3} is then adjusted until the desired range of A_{VGA} is met.

A secondary effect of this biasing of M_{N1} is that, based on Equation 2.4, the exponential increase of $g_{m_{N1}}$ will result in a dB-linear gain response. As ultrasound pulses through are attenuated both to- and from the reflection point, the amplitude is reduced exponentially and thus dB-linear gain compensation is favorable.



(a) g_m as a function of V_{eff}

(b) $\frac{g'_m}{g_m}$ as a function of V_{eff}

Figure 3.4: Properties of g_m and $\frac{g'_m}{g_m}$ in active region and the transistion region between triode and active region as a function of V_{eff}

Many of the same considerations made when dimentioning M_{N1}, M_{N2} and M_{N3} apply when dimentioning M_{B1} and M_{B2}. Biasing the back gate of M_{B1} with V_{Gain} increases $|V_T|$. Low I_B is desired when A_{VGA} is high, to reduce I_{B2}^2. Based on these observations, at $V_{Gain} = 0V$, the current mirror gain of the bias current mirror must be $A_{CM_B} = \frac{1}{10}$. This condition sets the (W/L)-ratio of M_{B1} and M_{B2} as:

$$\frac{(W/L)_{M_{B2}}}{(W/L)_{M_{B1}}} = \frac{1}{10} \tag{3.4}$$

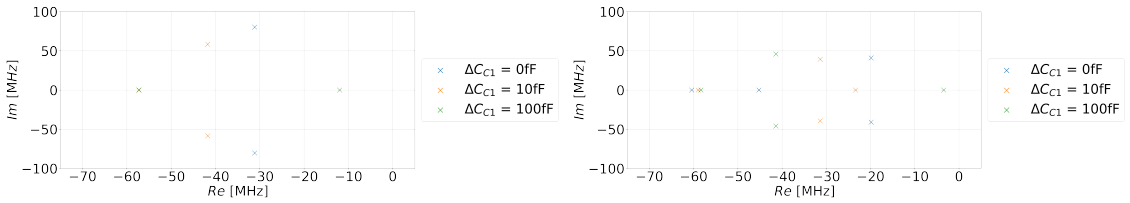
In the same way as for M_{N1}, M_{N2} and M_{N3} the width is set small while the length is set accordingly so that the desired I_B-range is met. Based on simulations the range of I_B was set from $I_B = 75nA$ for $A_{VGA} = 10$, to $I_B = 320nA$ for $A_{VGA} = 1$.

The simple cascode current mirror for supplying I_B is chosen as M_{B2} lacks headroom as it is a high-V_T device. A cascode transistor can therefore reduce the accuracy of I_B if M_{B2} is driven into the triode region. Substituting M_{B1} and M_{B2} with lower V_T devices can enable the use of a cascode current mirror, but R_{in} is considered low enough to reach specification with the simple current mirror topology and so the

added complexity is considered unnecessary.

M_{P1} and M_{P2} form a basic PMOS current mirror and are dimensioned based on simulation data to achieve the best possible noise figure and linearity in the VGA.

Stability can become an issue in an FVF current mirror with i small bias current. A capacitor, C_{C1}, is added at node (b) based on the stability criteria of an FVF presented in Equation 2.8. Its effects can be seen in the pole plot in Figure 3.5, as the Q-factor of the complex conjugate pair is reduced as more capacitance is added. The simulation data in Figure 3.5a suggests that additional capacitance is required at low gain settings. A variable capacitor, C_{N1}, is added in parallel with C_{C1} to increase the capacitance in node (b) at lower values of A_{VGA}. The g_m ratio of M_{N1} and M_{C1} changes with A_{VGA}, which is the reason for the variability of the Q-factor observed across the A_{VGA} range. The capacitor is an NMOS capacitor controlled by V_{Gain} and behaves as described in section 2.1.



(a) $A_{VGA} = 1$ (b) $A_{VGA} = 10$

Figure 3.5: Pole plot of VGA if C_{C1} is increased by ΔC_{C1}

In section 2.4 it is stated that increasing the capacitance at node (b) reduces the gain-bandwidth product (GB_{VGA}). As C_{in} is large and is decided by the capacitance of the CMUT array and all g_m of the input branch must be low to reduce noise, increasing the high-frequency pole at node (a) is not a viable option. Hence, the bandwidth is limited by I_B. As I_B must be low to reduce noise, reaching the bandwidth specified in Table 3.1 is difficult to achieve with a high phase margin. A tradeoff between oscillations and bandwidth must be made.

As mentioned, the operating point for the VGA changes with gain, which in turn impacts the frequency response of A_1. Depending on the severity, the change in linearity, phase response or gain of the amplifier can impact the stability, noise and linearity of the VGA.

Using the simulated values for g_m and r_{ds} and A_{Bias} from Equation 3.1, a theoretical input resistance is found using Equation 2.10:

$$R_{in} \approx 1.3k\Omega \tag{3.5}$$

3.4 Layout

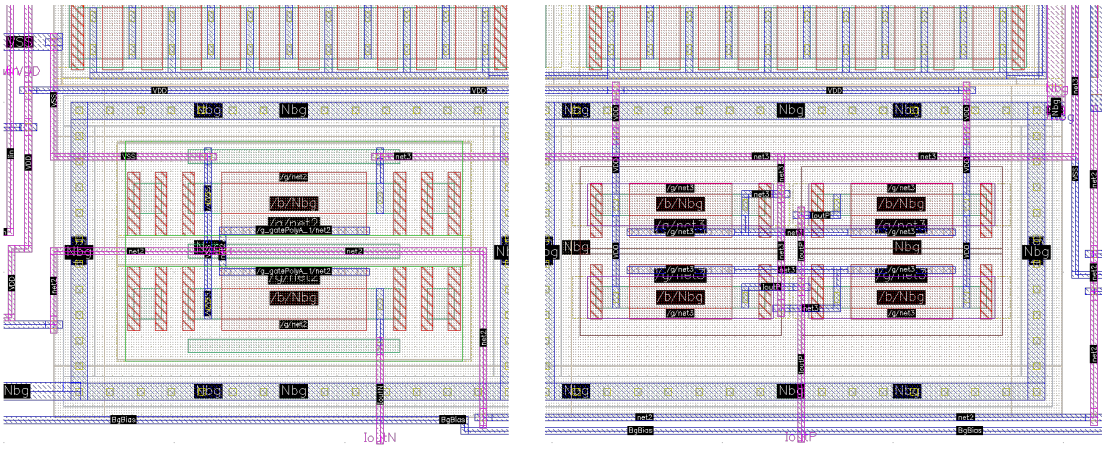
The complete layout of the VGA, Cascode Amplifier and FVF buffer is found in Appendix A. This section will highlight the most significant matching considerations in the layout.

Matching the transistors in current mirrors is essential for consistency between pre- and post-layout performance. As the current mirrir consisting of M_{N1}, M_{N2} and M_{N3}, as well as M_{B1} and M_{B2} uses dynamic biasing for M_{N1} and M_{B1}, they can not all be in the same well and is for this reason not possible to match using layout techniques. However, as dynamic body biasing introduces the option of calibrating the transistors, it is possible to calibrate M_{N1} and M_{B1} in a way that minimizes the effects of mismatch. As such, only M_{N2} and M_{N3}, and M_{P1} and M_{P2} must be matched.

M_{P1} and M_{P2} are laid out in a common centroid configuration, as seen in Figure 3.6b. M_{N2} and M_{N3} are too small to split for a common centroid or interdigitated layout. Instead, they are laid out in close proximity to minimize the mismatch due to wafer doping gradients, as seen in Figure 3.6a. Dummies are added to all sides of M_{N2} and M_{N3} to minimize diffusion effects. Guard rings are added around each pair and, as both pairs share N-Well, one side of the guard ring can be shared.

Care must be taken to keep each transistor at an equal distance from the edge of the well so that WPE affects each transistor equally. The well is extended upwards so that it is shared with M_{MA2} and M_{A1B} of the cascode amplifier and when integrated into the full SoC, the well should therefore be extended downward and utilized by a similarly biased subcircuit. The transistors are oriented in such a way that each similar feature of the matched transistors is the same distance from each well-edge. Extending the well right and left to match distances is not considered necessary because of this.

Several of the remaining transistors, such as M_{C1}, M_{A1} and M_{BP2}, will benefit from layout techniques to minimize the difference between pre- and post-layout properties. Additional matching efforts should be considered if pre- and post-layout simulations show significant differences.



(a) Nmos output current mirror of VGA (b) Pmos output current mirror of VGA

Figure 3.6: Output current mirrors of VGA

The size of the layout for the VGA, the FVF buffer and A_1 is presented in Table 3.2.

The post-layout simulations showed some differences in performance from the pre-

Table 3.2: Size of Layout

	Width [μm]	Length [μm]	Area [μm^2]
VGA	18.842	6.252	117.8
Folded Cascode Amplier	11.704	4.203	49.19
FVF Buffer	8.812	3.266	28.78

layout simulations, but this was improved by changing V_{cas} from $715mV$ to $800mV$.

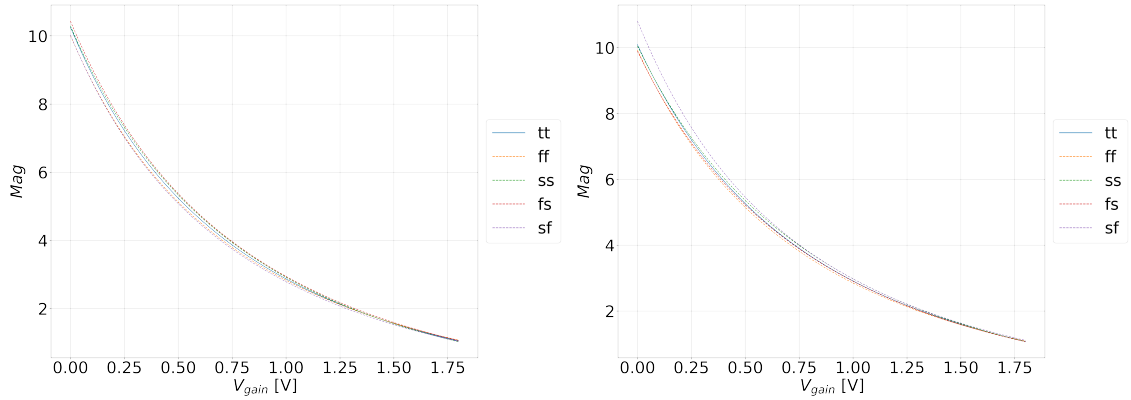
4 Results and Discussion

All the testbenches are shown in Appendix C

4.1 A_{VGA} Range

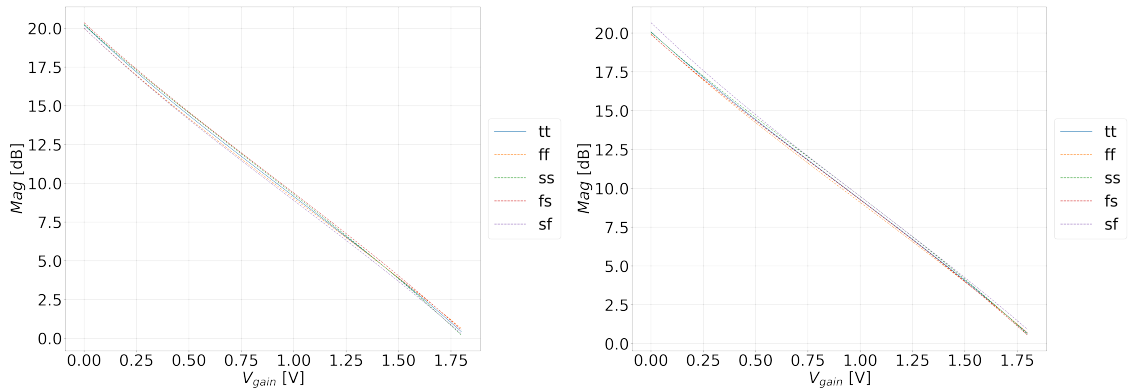
The gain range of A_{VGA}, as well as its unlinear relationship to its control voltage V_{gain}, can be seen in Figure 4.1. Figure 4.2 shows that A_{VGA} is instead approximately dB-linearly proportional to V_{Gain}, as expected when biasing M_{N1} at the transition between the triode- and active-region.

A_{VGA} is quite insensitive to process variation both in pre- and post-layout simulations. The process variation is especially low at low gains. The post-layout simulations show some deviation VGA gain in the sf-corner, but it is not deemed sufficient to necessitate improvements to the layout.



(a) Pre-Layout Simulation (b) Post-Layout Simulation

Figure 4.1: A_{VGA} (linear) against V_{gain}



(a) Pre-Layout Simulation (b) Post-Layout Simulation

Figure 4.2: A_{VGA} (dB) against V_{gain}

4.2 Capacitive Load of Gain Control Port

The back gate capacitance of M_{N1}, M_{B1} and C_{N1} combined is shown in Figure 4.3 for $A_{VGA} = \{1, 5, 10\}$. This shows that the maximum capacitive load on the signal generator for V_{gain} is $C_{bg} \approx 22fF$.

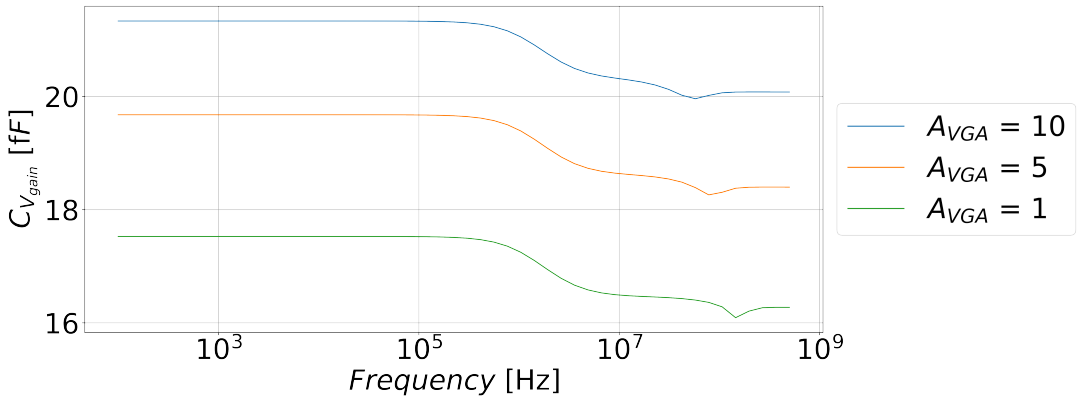


Figure 4.3: Simulated capacitance of VGA gain control port

4.3 Input Resistance

Figure 4.4 shows that the input resistance, R_{in}, is reduced as A_{VGA} is reduced, because $g_{m_{N1}}$ and $g_{m_{C1}}$ is increased as I_B is increased. Equation 2.3 implies that the reduction of R_{in} increases the amplitude of the input current,i_{in}. However, the testbench is configured as the electrical side of Figure 2.5 and tas such, i_{in} should react as the CMUT current would react to changes in R_{in}.

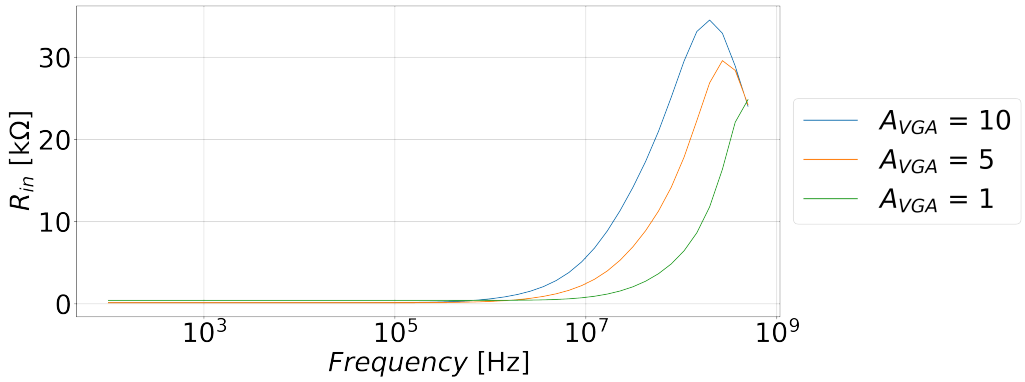


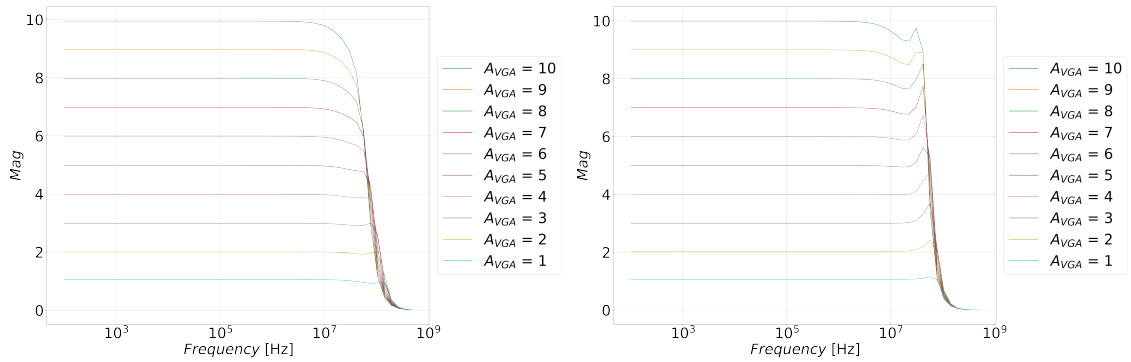
Figure 4.4: Simulated R_{in}

4.4 Magnitude Response of VGA

The magnitude response of the VGA is simulated in Figure 4.5. Both pre- and post-layout simulations show a flat response within the bandwidth specified in section 3.1. The bandwidth increases as the gain is reduced, as expected, as increasing $g_{m_{N1}}$

increases GB_{VGA}. This decreases the phase margin of the FVF, causing higher overshoot and longer oscillations as seen in Figure 4.6. Adding C_{N1} in parallel with C_{C1} reduces the bandwidth when A_{VGA} is low as its capacitance is proportional to V_{gain}. A switchable capacitor array at node b, or improving the variable capacitor range of C_{N1}, can improve the phase margin when A_{VGA} is low or for production runs operating in unfavorable corners. This, however, increases circuit complexity, power consumption and area.

Post-layout simulations (Figure 4.5b) show a more pronounced overshoot than the pre-layout simulations (Figure 4.5a). This is likely due to increased capacitance at node a or a difference in operating point in the active biasing circuit. As the phase margin of the FVF must be low to maintain the bandwidth at $BW = 20MHz$, adding more capacitance at node b to reduce the overshoot may not be a viable solution.



(a) Pre-Layout Simulation

(b) Post-Layout Simulation

Figure 4.5: Magnitude response of VGA across A_{VGA} range.

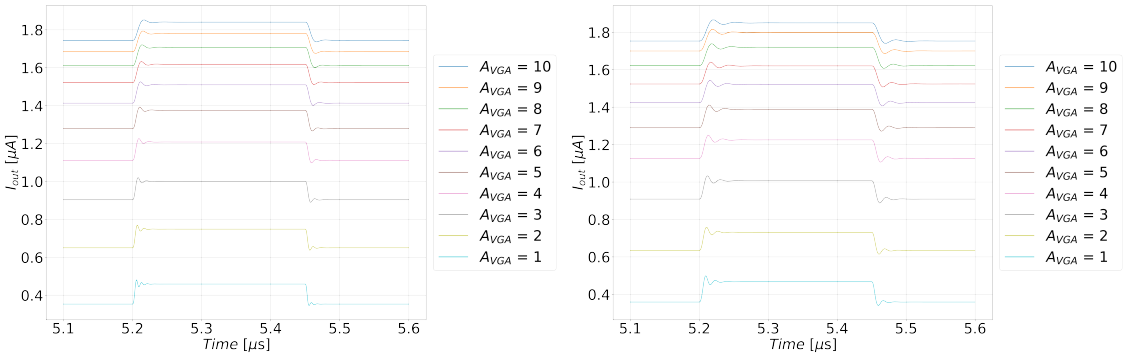
4.5 Settling Time

The settling time, t_{set}, of the oscillations in the step response, shown in Figure 4.6a, is summarized in Table 4.1 This reveals that the oscillations are more significant in post-layout simulations. The VGA is sensitive to capacitance in node b and c. The excess parasitic capacitance from the layout can cause the observed increase in t_{set}.

Table 4.1: Settling time of VGA (error ±5%), format: $t_{set}[ns]$ (A_{VGA} [linear])

	tt	ff	ss	fs	sf
$t_{set_{min}}$ (Pre-Layout)	12.91 (2)	13.91 (1)	10.57 (9)	22.49 (2)	10.2 (4)
$t_{set_{max}}$ (Pre-Layout)	21.0 (6)	31.2 (10)	32.49 (1)	29.76 (10)	22.38 (10)
$t_{set_{min}}$ (Post-Layout)	23.45 (1)	24.83 (1)	26.57 (2)	50.75 (10)	24.9 (1)
$t_{set_{max}}$ (Post-Layout)	38.7 (5)	39.16 (5)	39.78 (6)	75.57 (1)	43.9 (6)

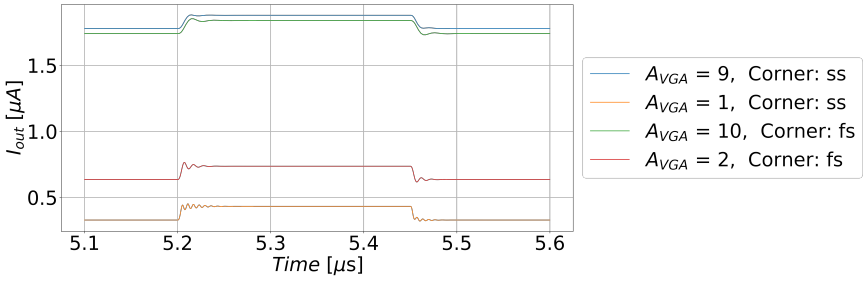
The post-layout simulations consistently result in longer t_{set} because of the parasitic capacitance discussed above. Figure 4.7 highlight the step response in ss and fs corners to illustrate the corner with the highest variability across A_{VGA} and longest t_{set} respectively. Adjusting the timing of the different feedback mechanisms in the



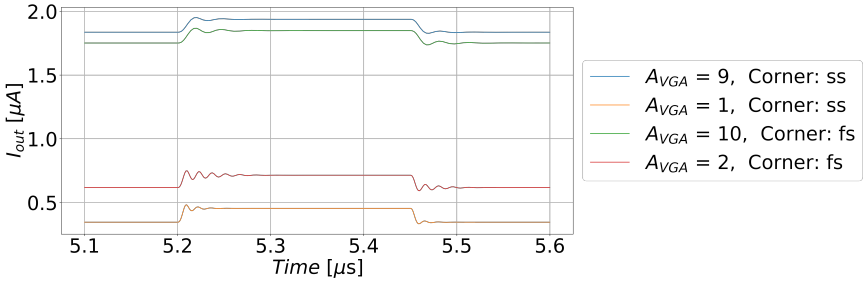
(a) Pre-Layout Simulation (b) Post-Layout Simulation

Figure 4.6: Step Response of VGA

circuit is critical to reducing the oscillating behaviors. Figure 4.8 highlights the timing of the feedback voltages, V_{in}, V_{fb} and V_{CM}, which shows that the increased oscillations at $A_{VGA} = 1$ arise when the speed V_{CM} increases relative to V_{in} and V_{fb} is increased, thereby reducing phase margin in that feedback loop.



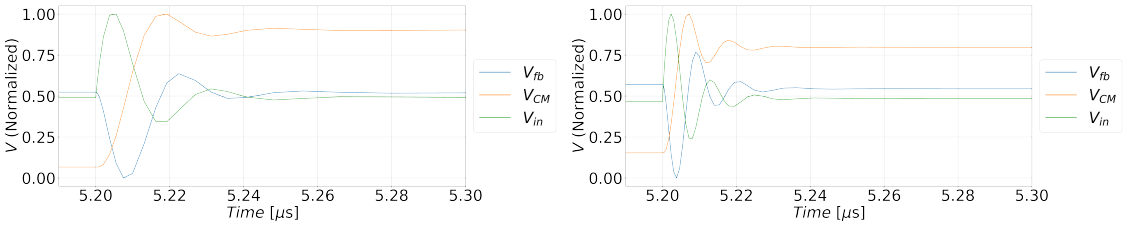
(a) Pre-Layout Simulation



(b) Post-Layout Simulation

Figure 4.7: Large deviation in t_{set} across A_{VGA} and corners

Looking at the simulated settling time in Table 4.1, it is clear the targeted settling time of $t_{set_{spec}} < 15ns$ is not always reached. This may be an issue for very fast pulse detection in ultrasound applications, but is less of an issue in for example continuous dopler measurements. The required settling time for different ultrasound applications must be taken into account when considering the viability of this VGA in the ultrasonic sensor.



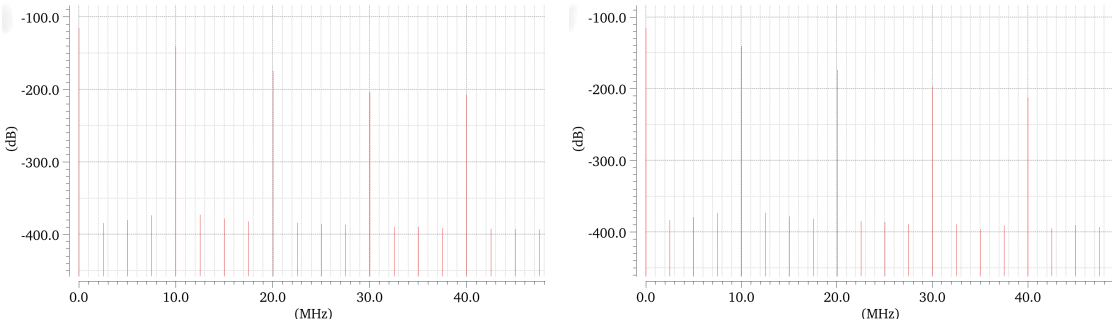
(a) $A_{VGA} = 10$ (b) $A_{VGA} = 1$

Figure 4.8: Relative timing of feedback loops

4.6 Linearity

Figure 4.10 shows the output current of the VGA when a 10MHz sine wave is applied to the input. The input signal is scaled with A_{VGA} so that the amplitude of i_{out} remains constant. All the results in this section are simulated with the amplitude of i_{in} ranging from $10nA$ to $100nA$. At higher amplitudes, the second harmonic component of i_{out} is increased beyond tolerable levels.

Looking at the spectrum of one of these sine waves (Figure 4.9), it is clear that the most significant undesired harmonic component is the second harmonic. The second harmonic distortion, $HD2$, is extracted in Table 4.2. The $HD2$ does not reach the target of $-40dB$, as specified in section 3.1. Several linearization techniques can be employed to improve this. As mentioned in section 2.4, adding cascode transistors and active bias circuits to M_{N2} and M_{N3} fixes $V_{ds_{N1}} = V_{ds_{N2}} = V_{ds_{N3}}$, which improves linearity. However, this necessitates the use of additional biasing amplifiers, which will increase the power consumption of the amplifier significantly. The $HD2$ reduction technique presented in [20] reports up to 9dB of $HD2$ reduction without a significant impact on either noise or power consumption. Considering this, $HD2$ of less than $-31dB$ in the VGA without the use of linearization techniques is considered to be able to satisfy the specified $HD2 < -40dB$. The linearization technique was not implemented due to the timing restrictions of the projects.

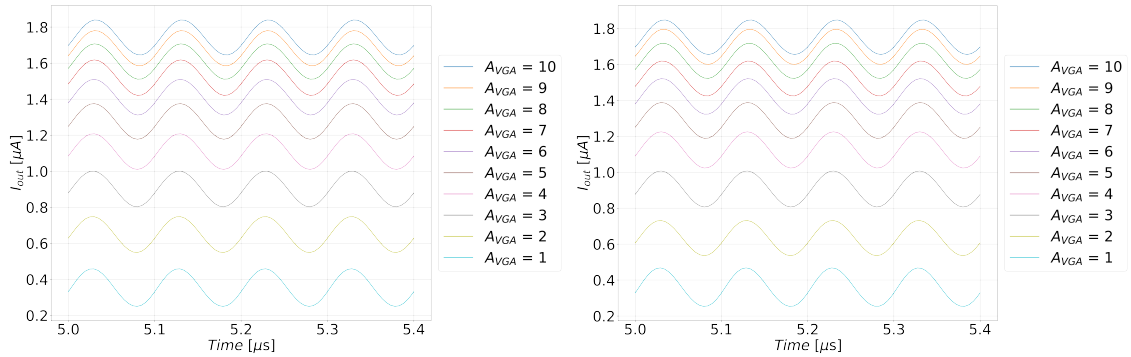


(a) Pre-Layout Simulation (b) Post-Layout Simulation

Figure 4.9: Spectrum of I_{out} sine wave at $A_{VGA} = 10$ and $i_{in} = 10nA$ in nominal corner

The $HD2$ was simulated using monte-carlo simulations as mismatch in the transistors can increase harmonic distortion. The impact of mismatch is not as significant in pseudo-differential amplifier topologies, as there is no differential

harmonic cancelation of even harmonic components.



(a) Pre-Layout Simulation

(b) Post-Layout Simulation

Figure 4.10: Transient simulation of a sine wave to illustrate linearity and constant amplitude

Table 4.2: HD2 supression of VGA

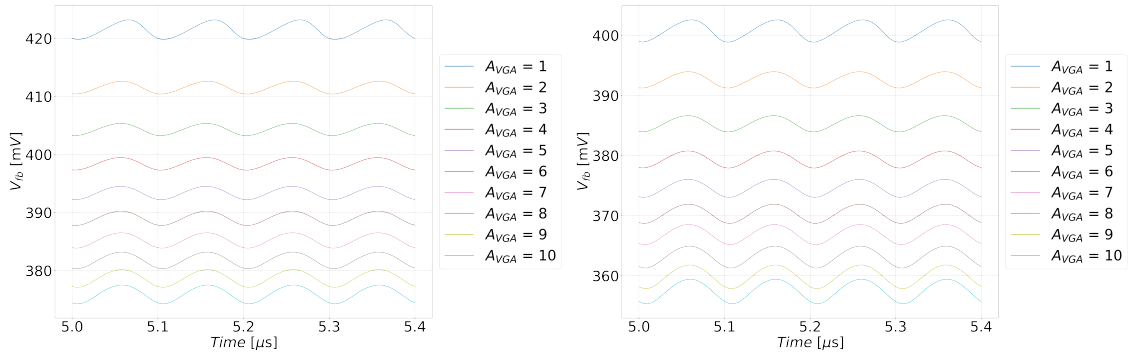
	min	nom	max	std	
$A_{VGA} = 10$ (Pre-Layout)	32.83	34.22	36.39	0.7185	dB
$A_{VGA} = 10$ (Post-Layout)	31.28	33.38	34.64	0.8125	dB
$A_{VGA} = 5$ (Pre-Layout)	34.30	35.44	37.07	0.6758	dB
$A_{VGA} = 5$ (Post-Layout)	32.95	34.49	35.67	0.7125	dB
$A_{VGA} = 1$ (Pre-Layout)	31.31	33.16	35.35	1.036	dB
$A_{VGA} = 1$ (Post-Layout)	28.95	30.81	32.36	0.8501	dB

Table 4.2 shows an redeuction of $HD2$ with decreasing A_{VGA}, until it falls off abruptly between $A_{VGA} = 2$ and $A_{VGA} = 1$. This looks to coincide with the sudden reduction in the linearity of the active bias amplifier, as seen in Table 4.3. Looking at the transient simulation in Figure 4.11, it is clear that as A_{VGA} is reduced, the amplifier goes into a nonlinear region due to the change in operating points in the input branch of the VGA.

Table 4.3: HD2 supression of Active Biasing Amplifier

	min	nom	max	std	
$A_{VGA} = 10$ (Pre-Layout)	23.16	24.40	26.70	0.7329	dB
$A_{VGA} = 10$ (Post-Layout)	21.80	23.70	24.77	0.7104	dB
$A_{VGA} = 5$ (Pre-Layout)	23.78	24.90	26.86	0.7460	dB
$A_{VGA} = 5$ (Post-Layout)	22.65	24.14	25.17	0.6276	dB
$A_{VGA} = 1$ (Pre-Layout)	14.62	16.85	18.08	0.9069	dB
$A_{VGA} = 1$ (Post-Layout)	17.04	18.03	18.88	0.6024	dB

Changing the operating points of the VGA also changes the frequency response of the bias amplifier as seen in Figure 4.12. Reducing A_{VGA} reduces A_{Bias} and increases the band width, while the phase is reduced. This reduces the phase margin of the A_1feedback loop, as seen in Table 4.4, which contributes to the increased oscillations at lower A_{VGA}, as seen in Figure 4.6. Due to incerased capacitance at node c,



(a) Pre-Layout Simulation

(b) Post-Layout Simulation

Figure 4.11: Sine response feedback

the phase margin of the active bias loop is increased, as stated above. This is a contributing factor for the increase in t_{set} seen in post-layout simulations.

Table 4.4: Phase margin for A_1 in active bias circuit

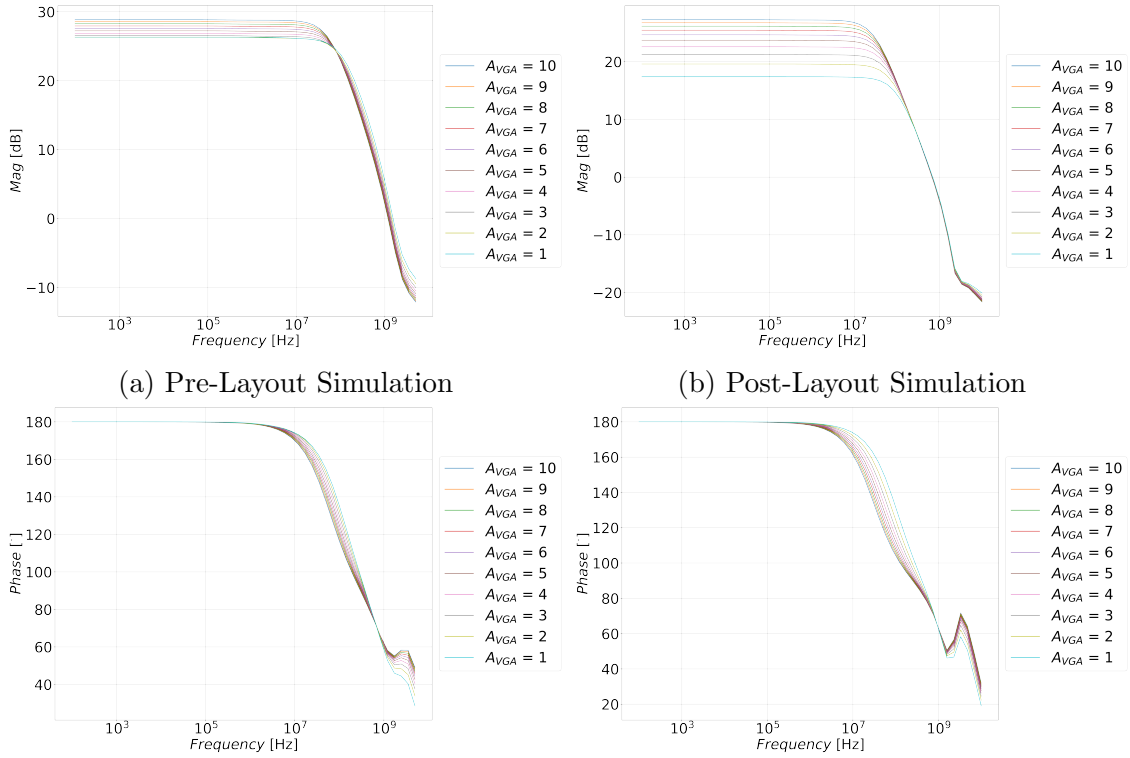
	tt	ff	ss	fs	sf
$A_{VGA} = 10$ (Pre-Layout)	59.04	65.9	53.64	62.23	54.52
$A_{VGA} = 10$ (Post-Layout)	56.21	63.91	49.81	60.4	48.08
$A_{VGA} = 5$ (Pre-Layout)	48.62	59.88	39.88	55.35	35.91
$A_{VGA} = 5$ (Post-Layout)	74.39	77.33	71.14	74.36	75.9
$A_{VGA} = 1$ (Pre-Layout)	74.63	78.21	70.48	74.01	77.67
$A_{VGA} = 1$ (Post-Layout)	76.42	82.29	69.44	73.88	79.41

A_{Bias} observed in simulation also deviates significantly from what is calculated in section 3.2. Also stated in section 3.2, this difference was known when finalizing the design and the simulation results were the main driver for iterations of the design of A_1. This benefited the design as effects of A_1 on design parameters such as $HD2$ and NF_{min} could be designed for, rather than the performance of A_1 as an isolated circuit. This deviation from the analytical model is likely from interactions with the FVF buffer or unforeseen interactions in the feedback loop.

4.7 Noise

NF_{min} of the VGA across corners is presented in Table 4.5. The maximum deviation from the specified noise figure of $NF_{min} < 3dB$ from Table 3.1 is $0.064dB$ in pre-layout simulations and $0.125dB$ in post-layout simulations. The small difference in pre- and post-layout simulations indicates that the layout does not contribute significant noise to the circuit. However, as only parasitic capacitance is extracted, the actual noise figure might be negatively affected by the extraction of parasitic resistances in the traces.

The most significant noise contributions from each circuit component are shown in Table 4.6. Improving NF_{min} requires reducing the thermal noise of M_{N1} and M_{B2} while not reducing the total noise power of the CMUTs. However, reducing the



(a) Pre-Layout Simulation

(b) Post-Layout Simulation

(c) Pre-Layout Simulation

(d) Post-Layout Simulation

Figure 4.12: Frequency Response of Active Biasing Amplifier

Table 4.5: Simulated Noise Figure of VGA

	tt	ff	ss	fs	sf	
NF(f) (Pre-Layout)	2.969	3.025	2.941	2.888	3.064	dB
NF(f) (Post-Layout)	2.967	2.957	2.987	2.922	3.125	dB

thermal noise of these components necessitates reducing the g_m of the transistors. This both impacts R_{in} and may reduce the available gain range of the VGA.

Table 4.6: Summary of noise contributions in total output noise.

	Output Reffered Noise $@f = 9.5MHz$ $[V^2/Hz]$	Prosentage of total ORN [%]
M_{N1} (Thermal)	3.45e-19	21.14
M_{B2} (Thermal)	1.79e-19	10.95
$CMUT < 1-9 >$	9.14e-20	5.60 (50.4 total)
P0	3.84e-20	2.36
M_{B1} (Thermal)	3.81e-20	2.34
M_{A1} (Thermal)	2.95e-20	1.81
M_{BP2} (Thermal)	2.58e-20	1.58
M_{A2} (Thermal)	2.03e-20	1.25
M_{N2} (Thermal)	1.98e-20	1.22
M_{N3} (Thermal)	1.95e-20	1.19

4.8 Power Consumption

The power consumption of the VGA, P_{VGA}, neglecting the FVF buffer, is presented in Table 4.7. Differences between pre- and post-layout simulations are small and can be neglected. P_{VGA} ranges between $27.14\mu W$ and $24.99\mu W$. This is due to the dynamic bias current of the VGA. As this range is so small, the average of $P_{VGA} \approx 26\mu W$ is considered as the static power consumption of the VGA, for practical purposes. Table 4.8 shows the power consumption of the biasing amplifier. The power consumption stays approximately constant at $P_{BA} = 24\mu W$. Any efforts to reduce the overall power consumption of the VGA should be focused on reducing the power consumption of the bias amplifier as this accounts for more than 90% of the total power consumption.

Table 4.7: Power consumption of VGA, P_{VGA}

	tt	ff	ss	fs	sf	
$A_{VGA} = 10$ (Pre-Layout)	26.75	26.34	27.14	26.5	27	μW
$A_{VGA} = 10$ (Post-Layout)	26.9	26.69	27.11	26.87	26.93	μW
$A_{VGA} = 5$ (Pre-Layout)	26.24	25.9	26.55	25.98	26.5	μW
$A_{VGA} = 5$ (Post-Layout)	26.4	26.26	26.52	26.35	26.44	μW
$A_{VGA} = 1$ (Pre-Layout)	25.2	24.99	25.37	24.91	25.48	μW
$A_{VGA} = 1$ (Post-Layout)	25.36	25.39	25.31	25.28	25.43	μW

Table 4.8: Power consumption of Active Bias Amplifier, , P_{BA}

	tt	ff	ss	fs	sf	
$A_{VGA} = 10$ (Post-Layout)	24.13	24.08	24.18	24.1	24.15	μW
$A_{VGA} = 5$ (Post-Layout)	24.15	24.1	24.2	24.13	24.17	μW
$A_{VGA} = 1$ (Post-Layout)	24.17	24.13	24.22	24.16	24.18	μW

The power consumption of the FVF buffer, P_{FVF} is presented in Table 4.9. P_{FVF} was neglected from the overall power consumption of the VGA as the buffer can be used to power several bias amplifiers. However, minimizing P_{FVF} will impact the total power consumption of the set of amplifiers it powers. In the active biasing circuit, the $\frac{W}{L}$ of M_{A1} and M_{BP2} are equal so that $V_{in} = V_{set}$. Using multipliers, M_{BP2} and I_{Buffer} can be scaled down by a factor m, while keeping the cascode amplifier unchanged to reduce P_{FVF}. However, this reduces $g_{m_{BP2}}$ which may limit the number of amplifiers it realistically can supply before the stability of the buffer is compromised.

Table 4.9: Power consumption of FVF Buffer, P_{FVF}

	tt	ff	ss	fs	sf	
$A_{VGA} = 10$ (Post-Layout)	15.94	15.95	15.83	15.86	15.99	μW
$A_{VGA} = 5$ (Post-Layout)	15.94	15.95	15.83	15.86	15.98	μW
$A_{VGA} = 1$ (Post-Layout)	15.94	15.95	15.83	15.86	15.98	μW

4.9 Comparison to Existing Works

Table 4.10: Performance Comparison

	This Work	[5]	[7]	[23]
Technology	22nm FDSOI	68nm CMOS	65nm CMOS	65nm CMOS
$BW[MHz]$	20	11.32	10	40
$f_0[MHz]$	10	5	5	N/A
Gain Range $[dB]$	0 $\tilde{}$ 20	7.4 $\tilde{}$ 13	0 $\tilde{}$ 20	-18 $\tilde{}$ 47
Gain Step	Continuous	2 bit	N/A (Digital)	Continuous
$NF[dB]$	2.967	2.98	3	N/A ($11nV/\sqrt{Hz}$)
$HD2[dB]$	-28.95	-56.63	N/A	-42
$Power[\mu W]$	26	68	100	2230
$Area[\mu m]$	117.8	375	8000	170000

The strengths and weaknesses of this VGA topology are highlighted when compared to existing VGA designs in Table 4.10.

Compared to the feedback-based topologies of [5] and [7], this VGA topology offers significantly higher bandwidth at comparable levels of power consumption, as stability issues surrounding the negative feedback loop tend to increase the power consumption requirements compared to open-loop topologies, like the VGA presented in this thesis [9]. [23] shows that using a resistive feedback structure in a high-bandwidth application is possible, however, the power consumption of this VGA is at least an order of magnitude higher than the others.

Continous gain control schemes can improve the gain accuracy which results in higher resolution conversions in the ADC. Digital gain control schemes require additional digital circuitry to adjust the gain, which increases both complexity, area and power consumption. The ramp generator and digital circuitry of [23] is shown to increase the overall area substantially.

The noise figure of the amplifiers is comparable across all the highlighted amplifiers. This is understandable as lowering the noise figure below 3dB has little impact on the noise performance of the system. Achieving a noise figure of $2.967dB$ with a design based on current mirrors is not widely reported in previous literature and is one of the major advances with this VGA design.

The point where this VGA suffers compared to the other topologies is in linearity. Feedback topologies tend to have good linearity, while open-loop topologies struggle [9]. However, with additional linearization techniques implemented, the $HD2$ of this VGA topology could be comparable to the other designs discussed here.

The low power consumption of this VGA is a significant improvement over the other topologies that are presented. Contrary to voltage-input amplifier topologies, low branch currents in this current mirror-based topology improve the noise figure, which incentivizes low power consumption. The only significant power consumption of the VGA originates in the bias amplifier, A_1, but as gain and linearity requirements of this amplifier is much less than the transimpedance amplifiers utilized in feedback-based VGAs, the power consumption can be lower.

Major benefits in the compactness of the VGA are also observed when comparing the area of the topologies, as the need for large switchable feedback networks is eliminated. Combined with the need for low-g_m transistors, the physical layout of the circuit can be made very compact.

The gain range of the amplifiers is not as interesting to compare as these are typically strict design specifications.

5 Future Work

The folded cascode amplifier, A_1 is the component with the largest room for improvement. A full redesign based on strategic design methodologies like the g_m/I_d-method can be very beneficial, as early issues in the design process shifted the design strategy of A_1 from one based on analytical methods, to an iterative trial and error based method. Proper design methods may for instance enable the reduction of power consumption in A_1, which is by far the most significant contribution to the total power consumption of the VGA.

Improving A_1 to increasing A_{Bias} will further decrease R_{in}, so more current can be transferred from the CMUT. This reduces the noise figure, increasing the overhead so that higher linearity or a larger range of A_{VGA} can be achieved.

Increasing the output voltage swing of A_1, and therefore also the linearity of the bias voltage driving M_{C1}, may reduce $HD2$ in the VGA at $A_{VGA} = 1$ so that fewer linearization techniques must be employed.

Linearization techniques, like the one in [20], must be implemented for this VGA to be a viable choice in the analog front-end of ultrasonic probes. Before implementing this HD2 reduction circuit, however, the transistors contributing the most harmonic distortion must be identified. Because of the timing restrictions of the project, this was not investigated.

Another option for reducing $HD2$ is to amplify the current from the CMUTs through a PMOS implementation of the VGA in parallel with the NMOS implementation presented in this thesis but without the pseudo-differential output stage. This could provide a fully differential output signal with the associated $HD2$ cancelation. Because of the low power consumption and small area of the VGA, this could be a viable option and still be competitive with existing designs.

Investigating if a low bandwidth feedback loop can be utilized to generate the dynamic bias current of the VGA is interesting as this would minimize the variation in operating points for A_1. Such a feedback loop would interfere with the main feedback mechanisms of the FVF current mirror and could destabilize the circuit if not designed correctly.

Changing V_{cas} in post-layout simulations was considered an adequate solution given the time restrictions. However, without the timing restrictions for the project, a better solution requires rethinking the layout of A_1, and reducing the parasitic capacitance of node (c) in the VGA.

Before a potential tape-out, the intermodulation distortion of the VGA must be examined. Low power amplifiers tend to struggle with intermodulation effects and may make the circuit less viable. This was not a part of the project specifications due to timing restrictions and was therefore not considered during the design process.

The temporary biasing circuit used in this thesis (see Appendix B Figure B.4) was not designed for either power efficiency or low noise performance. Large improvements can be made to this circuit and will be reflected in the performance

metrics of the VGA. The current bias network adds an additional power consumption of $P_{bias} = 16\mu W$ to the VGA, but it is not included in the total power consumption of the circuit (in Table 4.7) as little design effort was made to optimize it.

6 Conclusion

In this thesis, a current-based single-ended to differential VGA with a bandwidth of $20MHz$ is proposed for time-gain compensation in the analog front-end of ultrasonic sensors. This VGA is designed for CMUT-based probes and utilizes nine CMUTs in parallel to achieve a noise factor $NF_{min} = 2.967dB$. It utilizes dynamic back biasing which enabled continuous gain control through an analog control voltage V_{Gain} ranging from $0V$ - $1.8V$. The VGA has a gain range of $0dB$ - $20dB$. The design is compact, with an area of just $117.7\mu m$, and power efficient, with a power consumption of only $26\mu W$. Linearity is found to be an issue as the HD2 component reaches $-28.95dB$ at certain gain settings. With additional linearization techniques, however, this issue can be mitigated.

This VGA topology is competitive with existing designs on all discussed performance metrics except linearity.

The performance of the active biasing amplifier, A_1, is not optimal and improvements in its design can improve the linearity, power consumption and noise factor of the VGA as a whole.

More work is needed to characterize the intermodulation performance of the VGA before it can be considered a fully viable option in an ultrasonic imaging probe. This was omitted from the scope of the thesis due to timing restrictions.

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A Layout

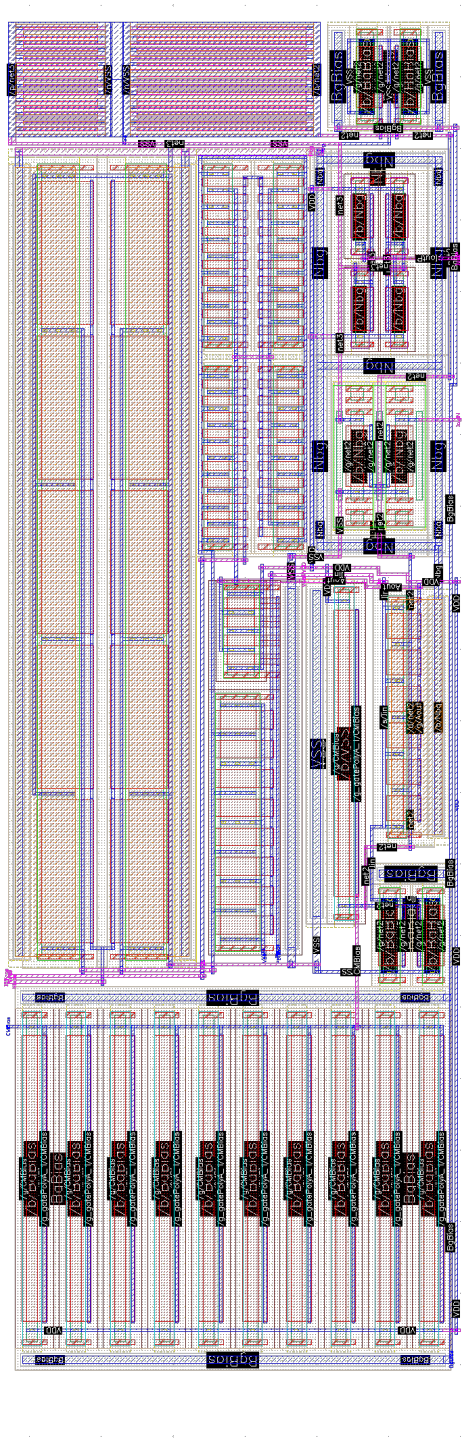


Figure A.1: Layout of VGA

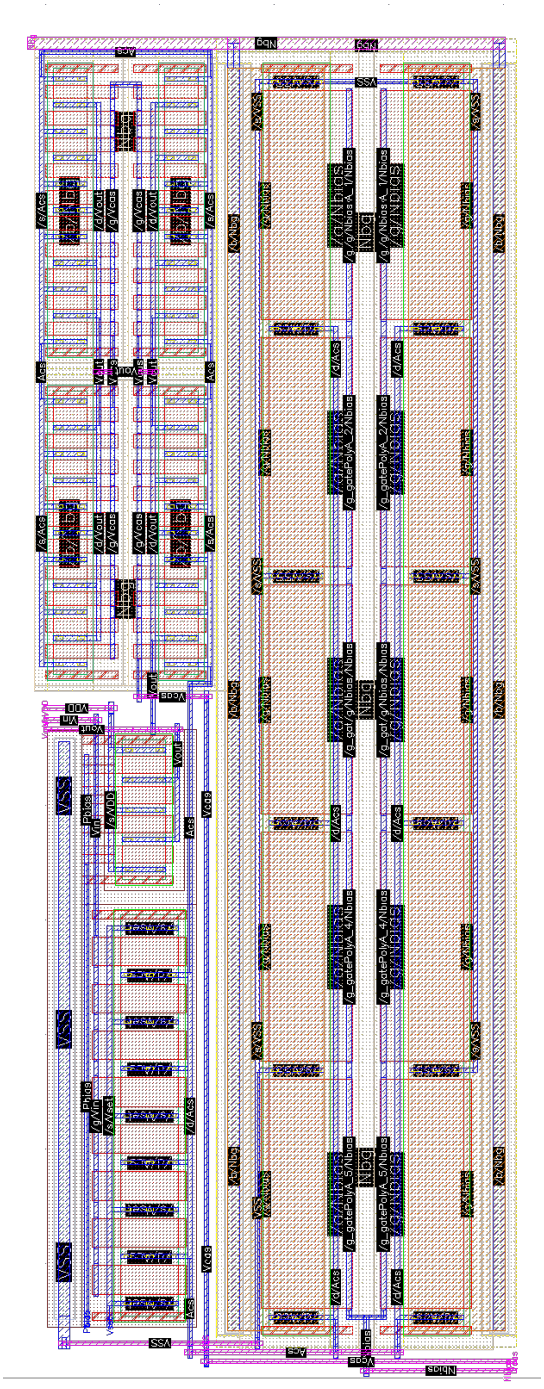


Figure A.2: Layout of Cascode Amplifier

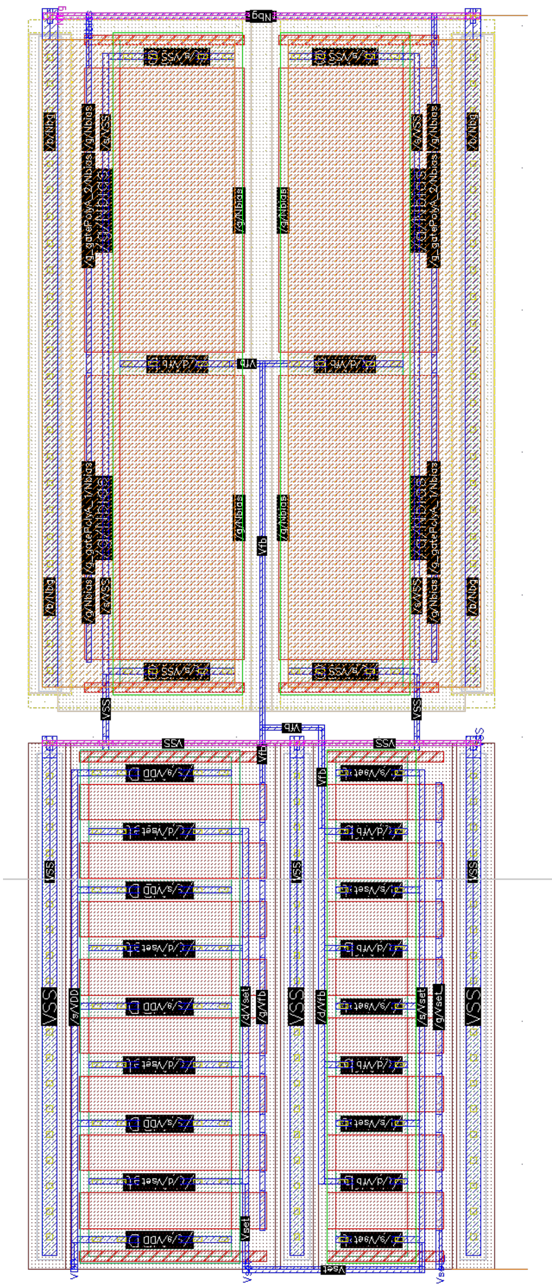


Figure A.3: Layout of FVF Buffer

B Schematic from Virtuoso

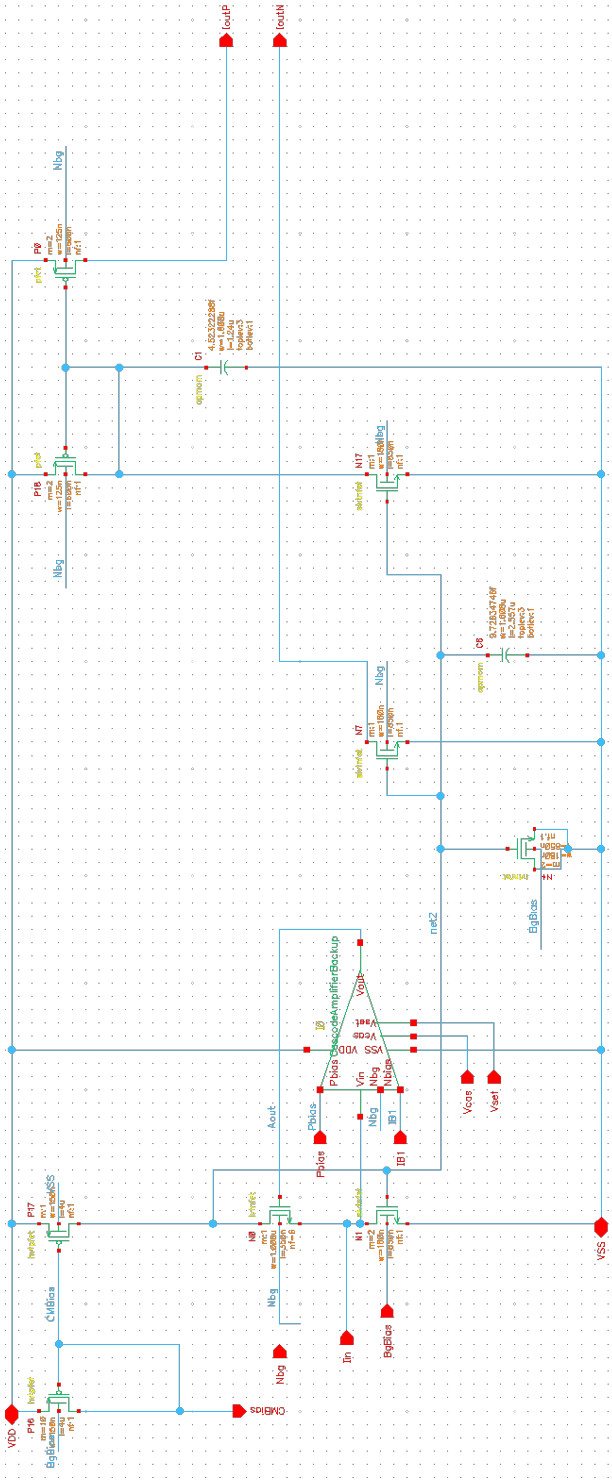


Figure B.1: Schematic of VGA

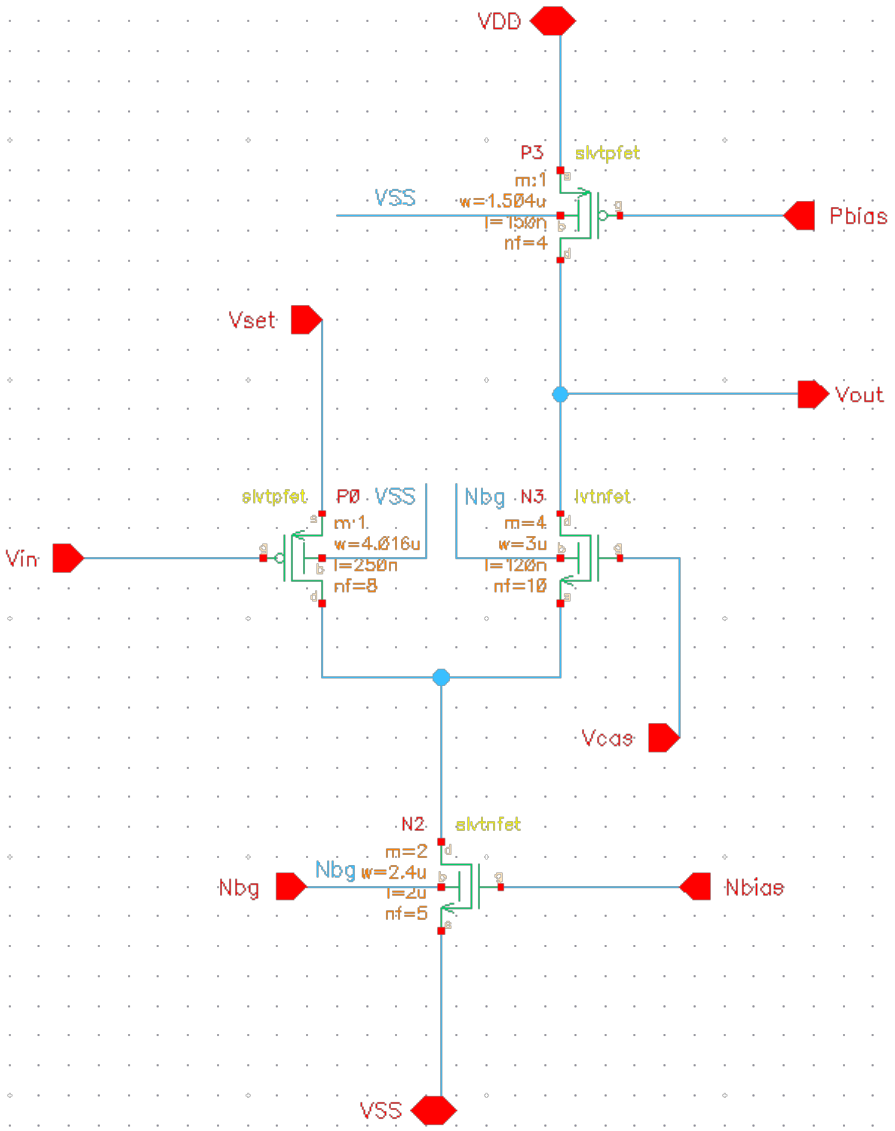


Figure B.2: Schematic of Cascode Amplifier

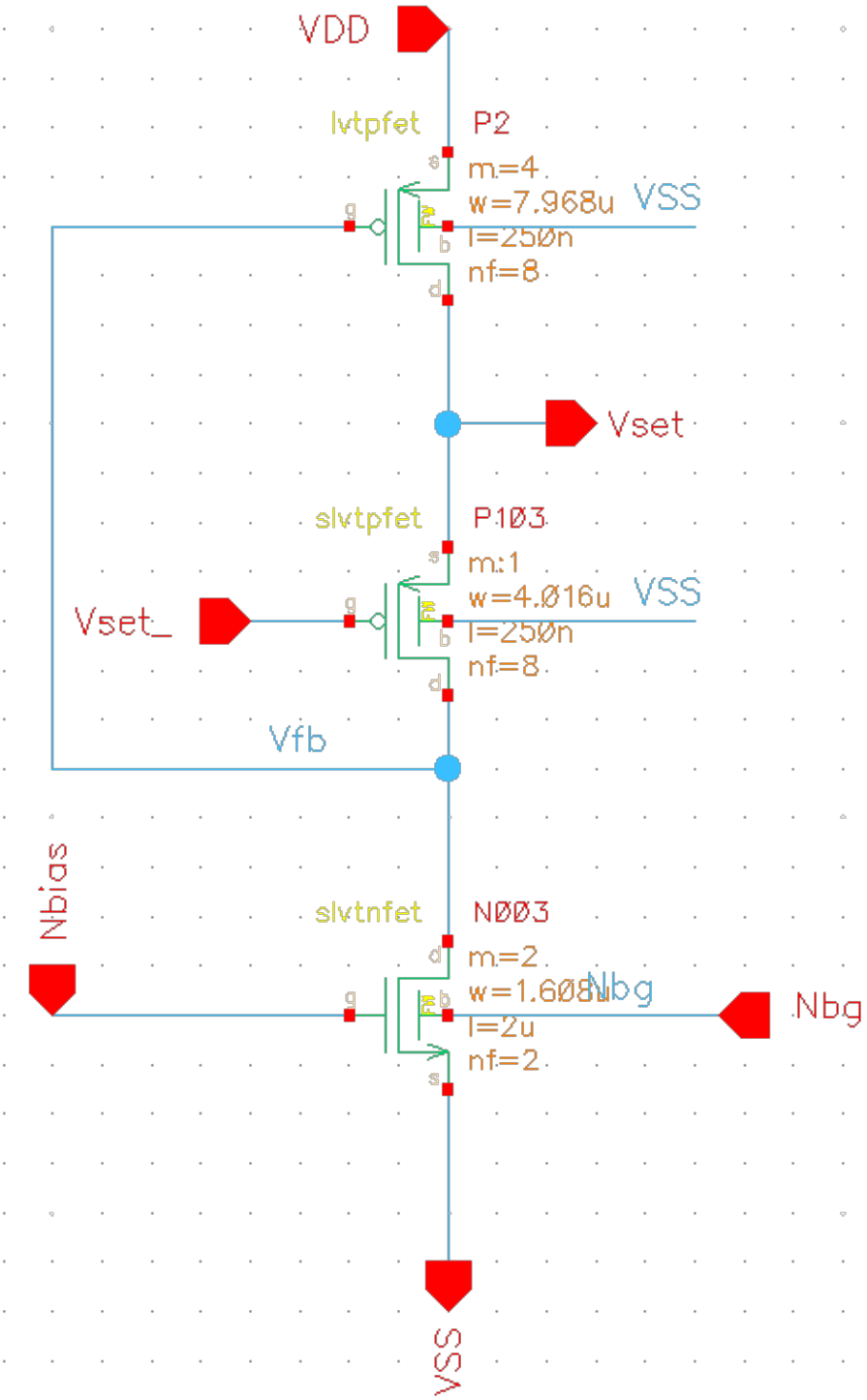


Figure B.3: Schematic of FVF Buffer

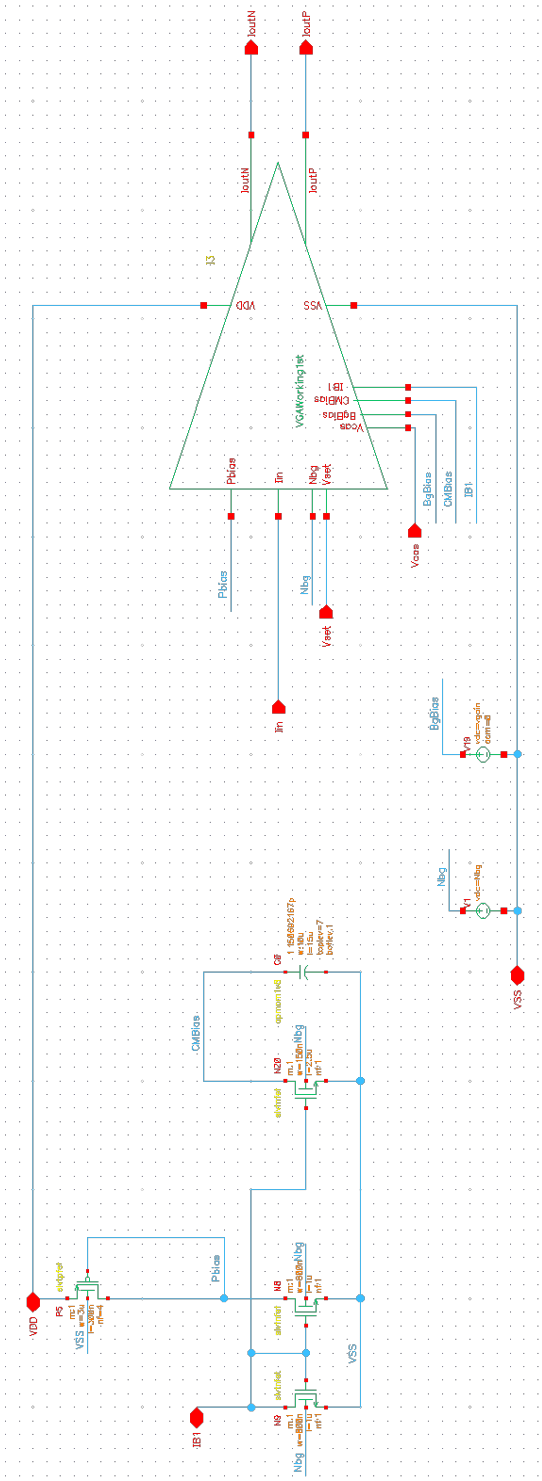


Figure B.4: Simple current mirror bias circuit for testing purposes

C Testbench Setup

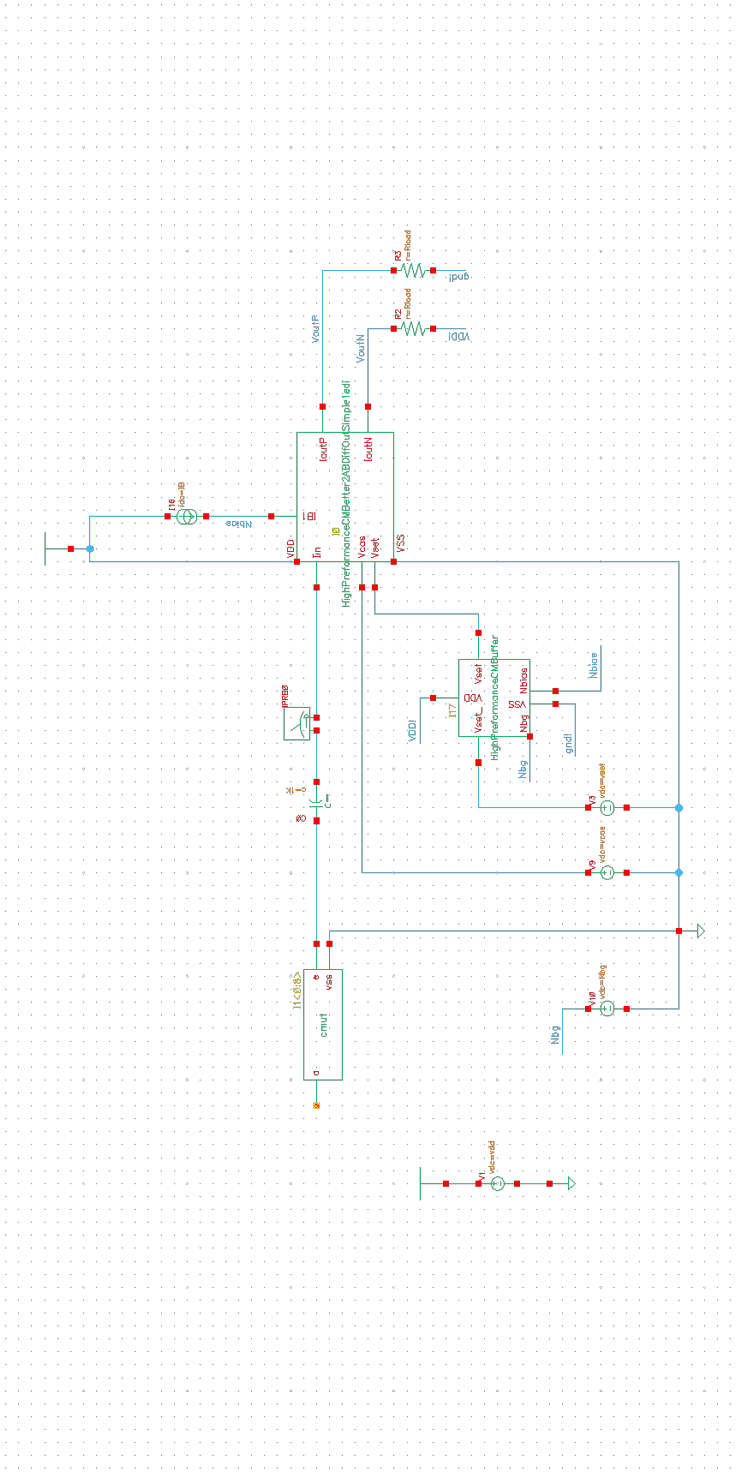


Figure C.1: Testbench for simulating Noise Factor

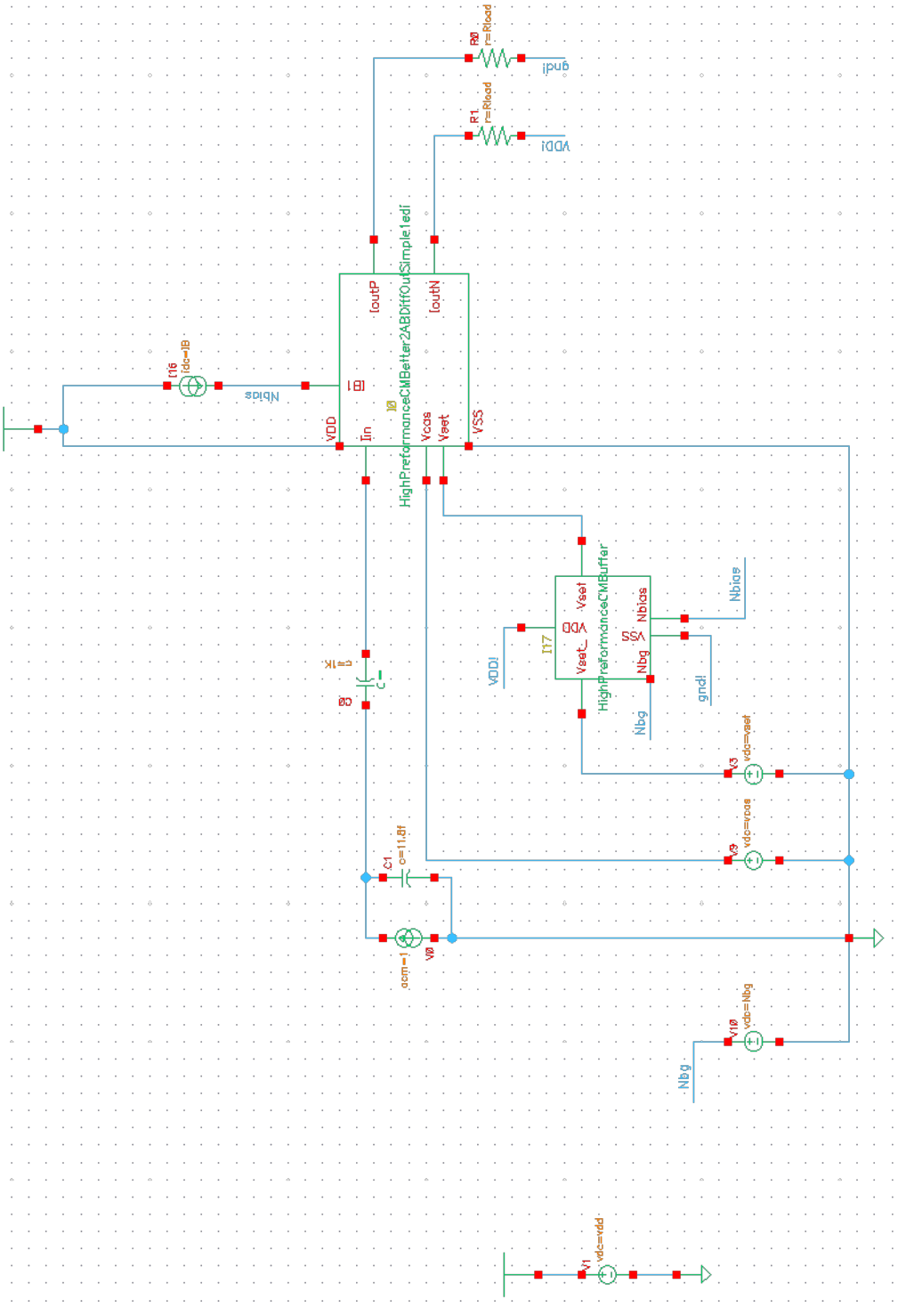


Figure C.2: Testbech for small signal analysis

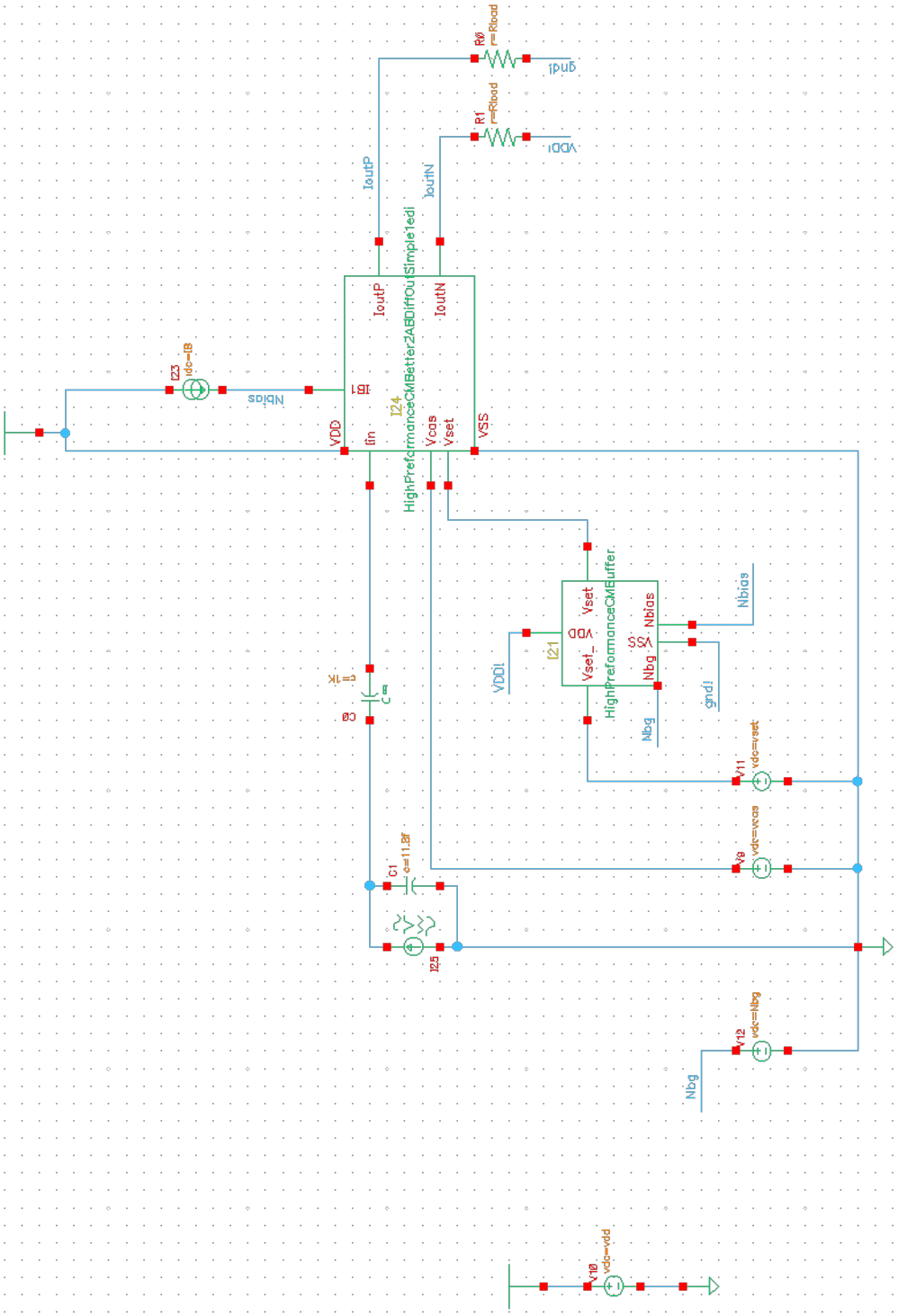
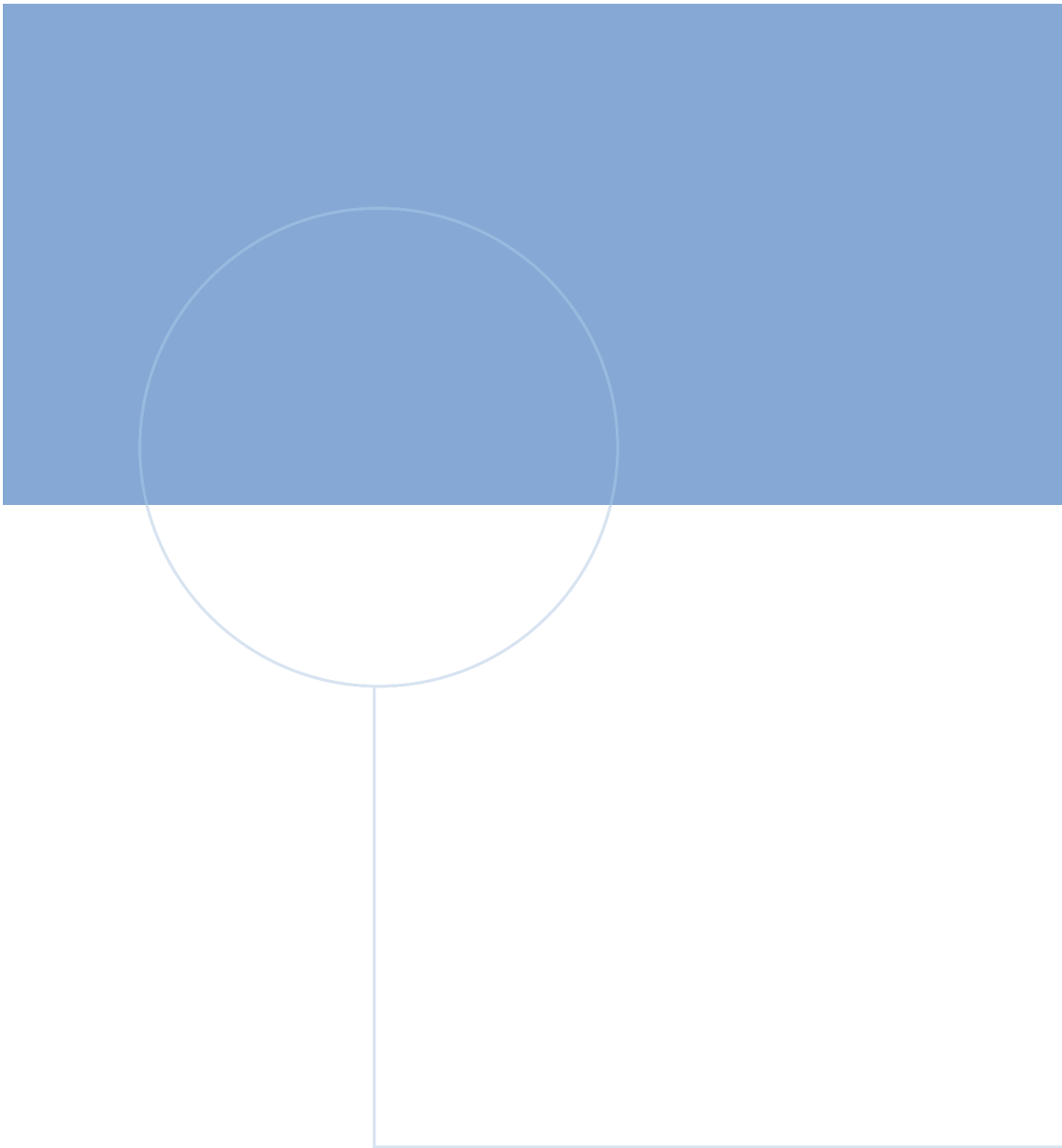


Figure C.3: Testbech for transient analysis



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