Master's thesis

NTNU
Norwegian University of Science and Technology
Faculty of Information Technology and Electrical Engineering
Department of Electric Power Engineering

Halvor Bratvold Ekren

# Investigation of a Four Level Voltage Active Gate Driver for Loss and Slope Control of SiC MOSFETs

Master's thesis in Energy and Environmental Engineering
Supervisor: Dimosthenis Peftitsis
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# Preface

This Master Thesis is the culmination of the two year Energy and Environmental Engineering study program (*MIENERG*) at NTNU (*Norges teknisk-naturvitenskapelige universitet*) Trondheim. This Thesis is part of the Adaptive Silicon Carbide Electrical Energy Conversion Technologies for Medium Voltage Direct Current Grids (ASiCC) research project. Furthermore, this Master Thesis is 100 % of the evaluation in the Electrical Energy, Master Thesis course (*TET4905*). This course is 30 ECTS credits.

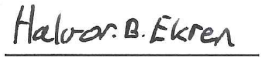
This year, both the Specialization Project and the Master Project have been a rewarding experience. Going from a literature study used to decide upon an active gate driver concept to performing simulations and experiments to verify the efficacy of this gate driver concept has been challenging and rewarding. I have increased my competence in LTSpice and Python. I have also gained experience with prototype development in a laboratory setting. In connection to my Master Thesis, I was able to be part of writing a paper. This paper was accepted at the 2022 IEEE 13th international symposium on power electronics for distributed generation systems (PEDG 2022) in Kiel, Germany. The paper will be presented in June of 2022. This Master Thesis is the continuation of the Specialization Project, submitted on 21.12.2021. Chapter 2, the list of terms and the list of abbreviations in this Master Thesis is based on work done in the Specialization Project [1]. However, these parts of the Thesis have been rewritten to improve clarity and conciseness and ensure they are relevant to the Master Thesis. The same is true for the list of terms and the list of abbreviations.

I want to thank my supervisor, Professor Dimosthenis Peftitsis. He has always been available to provide guidance and support when I needed it. His encouragement and assistance were crucial for the submission and overall quality of the PEDG paper.

I would also like to offer a great thanks to my co-supervisors, Ph.D. Candidates Daniel Alexander Philipps and Gard Lyng Rødal. Daniel has spent numerous hours helping and guiding me with all the aspects of my Master Thesis and the paper. Without Daniel, the scope and quality of this Thesis would not have been the same. Working with him in the power electronics laboratory has been a rewarding and educational experience for me. Gard provided me with guidance and encouragement and answered any questions I had. His contribution was crucial when the active gate driver concept was decided upon in the Specialization Project. Finally, I would also like to thank my girlfriend. Her support has been crucial during the writing period of the Master Thesis.

The overall process regarding the Master Thesis has been both rewarding and challenging. Being able to work a lot in the lab and perform experiments is something I will treasure. I am glad I choose this Master Thesis.

Trondheim, 14.06.2021



Halvor Bratvold Ekren

# Abstract

In this Master Thesis, a four level voltage active gate driver is introduced and tested with both simulations and experiments. The switching performance can be controlled by introducing an intermediate voltage level at turn-on and turn-off, controllable in both voltage amplitude and duration. A thorough simulation study was performed using a double pulse test circuit created in LTSpice, and evaluation functions, created in Python. The simulation study used three different models for the C3M0075120D Silicon Carbide (SiC) power Metal–Oxide–Semiconductor Field-Effect Transistor (MOSFET) from Wolfspeed. Based on the simulation study, the efficacy of the active gate driver concept was proved.

An exemplary selection of intermediate voltage level duration and a single voltage amplitude value was tested for the experiments. Experimental Double Pulse Tests (DPTs) were performed, examining the turn-on switching transient. In order to facilitate these experiments, a printed circuit board prototype of Active Gate Driver (AGD) was created. In addition, a DPT setup and gate driver control software were provided to perform the experimental DPTs. For the experiments, the C3M0075120K SiC power MOSFET from Wolfspeed was used. The measurement data from the experiments were processed and evaluated using Python functions created for these tasks. Based on the experimental results, the AGD prototype can influence the turn-on switching transient of the Device Under Test (DUT).

# Sammendrag

I denne masteroppgaven blir en styrekrets for silikon karbid metall-oksid-halvleder felteffekttransistorer (SiC MOSFET) introdusert. Denne styrekretsen introduserer midlertidige spenningsnivå som kan styres både i lengde og i spenningsamplitude.

Evnen til denne styrekretsen til å påvirke svitsjingen til en SiC MOSFET blir undersøkt via simulerte og eksperimentelle dobbel puls tester. I simuleringene blir tre forskjellige varianter av en model for C3M0075120D SiC MOSFETen fra Wolfspeed undersøkt.

For å gjennomføre simuleringene ble en dobbel puls test implementert i LTSpice og evalueringsfunksjonalitet ble implementert via Python. I eksperimentene blir C3M0075120K SiC MOSFETen fra Wolfspeed brukt. En prototype av stryekretskonseptet ble utviklet for å gjennomføre eksperimentene.

Basert på simuleringene og eksperimentene så er evnen til stryekretskonseptet til å påvirke svitsjingen til en SiC MOSFET bekreftet.

# Contents

# List of Terms

| Name | Description |
|---|---|
| Active region: | Operation region of MOSFETs where drain current is highly independent of the drain-source voltage. In this region, the drain current depends on the gate-source voltage. |
| Active temperature control | Control of junction temperature in power electronic devices by actively controlling the performance of the device. |
| Bandgap energy: | Minimum energy required to cause an electron to move up to the conduction band. |
| Conventional gate driver: | Gate driver concept turning on and off a MOSFET by using two voltage levels. |
| CTE: | Coefficients of thermal expansion (CTE) is a material property denoting how much the material expands when exposed to heat. |
| CPLD | Programmable logic device that can be used for many different applications. |
| Current source gate driver: | Gate driver concept turning on and off a MOSFET using a current source. |
| Cutoff region: | Region in the operation of a MOSFET where the conduction of current is almost zero. |
| Depletion type: | Type of MOSFET where a sufficient negative voltage must be applied between the gate and the source to stop conduction of current in the MOSFET. |
| Electromigration: | Transportation of matter caused by ions gradually moving through a conductor. |
| Enhancement type: | MOSFET type where a large enough positive voltage must be applied between the gate and source of the MOSFET to enable conduction. |
| Freewheeling diode: | Diode used to protect a circuit from damage from a sudden drop in current flowing in the circuit. |
| Integrated circuit: | Usually a big amount of MOSFETs integrated into a small chip. |
| Junction temperature: | Highest temperature of the semiconductor used in the device. |
| Low drop out regulator: | Device that can keep a constant output even though the input varies. |
| N-channel: | Type of MOSFET where the substrate is p-doped and the source and drain is n-doped. In these MOSFETs electrons are the charge carriers. |
| N-type doping: | Impurity introduced to a material to alter the electrical properties. N-type has free electrons. |

| Name | Description |
|---|---|
| Ohmic region: | Region in the operation of the MOSFET where the MOSFET acts as a resistor. |
| P-channel: | Type of MOSFET where the substrate is n-doped and source and drain is p-doped. In these MOSFETs electron holes are the charge carriers. |
| P-type doping: | Impurity introduced to a material to alter the electrical properties. P-type has free electron holes. |
| RUL: | Time before a device needs to be replaced or repaired. |
| SOA: | Plot found in MOSFET datasheets that show how the MOSFET can be operated at different voltage and current values. Can be used to identify operation points where the MOSFET can be safely operated. |

# Abbreviations

| Abbreviations | Full name |
|---|---|
| AGD | Active gate driver |
| ATC | Active temperature control |
| BJT | Bipolar junction transistor |
| C | Carbon |
| CGD | Convectional gate driver |
| CPLD | Complex programmable logic device |
| CSG | Current source gate driver |
| DBC | Direct Bonded Copper |
| DC | Direct current |
| DPT | Double pulse test |
| DSP | Digital signal processor |
| DUT | Device under test |
| ESR | Equivalent series resistance |
| ESL | Equivalent series inductance |
| FPGA | Field-programmable gate array |
| IC | Integrated circuit |
| IGBT | Insulated-gate bipolar transistor |
| LDO | Low drop out regulator |
| MOSFET | Metal-oxide-semiconductor field-effect-transistor |
| PWM | Pulse width modulation |
| RUL | Remaining useful life |
| SC | Short circuit |
| Si | Silicon |
| SiC | Silicon carbide |
| $SiO_2$ | Silicon dioxide |
| SMD | Surface mounted device |
| SOA | Safe operating area |
| SPI | Serial peripheral interface |
| SPICE | Simulation program with integrated circuit emphasis |
| TO | Transistor outline |
| UN | United nations |
| $V_f$ | Forward voltage |

# List of Figures

# List of Tables

# 1 Introduction

In 2015, the United Nations (UN) published their 17 sustainable development goals [2]. These goals are meant to steer the development of the world towards 2030. Goal seven is of significance when it comes to energy and electrification: "*Ensure access to affordable, reliable, sustainable and modern energy for all*" [2]. A significant part of reaching this goal involves increased utilization of renewable energy sources, such as solar and wind energy. For the utilization of these renewable energy sources, power electronics play a key part. The electrification occurring in several segments of society, such as the consumer, industry, or transportation segment, also suggests an increased presence of power electronics in the future [3]. Power electronics can be defined as the use of power semiconductor devices and circuits to convert and regulate electrical power [4]. Power semiconductor devices, such as the MOSFET, can serve as switches in an electric circuit. Switching devices are used to create converters that can alter the form of voltage and current waveforms [5]. Power semiconductor devices, such as the MOSFET, consist of several layers of semiconductor material. These layers have different material properties. One of these properties is how the material responds to change in heat [5]. Increased temperature causes the materials to expand. However, they do so at different rates. This can be an issue in renewable energy sources, where the power production is intermittent. A power semiconductor device exposed to a varying load current has a resulting temperature change. This leads to temperature induced stress on the device, which can, over time, contribute to the aging of the device, causing reduced lifetime and reliability. At worst, this stress can lead to device failure [6]. Reducing temperature induced stress would therefore be beneficial. One way to achieve this can be by utilizing the gate driver circuit to affect the performance of the power semiconductor device. The gate driver circuit provides or removes the charge needed to turn a power semiconductor device on or off [7].

The first step to accomplishing this is a gate driver concept capable of influencing the performance of the power semiconductor device. This Master Thesis introduces a gate driver concept capable of altering the switching performance of a discrete SiC MOSFET. The gate driver concept enables control over the switching losses, current and voltage overshoot, and the current and voltage slopes of a discrete SiC MOSFET. The gate driver concept accomplishes this by introducing an intermediate voltage level during the turn-on and turn-off process. This proposed gate driver concept is based on a literature review performed in a specialization report preceding this Master Thesis [1]. In order to investigate and verify the efficacy of the proposed gate driver concept, a comprehensive simulation study and experiments have been performed.

The goal of this Master Thesis can be summarized as:

**Achieving influence over the switching performance of a discrete SiC MOSFET utilizing a four level voltage active gate driver**

This structure of the Master Thesis is as follows: The relevant SiC MOSFET and gate driver theory is covered in Chapter 2. In this chapter, theory regarding modes of failure for SiC MOSFETs and accelerated lifetime tests (ALTs) are also presented. The last part of Chapter 2 presents a short literature study regarding gate driver concepts that can achieve Active Temperature Control (ATC) in the power semiconductor device. Chapter 3 presents the four level voltage AGD concept. In Chapter 4, the DPT circuit used for the simulation study is presented. This chapter also discusses how the proposed AGD concept is implemented in the simulations. The functionality needed to perform the simulation study and evaluate the results is also presented here. Chapter 5 details the design and assembly of a printed circuit board (PCB) capable of producing the gate voltage pattern needed for the proposed AGD concept. The rest of the experimental test setup is also presented in this chapter, alongside the functionality needed to process and evaluate the experiment results. The simulation study and experiment results are presented and discussed in Chapter 6. Chapter 7 presents a summary of the Master Thesis and evaluates the performance of the proposed AGD against the goal of the Master Thesis. The report is concluded with a chapter detailing further work (Chapter 8)

Based on the same proposed AGD concept, a part of the simulation study and the experimental DPTs presented in this Master Thesis was submitted to the 2022 IEEE 13th international symposium on power electronics for distributed generation systems (PEDG 2022). The paper was accepted and will be presented at the PEDG 2022 conference in Kiel, Germany, in June 2022. The paper was written in

cooperation with the main and co-supervisors of this Master Thesis. A preprint version of the paper can be found in Appendix 8.

# 2 Theory

This chapter will cover the basics of MOSFET structure, electrical properties, and operation principles. A short comparison between the material properties of Silicon (Si) and SiC is also introduced. The purpose of gate driver circuits and different gate driver concepts are also introduced in this chapter. The last part of this chapter introduces modes of failure within SiC MOSFET as well as papers introducing gate driver concepts capable of improving the reliability in SiC MOSFET through ATC.

This chapter of the Master Thesis was based on a similar theory chapter introduced in the Specialization Report preceding this Master Thesis [1]. In order to improve conciseness and clarity, irrelevant parts were removed, and most of the chapter was rewritten. To improve the visual profile of this Thesis, most of the figures in this chapter were also created instead of being taken from the references.

## 2.1 MOSFETs

This section of the chapter will present basic theory on MOSFETs, such as structure, turn on/off process, electrical properties, and operation principles. Critical phenomena for the operation of MOSFETs will also be covered.

#### Structure

In Fig. 1, the cross-section of a MOSFET cell can be seen. The MOSFET cross-section is the smallest structure that functions as a MOSFET. As can be seen in Fig. 1, the MOSFET has three terminal types, the drain (D), the source (S), and the gate (G). Several of these MOSFET cells in parallel form a MOSFET die [5]. In addition to the MOSFET cells, the die has metalized contact surfaces which enable the terminal of the MOSFET die to be connected to outer circuitry [8, 9]. These surfaces can be seen in Fig. 1. Different bonding techniques such as soldering, wire bonding, or sintering can be used to make connections to outer circuitry. Apart from the gate oxide and metalized contacts, the MOSFET cell consists of semiconducting material. Examples of these semiconducting material are Si or SiC [5, 8].

For the MOSFET to function, impurities must be introduced to regions of the semiconducting material. These impurities alter the electrical properties and are called doping. There are two types of doping: P-type doping and N-type doping. In P-type doping, an element lacking sufficient valence electrons is added to the semiconductor material. The lack of valence electrons causes free electrons in the semiconductor to move into these holes. This results in an area of the semiconducting material having more free holes than free electrons, making the holes the majority carrier. For N-type doping, an element with more an abundance of valence electrons is added to a region of the semiconductor material. This causes the semiconductor to have more free electrons than free holes, making the electrons the majority carriers. If Si is the semiconductor material, boron and phosphorous are examples of elements that can be used for P-type and N-type doping, respectively. [5, 8]

In the MOSFET cell seen in Fig. 1, the gate and source terminal is separated by an insulator (for example silicon dioxide [5]). The source and drain are parted by a semiconductor consisting of a $N^+PN^-N^+$ structure. A MOSFET with this structure is called an enhancement mode N-channel MOSFET. The area with P-doped semiconductor material in Fig. 1 is called the body region.

The voltage between the gate and the source terminal determines if the MOSFET cell conduct current or not. For an enhancement mode N-channel MOSFET, a positive gate-source voltage must be applied for the MOSFET to turn on. If this voltage is sufficient, a layer of free electrons (or free holes for P-channel MOSFETs [5]) will form in the part of the body region straight below the gate oxide. This connects the $N^+$ and $N^-$ regions of the semiconductor material and allows current to flow from the drain to the source. It is called an N-channel due to a channel (or layer) with the same majority carrier as the semiconductor material at the source and drain terminals being required to form in the body region for the MOSFET to conduct current. [8, 10]

Due to the NPN junction in the MOSFET cell, a parasitic bipolar junction transistor (BJT) is formed between drain and source. The body and the source region are shorted to combat this BJT turning on.

This can be seen in Fig. 1. However, this body-source short causes a $P^+N^-N^+$ structure to be formed between the drain and source. In this semiconductor structure, a PN-junction is included. This junction forms a diode. This diode is known as the body diode, and in third quadrant (negative drain-source voltage and drain current) operation, the diode is forward biased [5, 10]

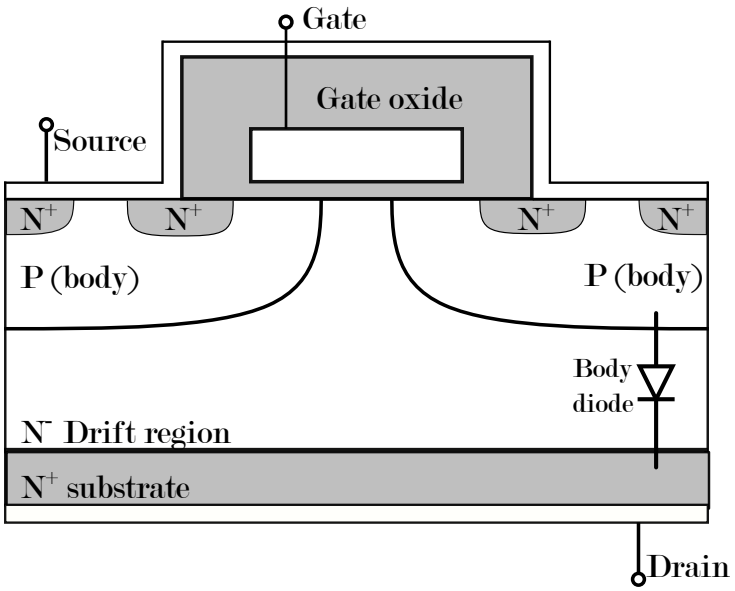



Figure 1: Cross-section of a N-channel MOSFET cell. Based on [5, 11, 12]

A circuit representation of s n-channel MOSFET can be seen in Fig. 2.

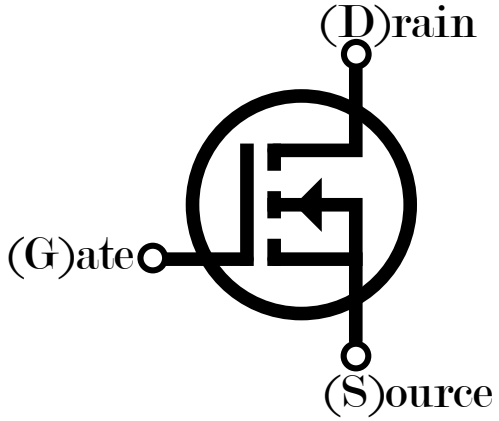



Figure 2: Circuit representation of a MOSFET

**Types of MOSFETs**

There are several types of MOSFETs. The four different types can be seen in Fig. 3. The types of MOSFETs are differentiated based on the doping profile and how the current flow is controlled. In N-channel MOSFETs, the body region is P-doped, and the source and drain layers are N-doped [13]. P-channel MOSFETs, the body region is N-doped, and the source and drain layers are P-doped [13]. Enhancement type MOSFETs needs a sufficiently large positive voltage between the gate and the source for current to flow from drain to source [14]. Depletion type MOSFETs require a sufficient negative gate-source voltage to stop current from flowing drain to source [14].

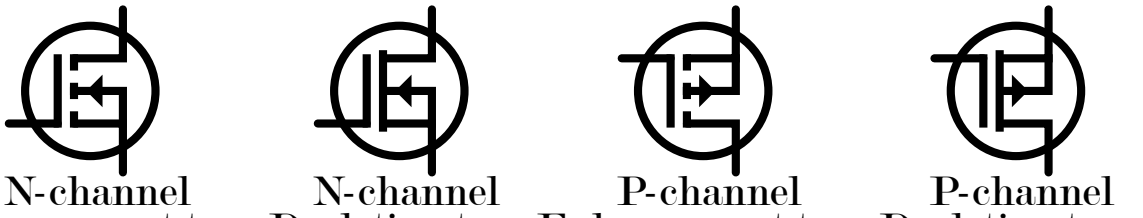



Figure 3: Circuit representation of different MOSFET types

**Formation of the Inversion Layer**

To turn on an enhancement, N-channel SiC MOSFET, which enables current to flow from the drain to the source of the MOSFET, sufficient positive gate-source voltage must be applied. How applying this gate-source voltage enables the enhancement, N-channel MOSFET to conduct current is detailed in Fig. 4. In Fig. 4a, a small positive gate-source voltage is applied. This causes a positive charge to build in the gate oxide region on top of the gate electrode. This can be seen in Fig. 4a The positive charge repels holes in the body region close to the gate electrode, leaving a layer of negatively charged acceptors. This is called the depletion layer, as it is depleted of positive majority charge carriers. As the gate-source voltage increases, the depletion layer grows in thickness, repelling more free holes. As free holes are repelled, free electrons also accumulate in the depletion layer. This can be seen in Fig. 4b. These electrons are generated by thermal-ionization caused by the growing depletion layer pushing free holes away. This layer of free electrons is called the inversion layer.

When the applied gate-source voltage reaches a specific value, called the threshold voltage, the density of free electrons in the depletion layer becomes equal to the concentration of free acceptors in the depletion layer. At this point, the inversion layer reaches from the drain to the source terminal, creating a highly conductive path. At this point, a current starts to flow from the drain to the source, called $i_{\mathrm{D}}$ This can be seen in Fig. 4c Increasing the gate-source voltage past the gate threshold voltage increases the conductivity of the inversion layer. There is a maximum voltage that can be applied between gate and source. Exceeding this voltage can cause a breakdown of the gate oxide, destroying the device. [5, 8]

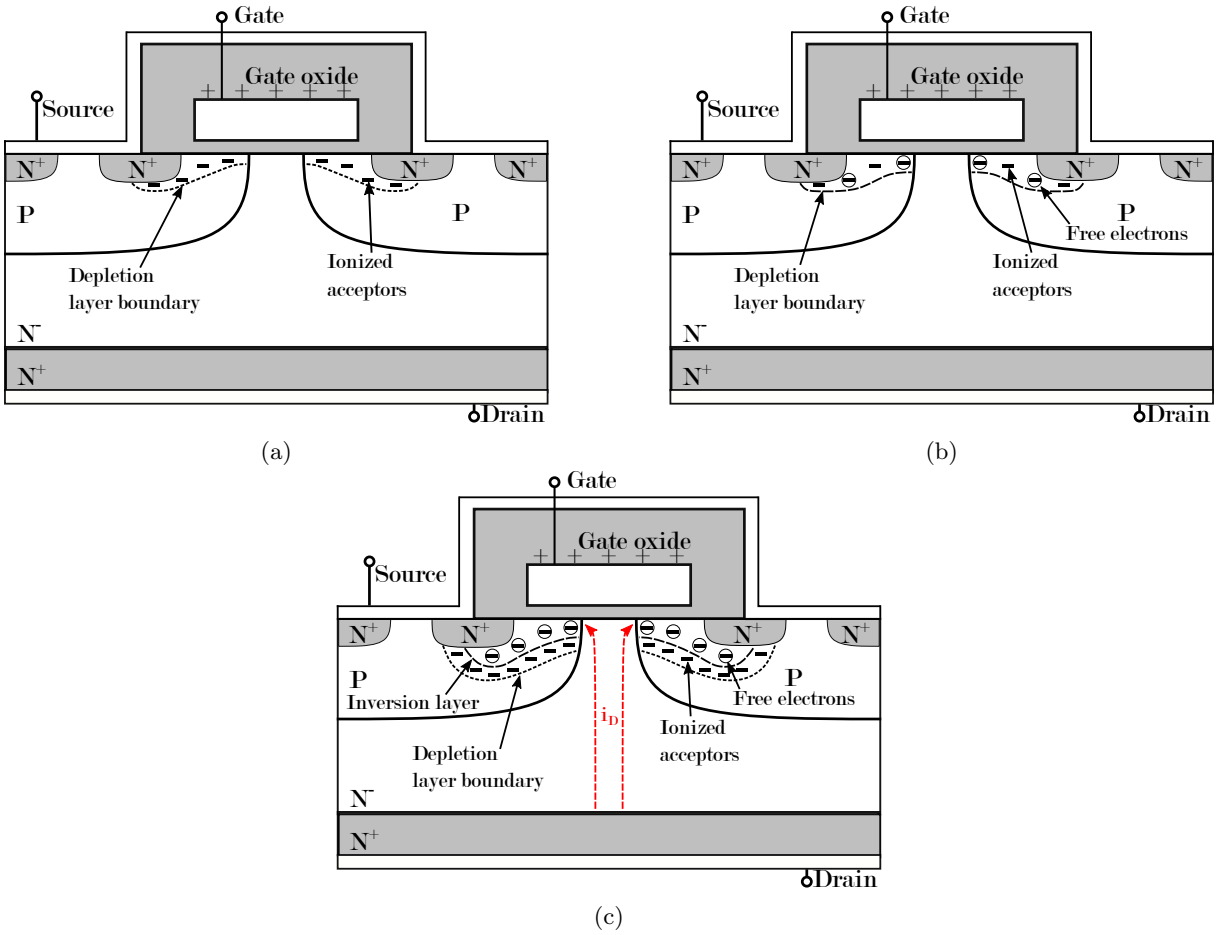



Figure 4: Formation of depletion layer and inversion layer. Based on [5, 11, 12]

### Materials - Silicon versus Silicon-Carbide

As mentioned in Chapter 1, power semiconductor devices will play a vital role in the electrification of society and the pivot to fossil-free energy production. To meet these challenges, significant effort has been put into improving the capabilities of power semiconductor devices. One of the results of this effort is Wide-bandgap devices, such as SiC and Galium Nitride (GaN) based devices. The focus of this Master Thesis will be in SiC MOSFETs.

Compared to Si, the traditional material used in power semiconductor devices, SiC has superior material qualities. Some of these material qualities include:

- **Bandgap Energy:** SiC has a bandgap energy approximately three times higher than Si. [15, 16]
- **Critical Field Breakdown Voltage:** SiC has a critical field breakdown voltage approximately ten times higher than Si.[15, 16]
- **Saturation Velocity:** SiC has a saturation velocity approximately two times higher than Si. [15, 16]
- **Electron Mobility:** Si has a electron mobility approximately 50 % times higher than SiC. [15, 16]
- **Thermal Conductivity:** SiC has a thermal conductivity approximately three times higher than Si. [15, 16]

These differences in material properties between SiC and Si lead to significant system benefits. The increased bandgap energy and critical field breakdown voltage allow for higher system voltages. Increased

saturation velocity and electron mobility enable lower switching losses, leading to higher switching frequency and smaller filters. Increased thermal conductivity leads to lower cooling demands. [17, 15]

There are also some differences in material qualities that could be disadvantageous if not taken into account. This includes the fact that SiC MOSFETs in general have low gate threshold voltage, low maximum negative gate voltage, and a big internal gate resistance. [18]

### Current-Voltage Characteristics

As mentioned earlier in this chapter, the primary function of a MOSFET is to act as a switch, where $v_{\mathrm{GS}}$ controls whether the MOSFET conducts current or not. Fig. 5 shows the relationship between $v_{\mathrm{DS}}$ and $i_{\mathrm{D}}$ as well as the impact of $v_{\mathrm{GS}}$ for a N-channel enhancement MOSFET. This is known as a current-voltage characteristic. As seen in Fig. 5, the current-voltage characteristic can be split into three different regions. If the $v_{\mathrm{GS}}$ is below a specific threshold value, known as threshold voltage ($V_{\mathrm{TH}}$), almost no current can flow through the device. This is known as the cutoff region. If $v_{\mathrm{GS}}$ is larger than $V_{\mathrm{TH}}$, the MOSFET is driven in to the ohmic region. Here, the MOSFET acts as a resistor and $i_{\mathrm{D}}$ depends on both $v_{\mathrm{DS}}$ and $v_{\mathrm{GS}}$. When $v_{\mathrm{DS}}$ reaches a specific value, the MOSFET transitions from the ohmic region to the active region. In this region, a higher $v_{\mathrm{DS}}$ will not yield a significantly higher $i_{\mathrm{D}}$. To increase $i_{\mathrm{D}}$ in this region, $v_{\mathrm{GS}}$ must be increased. drain-source breakdown voltage ($BV_{\mathrm{DSS}}$) is the maximum $v_{\mathrm{GS}}$ the MOSFET can withstand. [5]

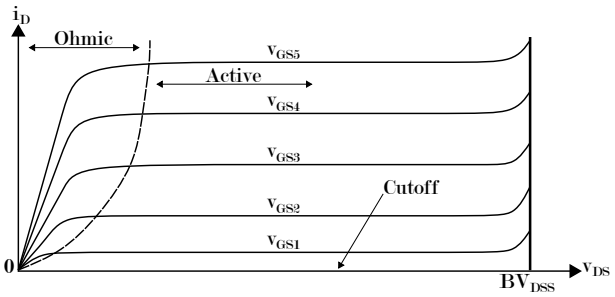



Figure 5: N-channel enhancement mode MOSFET current-voltage characteristic. Based on [5].

### Parasitic Elements

Electrical components, such as capacitors or inductors, have unwanted electrical properties that cause non-ideal behavior [19]. For example, the datasheets of capacitors often model these unwanted electrical properties as an equivalent series resistance (ESR) and equivalent series inductance (ESL) value [20]. In power electronic applications, unwanted electrical properties are often called parasitics.

The parasitic capacitances between the different terminals of the MOSFET are significant during switching transients [5, 21]. A circuit representation of an N-channel enhancement MOSFET with these parasitic capacitances can be seen in Fig. 6. $\mathrm{C}_{gd}$ is the parasitic capacitance between gate and drain. Similarly, $\mathrm{C}_{gs}$ and $\mathrm{C}_{ds}$ are the parasitic capacitances between gate-source and drain-source, respectively.

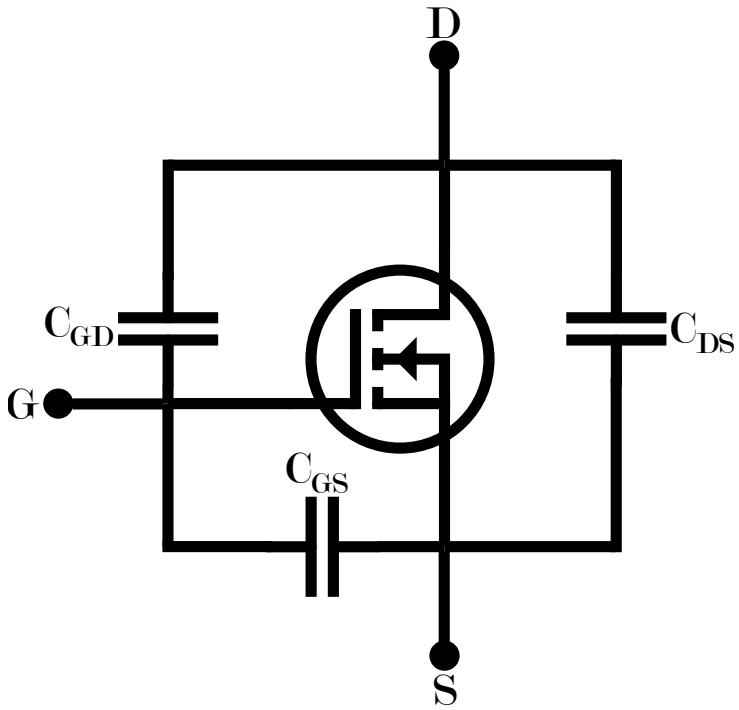



Figure 6: N-channel enhancement mode MOSFET with parasitic capacitances modelled. Based on [5].

In datasheets, equivalent device capacitances are usually provided instead of the parasitic capacitances between terminals. These are termed input capacitance ($C_{\text{iss}}$), output capacitance ($C_{\text{oss}}$) and reverse transfer capacitance ($C_{\text{rss}}$) and can be seen in Eq. 2.1. [21] These parasitic capacitances change in value based on the applied $v_{\text{DS}}$. [22, 21]

$$\begin{aligned} C_{iss} &= C_{GS} + C_{GD} \\ C_{oss} &= C_{DS} + C_{GD} \\ C_{rss} &= C_{GD} \end{aligned} \tag{2.1}$$

Equivalent device capacitances vary based on on the applied drain-source voltage. Fig. 7 show a plot of this for the C3M0075120K SiC power MOSFET from Wolfspeed [23].

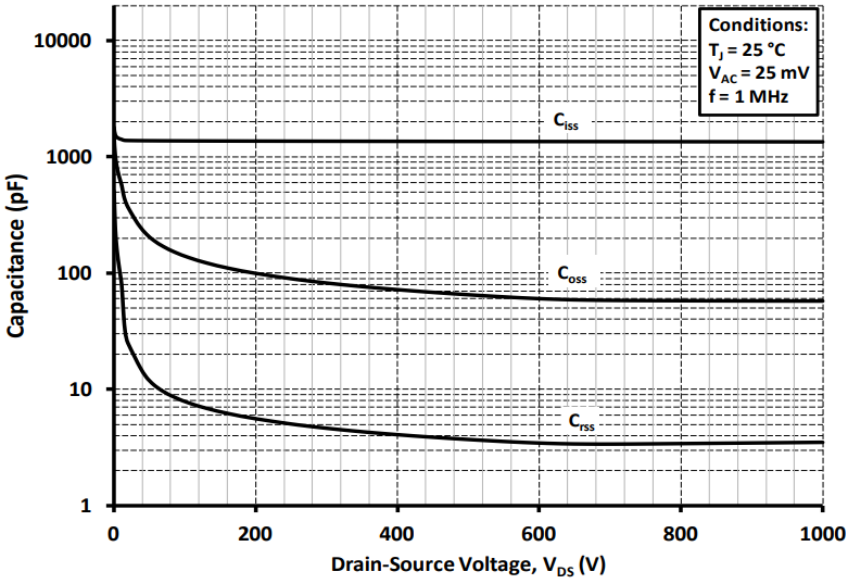



Figure 7: Equivalent device capacitances as function of drain-source voltage. From [23]

Fig. 8 displays a half bridge circuit, consisting of an upper MOSFET ($Q_{\mathrm{U}}$) and a lower MOSFET ($Q_{\mathrm{L}}$), with parasitic inductances and capacitances included. $\mathrm{L}_P$ is the lumped parasitic inductances present in the power loop of the half-bridge. This term include parasitic inductances from the DC-link voltage ($V_{\mathrm{DC}}$), the MOSFET packages and other parasitic inductances external to the device terminals. $L_{\mathrm{GX}}$ represent the inductance present in the gate loop of either the upper of lower device $R_{\mathrm{GX}}$ represent the total resistance present in the gate loop of either the upper or lower device. [24]

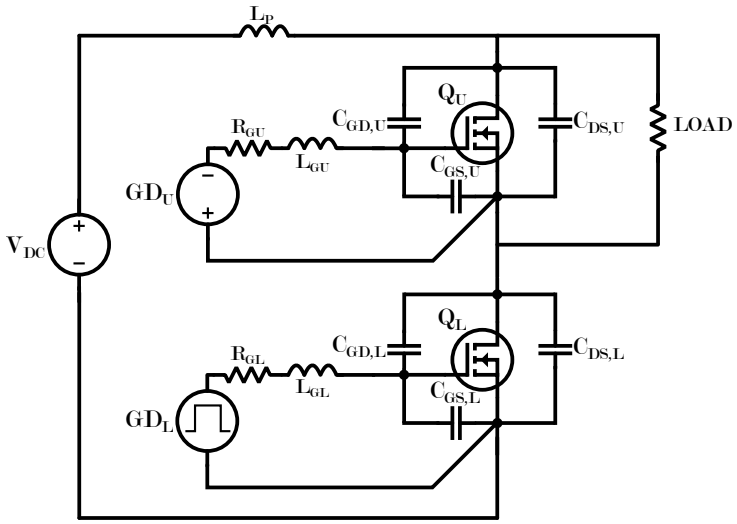



Figure 8: Half bridge circuit displaying important parasitic elements. Based on [24].

Parasitic elements influence the performance of power electronic applications. Resonance circuits can form between parasitic elements causing oscillations as well as voltage overshoot at turn-off. Capacitors oppose immediate changes in voltage and inductors oppose immediate changes in current [5]. Therefore, the presence of parasitics can also impact switching speed. If not properly considered and dealt with, parasitic elements can have major consequences. An example of this is inadvertent turn-on of the device. [25]

These consequences will be covered in more detail later in this Master Thesis.

### MOSFET Variants - Discretes and Modules

MOSFET devices come in two variants, discrete devices, and modules. Discrete MOSFETs consists of a single die, packaging, and contact pins for the gate, source, and drain terminals. Discrete MOSFETs is often without internal insulation and comes in different packages, such as the transistor outline (TO) family or in surface mounted device (SMD) packages. The lack of electrical insulation causes them only to contain one die. MOSFET modules have an insulated architecture. In MOSFET modules, the different electrical components are electrically insulated against the mounting surface. The mounting surface dissipates the heat generated [8].

MOSFET modules can house several dies in parallel per electrical function and come in several configurations, such as single switch, half-bridge, and H-bridge [26]. In the H-bridge configuration, two half bridge circuits are connected in the shape of the letter H. The load is connected in-between the two half bridge circuits. A single switch has the same schematic representation as seen in Fig. 6. A half bridge schematic representation can be seen in Fig. 8. The cross-section of a die in a MOSFET module package can be seen in Fig. 9. The different dies in the MOSFET module are soldered together using bond-wires. The dies are also soldered to a Direct Bonded Copper (DBC) substrate, which is soldered to a baseplate not visible in Fig. 9. The DBC substrate severs to transfer heat away from the die and provide electrical insulation [8].

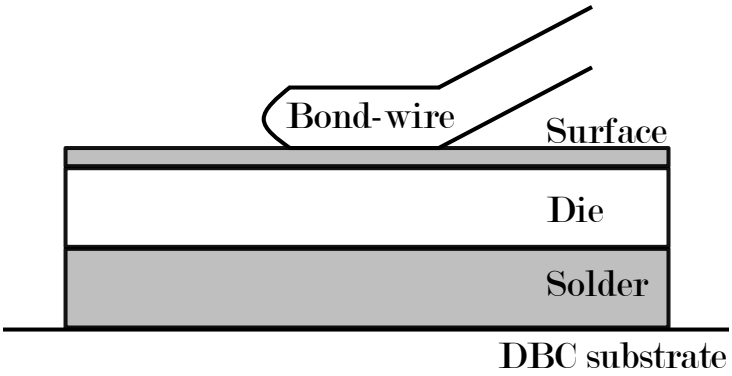



Figure 9: Cross-section of a MOSFET module package. Based on [12].

Inside a MOSFET module, internal tracks connect the electrical components inside the module. These internal tracks cause increased parasitic resistances and inductances compared to discrete MOSFETs. Isolated substrates within the modules also cause the increased parasitic capacitance, compared to discrete MOSFETs [8].

By comparing a discrete MOSFET (C3M0075120K from Wolfspeed) and a MOSFET module (CAB530M12BM3 from Wolfspeed), both 3rd generation devices from the same manufacturer with the same blocking voltage rating, differences between the types of MOSFETs can be identified. The choice of devices is arbitrary and exemplary. For the same junction temperature, C3M0075120K has a rated drain current of 30 A, while CAB530M12BM3 has a rated drain current of 225 A. Due to modules having dies in parallel, they can support higher currents. CAB530M12BM3 has much higher equivalent device capacitances compared to C3M0075120K. At similar testing conditions, CAB530M12BM3 has equivalent device capacitances in the nF range, while C3M0075120K has equivalent device capacitances in the pF range. Higher equivalent device capacitances cause slower switching speed, This is reflected in the datasheets of the two devices [23, 27].

### Idealized Switching characteristics of a MOSFET

Fig. 10 shows the idealized switching waveforms for an enhancement type MOSFET. The waveforms correspond to a circuit like the one in Fig. 8, where $Q_{\mathrm{U}}$ is the freewheeling device (FD) and $Q_{\mathrm{L}}$ is the switching device (SD). However, for simplicity, the parasitic inductances are neglected for the waveforms in Fig. 10 and the body diode of $Q_{\mathrm{U}}$ is assumed to be ideal [28].

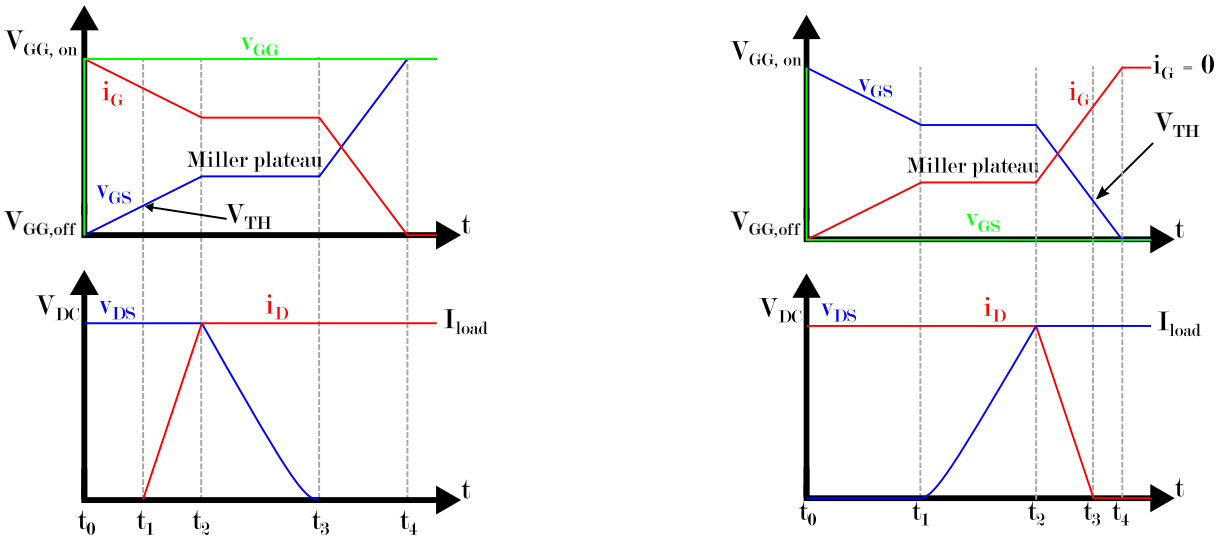



Figure 10: Ideal switching waveforms for a MOSFET during (a) turn-on and (b) turn-off. Based on [22, 28].

The turn on event, which can be seen in Fig. 10a can be split into three time intervals:

- **$t_0$ - $t_1$**: A $t_0$ gate driving voltage ($V_{GG}$) changes from $V_{GG,off}$ to turn-on driving voltage ($V_{GG,on}$). This causes gate current ($i_G$) to start flowing into the gate, which causes $v_{GS}$ to rise. [28]
- **$t_1$ - $t_2$**: When $v_{GS}$ reaches $V_{TH}$, $i_D$ starts to rise linearly until it reaches the load current value. $v_{GS}$ continues to rise. [28]
- **$t_2$ - $t_3$**: When $i_D$ reaches $I_{LOAD}$, $v_{DS}$ starts to drop. Linearly at first, but the rate of change lessens when $v_{DS}$ approaches its on-state value. In this time period $v_{GS}$ and $i_G$ remain constant, this time interval is known as the Miller plateau. This is due to almost all of $i_G$ charging $C_{GD}$ instead of $C_{DS}$. This time interval ends when $v_{DS}$ reaches its off-state value. At this point $v_{GS}$ resumes rising and $i_G$ resumes falling [28].
- **$t_3$ - $t_4$**: This interval ends when $i_G = 0$ and $v_{GS} = V_{GG,on}$ [28].

The process for turning off a MOSFET is similar to the turn-on process, but the commutation of drain current and gate-source voltage occur in reverse. This can be seen in Fig. 10b.

As seen in Fig. 10a and 10b, there is a time duration when $v_{GS}$ and $i_G$ is clamped at a certain voltage and current value, called the Miller plateau. During this plateau $v_{DS}$ must either fall to approximately 0 V or rise to $V_{DC}$. This depends on whether a turn-on or turn-off transition is occurring. During a turn-on transition, while $v_{DS}$ rapidly falls in value, $C_{GD}$ is discharged. This limits $i_G$ to precisely the $C_{GD}$ discharge current. If $i_G$ was different, a current would also flow into $C_{GD}$, causing an increase in $v_{GS}$. As can be seen in Fig. 5, increasing $v_{GS}$ causes more current to flow. This is impossible as the MOSFET is carrying the entire load current when the Miller plateau begins. Therefore, $v_{GS}$ must remained clamped during the fall of $v_{DS}$. Similarly, in a turn-off transition, while $v_{DS}$ rapidly rises in value, $C_{GD}$ is charged. This limits $i_G$ to exactly the $C_{GD}$ charge current. If this were not the case, current would also flow from $C_{GD}$, causing a decrease in $v_{GS}$, which reduces $i_D$. This is impossible as the load current can not be taken by the diode of the FD, due to the voltage commutation of the SD not being finished. Therefore, $v_{GS}$ must remained clamped during the rise of $v_{DS}$.

### Losses in the MOSFET

Losses in a MOSFET come from two primary sources: Losses stemming from switching transients and losses occurring when the device is fully on. These losses are called switching losses and conduction losses,

respectively. Using Eq. 2.2, average MOSFET conduction loss ($P_{\mathrm{C,M}}$) can be calculated. $P_{\mathrm{C,M}}$ depend on switching sime ($P_{\mathrm{sw}}$), on-state resistance ($R_{DS,on}$) and instantaneous drain current ($i_{\mathrm{D}}(t)$). [29].

$$P_{C,M} = \frac{1}{T_{sw}} \int_0^{T_{sw}} \left( R_{DSon} \cdot i_D^2(t) \right) dt \tag{2.2}$$

Switching losses can be calculated using eq. 2.3 and depend on turn-on switching loss ($E_{\mathrm{on}}$), turn-off switching loss ($E_{\mathrm{off}}$) and switching frequency ($f_{\mathrm{sw}}$). $E_{\mathrm{on}}$ and $E_{\mathrm{off}}$ are the products of the instantaneous values of $v_{\mathrm{DS}}$ and $i_{\mathrm{D}}$ during the turn-on and turn-off transients. [29]

$$P_{sw,M} = (E_{on,M} + E_{off,M}) \cdot f_{sw} \tag{2.3}$$

In Fig. 11, an example of $E_{\mathrm{on}}$ can be seen. A definition for when the switching transients occur is required to determine the switching loss energies. For example, in Fig. 11, the switching transients are defined as occurring when $v_{\mathrm{DS}}$ and $i_{\mathrm{D}}$ are between 10 and 90 % of their final on- or off-state values. The start of the switching transient is denoted as $\mathrm{t}_S$. The end of the switching transient is denoted as $\mathrm{t}_E$.

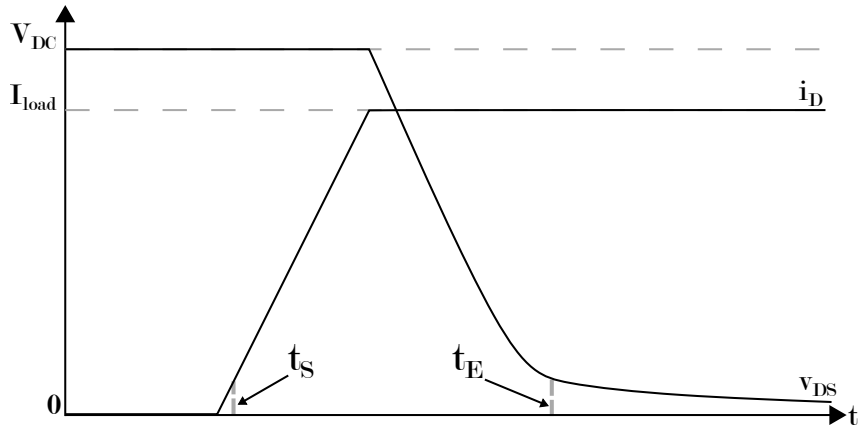



Figure 11: Example of the switching energy generated during a turn-on of a MOSFET. Modified from [22].

### Impact of Parasitic Elements

As mentioned earlier, the switching process presented in Fig. 10 is based on simplification and idealization. Had the parasitic inductances and the reverse recovery of the FD been considered, several factors would have influenced the switching waveforms seen in Fig. 10. The Miller effect was shown in Fig. 10 and w The impact of these phenomena includes:

**Overshoots:** During turn-on, an overshoot in $i_{\mathrm{D}}$ would occur. This is caused by the reverse recovery of the FD. The charge from the body diode in the FD flows into the SD, causing the overshoot in drain current. The body diode of the FD contains charge as it has been conducting the load current while the DUT was turned off. This charge must be discharged to that the body diode can conduct again when the DUT turns off [5, 8]. The overshoot in $i_{\mathrm{D}}$ could cause the failure of the SD if the maximum $i_{\mathrm{D}}$ of the MOSFET is exceeded. During the turn-off of a MOSFET, $i_{\mathrm{D}}$ falls rapidly. This fall in current causes a voltage drop across the parasitic inductance in the power loop, which is opposite in direction with regards to the increasing $v_{\mathrm{DS}}$. This results in a voltage overshoot in $v_{\mathrm{DS}}$ [28]. If this voltage overshoot causes the $v_{\mathrm{DS}}$ to surpass the breakdown voltage of the MOSFET, failure of the device could occur [30].

**Oscillations:** The parasitic inductances and capacitances present in the power loop will form a resonant circuit. During switching transients, these resonant elements will exchange energy, causing oscillations in both $v_{\mathrm{DS}}$ and $i_{\mathrm{D}}$. These oscillations are also called "ringing" [24].

## 2.2 Gate Drivers

The turn-on/turn-off process in a MOSFET can be compared to charging/discharging a capacitor. This means charge has to be provided and removed from the MOSFET in order to control it. To address this, dedicated gate driver circuits are used. These circuit are controlled and drive/remove charge into/from the power MOSFET [7].

Gate driver topologies can be sorted based on their adaptability. Passive gate drivers have a set way of operation, configured during production. In order to alter the functionality of these gate drivers, physical changes must be performed, such as changing the external gate resistance. On the other hand, active gate drivers are adjustable during operation. The operation of these gate drivers can be altered online. In this chapter, three gate driver concepts will be introduced.

### Conventional Gate Driver Concept

The most common gate driver concept is the Conventional Gate Driver (CGD) concept. In this concept, two voltage levels, $V_{\mathrm{GG,on}}$ and turn-off driving voltage ($V_{\mathrm{GG,off}}$), can be supplied to the gate of a MOSFET [31]. Fig. 12 is an example of the CGD concept. Utilizing two switches, controlled with a Pulse Width Modulation (PWM) signal, a power MOSFET can be controlled. Turning the upper switch on and the lower switch off, charge can be driven into the gate of the MOSFET. Changing the states of the switches, the gate of the MOSFET can be discharged. This will turn the MOSFET off.

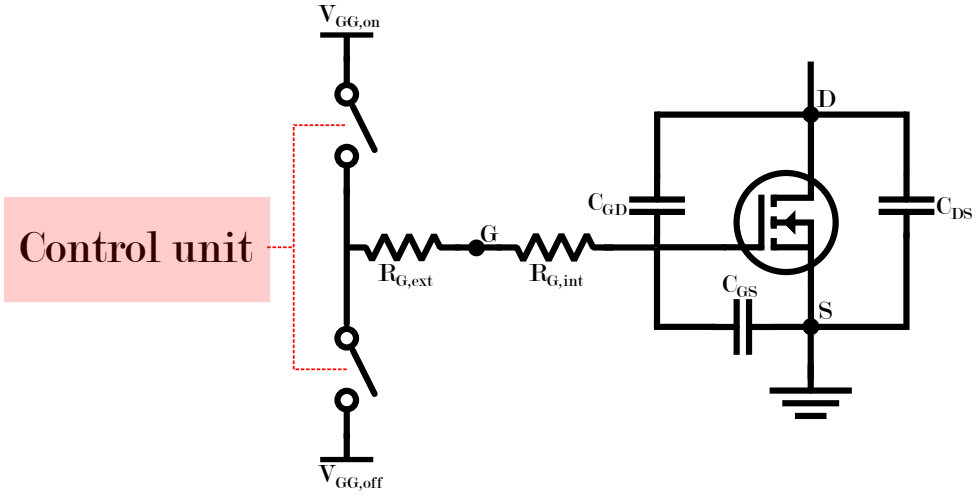



Figure 12: A schematic of a conventional gate driver. Based on [32].

### Current Source Gate Driver Concept

Compared to the CGD-concept, where constant voltage levels charge/discharge the gate of the power MOSFET, the Current Source Gate Driver (CSG)-concept utilizes a current source to deliver charge. An example of a CSG can be seen in Fig. 13. The CSG comprises four switches, a control unit, and an inductor. Through manipulating the switches, the inductor can be magnetized. By magnetizing the inductor with a positive polarity, with regards to the gate of the SD, a positive gate current can flow when the SD needs to turn on. For the turn off event, the inductor is charged with a negative polarity in terms of the MOSFET gate. The charge build up can be partially done before the SD need to turn on or off, utilizing pre-charge time intervals. The goal of this CSG is to reduce switching loss and loss in the gate driver itself, compared to operation using CGD. During the turn-on or turn-off event of a CGD, the gate current rises quickly to a max value and drops off in value. This can be seen in Fig. 10. However, in the CSG concept, the gate current is almost constant during the entire commutation process. This reduces switching times, thereby reducing switching losses. After the turn-on or turn-off of the power MOSFET, through the use of the four switches, the excess energy stored in the inductor can be returned

to the power supply of the CSG. This recovers gate energy that is dumped to ground in a CGD. The description of the CSG is based on [32].

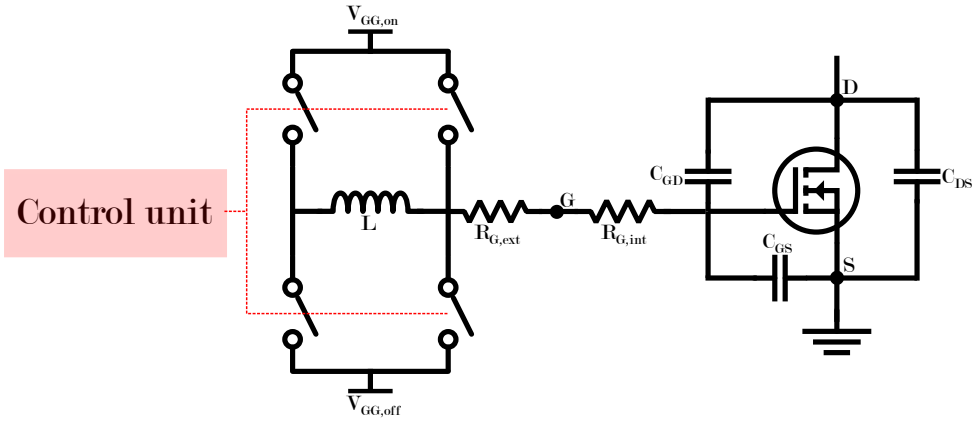



Figure 13: Exemplary schematic of a CSG. Based on [32]

### Multilevel Gate Driver Concept

In the CGD-concept, there are two voltage levels available. A turn on level and a turn off level. As opposed to that, in the multilevel gate driver concept, more voltage levels are used throughout the switching events. Yang et al. introduced a one intermediate voltage level at turn on and another at turn off [30]. Miyazaki et al. a 63 voltage level multilevel gate driver is introduced [33].

### Crosstalk

Due to the material properties of silicon carbide, SiC MOSFETs can operate at higher switching frequencies compared to MOSFET using other semiconductor materials. Increased switching speed makes the impact of parasitic elements in power electronic applications larger. Increased impact of parasitic elements causes large oscillations and overshoots during switching events, reducing the performance of the application [30].

One of the problems that stem from this is the crosstalk effect. This effect occurs when one of the devices in a half bridge setup goes through a switching event. Since the external gate resistance of the gate driver decouples the terminal voltage ($v_{\mathrm{GS}}$) from $V_{\mathrm{GG}}$, $v_{\mathrm{GS}}$ can vary in value. During the turn-on and turn-off event of a device, the internal capacitances of the device need to be charged/discharged. This will cause currents to flow to/from the device, not switching. These currents will interact with the gate resistance of the complementary device and induce a change in the gate-source voltage of the complementary device. This is known as crosstalk and occurs both at turn-on and turn-off in the SD. Fig. 14 shows the direction of currents generated by crosstalk when the upper device, $\mathrm{Q}_U$, turns on or off. When $\mathrm{Q}_U$ turns off, $\mathrm{C}_{DS,U}$ will begin to charge. This causes $\mathrm{C}_{GD,L}$ to discharge, which in turn causes current to be drawn from $\mathrm{C}_{GS,U}$ and $\mathrm{GD}_L$. These currents cause a negative spike in the $v_{\mathrm{GS}}$ of $\mathrm{Q}_L$. This causes a voltage drop, which is negative with regards to $\mathrm{GD}_L$, in the gate loop. This results in the gate-source voltage becoming more negative than the voltage level provided by $\mathrm{GD}_L$.

During the turn on of $\mathrm{Q}_U$, the $v_{\mathrm{GS}}$ of $\mathrm{Q}_L$ will experience a positive voltage spike. [34, 35]

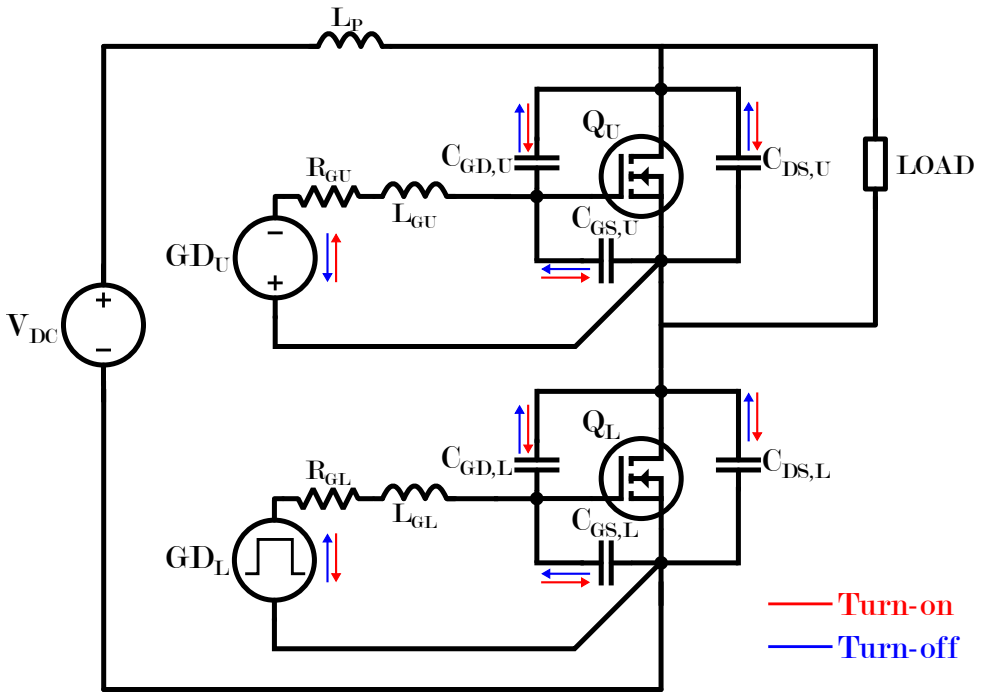



Figure 14: Two MOSFETs in half bridge configuration. The direction of current caused by crosstalk generated by $Q_U$ switching state. Based on [35].

The consequences of crosstalk can be severe. If the positive spike in $v_{GS}$ passes the gate threshold voltage of $Q_L$, it could cause $Q_L$ to turn on accidentally. This creates a short circuit in the bridge arm as both $Q_U$ and $Q_L$ conduct current. Shoot-through faults can have significant consequences. These short circuit currents cause increased losses due to the $Q_L$ blocking the entire supply voltage when $Q_U$ is on. Time duration with high current and high voltage cause increased losses. In the worst case, these faults can lead to thermal runaway in the device. Thermal runaway is a positive feedback loop where self-heating from losses in the device cause increased current to flow. This increased current causes increased losses, which cause increased heating [36]. In order to shoot through faults, there must be sufficient time between when the active device turns off, and the complementary device turns on. This is known as deadtime [37].

On the other hand, the negative voltage spike could cause the gate-source voltage to exceed the maximum negative gate voltage the MOSFET can withstand. This can lead to the breakdown of the gate oxide [34, 35].

## 2.3 Modes of Failure in Power Semiconductor Devices

In this chapter, modes of failure and their degradation mechanisms, device parameters indicating device fatigue and models predicting device lifetime for SiC power MOSFETs will be presented.

### Modes of Failure within power SiC MOSFETs

SiC MOSFETs face different types of stress, depending on the type of application and conditions the devices are used in. This causes fatigue, degradation, and potential faults to appear in different locations in the devices. Fatigue types can be split based on if they occur in the chip or the package [12].

For SiC MOSFETs there are three chip-level fatigue mechanisms that will be presented in this Master Thesis:

- **Gate Oxide Degregation**: As mentioned in Chapter 2.1, there are distinct differences in the

material properties of SiC and Si [38, 39]. Due to larger bandgap energy and higher P-based doping. SiC MOSFETs must have a thinner gate oxide layer compared to Si-based devices to maintain a reasonable threshold voltage [12]. However, the quality of the interface between semiconductor and gate-oxide when using $SiC/SiO_2$ is worse compared to $Si/SiO_2$. The Carbon (C) introduced with the SiC semiconductor yields defects in the semiconductor/gate-oxide interface. These defects causes charges to be trapped at and near the interface [40]. As the device is used, the trapped charges grow deeper and deeper inside the gate oxide layer, causing the defects to become larger [12, 41]. The consequences of this are decreased device lifetime, $V_{\mathrm{TH}}$ instability and increased gate leakage current, which causes increased losses [42, 43, 44]. Instability in $V_{\mathrm{TH}}$ increases the sensitivity of SiC devices to crosstalk as SiC devices have a low $V_{\mathrm{TH}}$. Gate oxide degradation can lead to the breakdown of the gate oxide, which causes device failure [45].

- **Stacking Fault**: In applications where the body diode of the SiC MOSFET is used to conduct the reverse current, the reliability of the body diode in the device is crucial [12]. Due to the material properties of SiC, SiC MOSFET devices are more vulnerability to bipolar degradation, compared to Si devices [46]. This degradation of the body diode is caused by the formation and expansion of Stacking Faults (SFs) within the body diode [47]. SFs are faults caused by dislocations in the crystal structure of the SiC semiconductor. These dislocations are driven by the recombination of electrons and holes [48]. Consequences of SFs are increased forward voltage ($V_{\mathrm{F}}$) and $R_{DS,on}$. If these SFs grow large enough, they can lead to increased leakage current and breakdown of the body diode. [47, 46]

- **Gate Dielectric Crack**: If a short circuit occurs or avalanche conditions are present, a large amount of heat is generated, which can cause a rapid increase in the temperature of the SiC chip [12]. Due to the mismatch of Coefficients of Thermal Expansion (CTE) in the different layers of the chip, which is caused by the material properties of the different layers in the chip, temperature changes cause mechanical stress within the chip [6]. This stress can cause cracks in the $SiO_2$ gate dielectric layer. High temperature in the chip can also cause the metalized source contact in the device to melt and flow into the cracks. The result is a conductive path between the gate and source of the device, reducing gate-source resistance ($R_{\mathrm{GS}}$). This could lead to device failure as a conductive path between gate and source prevents an electric field from forming. If no electric field can form, the device can not function [49, 36, 50].

Package-level fatigue types occur in the packaging of the device. Three package-level fatigue types will be presented in this Master Thesis.

- **Bond-Wire Fatigue**: Fatigue in the bond-wires of a SiC device can be caused by several mechanisms. During temperature variations, CTE mismatch between the bond-wires and their connection points causes stress. Over time, this stress can cause the formations and the growth of cracks in the heel of the bond-wire as well as between the surface of the die and the bond-wire. As the cracks between the surface of the die and the bond-wire grows the electrical connection becomes worse. Severe cracking can cause the bond-wire to lift off their connective points [51, 52]. Heating caused by the ohmic resistance in the bond-wires lead to voids to occur within the bond wires, creating more fatigue [52]. Electromigration, the movement of atoms within the bond-wires caused by electric fields [53], also cause voids [52]. Bond-wire fatigue causes increased $R_{DS,on}$ due to worsening electrical connection. Severe bond-wire fatigue can lead to an Open-Circuit (OC) fault [12].

- **Surface Reconstruction**: Elevated temperatures can cause several issues for the metal source layer of a SiC MOSFET. CTE mismatch between source layer and the SiC substrate can cause cracking and permanent deformation of the source layer. The consequence of this can be device failure in form of a OC fault [12, 54].

- **Solder delamination**: CTE mismatch causes cracks between to SiC die and solder layer to be formed and to grow. This cracking process is driven by swings in the junction temperature of the device. [12, 55, 56] Internal voids in the solder layer can also be formed by electromigration driven by the load current flowing trough the solder layer. [12] Die solder fatigue leads to increased junction-to-case thermal resistance in the device. [12, 55, 56]

### Accelerated Lifetime Tests and Degradation Assessment

For power electronic devices used in applications out in the field, it can take a long time for a fault to appear and cause device failure. Therefore, to investigate modes of failure and the reliability of devices in a more reasonable time frame, ALTs are performed. These tests cause rapid device degradation by exposing devices to exaggerated electrical and thermal stress. Several different ALTs are used to stress the devices in different ways. By observing the mode of failure caused by the stress, failure mode and stress type can be correlated [12].

These tests can be split into several categories:

- **Gate Oxide ALTs:** These ALTs aim to cause accelerated degradation of the gate oxide in the device. When the SiC MOSFET is operated in forward conduction (current flowing from drain to source), the electric fields generated by $v_{\mathrm{DS}}$ and $v_{\mathrm{GS}}$ are the main contributors to gate oxide degradation [12].
- **Thermal ALTs:** As mentioned earlier in this chapter, several modes of failure within SiC MOSFETs occur due to CTE mismatches in the layers of the devices. Thermal ALTs aim to trigger these modes of failure. There are several thermal ALTs, such as thermal cycling and thermal shock. These tests heat the devices using an external source and therefore, these tests does not cause any electromechanical stress on the devices. To cause more realistic aging in the SiC MOSFETs Power Cycling (PC) ALTs are used instead. PC ALTs cause temperature swings in the devices by injecting a current into the devices. Injecting a current causes the conduction losses of the devices to heat up and introduces thermomechanical stress between the different layers of the device [12].
- **Body Diode ALTs:** The body diode is an important component of a SiC MOSFETs. In diode-less applications where the internal body diode is used to conduct current, the reliability of the body diode is crucial. If there are no anti-parallel diodes used in the application, then the body diodes will have to conduct current during third quadrant operation. In body diode ALTs, SFs are induced to generate failures in the DUT. For example in a DC current injection test, the body diodes of the DUTs are tested by reverse conduction the DUTs with a constant load current. A negative $v_{\mathrm{GS}}$ is applied to ensure that the DUT are completely off [12].
- **Extreme Condition ALTs:** Unforeseen event, such as surges in temperature or electromagnetic noise, can occur during the operation of power electronic devices. Devices are expected to be able to operate in conditions outside the Safe Operation Area (SOA) for short amounts of time. SOA describes how long a device can be exposed to a current and voltage without taking damage [57]. Therefore, extreme condition ALTs are used to investigate device reliability during these events. Extreme condition ALTs can include repetitive Short Circuit (SC) or unclamped inductive switching tests [12].

As described earlier in this chapter, aging in the SiC MOSFETs causes different parameters in the devices to change. Parameters such as $R_{DS,on}$ or $V_{\mathrm{TH}}$ shifting in value due to aging of the device are examples of this. Seeing as different modes of failure cause different parameters to be altered, the monitoring of some of these parameters can be used to identify the condition of the devices [58].

### Lifetime Models

Utilizing device data collected from failure events or ALTs, models estimating the Remaining Useful Lifetime (RUL) of a device can be created [6, 59]. There are several different lifetime models.

Physics of Failure (PoF) models are based on how physical parameters in a device can reflect corresponding modes of failure. For example, gate oxide degradation can cause changes in $V_{\mathrm{TH}}$. The different PoF models can be sorted based on which mode of failure they use to determine RUL. For example, Eq. 2.4 shows a PoF model for the lifetime of the bond wires in a SiC MOSFET. $\mathrm{N}_f$ denotes the number of temperature cycles until failure in a device. $\Delta T$ is overall temperature experienced during a thermal cycle. $\Delta T_0$ denotes the elastic temperature range and usually does not have a big impact, while a and n are fitting values defined by PC tests. [59]

$$N_f = a \cdot (\Delta T - \Delta T_0)^{-n} \tag{2.4}$$

This model is based on the Coffin-Manson law, an empirical law which the relates the number of cycles until failure due to plastic deformation and material-dependent constants [60, 61]. The lifetime estimation of the bond wire can be improved by considering the impact of the average junction temperature has on the number of cycles until failure. By including an Arrhenius factor to Eq. 2.4, this can be done and can be seen in Eq. 2.5. $E_a$ is the activation energy, while $k_b$ is the gas constant [6, 59].

$$N_f = a \cdot (\Delta T_j)^{-n} \cdot e^{E_a/\left(k_b \cdot T_{j\_\mathrm{avg}}\right)} \tag{2.5}$$

In order to further improve the bond wire lifetime model, the Bayerer model also considers power-on time, $t_{on}$, current flowing in the bond wire ($I_w$), the blocking voltage, ($V_B$), and the diameter of the bond wire ($D_w$) [59, 62]. Eq. 2.6 shows the Bayerer model.

$$N_f = K \cdot (\Delta T_j)^{-\beta_1} \cdot e^{\beta_2/(T_j+273)} \cdot t_{\mathrm{on}}^{\beta_3} \cdot I_w^{\beta_4} \cdot V_B^{\beta_5} \cdot D_w^{\beta_6} \tag{2.6}$$

Data-driven models aim to estimate the RUL of a device without the need of physical mechanisms. Instead, the data-driven models use data either from failures or from condition monitoring. These models can monitor variables that directly or indirectly depict system health. Based on the monitored data, and comparing it to threshold values, these models provide an estimation of the RUL. The models are based on data, while the threshold values are set based on standards and experience by the designer. The RUL estimated by these data-driven models is normally in the form of probability density functions [59].

There are also hybrid models which aim to combine PoF models and data driven models [59].

## 2.4 Active Temperature Control in Power Semiconductor Devices

Thermal cycling, or junction temperature fluctuations, are a key factor in the degradation of power electronic devices [63, 64, 65, 66]. Mismatches in the CTEs in the different layers of the devices cause thermomechanical stress between the layers [12]. Therefore, being able to reduce the junction temperature fluctuations, and thereby thermal cycling, can contribute to increase the lifetime of the power semiconductor devices [63, 65]. ATC concepts can help realize this. ATC is done by controlling one or more parameters, such as switching frequency or load current, with the goal of controlling the junction temperature in the device. What parameters to control depend on at which level the ATC system is implemented. If the ATC system is at the converter level, what parameters that can be feasibly altered without impacting performance differs compared to a component level ATC system. Circuit parameters such as external gate resistance or gate-source voltage can also be modulated to achieve ATC. However, this requires gate driver circuits that support this functionality. What parameters to control depend on the application the devices are used in [63, 64, 65].

In this chapter, four papers showcasing how ATC can be achieved using AGD concepts will be presented. The goal of this chapter is to show how ATC can help improve the lifetime and reliability of power semiconductor devices.

#### Switching Loss Control Trough Controllable External Gate Resistance Network

In [63], an AGD concept being able to alter switching losses is presented. The AGD achieves this by altering the external gate resistance. Varying losses in the power semiconductor device is one of the main causes of temperature variation, and thereby on of the main causes for thermal cycling. Therefore, being able to manipulate these losses in order to keep the losses constant can help achieve ATC and reduce thermal cycling [63].

To create the proposed AGD in [63], several components are needed. The power supply is made up of a DC-DC converter and a linear regulator. A digital signal isolator and a Complex Programmable Logic

Device (CPLD) provides the control signals. These signals are sent to the seven gate driver units. The effective external gate resistance can be controlled by varying the amount of gate driver units activated. This effective external gate resistance is determined by the duty cycle of a PWM-signal sent by the CPLD. The longer higher the duty cycle of this PWM, the higher the effective external gate resistance. What duration of the signal corresponds to which resistance is handled using a state machine. Using the proposed AGD, the effective external gate resistance can be set to 16 different values [63].

Fig. 15 shows the proposed ATC.

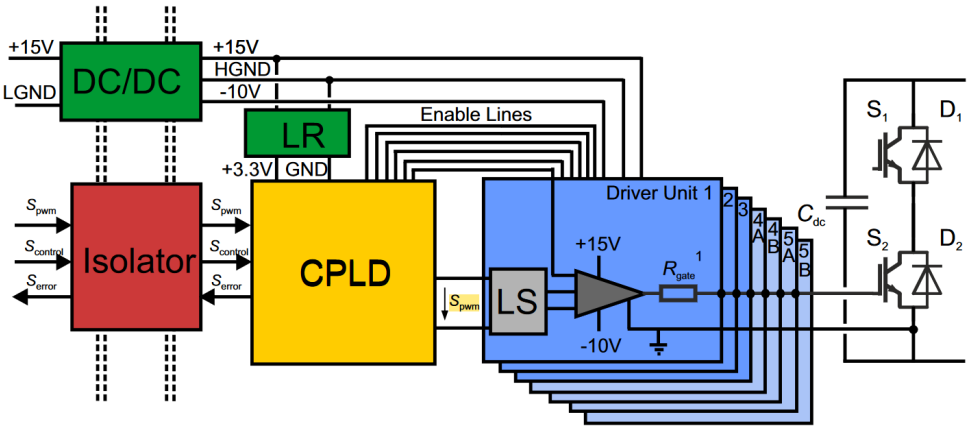



Figure 15: The proposed AGD from [63]. Screenshot from [63]

The AGD is used within a virtual heat sink control structure outlined in [63]. To experimentally verify the efficacy of the proposed AGD, two experiments were performed. One experiment used repetitive load cycles and an open loop estimation for the junction temperature. The other experiment used more realistic load cycles and a closed loop estimation. The AGD was tested in conjunction with the control structure on a decapsulated Hybridpack 2 power module, operated with a load emulator. Using a DC-link voltage kept at 25 % of the rated voltage for the module, a 20 % thermal cycle reduction was achieved [63].

This is a positive result for the efficacy of ATC. Compared to a CGD, the AGD, as well as the control system and the temperature sensing system proposed in [63] are more complicated. Even though the Hybridpack 2 contains Insulated-Gate Bipolar Transistors (IGBTs), the concept of manipulating switching losses to reduce temperature variations should hold true for MOSFETs as well seeing as switching losses are a significant source of loss in MOSFETs, especially at higher switching frequencies [5].

### Loss Control By Utilizing Variable External Gate Resistance and On-State Gate-Source Voltage

Similarly to [63], the AGD presented in [65] aims to help achieve ATC by sacrificing efficiency. By regulating external gate resistance and on-state gate-source voltage, losses in the power semiconductor device can be increased during light load conditions to mitigate junction temperature fluctuations. The AGD proposed in [65] can produce three different external gate resistance values, but considering that the output voltage of the proposed AGD can also be altered, eight total levels are available. A simplified schematic of the AGD can be seen in Fig. 16 and consists of a DC/DC converter and a resistor network. The control system providing the PWM-signal to the is not shown in Fig. 16. It is based on lookup tables derived from Simulation Program With Integrated Circuit Emphasis (SPICE) simulations. The lookup tables contain drain current and gate voltage data for the conduction phase. The switching phase uses gate resistance data as well.

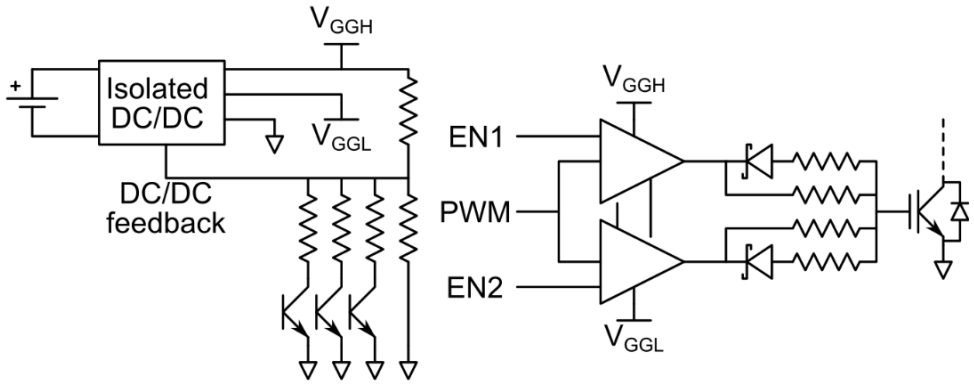



Figure 16: Simplified schematic of the AGD proposed in [65]. Screenshot from [65].

The proposed AGD was tested in both simulations and experiments. For the simulations, MATLAB and a SPICE-software was used. The simulations showed that the AGD is able to reduce temperature fluctuations for square wave load profiles, but for sinusoidal load profiles, the temperature cycling becomes worse. Using a lifetime model similar to Eq. 2.5, the ATC scheme improved the lifetime of the DUT for square wave load profiles. Regarding the experimental results, the AGD and the control system managed to reduce the temperature swing of a load change by 35 %. When tested on a 50 Hz sinusoidal waveform, the ATC system managed to control the losses in the device in order to reduce temperature swings.

The AGD and control scheme presented in [65] shows how ATC can improve the lifetime and reliability of SiC MOSFETs for certain load profiles. In the paper, 10 kHz was used as the switching frequency. This makes conduction losses the dominant source of losses. Considering that SiC MOSFETs can operate at much higher switching frequencies, the results could have been different if the switching frequency had been higher.

#### Switching Loss Control Utilizing Resistor-less Gate Driver

In [64], an ATC-scheme is introduced that aims to reduce thermal cycling by modulating the switching losses in a SiC MOSFET. Compared to [63] and [65], where the external gate resistance and gate-source voltage are changed in defined steps, [64] introduces an AGD that can modulate turn-on and turn-off losses of an SiC MOSFET in a step-less way. This is accomplished by utilizing auxiliary MOSFETs to provide charge to the gate of the primary SiC MOSFET. Depending on if the auxiliary MOSFETs are operated in the ohmic region or the saturation region, the turn-on and turn-off process of the primary MOSFET will differ. In the ohmic region, the auxiliary MOSFETs will act as resistors and the switching process of primary MOSFET will be similar to a CGD. On the other hand, if the auxiliary MOSFETs are operated in the saturation region, the switching process will be similar to a CSG.

The proposed gate driver and control scheme can be seen in Fig. 17. A power supply consisting of an isolated DC/DC module, a voltage regulator, a digital potentiometer and a Digital Signal Processor (DSP) provides the voltage determined by the control scheme to the auxiliary MOSFETs. The control scheme is based on measuring the junction temperature of the primary MOSFET and comparing it to a reference temperature. The calculated difference is used non-linear elements and the loss models to calculate the appropriate gate-source voltages for the auxiliary MOSFETs.

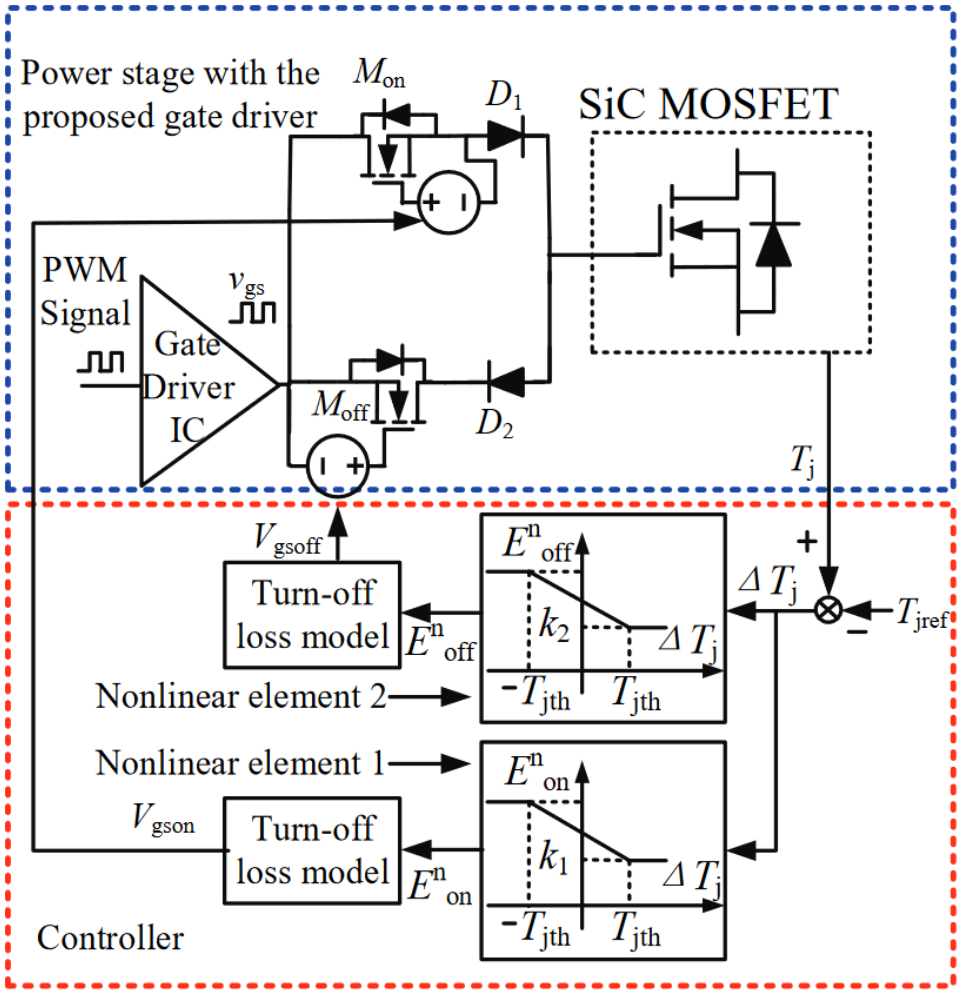



Figure 17: Gate driver concept and controller proposed in [64]. Screenshot from [64].

Two experiments were performed to verify the efficacy of the proposed AGD and the controller. First, a DPT was done to ensure that the loss models derived in [64] had satisfactory results on the measured losses. Second, to investigate the ATC capability of the proposed system, the AGD and the control scheme was tested within an experimental converter setup. When this experimental inverter was operated at a switching frequency of 10 kHz, the ratio between switching losses and total losses could be altered between 7.6 % and 12.3 %. At 20 kHz, this range was 14.2 % and 21.9 %. In the experimental set-up, the proposed ATC system was driving an open-packaged SiC MOSFET in a H-bridge. A change in the load current was induced with and without the ATC. The ATC system was able to reduce the temperature swing by 24.1 %. This reduction in the fluctuation of the junction temperature could increase the lifetime of the SiC MOSFET by 392 %, based on the lifetime model used in [64].

Seeing as a digital potentiometer is a digital component, utilizing this type in order to create step-less operation is not feasible. In digital components, every value must be discretized. Therefore, calling the gate driver presented in this paper step-less is not entirely correct. However, the gate driver is able to achieve ATC and increase device lifetime.

#### Controlled Shoot-through to achieve ATC

In the other three ATC-concepts introduced in this Master Thesis, controlling one or more circuit parameters has been the mechanism for achieving ATC. In [66], controlled shoot-through conditions are used to reduce temperature swings. The ATC-scheme presented in [66] is based on being used within a half-bridge circuit. In such a setting, one of the devices will be active, while the other device will

be free-wheeling. As the active device is carrying switching current and voltage, switching losses in the freewheeling device are almost zero. Over time, this difference in losses can lead to temperature swings.

To be able to cause controlled shoot-through faults, a AGD capable of creating three voltage levels are needed. In addition to the turn-on and turn-off voltage levels, a third level capable of driving the free-wheeling SiC MOSFET into the active region. Operation in this region entails large losses and it is these losses that are used to achieve ATC. As the shoot-through conditioon current travels along the leg of the half-bridge, the voltage and current waveforms of the load should not be distorted.

To verify the functionality of the proposed ATC-scheme, simulations and experiments were performed. Utilizing MATLAB/Simulink system simulations and SPICE based electrical simulations, for the same system parameters as the experiments, the ATC-scheme was shown to be able to keep the average power losses within 23 W to 25 W over a 20 ms. The half-bridge converter had a sinusoidal load pattern. Less fluctuations in the losses indicate a higher operating temperature, but lower temperature swings. Experiments and simulations were conducted under similar conditions and displayed good agreement. In the experiments it was also shown that the intentional shoot-through conditions had a negligible impact on the output voltage and output current.

By utilizing shoot-through faults instead of manipulating circuit parameters, the ATC concept should be able to operate more or less independent of the load current. The reliability of the control system of the AGDs in this system will be of the utmost importance as an uncontrolled shoot-through condition would destroy the SiC MOSFETs and the converter.

# 3 Four Level Voltage Active Gate Driver

In this chapter of the Master Thesis, the proposed AGD topology will be introduced. First, the $V_{GG}$ pattern intended to be produced by the AGD is introduced and described. Second, a schematic diagram of the proposed gate driver will be presented. This schematic diagram will show the components used to produce the intended gate voltage waveforms. Finally, the proposed AGD operating principle will be described in detail.

In the Specialization Report, the precursor to this Master Thesis, a literature review examining AGDs was presented. The goal of the literature review was to map existing literature regarding active gate driving of high power SiC MOSFETs [1]. Based on this literature review, an AGD concept was derived. This gate driver concept aims to control the switching losses and switching slopes of SiC power MOSFETs.

The AGD concept presented in this chapter of the Master Thesis is based on the gate driver concepts presented in [30] and [67]. However, the control system for the proposed AGD concept is different. How the control pules are applied to create the desired gate voltage pattern is also different from the gate driver concepts presented in [30] and [67]. Yang et al. introduced a gate driver concept where an intermediate voltage level is introduced at turn-on, and turn-off [30]. The timing of these two intermediate voltage levels can be controlled. Zhao et al. presented a gate driver topology where an intermediate voltage level during turn-off is introduced [67]. This intermediate voltage level can be altered both in duration and voltage amplitude. Initially, the AGD concept presented in this Master Thesis included a variable timing for the intermediate voltage levels, like in [30]. However, it was found that altering the timing and duration of the intermediate voltage levels had a similar impact on switching performance. Therefore, to simplify, the timing aspect was dropped from the simulation study and experimental performed in this Master Thesis.

## 3.1 Gate Voltage Pattern

The gate voltage pattern intended to be produced by the proposed AGD is shown in Fig. 18. The turn-on gate voltage pattern can be seen in Fig. 18a and can be divided into three time periods:

- **Before $t_1$:** $v_{GS} = V_{GG,off}$ as the gate driver is keeping its associated MOSFET turned off.
- **$t_1$ - $t_2$:** At $t_1$ $V_{GG}$ changes from $V_{GG,off}$ to the intermediate turn-on voltage ($v_{int,on}$).
- **After $t_2$:** At $t_2$ $V_{GG}$ changes from $v_{int,on}$ to $V_{GG,on}$.

For the turn-off switching event, the switching process is similar and can be seen in Fig. 18b. Instead of transitioning directly from $V_{GG,on}$ to $V_{GG,off}$, the intermediate voltage level occurs in-between.

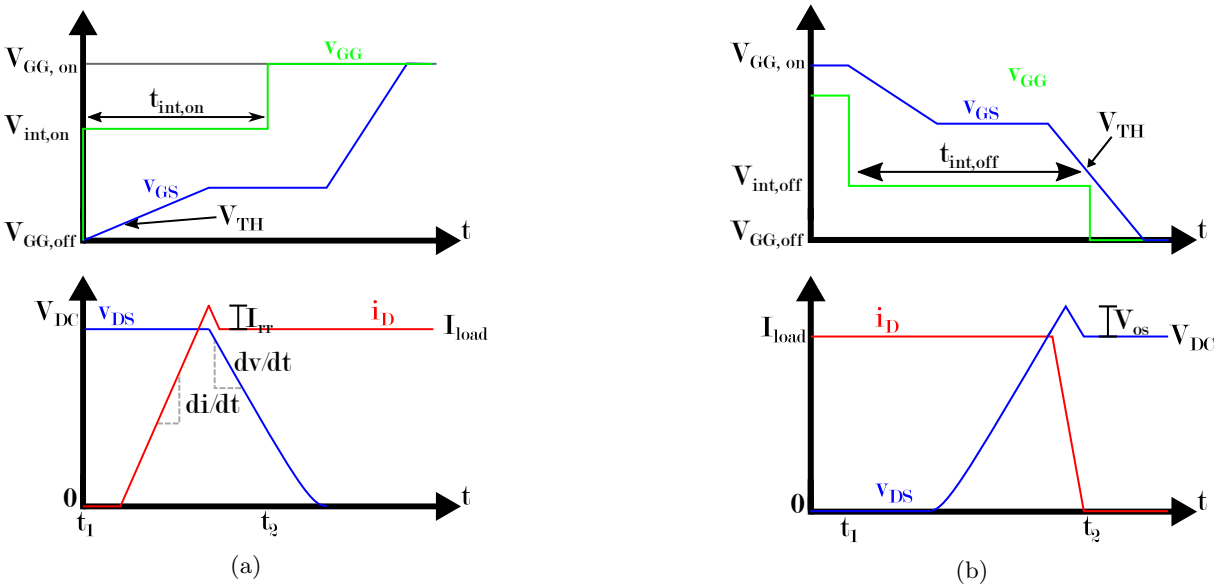



Figure 18: $V_{\mathrm{GG}}$ produced by the gate driver during turn-on (a) and turn-off (b)

Compared to the $V_{\mathrm{GG}}$ pattern produced by a conventional two level voltage gate driver like the one seen in Fig. 10, the introduction of controllable intermediate voltage levels introduces a degree of freedom regarding the gate charging/discharging process. The switching event can be slowed down by utilizing the intermediate voltage levels. Slowing down the switching transients leads to a slower voltage and/or current commutation, resulting in a lower voltage change rate (dv/dt) and current change rate (di/dt). If the switching process is slowed down, reverse recovery peak current ($I_{\mathrm{rr}}$) is reduced as the reverse recovery charge from the body diode of the FD has more time to be discharged. Similarly, voltage overshoot ($V_{\mathrm{os}}$) should also be reduced as $i_{\mathrm{D}}$ will fall slower. This will reduce the voltage drop across the parasitic inductances in the power loop. On the other hand, a slower voltage and current commutation will lead to higher switching losses due to a more extended time period with high $v_{\mathrm{DS}}$ and $i_{\mathrm{D}}$.

## 3.2 Proposed Active Gate Driver Schematic

In order to create the gate driver concept seen in Fig. 18a and 18b, a gate driver topology was created. A schematic of this gate driver topology can be seen in Fig. 19. The topology consists of two parts; the supply circuit and the AGD circuit. In order to provide the different voltage levels needed for $V_{\mathrm{GG,on}}$, $V_{\mathrm{GG,off}}$, $v_{\mathrm{int,on}}$ and intermediate turn-off voltage ($v_{\mathrm{int,off}}$), the supply circuit has an insulated DC-DC converter part. The insulated DC-DC converter consists of several interconnected DC-DC converters so that several voltage levels are accessible. The DC-DC converter transforms the power supply voltage into the voltage levels needed for the adjustable low dropout voltage regulators (LDOs). These can be seen in Fig. 19. Insulation between the voltage source and the adjustable LDOs as well as the AGD circuit is also provided by the DC-DC converter. $\mathrm{V}_H$ and $V_{\mathrm{GG,off}}$ are fed into three adjustable LDOs. These LDOs provides $V_{\mathrm{GG,on}}$, $v_{\mathrm{int,on}}$ and $v_{\mathrm{int,off}}$. The intermediate voltage levels are controlled in amplitude by changing the resistance in the feedback path of the adjustable LDOs and, thereby, its output voltage. $V_{\mathrm{GG,on}}$ can also be changed in amplitude, meaning that the proposed AGD can also influence the conduction losses of a MOSFET. However, this aspect of the gate driver is not investigated in this Master Thesis.

The AGD seen in Fig. 19 can realize the desired gate voltage pattern. Three half bridge units apply the voltage levels generated by the supply circuit to the gate. These half bridges consist of NMOSFETs. The duration of the intermediate voltage levels varies by controlling how long the different NMOSFETs are turned on and off. The control of the proposed AGD is performed by a control unit not seen in Fig. 19. The DUT circuit is included to illustrate how the AGD would connect to a MOSFET.

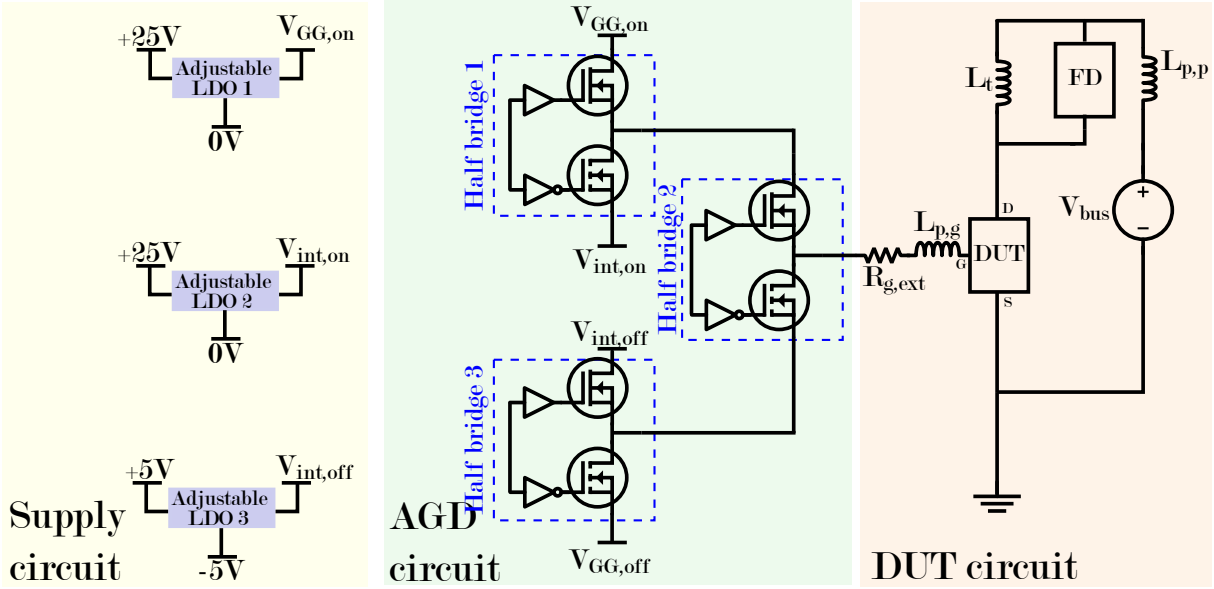



Figure 19: Schematic diagram of the proposed AGD

### 3.3 Operating Principle

As mentioned earlier, the goal of the proposed AGD is to control the switching losses and slopes of a SiC power MOSFET. These intermediate voltage levels are introduced during both the turn-on and turn-off event of the MOSFET. The intermediate voltage levels have an online-configurable amplitude between $V_{\mathrm{GG,on}}$ and $V_{\mathrm{GG,off}}$ and can be controlled in duration. Thereby, the charging/discharging of the power MOSFET gate can be controlled, influencing the switching devices' voltage and current commutation. Thereby, the switching losses are manipulated. Both the turn-off and turn-on intermediate voltage levels can be altered independently of each other. An application of the switching loss control is ATC of the power MOSFET. Using ATC, temperature fluctuations in power MOSFETs, occurring because of load current variation, can be partly compensated by increasing or decreasing the switching losses.

In order to turn a power MOSFET on or off, a certain amount of charge has to be supplied or removed from the gate of the MOSFET [68]. Fig. 20 illustrates this for a turn-on event of a power MOSFET. At $t_0$, $v_{GG}$ changes from $V_{\mathrm{GG,off}}$ to $V_{\mathrm{GG,on}}$. As $v_{\mathrm{GS}}$ begins to increase, $i_{\mathrm{G}}$ jumps from almost zero to its maximum value (this can be seen in Fig. 10a). From $t_0$ to $t_1$, the rising $v_{\mathrm{GS}}$ is caused by $C_{GD}$ and $C_{GS}$ being charged by $i_{\mathrm{G}}$. Parasitic capacitances in a MOSFET are $v_{\mathrm{DS}}$ dependent. In the $t_0$ - $t_1$ time period, $v_{\mathrm{DS}}$ is almost constant. Therefore, $C_{GD}$ and $C_{GS}$ have a negligible change in value. Since $C_{GS}$ >> $C_{GD}$, $i_{\mathrm{G}}$ mainly charges $C_{GS}$ From $t_1$ to $t_2$, the Miller plateau occurs. Here, $v_{\mathrm{DS}}$ falls, causing $C_{GD}$ to change in value. In Fig. 20, as mentioned in Chapter 2, it is assumed that the entirety of $i_{\mathrm{G}}$ flows into $C_{GD}$ during the Miller plateau. This causes $v_{\mathrm{GS}}$ to remain constant. All of $i_{\mathrm{G}}$ is required to support the change in voltage across $C_{GD}$. The Miller plateau ends when $v_{\mathrm{DS}}$ reaches its on-state value, causing $C_{GD}$ and $C_{GS}$ to stop changing in value. $t_2$ denotes the end of the Miller plateau in Fig. 20. Between $t_2$ and $t_3$, $v_{\mathrm{GS}}$ continues to rise. However, as $C_{GD}$ and $C_{GS}$ are much closer in value during this time period compared to $t_0$ to $t_1$. This causes the slope of $v_{\mathrm{GS}}$ to be different. In $t_0$ to $t_1$ the slope of $v_{\mathrm{GS}}$ is linear, while in $t_2$ to $t_3$ the slope of $v_{\mathrm{GS}}$ is exponential. At $t_3$, $v_{\mathrm{GS}}$ reaches $V_{\mathrm{GG,on}}$ and $i_{\mathrm{G}}$ drops to zero as the MOSFET is fully on. [68]

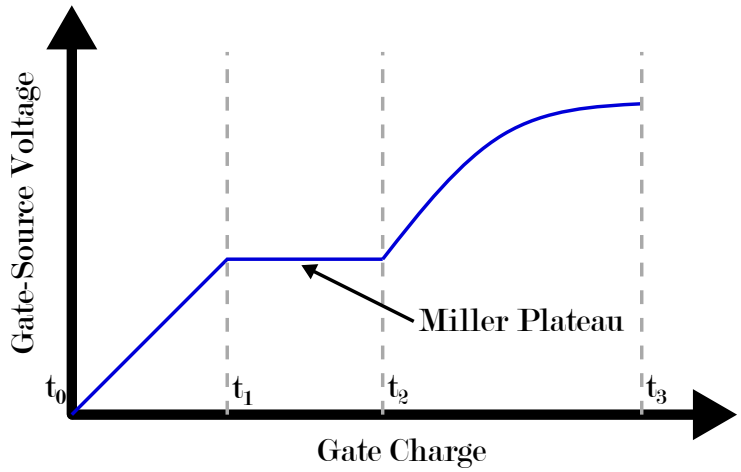



Figure 20: Exemplary plot showing the relationship between gate charge and gate-source voltage during turn-on. Based on [68]

In the proposed gate driver, External Gate Resistance ($R_{\mathrm{G,ext}}$) is a discrete component and thereby not online-adjustable. This results in the voltage amplitude of the intermediate voltage level being the mechanism for influencing the speed of which charge is being delivered/drawn from the gate. By changing the duration of the intermediate voltage levels, the duration of which $i_{\mathrm{G}}$ is altered can be influenced. The proposed AGD provides these two degrees of freedom manipulating power MOSFET switching performance.

How the AGD circuit presented in Fig. 19 translates to the voltage levels presented in Fig. 18 can be seen in Fig. 21, 22, 23 and 24. In order to produce the intermediate voltage level during turn-on, the lower NMOSFET in half bridge 1 and the upper NMOSFET in half bridge 2 are turned on. This is illustrated by Fig. 22a

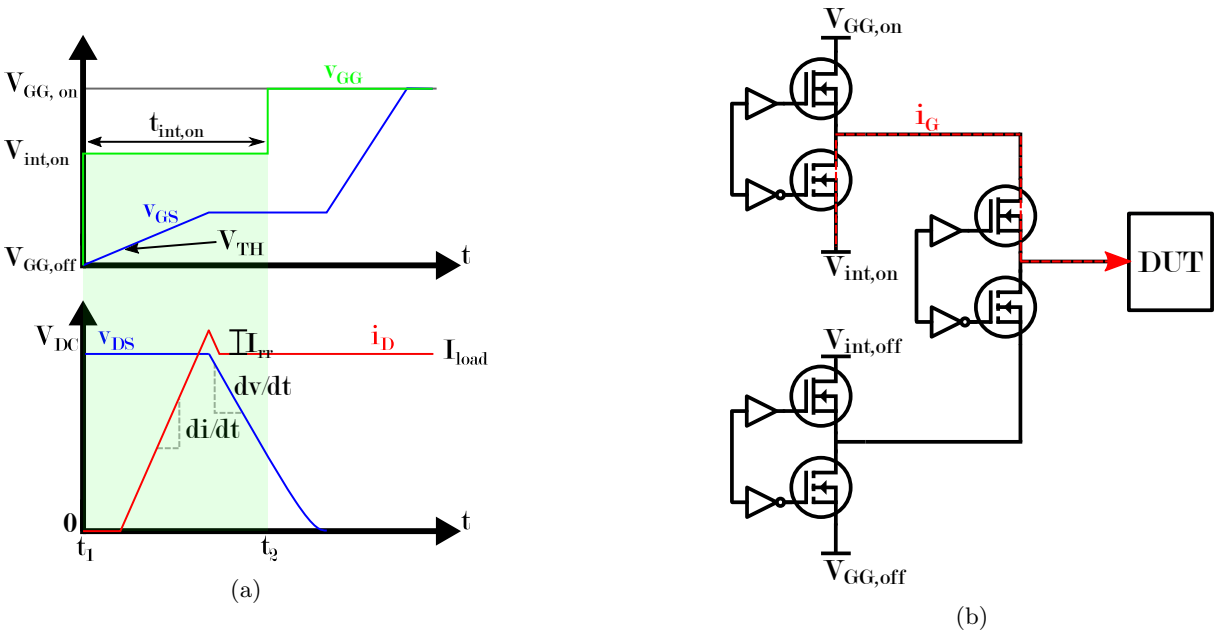



Figure 21: The $v_{\mathrm{int,on}}$ voltage level represented by waveforms (a) and gate current path (b)

The turn-on driving voltage level is supplied to the gate of the DUT, if the upper MOSFET in half-bridge 1 and the upper MOSFET in half-bridge 2 are conducting. This can be seen in Fig. 21a. As $V_{\mathrm{GG,on}} > \mathrm{V}_{int,on}$, the turn-on driving voltage level $V_{\mathrm{GG,on}}$ causes faster gate charging than the intermediate turn-on voltage level.

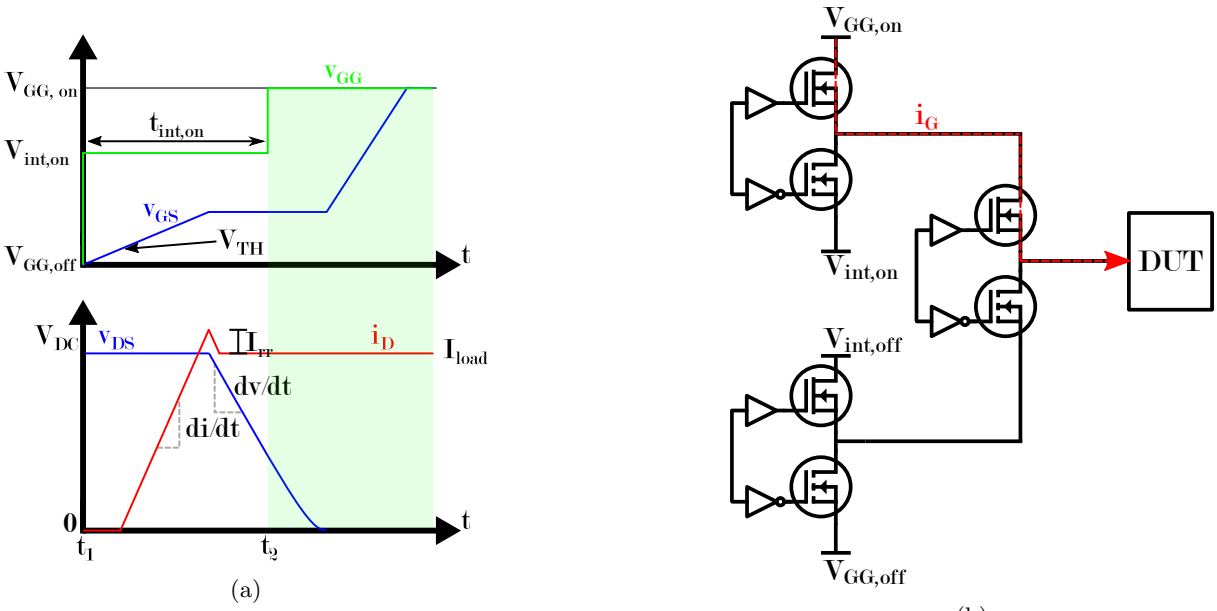



Figure 22: The $V_{GG,on}$ voltage level represented by waveforms (a) and gate current path (b)

To supply the intermediate turn-off voltage level to the gate of the DUT, the lower MOSFET in half bridge 2 and the upper MOSFET in half bridge 3 are conducting. This can be seen in Fig. 23a.

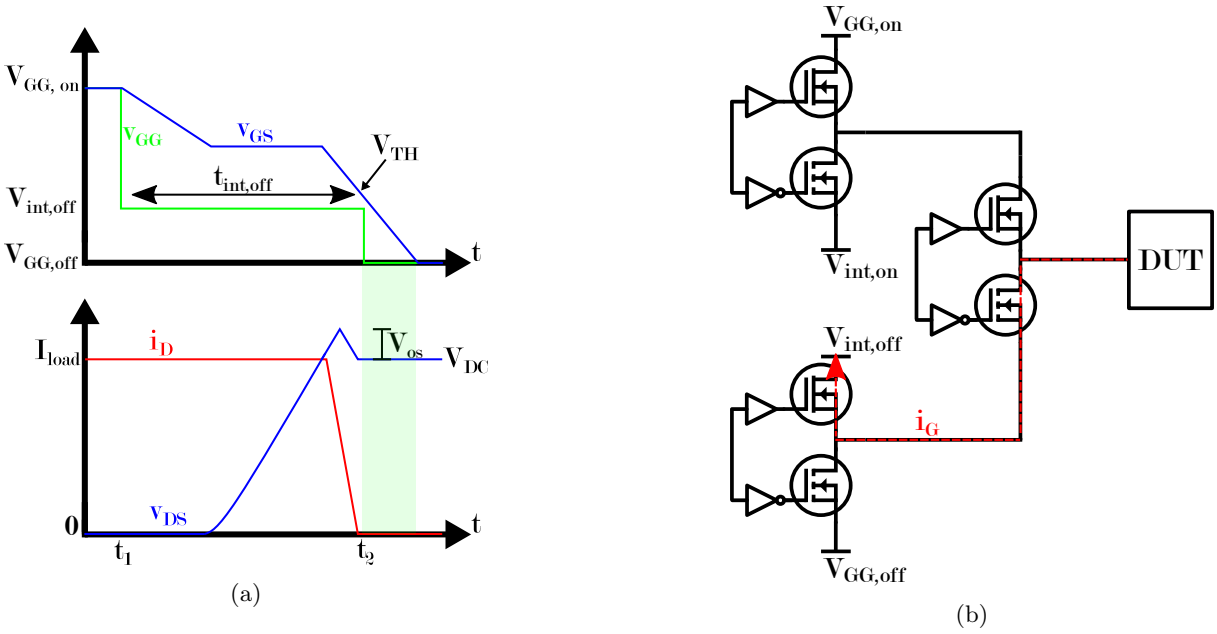



Figure 23: The $v_{\text{int,off}}$ voltage level represented by waveforms (a) and gate current path (b)

In order to supply the turn-off driving voltage level to the gate of the power MOSFET, the lower MOSFET in half bridge 2 and the lower NMOSFMOSFETET in half bridge 3 have to conduct.

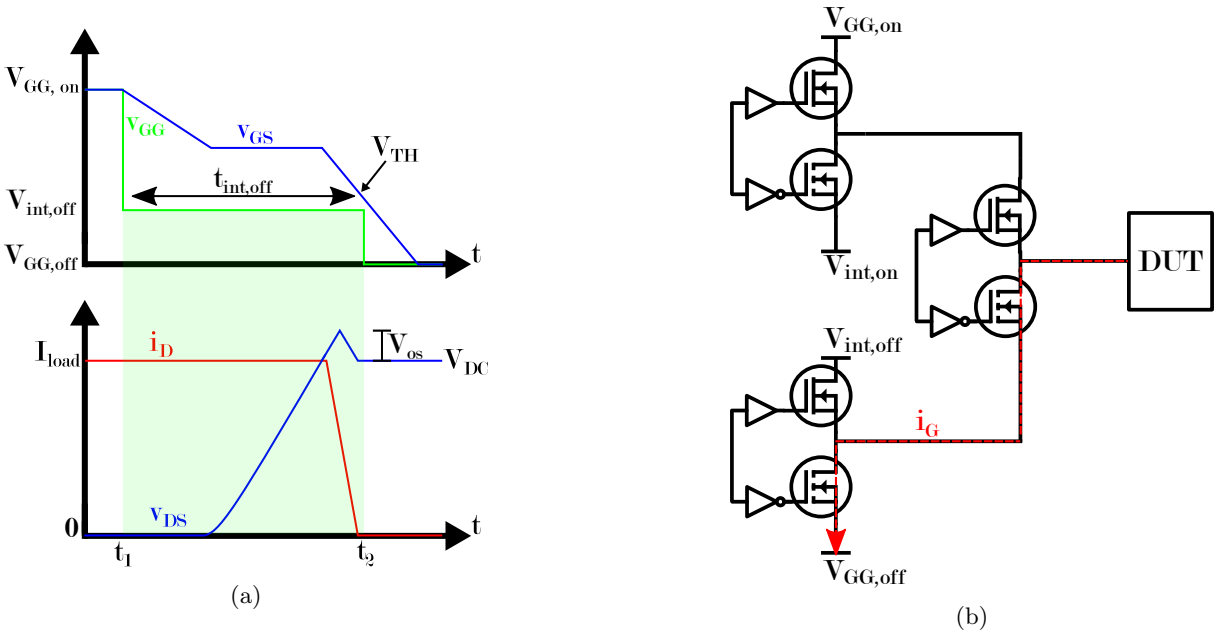



Figure 24: The $V_{GG,off}$ voltage level represented by waveforms (a) and gate current path (b)

# 4 Double Pulse Test Simulations

This chapter will present all the elements needed for the DPT simulations performed in this Master Thesis. First, the modelling of the DPT circuit in LTSpice is described and then, the MOSFET model used for the simulations is introduced. In the second part of this chapter, the implementation of the Python functionality used to perform and evaluate the simulations is introduced.

The evaluation functions used in this Master Thesis are the same as the functionality developed in [1]. Some minor improvements has been performed for this Master Thesis. All simulations performed and presented in this Master Thesis are new and not from the Specialization Project.

## 4.1 Double Pulse Tests

A DPT is a test performed to test and characterize the hard-switching turn-on and turn-off behavior of the DUT. In a DPT, the DUT is switched on and off for different operating conditions, such as drain current ($i_\mathrm{D}$) and device temperature. How the DUT will perform in different scenarios can be examined by varying these variables. A DPT setup has power switches in a half-bridge or a full-bridge setup. To control the current change rate (di/dt) during the magnetization phase of the DPT, a test inductor is included in the DPT setup. The magnetization phase is the time duration where the current in the DPT setup reaches the test current value. DPTs can be used to test DUT performance at different operating conditions such as, for example, rated current, rated voltage, or maximum device temperature. In addition, DPTs can be used to measure switching losses, switching time, crosstalk between DUT and FD, current and voltage overshoots as well as di/dt and dv/dt [69].

An exemplary waveform of the DUT drain current during a DPT can be seen in Fig. 25. The DPT is split into different phases: At $t_1$, the DPT is started by turning the DUT on, causing current to flow in the device. From $t_1$ - $t_2$ $i_\mathrm{D}$ increases linearly. The rise of the current is determined by the test inductor and the test voltage. The length of $t_1$ - $t_2$ depends on the desired test current ($I_\mathrm{test}$). This phase is known as the magnetization period. At $t_2$ the DUT is switched off. From $t_2$ - $t_3$, DUT is kept off. The duration of this time period depends on at what $i_\mathrm{D}$ the turn-on of the DUT should occur. This time period also has to have a minimum duration, known as the minimum hold-off time, to ensure that the turn-off of the DUT has been completed before the turn-on occurs. Otherwise, a shoot-through fault can occur. At $t_3$ DUT is switched on and kept on until $t_4$. In order to end the DPT, the DUT is switched off, and the inductor energy is dissipated using a discharge resistor not shown in Fig. 26. [70].

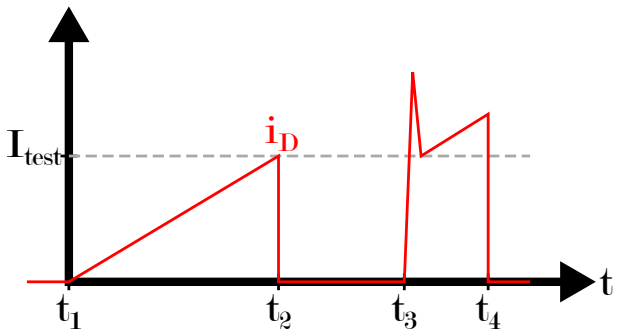



Figure 25: Exemplary $i_\mathrm{D}$ waveform during a DPT. Based on [69]

## 4.2 Idealized Double Pulse Test Circuit

A dedicated circuit is needed to perform DPTs. DPT circuits can consist of power semiconductor devices in either a half bridge or full bridge configuration [69, 70]. Fig. 26 shows a DPT circuit in a half bridge configuration. In parallel to the upper device, a test inductor ($L_t$) is connected. This inductor limits the di/dt during the magnetization phase [70]. $V_{DC}$ energizes the circuit. The upper device in the half-bridge is the FD, while the lower device is the DUT. In this DPT circuit schematic, parasitic inductances,

capacitances, and the external gate resistance are not shown. The upper device has a constant $v_{GS} = V_{GG,off}$ in order to ensure that the FD is freewheeling. On the other hand, the DUT is connected to a gate driver which keeps the DUT turned on for the $t_1$ - $t_2$ and $t_3$ - $t_4$ time intervals seen in Fig. 25. During $t_1$ - $t_2$, the current circulating in the circuit is equal to what is marked in Fig. 26a. For $t_2$ - $t_3$, the DUT is turned-off and current is circulating in the closed loop formed by the FD and $L_t$. This is shown in Fig. 26b. When going from the current flow seen in Fig. 26a to the current flow seen in Fig. 26b, there will be a time period where both $i_1$ and $i_2$ will be flowing like the current commutates. At $t_3$, the DUT starts to conduct current again. During $t_3$ - $t_4$, the two currents ($I_1$ and $I_2$ in Fig. 26) are superimposed on each other. $I_2$ is created by the reverse recovery charge in the FD having to be discharged [70]. $I_2$ is not present during the entire $t_3$ - $t_4$. After the reverse recovery charge has been discharged, $i_1$ will be the only current flowing through the DUT.

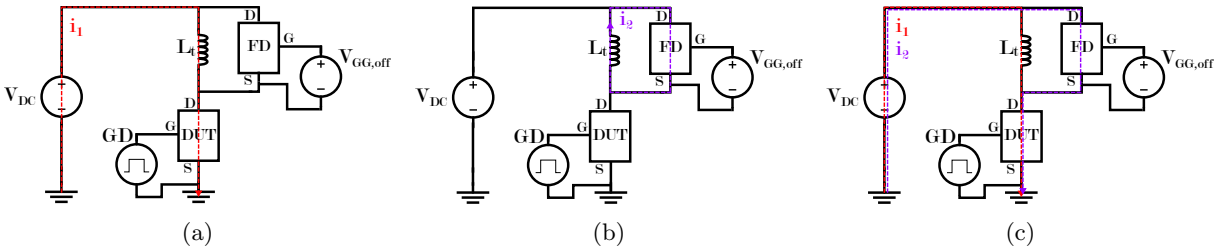



Figure 26: Exemplary half bridge double pulse test circuit schematic. Path of current(s) for $t_1$ - $t_2$ (a), $t_2$ - $t_3$ (b) and $t_3$ - $t_4$ (c). Based on [70]

## 4.3 Modelling of the Double Pulse Test Circuit

In order to examine the impact of the proposed AGD, a DPT model was created in LTSpice. The model consists of two parts: A DPT circuit model and a MOSFET model.

### DPT Circuit in LTSpice

The DPT circuit was modelled in LTSpice, which is a SPICE software from Analog Devices [71]. A screenshot of the DPT circuit that was implemented in LTSpice can be seen in Fig. 27. The DPT circuit consist of two MOSFETs in a half bridge setup. The upper MOSFET (U2) is connected in parallel to a test inductor. To energize the circuit, an ideal voltage source was used. In the model, the values of the different components are defined by variables, which can be seen enclosed in curly brackets in Fig. 27. Table 1 contains the identifier, a short description and the name of the variable that contains the component value.

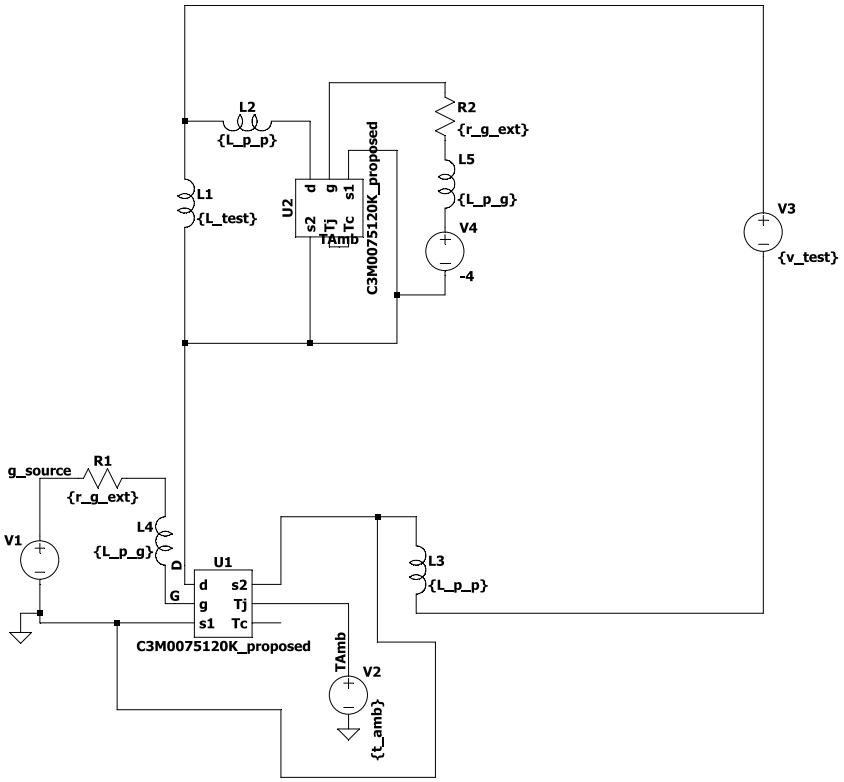



Figure 27: Screenshot of the LTSpice DPT circuit. Based on [23].

Table 1: Descriptions and parameters for the components in Fig. 27.

| **Component** | **Parameter** | **Description** |
|---|---|---|
| V1 | | Voltage source representing gate driver controlling DUT |
| V2 | t_amb | Sets the junction temperature of the DUT |
| V3 | v_test | Bus voltage |
| V4 | | Constant value of $-4\,\mathrm{V}$. Based on [23]. |
| U1 | | DUT |
| U2 | | Used as freewheeling device |
| R1 | r_g_ext | External gate resistance of DUT |
| R2 | r_g_ext | External gate resistance of freewheeling device |
| L1 | L_test | Inductive load being switched |
| L2 | L_p_p | Parasitic inductance in the upper part of the power loop |
| L3 | L_p_p | Parasitic inductance in the lower part of the power loop |
| L4 | L_p_g | Parasitic inductance in the upper gate driver |
| L5 | L_p_g | Parasitic inductance in the lower gate driver |

### MOSFET Models

For the simulations performed in this Master Thesis, a SPICE model for the 1.2 kV, 30 A C3M0075120K SiC Power MOSFET from Wolfspeed is used [23]. SPICE models for the devices offered by Wolfspeed can be found on their website [72]. However, the SPICE model provided by Wolfspeed has caused convergence issues when used in LTSpice simulations. This was caused by a discontinuous behavior in $i_\mathrm{D}$ at specific $v_\mathrm{GS}$ values, which caused issues in the transconductance of the SiC MOSFET model [22]. The manufacturer model of the SiC MOSFET was therefore improved to remedy this issue [22]. In this Master Thesis, three versions of the C3M0075120K SiC Power MOSFET model were used for the simulations. The first one is the model version presented that was [22]. The second version was based on utilizing a parameter fitting method for modelling static SiC Power MOSFETs presented in [73]. This fitting method was applied to

the first model to create the second model. The third version was based on the second version. However, parameters within the MOSFET model were manually altered to achieve switching performance closer to the performance seen in the experimental results. In the result chapter (Chapter 6), the first MOSFET model version will be referred to as the "original MOSFET model". The second model will be named the "fitted MOSFET model" and the third model will be referred to as the "manually altered MOSFET model".

Three different models for the SiC MOSFET were used in this Master Thesis for the simulation study to be as accurate as possible compared to the experimental results.

## 4.4 Gate Driver Concept Implementation

The proposed AGD concept presented in Chapter 3 uses a controllable ideal voltage source. This voltage source can be seen as component V1 in Fig. 27. In LTSpice, ideal voltage sources can provide an arbitrary time-dependent output. The voltage output can be defined using a look-up table format, where input data is provided as a list of time and voltage values [74]. Utilizing the piece-wise linear (PWL) function, the $v_{GG}$ patterns equal to those seen in Fig. 18a and 18b were created.

An exemplary $v_{GG}$ waveform can be seen in Fig. 28. In this example, the gate voltage pattern consists of ten time-voltage pairs. In Fig. 28, the turn-off intermediate voltage would be defined by the voltage value of points 3 and 4 and the duration between these two points.

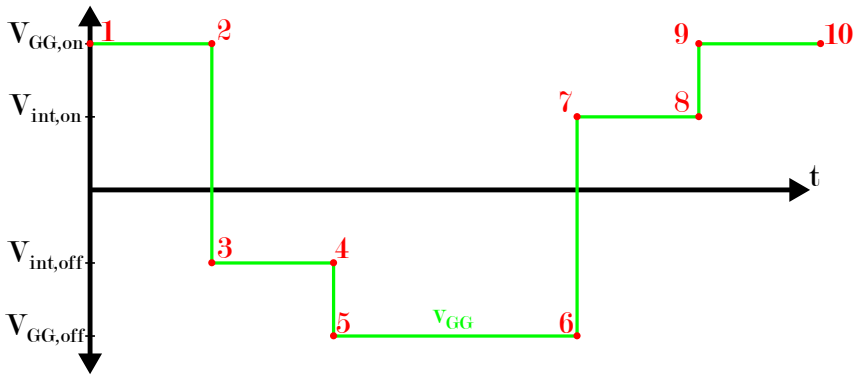



Figure 28: Example gate voltage waveform illustrating the PWL data approach

## 4.5 Double Pulse Test Simulation Sweeps and Evaluation Functionality

The proposed AGD concept allows altering the voltage amplitude and duration of an intermediate voltage level at turn-on and at turn-off. To investigate the impact of these two aspects, simulation sweeps were performed. Simulation sweeps consist of performing multiple simulations in a row. For each simulation, one of the sweeped variables changes value. In this Master Thesis, the simulation sweeps were performed changing two parameters: The intermediate voltage level amplitude and the intermediate voltage level duration. Based on the parameter values, PWL data for every possible combination of the entries in the two lists were created. For example, if both the voltage amplitude list and the duration list have 20 entries each, 400 simulations will be performed for that simulation sweep. For every combination, a DPT was simulated in LTSpice, and the waveform data from each simulation was saved. Using PyLTSpice, a library for Python [75], the simulation sweep process could be controlled using an integrated development environment (IDE) running Python. PyLTSpice enables LTSpice circuits to be configured and altered, as well as simulations to be initialized directly in Python [75]. The simulations are performed in LTSpice, but PyLTSpice enables LTSpice to be controlled through Python.

In order to investigate the efficacy of the proposed AGD, the simulation data had to be evaluated. Evaluation functions were implemented using Python. As DPTs are used to test a DUT during turn-on and turn-off, defining when the switching event occurs is crucial. In this Master Thesis, the turn-on and turn-off switching events are defined based on switching edges defined by $i_{\mathrm{D}}$ and $v_{\mathrm{DS}}$. This Master Thesis

utilizes the definition of switching edges presented in the C3M0075120K Silicon Carbide power MOSFET datasheet [23]. The turn-on event of the DUT consists of a current rise and a voltage fall. The current rise starts when $i_{\mathrm{D}} > 0.1 \cdot \mathrm{I}_{load}$ and ends when $i_{\mathrm{D}} < 0.9 \cdot \mathrm{I}_{load}$ The turn-off event of the DUT consists of a current fall and a voltage rise. The voltage rise starts when $v_{\mathrm{DS}} > 0.1 \cdot \mathrm{V}_{DC}$ and ends when $v_{\mathrm{DS}} < 0.9 \cdot \mathrm{V}_{DC}$. The turn-on event is the time interval from where the current rise begins to where the voltage fall ends. The turn-off event is the time interval when the current fall starts, and the voltage rise ends. Utilizing the Python function determining the switching transition, data corresponding to the turn-on and turn-off events could be extracted and further evaluated. Fig. 29 illustrates the switching time definition. In this figure, the points where the $i_{\mathrm{D}}$ and $v_{\mathrm{DS}}$ are within the definition described earlier are marked with green dots. Based on this definition of a switching event, the turn-on event in Fig. 29 occurs within the time period between the two lower green dots.

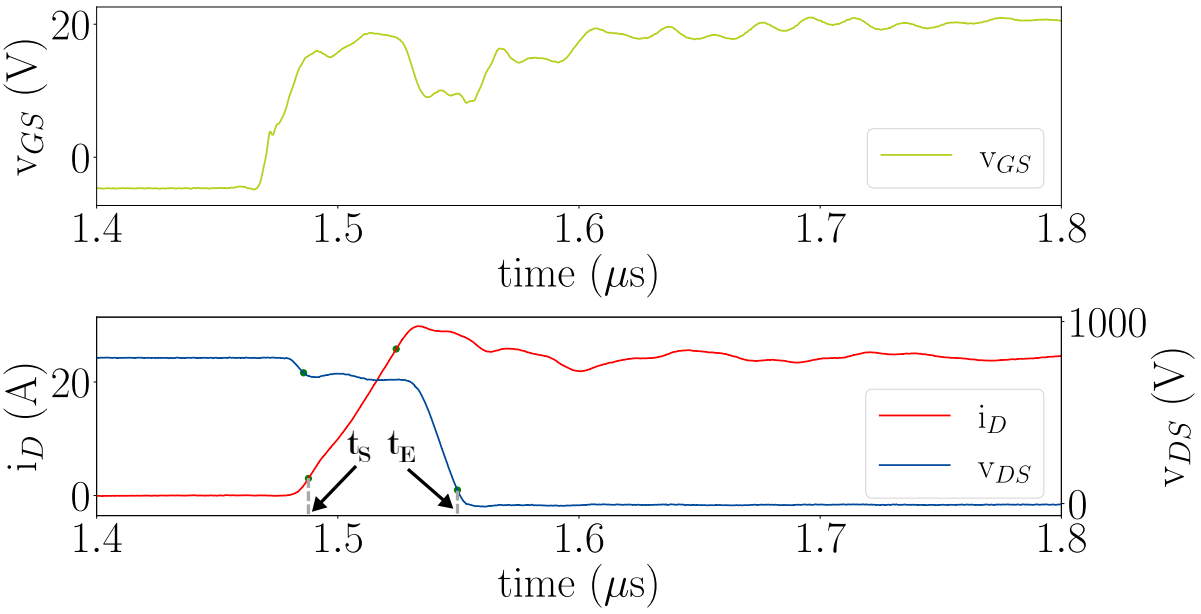



Figure 29: Exemplary drain current, drain-source voltage and gate-source voltage waveforms during a turn-on event.

To determine switching losses, the instantaneous power loss that occurs for each time step during the switching transient is calculated. The instantaneous power loss is integrated over the time duration, which defines the switching transient, yielding the average switching energy. Using the switching duration definition presented earlier, an example of how a turn-on event is defined can be seen in Fig. 11. Since a DPT only consists of two turn-on and turn-off events, the average turn-on and turn-off switching energy can be calculated from a single DPT. $I_{\mathrm{rr}}$ is calculated by subtracting the test current ($\mathrm{I}_{test}$) from the maximum value of $i_{\mathrm{D}}$ during the turn-on event. This definition of $I_{\mathrm{rr}}$ can be seen in Fig. 18a Similarly, $V_{\mathrm{os}}$ is calculated by taking the difference between DC-link voltage ($\mathrm{D}_{DC}$) and the maximum $v_{\mathrm{DS}}$ value during turn-off. The maximum di/dt and dv/dt is determined by calculating the differential between every value of $i_{\mathrm{D}}$, $v_{\mathrm{DS}}$ and their corresponding time value. Since the peak values define the stress on both the circuit and the switching device caused by di/dt and dv/dt, these values are presented in this Master Thesis. During turn-on, the maximum di/dt and minimum dv/dt are recorded. At turn-off, it is the minimum di/dt and maximum dv/dt that are recorded.

# 5 Double Pulse Test Experiments

This chapter will introduce the design and assembly process necessary for producing a PCB capable of implementing the proposed AGD concept. The gate driver control software and python functions used for experimental result processing and evaluation will also be introduced. In addition, the test setup used to perform DPTs with the AGD PCB prototype will be detailed [76].

## 5.1 Printed Circuit Board design

To design the PCB used in the experiments performed in this Master Thesis, the PCB design software Altium Designer [77] was used. A PCB for testing the efficacy of the proposed AGD on SiC MOSFET modules was also designed. However, due to time constraints and long production delays, this PCB was only designed and ordered, but it could neither be assembled nor tested yet.

#### Design and Assembly of Proposed Active Gate Driver Prototype

The PCB that can be seen in Fig. 30, shows the prototype of the proposed AGD. The PCB was designed to produce the gate voltage pattern presented in Chapter 3. The AGD PCB consists of three parts: The power board (marked in red), the adjustable LDOs (marked in green) and the gate driver board (marked in blue). The GD board will be introduced in greater detail later in this chapter.

The power board has several PEM2-S24-D5-S and PEM2-S24-D15-S DC-DC converters from CUI Inc mounted on it [78]. The input voltage to the power board is supplied by an external power supply. By combining the output voltages of the DC-DC converters, the voltage levels needed for the operation of the AGD are provided.

The adjustable LDOs consists of two parts: the adjustable LDOs itself and a digital potentiometer. An adjustable LDOs transforms its input voltage into another, lower voltage level at the output. The output voltage level can be adjusted by varying the value of a resistor connected between the adjustment pin and the reference of the LDO. By utilizing the digital potentiometer, the output voltage of the adjustable LDOs can be changed digitally. This is achieved by the digital potentiometer altering the voltage seen by the LDO between the adjustment pin and the reference of the LDO. As there is constant voltage difference between the adjustment and output pin, altering the voltage between adjustment pin and the LDO reference alters the output voltage of the LDO. The adjustable LDOs used in the PCB is the LM317 from Texas Instruments [79]. The digital potentiometer consists of several parts. A series connection of resistors form is arranged so that the connection points of the resistors are accessible. Low power BJTs are used to shorten these connection points to the reference voltage. Depending on the BJT that is both located furthest from the reference voltage and activated, the total resistance of the arrangement is determined. This potentiometer is controlled by signals provided by the control unit of the AGD (not seen in Fig. 30). In order to isolate the control unit, digital isolators are used. Connected to these digital isolators are I/O extenders. The I/O extenders take inputs from the control unit and translate them into high or low base input voltages of the BJTs. In the PCB, BC817UPN BJTs [80] are used. MAX7317 digital isolators [81] provide galvanic isolation and signal transfer. The I/O extenders are MAX22444CAWE+ from Maxim Integrated [82].

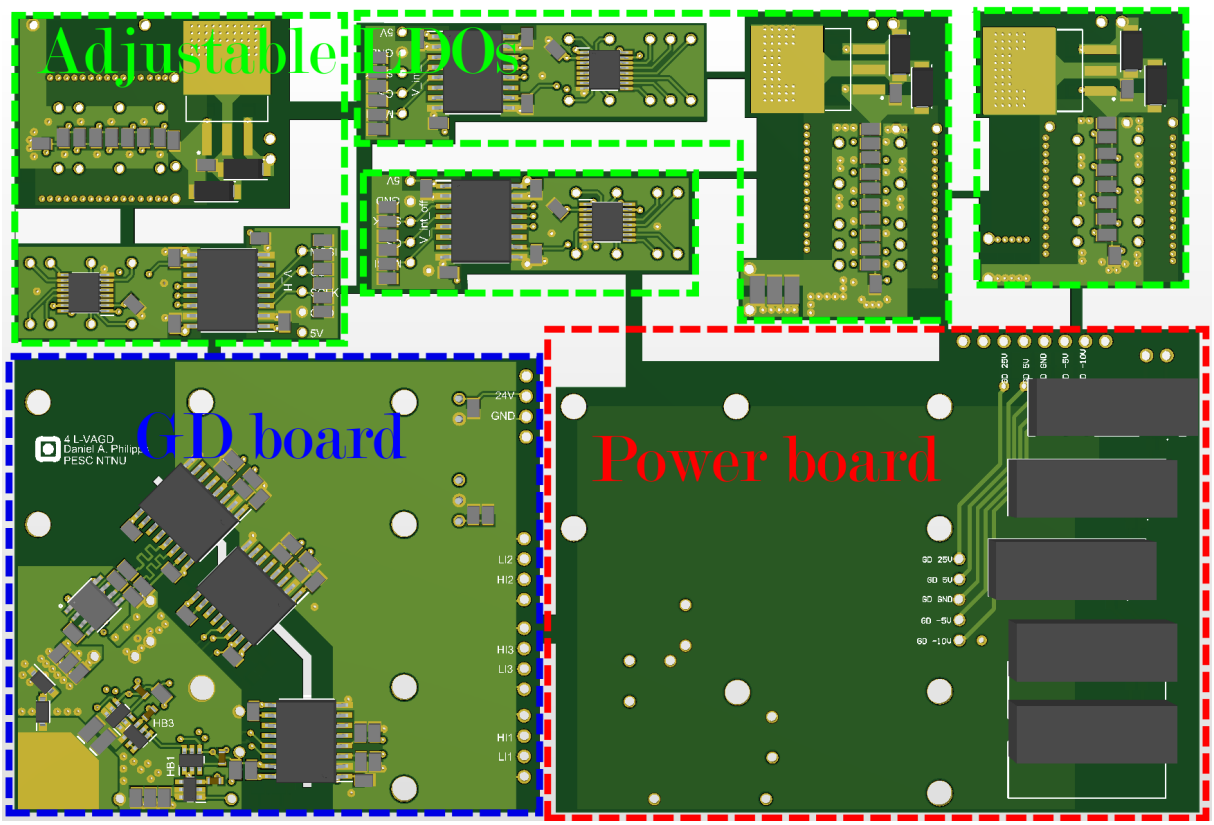



Figure 30: Picture from Altium Designer of the proposed gate driver prototype

### MOSFET Module Interface Design

In order to facilitate testing of the proposed AGD on SiC MOSFET modules, a PCB was created. This PCB can be seen in Fig. 31 and consists of the following elements:

- **MOSFET module:** The position where the SiC MOSFET module is attached to the PCB. This position of the MOSFET module is marked in red in Fig. 31.
- **Input voltage:** The input voltage to the module interface PCB is supplied at the point marked in black on Fig. 31.
- **Buffer capacitor:** Several buffer capacitors will be placed on the PCB, between the MOSFET module and the input voltage. The location of the buffer capacitors are marked in green on Fig. 31. Buffer capacitors serve as storage for the energy supplied/withdrawn to/from the gate at turn-on/turn-off.
- **Discharge resistor:** To dissipate the energy stored in the PCB after the experiment is completed, a discharge resistor is included in the PCB design.

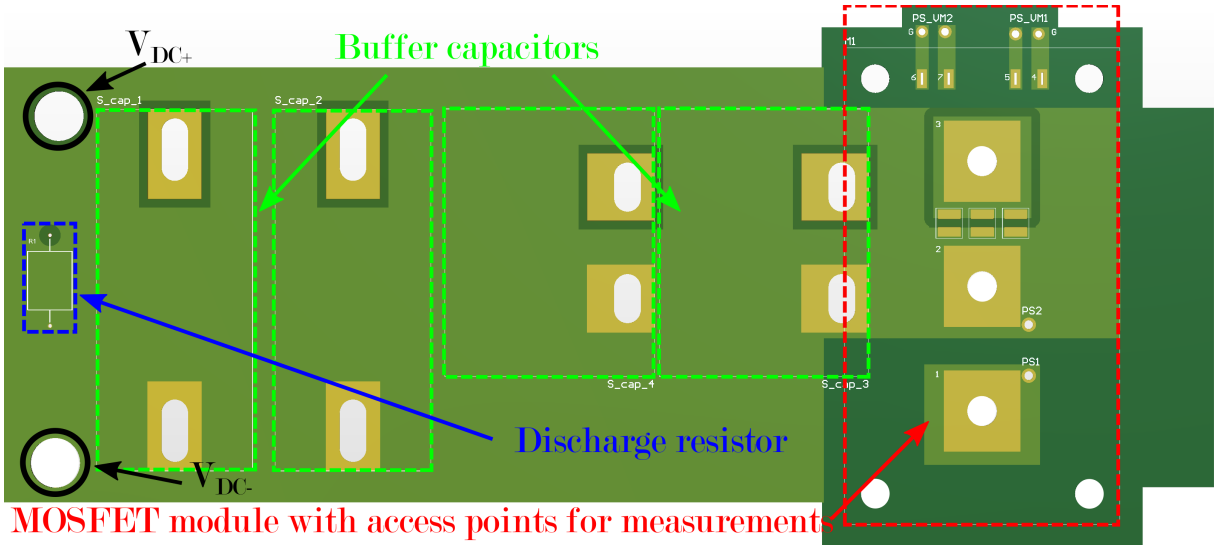



Figure 31: MOSFET module interface PCB design (3D view from Altium Designer)

A 1 MΩ axial resistor will be used as discharge resistor Capacitors of various sizes and technologies, such as ceramics, film and can capacitors, will be used as buffers capacitors. In order to mount the AGD PCB to the DUT test platform, so that AGD can be connected between the gate and source of the DUT, a mount fixture was designed and 3D printed. The design of the fixture was done in FreeCAD, a free computer aided design (CAD) software [83]. All the components was soldered onto PCBs in order to produce the finalized AGD prototype. The soldering work was performed in the power electronics laboratory at NTNU.

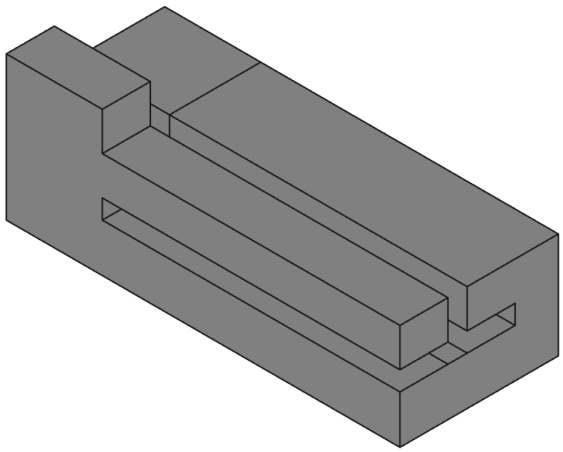


Figure 32: Screenshot from FreeCAD showing the fixture created to mount the AGD PCB to the device under test platform

## 5.2 Presentation of Active Gate Driver Prototype

The finalized AGD prototype can be seen in Fig. 33. The three half bridges seen Fig. 19 can be seen in Fig. 33. The adjustable LDOs and the power board is located behind the GD board. In order to provide insulation between the power part and the signal part of the GD board, an insulation barrier consisting of three digital isolators are used. The digital isolator used are the MAX22446 from Maxim Integrated. These are marked in red in Fig. 33. The three half bridges controlling which voltage level is supplied to the gate of the DUT are marked in yellow, while the external gate resistor is marked in Blue. The gate driver half bridges consists of the LM25101 half bridge gate driver from Texas Instruments [84] and

ZXMN10B08E6 MOSFETs from Diodes Incorporated [85]. Using the gate pad, marked in green, and the source pad, which is located behind the gate pad, the AGD prototype can be connected to the gate and source of the DUT.

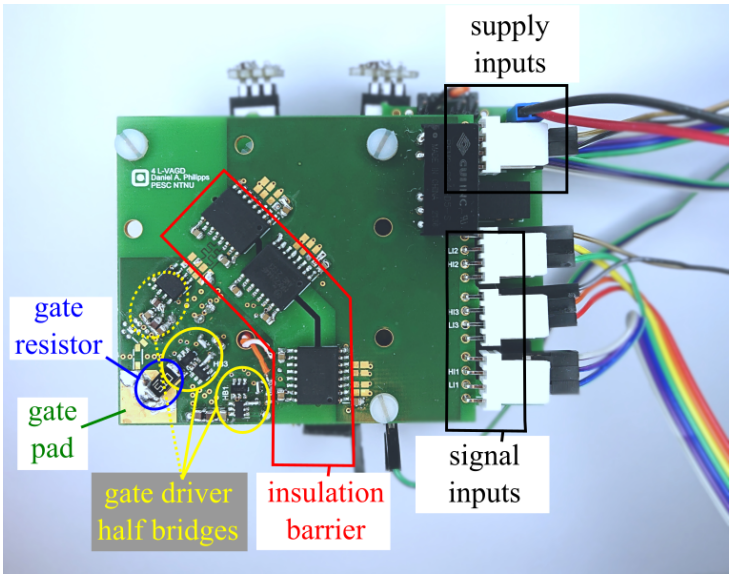



Figure 33: Photo of proposed AGD. Source pad is not seen in the photo. It is located behind the gate pad. Figure is from [76]

## 5.3 Presentation of Gate Driver Control Software

In order to verify the functionality of the AGD prototype, control software for the gate driver was needed. In this Master Thesis, existing gate driver control software developed at the power electronics laboratory at NTNU was used for the experimental DPTs.

## 5.4 Implementation of Experimental Result Processing and Evaluation

The data generated in the experimental DPTs has to be processed and evaluated to produce comparable results from the simulations. Compared to the simulation results, the experimental data has noise. In order to mitigate the impact of noise, several DPTs were performed under the same operating conditions. The results from these DPTs were averaged by the oscilloscope to produce the experimental data that was processed further and used for the generation of the experimental results presented in Chapter 6 This caused the functionality developed for the simulation study evaluation to define the switching times incorrectly. Initially, a Gaussian filter from the SciPy library in Python was implemented to smooth the experimental data [86]. However, this was dropped from the processing functionality to avoid information loss. Instead, the function used to determine when the switching event occurred for the simulation study was altered to avoid noise impacting the definition of the switching transients.

After the switching event time duration was determined, the same functions used in the simulation study were used to evaluate the experimental data.

## 5.5 Presentation of Test Setup

In order to test the proposed AGD prototype, a test setup was created. The test setup was presented in [87, 88] and consists of three parts. The first part is a DUT platform where the DUT, the AGD prototype and the FD is connected. The DUT platform connects to the rest of the test setup. The second part of the test setup is a balancing circuit, which is connected between the DUT platform and the power supply. The third part is the power supply itself.

### Device Under Test Platform

In order to perform DPTs where useful measurements are performed, several aspects should be taken into account. Parasitic inductance in the power loop should be minimized, as this inductance can cause large oscillations and overshoots in current and voltage. This distorts the voltage and current signals and causes the results not to represent the behavior of the DUTs. The location of the probing points, the places where measurements are performed, are also crucial to ensure measurement quality. A sufficient amount of capacitance is also required. These buffers capacitors should consist of different materials and be placed as close to the DUT. The buffering capacitance stores energy needed for the switching transient in the DUT. These capacitances also provide filtering. [88]

In this Master Thesis a low inductive DUT platform presented in [88] is used. This platform takes the aspects presented earlier into account. A picture of the DUT platform PCB can be seen in Fig. 34. A modified version of this DUT platform is used in this Master Thesis.

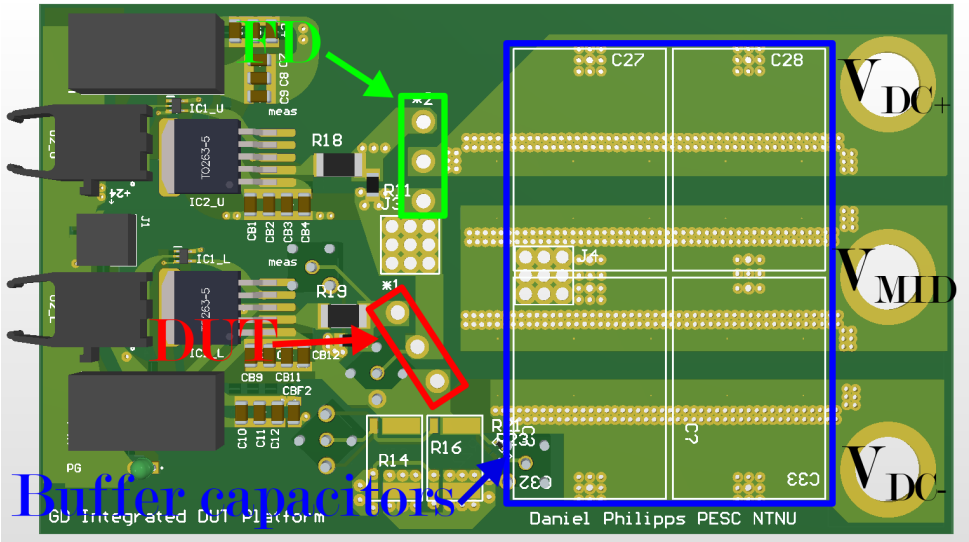



Figure 34: Screenshot of the low inductive DUT platform used for the DPTs. The platform is presented in [88]

To connect the AGD prototype to the gate and source pins of the DUT, the fixture introduced earlier in this Chapter was used. This can be seen in Fig. 35.

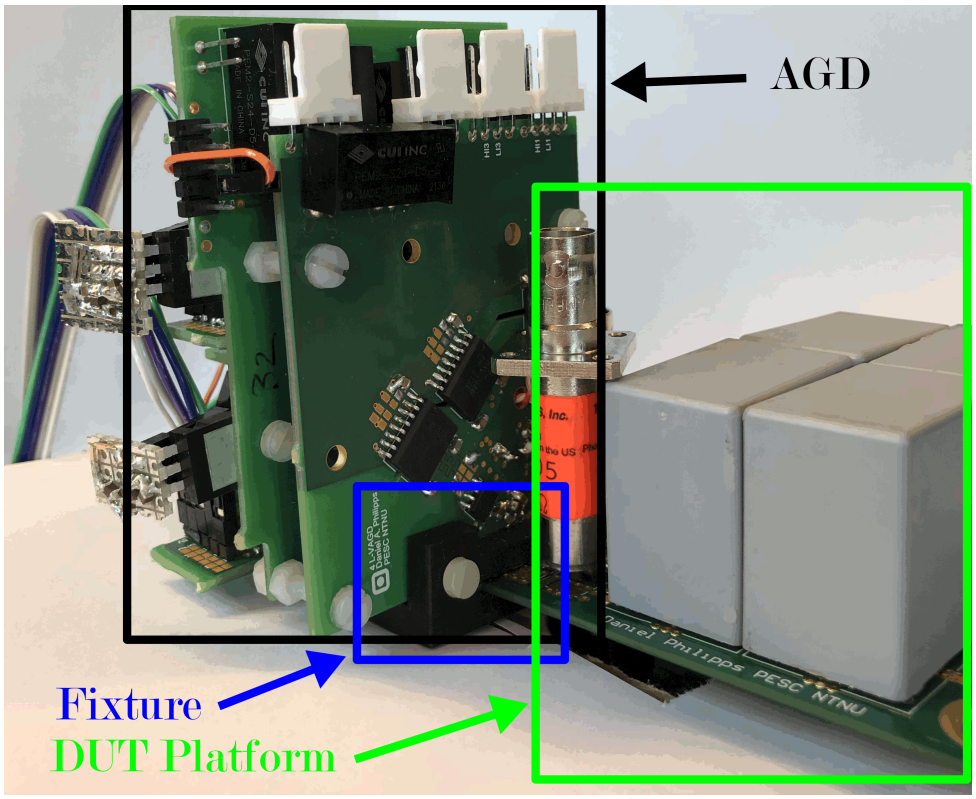



Figure 35: Photo showing the DUT platform and the AGD prototype being interfaced by using the fixture

### Balancing Circuit, Test Inductor and Power supply

A schematic of the total test setup can be seen in Fig. 36. The DUT platform corresponds to $S_1$ and $S_2$ in Fig. 36. This test setup was presented in [87]. The goal of the test setup is to facilitate DPTs where the measurements are of good quality so that they represent the actual performance of the DUT. To achieve this, several components are included in the test setup. $C_{buffer}$, $C_1$ and $C_2$ serve to stabilize the voltage from the power source. The capacitors also store energy, so sufficient energy is available during the switching transients of the DUT. The balancing circuit, consisting of two SiC MOSFET module in a half bridge configuration, balance the charge between $C_1$ and $C_2$. This ensures that the test inductor and the DUT have a positive average current during their operation. The inductor limits the current rise and helps to reduce the losses in the circuit to only include losses in the DUT, FD as well the parasitic losses in the inductor [87].

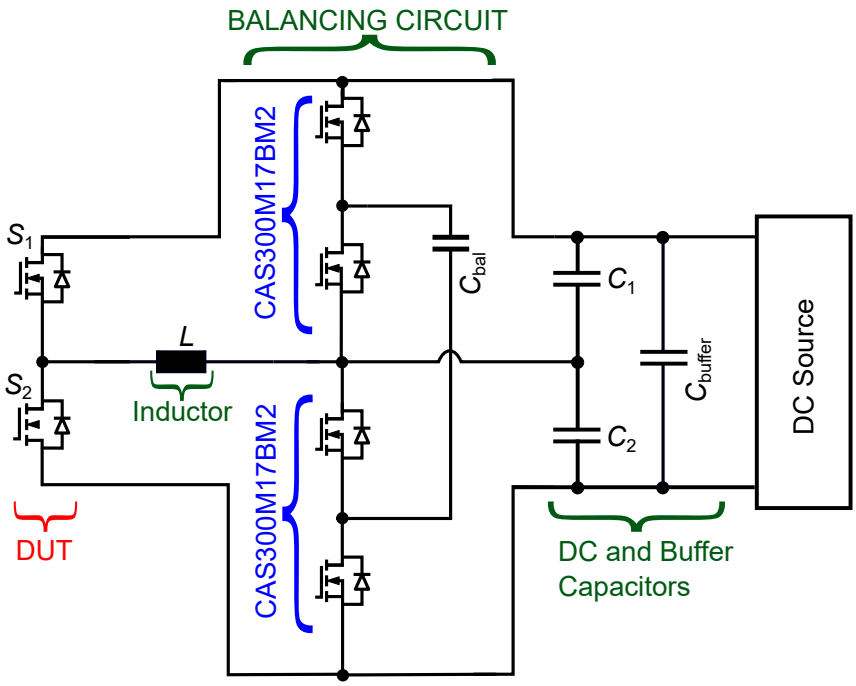



Figure 36: Schematic of the test setup used for the experiments performed in this Master Thesis. Schematic is from [87]

Fig. 37 shows a photo of the test setup. For the experiments performed in this Master Thesis, the part marked with DUT in Fig. 37 is exchanged for the DUT platform and the AGD prototype. The balancing circuit is controlled by a microcontroller which can be seen in Fig. 37.

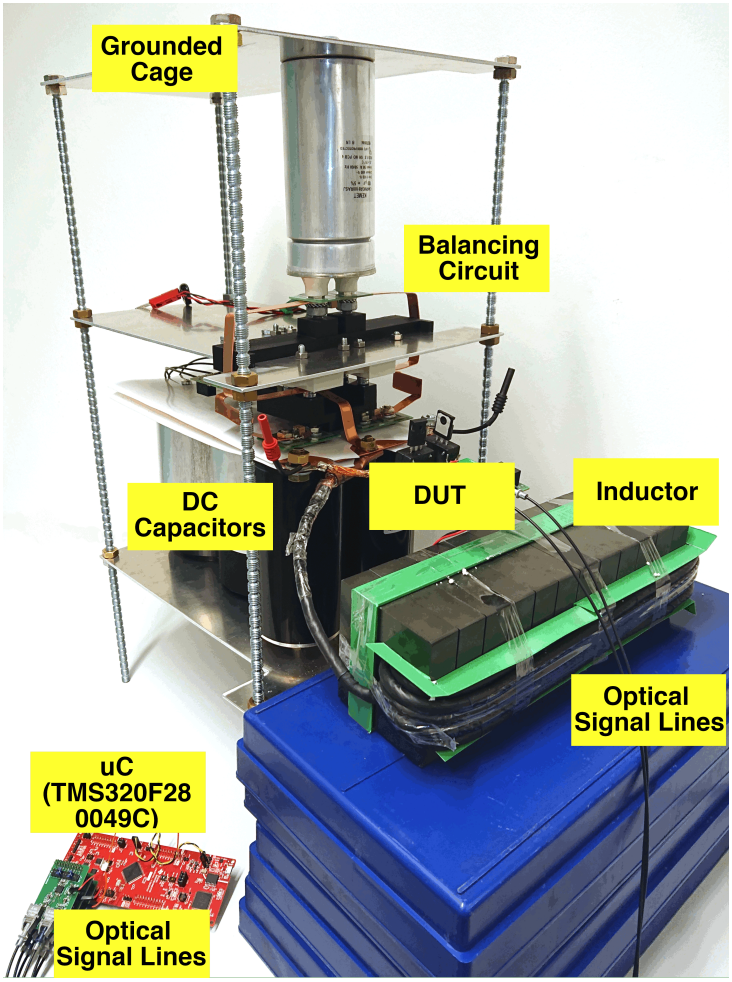



Figure 37: Photo of the test setup used for the experiments performed in this Master Thesis. Photo is from [87]

The low inducitve test platform used in this Master Thesis has sockets used for measuring $v_{\mathrm{GS}}$ and $v_{\mathrm{DS}}$ [88]. A Tektronix TPP1000 passive voltage probe was used for measuring $v_{\mathrm{GS}}$ [89]. To measure $v_{\mathrm{DS}}$, a Keysight 10076C passive voltage probe was utilized [90]. In order to measure $i_{\mathrm{D}}$, a SDN-414-05 coaxial current viewing resistor from T&M Research Products Inc. [91] was used. The measurements were recorded with a Tektronix DPO5104B oscilloscope [92]. The digital potentiometer inside the adjustable LDO boards seen in Fig. 30 are controller utilizing serial peripheral interface (SPI). The proposed AGD uses two sets of signals, a set of signals to create the wanted gate driving voltage patterns and a set of signals to set the amplitude of the intermediate voltage levels. A C2000 series microcontroller supplies all these signals by Texas Instruments [93].

The same microcontroller is also utilized to operate the balancing ciruit seen in Fig. 36 and 37 [87].

# 6 Results

In this chapter of the Master Thesis, simulation and experiment results will be presented and discussed. The parameters used during simulations and experiments will also be presented. The results obtained for both simulations and experiments will be discussed and analyzed based on the goal of the Master Thesis. Similarities and differences will also be highlighted.

## 6.1 Simulations Results

The simulations in this Master Thesis were performed using the LTSpice model, gate driver implementation, and simulation sweep functionality presented in Chapter 4. As mentioned in Chapter 4, two sets of parameter values were used for the discrete SiC MOSFET that served as the DUT and the FD. Separate simulations were performed for the turn-on and turn-off transient. The circuit parameters seen in Table 2 were used for both turn-on and turn-off switching event simulations. The circuit parameters correspond to the parameter names in curly brackets in Fig. 27. Time domain simulations corresponding to the $v_{\text{int,on}}$ and $t_{\text{int,on}}$ values used in the experiments (which are introduced later in this chapter) were also performed.

In the turn-on simulation sweep, 20 values of $v_{\text{int,on}} \in [\ 7\,\text{V}, 15\,\text{V}]$ and 20 values of $t_{\text{int,on}} \in [\ 0\,\text{ns}, 400\,\text{ns}]$ were used. This results in 400 simulations for the turn-on switching transient. Similarly, for the turn-off simulation sweep, 20 values of $v_{\text{int,off}} \in [\ -4\,\text{V}, 4\,\text{V}]$ and 20 values of duration of intermediate turn-off voltage level ($t_{\text{int,off}}$) $\in [\ 0\,\text{ns}, 400\,\text{ns}]$ were used. As three different versions of the C3M0075120K MOSFET were used for the SiC MOSFET model, over 2400 individual simulations were performed for the simulation results presented in this Master Thesis.

Table 2: Circuit parameters used during simulations

| $V_{\text{bus}}$ | $I_{\text{load}}$ | $R_{\text{g,ext}}$ | $L_{\text{t}}$ | $L_{\text{p,g}}$ | $L_{\text{p,p}}$ | $T_{\text{amb}}$ |
|---|---|---|---|---|---|---|
| 800 V | 20 A | 25 Ω | 110 µH | 1 nH | 5 nH | 25 °C |

The evaluation functionality presented in Chapter 4 was used on the data from the simulation sweeps. For each simulation in the simulation sweep, the duration of the switching events was determined. The $i_{\text{D}}$ and $v_{\text{DS}}$ values within the switching time duration were used to calculate $E_{\text{on}}$, $I_{\text{rr}}$, $V_{\text{os}}$, the maximum di/dt and the maximum dv/dt for that particular simulation. In this Master Thesis, $E_{\text{on}}$, $I_{\text{rr}}$, $V_{\text{os}}$, the maximum di/dt and the maximum dv/dt are referred to as switching performance indicators. Heatmaps were created after these switching performance indicators had been calculated for each simulation in the simulation sweep. In these heatmaps, the impact of altering $v_{\text{int,on}}$, $t_{\text{int,on}}$, $v_{\text{int,off}}$ and $t_{\text{int,off}}$ on the switching performance for the test and circuit parameters described in Table 2 can be seen. The evaluation functionality was also used to create graphs seen in Fig. 41 and 45.

#### Original MOSFET model

The heatmaps created using the evaluation functionality and the original MOSFET model introduced in Chapter 4 can be seen in Fig. 38 and 39.

Based on these heatmaps, the proposed AGD has a clear impact on the switching performance of the DUT. By varying $t_{\text{int,on}}$, $v_{\text{int,on}}$, $t_{\text{int,off}}$ and $v_{\text{int,off}}$, significant changes in the switching performance of the DUT can be observed. The heatmaps indicate that introducing the intermediate voltage levels slows down the switching transients. For example, if $t_{\text{int,on}}$ is increased, $I_{\text{rr}}$ is reduced and the rate of change for both $i_{\text{D}}$ and $v_{\text{DS}}$ is reduced. However, this comes at the expense of increased $E_{\text{on}}$.

For some$t_{\text{int,on}}$ and $v_{\text{int,on}}$ values, the influence of the AGD is much larger compared to other regions. This also holds for both the turn-on and the turn-off switching events. For the turn-on transient, if $v_{\text{int,on}}$ is close to either 15 V or 7 V, the impact of altering $t_{\text{int,on}}$ is strongly reduced compared to other values of $v_{\text{int,on}}$. For $v_{\text{int,on}} = 15\,\text{V}$, $t_{\text{int,on}}$ has no impact on switching performance, as 15 V is the on-state

driving voltage ($V_{\mathrm{GG,on}}$) of the DUT. At $v_{\mathrm{int,on}} \approx 7\,\mathrm{V}$, the switching event is delayed instead of slowed down. The impact of altering $t_{\mathrm{int,on}}$ has a negligible on the turn-on switching performance. The delay of the voltage and current commutation for $v_{\mathrm{int,on}} = 7.5\,\mathrm{V}$ can be seen in Fig. 40. Instead of slowing down the switching transients of $v_{\mathrm{DS}}$ and $i_{\mathrm{D}}$, they are delayed instead. This is especially true for the commutation of $v_{\mathrm{DS}}$. For $i_{\mathrm{D}}$, the current commutation is slowed down, but the current overshoot ($I_{\mathrm{rr}}$) remains almost constant. To ensure that the intermediate voltage level at turn-on has a significant impact on the switching performance, $v_{\mathrm{int,on}}$ and $t_{\mathrm{int,on}}$ must be varied within specific ranges. For achieving a large impact on $E_{\mathrm{on}}$, $v_{\mathrm{int,on}} \lessapprox 11\,\mathrm{V}$ and $t_{\mathrm{int,on}} \gtrapprox 100\,\mathrm{ns}$ are necessary. This can be seen in Fig. 38a. The impact of $v_{\mathrm{int,on}}$ and $t_{\mathrm{int,on}}$ on the other switching performance indicators ($I_{\mathrm{rr}}$, dv/dt and di/dt) is quite different. While $E_{\mathrm{on}}$ changes gradually, both when varying $v_{\mathrm{int,on}}$ and $t_{\mathrm{int,on}}$, the three other switching performance indicators change more abruptly when varying $t_{\mathrm{int,on}}$. Depending on the value $v_{\mathrm{int,on}}$, $t_{\mathrm{int,on}}$ must have a certain value to impact $I_{\mathrm{rr}}$, dv/dt and di/dt. If, for example, $v_{\mathrm{int,on}} \approx 11\,\mathrm{V}$, $t_{\mathrm{int,on}}$ must be approximately 100 ns for the intermediate voltage level to have an impact. In addition, this impact is nearly binary, if $t_{\mathrm{int,on}} \lessapprox 100\,\mathrm{ns}$ at $v_{\mathrm{int,on}} \approx 11\,\mathrm{V}$, there is almost no impact. However, if $t_{\mathrm{int,on}}$ is raised slightly, there is a large change in $I_{\mathrm{rr}}$, dv/dt and di/dt. If, on the other hand, $t_{\mathrm{int,on}}$ is raised further $I_{\mathrm{rr}}$, dv/dt and di/dt change very little in value. Keeping $t_{\mathrm{int,on}}$ fixed and varying $v_{\mathrm{int,on}}$, the impact of the intermediate voltage at turn-on changes more gradually.

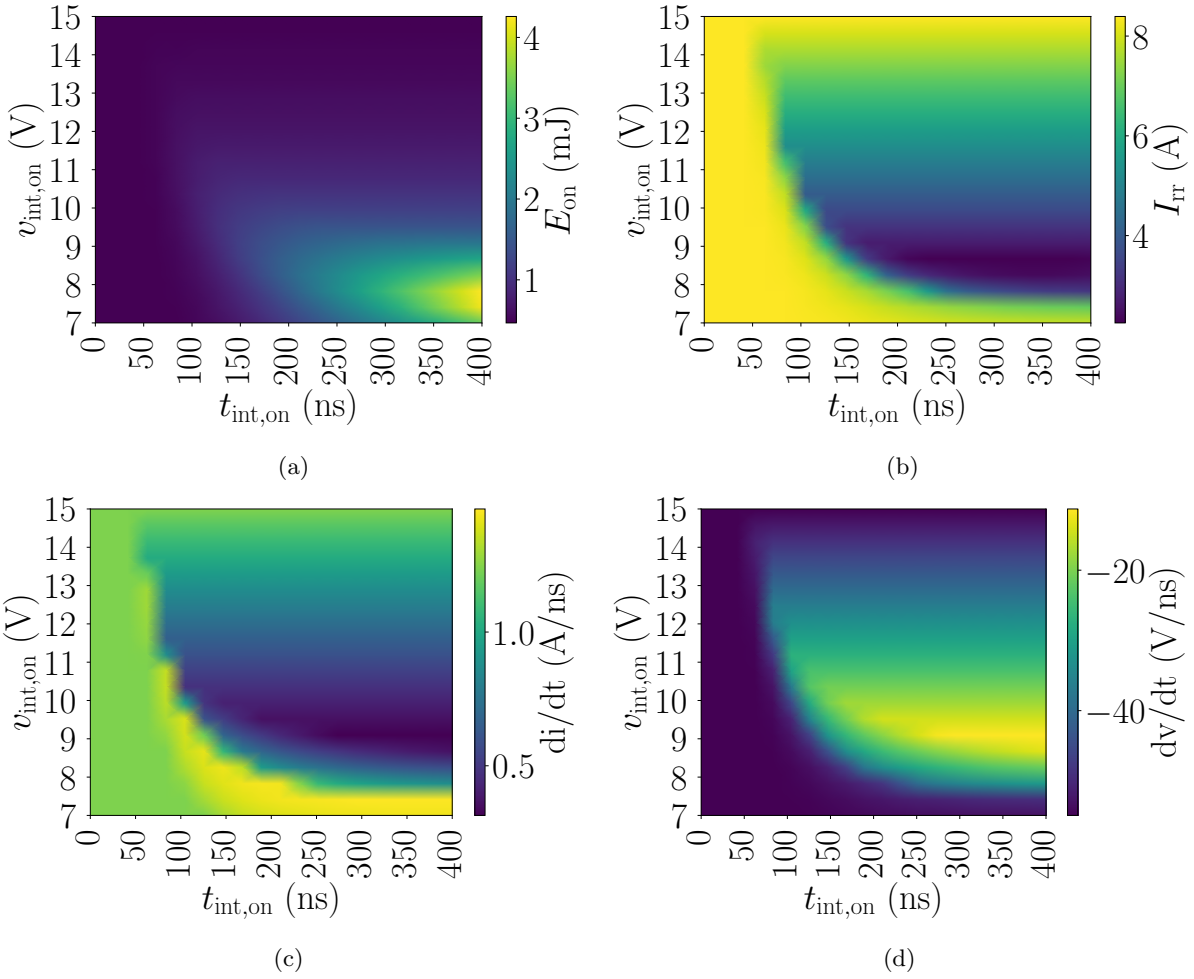



Figure 38: Influence of $v_{\mathrm{int,on}}$ and $t_{\mathrm{int,on}}$ on switching performance indicators during turn-on, using the original MOSFET model

The impact of the intermediate voltage level during turn-off also indicates that the proposed AGD concept can affect the switching performance of the DUT. Increasing $t_{\mathrm{int,off}}$ causes increased $E_{\mathrm{off}}$, while $V_{\mathrm{os}}$, dv/dt, and di/dt are reduced. This can be seen in Fig. 39.

For the turn-off switching transition, the impact of the intermediate voltage level is similar to the turn-on

switching transition. $V_{os}$ can be reduced and dv/dt and di/dt can be slowed down. However, this comes at an increase in $E_{off}$. Similarly to the turn-on transient, increasing $t_{int,off}$ has no effect until a certain value (which depends on the value of $t_{int,off}$). At this certain $t_{int,off}$, the switching performance indicators experience a significant change in value. Increasing $t_{int,off}$ past this threshold yields a significant change in switching performance. Altering $v_{int,off}$ results in a more gradual change in the performance of the DUT during switching.

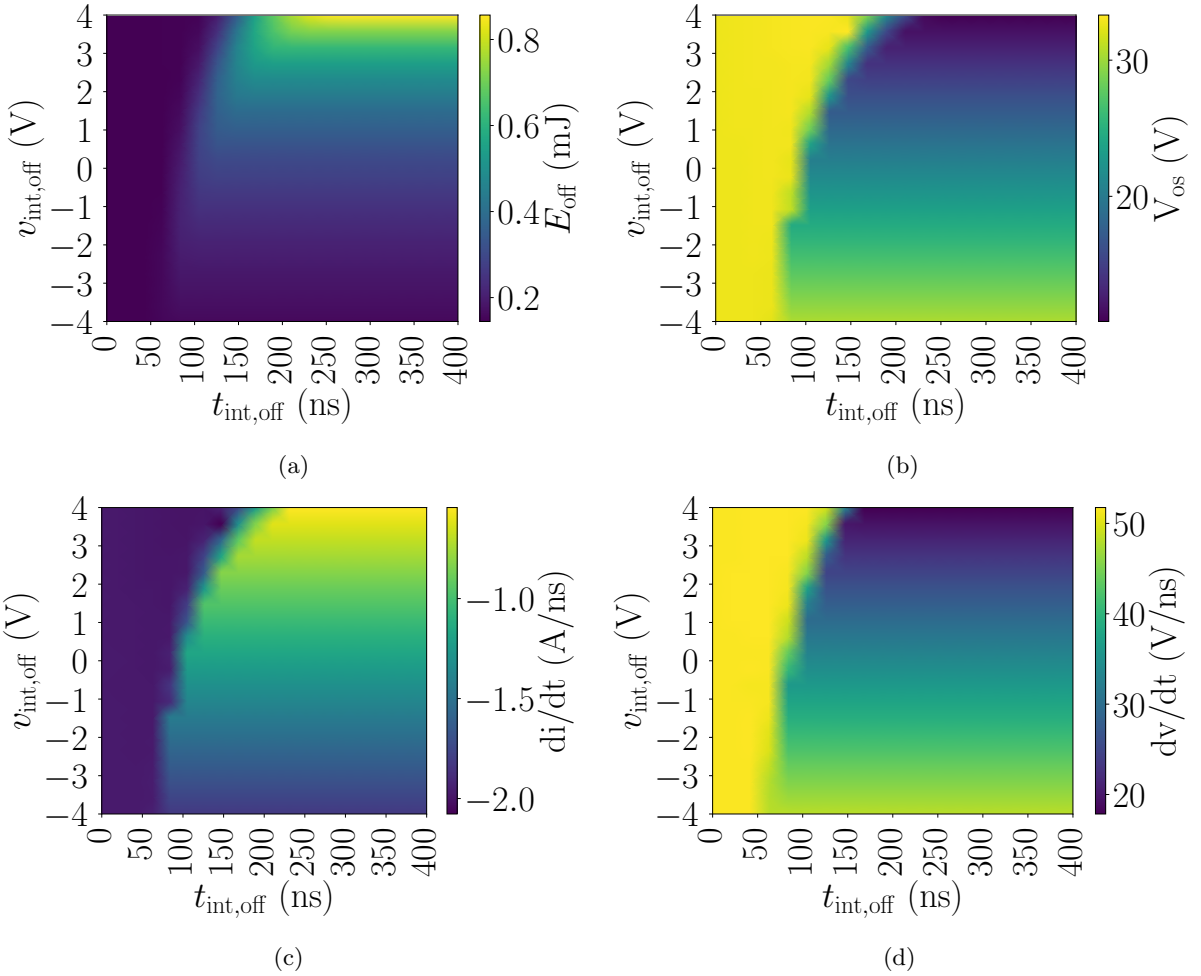



Figure 39: Influence of $v_{int,off}$ and $t_{int,off}$ on switching performance indicators during turn-off, using the original MOSFET model

As seen in Fig. 38 and 39, the values used for $v_{int,on}$, $t_{int,on}$, $v_{int,off}$ and $t_{int,off}$ have a large impact on the switching performance indicators. Therefore, care must be taken when choosing the value ranges for $v_{int,on}$ and $t_{int,on}$ at turn-on, and for $v_{int,off}$ and $t_{int,off}$ at turn-off. In order to reduce the processing speed and precision requirements for the control system, $v_{int,on}$, $t_{int,on}$, $v_{int,off}$ and $t_{int,off}$ should be altered in value ranges that result in small gradients in the switching performance indicators. If the rate of change in the performance parameters is small, the control system can be slower and less precise in its response than if the rate of change is significant. In the switching performance parameter heatmaps, there are regions where the rate of change differs greatly. For example, in Fig. 38d, for $t_{int,on} \gtrapprox 250\,\text{ns}$, altering $v_{int,on}$ from 7 V to 9 V has approximately the same impact on dv/dt as changing $v_{int,on}$ from 15 V to 9 V. However, the change in dv/dt happens much slower for $v_{int,on} \in [\,9\,\text{V}, 15\,\text{V}]$ compared to $v_{int,on} \in [\,7\,\text{V}, 9\,\text{V}]$. Therefore, the requirements for the control system of the AGD would be lessened if $v_{int,on} \in [\,9\,\text{V}, 15\,\text{V}]$. To achieve decoupling of voltage and current slopes from switching losses, the choice of control variable values is yet more restricted. During the turn-on transient (Fig. 38), the turn-on energy $E_{on}$ can be controlled without incurring big changes on dv/dt and di/dt if $v_{int,on} \approx 7\,\text{V}$ and $t_{int,on} \in [\,150\,\text{ns}, 400\,\text{ns}]$. This can also be achieved for turn-off transient (Fig. 39). For $t_{int,off} \gtrapprox 100\,\text{ns}$ and $v_{int,off} \lessapprox -2\,\text{V}$, dv/dt and di/dt can be altered without significant changes in $E_{off}$.

As can be seen in Fig. 39, if $v_{\text{int,off}}$ held constant, at a certain $t_{\text{int,off}}$ the switching performance indicators change values rapidly. For example, in Fig. 39a, if $v_{\text{int,off}} = 1\,\text{V}$, $E_{\text{off}}$ changes from approximately 0.2 mJ to 0.5 mJ if $t_{\text{int,off}}$ goes from 75 ns to 80 ns. The voltage amplitude of the intermediate voltage level is what determines how fast the charge is provided or removed from the gate. The intermediate voltage duration determines how long the charge rate is applied. Therefore, the combination of these two aspects determines the impact the intermediate voltage levels have on the switching transient. This means that the longer the intermediate voltage level at turn-off is applied, the more charge is removed from the gate of the DUT. This could explain how at approximately $t_{\text{int,off}} = 75\,\text{ns}$ increasing $t_{\text{int,off}}$ starts to increase $E_{\text{off}}$. At this point, sufficient charge has been removed to the gate, lower $v_{\text{GS}}$ to a value causing $v_{\text{DS}}$ to rise. This causes both $v_{\text{DS}}$ and $i_{\text{D}}$ to a relatively high value, yielding larger switching loss. Before this value of $t_{\text{int,off}}$, the intermediate voltage level delays the switching event instead of slowing it down.

To compare simulation and experiment results, time domain simulation results using the same $v_{\text{int,on}}$ and $t_{\text{int,on}}$ values as the experiments are plotted in Fig. 40.

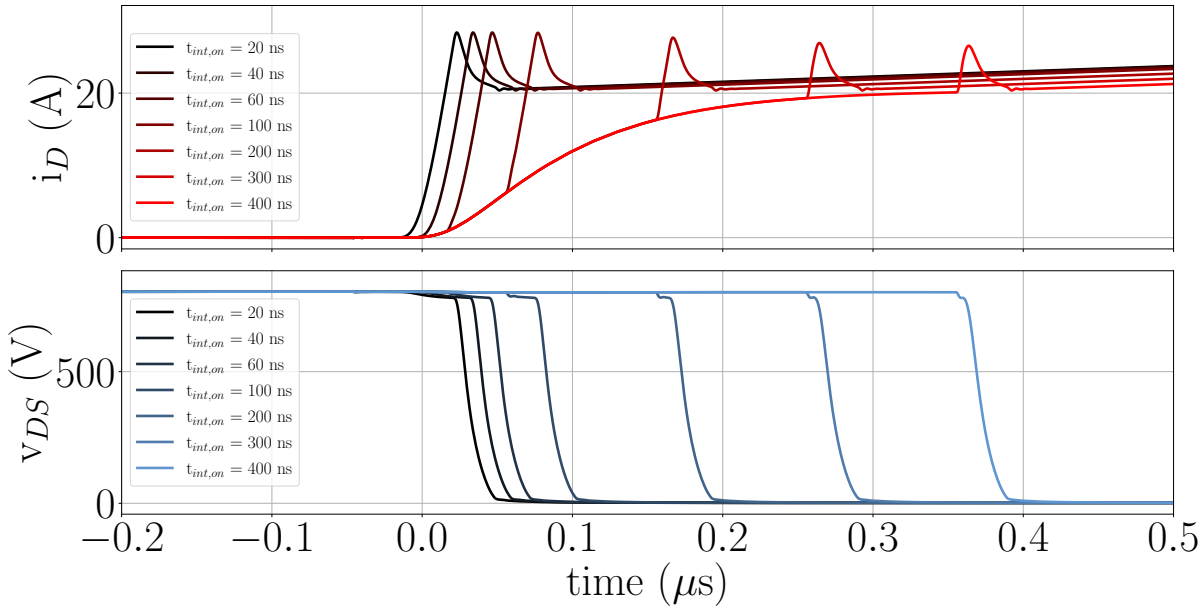



Figure 40: Simulated $i_{\text{D}}$ and $v_{\text{DS}}$ waveforms under variation of $t_{\text{int,on}}$, using the original MOSFET models

Fig. 41 display the switching performance indicators for these simulations.

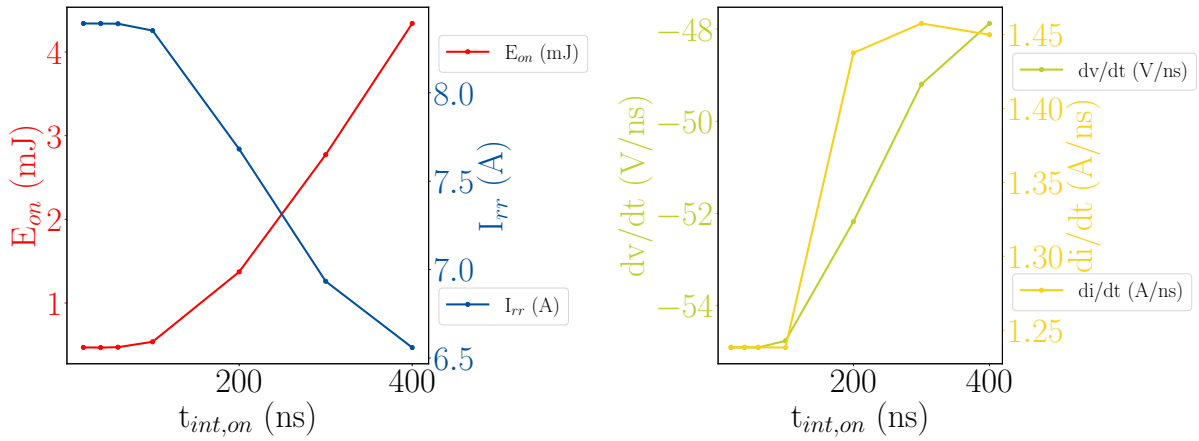



Figure 41: MOSFET switching performance indicators from time domain simulations, using the original MOSFET model

As mentioned earlier in this chapter, $v_{\text{int,on}} = 7\,\text{V}$ slows down the current commutation, but delays the voltage commutation. This can be seen in Fig. 40. By increasing the duration of the intermediate voltage level and thereby slowing down the switching event, the drain current changing rate should be decreased. However, in the time domain simulations, the opposite occurs. This can be seen in Fig. 41. This could be caused by the fact that even though the current commutation takes longer as $t_{\text{int,on}}$ is increased, the current overshoot amplitude and shape remain relatively similar for the different values of $t_{\text{int,on}}$. $t_{\text{int,on}}$ is varied from 20 ns to 400 ns only reduces the current overshoot by 1.5 A. This combined with the fact that it is the maximum di/dt and dv/dt that are calculated could explain the unexpected shape of di/dt in Fig. 41. The delay of the voltage commutation combined with the slowing down of parts of the current commutation explains the substantial increase in $E_{\text{on}}$ seen in Fig. 41a. Altering $t_{\text{int,on}}$ from 20 ns to 400 ns results in a 400 % increase of $E_{\text{on}}$. Had $v_{\text{DS}}$ been slowed down instead of delayed, the instantaneous loss of power would be less. This would integrate to a lower $E_{\text{on}}$.

### Fitted MOSFET Model

The simulation sweep heatmaps using the second MOSFET model can be seen in Fig. 42 and 43. For the turn-on switching event, there is a short range of $t_{\text{int,on}}$ values, for which varying $t_{\text{int,on}}$ has an impact on the switching performance indicators. For example, if $v_{\text{int,on}} = 7\,\text{V}$, $E_{\text{on}}$ (Fig. 42a), $I_{\text{rr}}$ (Fig. 42b) and dv/dt (Fig. 42d) can be manipulated by altering $t_{\text{int,on}}$ if $t_{\text{int,on}} \in [\,50\,\text{ns}, 80\,\text{ns}]$. If $t_{\text{int,on}}$ is not in this range, $t_{\text{int,on}}$ has a negligible impact on the switching performance indicators. The range of $t_{\text{int,on}}$ values that are able to impact the switching performance indicators, is reduced as $v_{\text{int,on}}$ increases. For di/dt, the range of $t_{\text{int,on}}$ values impacting the switching performance is more narrow.

For $t_{\text{int,on}}$ values below $t_{\text{int,on}} \in [\,50\,\text{ns}, 80\,\text{ns}]$, altering $v_{\text{int,on}}$ has a minimal impact on $E_{\text{on}}$, $I_{\text{rr}}$, dv/dt and di/dt. For $t_{\text{int,on}}$ values above $t_{\text{int,on}} \in [\,50\,\text{ns}, 80\,\text{ns}]$, decreasing $v_{\text{int,on}}$ increases $E_{\text{on}}$ and reduces $I_{\text{rr}}$ and the maximum rate of change in voltage and current.

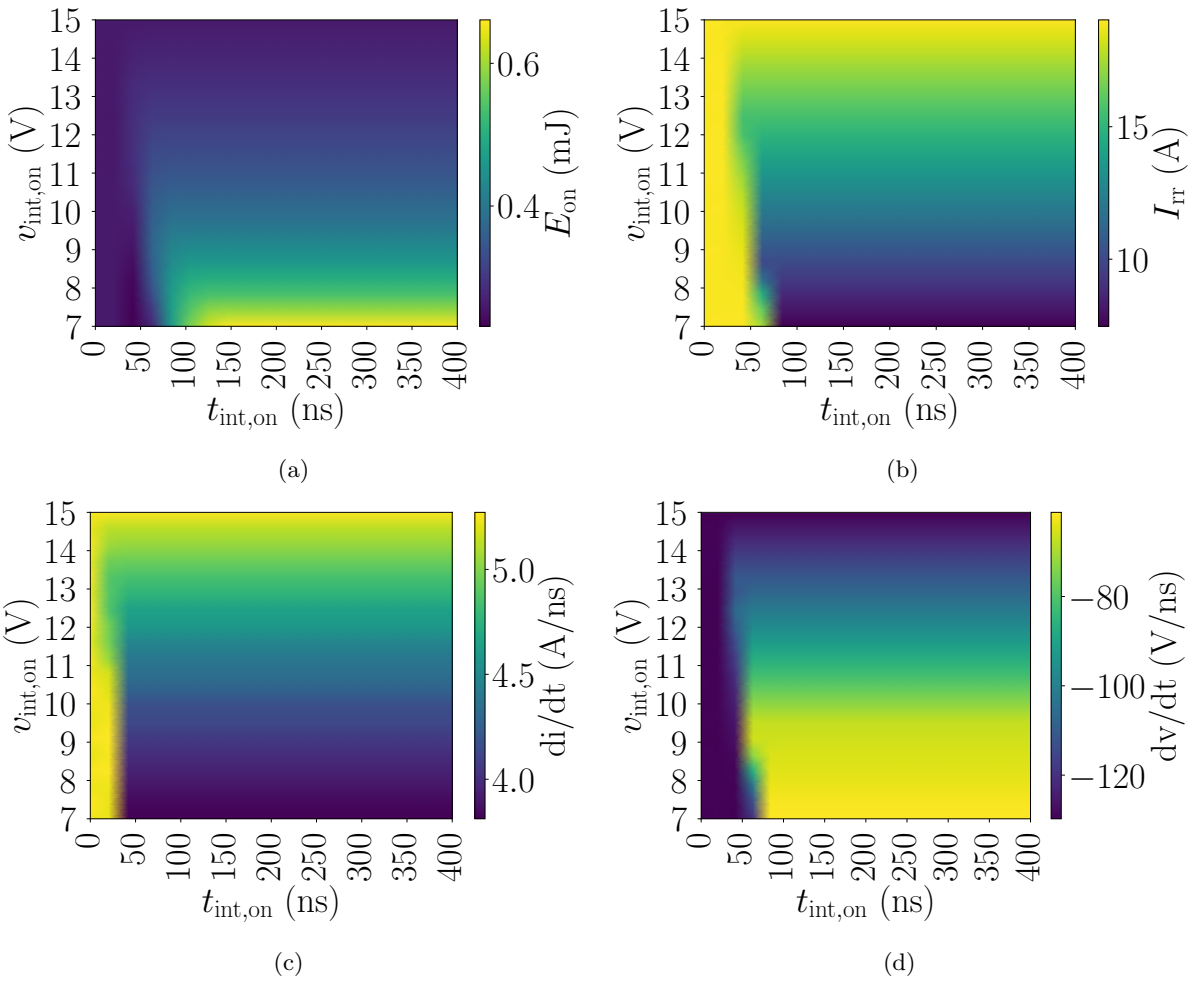



Figure 42: Influence of $v_{\mathrm{int,on}}$ and $t_{\mathrm{int,on}}$ on switching performance indicators during turn-on, using the fitted MOSFET model

Similarly to the turn-on switching event, there are ranges of $t_{\mathrm{int,off}}$ values, depending on $v_{\mathrm{int,off}}$, that enable $t_{\mathrm{int,off}}$ to change the switching performance at turn-off. For example, if $t_{\mathrm{int,off}} \in [\,75\,\mathrm{ns}, 100\,\mathrm{ns}]$, $V_{\mathrm{os}}$ (Fig. 43b), di/dt (Fig. 43c) and dv/dt (Fig. 43d) can be altered by changing $t_{\mathrm{int,off}}$. If $v_{\mathrm{int,off}} \in [\,-4\,\mathrm{V}, 2.5\,\mathrm{V}]$ and $t_{\mathrm{int,off}}$ is below the $t_{\mathrm{int,off}}$ value range of switching performance impact, changing $t_{\mathrm{int,off}}$ and $v_{\mathrm{int,off}}$ has no impact on the switching performance. If $v_{\mathrm{int,off}} \in [\,-4\,\mathrm{V}, 2.5\,\mathrm{V}]$ and $t_{\mathrm{int,off}}$ is above the $t_{\mathrm{int,off}}$ value range of switching performance impact, changing $v_{\mathrm{int,off}}$ has a clear impact on the switching performance indicators.

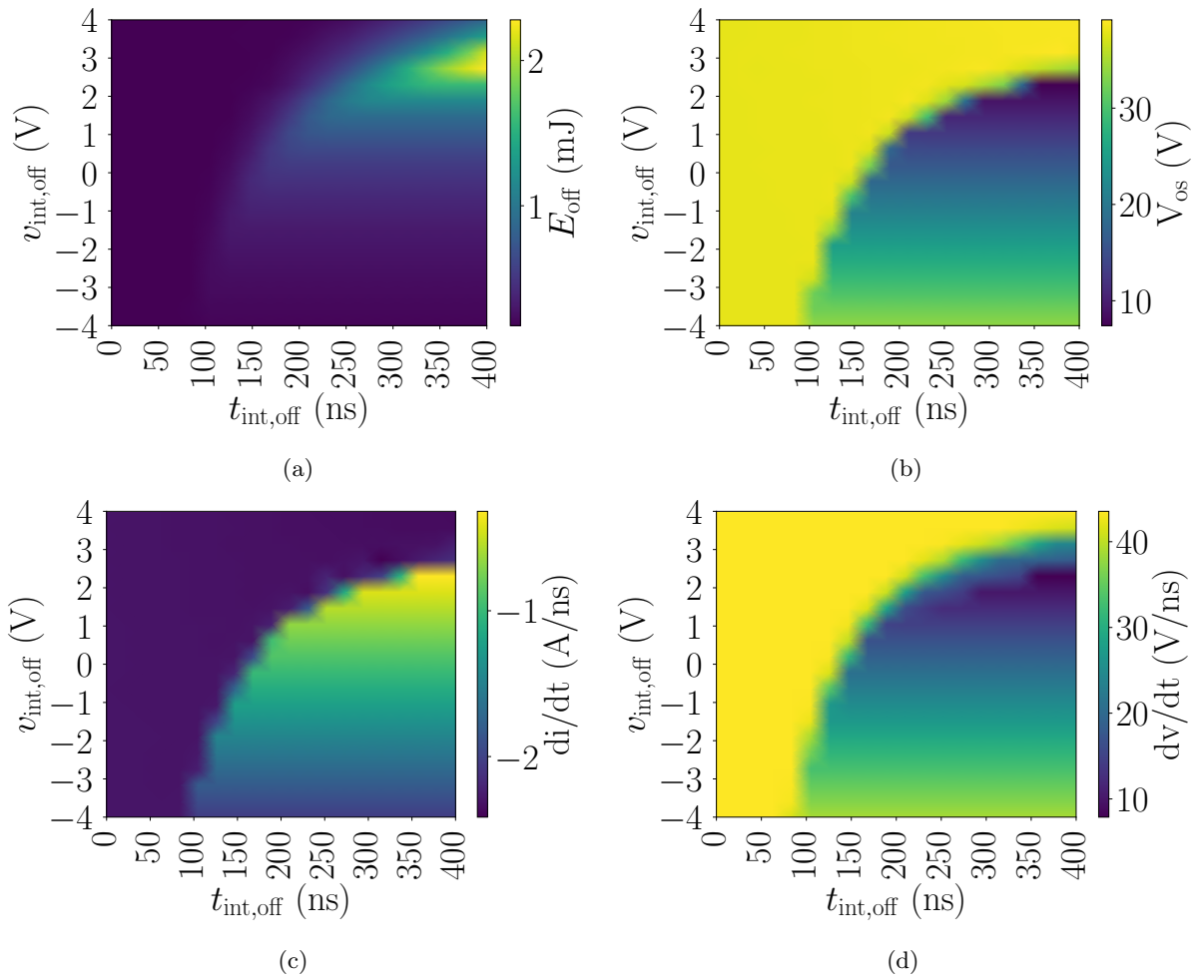



Figure 43: Influence of $v_{\text{int,off}}$ and $t_{\text{int,off}}$ on switching performance indicators during turn-off, using the fitted MOSFET model

Comparing the heatmaps for the original MOSFET model (Fig. 38 and 39) to the heatmaps for the fitted MOSFET model, several differences can be observed. Looking at Fig. 38 and 42, $t_{\text{int,on}}$ has less significant impact on the turn-on switching transient for the fitted MOSFET model. Using the fitted MOSFET model, the turn-on switching transient has lower $E_{\text{on}}$ and higher $I_{\text{rr}}$, dv/dt and di/dt compared to the original MOSFET model. Altering $v_{\text{int,on}}$ has a similar impact for the original and the fitted MOSFET model, except for $v_{\text{int,on}} \lessapprox 7.5\,\text{V}$. For the original model (Fig. 38), if $v_{\text{int,on}} \lessapprox 7.5\,\text{V}$ the impact on the switching performance indicators reverses. For example, in Fig. 38b, if $v_{\text{int,on}} \in [\,7.5\,\text{V}, 15\,\text{V}]$, decreasing $v_{\text{int,on}}$ reduces $I_{\text{rr}}$. However, for $v_{\text{int,on}} \lessapprox 7.5\,\text{V}$, decreasing $v_{\text{int,on}}$ reduces $I_{\text{rr}}$. For the fitted MOSFET model heatmaps, the impact of altering $v_{\text{int,on}}$ is the same for the entire range of $v_{\text{int,on}}$, as long as $t_{\text{int,on}}$ has a high enough value to not impact switching performance. This can be seen, for example, in Fig. 42b. If $t_{\text{int,on}} \gtrapprox 75\,\text{ns}$, decreasing $v_{\text{int,on}}$ causes $I_{\text{rr}}$ to increase.

For the turn-off switching transient, the switching performance parameter of the original MOSFET model and the fitted MOSFET model also have differences. In the fitted MOSFET model, which can be seen Fig. 42, there is a region of $v_{\text{int,off}}$ values where altering $t_{\text{int,off}}$ has no impact on $V_{\text{os}}$ (Fig. 43b), di/dt (Fig. 43c), and dv/dt (Fig. 43d). This is the case for $v_{\text{int,off}} \gtrapprox 2.5\,\text{V}$ for $V_{\text{os}}$ and di/dt as well. For dv/dt, $v_{\text{int,off}}$ must be greater than approximately 3.5 V for $t_{\text{int,off}}$ to have no impact. When it comes to the magnitude of the switching performance indicators, all the switching performance indicators except for $E_{\text{off}}$ have similar minimum and maximum values when comparing the original model and the fitted model. This can be seen in by comparing the colormaps of Fig. 42 and 43.

Fig. 44 show time domain simulations using the fitted MOSFET model. These time domain simulations are based on the same $t_{\text{int,on}}$ values and the same $v_{\text{int,on}}$ value as the time domains simulations in Fig.

40.

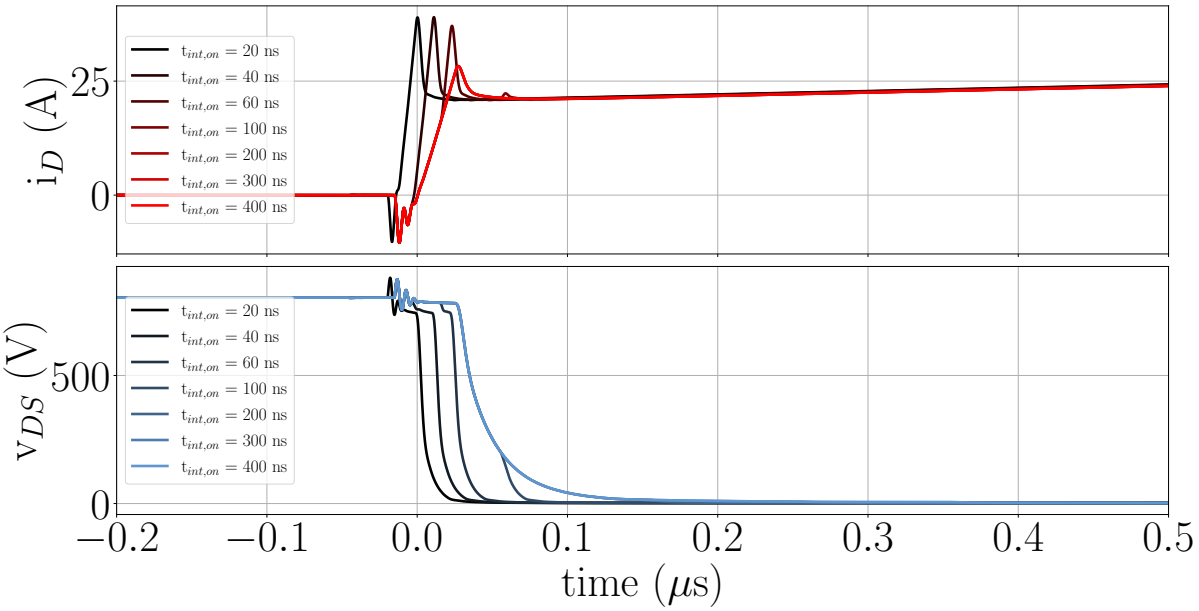



Figure 44: Simulated $i_{\mathrm{D}}$ and $v_{\mathrm{DS}}$ waveforms under variation of $t_{\mathrm{int,on}}$, using the fitted MOSFET model

Fig. 45 show the switching performance indicators from these simulations.

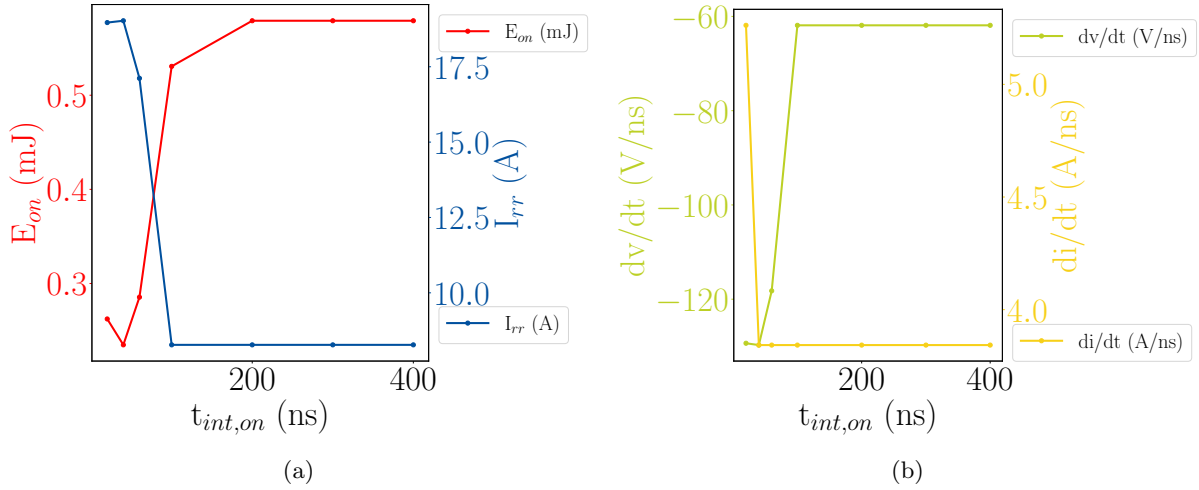



Figure 45: MOSFET switching performance indicators from time domain simulations, using the fitted MOSFET model

Significant differences can be observed in the time domain simulations of the original model and the fitted model. Firstly, in the original model (Fig. 40), there was no slowing down of the voltage commutation, only a delay. In the fitted MOSFET model, however, the voltage commutation is slowed down significantly, at the highest value of $t_{\mathrm{int,on}}$. This agrees more with the expected impact of the intermediate voltage levels. Compared to the original model, the current commutation also occurs significantly faster when using the fitted MOSFET model. This is especially prominent for $t_{\mathrm{int,on}} = 400\,\mathrm{ns}$. In the original model (Fig. 40), the drain current commutation from 0 A to 20 A takes approximately 3.6 µs. However, with the fitted model (Fig. 44), the same current commutation takes 3.6 µs. This drain current and drain-source voltage commutation speed acceleration mean that the turn-on event is shorter. This results in lower switching losses, but higher reverse recovery peak and voltage and current slopes. The increase in reverse recovery peak is caused by the discharge of the reverse recovery charge from the body diode of

FD also being accelerated.

When comparing the turn-off switching transient from the original and fitted MOSFET models, the fitted MOSFET does not seem to cause a shortening of the turn-off event. For the turn-on event, the original MOSFET model had a higher $E_{on}$ compared to the fitted MOSFET model. This is reversed for the turn-off event. The simulations performed with the two MOSFET models use the same $t_{int,off}$ and $v_{int,off}$ values. Therefore, the fact that the other switching performance indicators ($I_{rr}$, dv/dt, and di/dt) have similar maximum values between the models supports that the turn-off takes a similar amount of time between the models. The difference in $E_{off}$ seen between the MOSFET models could instead be caused by a difference in threshold voltage between the models. If there is an extended time duration where the fitted MOSFET model carries a portion of the bus voltage, instead of commutating completely, the switching losses would be increased. The oscillations in $i_D$ and $v_{DS}$, as well as the negative dip in $i_D$, were also not observed when using the original model. A drain current reversal under a positive load current, solely caused by the gate driver, is not realistic. The parameter fitting method used for creating the fitted model is a fitting method for describing static SiC Power MOSFET behavior. Since DPTs are dynamic tests, the inaccuracies seen in the fitted model could be caused by this. The fitting method was also based on experiments with $v_{DS}$ up to 60 V, while the DC bus voltage in the DPTs is 800 V.

### Manually Altered MOSFET Model

The heatmaps describing the impact of altering $v_{int,on}$, $t_{int,on}$, $v_{int,off}$ and $t_{int,off}$ on the switching performance when using the manually altered MOSFET model can be seen in Fig. 46 and 47.

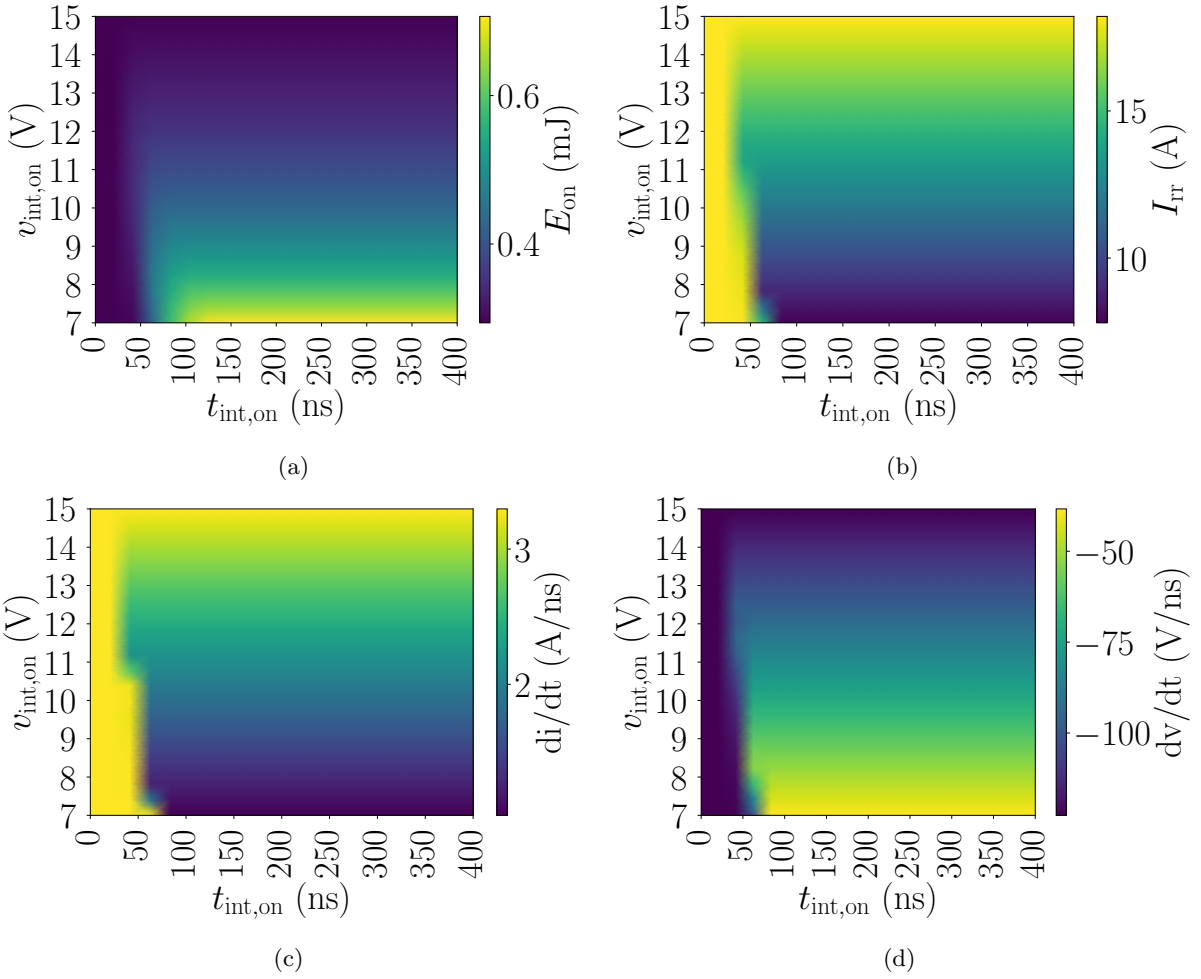



Figure 46: Influence of $v_{int,on}$ and $t_{int,on}$ on switching performance indicators during turn-on, using the manually altered MOSFET model

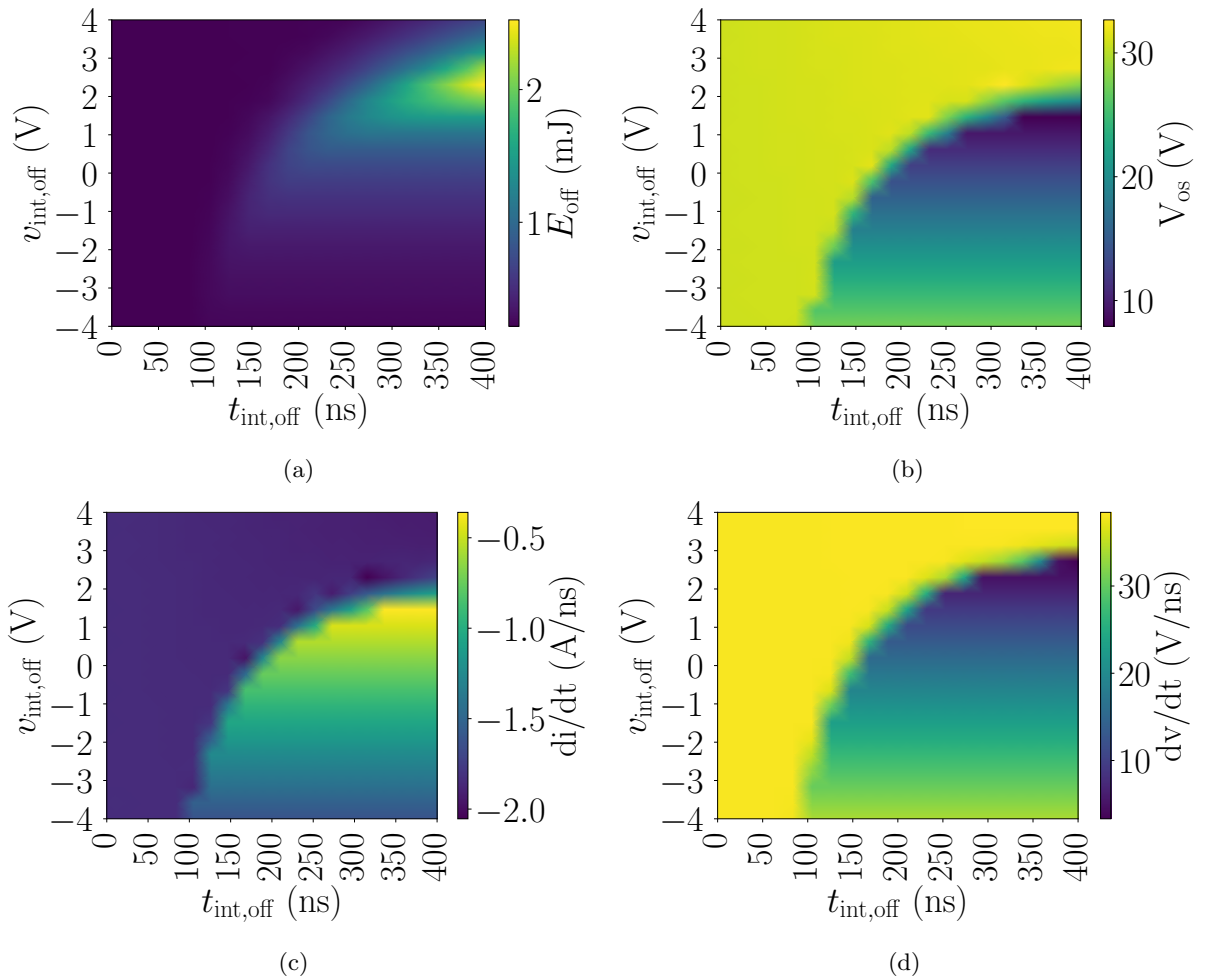



Figure 47: Influence of $v_{\text{int,off}}$ and $t_{\text{int,off}}$ on switching performance indicators during turn-off, using the manually altered MOSFET model

Comparing the heatmaps from the fitted model to the heatmaps from the manually altered model show that they are very similar. However, when comparing the time domain simulations, there are differences. The time domain simulations created with the manually altered MOSFET model can be seen in Fig. 48. The switching performance of the DUT MOSFET model can be seen in Fig. 49. When using the fitted model, there is a time duration for which $i_{\text{D}}$ becomes negative, as well as oscillations in $v_{\text{DS}}$ and $i_{\text{D}}$. These are not present when using the manually fitted model. This suggests that the manually altered model provides a more realistic description of the MOSFET compared to the fitted model.

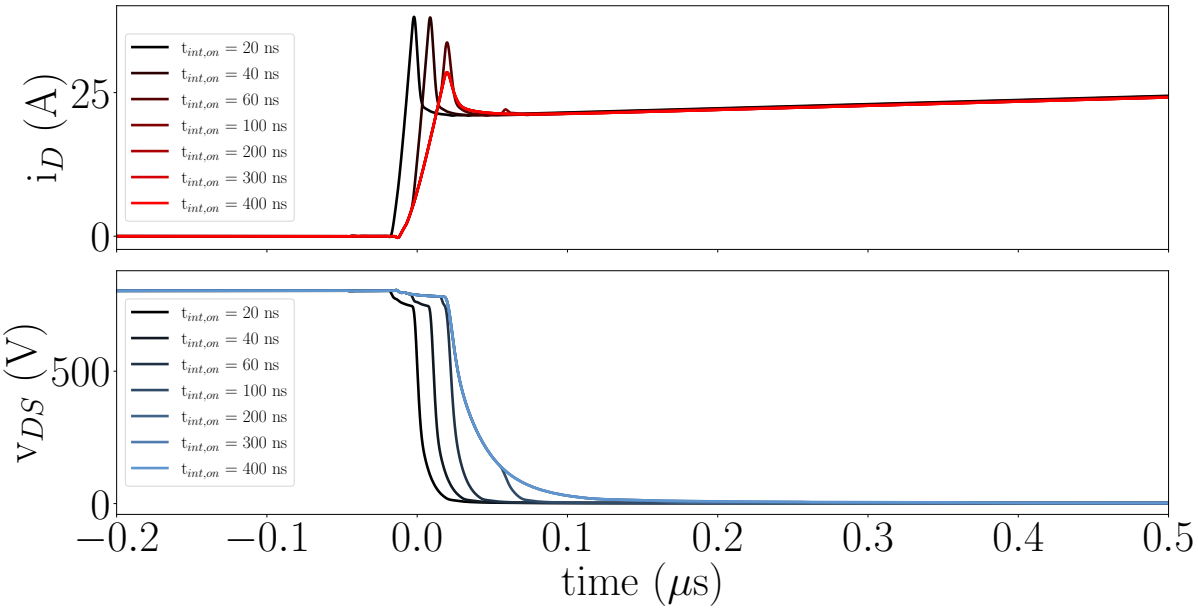
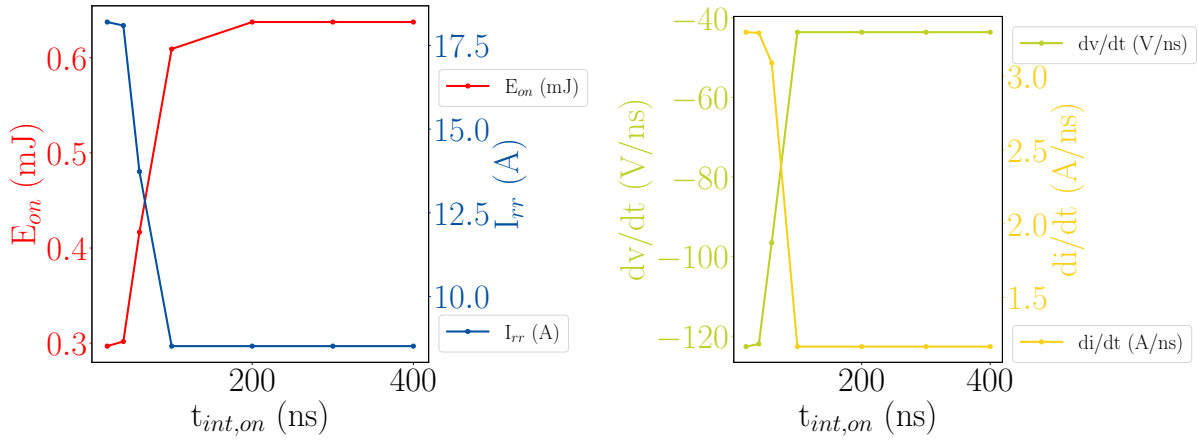



Figure 48: Simulated $i_{\mathrm{D}}$ and $v_{\mathrm{DS}}$ waveforms under variation of $t_{\mathrm{int,on}}$, using the manually altered MOSFET model




(a) (b)

Figure 49: MOSFET switching performance indicators from time domain simulations, using the manually altered MOSFET model

## 6.2 Experimental Results

In order to further investigate and validate the active gate driver concept presented in Chapter 3, experimental double pulse tests were performed in accordance with the test setup presented in Chapter 5. The test setup, as can be seen in Fig. 35 and 37, was combined and placed inside a test enclosure. The door of the enclosure has to be closed for the test setup to be energized. Fig. 50 is a picture of the test setup placed inside the test enclosure. Cardboard boxes were used to place the AGD, and the DUT platform on the same height as the microcontrollers. This was done to reduce the length of the signal cables. To connect the test inductor to the test circuit, an increased distance between the AGD and DUT platform from the test inductor was needed. Cardboard was also used for this. The test inductor can be seen in green and black below the AGD and DUT platform in Fig. 50.

The input voltage for the microcontrollers and the adjustable LDOs was provided by using power supplies located behind the microcontrollers. The grounded cage, presented in Fig. 37, can be see in the

background of Fig. 50. The rest of the test setup introduced in Chapter 5 is hidden behind the other components described earlier.

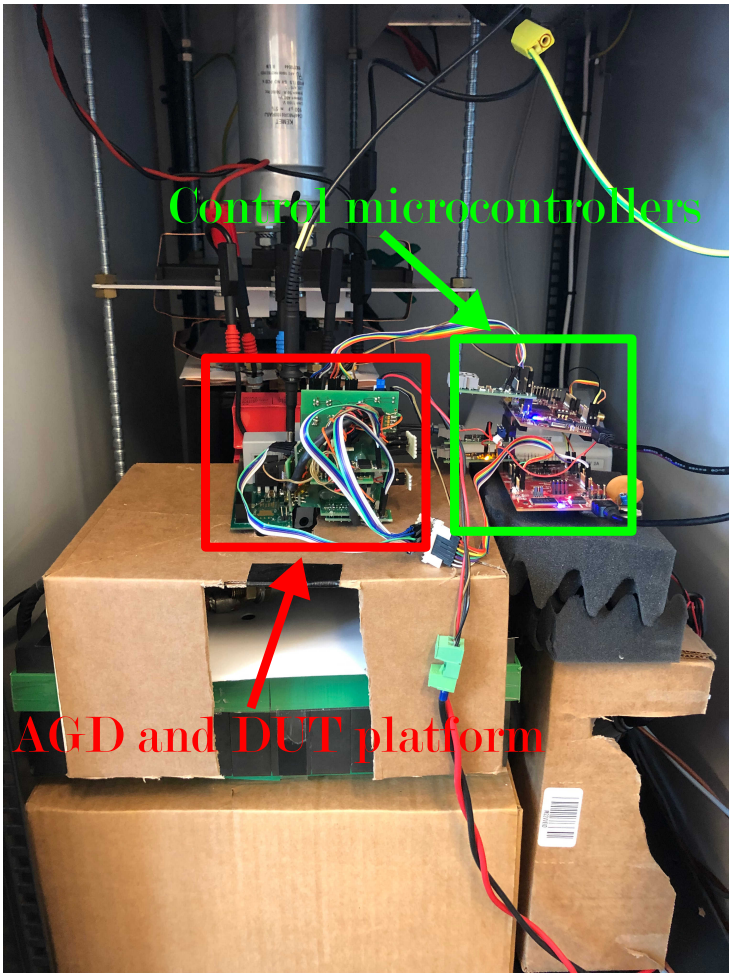



Figure 50: Photo showing the test setup used for the experimental DUTs inside the test enclosure.

The DUT and FD used for the experiments performed in this Master Thesis is the 1200 V 32 A C3M0075120D SiC Power MOSFET from Wolfspeed. [94]. Initially, the goal was to create heatmaps from the experiments similar to those from the simulation sweeps. Similar values for $v_{\text{int,on}}$, $t_{\text{int,on}}$, $v_{\text{int,off}}$ and $t_{\text{int,off}}$ to the values used in the simulations sweeps, were going to be used for the experiments. However, due to time constraints, experimental DPTs for an exemplary selection of $v_{\text{int,on}}$ and $t_{\text{int,on}}$ values were performed instead. In addition, the ability of the proposed AGD prototype to affect the gate-source voltage amplitude and duration was tested with a DC bus voltage of 0 V.

### Test of Voltage Amplitude and Duration Regulation

In order to verify the functionality of the AGD prototype, tests were performed with a DC bus voltage of 0 V. First, all the different gate-source voltage levels the AGD was designed to be able to produce were generated and measured. These measured voltage levels were compared to their design value. In Table 3, the design value and the measured value for the different voltage amplitudes of $V_{\text{GG,on}}$ can be seen.

Table 3: Voltage amplitudes for $V_{\mathrm{GG,on}}$ that can be generated by the AGD prototype

| **Level:** | **Design value [V]:** | **Measured value [V]:** |
|---|---|---|
| 0 | 10 | 10.22 |
| 1 | 11.25 | 11.322 |
| 2 | 12.5 | 12.722 |
| 3 | 13.75 | 13.922 |
| 4 | 15 | 14.922 |
| 5 | 16.25 | 16.122 |
| 6 | 17.5 | 17.322 |
| 7 | 18.75 | 18.522 |
| 8 | 20 | 19.722 |

In Table 4, the design value and the measured value for the different voltage amplitudes of $v_{\mathrm{int,on}}$ can be seen.

Table 4: Voltage amplitudes for $\mathrm{v}_{int,on}$ that can be generated by the AGD prototype

| **Level:** | **Design value [V]:** | **Measured value [V]:** |
|---|---|---|
| 0 | 7.5 | 7.522 |
| 1 | 8.75 | 8.922 |
| 2 | 10 | 10.122 |
| 3 | 11.25 | 11.322 |
| 4 | 12.5 | 12.722 |
| 5 | 13.75 | 13.922 |
| 6 | 15 | 16.322 |
| 7 | 16.25 | 16.322 |
| 8 | 17.5 | 17.522 |
| 9 | 18.75 | 18.722 |
| 10 | 20 | 19.922 |

In Table 5, the design value and the measured value for the different voltage amplitudes of $v_{\mathrm{int,off}}$ can be seen.

Table 5: Voltage amplitudes for $\mathrm{v}_{int,off}$ that can be generated by the AGD prototype

| **Level:** | **Design value [V]:** | **Measured value [V]:** |
|---|---|---|
| 0 | -5 | -5.878 |
| 1 | -3.75 | -4.678 |
| 2 | -2.5 | -3.478 |
| 3 | -1.25 | -2.078 |
| 4 | 0 | -0.878 |
| 5 | 1.25 | -0.322 |
| 6 | 2.5 | 1.522 |
| 7 | 3.75 | 2.722 |
| 8 | 5 | 3.8 |

Based on the voltage amplitudes seen in Table 3, 5 and 4, the adjustable LDOs in the proposed AGD prototype are able to alter the voltage amplitude of $V_{\mathrm{GG,on}}$, $v_{\mathrm{int,on}}$ and $v_{\mathrm{int,off}}$. There is some deviation between the design values and measured values for all voltage levels. This is to be expected, as the design values are ideal and do not take resistor, DC-DC converter, and LDO tolerances into account. For example, for the DC-DC converters used in the prototype, the accuracy of the output voltage changes based with respect to its load current. For situations where the load is low compared to the rated value of the converter, the output voltage can be expected to be higher than the rated output voltage. In the same way, if the load on the DC-DC converter is high, the output voltage can be expected to be lower than the rated output voltage [78]. The digital potentiometers, which are crucial for altering the output

voltage of the LDOs, do not produce the exact resistance values needed for the measured voltages to be equal to the design values.

In Table 4, both voltage level six and seven have the same measured value. This could be caused by a mistake during the assembly process and would have to be taken into account in the control software. In this Master Thesis, this is not an issue because level six and seven in Table 4 are higher in amplitude than the $V_{\mathrm{GG,on}}$ used in the experiments.

The ability of the proposed AGD prototype to control the duration of the intermediate voltage levels was also tested with a DC bus voltage of 0 V. The resulting $v_{\mathrm{GS}}$ waveforms can be seen in Fig. 51. Due to the presence of capacitance and resistance in the gate loop, $v_{\mathrm{GS}}$ cannot change instantaneously. This causes the $v_{\mathrm{GS}}$ slopes seen in Fig. 51 when $v_{\mathrm{GS}}$ changes from −5 V to 15 V or vice versa.

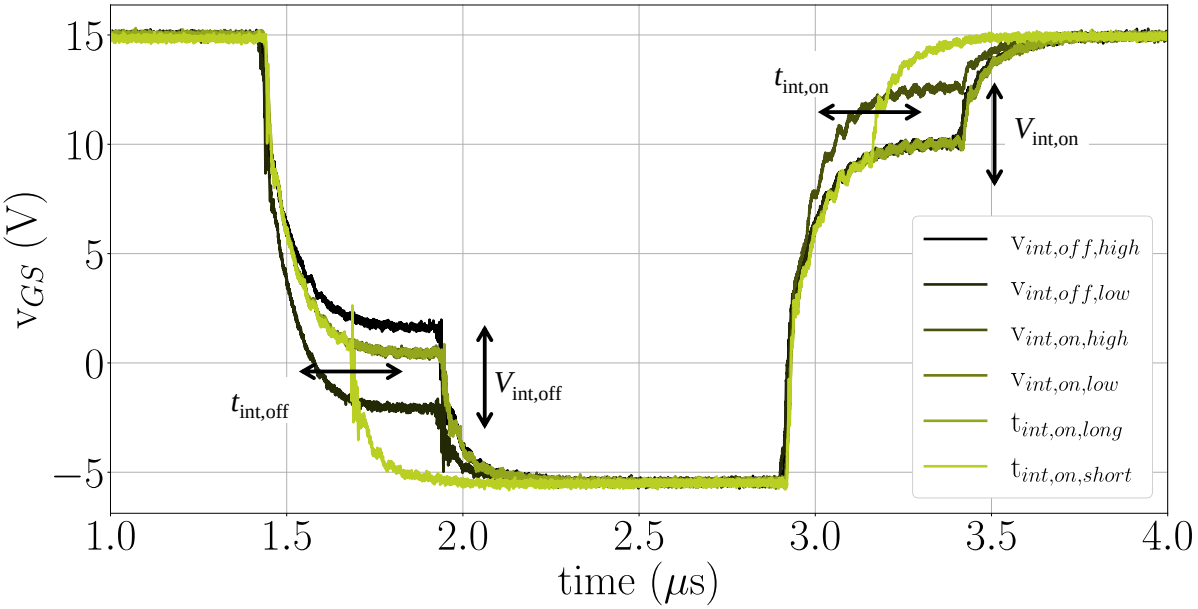



Figure 51: $v_{\mathrm{GS}}$ measurements at $V_{\mathrm{DC}} = 0\,\mathrm{V}$ varying $v_{\mathrm{int,on}}$ and $t_{\mathrm{int,on}}$ with the proposed gate driver

### High Power Experiments

For the experimental DPTs performed in this Master's Thesis, the values seen in Table 6 were used. To process and evaluate the experimental measurements, the functionality presented in Chapter 5 was used.

Table 6: Circuit parameters used during simulations

| $V_{\mathrm{bus}}$ | $I_{\mathrm{load}}$ | $R_{\mathrm{g,ext}}$ | $L_{\mathrm{t}}$ |
|---|---|---|---|
| 800 V | 20 A | 25 Ω | 100 µH |

Table 7 shows the values of $v_{\mathrm{int,on}}$ and $t_{\mathrm{int,on}}$ used in the experimental DPTs. As mentioned in Chapter 5, the oscilloscope used in the experiments can average several measurements before exporting the data. To make use of this feature, 15 samples of the same DPT (using the same $v_{\mathrm{int,on}}$ and $t_{\mathrm{int,on}}$ values) was performed before the average measurement data was exported.

Table 7: $t_{\mathrm{int,on}}$ and $v_{\mathrm{int,on}}$ values used during experiments

| $t_{\mathrm{int,on}}[ns]$ | 20 | 40 | 60 | 100 | 200 | 300 | 400 |
|---|---|---|---|---|---|---|---|
| $v_{\mathrm{int,on}}[V]$ | 7.5 | | | | | | |

The results of the experimental DPTs can be seen in Fig. 52 and 53. These two figures clearly show that the proposed AGD prototype can influence the turn-on switching performance of the DUT by increasing the duration of the intermediate voltage level at turn-on. By increasing $t_{\text{int,on}}$, the voltage and current commutation is slowed down. Comparing the minimal and maximum value of $t_{\text{int,on}}$ used in the experimental DPTs, the aim of the gate driver (described in Chapter 3) is accomplished. $E_{\text{on}}$ can be increased, while the reverse recovery is reduced alongside the voltage and current slopes.

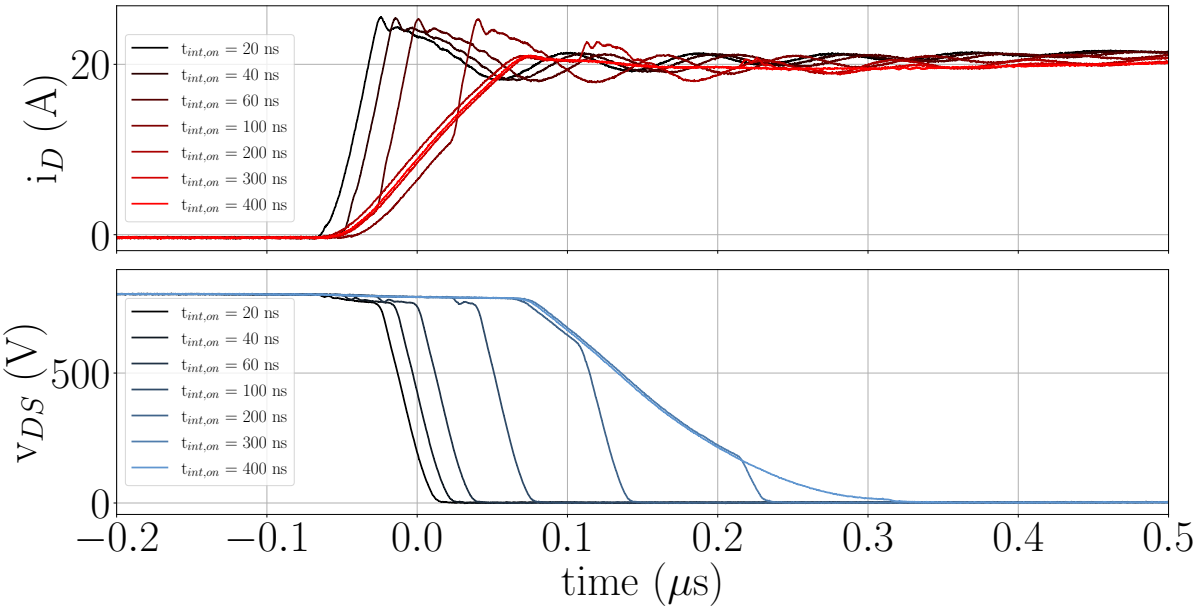
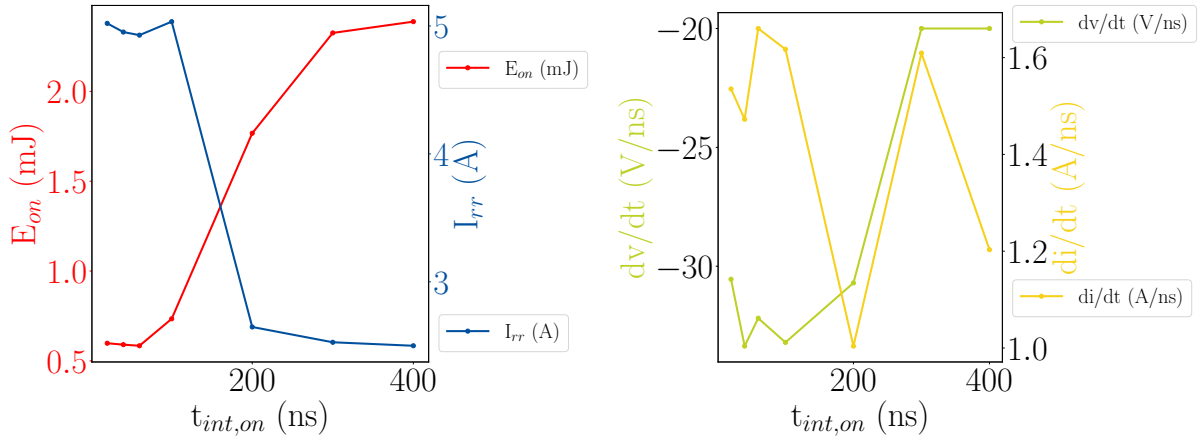



Figure 52: Experimental turn-on $i_{\text{D}}$ and $v_{\text{DS}}$ waveforms showcasing impact of altering $t_{\text{int,on}}$

However, when $t_{\text{int,on}}$ is increased from 200 ns to 300 ns di/dt increases instead of falling in value.




(a) (b)

Figure 53: Experimental MOSFET switching performance indicators

Several differences emerge when comparing the results from the time domain simulations to the experimental results. Compared to the time domain simulations, the time domain plot (Fig. 52) of the experimental measurements shows a clear slow down in both voltage and current commutation. Especially at higher values of $t_{\text{int,on}}$. Voltage and current commutations in the experiment (Fig. 52) are not followed in simulation results accurately, irrespective of which of the three models were used. The manually altered MOSFET model (Fig. 48) is the closest, but in this model, the voltage and current commutation occur faster than in the experiments. This difference becomes bigger at higher $t_{\text{int,on}}$ values.

The difference in commutation speed between the experiments and the manually altered MOSFET model result cause the simulations to underestimate $E_{\text{on}}$, while overestimating $I_{\text{rr}}$, dv/dt and di/dt.

Comparing the datasheets for the C3M0075120K (the DUT in the simulations) [23] and the C3M0075120D (the DUT in the experiments) [94], the C3M0075120D exhibit larger switching losses at similar testing conditions. This is opposite to what is observed when comparing the simulation and the experiments. Not using the same DUT in the simulations and the experiments is not ideal, but as the goal of this Thesis is to investigate the proposed AGD concept, this was deemed acceptable. Another difference between the simulations and the experiments is caused by the fitting method for creating the MOSFET model that is most similar to the experiments. As mentioned earlier in this chapter, the fitting method used to create the fitted MOSFET model is based on static characterization for gate-drain voltages up to 60 V. To make the MOSFET model more similar to the experiments, the fitting method should be used with dynamic characterization data with drain-source voltages up to 800 V.

In the experimental results, oscillations are much more prominent than in the simulation results, especially for $i_{\text{D}}$. This is expected as the electrical components used in the experimental setup are non-ideal. SiC MOSFETs have increased switching speed compared to Si. Increased switching speed causes increased di/dt and dv/dt. This causes resonant circuits, formed by parasitic elements throughout the AGD and DUT platform, to induce voltages and currents. The DUT platform and the AGD prototype was designed to reduce parasitics. However, parasitics can not be eliminated entirely. For example, the tracks in the PCB introduce parasitic inductances. Furthermore, real capacitors also have resistance and inductance, not only capacitance. Measurement devices can also pick up signals which are not the intended signals. This can be mitigated by placing the measurement points as close as possible to what is being measured. As mentioned earlier in this Thesis, the oscilloscope used in the experiments combines measurements from several DPTs. Due to noise not occurring simultaneously for each DPT, averaging several sets of measurement data reduce the impact of noise. This leads to improved measurement quality. The experimental setup also includes additional capacitors to provide voltage stabilization, energy for turn-on and turn-off, and to avoid rapid voltage changes in the control circuitry. This is not taken into account in the simulation model. For example, the power supply is modeled as an ideal voltage source in the simulations. In real life, this is not the case. However, based on the performance of the AGD prototype, the behavior of the circuit is dominated by the devices and the circuit itself. Outer circuitry, such as the power supply used in the experiments, does not seem to influence circuit behavior in a meaningful way.

Overall, the simulations indicate the impact the proposed AGD prototype can have on the switching performance of a discrete SiC MOSFET. However, as the amplitude of the switching performance indicators is considerably different between the simulations and the experiments, more experiments have to be performed in order to verify the ability of the AGD concept to decouple losses and dv/dt and di/dt.

# 7 Conclusion

In the electrification of society, power semiconductors will play an essential part. Silicon carbide, which enables increased switching speed and provides improved thermal capabilities, has become increasingly attractive as a semiconductor material. However, variable load currents can cause lifetime issues in renewable energy sources such as solar or wind energy due to temperature cycling. Therefore, reducing the temperature induced stress caused by temperature cycling would help increase device lifetime and reliability. A gate driver capable of influencing the switching performance of SiC MOSFETs could play a part in reducing temperature induced stress.

This Thesis introduced a four level voltage active gate driver that inserts an intermediate voltage level at the urn-on and turn-off transient of SiC MOSFETs. The intermediate voltage levels can be controlled both in amplitude and duration. Thereby, switching losses, current and voltage overshoot, and current and voltage slopes can be influenced. Being able to influence the switching performance of a SiC MOSFETs, the gate driver presented in this Thesis can be part of an active junction temperature control system. The active gate driver concept presented in this Thesis is based on a literature review performed in the Specialization Project preceding this Thesis.

In order to investigate the ability of the proposed active gate driver concept, a comprehensive simulation study was performed. In this simulation study, over 2400 double pulse tests were performed. Three different models for the C3M0075120K SiC power MOSFET from Wolfspeed were used in the simulation study. In order to perform the DPTs, a half bridge DPT circuit was created in LTSpice, and evaluation functions were created in Python. The circuit and the functions were developed in the Specialization Project preceding this Master Thesis. However, improvements were made for this Master Thesis. From the DPTs simulations, switching losses, voltage, and current overshoots, as well as current and voltage slopes, were calculated. These values were used to study and prove the ability of the proposed active gate driver to influence the MOSFET switching performance. By altering the duration of the intermediate voltage level at turn-on from 20 ns to 400 ns, the turn-on losses was increased from approximately 0.3 mJ to 0.7 mJ.

Experiments were performed to further verify the efficacy of the active gate driver concept. A PCB prototype of the proposed AGD concept was created in Altium Designer. This PCB was assembled and experimental DPTs were performed. The experimental DPTs performed in this Master Thesis were done using a provided half bridge DPT setup and gate driver control software. The C3M0075120D SiC power MOSFET from Wolfspeed was used as the DUT as well as the FD in the experiments. In order to process and evaluate the measurement data obtained from the experiments, the Python functions used for the simulation study had to be adapted to work with experimental measurements. One major challenge associated with this is that oscilloscope Analog-To-Digital Converters (ADCs) introduces noise to the measurement signal. Therefore, the evaluation function needs to feature better noise immunity for experiment measurements compared to simulation results. First, the ability of the AGD prototype to regulate intermediate voltage level amplitude and duration was verified at a DC bus voltage of 0 V. Afterward, DPT experiments were conducted for a single voltage amplitude value and an exemplary range of voltage durations. The turn-on switching transient was examined in these DPTs. The experimental data shows that the AGD prototype can influence switching losses, current and voltage overshoot, and both current and voltage slopes. For example, by altering the duration of the intermediate voltage level at turn-on from 20 ns to 400 ns, the turn-on losses were increased from approximately 0.6 mJ to 2.5 mJ.

# 8 Further Work

More experiments should be performed to investigate further the efficacy of the AGD prototype. This would provide a more complete characterization of the proposed AGD capabilities. As the experiments performed in this Thesis only used one voltage amplitude value, this aspect of the gate driver should be evaluated more thoroughly. In addition, experiments looking at the turn-off switching transient should also be performed. This is essential to confirm that the gate driver concept works for both switching transients.

As mentioned in Chapter 5, a PCB allowing for the AGD prototype to be tested on MOSFET modules were created but not assembled and tested due to time constraints and production delays. This PCB should be finalized, enabling DPTs experiments to be performed with modules. Considering that modules are generally slower to turn on and turn off, the proposed AGD could have an increased impact on modules. Performing DPTs at elevated device temperatures could be done.

As seen mention Chapter 3, the proposed AGD concept is able to change the turn-on driving voltage. This means that the gate driver concept should be able to influence the conduction loss of MOSFETs. However, this was not investigated in this Master Thesis. Therefore, looking into the ability of the proposed AGD prototype should be considered. When it comes to manipulating losses in the device to counteract temperature swings, it would be a valuable tool to influence the conduction losses. However, conduction loss manipulation could also have drawbacks. A thorough examination of this aspect of the proposed AGD would be beneficial in determining the efficacy of conduction loss manipulation.

When the results from the simulation study were compared to the experimental results, it was clear that the simulation model does not adequately depict reality. Therefore, improving the simulation model could be considered. By manually changing some of the parameters in the "fitted MOSFET model", the "manually altered MOSFET model" was created. Comparing these two models to the experimental results, it was clear that the simulation model can be improved to depict reality more accurately. The "fitted MOSFET model" was based on static $i_{\mathrm{D}}$-$v_{\mathrm{DS}}$ characterization data for $v_{\mathrm{DS}}$ up to 60 V. This means that using dynamic characterization data for $v_{\mathrm{DS}}$ up to 800 V instead should lead to a more accurate MOSFET model.

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# Appendix

# PEDG 2022

The following paper is a preprint version of a paper that will be preented at the $13^{th}$ International IEEE Symposium Power Electronics for Distributed Generation Systems in Kiel, Germany on the $26^{th}$ - $29^{th}$ of June 2022.

# Four Level Voltage Active Gate Driver for Loss and Slope Control in SiC MOSFETs

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***Abstract*—Silicon Carbide power semiconductors exhibit fast dynamic behavior. This facilitates the design of high efficiency and high power density converters. However, the resulting current and voltage changing rates demand extensive filtering to avoid electromagnetic interference and ensure safe operation. In addition, temperature fluctuations due to varying load currents from renewable energy sources pose challenges for power semiconductor device lifetime and reliability. Active temperature control can reduce temperature fluctuations, but affects switching slopes simultaneously. This leads to variable electrical stress on both device and circuit level. In this paper, a four-level active voltage-source gate driver for SiC MOSFETs is proposed, enabling manipulation of switching and conduction losses. Switching losses are manipulated by controlling the duration as well as amplitude of intermediate gate voltage pulses during switching transients. Conduction losses can be influenced by adjusting the positive gate voltage. Simulations indicate that the proposed gate driver allows decoupling switching loss and slope control. To validate the gate driver concept, a prototype has been built and evaluated in double pulse test experiments.**

***Index Terms*—Silicon Carbide, WBG, Active Gate Driver, Active Temperature Control**

## I. Introduction

Silicon Carbide (SiC) based Metal–Oxide–Semiconductor Field-Effect Transistors (MOSFETs) exhibit faster switching dynamics and lower on-state resistance for the same blocking voltages compared to their Silicon (Si) Insulated-Gate Bipolar Transistor (IGBT) counterparts [1]. Their fast switching speed means high voltage change rates (dv/dt) and current change rates (di/dt), that can cause strong Electro-Magnetic Interference (EMI), crosstalk, and potentially, a shoot-trough fault [2].

In addition, Renewable Energy Sources (RES) such as photovoltaics and wind power, have an intermittent power generation profile that translates into a varying converter load current. The resulting switching device loss and temperature fluctuations expedite bond-wire lift-off and solder delamination, which are major failure modes in power semiconductor devices [3]. Active Temperature Control (ATC) can reduce the amplitude of temperature stress cycles and thereby improve device reliability and lifetime [4], [5].

Several active gate driver (AGD) concepts that enable ATC by providing power loss manipulation during switching events as well as the conduction phase, have been presented in literature [2], [4]–[9], [12]. Current-source gate drivers allow precise gate capacitance charging and thereby switching transient control [6]–[8]. However, current control necessitates a high precision variable voltage source and a high bandwidth signal path to control it. This is needed to either set the operating point of a current mirror or saturation current source configuration of a semiconductor switch. As a consequence, current source type gate drivers are complex and prone to parameter drift as well as EMI.

Step-wise gate drivers alter the gate charging dynamics by activating a variable number of parallel output stages with different or identical serial resistors [3], [10], [11]. This approach exhibits an easier control than current source gate drivers because unlike controlled current sources, the paralleled output stages are simple topologies, and high precision resistors are easily available. With emerging digital electronics, a large amount of parallel output stages enables fine grain control of the gate charging process [10]. However, large digital bandwidths or complex digital signal sources such as Complex Programmable Logic Devices (CPLDs) or Field Programmable Gate Arrays (FPGAs) are needed on the gate driver, increasing EMI vulnerability. Besides, the necessary circuit layouts and components are both complex and costly.

Multilevel voltage gate drivers offer a compromise between power switch controllability and gate driver complexity. Intermediate voltage pulses with an amplitude between the positive and negative gate voltage during the switching transitions are produced by this gate driver type. Either the amplitude [2] or the timing [9] of these intermediate voltage pulses are controlled. This allows for switching loss, switching slope, and voltage as well as current overshoot control. Controlling either intermediate voltage pulse amplitude or timing however, leaves transient slopes and switching loss coupled and inseparable of each other.

This paper introduces a four level voltage active gate driver capable of manipulating switching losses and transient slopes of a discrete SiC MOSFETs. Variable intermediate voltage levels are supplied to the gate with a configurable duration during turn-on and turn-off. The proposed gate driver can influence the switching losses, switching slopes as well as voltage and current overshoot of SiC MOSFETs, extending the capabilities of earlier presented gate drivers [2], [9]. In addition, conduction losses are controllable by an adjustable positive gate voltage.

The rest of the paper is organized as follows: In Section

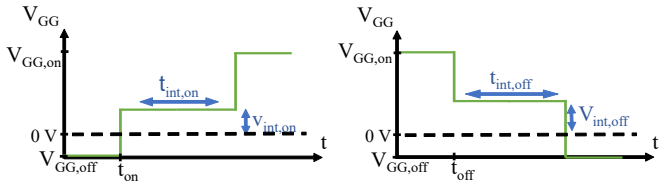



Fig. 1: $V_{GG}$-waveform during turn-on (a) and turn-off (b)

II, the proposed gate driver is introduced and the operational principle is explained. Section III shows the simulation results and IV presents the experimental results. In addition, the impact of the gate driver on the SiC MOSFET performance is discussed and the results are analyzed in these sections. Finally, conclusions are presented in Section V,.

## II. Proposed Four Level Voltage Active Gate Driver

The aim of the proposed active gate driver is to control the switching slopes and the switching loss of SiC power MOSFETs. To achieve this goal, a multilevel voltage gate driver applies an intermediate voltage level during switching that is between the positive and negative driving voltages. Thereby, the gate charging process can be controlled, which in turn influences the voltage and current transitions of the switching device and thus, the switching loss.

Figs. 1a and 1b show the proposed turn-on and turn-off gate driver voltage ($V_{GG}$) pattern. Before the turn-on switching instance ($t < t_{on}$), $V_{GG}$ equals the turn-off driving voltage ($V_{GG,off}$), and the MOSFET is kept in the off state. At $t = t_{on}$, the driver voltage is raised to the intermediate turn-on voltage ($v_{int,on}$). This voltage level is held for the duration of the intermediate turn-on voltage level ($t_{int,on}$). Afterwards, $V_{GG}$ is switched to the turn-on driving voltage ($V_{GG,on}$) and held at this voltage value until the next switching instance. At turn-off, this procedure is repeated. Both the intermediate turn-off voltage ($v_{int,off}$) and the duration of the intermediate turn-off voltage level ($t_{int,off}$) are chosen independently from their correspondents at turn-on.

In a conventional gate driver, a simple step is applied to the gate. Introducing an intermediate voltage step will add a degree of freedom to the gate charging speed. If, for example, a lower intermediate voltage level than the positive gate voltage is applied to the gate at turn-on, the gate charging process is slowed down. Depending on the duration of the intermediate voltage level, the slower gate charging process will slow down the current and voltage transitions. In addition, the switching loss is increased by prolonging the switching process.

Different operation schemes have been presented in literature [2], [9]. These differ from the proposed scheme of driving the multilevel voltage gate driver. Between the intermediate voltage level intervals and the high driving voltage, an interval of low driving voltage is inserted [2], [9] and varied in duration [9].

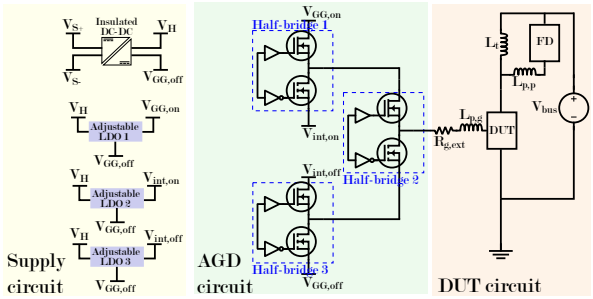



Fig. 2: Schematic diagram of the proposed gate driver

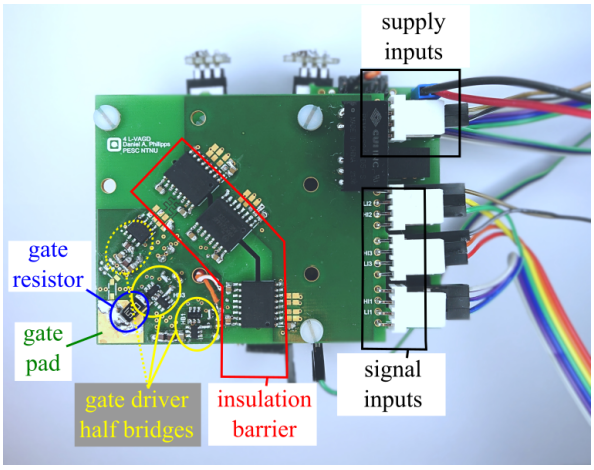



Fig. 3: Photo of proposed AGD. The source pad is located on the back side of the PCB, directly behind the gate pad.

Initially, introducing a variable time delay before the intermediate voltage level was considered. However, simulations showed that altering these time delays had a similar impact to altering the duration of the intermediate voltage levels ($t_{int,on}$ and $t_{int,off}$ in Fig. 1a and 1b). Therefore, the delay variation was not further investigated.

A circuit that can provide the desired voltage pattern has been derived. The schematic diagram of this proposed gate driver is shown in Fig. 2. The gate-drive circuit consists of two parts, the AGD circuit and the supply circuit. As can be seen from Fig. 2, three half-bridge circuits are used to provide the four voltage levels to the gate. Three of the four voltage levels are variable. They are provided by adjustable low-dropout regulators (LDOs), which can be seen in the supply circuit part of Fig. 2. This particularly includes the positive gate voltage, permitting control of the active region of the power MOSFET and thereby conduction losses.

To verify the functionality of the gate driver topology seen in Fig. 2, a gate driver prototype was built and tested. A photo of prototype circuit is shown in Fig. 3. The supply circuit, which is not shown in the picture, is located behind the main gate driver board. The output voltage of each adjustable LDO is controlled using a digital potentiometer inside the LDO

TABLE I: Circuit parameters used during simulations

| $V_{\text{bus}}$ | $I_{\text{load}}$ | $R_{\text{g,ext}}$ | $L_{\text{t}}$ | $L_{\text{p,g}}$ | $L_{\text{p,p}}$ | $T_{\text{amb}}$ |
|---|---|---|---|---|---|---|
| 800 V | 20 A | 25 Ω | 110 µH | 1 nH | 5 nH | 25 °C |

feedback loop. This digital potentiometer is controlled over SPI.

Both the signals required to create the desired patterns and the SPI signals to set the intermediate voltage levels are generated by a C2000 series microcontroller by Texas Instruments [14]. This microcontroller also provides the gate signals for the balancing circuit of the test setup that compensates for any imbalances that result from repeated double pulse tests [21].

## III. Simulation Results

To investigate the functionality and the electrical performance of the gate driver topology seen in Fig. 2, a simulation study was conducted. In this simulation study, hard-switching conditions of a double-pulse test were imposed on a MOSFET model that is driven by a model of the gate driver.

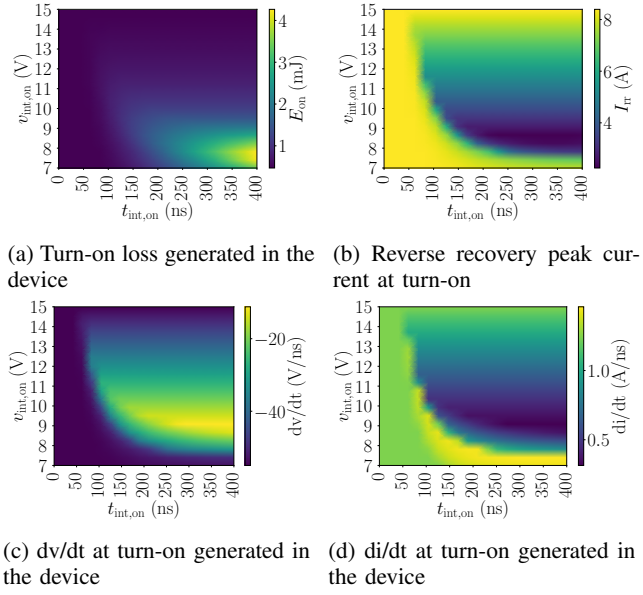
### A. Circuit Modelling

The circuit parameters used in the simulation are summarized in Table I. $V_{\text{bus}}$ is the DC-link bus voltage, $I_{\text{load}}$ the load current and $R_{\text{g,ext}}$ the external gate resistance. The load inductance is $L_{\text{t}}$, while $L_{\text{p,g}}$ and $L_{\text{p,p}}$ are the parasitic inductances in the gate and power loop respectively. $T_{\text{amb}}$ denotes the ambient temperature. A model of the Wolfspeed Silicon Carbide Power MOSFET C3M0075120K was used both as the device under test (DUT) and the free-wheeling device (FD). This model is a modified version of the manufacturer model, optimized for eliminating convergence errors [13].

### B. Gate Driver Modelling

An idealized model of the proposed gate driver was used for the simulations. It consists of an ideal voltage source providing the proposed gate voltage pattern and an external gate resistor. The voltage changing times of the voltage source were set to 1 ns. In a real application, the low power MOSFETs of the output stage are expected to provide slightly slower slopes. However, the power MOSFET input capacitance is so large, that this is expected to dominate the gate voltage dynamics instead of the low power MOSFETs. Hence, modelling the gate driver as described above is considered adequate.

The values of $v_{\text{int,on}}$ were varied from 7 V to 15 V, and $v_{\text{int,off}}$ from $-4$ V to 4 V. The pulse durations $t_{\text{int,on}}$ and $t_{\text{int,off}}$ were varied from 0 ns to 400 ns. The turn-on driving voltage was set to $V_{\text{GG,on}} = 15$ V and the turn-off driving voltage was set to $V_{\text{GG,off}} = -5$ V. The performance of the proposed gate driver was examined by looking at the turn-on switching loss ($E_{\text{on}}$), reverse recovery peak current ($I_{\text{rr}}$), turn-off switching loss ($E_{\text{off}}$), voltage overshoot ($V_{\text{os}}$), dv/dt, and di/dt. $I_{\text{rr}}$ is calculated from the simulation results as the difference between peak reverse recovery current and load current. Similarly, $V_{\text{os}}$ is determined as the peak overshoot voltage minus the DC bus voltage. Turn-on and turn-off transients were investigated separately.




(a) Turn-on loss generated in the device

(b) Reverse recovery peak current at turn-on

(c) dv/dt at turn-on generated in the device

(d) di/dt at turn-on generated in the device

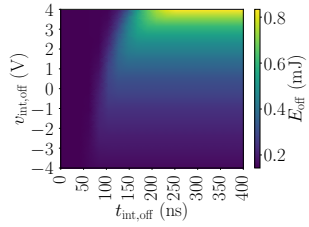
Fig. 4: Influence of $v_{\text{int,on}}$ and $t_{\text{int,on}}$ on performance parameters during turn-on

### C. Simulation Results Discussion

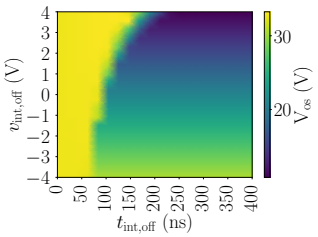
Fig. 4 illustrates various switching characteristics at turn-on under variation of $t_{\text{int,on}}$ and $v_{\text{int,on}}$. From Fig. 4, the impact of altering $t_{\text{int,on}}$ and $v_{\text{int,on}}$ is clearly visible. For some $v_{\text{int,on}}$ values, changing $t_{\text{int,on}}$ has no significant effect on the presented performance parameter values. For $v_{\text{int,on}}$ values $\lessapprox 12$ V, increasing $t_{\text{int,on}}$ leads to higher $E_{\text{on}}$. If $v_{\text{int,on}} \gtrapprox 12$ V, altering $t_{\text{int,on}}$ has a negligible impact on $E_{\text{on}}$. The impact of $v_{\text{int,on}}$ and $t_{\text{int,on}}$ on $I_{\text{rr}}$ and di/dt is very similar. If $t_{\text{int,on}}$ is below approximately 50 ns, changing $v_{\text{int,on}}$ has almost no impact. For the turn-on switching transient, there is a clear region where the AGD is able to impact $I_{\text{rr}}$ and di/dt. This region is where $t_{\text{int,on}} \gtrapprox 50$ ns and $v_{\text{int,on}} \in [\,8\,\text{V}, 13\,\text{V}]$. The behavior of dv/dt (Fig. 4c) is similar to $I_{\text{rr}}$ and di/dt, but the impact of $v_{\text{int,on}}$ and $t_{\text{int,on}}$ is inverted.

Fig. 5 illustrates various switching characteristics at turn-off under variation of $t_{\text{int,off}}$ and $v_{\text{int,off}}$. Altering $t_{\text{int,off}}$ and $v_{\text{int,off}}$ has a similar impact on all four switching characteristics. As can be seen in Fig. 5, there is a range of $t_{\text{int,off}}$ values where altering $v_{\text{int,off}}$ has a negligible impact on the switching characteristics. This range increases with increasing $v_{\text{int,off}}$. At $v_{\text{int,off}} = -4$ V, $t_{\text{int,off}}$ must be greater than approximately 60 ns before a large change in the switching characteristics is observed. When $v_{\text{int,off}} = 4$ V the large change happens when $t_{\text{int,off}} \gtrapprox 175$ ns. In general, $E_{\text{off}}$ and di/dt increases by increasing $v_{\text{int,off}}$, while $V_{\text{os}}$ and dv/dt decrease by increasing $v_{\text{int,off}}$.

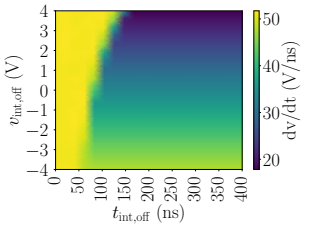
The simulation results show that the proposed AGD enables control of the switching performance of discrete SiC MOS-



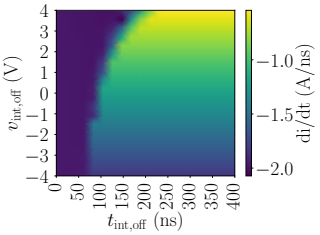

(a) Turn-off loss generated in the device




(b) Voltage overshoot at turn-off




(c) dv/dt at turn-off generated in the device




(d) di/dt at turn-off generated in the device

Fig. 5: Influence of $v_{\text{int,off}}$ and $t_{\text{int,off}}$ on performance parameters during turn-off

FETs. By introducing an intermediate voltage level during switching, the voltage drop across the external gate resistor can be actively lowered. The result is a lower gate current, charging the MOSFET input capacitance more slowly and thus the switching transients are slowed down. Since the external gate resistor is fixed, the amplitude of the intermediate voltage level, i.e. $v_{\text{int,on}}$ or $v_{\text{int,off}}$ respectively, determines the gate current and thus, the switching slope. This can be seen in Fig. 4 for $t_{\text{int,on}} \gtrapprox 75\,\text{ns}$ and $v_{\text{int,on}} \gtrapprox 7.5\,\text{V}$. In this region, changing $v_{\text{int,on}}$ affects the switching slope. Decreasing $v_{\text{int,on}}$ slows down the switching slope causing increased $E_{\text{on}}$ and dv/dt, while reducing $I_{\text{rr}}$ and di/dt. Increasing $v_{\text{int,on}}$ has the opposite effect on the switching characteristic.

The intermediate voltage amplitude is not immediately reflected at the gate of the MOSFET since the external gate resistor and the MOSFET input capacitance form a low-pass filter. Varying the duration of the intermediate voltage level therefore determines, for how long the slowdown described above is in effect, if it is shorter than the time constant of the RC low-pass filter mentioned above. If it is significantly longer, it determines the operating point that the MOSFET is held in with the respective $v_{\text{int,on}}$ and $v_{\text{int,off}}$ values. In Fig. 4 and 5, this impact can be seen. If the duration of the intermediate voltage levels ($t_{\text{int,on}}$ and $t_{\text{int,off}}$) are too short, $v_{\text{int,on}}$ and $v_{\text{int,off}}$ have a strongly reduced influence. This can be seen in Fig. 5, where a short $t_{\text{int,off}}$ value causes $v_{\text{int,off}}$ to have a negligible impact on the switching performance. The duration of $t_{\text{int,off}}$ required for $v_{\text{int,off}}$ to have a large impact on switching performance changes based on the value of $v_{\text{int,off}}$. For values of $v_{\text{int,off}}$ closer to $V_{\text{GG,off}}$, already shorter durations of $t_{\text{int,off}}$ lead to large changes in switching performance compared to more positive values of $v_{\text{int,off}}$. That is because more positive

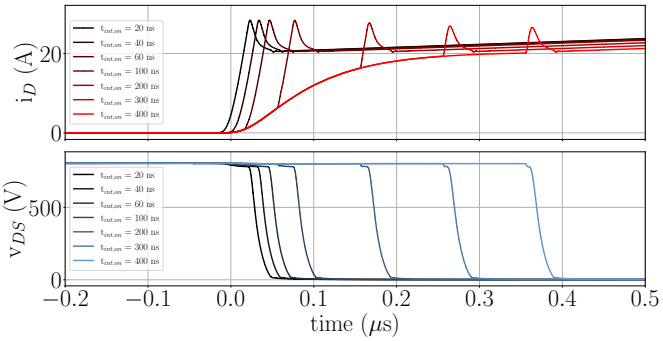



Fig. 6: Simulated drain current ($i_{\text{D}}$) and drain-source voltage ($v_{\text{DS}}$) waveforms under variation of $t_{\text{int,on}}$

$v_{\text{int,off}}$ values slowing down the switching process.

### D. Switching Transient Control

For each switching instance, there are two control variables to manipulate the MOSFET switching performance: $v_{\text{int,on}}$ and $t_{\text{int,on}}$ for turn-on; $v_{\text{int,off}}$ and $t_{\text{int,off}}$ for turn-off. Designing an effective and stable control, the following aspects have to be considered. Controlling the MOSFET behavior requires less precision in the control system in regions, where the controlled variable exhibits small gradients. For example, Fig. 4c shows that for $t_{\text{int,on}} \gtrapprox 250\,\text{ns}$, varying $v_{\text{int,on}}$ from $7\,\text{V}$ to $9\,\text{V}$ has the same effect as varying it from $15\,\text{V}$ to $9\,\text{V}$. However, the gradients are greatly different. As earlier mentioned, high precision voltage control is challenging. Hence, a variation of $v_{\text{int,on}}$ between $9\,\text{V}$ to $15\,\text{V}$ is more desirable for dv/dt control.

On the other hand, to achieve decoupling of the voltage and current slopes (dv/dt and di/dt) and the switching loss, additional requirements on the choice of control variable combinations must be accepted. For the turn-on transient (Fig. 4), $v_{\text{int,on}} \approx 7\,\text{V}$ and $t_{\text{int,on}} \in [\,150\,\text{ns}, 400\,\text{ns}]$, the turn-on energy $E_{\text{on}}$ can be altered without large changes in dv/dt and di/dt by varying $t_{\text{int,on}}$. If $v_{\text{int,on}} \in [\,11\,\text{V}, 15\,\text{V}]$ and $t_{\text{int,on}} \in [\,100\,\text{ns}, 400\,\text{ns}]$, dv/dt and di/dt can be manipulated without incurring large changes in $E_{\text{on}}$. For the turn-off transient (Fig. 5), the voltage and current slopes can be changed without large changes in $E_{\text{off}}$ if $t_{\text{int,off}} \gtrapprox 100\,\text{ns}$ and $v_{\text{int,off}} \lessapprox -2\,\text{V}$.

### E. Exemplary Time Domain Simulation Data Evaluation

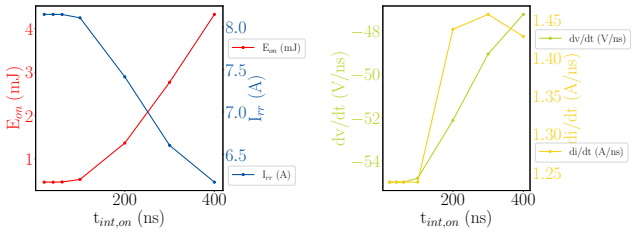
To investigate the accuracy of the simulations and to directly compare simulations to experiments, exemplary time domain simulation data is shown in Fig. 6. The $v_{\text{int,on}}$ and $t_{\text{int,on}}$ values of these simulations equal the configuration of the experiments that will be shown in Section IV.

Based on the waveforms in Fig. 6 $E_{\text{on}}$, $I_{\text{rr}}$, di/dt and dv/dt were calculated in the same way as Fig. 4 and 5. These switching performance parameters can be seen in Fig. 7.

## IV. Experimental Results

### A. Description of the Test Setup and Measurement System

A prototype of the proposed AGD was built and tested with a Wolfspeed C3M0075120D Silicon Carbide Power MOSFET




(a) (b)

Fig. 7: Simulation MOSFET switching performance parameters

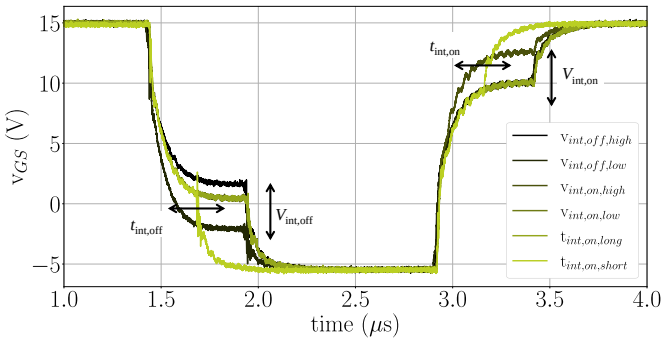



Fig. 8: $v_{GS}$ measurements at $V_{DC} = 0\,V$ varying $v_{int,on}$ and $t_{int,on}$ with the proposed gate driver

[22]. The DUT and FD were mounted on a low inductive test platform that is optimized for dynamic characterization of high switching speed wide-bandgap MOSFETs [19]. This platform has sockets for measuring the gate-source voltage ($v_{GS}$) and $v_{DS}$. $v_{GS}$ was measured using a Tektronix TPP1000 passive voltage probe [16], $v_{DS}$, using a Keysight 10076C passive voltage probe [17]. $i_D$ was measured using a SDN-414-05 coaxial current viewing resistor from T&M Research Products Inc. [15]. The measurements were recorded with a Tektronix DPO5104B oscilloscope [18].

### B. Gate-Source Voltage Measurement

To verify the functionality of the proposed gate driver, experiments were performed with a DC bus voltage of 0 V first. The gate source voltage measurements of these experiments are shown in Fig. 8. Despite the low-pass filtering effect of the MOSFET input capacitance and the external gate resistor, the AGD prototype is able to generate the proposed gate voltage pattern. $v_{int,on}$ and $v_{int,off}$ were varied from low to a high value. $t_{int,on}$ and $t_{int,off}$ were varied from a short to a long duration.

### C. High Power Experiments

An exemplary full series of $t_{int,on}$ values and a single $v_{int,on}$ value were used for the experiments. The experiment parameters are summarized in Table II.

The experiments were performed at a load current of 20 A, a load inductance of 100 µH, a DC-link bus voltage of 800 V,

TABLE II: $t_{int,on}$ and $v_{int,on}$ values used during experiments

| $t_{int,on}[ns]$ | 20 | 40 | 60 | 100 | 200 | 300 | 400 |
|---|---|---|---|---|---|---|---|
| $v_{int,on}[V]$ | 7.5 | | | | | | |

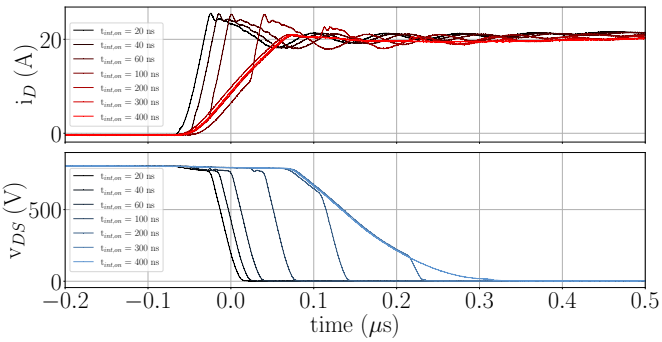
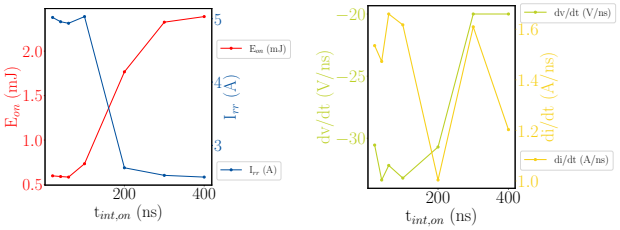



Fig. 9: Experimental turn-on $i_D$ and $v_{DS}$ waveforms showcasing impact of altering $t_{int,on}$

and an external gate resistance of 25 Ω. Time domain measurements are presented in Fig. 9. The performance parameters presented in Fig. 10 are the same as those highlighted in Section III and were defined and calculated in the same way.




(a) (b)

Fig. 10: Experimental MOSFET switching performance parameters

Figs. 8, 9 and 10 prove the ability of the proposed AGD to impact the turn-on switching transient of the DUT. The proposed AGD prototype operates as expected.

Increasing the duration of $t_{int,on}$ has a clear impact on $v_{GS}$ and $i_D$. Especially for higher values of $t_{int,on}$ (300 ns and 400 ns), the proposed AGD significantly reduces voltage and current slopes.

### D. Experiment and Simulation Results Comparison

Comparing Figs. 6 and 9, some differences become clear. In simulations (Fig. 6), the intermediate voltage level at $v_{int,on} = 7.5\,V$ has a purely delaying effect on the voltage commutation, dv/dt remains constant in good approximation. Meanwhile, in experiments (Fig. 9), $v_{DS}$ has a delaying effect on the voltage commutation for small values of $t_{int,on}$, but also reduces dv/dt for higher values of $t_{int,on}$. The drain current, $i_D$ is relatively similar in Figs. 6 and 9 except from excessive oscillations in the experimental results and a higher $I_{rr}$ in the simulations. This is caused by differences between

the simplified circuit model and the real circuit, as well as the SPICE MOSFET and the actual switching device. The circuit parasitics are reduced to a single power loop inductance for the simulation, whereas in reality, multiple parasitic inductances and capacitances are distributed throughout the circuit and interact with each other. Previous work has shown that among other aspects, especially the quasi-saturation and saturation regions are not well represented in manufacturer SPICE models [20]. Simulated saturation currents are therefore lower than what can be found in experiments. This can explain the deviation between simulation and experiment.

## V. Conclusion

This paper presents an active variable four-level voltage gate driver for SiC MOSFETs. Intermediate voltage pulses that are configurable in amplitude and duration, can be applied to the gate during switching and thereby control the switching transients. An extensive simulation study has demonstrated the potential of the proposed gate driver to decouple voltage and current slopes (dv/dt and di/dt) and the switching losses ($E_{\text{on}}$ and $E_{\text{off}}$) to a certain degree, if the control variables ($v_{\text{int,on}}$, $v_{\text{int,off}}$, $t_{\text{int,on}}$ and $t_{\text{int,off}}$) are chosen accordingly.

A prototype of the proposed gate driver has been built and tested on a Wolfspeed C3M0075120D Silicon Carbide Power MOSFET. Sample measurements have been presented in this paper. Both simulation and experimental results show that the AGD is able to control $E_{\text{on}}$, $I_{\text{rr}}$, dv/dt and di/dt in the DUT during switching.

## VI. Acknowledgement

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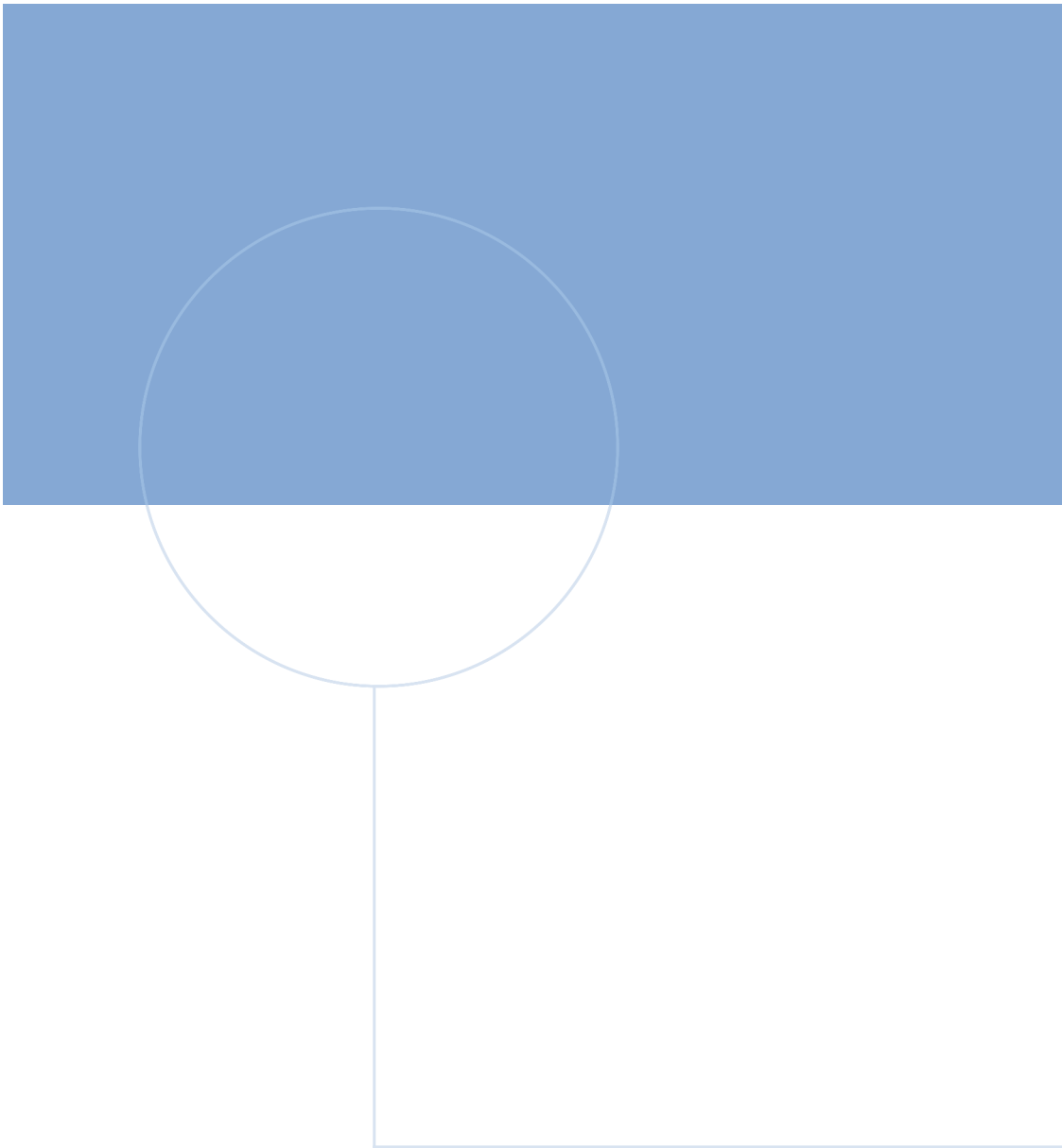

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