Kjetil Langelid

Investigation of series connected SiC MOSFETs in a low inductive layout

Master's thesis in Energy and Environmental Engineering
Supervisor: Dimosthenis Peftitsis
Co-supervisor: Tobias Nieckula Ubostad
June 2022

Master's thesis

NTNU
Norwegian University of Science and Technology
Faculty of Information Technology and Electrical Engineering
Department of Electric Power Engineering

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Sammendrag

I denne masteroppgaven ble to kraft-halvleder moduler designet med mål om å oppnå et lav inductivt design samtidig som det opprettholdes sikker drift under høyspennings- og temperaturforhold. Kraft-halvleder modulene ble designet i ANSYS Electromagnetic Suite.

For å undersøke induktansen til modulene og hvordan ulike faktorer påvirker induktansen, ble programmet ANSYS Q3D Extractor brukt til simuleringer. Forslag til hvordan man kan redusere induktansen er lagt frem og de største kildene til induktansen er blitt identifisert.

ANSYS Maxwell ble brukt for å undersøke de elektriske feltene i modulene, med fokus på bestemme en sikker avstand mellom spenningspotensialene for å hindre overspenninger. Effekten av innkapslingsmaterialer og tykkelsen på det keramiske underlagene fremheves.

For å studere de termiske egenskapene til modulene, ble ANSYS Workbench valgt av programvare. De termiske motstandene til modulene ble simulert med en variasjon av kjøleflenser, og effekten av å flytte chipene nærmere hverandre blir presentert.

For å kunne teste modulene på lab, måtte layouten bli designet i kretskort design programmet, EasyEDA. I lab eksperimentene ble kildene til spenningsubalansen mellom transistorene oppdaget og forslag til hvordan forbedre spenningsbalansen ble presentert.

Abstract

In this thesis, two power modules have been designed with the goal of achieving a low inductive layout while still maintaining safe operation under high voltage and temperature conditions. The power modules were designed in ANSYS Electromagnetic Suite.

To investigate the inductances and how various factors impact the total inductance of the modules, the program ANSYS Q3D Extractor was used for simulations. Suggestions on how to reduce the stray inductance for the designs are made, and the largest sources of the inductance are identified.

In ANSYS Maxwell, the electrical fields in the module were investigated with a focus on deciding a safe distance between voltage potentials to prevent breakdown voltages. The effect of encapsulants and thickness of the ceramic substrates are highlighted.

To study the thermal characteristic of the power modules, ANSYS Workbench was the choice of software. The thermal resistances of the modules with a variation of heatsinks and as the dies were moved closer is presented.

In order to be able to test the power modules in a lab, the power modules were designed in the electric circuit designing program, EasyEDA. In the lab experiments, the sources causing voltage unbalance between transistors connected in series are identified, and suggestions on how to solve these challenges are made.

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List of acronyms

AC	Alternating Current
AlN	Aluminium Nitride
Cu	Copper
DBC	Direct Bonded Copper
DC	Direct Current
DPT	Double Pulse Test
EDA	Electronic Design Automation
FEA	Finite Element Analysis
FEM	Finite Element Method
FET	Field Effect Transistor
HTC	Heat Transfer Coefficient
JFET	Junction-Gate Field-Effect Transistor
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
PCB	Printed Circuit Board
PU	Per Unit
RC	Resistance Capacitance
SBD	Schottky Barrier Diode
SCPM	Super Cascode Power Module
Si	Silicon
SiC	Silicon Carbide
SPICE	Simulation Program with Integrated Circuit Emphasis
WBG	Wide Bandgap

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1 Introduction

In this chapter, the background, the scope, and the structure of the thesis are presented.

1.1 Background

As the demand for power modules with greater power ratings is ever-increasing, the industry is facing problems that require new thinking. Challenges when manufacturing higher power modules are high breakdown voltages, low on-state voltages, and resistances of the modules, dealing with high-frequency switching and enlarged power dissipation as the power levels increases. The conventionally used silicon(Si)-based power modules are reaching their limit with regard to the increasing demand for higher voltages, higher temperatures, and higher switching frequencies. Power devices using silicon carbide (SiC) have an inherent advantage as the material has physical properties that excel under the conditions as mentioned earlier when compared to Si devices. An application area where SiC-devices are starting to overtake the Si-devices is in the electrical vehicle(EV) market[1]. As a result of the highly competitive EV market, the shift from Si to SiC has already begun. Leading EV manufacturer Tesla is already using SiC power module devices in their Model 3, which compels other manufacturers to follow.

Due to the nature of high frequency switching speed, the SiC Metal Oxide Semiconductor Field Effect Transistor (MOSFET) is significantly more affected by the parasitic inductances in a power module package than the Si MOSFETs. The parasitic elements can result in overvoltages and oscillations as the frequency and hence, the dV/dt of the power semiconductor increases. To fully utilize the inherent advantages of SiC, new technologies with clever packaging to reduce parasitic elements and good power dissipation management are crucial. The sources of the parasitic inductances need to be investigated, and solutions on how to overcome the overvoltages and oscillations need to be figured out. Another problem the industry faces as the voltage levels are increasing is the use of SiC MOSFETs connected in series. To reach the desired voltage levels in medium voltage application, SiC MOSFETs in series could be a solution. However, voltage distribution across the MOSFETs could prove to be a challenging problem[2].

1.2 Scope of the Project

The objective of this report will be to gain a better insight into the functioning of the MOSFET by utilizing simulation tools and 3D design technology to investigate parasitic inductances, electric field performance, and thermal performance of a power module. Simulations of the module are performed in ANSYS Q3D to extract the parasitic inductances, ANSYS Maxwell is used to obtain electric field results, and ANSYS Workbench Steady-State Thermal is used to get the thermal characteristics of the module. Lastly, lab experiments are performed to validate the simulation results and to see the capabilities of the designed power modules in this thesis.

1.3 Project structure

This thesis is divided into seven chapters, starting with Chapter 1, which is the introduction of the problem to be investigated and the scope of the project. Chapter 2 presents the advantages SiC inhabits over Si, the theory of the MOSFET operation principles, and the impact of stray inductances on the switching capabilities

of the MOSFET. Chapter 3 presents various state-of-the-art articles used to gain a better understanding of possible solutions which can contribute to solving the challenges presented in the thesis. In Chapter 4, the traditional packaging layout is presented and discussed together with the new designs for packaging layouts made during this thesis.

Chapter 5 introduces the workings and results from simulations of inductances, electrical fields, and thermal capabilities of the new power module designs. Lab experiments to validate the simulated results and investigate the switching characteristic of transistors in series are also presented. Lastly, the results obtained from the simulation and lab experiments are discussed in detail in Chapter 6, and in Chapter 7, the final conclusions of the thesis are drawn, and suggestions for further work are presented.

2 Semiconductor devices

Semiconductor devices have historically utilized Si-based devices in power electronics. However, as the market demands higher efficiency, higher voltages, and higher switching frequencies, the physical properties of silicon are not adequate. SiC has physical properties and characteristics that outperform Si in several critical areas and is increasingly more prevalent in power electronics today. In this chapter, the properties of both Si and SiC will be presented as well as the required theory to understand the workings of MOSFETs.

2.1 Properties of Si and SiC

As previously mentioned, SiC possesses several favorable physical properties with increased voltage and frequency. SiC has various polytypes with various physical characteristics. However, as research suggests the 4H-SiC polytype to be the ideal polytype for power devices, it is natural that this configuration is analyzed and discussed in this project[3].

Table 2.1 shows some of the inherent advantages SiC has over the conventionally used Si. The dielectric breakdown voltages are ten times larger for SiC compared to Si, and the bandgap energy is almost three times larger[4]. The thermal conductivity is over three times greater for SiC compared to Si. Higher bandgap energy results in reduced leakage currents, which, together with high thermal conductivity, allows SiC-based devices to operate under high temperatures. Increased breakdown field strength results in SiC devices having an increase of theoretically ten times that of Si devices. Since the breakdown field strength is significantly stronger, it allows for thinner wafers and, therefore, lower on-state resistance.

Table 2.1: *Silicone and Silicone Carbide electrical characteristics[4].*

Properties/Material	Si	SiC
Breakdown Field $(V/cm) \cdot 10^6$	0.3	3
Thermal Conductivity (W/cm°C)	1.5	4.9
Electron Mobility (cm^2/Vs)	1400	900
Band Gap Energy (eV)	1.12	3.26

2.2 Structural design of MOSFETs

Figure 2.1 depicts the circuit symbol of an n-type enhancement mode MOSFET. The direction of the arrow shows the direction of current flow when voltage is applied over the gate-source terminals. There are two types of MOSFETs, the n-type and p-type, but the p-type is not discussed in this thesis due to lack of relevancy[5].

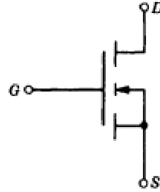


Figure 2.1: *Circuit symbol for n-type MOSFET[5].*

The cross-section of a MOSFET is depicted in Figure 2.2. The MOSFET consists of various types of p- and n-type layers, which illustrates the doping of the layer. As shown, the n+ layers are connected to the drain and source of the MOSFET. The p-layer is also referred to as the body, and the n-layer is the drift region. Notably, the MOSFET structure has three terminals; gate, source, and drain[5].

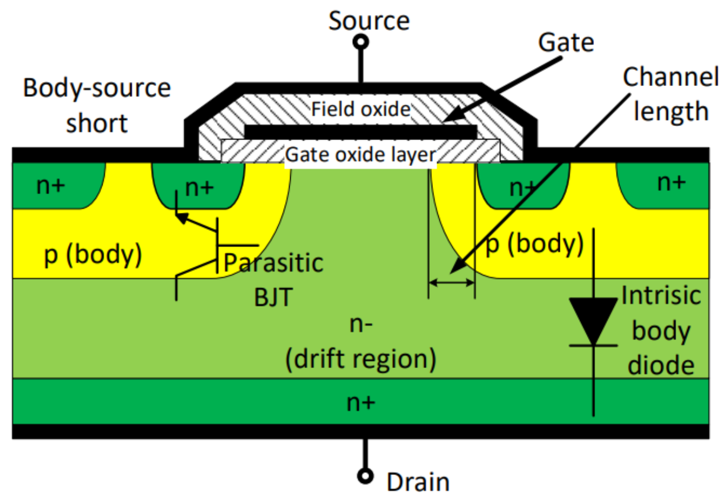


Figure 2.2: *Structure of MOSFET[6].*

The MOSFET gate consists of a gate oxide layer, an insulating region, and the gate conductor. As positive voltage, $V_{GS,1}$, is applied to the gate, a positive charge is formed on the gate. Consequentially, there is formed a negatively charged layer under the gate oxide which can be seen in Figure 2.3. The negatively charged region is referred to as the depletion region and is filled with ionized acceptors[5].

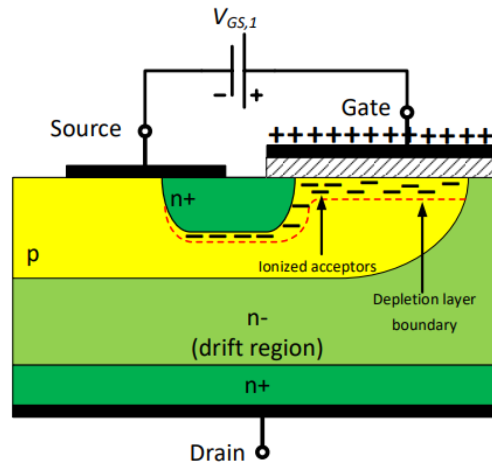


Figure 2.3: *Depletion layer begins forming as voltage, V_{GS1}, is applied at the gate[6].*

Increasing the voltage over the gate results in the depletion layer growing wider. The charge over the gate repels holes in the body region of the MOSFET, and a negatively charged region is formed under the gate. The newly formed region forms an electrical interconnection between the n+ source region and the n- drift region. When a certain level of voltage, $V_{GS,2}$, is applied over the gate is reached, the depletion layer starts filling up with electrons as depicted in Figure 2.4[5].

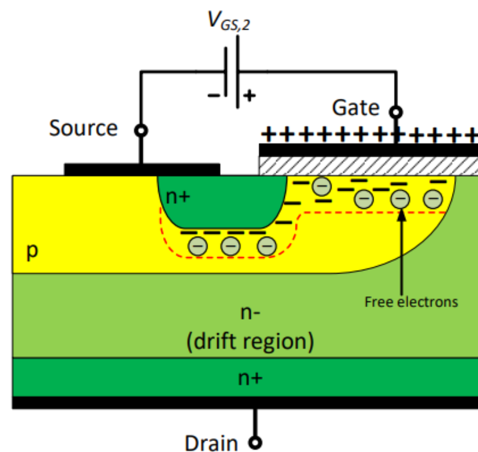


Figure 2.4: *Voltage at gate is increasing, $V_{GS,2}$>$V_{GS,1}$, and free electrons are drawn to the gate oxixe. Depletion layer thickens [6].*

As the voltage keeps increasing to a specific threshold value, $V_{GS,3}$, the depletion layer keeps increasing in width. Eventually, the negative charge density becomes larger than the density of positive holes in the body region. The inversion layer is formed when the negative charge density becomes greater than the density of positive holes, and the region has now effectively become a n- layer. Due to the inversion layer, current can

now freely flow between the source and drain terminals of the MOSFET. Further increasing the voltage results in more current being allowed to flow between the terminals freely, and the on-resistance of the MOSFET decreases.

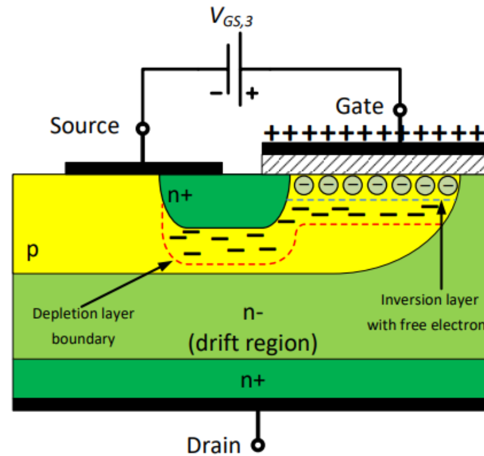


Figure 2.5: *Voltage is increased,* $V_{GS,3}$ > $V_{GS,2}$*, and the inversion layer is created [6].*

2.3 Intrinsic parasitics in the MOSFET

Figure 2.6 depicts the inherent parasitic capacitances of the MOSFET structure. Due to the nature of the MOSFET, the charge will flow between these parasitic as a voltage is applied to the MOSFET. The circuit equivalent of the parasitics is illustrated in Figure 2.7. These capacitances are the gate-source capacitance C_{gs}, drain-source capacitance C_{ds} and gate-drain capacitance C_{gd}[5].

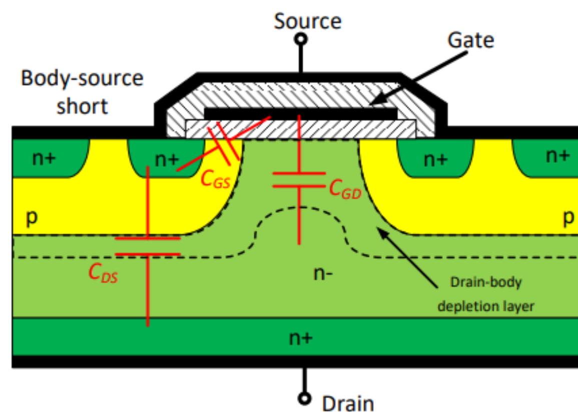


Figure 2.6: *Cross section of MOSFET including highlighting the capacitive connections between the terminals[6].*

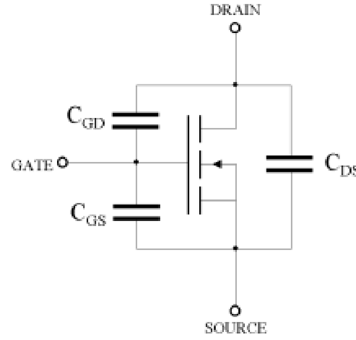


Figure 2.7: *Equivalent circuit for parasitic capacitances in the MOSFET[7].*

The value of the depicted capacitances depends on various physical properties of the MOSFET, such as the width of the drift region, gate oxide layer, and depletion layer. As the regions mentioned earlier depend on the applied voltage, the parasitic capacitances also vary with the applied voltage. Equation 2.1 depicts how capacitance is calculated.

$$C = \frac{\epsilon A}{d} \tag{2.1}$$

Where C is the capacitance, ϵ is the dielectric permittivity, A is the overlap area of the plates, and d is the distance between the plates. In Figure 2.6 it can be seen that the C_{gs} and C_{gd} are dependent on the depletion and gate-oxide layer. Meanwhile, C_{ds} is dependent on the drift layer characteristics.

In the industry and typically on datasheets, the parasitic capacitances are termed by the utilization it performs in applications. Equation 2.2 shows the capacitances C_{iss}, C_{oss} and C_{rss}. Respectively, these capacitances are the input capacitance, output capacitance, and reverse transfer capacitance[8].

$$\begin{gathered} C_{iss} = C_{gs} + C_{gd} \\ C_{oss} = C_{ds} + C_{gd} \\ C_{rss} = C_{gd} \end{gathered} \tag{2.2}$$

2.4 MOSFET switching characteristics

The SiC MOSFET's sizeable cross-sectional area results in a low on-resistance compared to the conventionally used Si IGBT, increasing the device's switching speed significantly. The conventional MOSFET has large recovery currents, which results in substantial losses, especially under high switching frequencies. The SiC MOSFET, when paired with a SiC Schottky diode(SBD), has high-speed recovery and is less prone to higher temperatures than other power devices. The increased recovery performance of the SiC device leads to significantly lower turn-on losses and is another area where the SiC device outperforms the conventional devices[3][9].

2.4.1 Turn on characteristics

The turn on process of the MOSFET can be divided into four intervals and is portrayed in Figure 2.8.

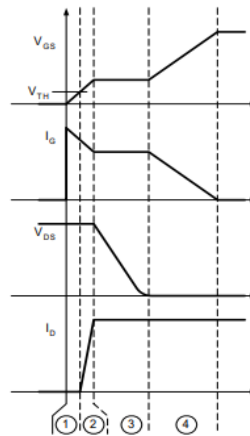


Figure 2.8: *Turn on intervals[9].*

When the switch turns on, the input capacitance of the device starts to charge until it reaches its threshold value. Almost all gate current charges the gate-to-source capacitor in the first interval. However, some current will also flow through the gate-to-drain capacitor, as the voltage over the gate increases, the voltage over the gate-to-drain decreases. Since the drain voltage and current are not affected, the first interval is referred to as the turn-on delay interval[9].

The MOSFET starts conducting current when the voltage reaches the threshold level. However, the voltage keeps increasing until it reaches the Miller plateau. The Miller plateau is when the gate voltage is clamped to a specific value and remains constant until sufficient charge has been added or removed to the device for it to switch. The gate-to-source voltage increases and currents start flowing into the gate-to-source and gate-to-drain capacitors. The drain-source voltage keeps constant at the same level as during turn-off, and the drain current rapidly increases[9].

When the gate voltage is sufficiently charged, the rectifier diode is turned off, allowing the drain voltage to start falling. The gate-to-source voltage keeps constant. As the drain-to-source voltage decreases, the gate current is diverted, and the gate-to-drain capacitor discharges[9].

In the last interval, the voltage applied on the gate of the MOSFET is increased to heighten the conductivity of the device. Since higher gate voltages result in lower internal resistances in the MOSFET, it is beneficial to use voltages above the threshold level. Charging the two gate capacitors guarantees the voltage reaches its highest potential since the current is being split between said capacitors. The drain current keeps stable. However, the drain-to-source voltage decreases to some extent due to the on-resistance decreasing[9].

2.4.2 Turn off characteristics

The turn off process of a MOSFET can be divided into four intervals and is portrayed in Figure 2.9, and is practically backtracking of the turn on intervals[9].

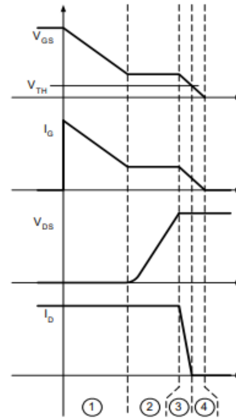


Figure 2.9: *Turn off intervals[9].*

The turn-off process starts by discharging the C_{ISS} capacitance until the Miller plateau is reached. Current flows from the C_{ISS} and through the gate-to-source and gate-to-drain capacitors. The drain current keeps at a constant. Meanwhile, the drain voltage is moderately increasing as the overdrive voltage diminishes[9].

In the second interval, the gate-to-source voltage and gate current remain stable. This is due to the gate current resulting from the charging current from the gate-to-drain capacitor. Drain-to-source voltage increases until the rectifier diode clamp the voltage at its final value[9].

Initially, the internal diode gives the load current another conducting path for the load current. During this interval, the gate-to-drain capacitor is discharging the gate current as it was entirely charged earlier. The gate voltage falls from the Miller plateau until it reaches the voltage threshold. Gate-to-source voltage is decreasing, and drain current quickly falls to zero. Drain voltage keeps constant because of the forward-biased diode[9].

In the final interval, the input capacitor is entirely discharged, and the gate-to-source voltage decreases until it is either zero or negative. The drain voltage and current remain unaffected[9].

2.5 Importance of parasitics on switching performance

The importance of parasitics such as stray inductance and parasitic capacitances is becoming increasingly critical as the frequency of power modules constantly rises to satisfy the demand. Stray inductance leads to overshooting of the voltage and can result in uneven distribution of current, leading to unwanted heating or excessive electrical stress on components. As stray inductance becomes more of a problem with power ratings and frequency increasing, improved power module layouts are required to maximize the potential of the new SiC power dies.

As earlier mentioned, the SiC MOSFET has inherent advantages over the conventional power dies, such as operating with much higher switching frequencies and faster transients. However, as the switching speeds increase, the effect of losses will increase in relation to the frequencies resulting in dealing with the switching losses of the MOSFET, a complex concern. Voltage overshoots become more of a problem as the frequency increases. The solution to the problem is dealing with the stray inductances which cause ringing and overshooting of the voltage.

The most influential parasitics for transistors during switching operation are depicted in Figure 2.10. The parasitic capacitances; gate-to-drain capacitance C_{gd}, gate-to-source capacitance C_{gd} and drain-to-source capacitance C_{ds}, of a MOSFET is depicted together with the internal gate resistance and the stray inductances. The stray inductances are divided into the gate loop inductance L_{gs}, common source inductance L_{cm} and the power loop inductance L_p[10].

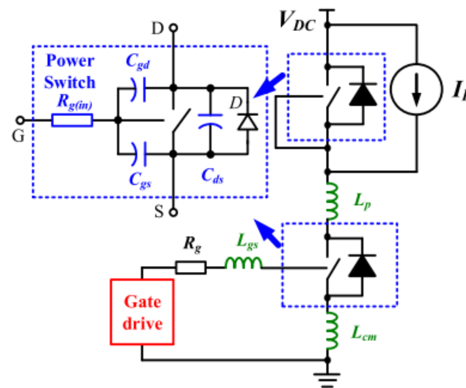


Figure 2.10: *Parasitics in MOSFETs during switching[10].*

Gate loop inductance is the inductance of the bond wires, gate terminals, and the tracks in the DBC. In [11], the gate loop inductance slows down the current coming from the gate drive resulting in increased switching times. During switching, the gate inductance and the gate capacitances could create oscillations, and the inductance delays the gate current. Voltage over the parasitic elements contributes to slower switching as less applied voltage leads to slower switching.

Common source inductance is the inductance that is shared between the main current path and the gate loop. The effects of the common source inductance are that it leads to slower switching speeds and increased

losses. However, as investigated in [12] the common source inductance is negligibly small as the Kelvin source is introduced to the modern packaging.

The power loop inductance is usually the most significant inductance due to the parasitic elements of the bond wires, terminals, and the DBC. Therefore, it typically also has the greatest effect on the switching performance of the module. As the inductance resonates with the output capacitance, it causes ringing and overvoltages during turn-off.

At high switching speeds, the parasitic inductances can result in considerable voltage overshooting during turn-off. Another effect of the parasitic inductances and capacitances is that the stored energy will cause ringing as the energy flows back and forth between the parasitics. Therefore, a low inductive packaging layout is crucial to minimize the voltage overshoot and ringing caused by the parasitics.

3 State of the art

In this chapter, articles describing the state of the modern power module market are presented. New ways of analyzing and designing power modules are gathered from available literature and discussed. Sections especially utilized during the making of this thesis are highlighted. As mentioned in earlier chapters, the most critical issue is dealing with the inherent parasitics while maintaining a highly functional and efficient power module.

3.1 400 A, 1200 V SiC power module with 1nH commutation inductance

The SKiN technology from Semikron is depicted in Figure 3.1. SKiN technology uses silver diffusion sintering joints to replace the bondwires. Additionally, the bondwires interconnecting the topside of the die and the DBC in conventional power modules are replaced with a two-layer sintered flex board. Between the two conducting paths of the flex board, there is an isolating layer to create electrical insulation. The lower layer of the flex board connects the power dies and the DBC. Replacing the conventional bond wires, which account for large inductances, with the sintered flex foil allows for connecting much larger surface areas than bondwires.

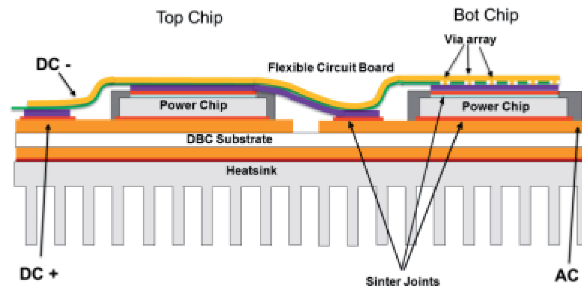


Figure 3.1: *SKiN technology[13].*

The top layer of the flex foils carries the negative DC potential making the DBC layout simple by only including the DC positive and AC potential. As the top layer conducts the DC negative potential and the bottom layer conducts the DC positive layer, the layout results in a very low inductive design as large areas carrying opposing current overlap. Due to the opposite current flows, the magnetic flux cancellation effect cancels out the electrical fields generated by each conducting path. The result can be observed in Figure 3.2, where the current density of the top layer is concentrated in areas where the two conducting layers overlap.

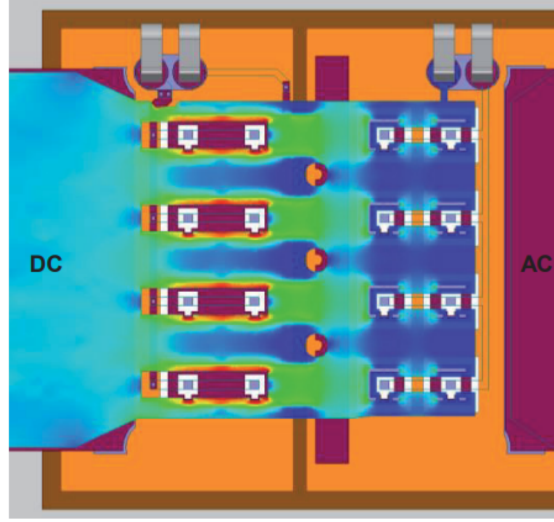


Figure 3.2: *High-frequency current distribution over the simulated SKiN power module[13].*

3.2 A Lumped Thermal Model Including Thermal Coupling and Thermal Boundary Conditions for High Power IGBT Modules

This article presents a solution to make more efficient and precise thermal models by utilizing a lumped three-dimensional thermal model. Finite Element Method(FEM) is used to solve the geometry by dividing it up into a finite number of elements and solving differential equations to get realistic results. For thermal simulations, there need to be specified boundary conditions. In this case, the chip is classified as the heat source, and the heat sink is the cooling system. The thermal characteristics of the module are calculated by solving the differential equation Equation 3.1.

$$\frac{\partial}{\partial t}T(x,t) - \alpha \Delta T(x,t) = \frac{q_{\text{loss}}}{C_p \rho}, \quad \alpha = \frac{k_{\text{th}}}{C_p \rho} \tag{3.1}$$

Where T is the temperature at a specified point at a specific time, k_{th} is the thermal conductivity, C_p is the thermal capacitance, and ρ is the density of the material at a point, q_{loss} is the power loss density. Equation 3.1 shows that the temperature is a function of the power loss density.

ANSYS Icepak was used to simulate the geometry with regard to the heat equation. ANSYS Icepak uses a numerical solver, Fluent, to solve the equations after the project model has been through the meshing process. The meshing divides the model into smaller geometries to simplify the process when the differential equations are applied. The temperature difference is divided by the total power dissipation to calculate the thermal impedance between two nodal points. The nodal points are usually positioned in the most critical areas where most faults transpire. These areas are the interconnection between the bondwires and the DBC and the thin soldered layers. In [14], the nodal points are distributed through the layers of the module, which are depicted in Figure 3.3.

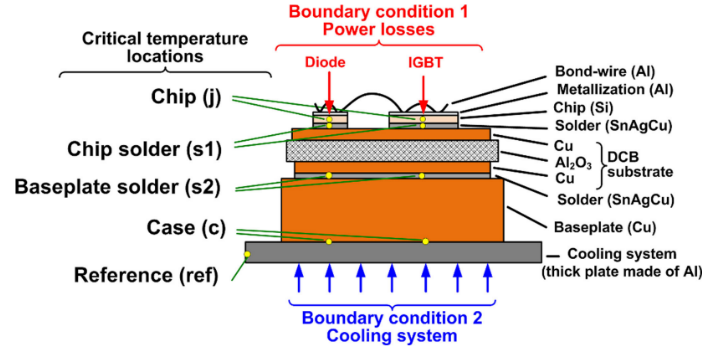


Figure 3.3: *Layers and boundary conditions for the IGBT module[14].*

In the article, various simulation methods where the FEM modeling is simulated with various heatsink and heat sources are studied to understand better how it affects the results. Firstly, a heatsink with a fluid cooling system is investigated. Different cooling mechanisms are examined for the heat sink. Each cooling mechanic is extracted by using the heat transfer coefficient(htc) of the cooling system and modeling it as a plate absorbing the heat dissipated. The htc represents how much heat is transferred per area and ΔT between the fluid dissipating the heat and the heat source, which is solid in this case. To calculate the value Equation 3.2 is used.

$$\text{htc} = \frac{q}{\Delta T} \left(\text{W/m}^2\ \text{K} \right) \tag{3.2}$$

Where q is the heat flux and ΔT is the difference in temperature between two surface areas. The transient thermal impedances are then extracted for different htc values. Simulations with various fluid cooling systems demonstrated the case to reference layer as the module's most affected layer.

Continuing, the heat sink was simulated with fixed case temperatures. Instead of the htc being modeled as a plate in the aforementioned simulations, the plate is now set as a fixed case temperature. Two ways of defining the boundary conditions are using conductive heat transfer with constant temperature or convective heat transfer with the corresponding htc. As constant case temperature is hard to achieve in practice, the latter option is chosen. Results revealed the junction to chip solder connection to be the most influenced section when the boundary, as mentioned earlier conditions are applied. These results are explained by a temperature shock being injected into the module resulting in the heat not propagating to the lower layers. Therefore, the most affected sections are the upper layers.

Lastly, the simulations are performed with a varying heat source where the htc is set to a constant value, and the power dies apply a variation of power losses. The simulation results show the section between the junction to the chip solder to be the most influenced section of the module.

FEM simulations can be time-consuming depending on the accuracy of the meshing and dependent on the duration of the profile being simulated. Therefore, thermal resistances in critical areas are extracted and modeled to a lumped RC thermal network. The lumped thermal network allows for accelerated simulations due to the simplified equivalent electrical elements being less complex than 3-D modeling.

3.3 Overview of Digital Design and Finite Element Analysis in Modern Power Electronic Packaging

The importance of digital design during the investigation of power module design is highlighted in [15]. To better understand new and complex packaging technologies, utilizing finite element analysis(FEA) makes the task simpler. Different differential equations can be solved to obtain thermal expansion, mechanical stress, and electrical and magnetic field. To simplify this task, FEA splits the geometries of the model into smaller parts referred to as finite elements. As packaging becomes increasingly denser, the ability to do accurate measurements also becomes increasingly more difficult due to the intrusive nature of current measurement. Increased resonance frequency due to dense packaging leads to the bandwidth being out of the scope of many conventional measurement tools. Several other factors also cause accurate measurements to be increasingly more difficult. Therefore, FEA simulations can be a solution where measuring tools are inadequate.

ANSYS Q3D Extractor inhabits three ways of addressing parasitics to obtain parasitic elements. Figure 3.4 shows Method A, B, and C, respectively. Method A calculated the parasitics by analyzing each trace individually. Due to Method A excluding the mutual coupling effect between inductances, it is only recommended for low switching frequencies where electric and magnetic cancellation is negligible. Method B investigates each loop carrying current and includes the electric and magnetic fields. Considering the entire loop could lead to misleading results when modeling the equivalent circuit. In Method C, both previous techniques are applied as the inductances are calculated with Method A, and the coupling effect between the inductances is considered as in Method B. The drawback of Method C is the difficulty of calculating the proper loop inductances.

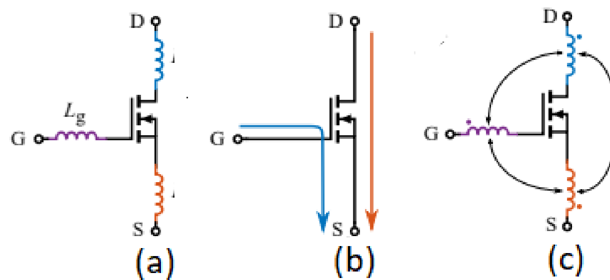


Figure 3.4: *(a) Self inductance method. (b) Current loop method. (c) Mutual coupling and self inductance method[15].*

As the power module market increasingly demands higher voltage devices, electrical fields' effects become even more critical. In finite element simulations, the electrical fields are highly dependent on the meshing of the model. Increasing the accuracy of the mesh is vital to get more realistic results. However, in [15], it is revealed that finer meshing could result in the calculated electrical field strength being unrealistic due to the field crowding. Field crowding is a phenomenon depicted in Figure 3.5. In the two areas A_1 and A_2, the same electrical fields are applied, yet the electrical field calculated in A_2 is higher because the area is smaller. Therefore, the field crowding effect has to be carefully considered during simulations.

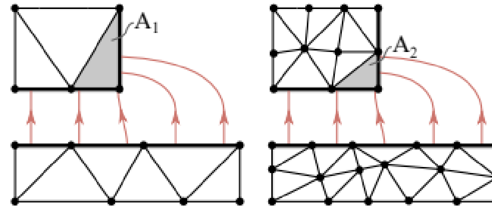


Figure 3.5: *Field crowding effect as a result of finer meshing of geometry[15].*

Lastly, it should be noted that slight differences between the simulation model and the real-life device should always be taken into account. Surface roughness leading to small voids could potentially be sources for partial discharges. Discharges lead to deterioration of the surface properties and skew results.

3.4 6.0kV, 100A, 175kHz super cascode power module for medium voltage, high power applications

In Figure 3.6, the electrical schematic of a serial string of SiC JFETs with a balancing circuit is depicted. The transistors denoted with gate and source are the controlling MOSFET Q7. The resistance, R1, initiates a bias current for the diodes in the balancing circuit. Hence, the static balancing voltage for the circuit is set. The rise and fall times of all the switches, Q1-Q5, can be varied by changing the resistance values R2-R6. Due to the nature of switches in series, the JFET closest to the gate and source terminals will dissipate significantly more power than the other JFETs. Therefore, the balancing setup shifts voltage away from the lowest JFET in the stack. The power dissipation is more evenly spread out throughout the power module by spreading out the voltage.

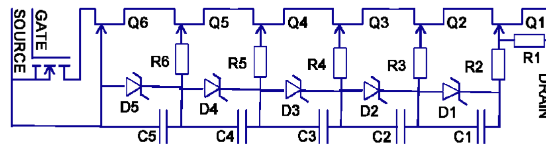


Figure 3.6: *Electrical schematic of the SCPM[16].*

Connecting the JFETs in a serial connection would result in varying switching times due to the variable capacitances referred to ground for each JFET. Therefore, capacitances with varying sizes are connected to each JFET's gate terminal to synchronize the JFETs. The charge flowing through the capacitors flows to the stored charge in the drain junction of the JFETs. Due to the capacitors of the balancing circuit being connected in series, the charge flows from the highest potential down to ground through the capacitors. When calculating the capacitor values, the drain-source charge, Q_{DS}, was assumed to be 300nC, with a 1kV reference value over each transistor. Therefore, the capacitance of Q1 was set to 300pF and increased with 300pF for each step in the circuit. According to [16], the actual bus voltage is lower than the designed value. Therefore, the lower JFETs were intentionally set to block lower voltages to transfer losses to JFETs in the upper part of the stack.

In Table 3.1 the switching losses of each JFET together with the voltages over the transistors are presented. The switching losses over the lowest JFET, Q6, in the structure dissipate significantly more power than the other JFETs. Higher in the circuit, the switching losses of the transistors decreases, ending at roughly half the switching energy over Q1 compared to Q6. Excluded from the electrical circuit schematic, there is a controlling MOSFET Q7, deciding the turn off of the devices. The MOSFET is needed as JFETs are naturally turned on. Connecting the MOSFET in series allows for a naturally off module which is safer to operate.

Table 3.1: *LTSpice simulations showing switching losses and voltages across JFETs and the MOSFET[16].*

	Q1	Q2	Q3	Q4	Q5	Q6	Q7
$E_{sw}(mJ)$	479.2	658.9	776.6	847.6	808.6	1008	5.47
$V_{off}(V)$	1253	1076	976	923	863	890	16

In Figure 3.7 the rise and fall over each JFET and the controlling MOSFET is presented. The voltage distribution over the transistors is very balanced for the SCPM structure.

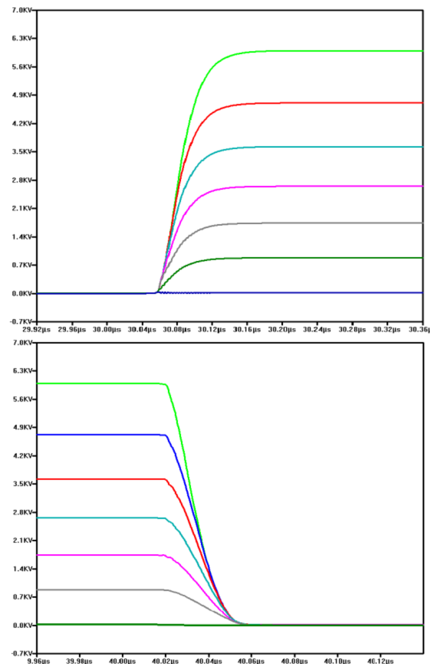


Figure 3.7: *Rise/fall of voltage over the JFETs and the MOSFET[16].*

The most beneficial aspect of the Super Cascode power module is the advantage of utilizing JFETs in series to increase the voltage level of the package. Meanwhile, the controlling MOSFET determines the switching, and only one driver circuit is therefore required. The single controlling MOSFET removes the problem of gate impedance matching and propagation delay skew that occurs as several gate drivers are introduced.

4 Design of SiC power module packages

This chapter presents and discusses the conventionally used packaging method for power modules. Following, the packaging designs developed for this thesis are presented and explained in detail. As mentioned in earlier chapters, the thesis aims to enhance the packaging layout to better utilize the inherent benefits of SiC over the traditionally used Si. SiC-based devices allow for higher switching frequencies, temperatures, and voltage, thus making the design process of the power module even more important to utilize SiC to its utmost capability. Higher switching speed leads to stray inductances having a more significant impact on the performance capability of the power module. Higher voltages mean that the rated power of the power modules is increased, but as voltage increases, the risk of breakdown voltages has to be taken into account. Balancing the geometries and distancing between components within the module is a complex task when all the factors mentioned above have to be considered.

4.1 Traditional packaging layout

In Figure 4.1 the most conventionally used power module configuration is presented[17]. The baseplate absorbs heat from the substrate while also offering structural support for the substrate. The heat sink is usually connected to the baseplate to improve the heat dissipation of the module further. The substrate is a sandwich structure with direct bonded copper(DBC) on the top and bottom layer and an electrical isolating ceramic layer between the DBCs. The substrate, usually ceramic and, in this design, AlN, operates as an insulator that electrically separates the top and bottom layer and has good thermal conductivity to transfer heat to the baseplate. The copper layer on the top of the substrate ensures the electrical path with the power dies of the module soldered onto this layer. The power semiconductors are the heat source during operation and produce the majority of the heat.

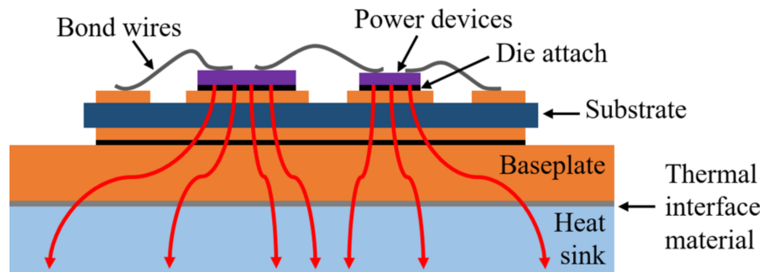


Figure 4.1: *Cross-section of conventionally used power module[17].*

The power dies usually have their drain on the bottom of the die and is connected to the aforementioned top copper layer through soldering. The gate and source connections are on the top of the power die and are electrically connected to the gate terminal and top copper layer with bonding wire. The upper parts of the power module are often encapsulated with materials like epoxy or silicon gel. Encapsulant is used to protect the devices of the module from unwanted environmental conditions such as moisture or dust. Furthermore, the encapsulants have higher dielectric breakdown voltages than air, resulting in more compact packaging being possible, which could lead to lower inductance and less loss. The structure and arrangement of the components in the power module determine the module's capabilities, and it is essential to design the

layout to best enhance the module's effectiveness. Therefore, the geometry and arrangement of components are crucial to getting as small parasitics as possible while keeping safe distances between various voltage potentials and ensuring that the power module has sufficient thermal management during operation.

4.2 New designs for packaging layouts

To fully utilize the inherent advantages SiC-based devices have over the conventionally used devices, the objective of the designed packaging layouts was to reduce parasitic inductances while ensuring safe operation in high voltage and temperature environments.

4.2.1 General designs of the new modules

The designed modules have a power loop where four SiC MOSFETs are connected in series. Each die has one designated copper island, and the return path for the current is made of copper. The return path is either placed straight above or under the top layer of the DBC and will be explained more in detail later in this chapter. The power semiconductors chosen are "CPM3-1200-0021A Silicon Carbide Power MOSFET" from Cree[18], but are only simulated as either copper or silicon depending on whether they are in their turn on or off state in simulations. The gap between each copper island of the DBC was set to 2.5mm to ensure safe operation without any voltage breakdowns between different voltage potentials. In later chapters, there will be simulations where the gap distances are reduced to observe the effect it has on the stray inductance, the electrical field strength, and the thermal capabilities of the module.

Bondwires connect the top of the die, the source of the die, to the copper island of the next die, which is on the same voltage potential as the drain of the MOSFET. Bondwires are the most universally used interconnection method for power modules. However, because of the high self-inductance of the bondwires, the parasitic inductances may limit the functionality of the module. According to [19], as the number of wires coupled in parallel increases, the parasitic inductance of the bondwires significantly decreases. Meanwhile, the resistance of the bondwires also decreased as the wires were connected in parallel. Consequently, the bondwires were placed as close as possible while still following the recommended pad sizing for each bondwire. The bond wires are eight bondwires made out of aluminum connected in parallel interconnecting the power loop where each bond wire has a diameter of 200 µm. According to [20], the typical fusing current for each bond wire is 11-12A resulting in the bondwires being capable of carrying currents up to 88-96A, which is in line with the rated current for the chosen power dies[18] where the drain current varies from 100A to 74.5A depending on the temperature. Eight bondwires were the maximum amount possible to fit along the die when taking the recommended pad size into account[20].

From the previous specialization project[21], it was discovered that RC snubbers were crucial when the transistors were connected in series. Therefore, an RC snubber was connected in parallel with the copper islands of each die. The RC snubber improves the performance of the switching by dampening ringing and reducing the voltage spikes. However, during simulations, the RC snubbers are not included, due to representing them as pure copper gave unrealistic results and were therefore excluded. Gate terminals are located on the right-hand side of the electrical conduction path but were excluded from simulations due to not carrying current as simulations of the power loop were performed. To get a low inductive internal commutation path, the return path is placed (above or) under the electrical path of the DBC in both designs,

making the commutation current flow in opposite directions. As the current conducting areas flow in opposite directions and overlap, the mutual inductance of the paths increases, and the effective inductance is decreased. In Equation 4.1 the relation between the effective inductance, the self-inductances, and the mutual inductance is shown.

$$L_{\text{module}} = L_{l1} + L_{l2} - 2M_{l1l2} \tag{4.1}$$

L_{module} is the total effective power loop inductance of the module, L_{l1} and L_{l2} are the self-inductances of the upper and lower current paths, and M_{l1l2} is the mutual inductance between the two current paths. To gain a very low inductive design, it is essential to keep the self-inductance low and have a good mutual inductance connection between the current paths.

Both the Halfbridge and NegativeLayer packaging layouts were partly inspired by the SKiN technology[13]. Both designs use overlapping current paths to utilize the magnetic flux cancellation to high a high mutual inductance between the paths. However, the layouts do not utilize the sintered two-layer flex board due to problems with implementing the flex board geometry in simulation software and not having the ability to recreate it for the lab experiments. Another reason for using the conventional bondwiring was because the "HB30 Heavy Wire Bonder"[22] was supposed to be used to create the bondwires. However, due to an error when soldering the dies on top of the DBC in the "Elprolab", the lab experiment was never carried out at NTNU. The faulty DBC is depicted in Figure 4.2, where the substrate has cracked, possibly due to the difference in thermal expansion between copper and AlN. The experiments were instead carried out at EFD Induction as a backup plan. However, during the lab experiments at EFD Induction, the SiC FETs, UF3SC120040B7S[23], were utilized as it was the only available option at EFD Induction and the PCB made were slightly changed to be compatible with the TO-263-7L package of SiC JFET die. EFD Induction is a company making products for induction heating, based in Skien.

(a)

(b)

Figure 4.2: *Soldering error at "Elprolab" at NTNU causing the substrate to crack.*

4.2.2 Halfbridge packaging layout

The final design of the Halfbridge model is depicted in Figure 4.3. The return path of the current is placed directly above the DBC to get as much magnetic field cancellation as possible. The return path is transparent in order to see the entire layout. The distance between the return path and the top of the bondwires, the highest point on the top DBC, is set to 2.5mm to ensure no voltage breakdowns. In later chapters, the distance will be varied to see the impact it has on the total power loop inductance of the model.

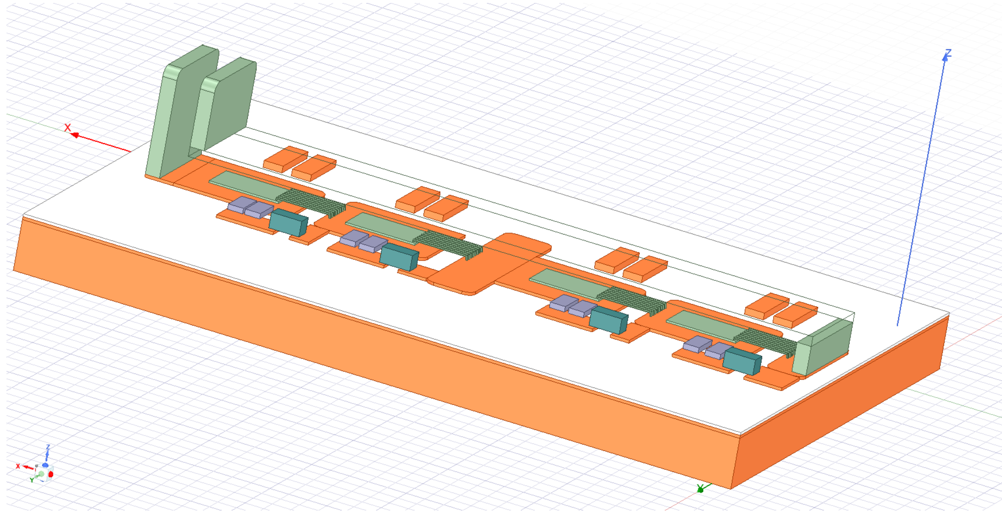
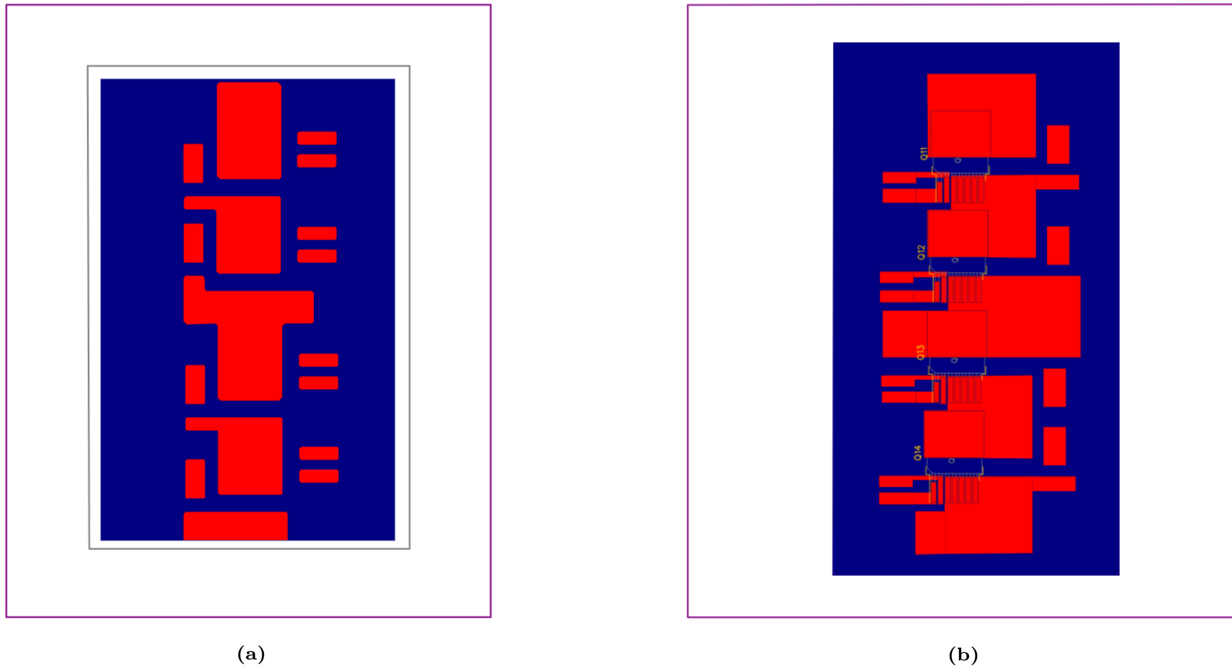


Figure 4.3: *Halfbridge model designed in ANSYS Electromagnetic Suite.*

To be able to order the DBC of the Halfbridge module, the layout of the DBC had to be designed in an electronic design automation(EDA) program. Due to previous experience, the program EasyEDA was used to design the DBC layout. In case of fault during the recreation of the power module at NTNU, another design was also created to specifically fit the UF3SC120040B7S SiC FETs that were available at EFD Induction for testing. The finished designs are depicted in Figure 4.4, where the originally created DBC design is (a), and the specifically designed layout for testing at EFD Induction is (b).



(a) (b)

Figure 4.4: *Halfbridge model designs in EasyEDA with the model tested at NTNU on the left(a) and the model tested at EFD Induction on the right(b).*

In Table 4.2, the thicknesses of each layer are presented. In this thesis, the solder layers and the metallization on the sides of the dies are left out due to complications in simulations and not affecting the parasitics to any significant degree. The sizes of conventional power modules influence the outer dimensions of the power modules designed. However, as the primary goal of the thesis is to make a low inductance power module, the outer dimensions were slightly decreased. The Halfbridge module width and length are 50 and 76mm, respectively.

Table 4.1: *Thicknesses of the layers in the Halfbridge model.*

Layer	Material	Thickness (µm)
SiC MOSFET	Si/SiC	200
Copper islands	Copper	300
Return path	Copper	1000
DBC ceramic	Aluminium Nitride	630
DBC baseplate	Copper	5500

In Figure 4.5, the current paths of the Halfbridge model are depicted. The conducting top DBC layer will be referred to as the positive path, and the sink terminal will be referred to as the return path.

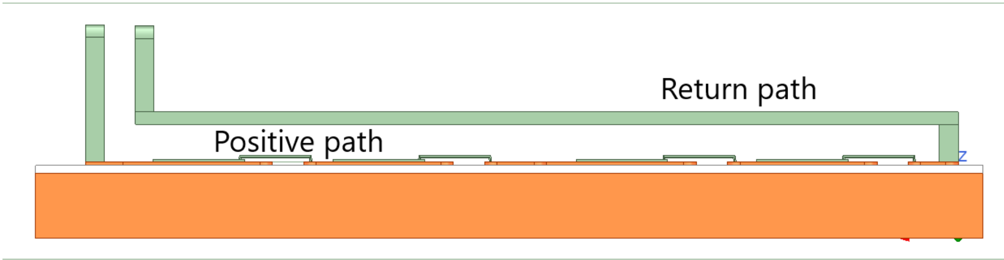


Figure 4.5: *Current paths in the Halfbridge model.*

4.2.3 NegativeLayer packaging layout

The NegativeLayer module is depicted in Figure 4.6 and utilizes the phenomena of magnetic field cancellation between the positive and return current paths. However, in the NegativeLayer layout the return path for the commutation current is located under the top side DBC with a layer of AlN sandwiched in between. Notably, the NegativeLayer module requires two ceramic substrate layers, which could lead to larger thermal resistance. The thermal resistance will be investigated in detail in the thermal analysis chapter.

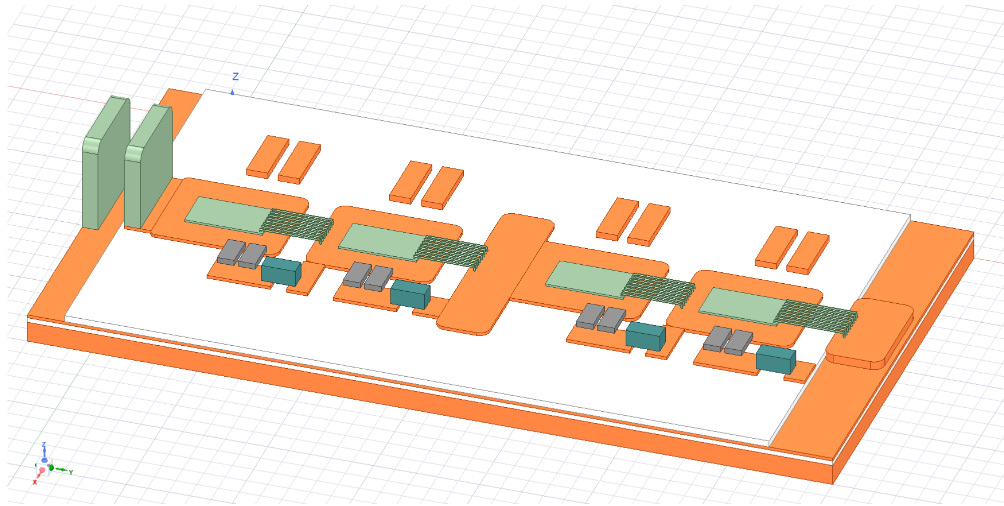
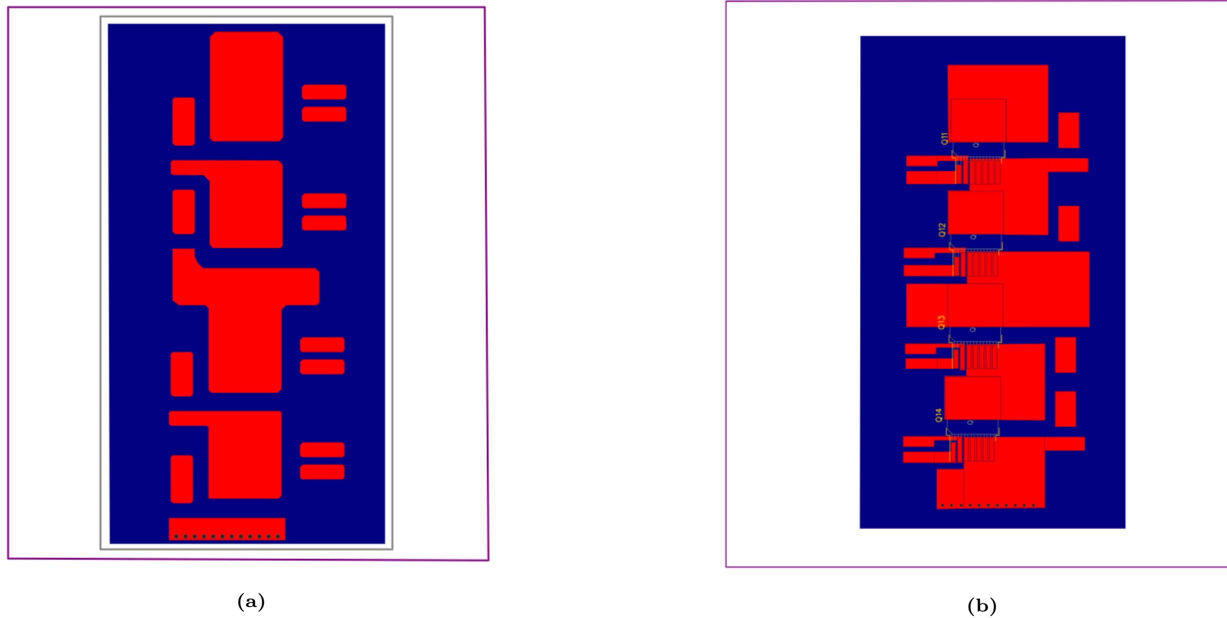


Figure 4.6: *NegativeLayer model designed in ANSYS Electromagnetic Suite.*

To be able to order the DBC of the NegativeLayer module, the layout of the DBC had to be designed in an electronic design automation(EDA) program. The finished designs are depicted in Figure 4.7, where the originally created DBC design is (a), and the specifically designed layout for testing at EFD Induction is (b).



(a) (b)

Figure 4.7: *NegativeLayer model designs in EasyEDA with the model tested at NTNU on the left(a) and the model tested at EFD Induction on the right(b).*

In Table 4.2, the thicknesses of each layer are presented. The NegativeLayer module width and length are 40 and 76mm, respectively.

Table 4.2: *Thicknesses of the layers in the NegativeLayer model.*

Layer	Material	Thickness (µm)
SiC MOSFET	Si/SiC	200
Copper islands	Copper	300
Return path	Copper	300
DBC ceramic	Aluminium Nitride	630
DBC baseplate	Copper	4000

Figure 4.8 the current paths of the Halfbridge model are depicted. The conducting top DBC layer will be referred to as the positive path, and the copper layer under the first ceramic substrate from the top will be referred to as the return path.

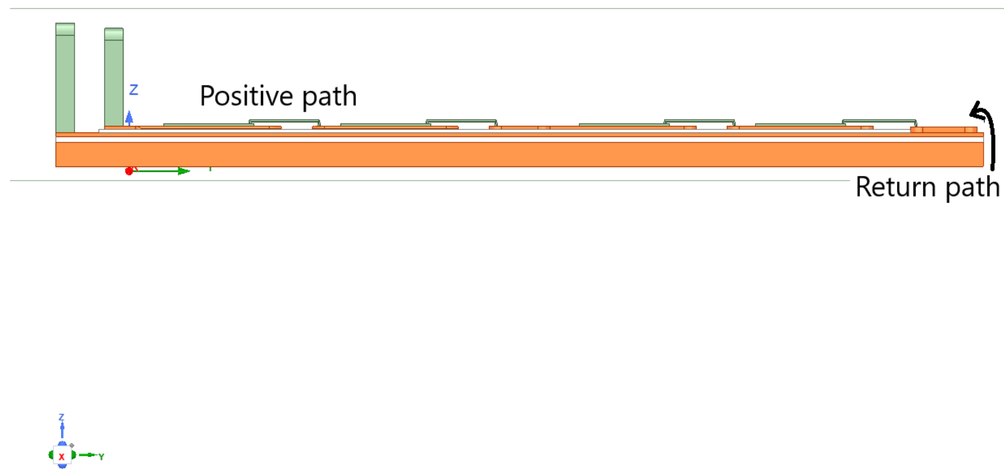


Figure 4.8: *Current paths in the NegativeLayer model.*

5 Simulation and lab experiment results

In this chapter, FEM software, such as ANSYS Q3D Extractor, ANSYS Maxwell, and ANSYS Workbench, is used for simulations, and the results are presented. First, the inductances extracted using ANSYS Q3D Extractor are presented. Subsequently, the electrical fields are simulated using ANSYS Maxwell and presented. Next, the thermal capability of the module is simulated with ANSYS Workbench Thermal Steady-State Analysis, and the results are presented. Lastly, the results from the lab experiments are presented.

5.1 Extraction of parasitics in ANSYS Q3D Extractor

In all paths where current flows, there will be inherent resistance, inductance, and capacitance in all conductors to some degree. As these elements are unavoidable, they can only be dealt with by placing the geometry of the power module in a way where the module layout takes advantage of natural phenomena to make an efficient package. An example of using the electromagnetic phenomena, magnetic flux cancellation, to reduce the inherent inductance of the package is by overlapping cross-sectional areas where current flows in opposite directions to cancel out the magnetic flux causing inductance. Calculating parasitics in complex geometries such as a power module requires the use of programs due to calculations by hand would be far too time-consuming and complicated. ANSYS Q3D Extractor was utilized in this thesis to extract desired inductances of the power module layouts.

To simulate the various models being tested in this project, the program ANSYS Q3D Extractor was selected due to its reliability and the supervisors' previous experience with the program. ANSYS Q3D Extractor can simulate both DC and AC. For the DC simulations, the inductance and resistance are approximately constant with frequency. For AC simulations, the inductance will be lower than the DC inductance in most cases due to AC simulations taking phenomena such as skin effect into account. Resistances for AC simulations increase by the square root of the frequency due to the skin depth decreasing with frequency, reducing the cross-section for current flow.

Every electromagnetic phenomenon can be described by using Maxwell's equations. The fundamentals of the equations above relate the electric field to the magnetic field and are dependent on the materials' electric permittivity, conductivity, and magnetic permeability. ANSYS utilizes a simplification of Maxwell's equations. ANSYS divides the conducting elements into a finite element mesh to calculate the inductance. Current is then applied to the source terminals. The electrostatic potential and volume current density is then computed for the conducting elements using a conduction solver. The inductances are then computed by evaluating the magnetic fields produced by the current.

5.2 Inductance simulation of newly designed packages

In this subsection, the inductance simulations are presented. Notably, the thickness of the substrate is 0.63mm, the gap between each individual voltage potential is 2.5mm, and a frequency of 10kHz can be assumed if nothing else is specified.

5.2.1 Bondwiring types

ANSYS Q3D Extractor allows for three types of bondwire structures, which are depicted in Figure 5.1, and the length of all the bondwires is 5.4mm.

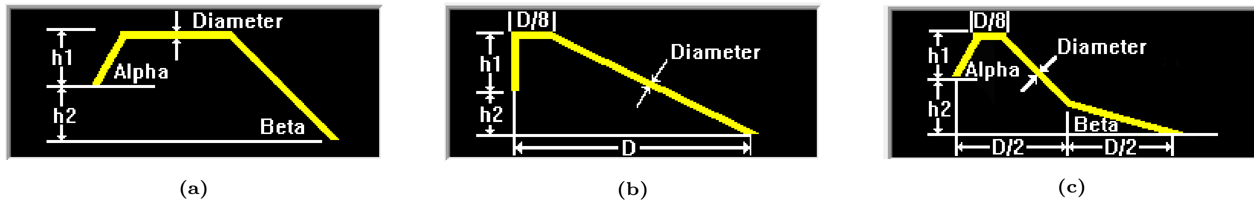


Figure 5.1: *Bondwire type Low (a), JEDEC 4-Point (b) and JEDEC 5-Point(c).*

The inductance simulations with different bondwire types were simulated with the Halfbridge module, and the results are depicted in Table 5.1. The results show that the type of bondwire plays a very small role on the total power loop inductance of the module.

Table 5.1: *Bondwire types' effect on power loop inductance.*

Bonding method	Inductance(nH)
Low	24.228
JEDEC 4-Point	24.274
JEDEC 5-Point	24.038

5.2.2 Varying the gap between the terminals and width of the terminals

To see how the size and placement of the terminals impact the inductance of the module, simulations with varying gaps distances between the terminals and widths of the terminals are performed. The terminals with gap distance and width are shown in Figure 5.2.

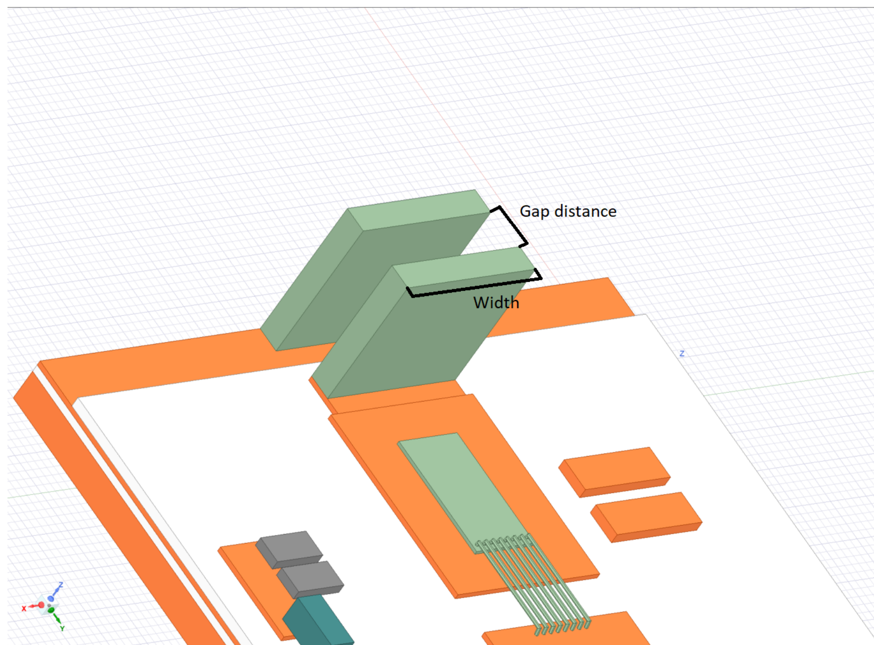


Figure 5.2: *Illustrating the terminal width and gap distance.*

In Table 5.2 and Table 5.3, the inductance simulation results are presented.

Table 5.2: *Variation in terminal gaps' affect on inductance for NegativeLayer model.*

Gap distance(mm)	DC Inductance(nH)	AC Inductance(nH)
0.5	20.834	8.410
1	21.147	8.802
1.5	21.711	9.436
2.5	21.967	9.768

Table 5.3: *Variation in terminal widths' affect on inductance for NegativeLayer model.*

Terminal width(mm)	DC Inductance(nH)	AC Inductance(nH)
1	25.783	13.274
5	22.963	10.621
7	22.407	10.108
9	21.967	9.768

5.2.3 The impact of the ceramic substrate thickness and the gap distance between current paths

To see the impact of the magnetic flux effect on the NegativeLayer module, simulations with different substrate thicknesses, 0.63mm and 0.25mm in Figure 5.3 and Figure 5.4, respectively. At 10GHz, the inductance of the module with a 0.63mm and 0.25mm substrate is 9.8nH and 7.2nH, respectively.

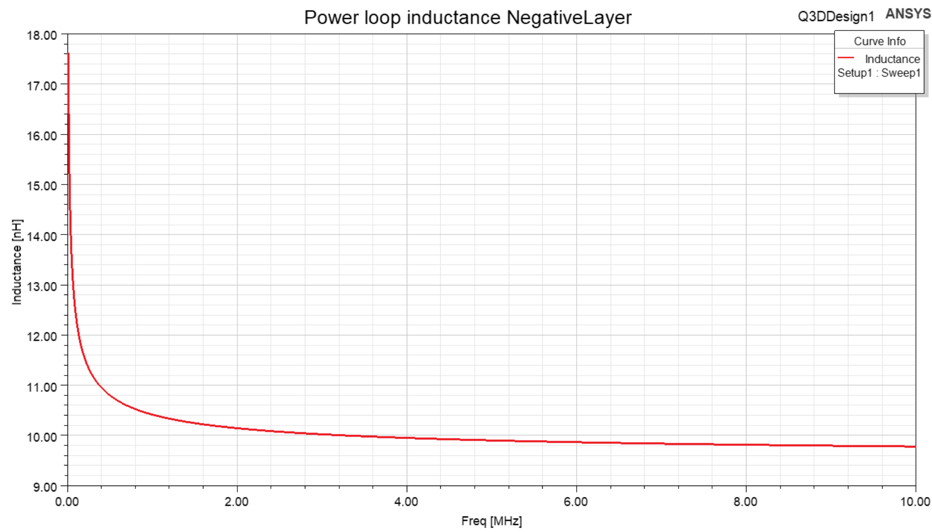


Figure 5.3: *Inductance sweep simulation for NegativeLayer module with 0.63mm substrate thickness.*

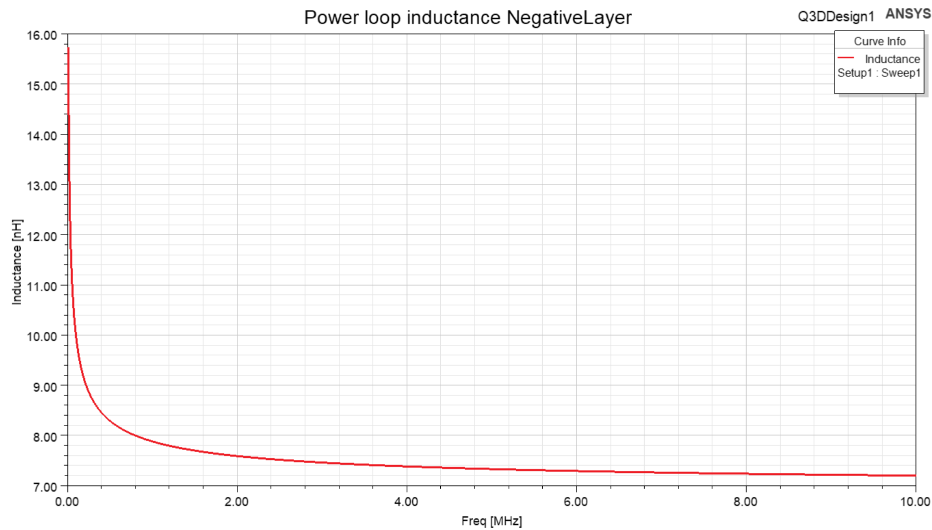


Figure 5.4: *Inductance sweep simulation for NegativeLayer module with 0.25mm substrate thickness.*

To see how the magnetic field cancellation impact the Halfbridge module, simulations with different gap sizes between the positive path and the return path of the current are depicted in Figure 5.5 and Figure 5.6.

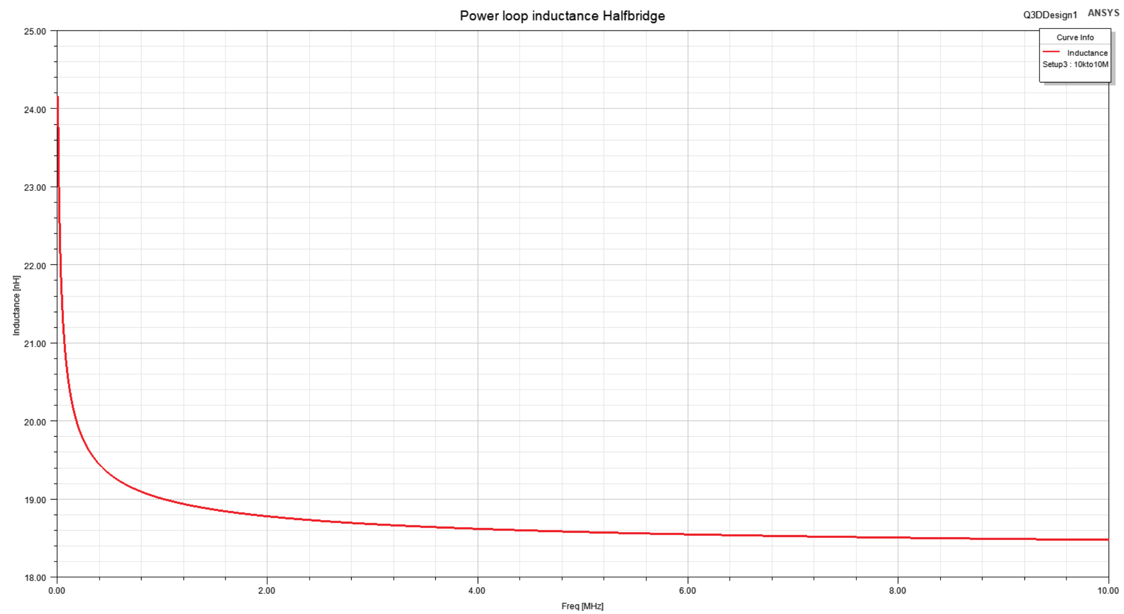


Figure 5.5: *Inductance sweep simulation for Halfbridge model with 2.5mm gap between current paths.*

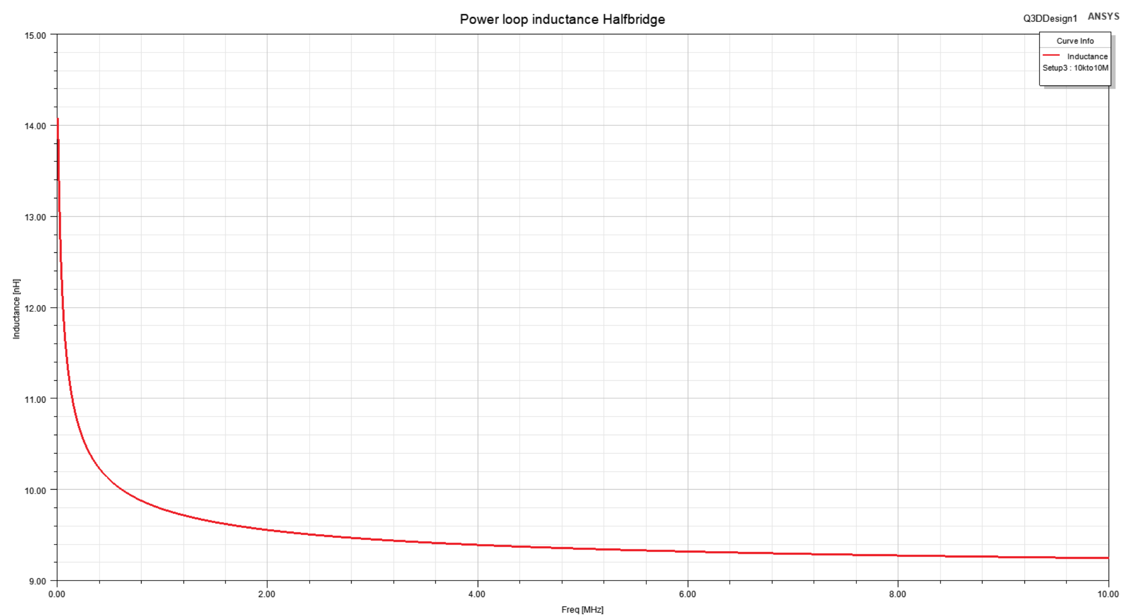


Figure 5.6: *Inductance sweep simulation for Halfbridge model with 0.5mm gap between current paths.*

5.2.4 Comparing the inductace of each current path and the total effective inductance of the module

In order to investigate the effect of the mutual inductance of the power module, the positive path and return path of the power module were simulated separately to remove the magnetic field cancellation effect. Results from inductance simulation performed for the positive path, the return path, and total loop inductance are displayed in Table 5.4 for the NegativeLayer module.

Table 5.4: *Inductances of the positive path, the return path and the total loop inductance of the NegativeLayer module.*

Electrical path	Inductance(nH)
Positive path	40.029
Return path	25.739
Total loop inductance	9.489

The corresponding values for the Halfbridge module are presented in Table 5.5.

Table 5.5: *Inductances of the positive path, the return path and the total loop inductance of the Halfbridge module.*

Electrical path	Inductance(nH)
Positive path	43.856
Return path	30.983
Total loop inductance	20.858

5.2.5 Varying the gap distance between the copper layers in the power module

In Figure 5.7 and Figure 5.8, the gap sizes between the copper islands is set to 2.5mm and 1.0mm, respectively.

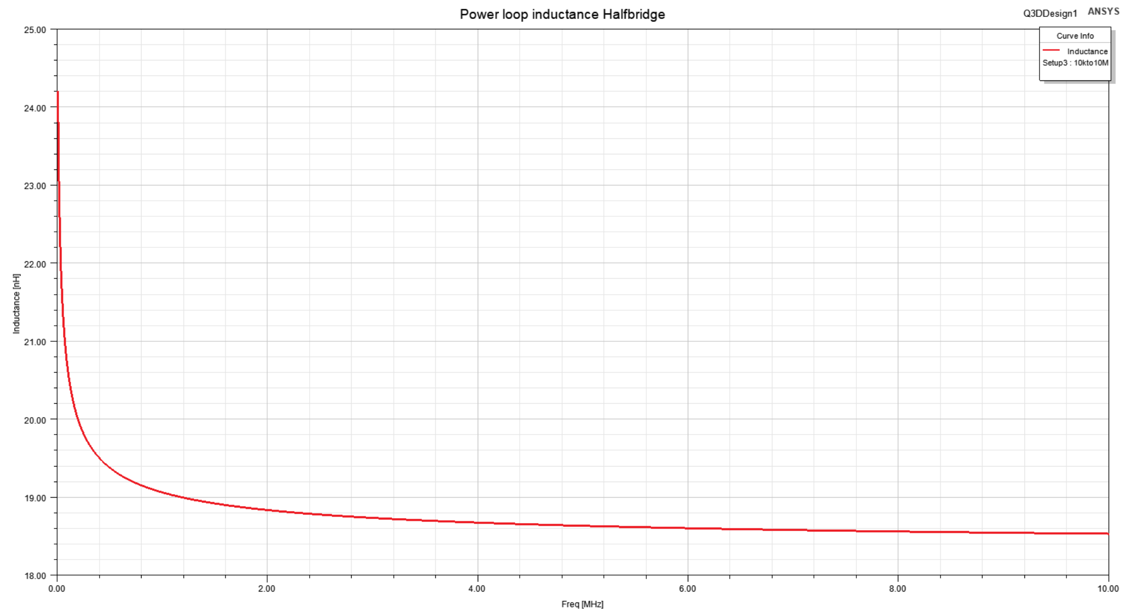


Figure 5.7: *Inductance sweep simulation for Halfbridge model with 2.5mm gap between copper islands.*

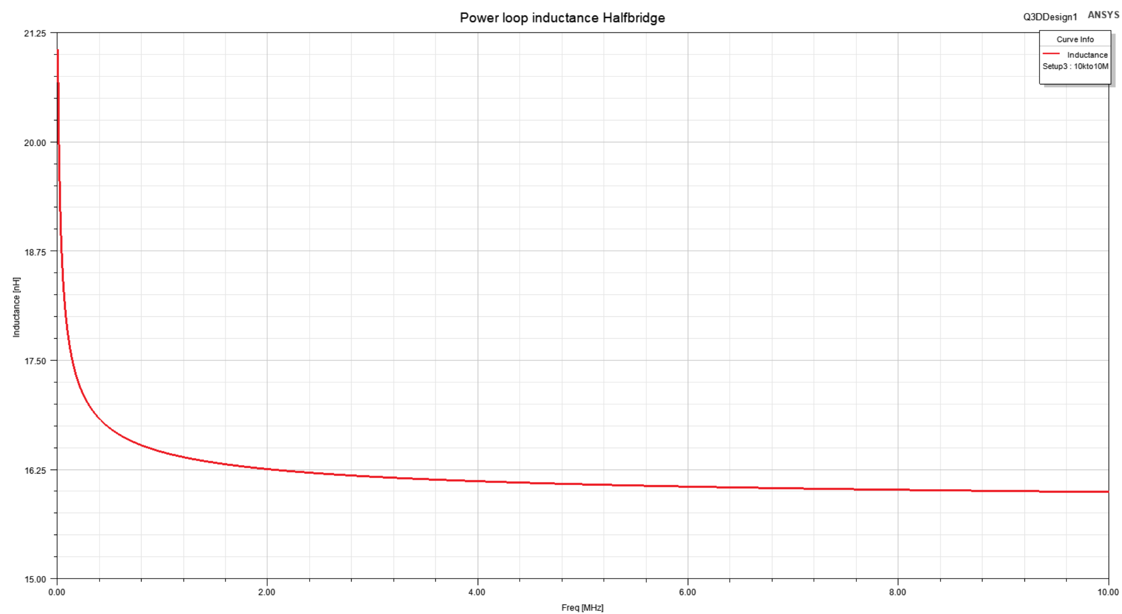


Figure 5.8: *Inductance sweep simulation for Halfbridge model with 1.0mm gap between copper islands.*

5.3 Electrical field simulation in Maxwell

Simulations for electrical fields were run in ANSYS Maxwell. Maxwell approximates the geometry of the objects into tetrahedral blocks in 3D and utilizes the Finite Element Method(FEM) to solve Maxwell's equations. The sum of the tetrahedra is referred to as the finite element mesh or mesh. Deciding the mesh resolution is essential for getting accurate results. In critical areas such as edges and at the interconnection of the bondwires and the DBC, it is especially crucial to have a fine mesh to get accurate results. If the mesh is not accurate enough, it could lead to misleading results. The drawback of having very fine meshing is longer simulation times, and the results could be affected by the field crowding effect as explained in [15]. Due to the amount of computing power needed to simulate very fine mesh, the critical areas are usually the only regions where fine meshing is particularly important. In Maxwell, the user can choose various meshing methods to obtain the wanted meshing.

Initially, Maxwell checks for errors and intersections, and the objects are meshed in order to perform field calculations. Before the solution process is started, Maxwell automatically meshes all model objects. However, the initial mesh is usually too unprocessed and not accurate enough, especially around critical areas. Adaptive meshing is performed to ensure better accuracy. The adaptive meshing refines the areas with stronger fields to provide accurate results. To what extent the adaptive meshing method refines the object is determined by the energy error threshold set by the user or when the maximum number of passes is reached. Stricter error thresholds increase the accuracy of the meshing. Notably, the adaptive meshing process is only available for static simulations.

In the electrical field simulations part, the measurement points on the module are depicted in Figure 5.9. The measure points are chosen due to the importance of fields on the edges and the impact of the bondwires during switching. From this point on the, "Point 1" is referred to as the "critical point". In plots where the distance from the copper island increases, the starting point is in "Point 2" and is moving towards the next copper island.

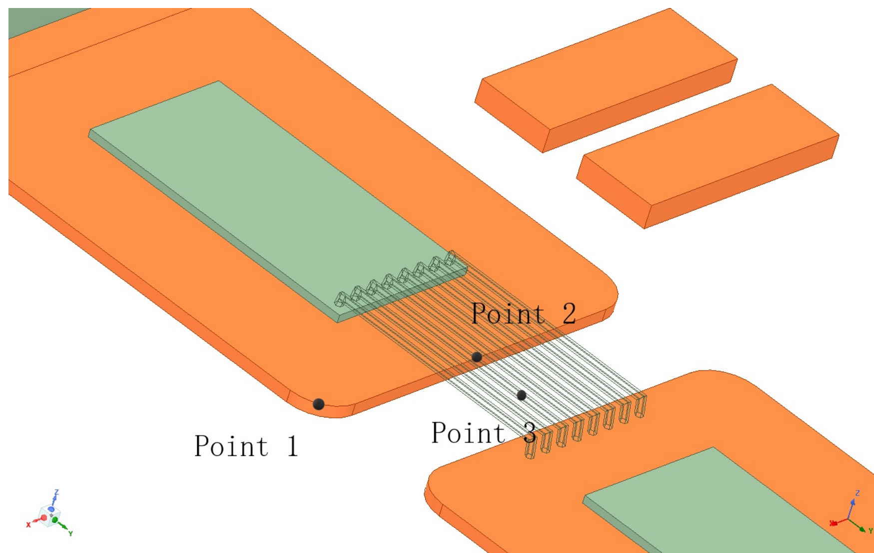


Figure 5.9: *Measure points used in Maxwell simulations.*

5.3.1 Effects of mesh

To obtain the desired meshing, the Electrostatic Solver was chosen as it can utilize the adaptive meshing. Parameters were set to simulate a maximum of 28 passes with a percent error of 0.01%. Refinement per pass was set to 30%, and the solution matrix was only solved after the last pass. The meshing used in the electrical field simulations is depicted in the Figure 5.10.

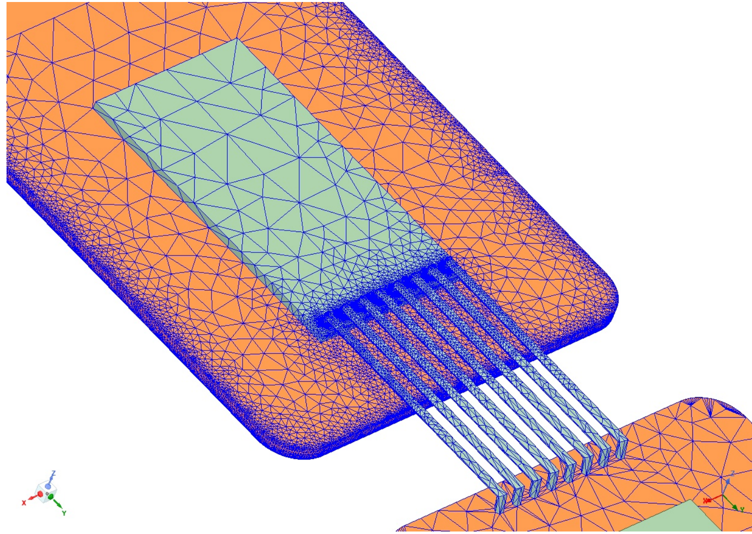


Figure 5.10: *Mesh used for Maxwell simulations.*

In all pictures of the electrical fields presented in a line, it is important to note that for the some results the nodal point chosen to document the electrical field are sometimes just a couple picometer above the stated point due to the electrical field value being set to no value if the nodal point is exactly on the intersection of the mesh elements. More information on how selecting the correct nodal point for the mesh is important can be found in section 3.3 and in [24], where it is stated that the electrical field at a perfectly sharp edge is infinite. In Table 5.6, the electrical field is measured at the critical point of the DBC, meaning the edge of the DBC, and the impact of meshing is shown.

Table 5.6: *Effects of increasing the mesh accuracy.*

Grading of mesh	E(V/m)
Innacurate mesh	8.296e+6
Finer mesh	1.925e+7

5.3.2 Electrical fields while edges are sharp

Conventionally, power module packages are filled with encapsulant to prevent electrical field breakdowns between different voltage potentials[25]. In Figure 5.11, the difference between the air and silicone gel used as encapsulant is depicted. In [26], the dielectric constant for silicon gel at 60Hz is 2.7 and was used throughout all of the simulations.

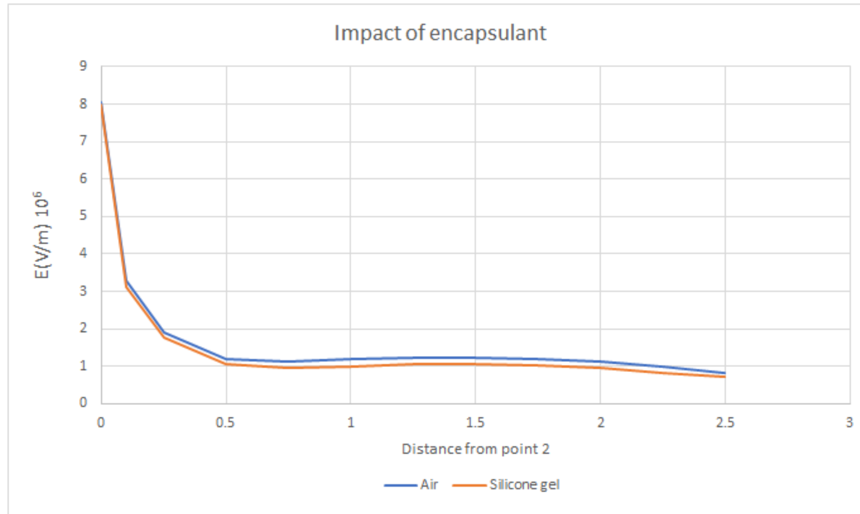


Figure 5.11: *Impact of air vs silicone gel.*

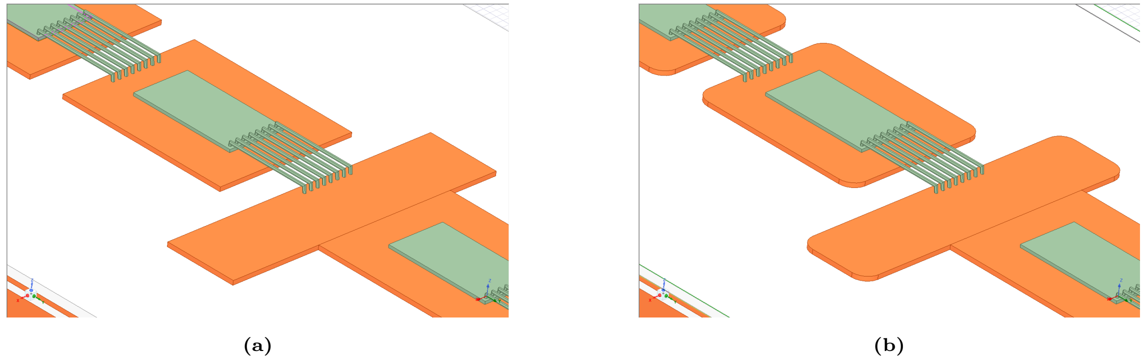
The electrical field strength at the critical point with different encapsulants is shown in Table 5.7. At the critical point, the difference in using silicone gel compared to air was a decrease in electrical field of 6%.

Table 5.7: *Electrical field strength at the critical point when edges are sharp.*

Encapsulant	E(V/m)
Air	2.387e+7
Silicon gel	2.245e+7

5.3.3 Effects of rounding edges

Until this point, during simulations, the model layout had sharp edges. However, from this point on, the simulations will have rounded edges to decrease the electrical field in vulnerable areas. Figure 5.12 shows the difference between sharp and round edges.



(a) (b)

Figure 5.12: *Sharp edges (a) and round edges (b).*

The edges of the DBC were rounded to remove and distribute the electrical field throughout the edge instead of concentrating the electrical field on the sharp edge. The effect of rounding edges has been demonstrated in [24]. The effect of rounding the edges can be seen in Table 5.8. The difference in electrical field strength is significant when comparing the electrical field strength found in Table 5.7 and Table 5.8.

Table 5.8: *Electrical field strength at the critical point when edges are round.*

Encapsulant	E(V/m)
Air	8.717e+6
Silicon gel	7.280e+6

In Figure 5.13, the electrical field strength along point 2 as the edges are rounded is shown.

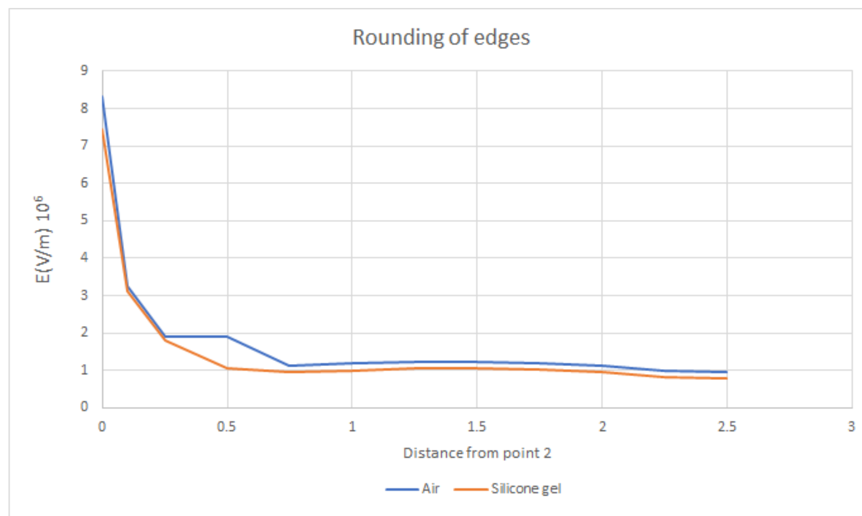


Figure 5.13: *Effects of rounding the edges.*

Due to the significant effect rounding the edges had on the electrical field simulations, it was experimented with rounding all the edges of the copper island as depicted in Figure 5.14. The electrical field strength in the critical point was further reduced to $4.0498 \cdot 10^6$V/m as the edges were even more curved.

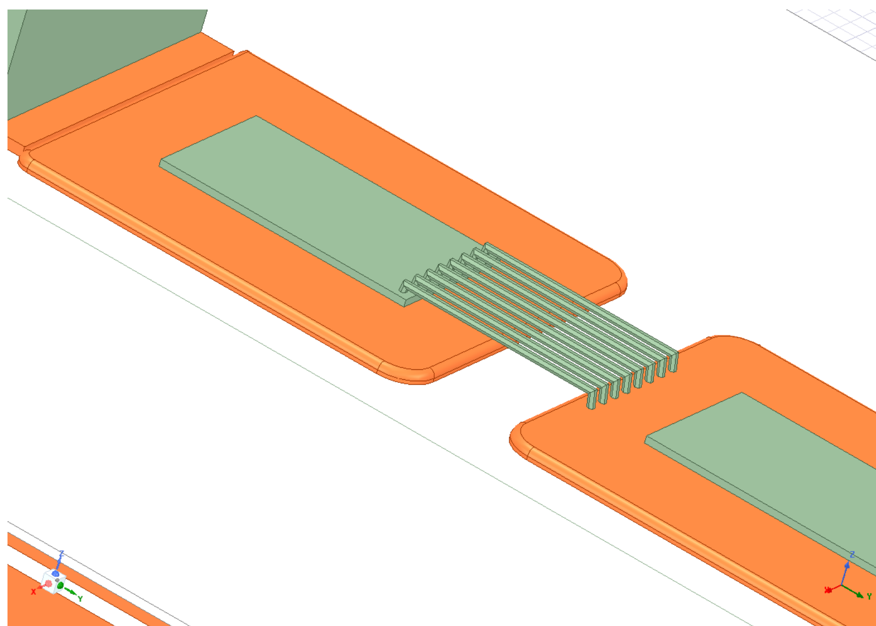


Figure 5.14: *Rounding all the edges of the copper islands.*

5.3.4 Varying bondwire height

In order to investigate the bondwires' impact on the electrical field around the SiC MOSFET die, the height of the bondwires was varied to observe the influence as the height was increased. The bondwire heights were increased from the standard height used in this thesis of 0.2mm to 0.4mm, 0.8mm, and 1.2mm. The results of the simulations are depicted in Figure 5.15.

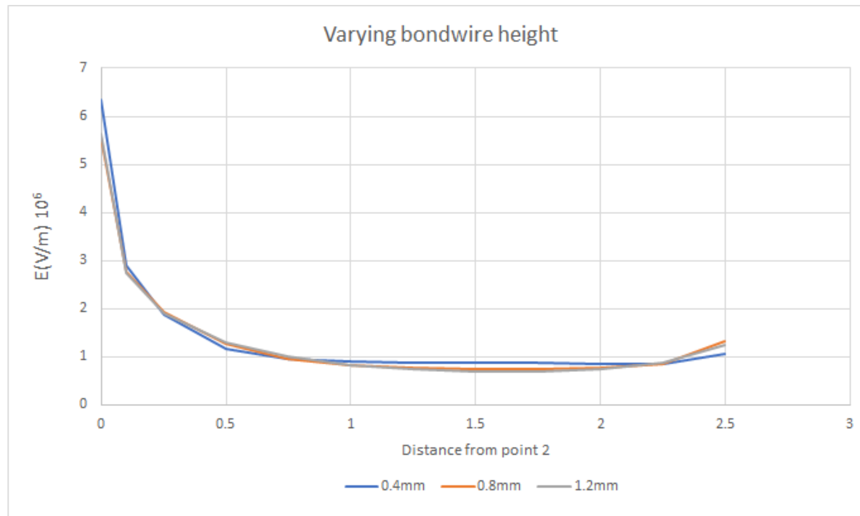


Figure 5.15: *Effects of varying bondwire height.*

In Table 5.9 the impact of varying bondwire height on the electrical field strength in the critical point is depicted.

Table 5.9: *Electrical field strength at critical point with varying bondwire height.*

Height of bondwires(mm)	E in critical point(V/m)
0.4	7.849e+6
0.8	7.718e+6
1.2	7.749e+6

In Figure 5.16 and Figure 5.17 the electrical field over the copper island with a bondwire height of 1.2mm and with air and silicon as encapsulants are depicted, respectively. The simulations show that the electrical field is reduced from $2.216 \cdot 10^6$V/m to $2.084 \cdot 10^6$V/m at the highest electrical field strength, as silicon gel is used as an encapsulant compared to air.

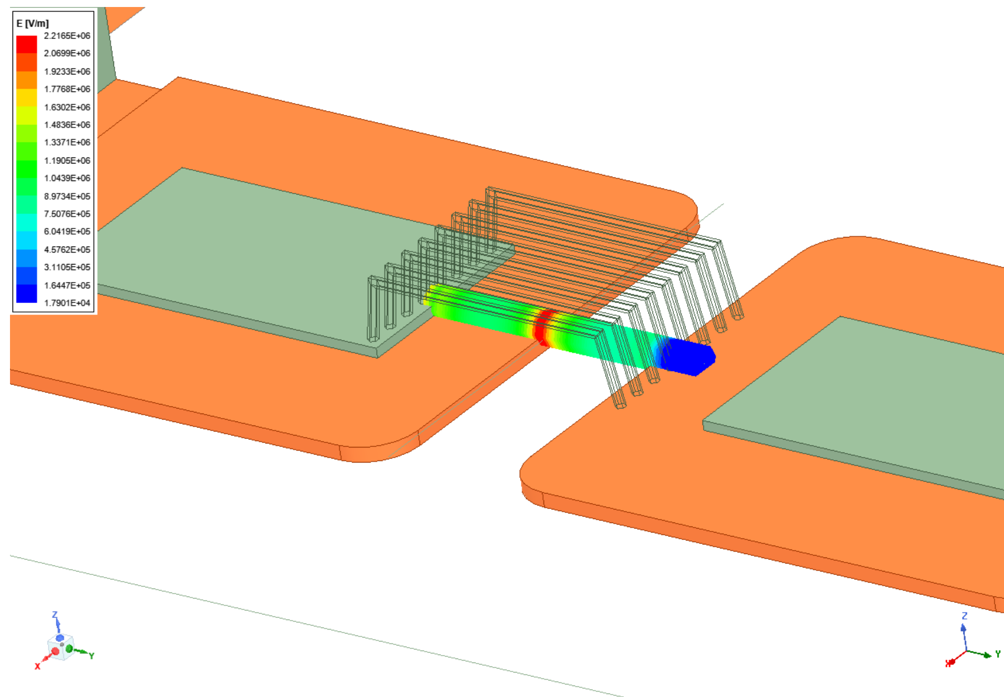


Figure 5.16: *Electrical field under bondwires with height of 1.2mm with no encapsulant and simulated with air.*

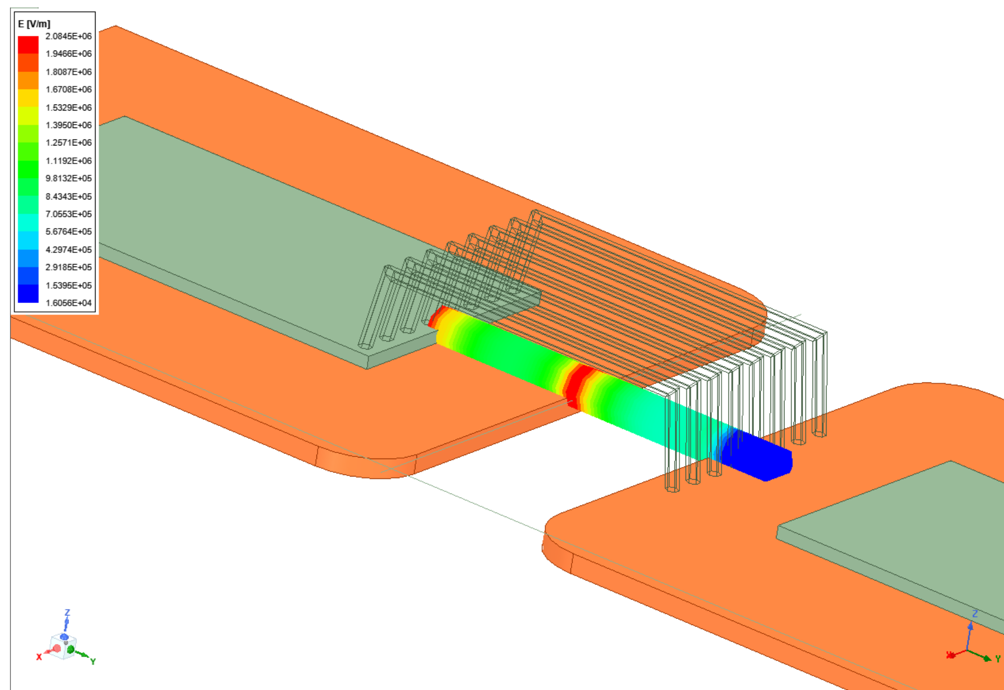


Figure 5.17: *Electrical field under bondwires with height of 1.2mm with encapsulant silicon gel.*

5.3.5 Varying the thickness of the ceramic substrate for the NegativeLayer model

The effects of varying the substrate thickness of the NegativeLayer model are depicted in Figure 5.18.

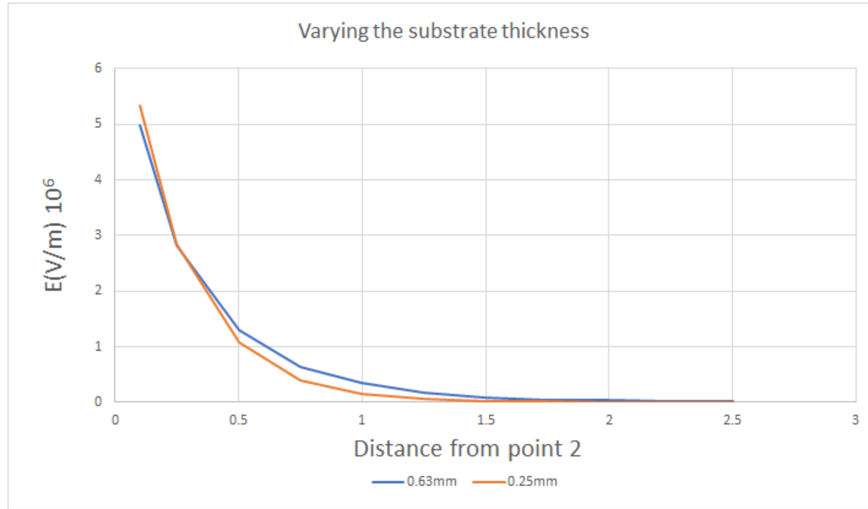


Figure 5.18: *Effects of varying the substrate thickness.*

As the results in the latter part of the graphs are hard to observe, the values were also placed in tabular form in Table 5.10.

Table 5.10: *Electrical field strength with varying substrate thickness.*

Distance from point 2(mm)	0.63mm substrate thickness E(V/m)	0.25mm substrate thickness E(V/m)
0.1	4.993e+6	5.327e+6
0.25	2.819e+6	2.849e+6
0.5	1.301e+6	1.067e+6
0.75	6.450e+5	4.020e+5
1.0	3.422e+5	1.570e+5
1.25	1.759e+5	5.530e+4
1.5	8.690e+4	1.840e+4
1.75	5.021e+4	7.840e+3
2.0	3.001e+4	4.121e+3
2.25	1.842e+4	2.388e+3
2.5	1.211e+4	4.524e+3

5.3.6 Varying the distance between positive and return path for the Halfbridge model

In Figure 5.19 the electrical fields between the two copper islands are depicted with different distances between the positive and negative paths.

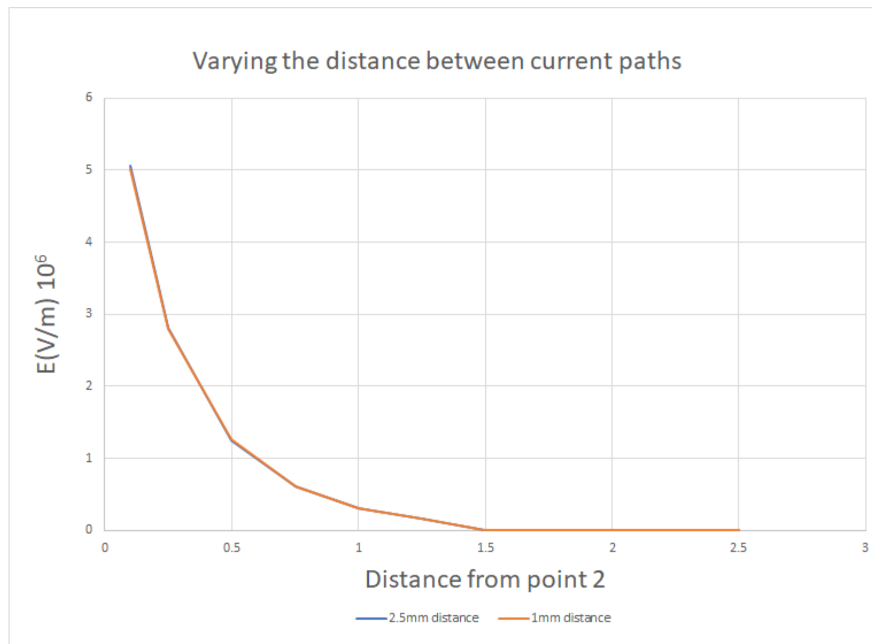


Figure 5.19: *Effects of varying the distance between current paths.*

The difference in distance between the two paths is shown to have no impact on the electrical field strength between the copper islands. However, the electrical field strength at the critical point was increased from 6.773e+6V/m to 8.588e+6V/m as the distance was reduced from 2.5mm to 1.0mm, respectively.

5.4 Thermal characteristics of newly designed modules

When designing a power module, it is crucial for the module to have sufficient thermal capabilities to function under high-temperature operation. The heat generated at the power dies has to be dissipated through the structure efficiently to not overheat the module, which can cause considerable thermal stress and faults. To start, the thermal resistance is calculated with an ideal heatsink. The power module calculations are performed to determine how much power is dissipated at each die. After calculations, thermal simulations with a variation of heatsinks are performed and discussed. Notably, due to the structural differences between the Halfbridge and NegativeLayer model, the latter inherently has a larger thermal resistance. The reason is the multiple ceramic layers, which have a lower thermal conductivity than copper. Therefore, only the NegativeLayer model is included in the thermal analysis.

5.4.1 Thermal analysis theory in ANSYS Workbench

The temperature is solved by the following Equation 5.1 for the steady-state thermal analysis in ANSYS Workbench and is based on Fourier's Law. The solver assumes no transient effects, and K and Q can be both constants or functions of the temperature.

$$[K(T)]\{T\} = \{Q(T)\} \tag{5.1}$$

Where K is the heat flow within the solid, Q is the heat flux, heat flow rate and, convection which are treated as boundary conditions.

Thermal analysis in ANSYS supports all geometries such as solids, surfaces, and line bodies. The geometries have to be assigned a material that has to include the thermal conductivity characteristic of the material. In steady-state thermal analysis, thermal conductivity is the only required property for materials. Thermal conductivity can depend on the temperature for some materials presented in a table. As the model's geometry is being set up, ANSYS Mechanical automatically generates the contact regions to enable heat transfer between components. Heat transfer is only possible if the component surfaces are connected or if the pinball region(reach of the thermal boundary) is within reach of one another as depicted in Figure 5.20. Perfect thermal contact between all surfaces is assumed during simulations, resulting in no variance in temperature transfer due to factors such as surface roughness, oxidation, or contact pressure[27].

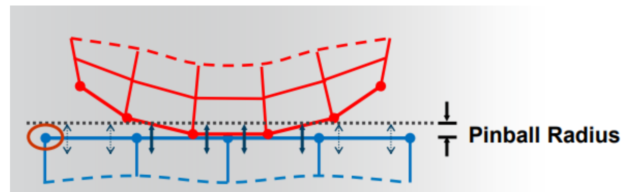


Figure 5.20: *Connecting pinball regions between two surfaces[27].*

When simulating conduction and convection, ANSYS Mechanical goes through the following procedure. ANSYS Mechanical uses the first law of thermodynamics that states that all thermal energy is conserved and uses this in a differential control volume. Fourier's law is then used to relate the heat flux vector to the thermal gradients. Specified temperatures, heat flow, and convection are assumed to cover the entire element

surface. For radiation, the Stefan-Boltzmann is extended for the system of N(number of surfaces radiating) enclosures. The Siegal and Howell equations give the energy balance, which correlates the energy losses to surface temperatures[28].

5.4.2 Thermal resistance of the power module with ideal heatsink

The thermal resistance of a geometry is defined by Equation 5.2[5].

$$R_{th} = \frac{d}{\lambda A} \tag{5.2}$$

R_{th} is the thermal resistance, d is the layer thickness of the geometry, λ is the thermal conductivity of the geometry's material, and A is the cross-sectional area of the heat transfer. In [29], the thermal conductivity for SiC was gathered. The thermal conductivity of copper and AlN was already implemented in ANSYS Workbench.

To calculate the total thermal resistance of the power module, Equation 5.2 has to be calculated for each layer. However, certain assumptions are made to simplify the calculations. The maximum junction temperature is set to 100°C because higher temperatures could result in a shorter lifetime for the module even though the rated temperature is higher. The module is assumed to be water-cooled with a water temperature of 40 degrees. The water temperature is set relatively high to ensure the power module functions in high-temperature climates. Another assumption made for the simulation is that half of the thermal resistance is from junction to case and the other half is from case to ambient. This assumption is made due to the models designed not including a heatsink connected to the baseplate. Therefore, the temperature difference is set to half to make up for the lack of heatsink in the simulations.

$$\Delta T = 100°C - 40°C = 60°C = \frac{60°C}{2} = 30°C \tag{5.3}$$

In Figure 5.21, the NegativeLayer model being used during simulations is depicted.

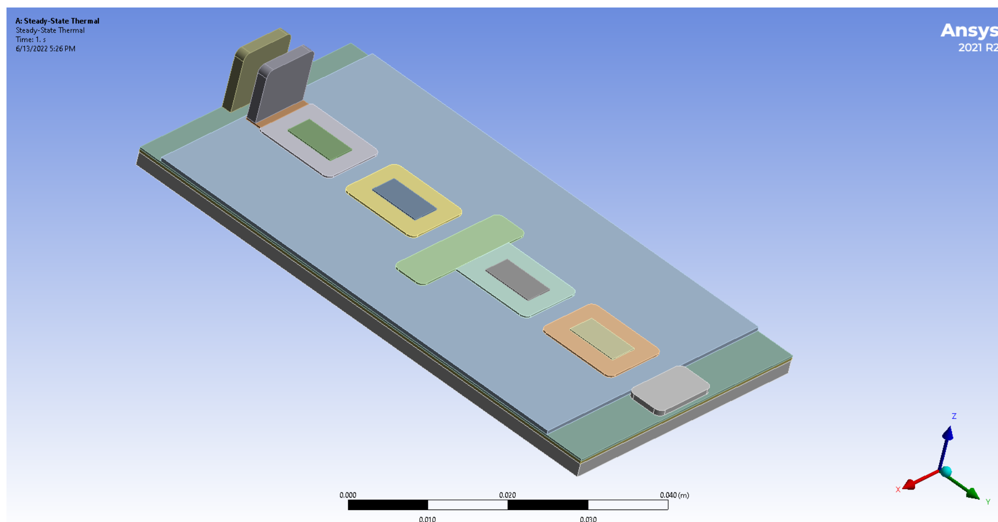


Figure 5.21: *NegativeLayer model in Workbench Steady-State Thermal.*

In Figure 5.22, the meshing used in the thermal simulations is depicted. As the meshing is rather fine, Figure 5.23 shows a zoomed-in picture to see the meshing better.

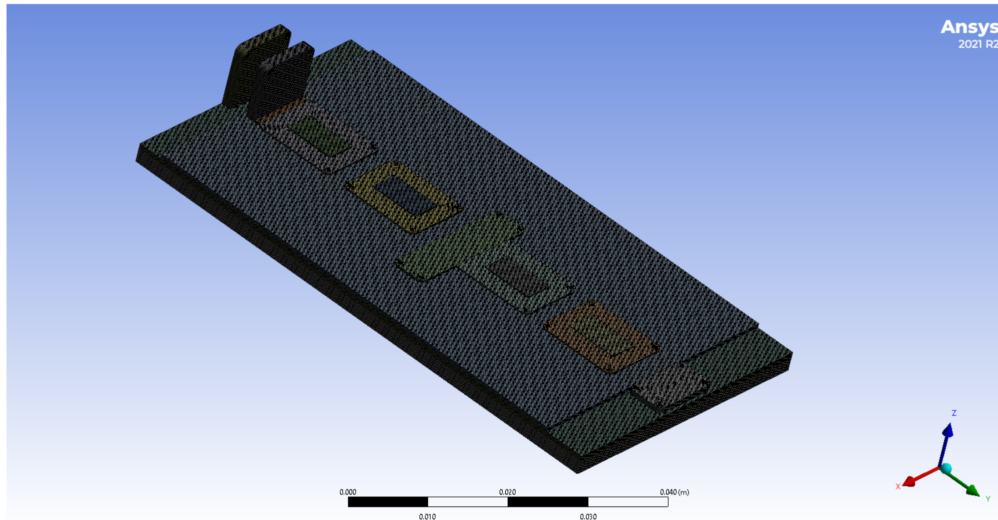


Figure 5.22: *Meshing used for thermal simulations.*

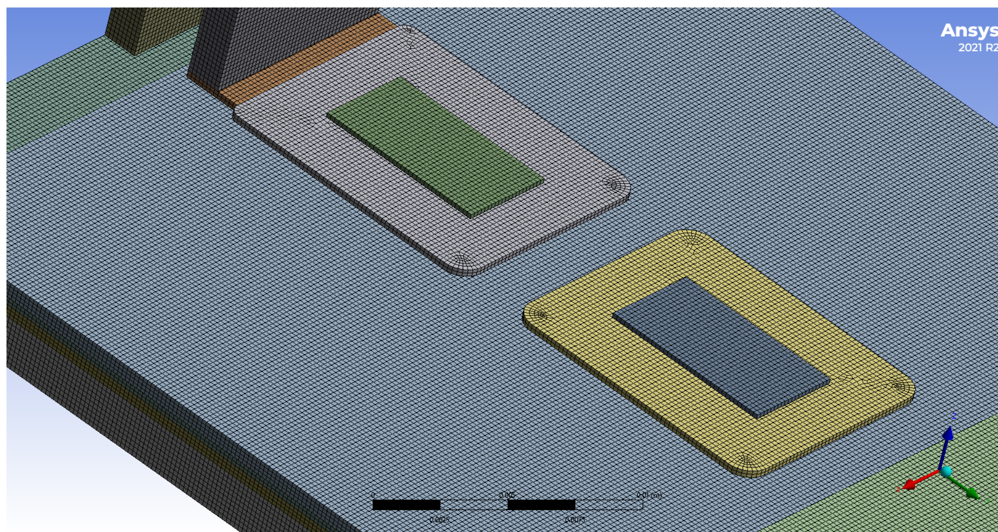


Figure 5.23: *Zoomed picture of meshing used for thermal simulations.*

The thermal resistance, R_{th}, was simulated by applying 30W to each SiC MOSFET in the power module. The temperature distribution is shown in Figure 5.24. And the temperature difference is 34.7°C at the peak value and 22°C for the ambient temperature, resulting in a ΔT of 12.7°C. Notably, the baseplate of the module is set to constant 22°C and the heatsink is treated as an ideal heatsink for this scenario.

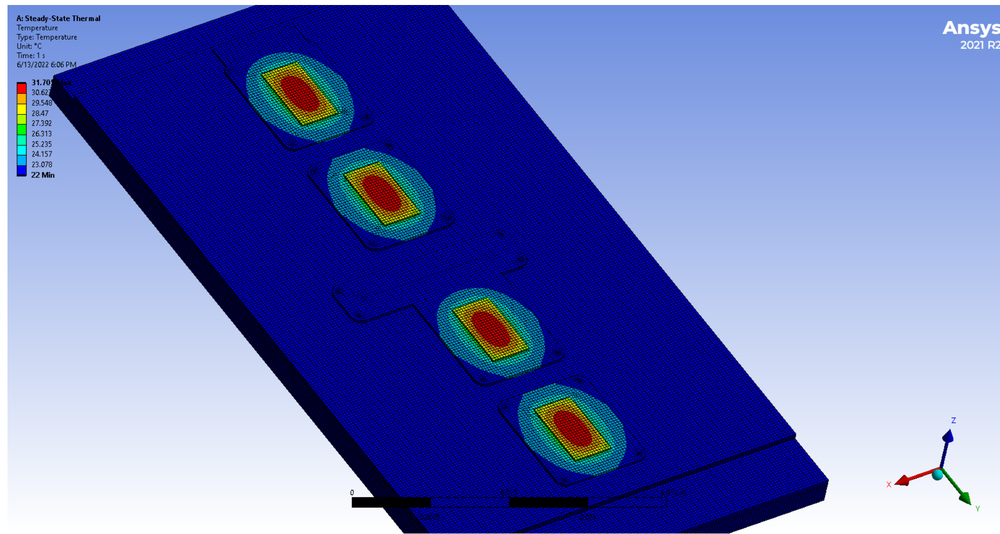


Figure 5.24: *Heat distribution as the power are applied at the dies.*

Using Equation 5.4 the resulting thermal resistance for each die was calculated.

$$R_{th} = \frac{\Delta T}{P} = \frac{12.7°C}{30W} \tag{5.4}$$

The thermal resistance of each die is calculated to be 0.423K/W. The maximum amount of power generated by the dies allowed for a functional operation within the set boundaries is given by Equation 5.5.

$$P_{max} = \frac{\Delta T}{R_{th}} = \frac{30°C}{0.423°C/W} \tag{5.5}$$

Resulting in a total allowed power generated at the die of 70.9W.

5.4.3 Power loss calculation

A hypothetical scenario where the module is used in a DC to DC buck converter with a 99% duty cycle is used to calculate if the total power losses exceed the boundaries set. The converter is depicted in Figure 5.25. As the duty cycle is 99%, the turn off and turn on current are approximately the same. Having a duty cycle at 99% means operation of the converter under worst-case conditions as the switching current is always assumed to be its peak value.

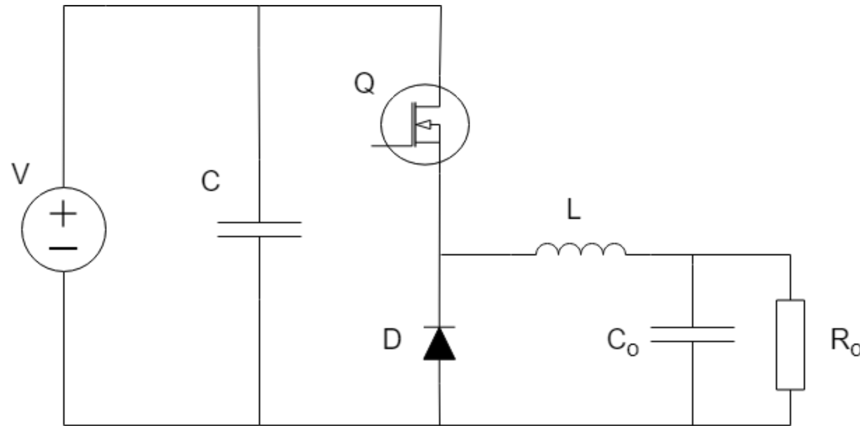


Figure 5.25: *Example circuit of a DC to DC buck converter.*

As the power die[18] does not include datasheets for the switching energies, the packaging C3M0021120K which has the same chip inside, with the same voltage and current with a resistance of 21mΩ at 25°C was chosen[30]. The on-resistance was given to be 1.25 P.U. at 100°C junction temperature, resulting in an on-resistance of $26.25m\Omega$. The drain current is chosen to be 43A.

Power loss in a semiconductor can be calculated using Equation 5.6. The total power losses of the MOSFET consist of the switching losses, conduction losses, and blocking losses(leakage losses). However, the blocking losses are usually negligible and will therefore not be included in the calculation of the power losses. Switching losses occur as the transistor switches on and off. Meanwhile, the conduction losses occur only when the switch conducts current.

$$P_{\text{MOSFET}} = P_{\text{switching}} + P_{\text{conduction}} \tag{5.6}$$

Conduction losses are the losses generated in the transistor's on-resistance as the current goes through the body diode. The transistor's on-resistance is often referred to as R_{on} and is the inherent resistance of the semiconductor. As mentioned in earlier chapters, the on-resistance is decided by various factors such as the voltage over the device and the temperature. Resistance increases with increased temperatures, and the on-resistance is therefore often presented as curves or datasheets. Equation 5.7 shows how the conduction losses of the device are dependent on the drain current, I_{on}, when the transistor is on and the on-resistance R_{on}.

$$P_{\text{conduction}} = {I_{on}}^2 * R_{on} \tag{5.7}$$

Notably, as the device is not conducting for the entirety of the duration, the conduction losses have to be

multiplied by the square root of the duty cycle of the device. Using the conduction formula for the specified values and including the duty cycle, the resulting conduction loss is 48.1W.

Switching losses are a result of the overlapping interval of current and voltage during turn off and turn on. The transistor's intrinsic capacitance stores energy dissipated in the turn-on and plays the role of a snubber in turn off. Therefore, the switching losses are dependent on the generated turn-on energy and the turn-off energy in relation to the switching frequency. There are various ways of calculating the switching losses, such as looking at the time it takes to turn on and off the device, and it can be calculated using the output capacitance value of the device. Equation 5.8 shows one of the numerous formulas that can be used to calculate the switching losses.

$$P_{sw} = (E_{sw,on} + E_{sw,off}) \cdot f_{sw} \tag{5.8}$$

Where P_{sw} is the switching losses, $E_{sw,on}$ is the turn-on energy generated, $E_{sw,off}$ is the turn-off energy generated, and f_{sw} is the switching frequency of the device. Since all the MOSFET dies are connected in series for the packaging layouts presented in this thesis, the current is equal in all dies. However, the voltage may vary due to various factors but is assumed to be evenly allocated over the transistors. The switching energies are obtained from the datasheet [30] and the total switching energy is 1.1mJ at 800V. At a switching frequency of 20kHz, the total switching loss is 22W. Using Equation 5.6 the total losses is 70.1W. Meaning that for the scenario chosen, the power loss are not exceeding the total allowed power loss.

5.4.4 Thermal resistance of the power module with water cooling heatsinks

In order to get a more realistic result than the ideal heatsink, keeping the baseplate at a constant temperature of 22°C, the following simulations will be with a heatsink of both 3000 W/m^2K and 10000 W/m^2K heat transfer coefficients, respectively. The chosen values are based on the article [14], where 3000 W/m^2K is a low htc value for heatsinks using water cooling and 10000 W/m^2K is the maximum htc. Next, the module is simulated for a heatsink technology utilizing flow cooling channels under the DBC to achieve a high heat transfer coefficient of 20000 W/m^2K[31]. Lastly, the gap distances between the copper islands are reduced from 2.5mm to 1mm to see the impact on the thermal capability of the module. For the last simulations, the heatsink with a htc of 10000 W/m^2K was chosen. The same ambient temperature of 22°C and power loss of 30W per die is used for all of the simulations performed in this sub-chapter.

In Figure 5.26, the heat distribution with a heatsink capable of constant convection of 3000W/m^2K is depicted. The heat distribution on the underside of the baseplate is depicted in Figure 5.27.

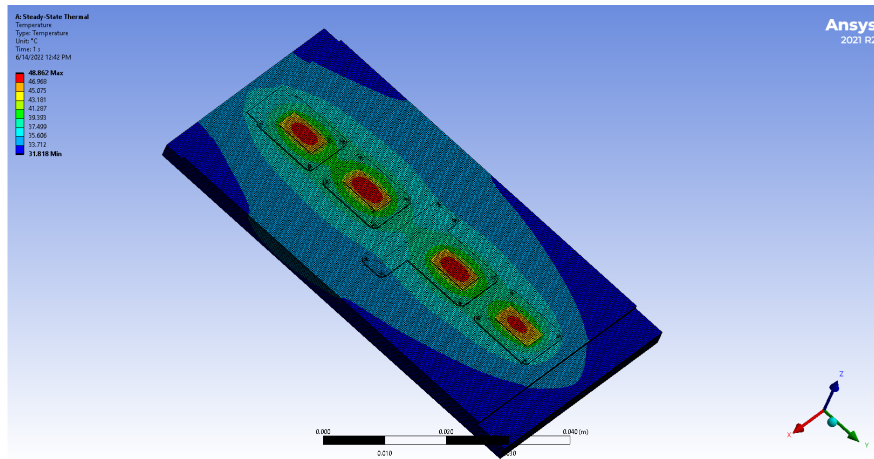


Figure 5.26: *Heat distribution on the top of the DBC for a heatsink with a htc of 3000 W/m^2K.*

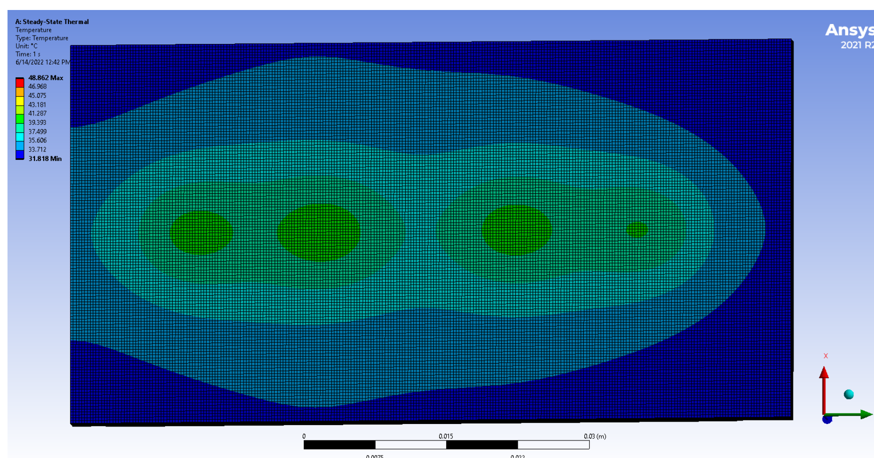


Figure 5.27: *Heat distribution on the bottom of the baseplate for a heatsink with a htc of 3000 W/m^2K.*

The temperature difference for the heatsink with 3000 W/m^2K htc is roughly 26.9°C:

$$\Delta T = 48.9°C - 22°C = 26.9°C \tag{5.9}$$

Using Equation 5.4 the calculated thermal resistance of the module is 0.897°C/W. The maximum amount of power allowed to be generated at each die is found using Equation 5.5 and was calculated to be 33.4W.

In Figure 5.28, the heat distribution with a heat sink capable of constant convection of 10000W/m^2K is depicted. The heat distribution on the underside of the baseplate is depicted in Figure 5.29.

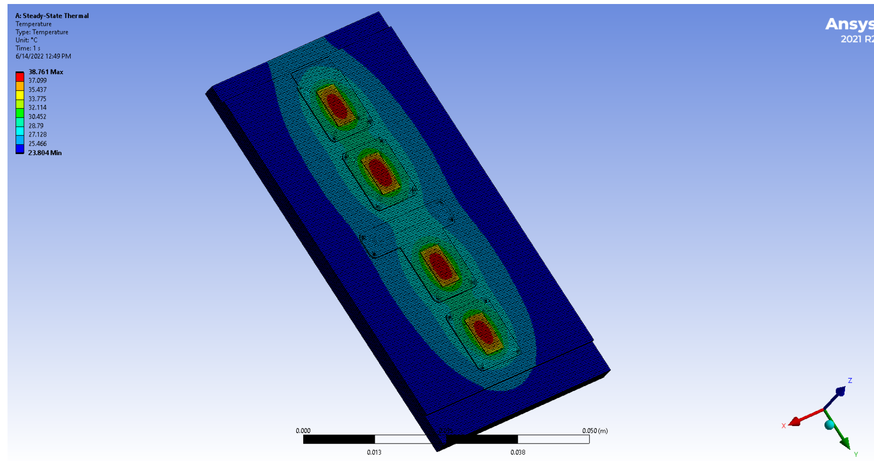


Figure 5.28: *Heat distribution on the top of the DBC for a heatsink with a htc of 10000 W/m^2K.*

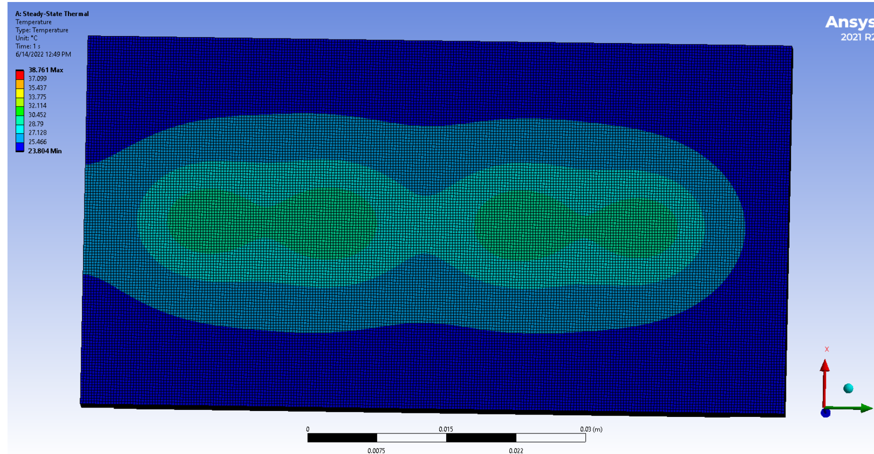


Figure 5.29: *Heat distribution on the bottom of the baseplate for a heatsink with a htc of 10000 W/m^2K.*

The temperature difference with the heatsink with 10000 W/m^2K htc is roughly 16.8°C:

$$\Delta T = 38.8°C - 22°C = 16.8°C \tag{5.10}$$

Using Equation 5.4 the calculated thermal resistance of the module is 0.56°C/W. The maximum amount of power allowed to be generated at each die is found using Equation 5.5 and was calculated to be 53.6W.

In Figure 5.30 the heat distribution with a heat sink capable of constant convection of $20000 W/m^2K$ is depicted. The heat distribution on the underside of the baseplate is depicted in Figure 5.31.

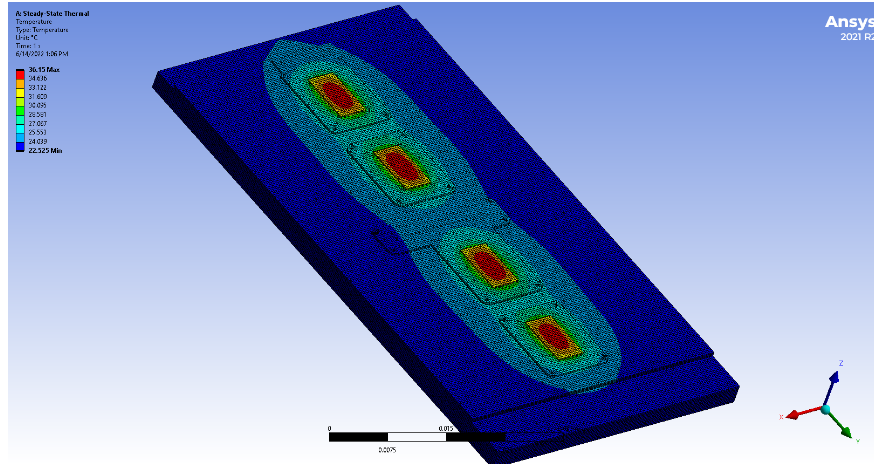


Figure 5.30: *Heat distribution on the top of the DBC for a heatsink with a htc of 20000 W/m^2K.*

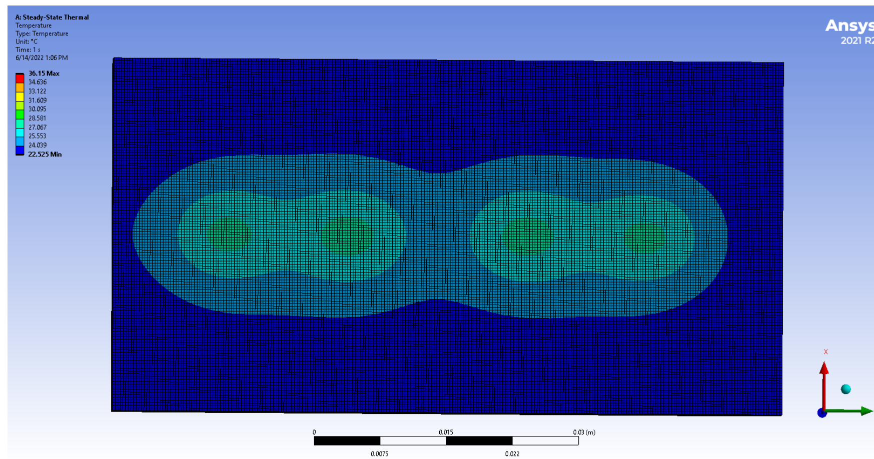


Figure 5.31: *Heat distribution on the bottom of the baseplate for a heatsink with a htc of 20000 W/m^2K.*

The temperature difference with the heatsink with 20000 W/m^2K htc is roughly 14.2°C:

$$\Delta T = 36.2°C - 22°C = 14.2°C \tag{5.11}$$

Using Equation 5.4 the calculated thermal resistance of the module is 0.473°C/W. The maximum amount of power allowed to be generated at each die is found using Equation 5.5 and was calculated to be 63.4W.

Lastly, the effect of moving the copper islands closer to each other on the heat distribution is depicted in Figure 5.32. The heat distribution on the underside of the baseplate is depicted in Figure 5.33.

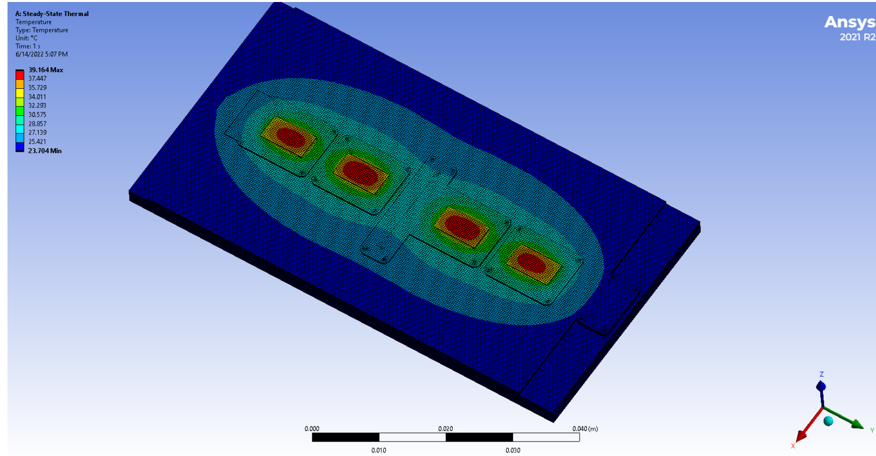


Figure 5.32: *Heat distribution on the top of the DBC as dies are moved closer for a heatsink with a htc of 10000* W/m^2K .

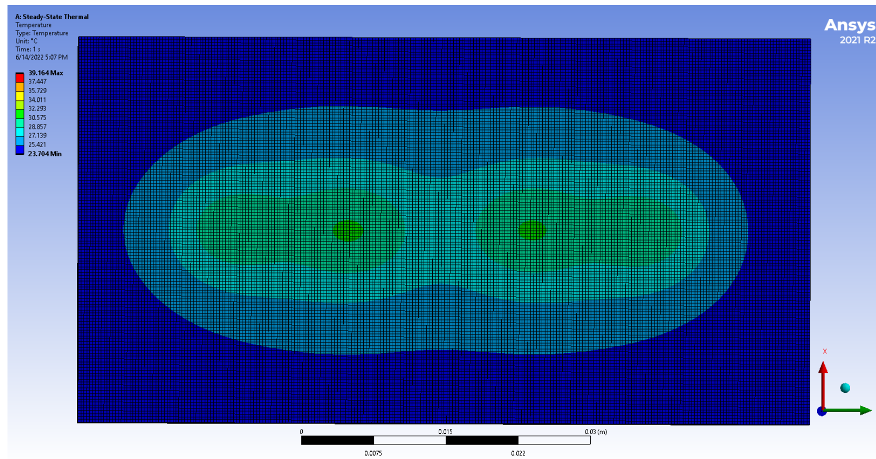


Figure 5.33: *Heat distribution on the bottom of the baseplate as dies are moved closer for a heatsink with a htc of 10000* W/m^2K.

The temperature difference with the heatsink with 20000 W/m^2K htc is roughly 17.2°C:

$$\Delta T = 39.2°C - 22°C = 17.2°C \tag{5.12}$$

Using Equation 5.4 the calculated thermal resistance of the module is 0.573°C/W. The maximum amount of power allowed to be generated at each die is found using Equation 5.5 and was calculated to be 52.4W.

5.5 Lab experiments performed at EFD Induction

Pulse testing of the Halfbridge layout was performed at EFD Induction. The setup used is depicted in Figure 5.34. To make ensure no faulting would occur during testing, the first results presented are performed at 300V DC and with a 42A peak current but are later increased. Initially, the gate drivers used to control the SiC JFET cascodes were the "1ED020I12-F2" model [32]. Later in the chapter, the gate driver is replaced by a newer model, "ADuM4136"[33], as the first gate driver was not accurate enough.

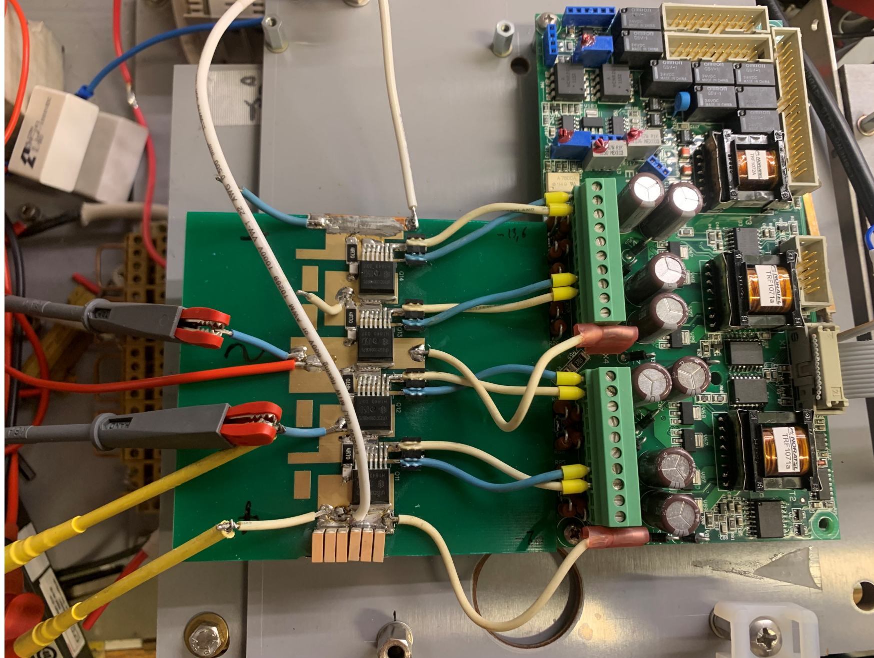


Figure 5.34: *Testing jig used at EFD Induction.*

The RC snubber circuits were implemented with regards to the recommendation in [34]. However, the recommendations are intended for a TO-247-3L package that inhabits larger parasitics than the TO-263-7L used during measurements. The recommendations were a resistance of 5Ω, resistance used in experiments is 4.7Ω, and a capacitor of 330 pF, where the resistance type and capacitor type were "a low value flat chip resistor" [35], and ceramic chip capacitors [36], respectively. Due to previous experience gained from [21] rather, large RC snubbers were required to get an even voltage distribution over transistors connected in series. Therefore, the choice was to start with a relatively large RC snubber compared to the recommendations. A DC link was connected between the module terminals to stabilize the voltage. The DC link consisted of two ceramic type FA3 1.5µF rated for 700V [37] connected in parallel. The capacitor was chosen due to its low inductance.

For measurement the voltage probes "HDV3206" [38], current probe "Tektronix p6021"[39] and current probe "CP031"[40] was used. The oscilloscope used was a "Wavesurfer 3034" from Teledyne LeCroy, [41]. Turn on voltage is 14V with a gate resistor of 2.2Ω, and turn off voltage is set to -8V with a gate resistor of 1Ω. Recommended turn on and turn off resistors are 10Ω and 22Ω, respectively. Due to the resistances during

testing being significantly smaller, the switching is faster than the recommended switching times. This was done intentionally to test the low inductive layout designed in the thesis.

In Figure 5.35, the electrical diagram of the setup is depicted. V_{var} is a variable voltage source, C_{in} is the DC link capacitance, GD is the gate drivers for each transistor, L is the load inductance, C1 is the resonance capacitor, C2 and C3 are the voltage splitting capacitors to get a midpoint and R13 is the thirteen 1Ω resistances connected in parallel. Notably, there are kelvin connections between the gate driver and the transistors and RC snubbers connected in parallel with each transistor which is not included in the figure.

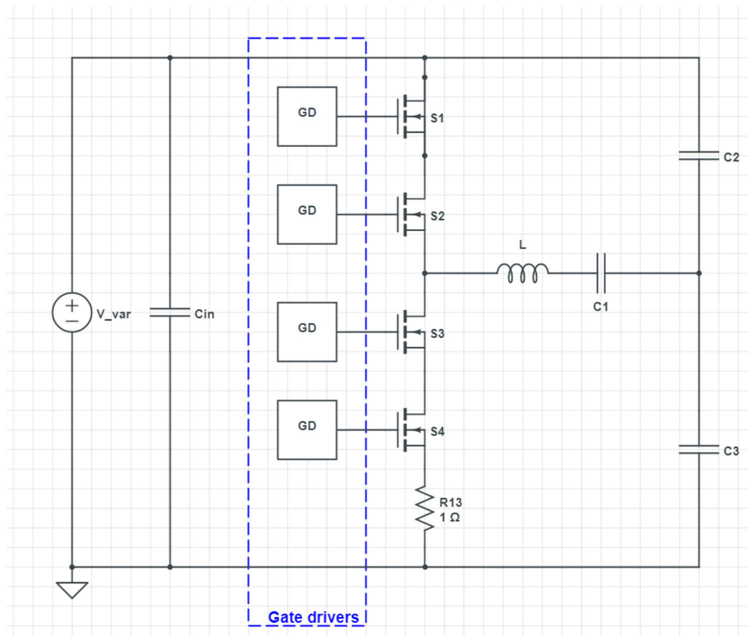


Figure 5.35: *Testing circuit diagram of the setup used at EFD Induction.*

The jig has the ability to vary the on time(T1) of the signal and the blanking time between the upper and lower switch(T2). The signal is illustrated in Figure 5.36. By adjusting the time intervals, it is possible to vary between soft switching, meaning switching close to zero current, and hard switching, switching at higher currents, of the transistors.

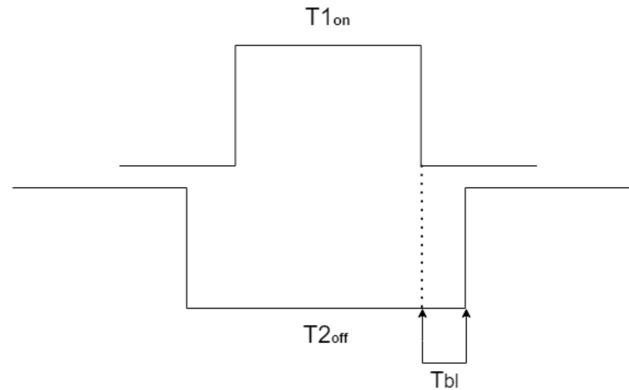
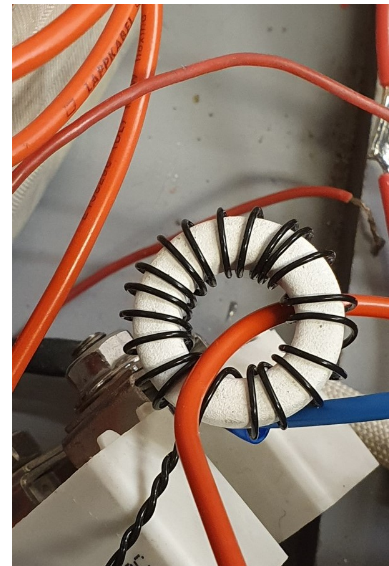


Figure 5.36: *Adjustable blanking time, T_{bl}, and on time, T1.*

It is important to note that the gate current was measured with a 5 turn winding depicted in Figure 5.37(a), and the output current of the module was measured with a 20 turn winding depicted in Figure 5.37(b). This has to be taken into account when going through the waveforms.

(a)



(b)

Figure 5.37: *Gate current 5 turn winding(a) and output current 20 turn winding(b)*

5.5.1 Time delay from gate drivers and effects of jitter

The time delay from the moment the gate driver sends the signal to the transistor turns off was measured to be 47-48ns and is depicted in both Figure 5.38 and Figure 5.39. The current measurements, the red and green waveforms, start falling, but the voltage does not rise until 47-48ns has passed. During measurements, the red current waveform and the yellow voltage waveform are the gate current and the voltage over the transistor. Likewise, the green current waveform and the blue voltage waveform belong to the other JFET connected in series.

In Figure 5.38, the green gate current starts falling first, resulting in most of the voltage over the "blue" transistor. In Figure 5.39 the roles are reversed as the gate driver[32] has significant jitter. Jitter in the signal sent by the gate driver results in the JFETs to turn off with different time delays for each pulse.

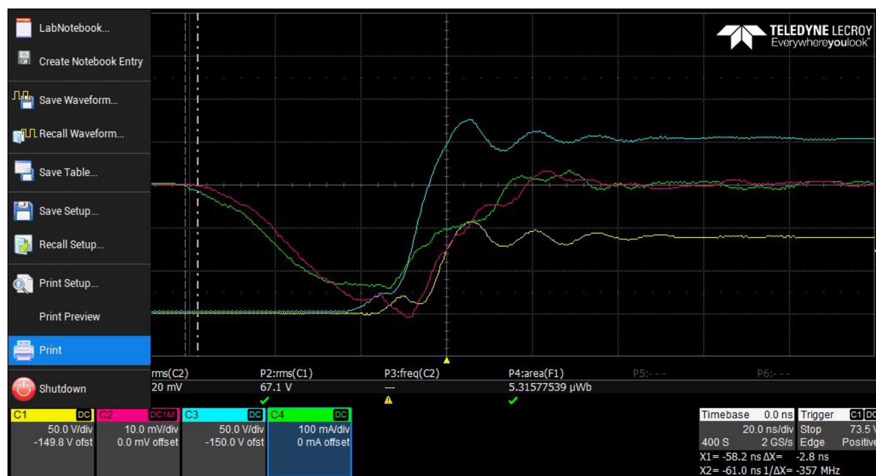


Figure 5.38: *Blue transistor leading.*

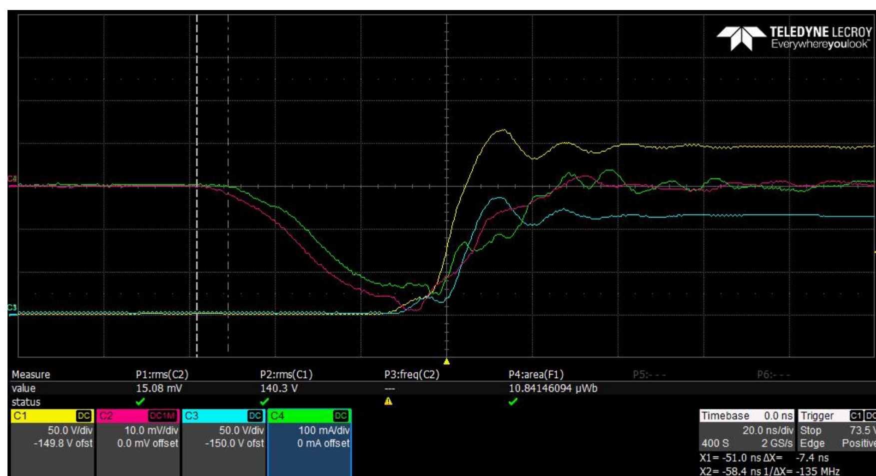


Figure 5.39: *Yellow transistor leading.*

In Figure 5.40, the gates driver of the two transistors started simultaneously, resulting in a more evenly distributed voltage across the JFETs compared to the other pulses. However, this outcome only happened occasionally as the jitter caused the gate signals to vary significantly for each pulsing.

Figure 5.40: *Good results with good voltage balancing.*

5.5.2 Voltage probe comparison and calculation of parasitic capacitance of copper islands

Due to the variation in results, the voltage probes was tested to see if the difference between the probes was the source of the variations. The results are depicted in Figure 5.41, illustrating a 1.6ns delay between the probes.

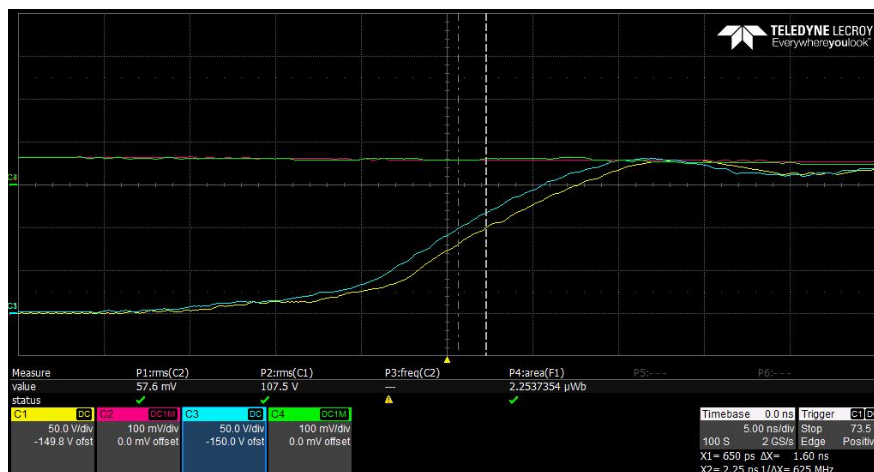


Figure 5.41: *Delaying between probes.*

In order to see if the uneven voltage distribution is caused by the parasitic capacitance of the copper islands to the return path, as highlighted in [16], calculations were performed. Calculating the capacitance of each copper island with Equation 5.13 yields a capacitance value of roughly 7.5 pF. Compared to the output

capacitance of the JFET, which is 280pF[23], it is negligible, leading to no uneven voltage distribution over the JFETs. However, it might be more of an issue as the voltage increases due to the increased dV/dt as the parasitic capacitance was low compared to the output capacitance. The parasitic capacitance was not deemed the source of the voltage balancing problems.

$$C = \frac{\varepsilon_r \varepsilon_0 A}{d} = \frac{4.4F/m \cdot 8.85 \cdot 10^{-12} F/m \cdot 0.015m \cdot 0.02m}{0.0155m} = 7.5pF \tag{5.13}$$

where ε_r is the relative permittivity of the FR-4 material, ε_0 is the permittivity of air, A is the areal of the copper island and d is the distance between the two conducting paths.

5.5.3 Implementing the new gate driver and adding resistors in parallel with the transistor

In an attempt to make the static voltage distribution more even, resistors were connected in parallel with each transistor. The resistance value was calculated with regards to the leakage current at drain-source breakdown voltage at 1200V[23]. The leakage current value was given at 1mA and the minimum voltage value of 1.2kV. If the leakage current is assumed to be linear with the breakdown voltage, the leakage current would be 625µA at 750V. The resistance value is then calculated to be 1.2MΩ. The estimations are moderate as the leakage current would, in reality, decrease faster than linearly as it is assumed to be.

To test if the uneven voltage distribution was caused as a result of the jitter of the 1ED020I12-F2[32] gate driver, a new and improved gate driver, ADuM4136 [33], was implemented. Figure 5.42 shows that as the new gate driver was implemented, the time from the gate signal to transistor turn off is reduced due to lower resistance in the output buffer of the gate driver. Most notably, the voltage distribution over the JFETs became significantly more even as the jitter is much smaller for the ADum4136 driver compared to the 1ED020I12-F2 driver[33][32].

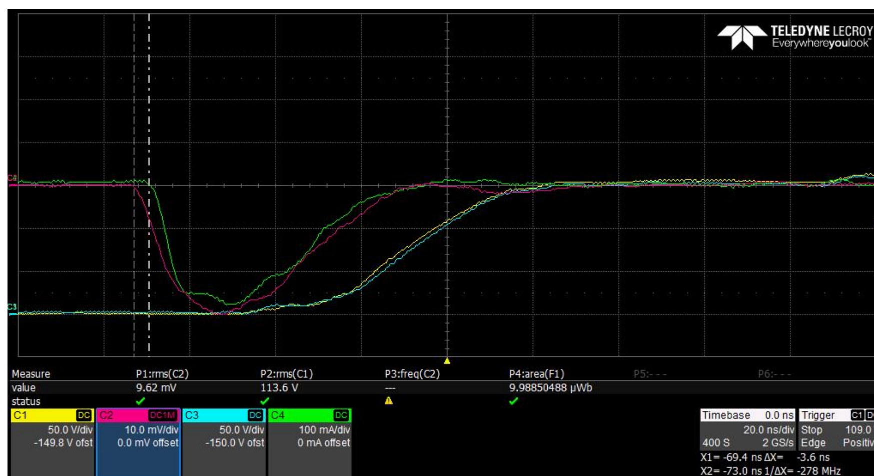


Figure 5.42: *Voltage distribution as the new gate driver, ADuM4136, is implemented.*

5.5.4 Highlighting the differences between soft and hard switching at turn off

To show the difference between soft switching and hard switching, Figure 5.43 depicts the voltage balance with soft switching, and Figure 5.44 depicts the voltage balance with hard switching. The difference between soft and hard switching is the current level at turn off. If the transistor is turned off while most of the current is still flowing in the channel, it is referred to as hard switching. On the other hand, if most of the current has been used to charge the output capacitance, resulting in much lower dV/dt, the transistors will soft switch and have significantly lower switching losses. Soft switching also leads to the voltage balancing being more evenly distributed over the transistors.

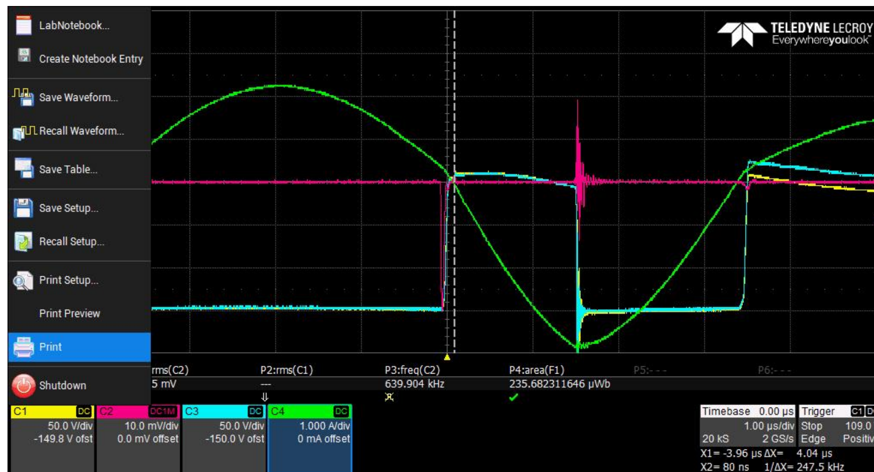


Figure 5.43: *Voltage distribution over the transitors when soft switching.*

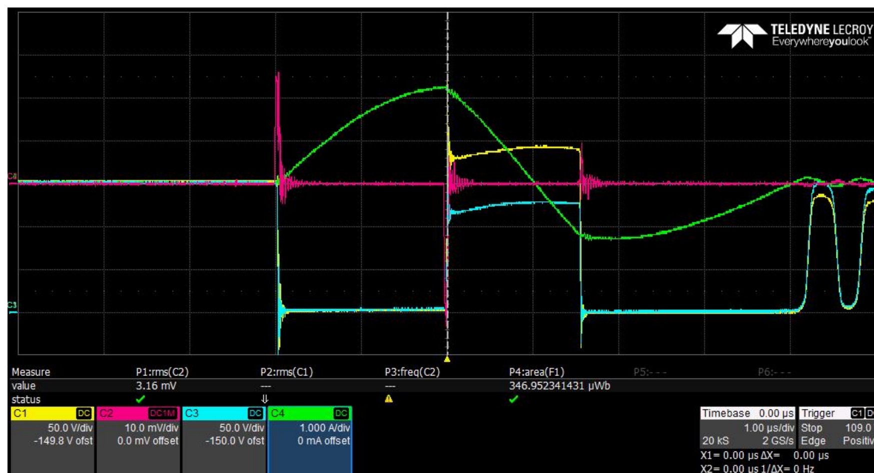


Figure 5.44: *Voltage distribution over the transitors when hard switching.*

In Figure 5.45 the consequences of hard switching are even more apparent. Hard switching causes significant oscillations and voltage unbalancing over the transistors. From the waveforms, it can be seen that the time delay between the gate current waveforms is 3.6ns.

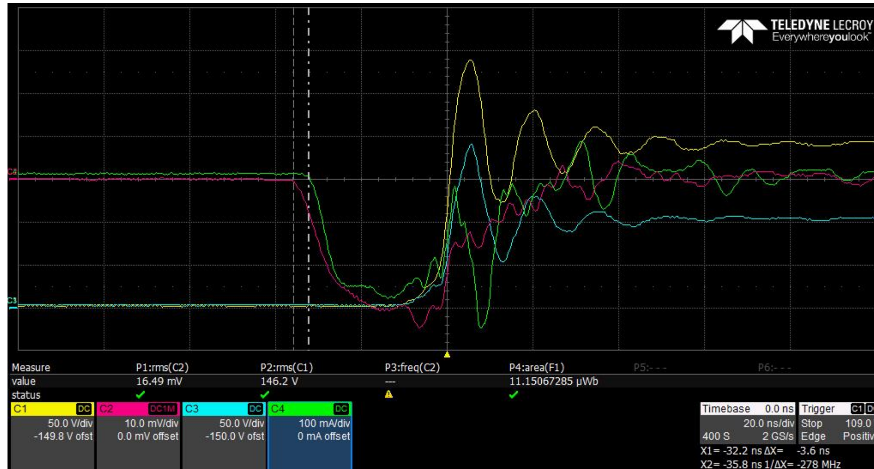


Figure 5.45: *Voltage unbalance and oscillations as a result of hard switching.*

5.5.5 Current probe comparison and tuning the gate drivers

Due to a time delay between the gate currents of 3.6ns in Figure 5.45, the current probes needed to be compared to see if the difference of the probes was the source of the time delay. In Figure 5.46, the current probes are connected to the same gate loop to see the difference between the probes. It can be seen from the waveforms that there is a time delay between the current probes of 1.8ns. Meaning the rest of the time delay, 1.8ns is the difference between each gate driver.

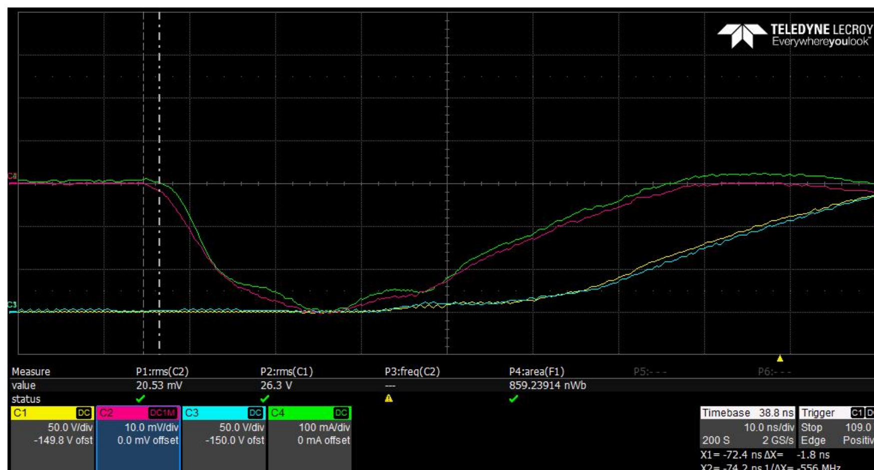


Figure 5.46: *Current probe comparison.*

To make up for the time delay between the two gate signals from the drivers there needed to be added a capacitor to make up for the roughly 2ns delay. In Figure 5.47, the gate driver input filter is presented. Notably, this is only a generic representation, and the real value of the R_8 and C_{82} is 22Ω and 680pF, respectively.

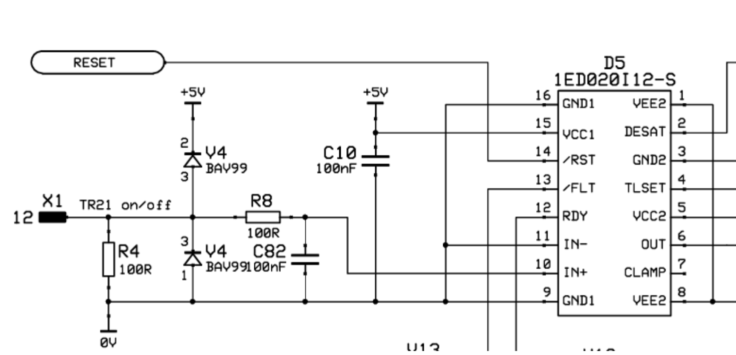


Figure 5.47: *Gate driver input filter(schematic illustrated is the EICE driver).*

The RC time constant of the 22Ω and 680pF is calculated to be roughly 15ns by using Equation 5.14. A capacitor of 100pF was connected in parallel C_{82} capacitor to bring the total capacitance up to 780pF.

$$\tau = R \cdot C \tag{5.14}$$

Figure 5.48 depicts the hard switching as the extra capacitance was added to the gate circuit with the previously leading gate current. From the waveforms, we can see that the yellow voltage wave was delayed by too much, and consequentially the other(blue) transistor turned off first, and most of the voltage ended up over the "blue" transistor.

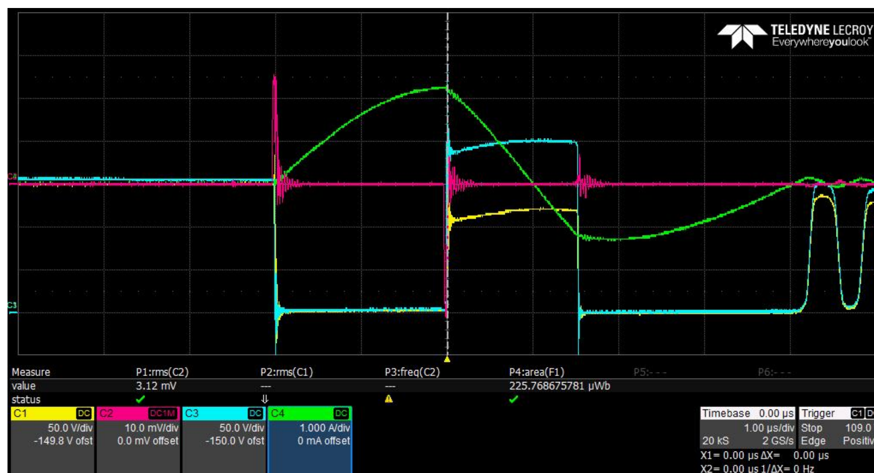


Figure 5.48: *Change in leading current due to the extra capacitor being added.*

As the previous results showed that the extra capacitance added made the blue transistor turn off faster, the gate circuits needed to be more finely tuned. In Figure 5.49, a 47pF capacitor was connected in parallel with the C_{82} gate driver to get better gate signal matching. This gave a very good voltage sharing as the transistors now turn off at approximately the same time.

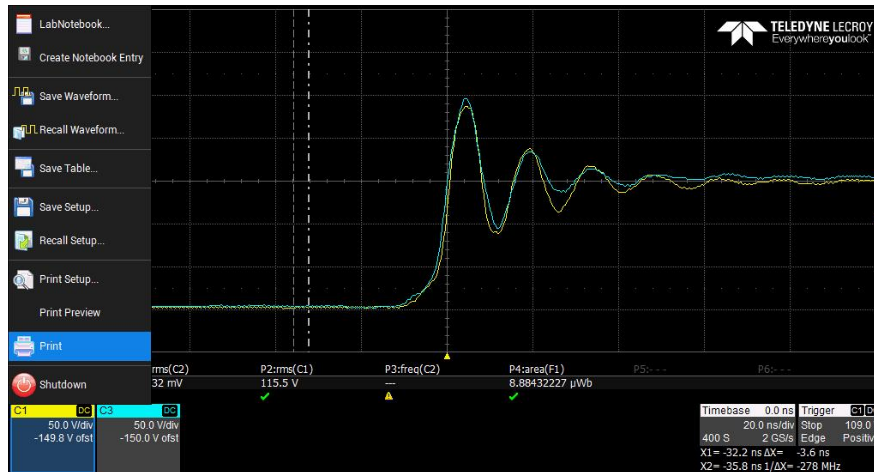


Figure 5.49: *Even voltage balance as a result of tuned gate circuits.*

5.5.6 Increasing the applied voltage

To this point, the testing was done at relatively low voltage of 300V DC. In the next experiments the jig is used to its full capability of 600V DC and with a peak current of 64A. In Figure 5.50, hard switching at the higher voltage is depicted. Figure 5.51 shows that the voltage balance becomes slightly more uneven at higher voltages. The voltage balance differences could result from the varying C_{oss} as a function of the voltage across the transistors[23]. Since the capacitance decreases with voltage, the voltage balance is more impacted by the parasitic capacitance of the copper islands. However, the voltage balance is still reasonably even due to the tuning of gate circuit signals.

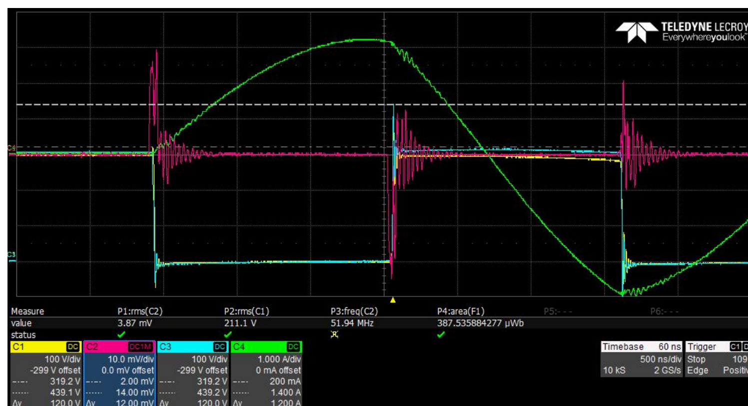


Figure 5.50: *Hard switched for the increased voltage.*

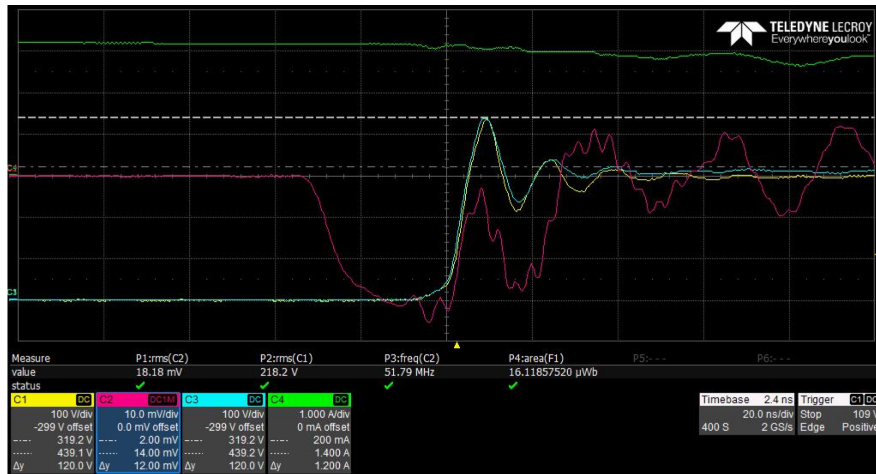


Figure 5.51: *Zoomed picture showing the voltage oscillations.*

In Figure 5.52, soft switching of the transistors at higher voltage is depicted. Figure 5.53 shows how the oscillations are almost entirely gone during soft switching.

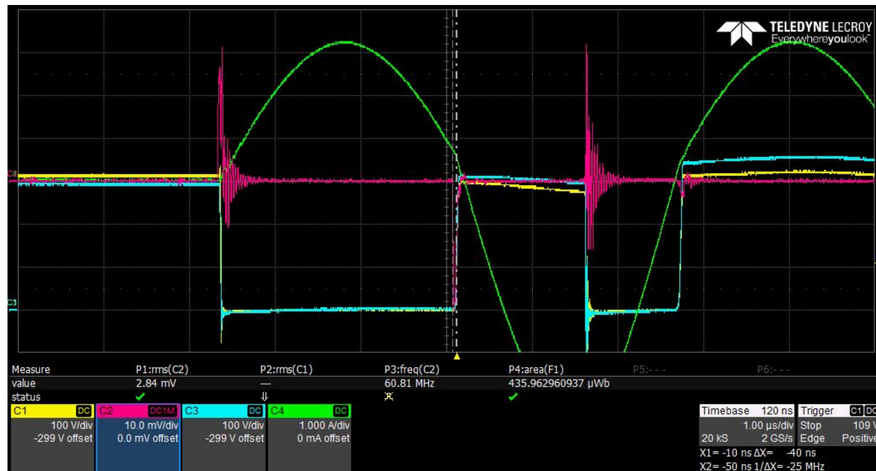


Figure 5.52: *Soft switching tuned at 600V and 64A.*

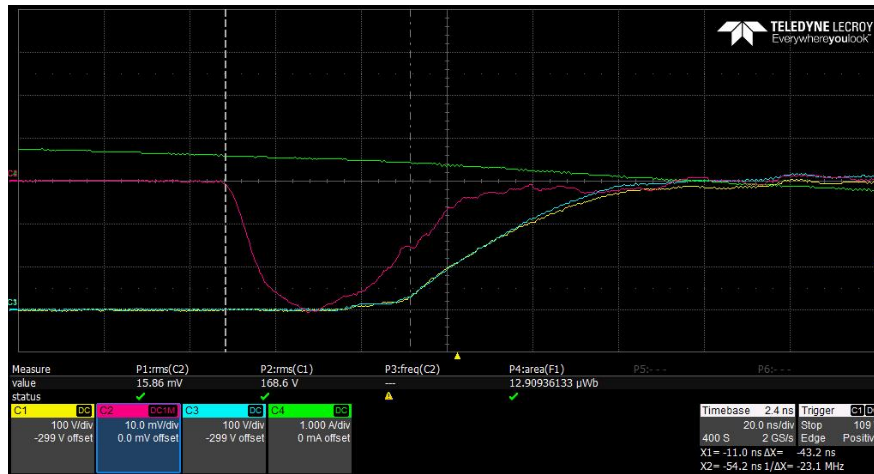


Figure 5.53: *Zoomed soft switching tuned at 600V and 64A.*

5.5.7 Measurement of current in the module and calculating the inductance of the module

To be able to measure current in the module, $13 \cdot 1\Omega$ current sense resistors with 1% tolerance[35] were connected in parallel to make it possible to make current measurements within the power loop. The total resistance of the parallel connection results in a total of $76.92\text{m}\Omega$. The resistance is connected in series with the power loop on the edge of the module, as depicted in Figure 5.54, the turn-off current is slightly decreased to 57A.

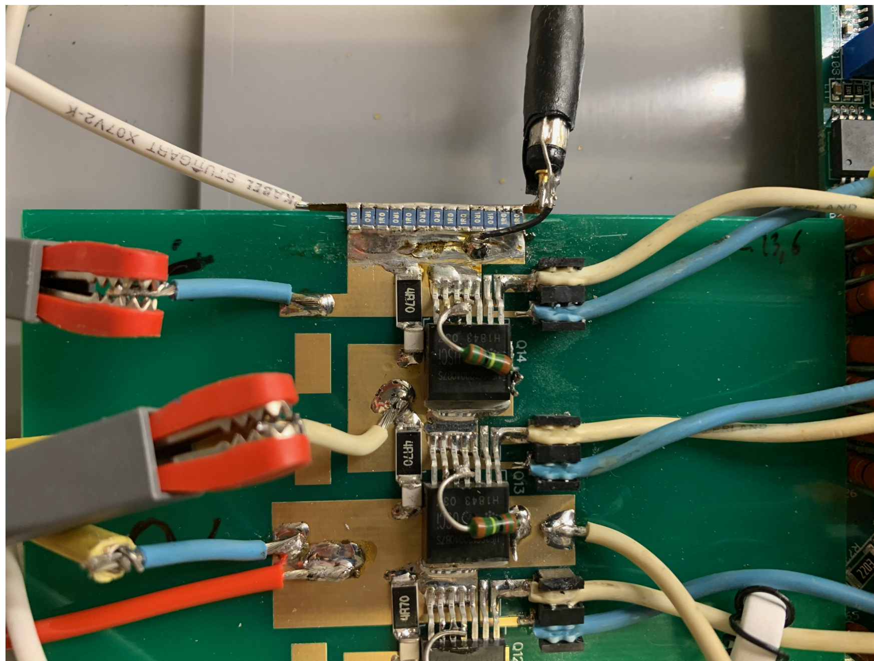


Figure 5.54: *13 1Ω resistances connected in series at the end of the positive current path.*

In Figure 5.55 and Figure 5.56 the overvoltages over each transistor in the lower side transistors are measured.

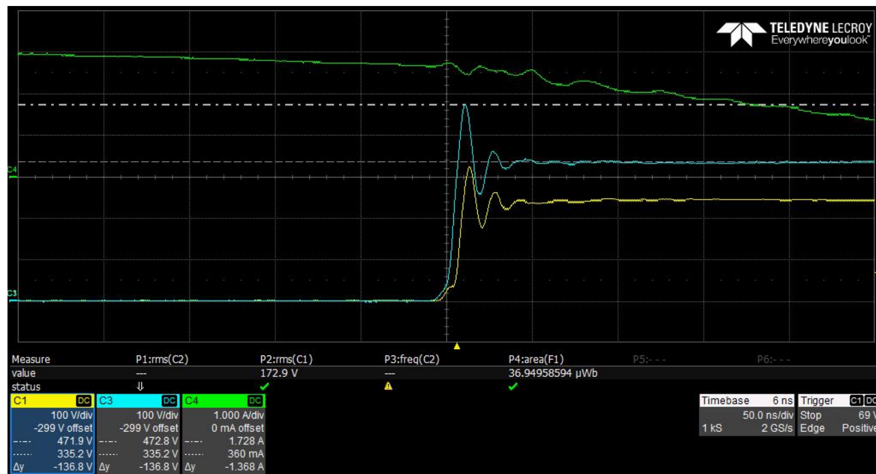


Figure 5.55: *Overvoltages of the "blue" transistor.*

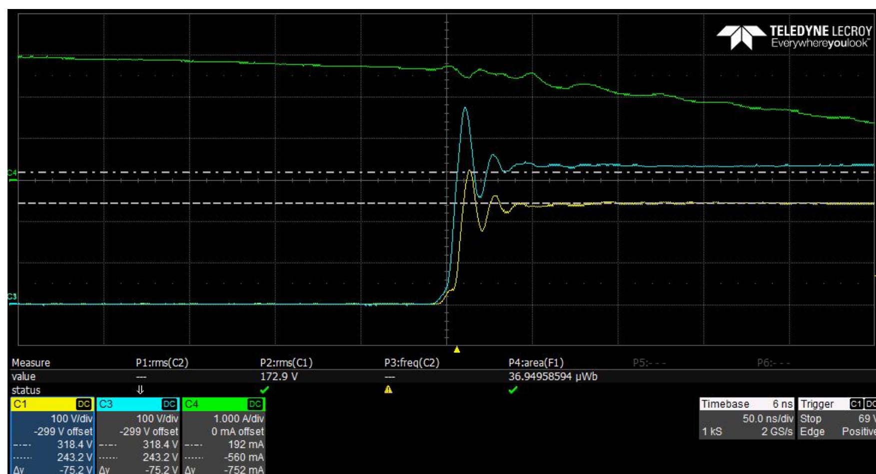


Figure 5.56: *Overvoltages of the "yellow" transistor.*

The overvoltages, together with the di/dt measured in Figure 5.57 are used to calculate the inductance.

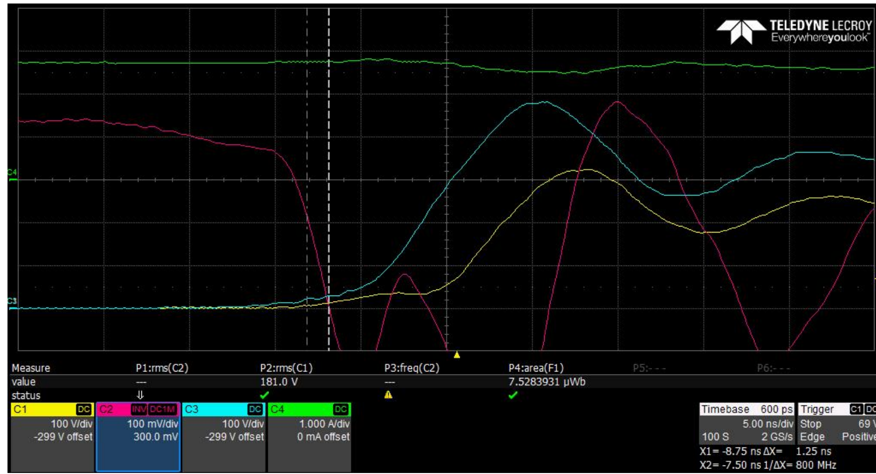


Figure 5.57: *Measurement of di/dt.*

As there is 1V/division of the oscilloscope and dividing that value by the resistance 76.92mΩ, the resulting ampere per division is 13A/division on the oscilloscope. Measurements done in Figure 5.57, shows the di/dt to be $2 \cdot 13A/1.25ns$ resulting in a final di/dt of 20.8A/ns. Overvoltages are measured in Figure 5.55 and Figure 5.56 to the be 136.8V and 75.2V, respectively. By using Equation 5.15, the total inductance of the layout is calculated to be 10.2nH. For reference, the inherent inductance in the JFET packages is given in the SPICE model to have a drain inductance of 3nF and a source inductance of 2nF. By multiplying the inherent inductance of the packages with the number of transistors used, the total inductance only from the packages is 20nH, showing the magnetic field cancellation's significant impact on the inductance of the power module layout.

$$L = \frac{V}{\frac{di}{dt}} \tag{5.15}$$

where L is the inductance, V is the overshooting voltages and di/dt is the rate of change of current.

5.5.8 Implementing a larger RC snubber for better voltage balance

As it can be seen from Figure 5.58, the voltage balancing between the transistors is quite uneven due to no gate signal matching for the lower series-connected transistors. The RC snubber connected in parallel for each transistor is only a 4.7Ω resistor and a 330pF capacitor.

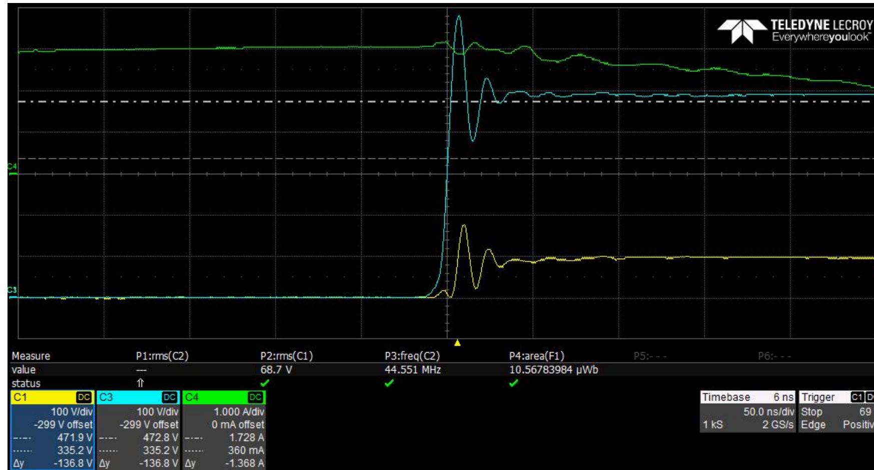


Figure 5.58: *Significant uneven voltage distribution across the lower series connected transistors.*

The results of the specialization project written in preparation for this thesis[21] showed that large RC snubbers were needed to get better voltage sharing between the series-connected transistors. Additional resistances and capacitors were added to the snubber circuits. Using the experience gained from the previous project, another 4.7Ω resistor and a 1nF capacitor were added and are depicted in Figure 5.60. The total resulting RC snubber was then 2.35Ω and 1330pF. As the transistor package utilizes a controlling MOSFET connected in series with a SiC JFET, the gate-to-drain capacitance is small, and the connection to the gate is only minor. As the voltage over the MOSFET is very low, only roughly 30V, the large gate-source loop will not affect the MOSFET significantly.

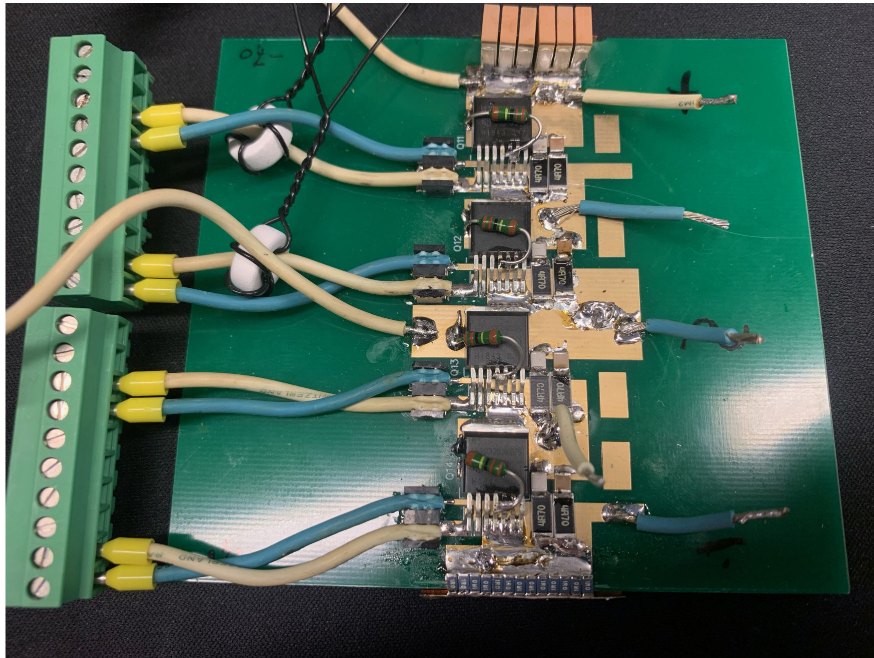


Figure 5.59: *Additional RC snubber added to the snubber circuits*

Figure 5.60 depicts how the voltage distribution was significantly improved. However, the voltage over the transistors is still distributed too unevenly for the module to function under high voltage operation. In order to achieve a better voltage balance, the gate circuits of the lower transistors could also be tuned. However, this was not done as the effect had already been highlighted.

Figure 5.60: *Improved voltage distribution as additional snubbers are added.*

6 Discussion

From the results in Table 5.2 and Table 5.3, it is clear that the terminal significantly impacts the total power loop inductance. By varying the width of the terminals from only 1mm to 9mm, the total inductance is reduced by 24% for DC simulations and 26% for AC simulations. As these results are only simulated for a frequency of 10kHz, the difference could potentially be even larger for higher frequencies as the magnetic cancellation would be more prominent. In conventional power module packages, the terminals are large sources of inductance as they are often relatively large in size compared to the total package layout. However, from the simulation results, the greater the width of the terminals, the lower the inductance due to the magnetic field cancellation and widening the current path. As the gap between the terminal decreased, the inductance of the power modules also decreased. By reducing the gap distance from 2.5mm to 0.5mm, the DC inductance is decreased by 5% and the AC simulations 14%. The same rule applies to the simulations for gap distance, as the results would presumably show that the difference would be even more significant at higher frequencies.

In Figure 5.5 and Figure 5.6, the total loop inductance difference as the gap between the positive path of the Halfbridge module and the return path for the current is changed from 2.5mm to 0.5mm is shown. The inductances at 10MHz are roughly 18.5nH and 9.25nH with 2.5mm and 0.5mm gap sizes, respectively. At 10kHz, the inductance with varying gap distances is roughly 24.2nH and 14.1nH. The same trend is showing in Figure 5.3 and Figure 5.4, where the total loop inductance at 10MHz was reduced from 9.8nH to 7.2nH when the substrate thickness were reduced from 0.63mm to 0.25mm. At 10kHz, the inductance was reduced from 17.6nH to 15.7nH when the substrate thickness was reduced. These results show the substantial effect reducing the distance between the positive path, and the return path of the module has on the total power loop inductance. The inductances for the Halfbridge module are reduced by 50% for higher frequencies and 42% for lower frequencies.

For the NegativeLayer module, the inductance is reduced by 27% for higher frequencies and 11% for lower frequencies. The impact on the Halfbridge module is significantly higher due to the distance being reduced compared to the distance change for the NegativeLayer module. In both Table 5.4 and Table 5.5, the total inductance of the positive and return path is simulated and compared to the total loop inductance. The total inductance of the Halfbridge module and the NegativeLayer module are 74.842nH and 65.768nH, respectively. Comparing the total inductance without magnetic flux cancellation to the scenario where the cancellation is in effect results in a total inductance decrease of 72% for the Halfbridge module and 85% for the NegativeLayer module.

For the new packaging layout designs in this thesis, the gap distance between the copper islands of the DBC was set to 2.5mm to prevent breakdown voltages between the different voltage potentials. However, according to Paschen law[42], the gap size might have been too conservative to achieve a very low inductive power module packaging layout. Especially if silicon gel was used as encapsulant rather than air encapsulating the power dies and the DBC of the module. The dielectric constant is about three times higher for silicon gel compared to air[26], and adding silicon gel would reduce the risk of moisture or dust in the power module contaminating the environment and making voltage breakdowns more probable. In Figure 5.7 and Figure 5.8, it is shown that the inductance of the power module is significantly decreased as the gap distance, and therefore the power loop length is reduced. By reducing the gap distance from 2.5mm to 1.0mm, the inductance at 10MHz is reduced by 14% and at lower frequencies, the inductance is reduced by roughly 12.5%.

Bondwires represent a large part of the inductance in power modules due to the self-inductance of the bondwires being high as a result of a small diameter and a narrow conducting path. Therefore, using multiple bondwires connected in parallel or utilizing technology like the flex foil used in [13] could result in a significantly lower stray inductance as the conducting path of the interconnection is wider. In a more realistic scenario, the bondwires could also lead to even more stray inductance than presented in this thesis due to the bondwires having to be placed on the padding of the die[18]. During simulations, the bondwires were connected to the end of the die to get bondwires as short as possible and for simplicity's sake. Various types of bondwires were simulated. However, the different bondwire types did not have a significant impact on the inductance of the layout. During the lab experiments, the bondwires were not included as the layout was specifically designed for a TO-263-7L package, the impact of the bondwires on the inductance was therefore not observed in the lab experiments.

In the lab experiments, the inductance of the layout was found to be 10.2nH, which is pretty accurate compared to the NegativeLayer layout which is approximately 9.8nH with a substrate thickness of 0.63mm and at 10MHz. The NegativeLayer module is chosen as it inhabits a structural design comparable to the module tested in the lab experiment. However, there are still differences between the tested module and the NegativeLayer model, such as the use of bondwires during simulations, as earlier mentioned, compared to the TO-263-7L package and the DC link capacitors having an inherent inductance. The FR-4 substrate was also significantly thicker than the simulated substrates, with a thickness of 1.55mm compared to the 0.63mm, which was the thickest of the simulations. If the thickness of the PCB print was reduced to 0.63mm in the lab experiments, the total inductance could be significantly decreased.

The drain inductance and source inductance of the SiC FET was found to be 3nF and 2nF, respectively, in the SPICE model from Wolfspeed[23]. Therefore, the resulting inductances from all the SiC FET packages are 20nF as there are four SiC FETs in the power loop. Since the total power loop inductance was found to be 10.2nF, the magnetic field cancellation is shown to have a significant impact on the inductances as the total loop inductance is 50% of the inherent inductance of the packages. When only the inductance of the packages are compared, the total loop inductance, without the magnetic field cancellation, of the module should be significantly more than only the inherent package inductance, further adding to the great effect the magnetic field cancellation has on the inductance. The effect would be even more exacerbated if the substrate during the lab experiments were thinner.

Voltage simulations were not included in the simulation chapter using ANSYS Maxwell as the voltage would be determined by the capacitive connection between each copper island and the copper layer below each island. The capacitive connection was calculated in 5.5 and was considered insignificant compared to the output capacitance of the power dies used in the experiments[23], and were therefore excluded from the simulations. The electrostatic solver was chosen in the electric field simulations performed in Maxwell due to issues when utilizing the electric transient solver. The electrostatic solver only computes static (DC) electric fields, and the simulations for electrical fields are therefore not simulated for transient voltages. However, to make simulations for investigation of the electrical fields when one MOSFET is turned off, 2kV was applied at the terminal, and 1kV was applied on the copper island after the turned off MOSFET. The electric transient simulations could be performed in future works to get more realistic electrical fields during the switching of the MOSFETs.

As discussed in 5.3 and [15], there are certain difficulties as meshing is introduced to simulations. In Table 5.6 the electrical field difference is shown as the meshing accuracy of the geometries in the model is increased. Judging whether the results are due to the meshing representing a more realistic model or if the electrical field is increased due to the crowding effect is difficult. However, by rounding the edges of the DBC, the electrical field was significantly reduced at the critical point. The electrical field was reduced by 68% when the encapsulant was silicon gel and 63% under air simulations. Comparing Figure 5.11 and Figure 5.13 the results along point 2 seems to be relatively similar. Lastly, as all of the edges of the DBC were rounded as depicted in Figure 5.14, the electrical field strength was further reduced to $4.0498 \cdot 10^6$E. Resulting in another significant reduction of electrical field strength at the critical point of 82% compared to the electrical field with sharp edges. These results highlight the importance of rounding the edges of the DBC as the electrical fields are significantly decreased, and the module is better protected against electrical stress.

In the electrical field simulations, there were also simulated instances with different heights of the bondwires. The electrical field in the critical point depicted in Table 5.9 seems not to be particularly affected by the variation in height as it only changes with roughly 1.5% between the lowest and the highest value. In Figure 5.15 the impact of the varying bondwire height along point 2 between the two copper islands is shown. There was almost no change from 0.8mm to 1.2mm. However, there are differences between the 0.4mm height bondwire and the two aforementioned, as the electrical field is reduced exactly at the first copper islands for the higher bondwires. Notably, the reverse effect appears for the second copper islands, where the higher bondwires have a larger electrical field.

The results from changing the ceramic substrate thickness are depicted in both Figure 5.18 and Table 5.10. Around the first copper island, the electrical field is strongest as the substrate is thinner. This trend changes after 0.25mm from the first copper layer as the electrical field is now larger for the thicker substrate. For the last section between the copper islands, it is hard to see the difference between the plots, but from the table values, it is shown that the latter trend is still ongoing. As the measuring point are closer to the second copper island, the electrical field strength for the thicker ceramic substrate is 2-7 times stronger than the electrical field for the thinner ceramic substrate simulation.

According to [43], the average voltage breakdown of silicon gel is 14kV/mm at a gap distance of 1mm for AC voltage. The average breakdown voltage is further increased to 33kV/mm when DC voltage is applied. In the electrical field simulations, the peak value of the fields was $1.925 \cdot 10^7$ V/m in the critical area, which is 19.25kV/mm when converted. However, the electrical field peak value was during the sharp edge simulations. As the edges were rounded, the electrical field at the critical point was reduced to 7.28kV/mm and even further to 4.05kV/mm as all edges were rounded. Therefore, it should be possible to move the copper islands significantly closer to each other without worrying about voltage breakdowns between them. The height of the die in the simulations was set to 0.2mm, meaning the distance from the drain potential of the first copper island to the drain potential of the other MOSFET(the bondwires) is only 0.2mm. In Figure 5.17 the peak electrical field value was 2.08kV/mm, meaning there would be no voltage breakdowns even if the distance were only 0.2mm to the bond wire. Notably, the simulation assumes silicon gel without air bubbles.

In the thermal simulations scenario with an ideal heatsink, the thermal resistance of the NegativeLayer module is found to be 0.423°C/W. Instinctively, the thermal resistance of the NegativeLayer module should be higher than the thermal resistance of conventional modules due to the design's structural differences. The NegativeLayer module has two ceramics layers which increase the thermal resistance due to the material's thermal conductivity. The higher thermal resistance can be explained by the module being naturally thicker because of the increased number of layers. The cross-sectional areas of the power module are not as big due to the module being smaller than conventional modules, which could also lead to larger thermal resistance. The module was shown to be able to operate within a DC to DC converter under conditions of 1600V if there is an even voltage balance over the transistors and 43A drain current. The resulting power rating of the module would then be 68.8kW. Notably, the converter's duty cycle was set to 99%, demonstrating a worst-case scenario with a switching frequency of 20kHz. For lower duty cycles and frequencies, the module should be able to operate for even higher currents.

In the simulations with various heat transfer coefficients at the bottom of the baseplate, the thermal resistance varied significantly depending on the htc. For the bad water cooling heatsink with a htc of $3000 W/m^2K$, the thermal resistance was found to be 0.897 °C/W, which is most likely not acceptable for high-temperature operation. As the htcs were increased to $10000 W/m^2K$ and $20000 W/m^2K$, the thermal impedances were reduced to 0.56°C/W and 0.473°C/W, respectively. The total power allowed generated at the die was increased by 60.5% and 89% when replacing the worst heatsink with the improved ones. Interestingly, the thermal resistance of the module was only increased by 2.3% when the copper islands and the dies were moved closer to each other. The more densely packed module was a viable option for lowering the inductance as the electrical fields were not close to exceeding the safe values for breakdown voltage, and the thermal resistance was only slightly increased.

The significant importance jitter plays when transistors are connected in series is clearly shown in 5.5. With the first gate driver, the variance of results was considerable. The voltage balance across the transistors was constantly changing for each pulse, making the use of this driver not suitable for series connection of SiC MOSFET/SiC JFET cascodes. As shown in the lab experiments and the specialization project written before this thesis [21], only a couple of nanosecond differences in the timing of the gate signals can result in significant voltage unbalance. As the more modern gate driver, ADuM4136, was introduced, the jitter was significantly reduced, and the results became more reliable. However, even with a modern gate driver, there is a level of voltage unbalance, which would not be acceptable during operation.

In the lab experiments, it was shown that it was possible to tune the gate circuits to get matching gate signals, resulting in a more even voltage balance over the transistors. However, this is not a viable solution for mass-producing power modules as it requires testing and tuning each gate driver. To compensate for the variation in the gate drivers, only one controlling device, such as presented in [16], could be implemented to eliminate the challenges of utilizing several drivers. Additionally, it was shown in both the lab experiments and the specialization project that large RC snubbers were crucial to gaining better voltage balance over the transistors and dampen voltage oscillations. Lastly, the difference between soft switching and hard switching is highlighted. The voltage balance and oscillations are significantly improved by soft switching the devices.

7 Conclusion and suggestion for further work

This chapter will present the major conclusions drawn from all of the work done in this thesis and discuss further work that can improve the designs.

7.1 Conclusion

In this thesis, the theoretical background required to understand the operation of the MOSFET is presented to provide context for the following chapters. The state-of-the-art chapter presents several articles highlighting new and advanced technologies used as reference when designing the new power modules. During this thesis, two power module designs, Halbridge and NegativeLayer, were designed to achieve a low inductive power module layout while still considering challenges such as voltage breakdowns and thermal management.

To achieve a low inductive design, the magnetic flux cancellation phenomena was used to cancel out the inductance between the positive and return paths for the current in both designs. In the Halfbridge module, the return path was placed over the positive path. In the NegativeLayer module, the return path was placed under the positive path with a ceramic substrate between the paths. The inductance simulations of the two packages revealed how many factors affected each module's total loop inductances. For both layouts, the width and gap distance between the overlapping terminals and the length of the distance between the copper islands of the DBC played a large role in the inductance. By decreasing the distance between the positive and return path carrying the current, the total power loop inductance was significantly reduced. Utilizing the magnetic flux cancellation, the total effective power loop inductance was significantly reduced for both the Halfbridge module and the NegativeLayer module.

In the electric field simulations, it was discovered that by rounding the edges of the DBC, the electric field strength was substantially reduced. First, the vertical edges of the DBC were rounded, resulting in a decrease in electrical field strength at the critical point of 68%. By rounding the horizontal edges of the DBC as well, the electrical field strength was further reduced at the critical point by 82%, compared to the electrical field strength when all edges were sharp. The effect of rounding the edges was conclusive. However, it is unknown how much of the difference in the result was due to the field crowding effect. The effect of using silicon gel as an encapsulation compared to air was also discovered to result in weaker electrical fields around the DBC. The effect of silicon gel was especially apparent at the critical point of the DBC. Decreasing the thickness of the ceramic substrate for the NegativeLayer model also resulted in the electrical field strength being significantly reduced.

The thermal capabilities of the NegativeLayer module were analyzed in the thermal simulations. The thermal resistance of the module was discovered to be 0.423K/W, with an ideal heatsink constantly keeping the temperature of the bottom side of the baseplate to 22°C. When calculating the power losses for the SiC MOSFET dies chosen in this thesis, the worst-case scenario was assumed as the converter's duty cycle was set to 99%. Under these conditions and with a voltage of 800V and a drain current of 43A, the power generated at each die was still lower than the acceptable power generated at the die with the simulated thermal resistance. Thermal simulations for various water cooling heatsinks were performed, and the thermal resistances for each case were found. Although the NegativeLayer module has several ceramic substrates and has many different layers, the thermal resistance of the module was sufficient for heatsinks with good heat transfer coefficients.

Notably, the thermal resistance of the module was only slightly increased as the distance between the copper islands in the DBC was reduced from 2.5mm to 1mm.

In the lab experiments performed at EFD Induction, the importance of accurate gate drivers and the significant difference between soft and hard switching was discovered. Replacing the older gate driver resulted in significantly less jitter and more even voltage distribution over the series-connected transistors. However, even with modern gate drivers, the voltage distribution was still uneven due to the gate drivers turning off the transistors at different times. In order to use transistors connected in series with separate gate drivers, the accuracy needed is extremely high, and the delay between the signals of the gate drivers cant be more than 2-3ns. Better results were obtained as the gate circuit was tuned by adding capacitance manually, but manually tuning the gate circuits is not a viable solution if the power modules are mass manufactured. Resistors were connected in series with the transistors to be able to measure the current. The current, together with the overvoltages, resulted in the inductance of the module being 10.2nH. The inherent drain and source inductance of each package was found to be 3nH and 2nH, respectively, meaning that magnetic flux cancellation was of great significance. Lastly, additional snubbers were added in parallel with each die to try to even out the voltage balance. However, the lab experiments highlight how difficult achieving an even voltage balance over the transistors is when connecting transistors in series.

7.2 Suggestion for further work

In this thesis, it has been discovered that conventional power module packaging technologies have much room for potential to make packages that are more compact and have less inductance while still maintaining safe distances for voltage breakdowns and good thermal capabilities. Some suggestions for improving the power module designs for further work are presented.

To continue to improve the power modules designed in this thesis, it would be interesting to investigate how low the inductance of the package could get if the gap distances were reduced while still keeping a safe distance to prevent voltage breakdowns. It was discovered in this thesis that the inductance was greatly reduced as the copper islands were moved close to each other to obtain a more dense package. Advanced interconnection methods such as the flex foil technology used in the SKiN technology could even further reduce the inductance.

In the thermal analysis section of the thesis, it would be interesting to investigate further how to improve the thermal capabilities of the designs. Including the soldering layers and adding a heatsink in the thermal simulations should also be implemented to get a more realistic picture of the thermal characteristic of the power modules.

As was discovered in the lab experiments, the gate drivers have to be extremely accurate, more than the modern gate drivers we have currently, to achieve an even voltage balance over transistors in series. A solution to the problem could be to utilize several JFETs in series with a controlling MOSFET as done in [16]. Controlling the switching of the transistors eliminates the problem of the gate drivers not being accurate enough.

The capacitive parasitics were not investigated during this thesis. This could be something that can be interesting to examine in-depth to gain an even deeper understanding of how the layout of the packaging

designs impacts the capabilities of the power module. In other articles investigating the series connection of transistors, the parasitic capacitance has been shown to play a significant role in the switching capabilities of the transistors and should therefore be further investigated.

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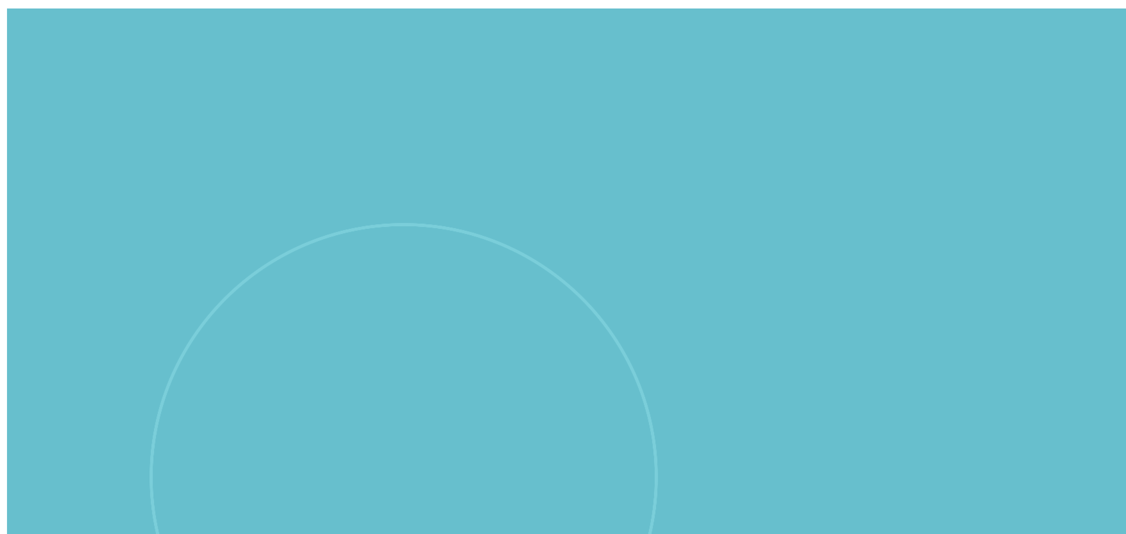
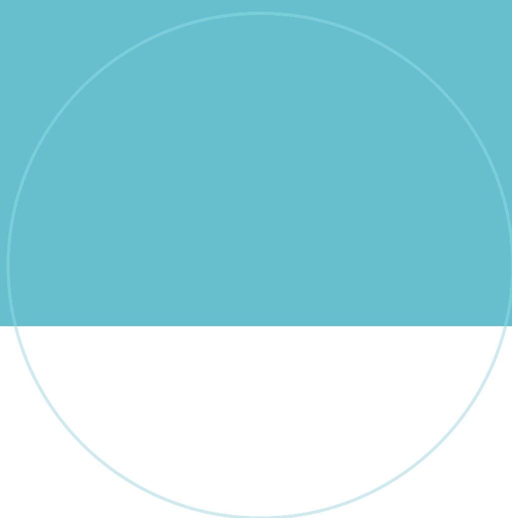

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