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Performance Evaluation and Limitations of Overvoltage Suppression Circuits for Low- and Medium-Voltage DC Solid-State Breakers

ANDREAS GIANNAKIS (Student Member, IEEE), AND DIMOSTHENIS PEFTITSIS (Senior Member, IEEE)

Department of Electric Power Engineering, NTNU, 7491 Trondheim, Norway

CORRESPONDING AUTHOR: ANDREAS GIANNAKIS (e-mail: andreas.giannakis@ntnu.no)

ABSTRACT This paper presents a design and performance evaluation of three different overvoltage suppression circuits employed in a solid-state circuit breaker for medium- to high-power and low- to medium-voltage DC grids. The evaluated criteria are the requirements for passive components, as well as the breaker performance in terms of peak switch overvoltage, peak short-circuit current, fault clearance time and rate of voltage rise during the fault clearing process. Additionally, the impact of the stray inductance in the solid-state breaker design on the anticipated overvoltage is also investigated. Design and operating limitations of each configuration from an application perspective are also discussed. From simulations of a 1.8 kV and 500 A breaker for high-power medium-voltage DC applications it is shown that the most effective overvoltage suppression is achieved by means of using a metal-oxide varistor and a snubber capacitor connected in parallel with the main switch at a cost of high fault current. A medium-power solid-state DC breaker prototype rated at 1.5 kV and 50 A was also designed and constructed. The experimental results reveal that using only a metal-oxide varistor can be sufficient when the breaker employs high-voltage discrete semiconductors with long current falling time and is used in medium-power medium-voltage grids.

INDEX TERMS DC circuit breakers, insulated gate bipolar transistors, overvoltage protection, short circuit currents, snubbers.

I. INTRODUCTION

Low-and medium-voltage DC (LVDC and MVDC) grids are attractive grid concepts for electricity distribution due to their advantageous characteristics compared to the MV alternating current (AC) counterparts [1]–[7]. A decisive factor for the envisaged expansion of LVDC and MVDC grids is the advancement in high-power semiconductors technology [7]. Recently, a vast variety of LVDC and MVDC grid applications such as collector grids for offshore wind and solar power [7]–[10], marine vessels [6], [11]–[13] and other industrial applications [14]–[18] has been identified.

Today, one of the main showstoppers for LVDC and MVDC grid realization is the lack of high performance short-circuit protection systems [1], [19]. The inherently low inductances occurring in these grid concepts, mostly due to the short power lines and the absence of transformers (i.e. lack of leakage inductance), lead to the rapid rise of the fault current. As a result, the short-circuit current reaches excessive values and imposes the need for very fast fault breaking mechanisms. Traditional mechanical AC breakers cannot clear direct fault currents due to the absence of natural zero crossing for the current. Three main direct current circuit breaker (DCCB) topologies have been proposed so far [1], [20], [21]: mechanical DCCBs with active/passive resonance circuit, solid-state DCCBs [22], [23] and hybrid DCCBs [24]–[27]. The most suitable type of DCCB for LVDC and MVDC grids should be chosen based on the design and operating constraints of the loads and power sources connected to the grid, as well as, the design and operating limitations arised in the grid itself.

Today, the ever-increasing integration of renewable energy sources [28] and large-scale battery storage systems, as well as, electrification of marine vessels using DC distribution grids onboard [11], necessitate the use of fast-performing DC protection systems. For example, if sensitive loads (e.g. loads onboard a marine vessel) or sensitive power sources (e.g. utility-scale battery storage systems) are integrated with

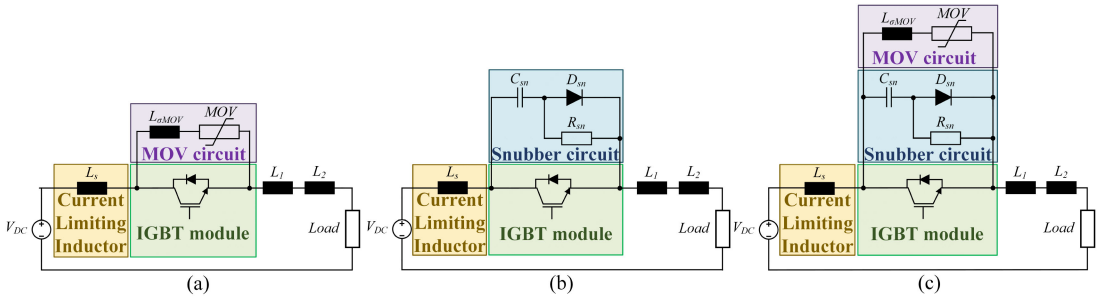

FIG. 1. **The three investigated configurations: (a) CON1, (b) CON2 and (c) CON3.**

the DC grid, a priority is to limit and clear the short-circuit current in a relatively short time. Short clearing time is the key to ensure sufficient reliability of sustainable electricity supply, which becomes more dominant in multi-terminal MVDC grids [29], [30]. In such cases, the solid-state CB will be the favorable breaker solution for the MVDC grid operators and it is, therefore, analyzed in this paper.

The major design challenge of a solid-state CB is the high conduction power losses and the overvoltage suppression circuitry design and size [31]–[34]. Increased voltage ratings of power semiconductors might soften the design requirements of the overvoltage suppression circuits for a given grid voltage. However, the anticipated conduction losses will increase as the breakdown voltage capability increases. Therefore, choosing and designing the overvoltage suppression circuitry properly is crucial for an optimized operation of the solid-state breaker. The contribution of this paper is to investigate and evaluate the impact of three overvoltage suppression configurations on the solid-state CB design and performance, as well as, on the overall design of the breaker for medium- and high-power DC applications rated up to $1.8kV_{DC}$. A down-scaled prototype that is suitable for medium-power and low- to medium-voltage applications (rated at $1.5kV_{DC}$) has been built, where a single high-voltage discrete semiconductor device can be used as the main switch for the solid-state breaker. Additionally, simulations have been performed for high-power MVDC applications employing high-power and high-voltage semiconductor modules in order to demonstrate the suitability and performance of three overvoltage suppression configurations at high-power grid cases.

The paper is organized as follows. The main challenges of solid-state DCCBs is analyzed in Section II. The circuit analysis and the design principles of the investigated overvoltage suppression configurations employed in a solid-state breaker are presented in Sections III and IV, respectively. Section V presents the case study and the simulation results for high-power $1.8kV_{DC}$ applications. The down-scaled prototype and the experimental results for medium-power solid-state DC breakers rated up to $1.5kV_{DC}$ are described in detail in Section VI. Finally, Section VII summarizes the presented study and provides the main conclusions.

II. MAIN CHALLENGES OF SOLID-STATE CIRCUIT BREAKERS

The main structure of an interrupting solid-state breaker is illustrated in Fig. 1. High-voltage semiconductor devices and voltage clamping circuitries are key components for the realization of solid-state CB. The required overvoltage suppression circuitries protect the switches from overvoltage caused by the inductances involved in the DC grid. In other words, these circuitries must be capable to dissipate the energy stored in the above mentioned inductances.

In literature, several overvoltage suppression topologies for high-voltage semiconductor devices have been identified [35]. However, the majority of them is applied to switches employed in switch-mode power converter topologies rather than solid-state breakers. Liu *et al.* in [34] presented a comparative study of three overvoltage suppression schemes for solid-state breakers for low-voltage applications rated at $\pm 200V_{DC}$. However, when higher voltage applications are need to be considered, different design and operating principles in terms of voltage isolation and utilization of the blocking capabilities of high-voltage switching devices are imposed. This is associated with larger parasitic inductances in the breaker circuit layout due to the larger physical size of the components, as well as the longer electrical conductors. Additionally, the impact of the breaker design on the stress of other grid components may also be more severe due to higher power. Therefore, a comparative study on various overvoltage suppression schemes for solid-state DCCBs rated at higher than $400V_{DC}$ in terms of design and performance is necessary. In this study, three overvoltage suppression configurations will be analyzed and investigated, emphasizing the transition from low-voltage to medium-voltage applications by means of experiments. These are the Metal-Oxide Varistor (MOV) (CON1), the Resistive-Capacitive-Diode (RCD) snubber circuitry (CON2) and the combination of both MOV and RCD snubber circuitry (CON3). The evaluation criteria are: (i) the peak switch voltage ($V_{sw_{peak}}$), (ii) the peak short-circuit current ($I_{sc_{peak}}$), (iii) the clearance short-circuit time (t_{cl}), (iv) the switch voltage rise rate (dv_{sw}/dt), and (v) the energy dissipation in the switch (E_{sw}), as well as the requirements for passive components.

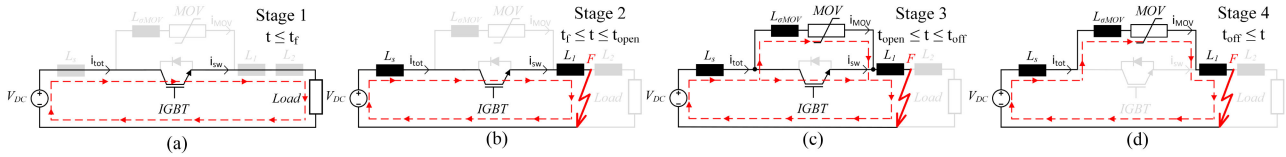

FIG. 2. Schematic diagrams of the discrete operating stages of the solid-state DCCB CON1.

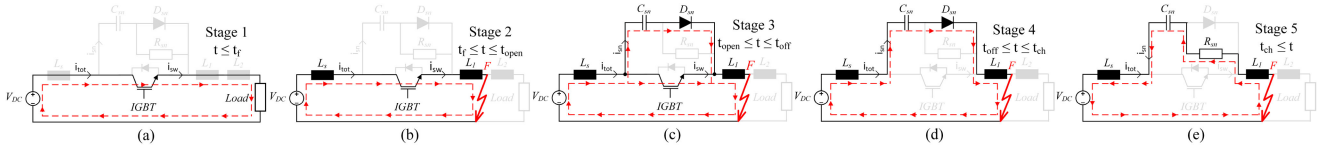

FIG. 3. Schematic diagrams of the discrete operating stages of the solid-state DCCB CON2.

III. CIRCUIT ANALYSIS AND OPERATING PRINCIPLES OF CON1, CON2 AND CON3

This section presents the operating principles of the three overvoltage suppression circuitries that are investigated. For the present analysis, as well as for the rest of the investigations the Insulated Gate Bipolar Transistors (IGBTs) have been considered for the switches in the breaker.

A. CON1: SOLID-STATE DCCB WITH MOV

Fig. 1(a) illustrates a solid-state DCCB consisting of a current limiting inductor, L_s, an IGBT switch and a MOV connected in parallel. In addition to these, the stray inductance of the MOV path, ($L_{\sigma MOV}$), has been taken into account. Four operating stages during a short-circuit condition can be identified and they are illustrated in Fig. 2.

- Stage 1: $t \leq t_f$: It represents the stage without any short-circuit fault occuring in the line (i.e., prior to t_f). The DC current flows from the source to the load through the power semiconductor device.
- Stage 2: $t_f \leq t \leq t_{open}$: The short-circuit occurs at the time instant t_f, which initiates the next stage. The current limiting inductor limits the rise of the fault current to a specified value within a certain time interval.
- Stage 3: $t_{open} \leq t \leq t_{off}$: The fault is detected and the command to turn-off the power semiconductor device is given at the time instant t_{open}. Then, the voltage across the device starts to increase until it reaches the clamping voltage of the varistor. When this happens, the current through the IGBT falls and it commutates to the MOV branch. The time instant t_{off} denotes the zero crossing of the semiconductor current and therefore, the end of stage 3. During this stage, the power dissipation in the switch can be excessively high, which might degrade the device characteristics.
- Stage 4: $t_{off} \leq t$: Once the short-circuit current has completely commutated to the MOV, the last stage is initiated. The short-circuit has been cleared when the MOV voltage drops to the clamping voltage.

B. CON2: SOLID-STATE DCCB WITH RCD SNUBBER

The use of an RCD snubber circuit connected in parallel to the main switch aims at suppressing the overvoltage during the fault interruption process. Fig. 1(b) illustrates a solid-state DCCB with RCD snubber circuit and Fig. 3 shows the different operating stages during a fault clearance process.

- Stage 1: $t \leq t_f$: Fig. 3(a) shows the normal operation of the DC grid before the short-circuit occurs.
- Stage 2: $t_f \leq t \leq t_{open}$: Stage 2 is initiated when the short-circuit occurs and it lasts until the fault has been detected and a command has been given to open the switch (t_{open}). During this interval, the fault current is limited by means of the current limiting inductor.
- Stage 3: $t_{open} \leq t \leq t_{off}$: The switch current starts falling at the time instant t_{open} and it commutates to the snubber circuit through the diode, D_{sn}. Then, the snubber capacitor C_{sn} starts to charge. The end of this stage has been reached once the switch current becomes zero.
- Stage 4: $t_{off} \leq t \leq t_{ch}$: After the IGBT turns-off completely, the capacitor will keep charging and thus, the total current I_tot continues to increase. The duration of this stage depends on the magnetic energy stored in the L_s. The complete charging of the snubber capacitor at t_{ch} ends this stage.
- Stage 5: $t_{ch} \leq t$: The last stage includes the discharge of the snubber capacitor through the snubber resistor R_{sn}, which results in an inverse power flow. The value of the resistor determines whether oscillations will occur or not.

C. CON3: SOLID-STATE DCCB WITH MOV AND RCD SNUBBER

The CON2 requires high snubber capacitance in order to suppress the overvoltage. On the other hand, the use of high snubber capacitance leads to a high total fault current. Therefore, the use of both MOV and RCD may tackle this challenge. Fig. 1(c) illustrates a solid-state DCCB connected with both

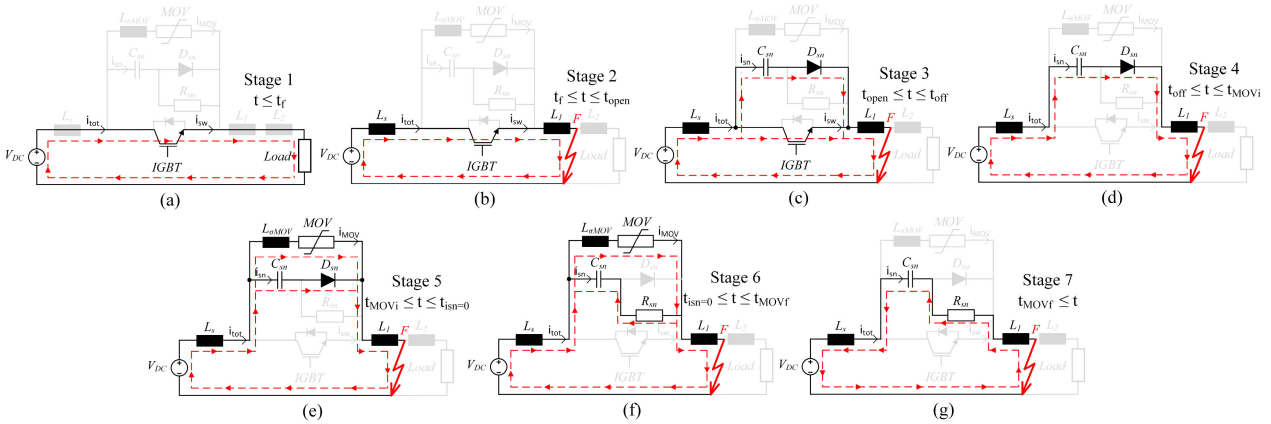

FIG. 4. Schematic diagrams of the discrete operating stages of the solid-state DCCB CON3.

RCD snubber circuit and MOV, while its operating stages during a fault clearance are shown in Fig. 4.

- Stage 1: $t \leq t_f$: Fig. 4(a) depicts the equivalent circuit before the fault occurrence.
- Stage 2: $t_f \leq t \leq t_{open}$: A pole-to-pole short-circuit fault occurs at the time instant t_f. The power semiconductor device receives the command to start the turn-off process at t_{open}. The time interval between t_f and t_{open} is considered as stage 2.
- Stage 3: $t_{open} \leq t \leq t_{off}$: Stage 3 includes the turn-off process of the power semiconductor device. It commences when the IGBT current starts to decrease at t_{open}, and it ends when this current reaches zero at t_{off}. Fig. 4(c) illustrates the equivalent circuit of this stage. In particular, the fault current commutates from the IGBT path to snubber path, through the snubber diode (D_{sn}) and capacitor (C_{sn}).
- Stage 4: $t_{off} \leq t \leq t_{MOVi}$: Stage 4 starts when the current of the IGBT is zero and lasts until the voltage across the switch reaches the MOV clamping voltage at t_{MOVi}.
- Stage 5: $t_{MOVi} \leq t \leq t_{isn=0}$: The next stage includes current commutation from snubber circuit to the MOV branch. It is completed at the time instant $t_{isn=0}$, which denotes the moment that the snubber current reaches approximately zero. The arising equivalent power circuit is illustrated in Fig. 4(e).
- Stage 6: $t_{isn=0} \leq t \leq t_{MOVf}$: The negative snubber current initiates the next phase. Stage 6 lasts until the voltage across the IGBT drops below the clamping voltage of the MOV at t_{MOVf}. Fig. 4(f) shows the equivalent circuit of stage 6.
- Stage 7: $t_{MOVf} \leq t$: The deactivation of the MOV initiates the final stage. Fig. 4(g) illustrates the equivalent circuit of stage 7.

IV. DESIGN PRINCIPLES OF CON1, CON2 AND CON3

The design of the three investigated overvoltage suppression configurations requires the following assumptions to be made for simplicity: (i) IGBTs have been considered for the switches in the breaker design due to their ruggedness over other high power semiconductor devices; (ii) on-state resistances of IGBTs are neglected; (iii) stray inductance of the IGBT module is low enough and thus, it is neglected; (iv) line inductances are neglected as well; (v) a simple passive gate drive unit is considered for all configurations.

A. CON1: DESIGN PRINCIPLES OF A SOLID-STATE DCCB WITH MOV

The main structure of the first investigated breaker configuration is illustrated in Fig. 1(a). The fault occurs at the instant time t_f, and after some delay (sensing, communication, coordination etc.) the breaker initiates the breaking process (at t_{open}). It must be mentioned that the communication and coordination delay among several breakers in a multi-terminal MVDC grid can be critical, and thus, it should be taken into careful consideration. In literature, several protection schemes applied in multi-terminal DC grids for fast fault detection have been proposed and investigated [36], [37]. Initially, the current limiting inductor L_s must be designed in order to limit the short-circuit current to values lower than a desired maximum current. This can be lower than either the maximum turn-off current rating of the main switch in the breaker $I_{sw_{max}}$ or a maximum allowable current $I_{sc_{max}}$ defined by the grid operators. Therefore, the following expression must be fulfilled:

$$L_s \geq \frac{V_{DC}}{\frac{I_{sc_{max}} - I_{thres}}{t_{open} - t_f}} \tag{1}$$

where, V_{DC} is the nominal DC grid voltage and I_{thres} is the threshold current that trips the breaker. Regarding the MOV design, several factors must be taken into consideration. Fig. 5 shows a characteristic curve of a varistor, highlighting the different operating regions along with the most significant factors. The normal operating region is defined by the voltage "V_{DC}," while the leakage current region is defined by the voltage "$V_{1\,mA}$" at 1 mA of varistor current. The transient operating region follows and lastly, the surge current area, which starts when the varistor voltage becomes higher than the clamping

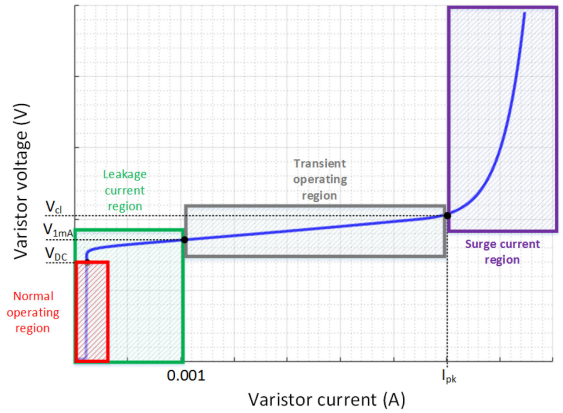

FIG. 5. **Characteristic curve of a Metal-Oxide Varistor.**

voltage, V_{cl} which is given at a specified current I_{pk}. Therefore, the choice of a varistor should consider all the above mentioned parameters. In particular, it must be ensured that the varistor operates in the normal operating region under no fault condition. Moreover, V_{cl} and I_{pk} must be chosen in such a way, that the overvoltage caused by the high di/dt during the IGBT turn-off and the presence of the current limiting inductor ($L_s \cdot di/dt$), will not damage the high-power semiconductor device employed in breaker. In other words, the varistor DC voltage, "V_{DC}," must be higher than the voltage of the DC grid, while V_{cl} needs to be greater than the DC grid voltage but much lower than the breakdown voltage of the semiconductor device, with I_{pk} to be close to the anticipated fault current which will commutate to the MOV branch. In addition, two more parameters of a varistor must be considered. The first one is the peak pulse current that must be within the anticipated peak short-circuit current. The second one is the single pulse energy at given current waveforms, which must higher than the actual energy dissipation in the MOV. Finally yet importantly, it should be mentioned that there are different types of varistors leading to different characteristic curves.

However, the connection path of the MOV to high-voltage semiconductor devices introduces significant stray inductance, $L_{\sigma MOV}$, which might cause voltage spikes [38]. This can be catastrophic for the device. Specifically, the $L_{\sigma MOV}$ must be kept as low as possible in order to secure a safe operation of the breaker. In other words, the IGBT will experience an overvoltage higher than the MOV clamping voltage equal to $L_{\sigma MOV} \cdot di/dt$. The rate of the current fall can reach few $kA/\mu s$ depending on the drive circuit and IGBT technology. A possible solution to that is to decrease the fall current rate during turn-off by means of the gate drive unit. However, this would lead to high energy dissipation in the switch, which might thermally destroy it.

B. CON2: DESIGN PRINCIPLES OF A SOLID-STATE DCCB WITH RCD SNUBBER

The current limiting inductor for CON2 is calculated using (1). Employing CON2, the peak voltage across the breaker and the voltage rise across the switch (dv_{sw}/dt) can be adjusted by means of choosing a proper snubber capacitance C_{sn}. On the other hand, the charging of the snubber capacitor forces the short-circuit current to reach higher values than the tripping value. This may cause severe damages to the electrical equipment connected to the grid (i.e. voltage source converters). In other words, high values of the capacitance lead to low switch overvoltages but also results in high fault currents. The snubber capacitance can be extracted by taking into account the energy stored in the current limiting inductor and applying the energy conservation law, as follows:

$$C_{sn} = \frac{L_s I_{sc_{max}}^2}{(V_{sn_{max}} - V_{DC})^2} \tag{2}$$

where, $V_{sn_{max}}$ is the peak voltage across the snubber capacitor, and it is assumed to be equal to the peak switch voltage. Regarding the snubber resistance R_{sn}, which provides a discharge path for the snubber capacitor, it can be designed in a way that there will be no oscillations caused by the resonance circuit formed by the snubber capacitor C_{sn} and current limiting inductor L_s as illustrated in Fig. 3(e). Therefore, it must be designed according to the following formula [39]:

$$R_{sn} \geq 2\sqrt{\frac{L_s}{C_{sn}}} \tag{3}$$

Additionally, the snubber resistance must be designed and minimized taking into consideration the desired reclosure time of the breaker. Last but not least, stray inductance in the snubber circuit path is also inevitable. It can cause small voltage oscillations across the high-power semiconductor device due to the fault current commutation and the presence of the snubber capacitor. However, this impact is less severe for the high-power semiconductor device compared to the stray inductance in the MOV path since a potential overvoltage spike due to the aforementioned voltage oscillations can be seen by the MOV and hence, the switch will be protected.

C. CON3: DESIGN PRINCIPLES OF A SOLID-STATE DCCB WITH MOV AND RCD SNUBBER

The design of the current limiting inductor is similar to the previous cases, i.e. by using (1)). The snubber capacitance must be designed in order to control the dv_{sw}/dt of the switch and thus, to protect the device from high thermal stress due to hard switching. This can be severe in case that the short-circuit current reaches high values and hence, the switch needs to experience simultaneously high current and high voltage for a short time interval. This might cause the failure of the IGBT due to excessive thermal stress. In other words, the energy dissipation in the device due to hard switching should remain within specified energy limits [39], [40]. Additionally, a significant high dv_{sw}/dt can also lead to mistrigger of the high-power semiconductor device employed in the breaker, which means that the device can turn-on accidentally and hence, the fault cannot be cleared. Besides that, the snubber capacitor can provide a smooth current commutation from the snubber

TABLE 1 Comparative Evaluation of CON1, CON2 and CON3

Configuration	Advantages	Disadvantages
CON1	Simple circuit Short fault clearance time	High voltage spike due to MOV stray inductance Possible ringings between stray inductances and capacitances Thermal stress of the switch No dv_{sw}/dt control
CON2	No thermal stress of the switch dv_{sw}/dt control No ringings	High total short-circuit current Long fault clearance time Need for high snubber capacitance Need for snubber resistor during the snubber capacitor discharge Need for diode with high surge current capability
CON3	No thermal stress of the switch dv_{sw}/dt control Low voltage spikes Need for low snubber capacitance	Long fault clearance time Need for snubber resistor during the snubber capacitor discharge Need for diode with high surge current capability Possible ringings between stray inductances and capacitances

TABLE 2 DC Power Grid Parameters

Parameter	Symbol	Value	unit
DC voltage	V_{DC}	1.8	kV
Load current	I_{load}	500	A
Line inductances	L_1, L_2	0.1	μH
Threshold current	I_{thres}	1	kA
Sensing and communication delay	t_{delay}	2	μs
Maximum allowable current	$I_{sc_{max}}$	1.2	kA
Voltage of MOV at $1mA$ DC current	V_{1mA}	1.95	kV
Clamping voltage of MOV	V_{cl}	2	kV
MOV current at V_{cl}	I_{pk}	200	A
MOV stray inductance	$L_{\sigma MOV}$	500	nH

circuit to the MOV branch, which will lead to low voltage spikes in the switch due to the MOV stray inductance. In other words, the current commutation from the snubber path to the MOV branch, can be controlled by means of snubber capacitor design. Therefore, the capacitance can be significantly lower compared to CON2 since the MOV will mostly dissipate the energy stored in the L_s. Equation (3) may also be considered for the snubber resistance R_{sn}.

The choice of an appropriate varistor depends on the DC voltage of the grid, as well as on the nominal current. The design of the MOV for this case is similar to the CON1. Table 1 summarizes the advantages and the drawbacks of each investigated configuration.

V. CASE STUDY AND SIMULATION RESULTS FOR HIGH-POWER DC SOLID-STATE BREAKERS RATED AT 1.8kV_{DC}

The high-power DCCBs shown in Fig. 1 have been modeled and simulated in a high-power MVDC grid with the parameters shown in Table 2. The IGBT (ABB 5SNA1300K450300) has the ratings of 4.5 kV and 1.3kA, while the considered parameters for the MOV modeling with respect to Fig. 5 are shown in Table 2. Lastly, a sensing and communication delay of 2μs has been considered [36].

TABLE 3 Comparative Results of CON1,CON2 and CON3 With Respect to the Passive Components Requirements

Configuration	L_s $[\mu H]$	C_{sn} $[\mu F]$	$P_{R_{sn}}$ $[kW]$	$\int I^2dt$ $[A^2s]$	E_{mov} $[J]$
CON1	34.2	-	-	-	282
CON2	34.2	100	1500	954	-
CON3	34.2	10	14	31.5	433

TABLE 4 Comparative Results of CON1, CON2 and CON3 With Respect to the Breaker Operation

Configuration	$I_{sc_{peak}}$ $[A]$	$V_{sw_{peak}}$ $[V]$	dv_{sw}/dt $[V/\mu s]$	t_{cl} $[ms]$
CON1	1209	4332	8000	0.280
CON2	3246	3667	32	1.031
CON3	1543	2265	150	0.475

A. COMPARATIVE STUDY OF CON1, CON2 AND CON3

For this case study, the evaluated parameters are the requirements for passive elements and the performance indices summarized in Section II. Table 3 presents the requirements for passive components for each configuration. The required current limiting inductor is the same for all configurations according to (1). Furthermore, it is clearly seen that the snubber capacitance in CON2 is much higher than in CON3. Similarly, CON2 requires snubber diode and resistance with higher power dissipation capabilities and power ratings compared to CON3. Lastly, the energy that the MOV must dissipate in CON1 is lower compared to CON3.

Table 4 shows the electrical performance of the breaker for the three configurations. The high snubber capacitance in CON2 leads to significantly high short-circuit current as described above. More specifically, the total short-circuit current reaches 3246 A, while in CON1 and CON3, it reaches 1209 A and 1543 A, respectively. On the other hand, the lack of snubber capacitance in CON1 results in high switch overvoltage, which might causes a voltage breakdown. In particular, the switch voltage reaches 4332 V, which is close to the IGBT

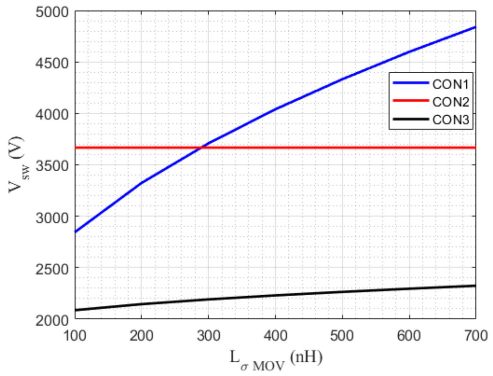

FIG. 6. Impact of the MOV stray inductance on the switch peak voltage for all configurations.

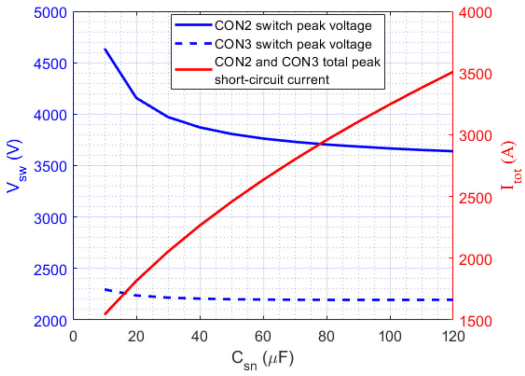

FIG. 7. Impact of the snubber capacitance on the switch peak voltage and total peak short-circuit current.

breakdown voltage, i.e. 4500 V and thus, it can be catastrophic for the device. On the contrary, CON2 limits the overvoltage to 3667 V and CON3 to 2265 V. In addition, the rate of voltage rise in CON1 is much higher compared to other two configurations. This can cause several issues which will be explained below. Furthermore, CON1 achieves the shortest clearance time, while CON2 needs the longest time among all. In particular, CON1, clears the fault within 0.28 ms, CON3 within 0.475 ms and CON2 requires more than one millisecond to interrupt the short-circuit current. For CON2 and CON3, the clearance times include the snubber capacitor discharge time interval.

B. IMPACT OF THE $L_{\sigma MOV}$ AND C_{sn} ON THE BREAKER OPERATION

The stray inductance of the MOV path is of great importance due to its impact on the switch overvoltage. Fig. 6 illustrates the switch peak voltage for the three configurations under various $L_{\sigma MOV}$. The absence of MOV (i.e. $L_{\sigma MOV} = 0$) in CON2 results in a constant peak switch voltage. CON3 keeps clearly the switch overvoltage significantly lower compared to CON1 and CON2 for the entire stray inductance range.

CON2 and CON3 require snubber capacitors connected in parallel to the switch. The control of the voltage rise when the IGBT turns-off is the main design target. The total fault current and the peak switch voltage are affected by the snubber capacitance. Therefore, an appropriate choice for C_{sn} must be made. Fig. 7 illustrates the impact of the snubber capacitance on the peak switch voltage and on the peak total short-circuit current. It should be mentioned that the latter parameter is the same for both configurations. The high capacitance required for CON2 in order to keep the peak voltage below a certain value can be achieved at the cost of high peak fault current. On the other hand, CON3 requires a much smaller snubber capacitance and hence, the peak current remains at a low value as well.

Last but not least, Fig. 8 shows the impact of both snubber capacitance and MOV stray inductance simultaneously on the peak switch voltage for CON3. An interesting observation

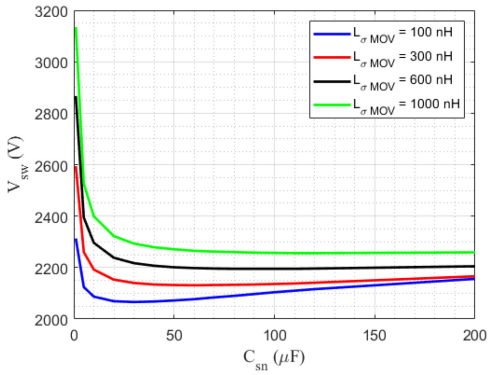

FIG. 8. Impact of the snubber capacitance on the switch peak voltage for CON3 under several MOV stray inductances.

is that for low $L_{\sigma MOV}$, there is a snubber capacitance which minimizes the switch overvoltage. Beyond this value, the overvoltage becomes higher as the capacitance increases. The reason to this is that the impact of a low $L_{\sigma MOV}$ is smaller compared to the snubber capacitance.

C. CHOICE OF OVERVOLTAGE SUPPRESSION CIRCUIT FROM AN APPLICATION PERSPECTIVE

An overall performance evaluation of CON1, CON2 and CON3 through simulations revealed the need for both MOV and snubber circuitry in order to successfully suppress overvoltages in a DC solid-state breaker rated at $1.8kV_{DC}$. On the one hand, CON3 requires a higher number of components compared to CON1 and CON2. However, CON3 minimizes the required snubber capacitance by at least one order of magnitude compared to CON2 and it provides immunity to the breaker against the stray inductances in the MOV path. Therefore, the possibility of the switch to break by overvoltage caused by stray inductances is significantly lower compared to CON1.

The presented study can be further extended to several application areas requiring different MV and power levels. The impact of the nominal grid voltage and current on the design of CON1, CON2 and CON3 can be assessed by examining (2)

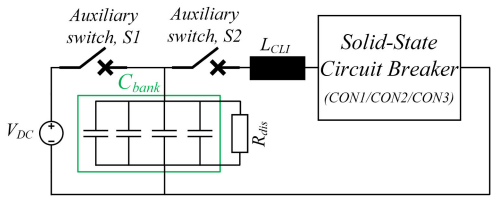

FIG. 9. Schematic diagram of the test circuit.

and Fig. 7. An increase of the direct grid voltage requires high snubber capacitance for an efficient overvoltage suppression. This, however, leads to high currents that are drawn from the VSC during a fault. Therefore, the designs of CON2 mostly, and CON3 depend on the level of the DC voltage. Similarly, a load increase can also affect the design of the snubber circuitry in CON2 and CON3. The magnetic energy stored in L_s is proportional to the load current square, and thus, the needed capacitance must increase accordingly. Moreover, depending on the application needs, and the fault-clearance requirements (in terms of time and maximum allowed grid current) CON1 might also be found to be a suitable overvoltage suppression concept. This, in particular, may be suitable if the current drawn from the VSC must be kept low. On the other hand, if the constraints of the maximum line current during a fault is softened, CON3 seems to enable several benefits, even though the components count is higher than CON1.

VI. EXPERIMENTAL RESULTS FOR MEDIUM-POWER DC SOLID-STATE BREAKERS RATED AT 1.5kV_{DC}

The schematic diagram of the down-scaled test setup that was used for the experimental procedure is shown in Fig. 9. The auxiliary switch, S_1 is used for charging the capacitor bank, C_{bank}, while the auxiliary switch S_2 blocks the charging of the snubber capacitor prior to the breaking operation. For the down-scaled prototype, the solid-state switch is a high-voltage and medium-power IGBT that is rated at 3.6 kV and 50 A (IXYS IXBX50N360HV, technology of Bipolar MOS Transistor), which is suitable for a medium-power breaker. Proper pulses are provided to S_2 and to the main switch in order to achieve a desired turn-off current. Fig. 10 shows a photo of the laboratory prototype of the solid-state CB along with all the required components. This laboratory prototype is configurable and thus, it is suitable for testing the three investigated solid-state breaker configurations CON1, CON2 and CON3.

Table 5 summarizes the design parameters for the test circuit. Three different voltage levels have been considered, i.e. 700 V, 1100 V and 1500 V highlighting the transition from low-voltage grids (700 V) to medium-voltage grids (1100 V and 1500 V). A fixed gate pulse of 20μs for the main switch has been taken into account, which includes all possible delays due to fault current sensing, communication, etc., until the fault identification in order to start the fault clearance procedure. A radial leaded varistor (Littelfuse

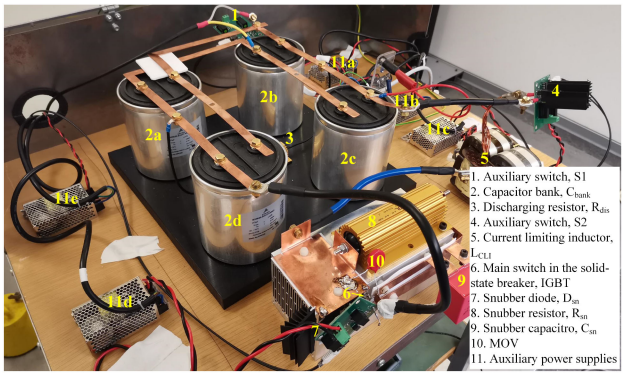

FIG. 10. Photograph of the experimental solid-state DC circuit breaker prototype.

TABLE 5 Parameters of the Experimental Setup

Parameter/Component	Value
Auxiliary switches, S_1, S_2	IXYS, IXBX50N360HV
Input voltage, V_{DC}	$700 - 1500V$
Capacitor bank, C_{bank}	$860\mu F$
Discharge resistor, R_{dis}	$47k\Omega$
Current limiting inductor, L_{CLI}	$660\mu H$
Main switch in solid-state CB, IGBT	IXYS, IXBX50N360HV
Snubber diode, D_{sn}	GeneSiC, GB25MPS17-247
Snubber resistor, R_{sn}	500Ω
Snubber capacitor, C_{sn}	$0.15 - 2\mu F$
Metal-Oxide Varistor, MOV	V1000LA160BP

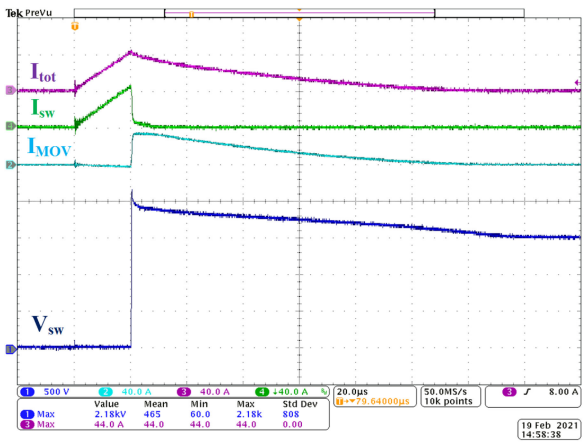

FIG. 11. Experimental results for the CON1 at 1500V_{DC} and 44 A turn-off current.

"V1000LA160BP") has been used for the lab prototype of the DC breaker.

A. EXPERIMENTAL RESULTS EMPLOYING CON1

The switching performance of the solid-state breaker employing CON1 with $V_{DC} = 1500$ V is shown in Fig. 11. It can be seen that the maximum voltage across the IGBT remains well below its breakdown voltage. It reaches 2.18 kV, while

TABLE 6 Experimental Results for CON1

V_{DC} [V]	$V_{sw_{peak}}$ [kV]	$I_{tot_{peak}}$ [A]	dv_{sw}/dt [$kV/\mu s$]	E_{sw} [mJ]	t_{cl} [μs]
700	2.04	21.2	7.5	16.8	16
1100	2.10	33.2	11	21	31
1500	2.18	44	13.5	41	130

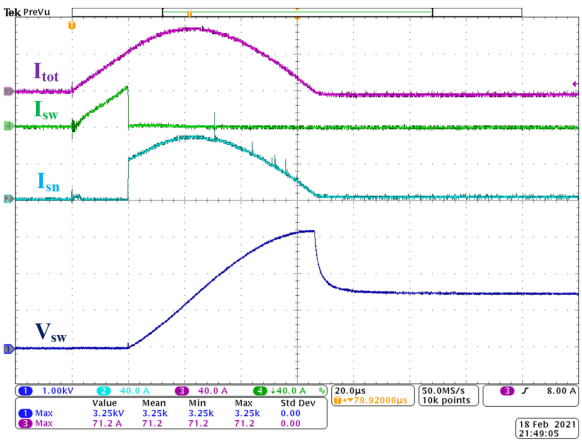

FIG. 12. Experimental results for the CON2 at $1500V_{DC}$ and $71.2\,A$ turn-off current with $C_{sn} = 1\mu F$.

the peak turn-off current is $44\,A$. On the other hand, the rate of voltage rise, dv_{sw}/dt is above $13\,\text{kV}/\mu s$, which cannot be acceptable at most applications, especially when high-power semiconductor modules are employed. In addition, it should be mentioned that the discrete high-voltage IGBT used in the lab prototype, inherently exhibits long current falling times. This leads to low di/dt values and hence, the anticipated overvoltage due to the stray inductance in the MOV path can remain relatively low. However, in a high-power IGBT module rated at the same voltage but at much higher current, the di/dt values can be 100 times higher. This would lead to significantly higher overvoltage values, as it will be analyzed in the next section. Based on the measurements, it is observed that the line current is interrupted within $130\mu s$, which is counted from the time instant that the gate turn-off pulse is provided to the main switch of the breaker. Last but not least, using CON1, the expected thermal stress of the IGBT must also be considered in the design process. Using experimental data, the switching energy has been found to be $41mJ$. In a high-power application, this energy will be significantly higher causing severe thermal damages in the IGBT. Table 6 summarizes the results for the three direct voltage cases employing CON1, i.e., $700V_{DC}$, $1100V_{DC}$ and $1500V_{DC}$.

B. EXPERIMENTAL RESULTS EMPLOYING CON2

The fault clearing process when employing CON2 with snubber capacitance of $1\mu F$ is illustrated in Fig. 12 for a direct grid voltage of $1500V_{DC}$. It is observed that the peak switch voltage reaches 3.25 kV at $71.2\,A$ turn-off current. In addition, the line

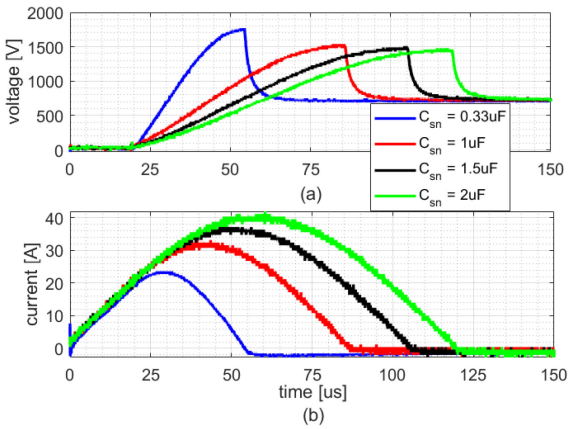

FIG. 13. Experimental results for CON2 at $700V_{DC}$ with several snubber capacitances: (a) switch voltage and (b) line current.

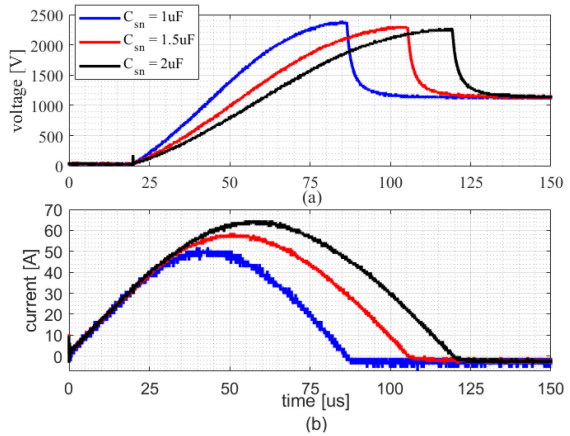

FIG. 14. Experimental results for CON2 at $1100V_{DC}$ with several snubber capacitances: (a) switch voltage and (b) line current.

current crosses zero point after $65\mu s$, and then, it becomes negative due to the snubber capacitor discharge. It should be mentioned that the clearance time can be considered longer if the negative residual current must be taken into account. However, if an ultra fast disconnector is connected in the DC line for galvanic isolation after the fault clearance, the first zero crossing of the current can be sufficient. Moreover, the switch voltage increases with a rate that is approximately 200 times slower compared to CON1 at the same DC voltage. Additionally, by using CON2, the thermal stress in the IGBT during the switching process becomes approximately zero due to the soft switching process.

Further results on turn-off process with various snubber capacitances, and at direct voltages of $V_{DC} = 700\,\text{V}$, $V_{DC} = 1100\,\text{V}$ and $V_{DC} = 1500\,\text{V}$ are illustrated in Figs. 13 , 14 and 15 . From these figures, it can be observed that the higher the snubber capacitance is chosen, the lower the switch overvoltage becomes, while the switch peak current increases. However, in case of $V_{DC} = 1500\,\text{V}$, the $V_{sw_{peak}}$ is slightly increased when the snubber capacitance increases from $1.5\mu F$

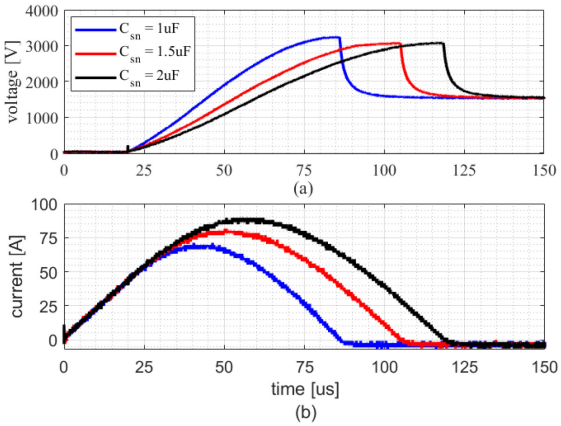

FIG. 15. Experimental results for CON2 at $1500V_{DC}$ with several snubber capacitances: (a) switch voltage and (b) line current.

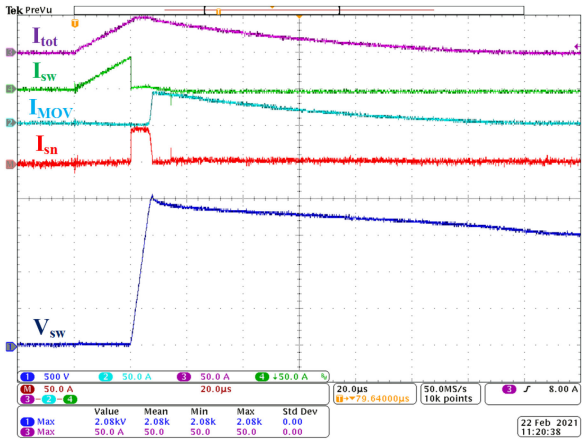

FIG. 16. Experimental results for the CON3 at $1500V_{DC}$ and $50\,A$ turn-off current with $C_{sn} = 0.15\mu F$.

TABLE 7 Experimental Results for CON2

V_{DC} $[V]$	C_{sn} $[\mu F]$	$V_{sw_{peak}}$ $[kV]$	$I_{tot_{peak}}$ $[A]$	dv_{sw}/dt $[V/\mu s]$	E_{sw} $[mJ]$	t_{cl} $[\mu s]$
700	0.33	1.77	23.6	70	~ 0	35
700	1	1.54	33.2	33	~ 0	65
700	1.5	1.51	38	24	~ 0	85
700	2	1.48	42	20	~ 0	100
1100	1	2.40	52	50	~ 0	65
1100	1.5	2.31	58.8	39	~ 0	85
1100	2	2.28	64.8	32	~ 0	100
1500	1	3.25	71.2	70	~ 0	65
1500	1.5	3.09	81.6	61	~ 0	85
1500	2	3.10	89.6	45	~ 0	100

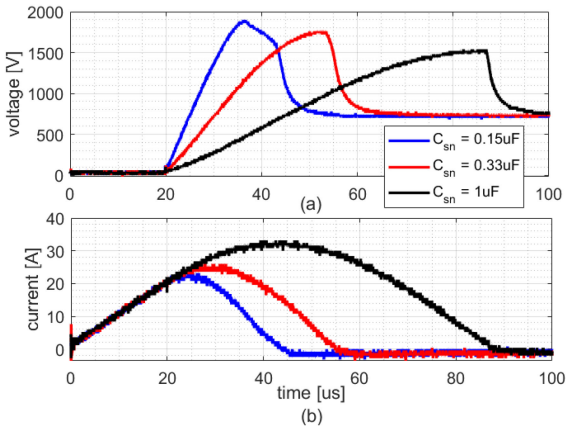

FIG. 17. Experimental results for CON3 at $700V_{DC}$ with several snubber capacitances: (a) switch voltage and (b) line current.

to $2\mu F$ due to the significant current increase. This is in accordance with Fig. 8. A summary of the experimental results is presented in Table 7. Similar to the simulations presented in Section V, the experimental results reveal that the choice of the capacitor value depends on (2). Therefore, based on the limitations arise by the MVDC grid design and operating limitations, i.e., DC voltage, current limiting inductor value, a proper snubber capacitance can be chosen in order to minimize either the peak short-circuit current ($I_{sc_{max}}$) or the peak snubber voltage.

C. EXPERIMENTAL RESULTS EMPLOYING CON3

The experimental results employing CON3 at $1500V_{DC}$ and a snubber capacitance of $C_{sn} = 0.15\mu F$ are illustrated in Fig. 16. As shown from the measurements, the switch overvoltage reaches 2.08 kV at $50\,A$ of turn-off current, while dv_{sw}/dt is $325\,\mathrm{V}/\mu s$. This rate of voltage rise is approximately 41 times lower compared to the case with CON1. By using CON3, the thermal stress in the IGBT is also minimized due to the presence of the snubber capacitor, which allows fault current commutation significantly faster. The fault current in the line crosses zero after $135\mu s$. Similarly to CON2, the clearance time can be considered longer if the negative residual current must be taken into account.

Figs. 17, 18 and 19 show further experimental results at three DC voltages, employing three snubber capacitances at each voltage level. Similarly to CON2, for higher values of the snubber capacitance, the anticipated fault line current is also higher. However, due to the presence of MOV, the peak switch voltage cannot be higher than the clamping voltage. On top of that and in contrast with the CON1, when high stray inductance in the MOV branch occurs, the low di/dt in the current commutation between the snubber capacitor and the MOV would not cause severe overvoltages. Table 8 summarizes the numerical results based on the experiments.

D. DISCUSSION ON THE EXPERIMENTAL RESULTS

This section has presented an experimental performance evaluation of three overvoltage suppression configurations for solid-state DC circuit breakers. The first configuration, CON1 has shown a superior performance in terms of short line current interruption times and low peak fault current in the DC

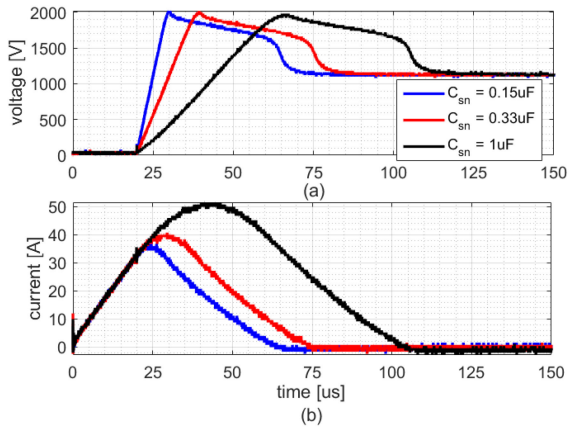

FIG. 18. Experimental results for CON3 at $1100V_{DC}$ with several snubber capacitances: (a) switch voltage and (b) line current.

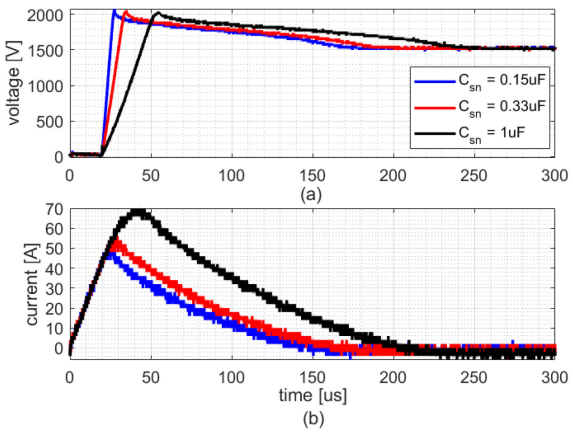

FIG. 19. Experimental results for CON3 at $1500V_{DC}$ with several snubber capacitances: (a) switch voltage and (b) line current.

TABLE 8 Experimental Results for CON3

V_{DC} $[V]$	C_{sn} $[\mu F]$	$V_{sw_{peak}}$ $[kV]$	$I_{tot_{peak}}$ $[A]$	dv_{sw}/dt $[V/\mu s]$	E_{sw} $[mJ]$	t_{cl} $[\mu s]$
700	0.15	1.90	23.2	145	~ 0	23
700	0.33	1.76	26	75	~ 0	34
700	1	1.54	33.2	32	~ 0	68
1100	0.15	2.02	36.8	235	~ 0	40
1100	0.33	2.02	40.8	120	~ 0	52
1100	1	1.98	51.6	51	~ 0	83
1500	0.15	2.08	50	325	~ 0	135
1500	0.33	2.06	56	168	~ 0	150
1500	1	2.04	70	70	~ 0	183

line. However, the thermal stress of the high-voltage semiconductor device is high, while the blocking voltage of the switch increases rapidly. The last disadvantage is magnified when high-power semiconductor modules are used due to the high-current capability and their high inherent stray capacitances. Last but not least, the current falling time in a high-power module can be much shorter than in a discrete device, and hence, this would lead to more severe module overvoltages due to the presence of stray inductance in the MOV loop.

The second configuration, CON2, has shown to be a possible candidate to suppress the switch overvoltage in a solid-state DC breaker topology used in low-voltage DC grids. On the other hand, when the direct voltage increases, the required snubber capacitance in the CON2 is also increasing, resulting in significant high total current. Finally, CON3 can be considered for medium-power applications, minimizing the required snubber capacitance compared to CON2, and reducing the thermal stress of the IGBT, and the rate of voltage rise during the turn-off process compared to CON1.

VII. CONCLUSION

This paper presents a comparative study of three overvoltage suppression configurations for DC solid-state circuit breakers rated up to $1.8kV_{DC}$. The performance evaluation of these three configurations has been conducted experimentally and by simulations. From experiments, it is revealed that CON1 can be considered for a solid-state DC breaker when medium-power high-voltage semiconductor discrete devices are used, due to their inherent long current falling time. Thus, low di/dt and low thermal stress are anticipated for the devices. In addition, the experimental results showed that the required snubber capacitance for CON2 must be high enough in order to keep the switch overvoltage within safe limits, at a cost of a high line current. On the other hand, CON3 performs better over the other two configurations in terms of keeping the switch voltage low even when a low snubber capacitance was employed, and hence, the line current increases slightly compared to CON1.

In a $500A$, $1.8kV_{DC}$ application, the simulations reveal that CON1 experienced the highest switch overvoltage, while CON3 achieved the lowest overvoltage. Furthermore, the peak short-circuit current reached a value of $4kA$ in CON2, while in CON1 and CON3 this current was limited to approximately $1.2kA$ and $1.5kA$, respectively. Undesired oscillations and high rate of rise of the switch voltage have been observed in CON1, while this configuration cleared the short-circuit current in a shorter time compared to CON2 and CON3. Lastly, CON1 has been shown to be more sensitive to the MOV stray inductance, experiencing an overvoltage of 2500 V that is higher compared to CON3 as the MOV stray inductance becomes $700nH$.

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ANDREAS GIANNAKIS (Student Member, IEEE) was born in Edessa, Greece, in 1991. He received the Diploma in electrical and computer engineering from the University of Patras, Patra, Greece, in 2014, and the MSc. degree in electric power engineering from the Democritus University of Thrace, Xanthi, Greece, in 2016. He is currently working towards the Ph.D degree with the Department of Electric Power Engineering, Norwegian University of Science and Technology, Trondheim, Norway. His main research interests include circuit breaker concepts for DC power grids, focusing mostly on solid-state, and hybrid topologies.

DIMOSTHENIS PEFTITSIS (Senior Member, IEEE) was born in Kavala, Greece. He received the Diploma (Hons.) in electrical and computer engineering from the Democritus University of Thrace, Xanthi, Greece, in 2008, and the Ph.D. degree from the KTH Royal Institute of Technology Stockholm, Sweden, in 2013. He is currently an Associate Professor of power electronics with the Department of Electrical Power Engineering, Norwegian University of Science and Technology (NTNU), Trondheim, Norway where he has been a Faculty Member since May 2016. From 2013 to 2014, he was a Postdoctoral Researcher involved in the research on SiC converters with the Department of Electrical Energy Conversion, KTH Royal Institute of Technology. He also worked as a Postdoctoral Fellow with the Lab for High Power Electronics Systems, ETH Zurich, where he was involved in dc-breakers for multiterminal HVDC systems from 2014 to 2016. He has authored or coauthored more than 60 journal and conference papers. He is the Co-Author of one book chapter and the presenter of five conference tutorials. In his final year of studies, he spent six months in ABB Corporate Research, Vsters, Sweden, writing his thesis. His research interests include the area of power converters design using WBG devices (e.g. SiC, GaN) including adaptive drive circuits, dc-breaker design for MV and HVDC systems, as well as reliability assessment and lifetime modelling of high-power semiconductor devices, including reliability of SiC power switches. Dr. Dimosthenis is a Member of Outstanding Academic Fellows Programme with NTNU, a member of EPE International Scientific Committee and currently serves as the Chairman on the Norway IEEE Joint Power Electronics Society/Industry Applications Society/Industrial Electronics Society Chapter.