A Flexible Test Setup for Long-Term Dynamic Characterization of SiC MOSFETs under Soft- and Hard-Switching Conditions

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Abstract

Due to the superior material characteristics of Silicon Carbide (SiC), the use of SiC MOSFETs enables higher system power density or efficiency depending on the design perspective. To identify the improvement potential in the operation of a device, precise characterization is crucial. This paper presents a flexible and easily reconfigurable test setup to characterize the dynamic behavior of SiC MOSFETs under both hard- and soft-switching conditions at blocking voltages of up to 900 V and currents up to 300 A. It features a balancing circuit that enables long term test operation in both switching modes and as a future power cycling test setup.

1 Introduction

Silicon Carbide (SiC) is attractive for use in future high power electronic converters (PECs) due to its higher temperature resiliency, faster charge carrier dynamics and higher specific breakdown voltage [1], [2]. Device characteristics differ substantially from Silicon (Si) counterparts [1], [3], [4]. To facilitate the design of power electronic converters employing SiC devices, simulation models need to reflect both static and dynamic device behavior accurately.

Static characterization is carried out using power device characterizers (e.g. the B1505A by Keysight [5]). Dynamic characterization, however, usually demands multiple steps. In a first step, the device capacitances are measured with a power device characterizer (like the above-mentioned). The remaining parasitic elements and other parameters impacting the dynamic device behavior are determined by fitting switching behavior in simulations to experimental measurements. Conventionally, Double Pulse Test (DPT) experiments at various current and voltage levels as well as various device temperatures are used yielding hard-switching waveforms [6].

By applying further tests, dynamic device characteristics are enhanced. Soft switching (SSW) tests give extended characteristic information. In addition, device behavior is subject to changes due to aging introduced by time and wear. In that regard, results of long term tests provide even more detail to the device behavior representation. Steady state observations and conditions close to a real application are imposed. This enables the extraction of further meaningful information on the potential application performance of the Devices Under Test (DUTs). On top of that, long term tests are also used for thermal device characterization in a calorimetric setup [7].

Some currently available test circuit designs allow soft switching tests. However, they either lack steady state and long term test capability or fail at retaining a compact and simple circuit that does not alter the characteristics of the DUTs. Single soft-switching tests can be enabled by adding a switchable resonant circuit branch to a DPT setup [8]. Nevertheless, the investigation of continuous operation is not possible with such a setup. Another approach is to use a power-in-the-loop configuration of two soft-switching resonant LLC converters [9]. While this presents an efficient and low-loss alternative, it results in a large test setup with a multitude of components. This complicates the isolated investigation of single devices or modules. SiC MOSFETs feature strongly accelerated conduction channel dynamics. This is illustrated by the fact that their switching behavior is dominated by their parasitic capacitances, even

though they are significantly smaller compared to Si counterparts. As a result of that, soft-switching can occur without any additional external capacitances for a range of operating conditions if fast gate drive units are used [3], [4]. Using a half-bridge converter with additional snubber capacitors parallel to the DUTs provides soft-switching characteristics with fewer devices [10]. However, soft-switching is enforced, covering the natural behavior of DUT and leading to an incomplete representation of the device characteristics. Thereby, the amount of meaningful information on the DUT is reduced to a minimum. Also, resistive losses occur in the load and need to be extracted from the circuit.

This paper presents a low-loss test setup to perform accurate dynamic characterization tests on SiC MOSFETs under hard- and soft-switching conditions for both short and long term investigation. The test-setup consists of a half-bridge converter with an inductive load and a balancing circuit. The circuit does not contain any additional snubber elements. DPTs as well as continuous soft- and hard-switching tests can be performed with this configuration. Using an inductive load, losses in the circuit are reduced to the device losses as well as parasitic losses in the inductor and in a dedicated balancing circuit. This balancing circuit transfers charge between the two DC-capacitors in the half-bridge configuration. This facilitates the operation of the DUT and inductor with a positive average current as in conventional synchronous converters.

The paper is structured as follows. Section 2 introduces the test setup design. In section 3, sample measurements are presented to illustrate the functionality of the test setup. Finally, the findings are summarized in section 4 and an outlook on future improvements is given.

2 Test Setup

Table 1 contains the major design parameters for the test setup, Fig. 1 shows a schematic diagram and Fig. 2 a photo of the test setup.

2.1 General Information

Measurements are taken with the Tektronix DPO 5405B Oscilloscope and high-bandwidth current- and voltage probes (CWTMini HF6 rogowski coil,

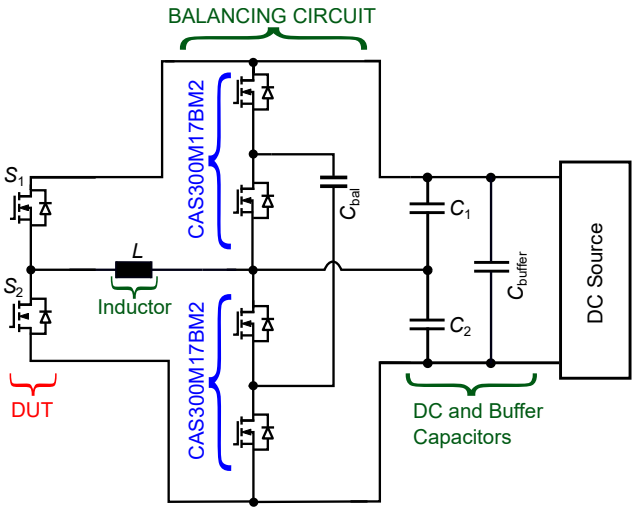


Fig. 1: Schematic Diagram of the Test Setup Circuit

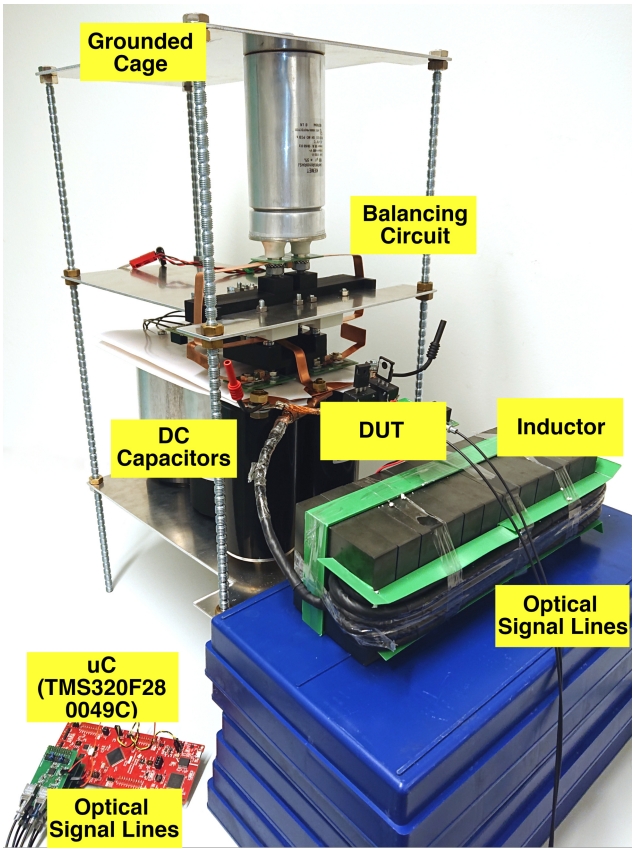


Fig. 2: Photo of the Test Setup

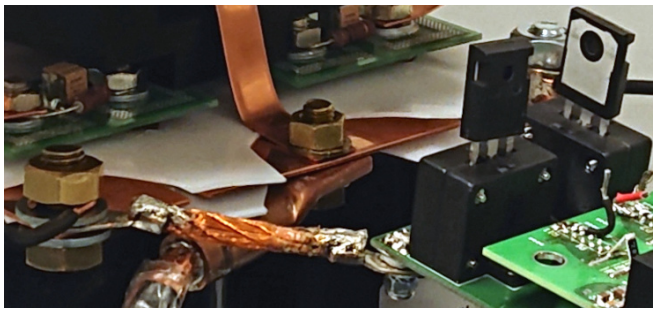


Fig. 3: DUT Coupling in Detail

Tab. 1: Test Setup Design Choices

Test Entity	Maximum Value
Current (DUT)	300 A
Voltage (DUT)	1.5 kV (2 kV)
Switching Frequency (DUT during SSW Test)	150 kHz
Switching Frequency (Balancing Circuit)	25 kHz

Tektronix TPP1000 and TPP0850 passive voltage probes). The circuit is energized by a high voltage power supply with maximum ratings of 1.5 kV and 100 A [11]. Changing the power supply will allow the circuit to operate at a maximum voltage of 2 kV.

2.2 Capacitive Energy Storage

The test setup comprises the passive part of a half-bridge converter, i.e. $C_1 = C_2 = 500\,\mu F$ 1.1 kV film capacitors in series and an inductor attached to the midpoint. To stabilize the DC bus voltage, two additional $C_{buffer} = 215\,\mu F$ 2 kV film capacitors are used in parallel with the series connection of C_1 and C_2.

A balancing circuit ensures the equal distribution of the DC voltage among C_1 and C_2 during long term tests. It consists of $C_{bal} = 100\,\mu F$ 1.1 kV film capacitor and two series connected 1.7 kV SiC MOSFET half-bridge modules of type CAS300M17BM2 by Wolfspeed. They are synchronously operated with a duty cycle of 50 %, connecting the balancing capacitor to the lower DC capacitor during the first half and the upper DC capacitor during the second half of a switching period [12].

Choosing the balancing circuit switching frequency correctly will minimize the transient influence on the test circuit voltages [12]. Also, the losses that occurring due to the resistive charge transfer between the DC capacitors and the balancing capacitor respectively can be reduced. When the balancing circuit switches, transient oscillations may occur because fast SiC modules are used in the design. To minimize their influence on the measurements, the balancing circuit is deactivated, the measurement is taken and only afterwards, the balancing circuit is activated again. Due to the large size of the capacitors C_1, C_2 and C_{buffer}, this does not have an effect on the current and voltage set points.

To compensate for their parasitic inductance and resistance, C_1, C_2 and C_{bal} are equipped with a parallel 750 nF 900 V ceramic capacitor each. Copper bus bars of 250 µm thickness and a minimal width of 38 mm act as main conductors. The circuit terminals are as close to the capacitor array as possible.

2.3 Inductive Energy Storage

For the inductor, the ferrite material 3C94 is chosen because it exhibits low losses for a maximum switching frequency of 150 kHz [13]. Several U- and I-shaped ferrite blocks in parallel form the inductor core. The number of parallel U-I-pairs determines the inductor scale, i.e. inductance and cross-sectional area. By providing a sufficiently large cross-sectional area, saturation is avoided for the maximum current of 300 A. 3D-printed PLA spacers are used for setting the air gap of the inductor, fine-tuning both the inductance and the maximum magnetic flux density in the core. Stranded wire with a total of 6390 strands with a diameter of 0.071 mm each is chosen as conductor [14]. Apart from reducing the impact of the skin effect, this also guarantees an adequate total cross sectional conduction area and thus current carrying capacity, so that ohmic losses in the copper are minimal.

2.4 Flexible DUT Coupling

An important factor in the coupling of DUTs is flexibility. Therefore, the test circuit presented in this paper features mounting points as an interface to test fixtures that are individually built for the DUTs. As an example, a test fixture that fits discrete devices in a TO-247-3 housing and how this is attached to the main circuit can be seen in Fig. 3. It features a test socket for the devices and thereby enables fast exchange of devices without any soldering. In a future version, the test fixture will incorporate stabilizing capacitors close to the DUTs for even lower power loop inductance.

In addition to the increased flexibility and reusability of the basic test circuit, the usage of individual test fixtures facilitates circuit extensions by means to employ continuous testing. Furthermore, individual test fixtures allow for tailored probing solutions that

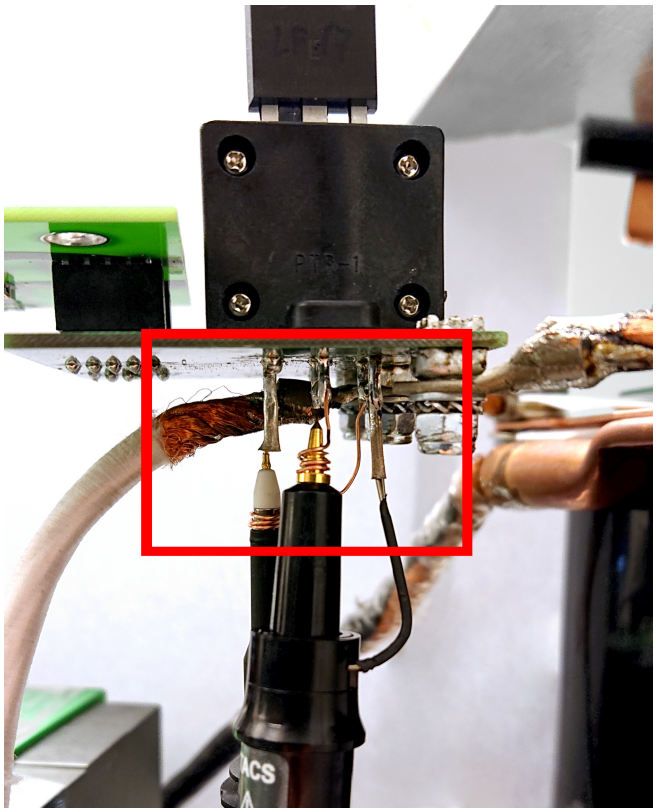


Fig. 4: Custom Probing Points on a TO-247-3 Test Fixture

minimize the measurement path inductance and thus provide more accurate and reliable results. An example for a tailored probing solution is shown in Fig. 4.

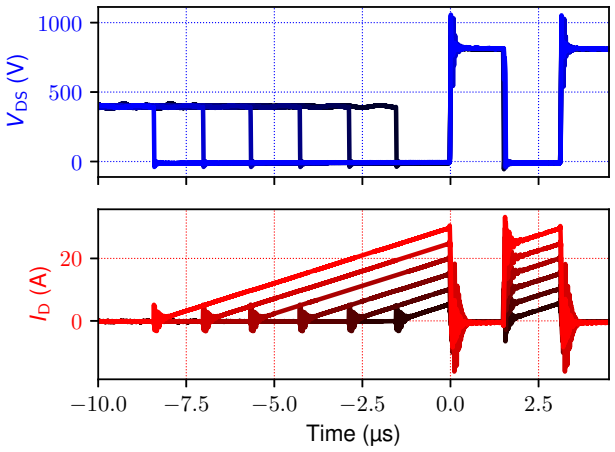
2.5 Gate Drive

A passive gate driver is used to drive both the DUTs and the balancing circuit switches. It does not feature any cross talk suppression circuit like miller clamping or similar [15].

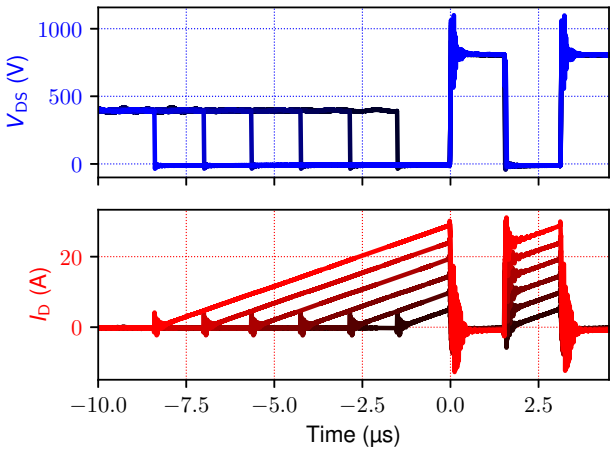
The gate signals for both the balancing circuit and the DUTs come from a single source, a Texas Instruments TMS320F280049C microcontroller launchpad. Stackable and reconfigurable adapters each transform a pair of electrical into optical signals. One header section of the four on the launchpad can serve up to four independent gate signal pair sources.

3 Experimental Results

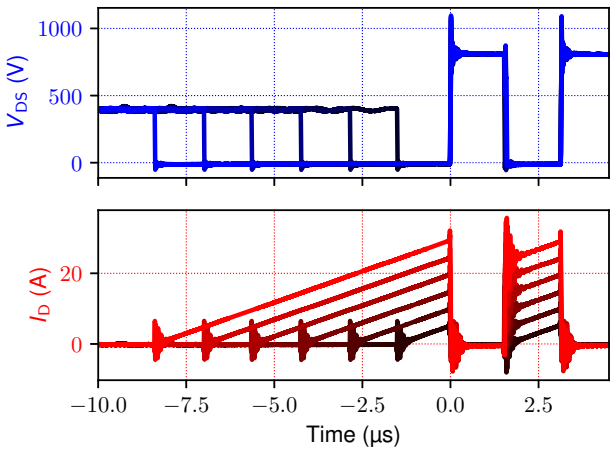
Five device types have been tested with the presented test circuit. One set of ten DUTs samples each of three manufacturers, namely Wolfspeed



(a) Wolfspeed C3M0075120D

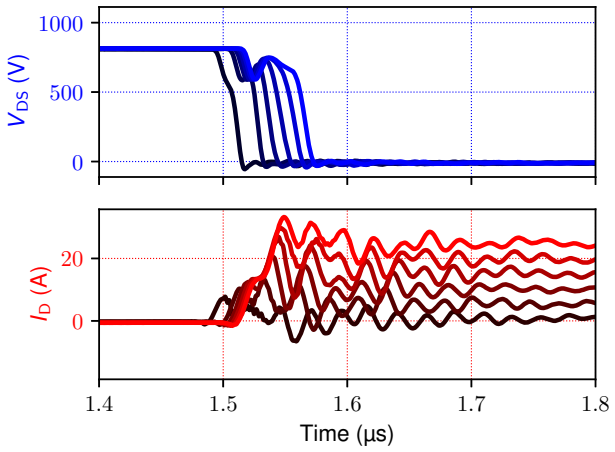


(b) ROhm SCT3080

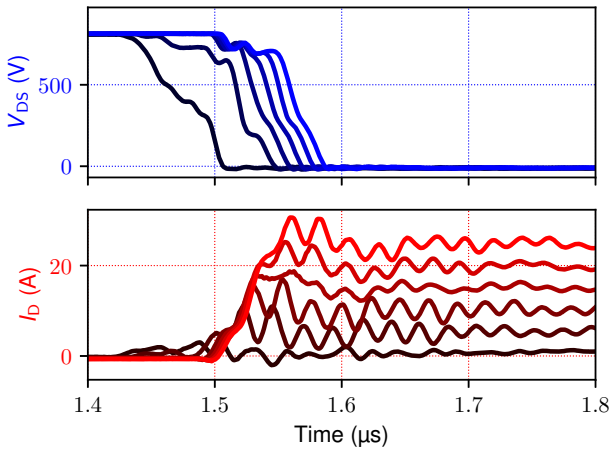


(c) Littlefuse SIC1MO120F0120

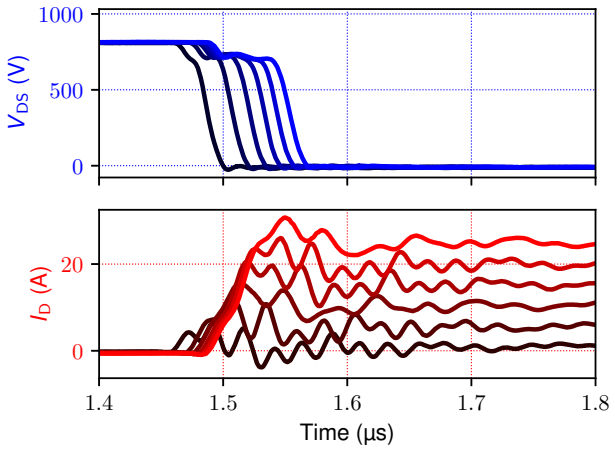
Fig. 5: Double Pulse Test Measurements at an external gate resistance of 5.4 Ω



(a) R_G =5.4 Ω

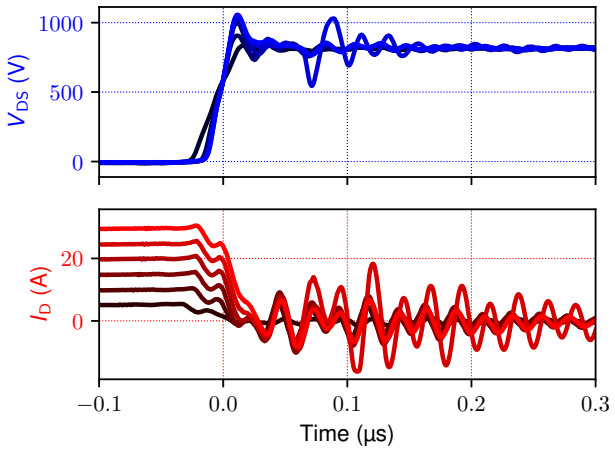


(b) R_G =10 Ω

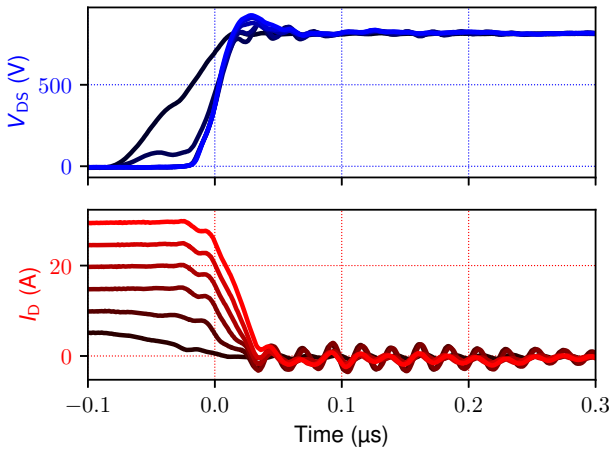


(c) R_G =16.7 Ω

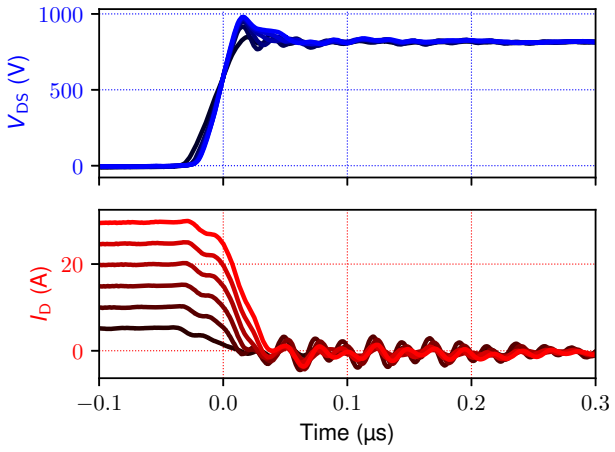
Fig. 6: Turn-on Waveforms of the C3M0075120D MOSFET employing various gate resistor values



(a) R_G =5.4 Ω



(b) R_G =10 Ω



(c) R_G =16.7 Ω

Fig. 7: Turn-off Waveforms of the C3M0075120D MOSFET employing various gate resistor values

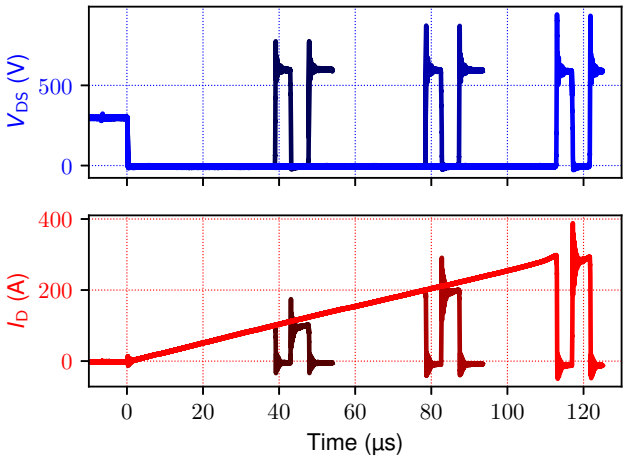


Fig. 8: Wolfspeed CAS300M17BM2 Double Pulse Test at a Test Voltage of 600 V, Test Current of up to 300 A, and using a 10 Ω Gate Resistor

(C3M0075120D), Rohm (SCT3080), and Littlefuse (SIC1MO120F0120), which are all delivered in a TO-247-3 packages, as well as one TO-247-3 STMicro SCT30N120 MOSFET and one half-bridge module CAS300M17BM2 by Wolfspeed have been subjected to the following tests:

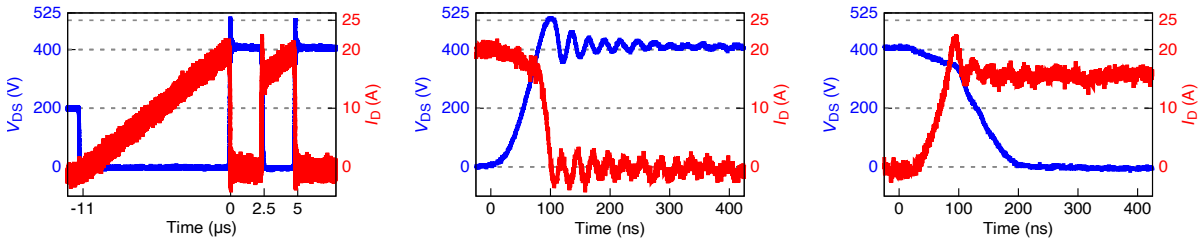
- Ten sample devices of type C3M0075120D by Wolfspeed at a voltage of 800 V, current levels of 5 A, 10 A, 15 A, 20 A, 25 A, and 30 A using gate resistor values of 5.4 Ω, 10 Ω, and 16.7 Ω.
- Ten sample devices of type SCT3080 by ROhm and SIC1MO120F0120 by Littlefuse at a voltage of 800 V, current levels of 5 A, 10 A, 15 A, 20 A, 25 A, and 30 A using a gate resistor value of 5.4 Ω.
- A single sample device of type CAS300M17BM2 by Wolfspeed
  - at a voltage of 600 V, current levels of 50 A, 100 A, 150 A, 200 A, and 250 A using a gate resistor value of 5.4 Ω.
  - at a voltage of 600 V, current levels of 50 A, 100 A, 150 A, 200 A, 250 A, and 300 A using a gate resistor value of 10 Ω.
  - at a voltage of 800 V, current levels of 50 A and 100 A using a gate resistor value of 10 Ω.
  - at a voltage of 600 V, current levels of 50 A, 100 A, 150 A, 200 A, 250 A, and 300 A using a gate resistor value of 16.7 Ω.
- A single sample device of type SCT30N120 by STMicro at voltage levls of 400 V, 600 V, and 800 V, a current level of 20 A using a gate resistor value of 50 Ω.

Various results of hard switching DPTs at a test voltage of 800 V, current levels of 5 A, 10 A, 15 A, 20 A, 25 A and 30 A and using 5.4 Ω as gate resistor value are shown in Fig. 5. Each figure shows six mean waveforms of ten individual devices and thus represents sixty experiment results. The devices behave differently, which can be easily seen inspecting the waveforms in Fig. 5.

Figures 6 and 7 show detail views of the turn-on and turn-off instances of the C3M0075120D MOSFET at the three gate resistor values 5.4 Ω, 10 Ω and 16.7 Ω current levels of 5 A, 10 A, 15 A, 20 A, 25 A and 30 A and a test voltage of 800 V. Again, each figure shows six mean waveforms of ten individual devices and thus represents sixty experiment results. The device behaviour depends strongly on the gate resistor value and the current levels as can be clearly identified by looking at the waveforms. The low current waveforms partly differ considerably from the rest of the waveforms. This is due to two factors. First, the commutation process is substantially slower for a low test current. This amplifies the nonlinear characteristics of the DUTs and is not representative for the rated operation of the device. Second, the waveforms are subject to an offset in time after applying a post processing software trigger which is dependent on the waveform slope.

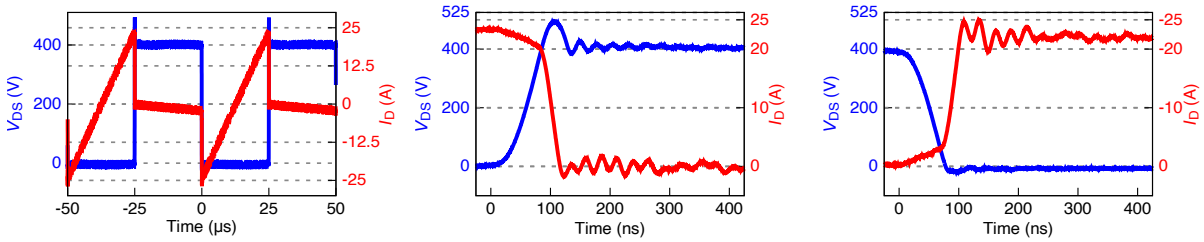
In Fig. 8, a choice of DPT results of the Wolfspeed CAS300M17BM2 half bridge module are shown. This choice includes experiments at a voltage of 600 V and currents of 100 A, 200 A, and 300 A using a 10 Ω gate resistor. This illustrates the large range of test currents that the presented test circuit supports.

Figures 9 and 10 show sample measurements of a DPT and a soft-switching test respectively, operating two SCT30N120 SiC MOSFETs in a half-bridge configuration at a test voltage of 400 V and a test current of 20 A. The soft-switching measurement is subject to an averaging measurement (25 cycles) and thus appears less noisy than the single-shot DPT measurement. The



(a) Overview (b) Turn-Off (c) Turn-On

Fig. 9: DPT Measurements of STMicro SCT30N120 MOSFET



(a) Overview (b) Turn-Off (c) Turn-On

Fig. 10: Soft-Switching Test Measurements of STMicro SCT30N120 MOSFET

DPT measurements presented earlier feature the mean of ten devices. Therefore, also those seem to be less noisy than the DPT result of the single SCT30N120 MOSFET. The presented results meet the experiment expectations. The hard- and soft-switching turn-off processes occur under almost identical conditions. This is confirmed by the measurement. During the DPT, a hard turn-on process with overlap of voltage and current is observed whereas in the soft-switching test, the reversed inductor current leads to a resonant current commutation and soft turn-on with a significantly reduced overlap of voltage and current.

Gate voltage spikes introduced by cross talk reach up to –10 V and can destroy the gate oxide layer of MOSFETs. Hence, continuous soft switching tests have been limited to a test voltage of 400 V and executed with a gate resistance of 50 Ω. For soft switching tests utilizing the entire voltage region of the test circuit, an active gate drive circuit is to be developed that features either miller clamping [15] or current source driving.

4 Conclusion

This paper presents a flexible and reconfigurable test setup for the dynamic behavior characterization of SiC MOSFETs. It facilitates the investigation under both hard- and soft-switching conditions in both short- and long-term tests. Extensive tests of a multitude of devices and different device types have been performed to proof the flexibility of the circuit. Measurement results are shown to demonstrate the successful application of soft- and hard-switching tests to five different MOSFET models by four different manufacturers. The test setup is versatile, easily modifiable and upgradable because of its modularity.

A potential for improvement is the development of an even lower inductive power loop featuring more support capacitors closer to the DUT. Also, a custom high bandwidth current sensor can be easily integrated. Finally, using a more sophisticated gate driver will enable soft-switching tests in the entire rated operation region.

5 Acknowledgement

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