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Isolated High-Frequency Link PFC Rectifier with High Step-Down Factor and Reduced Energy Circulation

Andrei Blinov, *Senior Member, IEEE*, Dmitri Vinnikov, *Senior Member, IEEE*, Enrique Romero-Cadaval , *Senior Member, IEEE*, João Martins, *Senior Member, IEEE*, Dimosthenis Peftitsis, *Senior Member, IEEE*

***Abstract*— This paper presents an isolated single-stage AC-DC high-frequency link full-bridge cycloconverter (HFLC) with high conversion ratio. Despite certain advantages, such topologies generally suffer from transformer leakage inductance problems and lack of effective modulation methods, particularly in the AC-DC operation mode. In this study, for the input current regulation with the power factor correction (PFC) of the HFLC, a novel phase shift modulation (PSM) method is used. It allows soft-switched turn-off of the DC-side transistors and zero current switching of the AC-side matrix switches without additional circuits or topology modifications. The introduced time-varying regulation of the peak current can be easily implemented; as a result, merely minor energy circulation occurs. Moreover, two of the AC-side transistors operate with fundamental frequency. Design constraints of the concept are analyzed and discussed. For verification, a 1.2 kW 230 VAC to 48 VDC experimental prototype is used.**

***Index Terms*— PFC rectifier, AC-DC power converters Energy storage, Power supplies, Soft switching, Zero current switching, Zero voltage switching.**

I. Introduction

HIGH dependency of the modern society on electronic equipment together with increasing penetration of renewable energy, battery storage and DC grid technologies have increased the role of power electronic interfaces for providing sustainable electric energy supply. For example, in the telecom applications, converters are used for the interface between the AC and 48 V DC bus voltages [1][2]. This voltage level is also proposed for battery storage and lighting systems in the future DC homes [3]. Furthermore, the growing use of light electric vehicles powered by batteries implies the necessity of chargers supplied from the AC grid. In most of those cases, AC mains should be generally interfaced with a relatively low DC voltage 12…48 V. Power electronic converters for such applications typically employ a transformer to provide the required voltage matching and galvanic isolation. Modern designs aim to take advantage of high-frequency transformers to reduce the volume and weight of the interface system. Typically, a two-step energy conversion is utilized, where the non-isolated AC-DC stage is connected to the isolated DC-DC converter through an intermediate DC-link [4].

Another approach is to use single-stage conversion with high-frequency link converter topologies (HFLCs), also referred to as cycloconverters or isolated matrix converters [5]. These systems have no intermediate DC-link and thus high-voltage (typically around 400…500 V for 230 VAC grid voltage) electrolytic capacitors can be completely avoided. One of the drawbacks of the HFLC lies in the voltage spikes across the AC-AC (matrix) stage transistors due to current mismatch between the transformer leakage and the grid filter inductances. A range of advanced modulation strategies have been proposed [6][7][8][9] to mitigate this problem and provide soft switching transients for semiconductors. As a result, the state-of-the-art HFLCs can

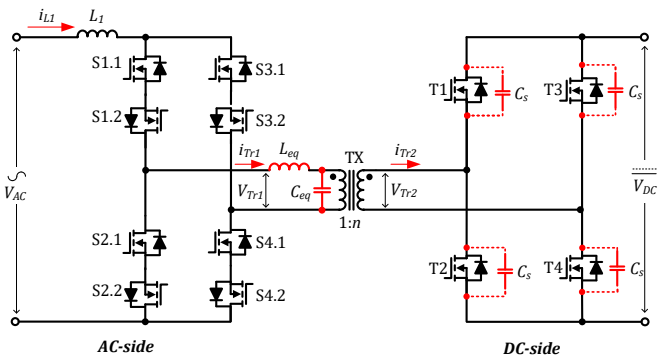

Fig. 1. Full-bridge HFLC topology.

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A. Blinov and D. Vinnikov are with the Department of Electrical Power Engineering and Mechatronics, Tallinn University of Technology, Tallinn, 19086, Estonia (e-mail: andrei.blinov@taltech.ee; dmitri.vinnikov@taltech.ee).

Enrique Romero-Cadaval is with the Extremadura University, 06006 Badajoz, Spain (e-mail: eromero@unex.es).

J. Martins is with the Department of Electrical Engineering, Faculty of Sciences and Technology, NOVA University of Lisbon, 2829-516 Caparica, Portugal (e-mail: jfmartins@fct.unl.pt).

D. Peftitsis is with the Norwegian University of Science and Technology 7012, Trondheim, Norway (e-mail: dimosthenis.peftitsis@ntnu.no).

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demonstrate characteristics comparable to those of two-stage solutions and are generally proposed for uninterruptable power supply, photovoltaic and battery applications [5]. Another potential advantage of the HFLC lies in the capability of bidirectional operation, which is an essential property when energy exchange between the AC and the DC sources is assumed. Unfortunately, existing research mainly focuses on the DC-AC (inverter) operation mode.

Since the nature of the DC-AC and AC-DC operation of HFLCs is not the same, other modulation methods have to be developed. In fact, recent studies have addressed this issue from different angles. In [8], the hard switching operation during the AC-DC rectifier mode is assumed. The converter in [10] uses an auxiliary low-power flyback converter to transfer energy during the energy flow from the AC side. The HFLC from [11] enables the capability of instantaneous power AC to DC power flow by adjustments in the modulation strategy to avoid open-circuit condition of the matrix stage. However, in this mode, the converter seems to exhibit a non-optimal transient at the start of the active state and relies on the use of the snubber circuit. Another concept that demonstrates the capability of instantaneous AC to DC power flow is based on a modified HFLC, which contains a second transformer and an extra switching leg at the DC-side along with a small RCD clamp to mitigate the error of the on-line computation of the switching instances [12].

The solutions mentioned have addressed AC-DC operation rather briefly, while experimentally it was demonstrated only during non-unity power factor operation in the inverter mode. Furthermore, in general, those topologies rely on some sort of clamping circuits or include significant modifications and added components. Such configurations with extra transformers, active switches and feedback loops add extra complexity to the baseline full-bridge topology and limit its feasibility.

The pulse-width modulation (PWM) method intended for continuous AC-DC power factor correction (PFC) operation mode without auxiliary circuits presented in [13] was further developed in [14] to allow two of the AC-side transistors operate with fundamental frequency during each half-period of the sinusoidal voltage. The principle is based on the application of short-time voltage of the opposite polarity to the transformer using the DC-side bridge prior to the start of the active state. This forces current increase from zero to the value of load current, allowing soft transient of the AC-side devices. On the other hand, in a particular implementation [14], the amount of circulating current is rather high, since the topology is operating with constant peak current that is higher than the amplitude value of the sinusoidal current drawn from the grid. Moreover, in the realized modulation method, the DC-side transistors were operating at double switching frequency.

This paper describes a new AC-DC phase-shift modulation (PSM) method for the HFLC [15]. The aim is to address the shortcomings mentioned and combine most of the advantages from existing state-of-the-art developments. The method proposed provides low duty cycle loss and allows the turn-off transient of the DC-side devices to be assisted with lossless snubber capacitors. During each grid half-period, two of the AC-devices are always on, while the rest turn off with zero current switching (ZCS). Moreover, the HFLC does not rely on an extra snubber or clamping circuits and none of the power semiconductor devices exhibit increased operating frequency.

The paper is organized as follows: Section II describes the proposed modulation technique; Section III addresses theoretical design constraints; Section IV presents the experimental verification; the conclusions are summarized in Section V.

II. Proposed Modulation Method

As it follows from the analysis in the previous section, despite several advantages, practical feasibility of the HFLCs with PFC is still limited due to several shortcomings. For instance, there was no simple and effective strategy that would allow AC-DC operation without relying on topology modifications, extra circuits or having excessive energy circulation.

The case study topology is a full-bridge HFLC shown in Fig. 1. When interfacing 230 V_{AC} mains with a relatively low voltage DC (48 V), a transformer with a relatively high turns ratio is required. In general, this leads to increased leakage inductance of the transformer and increased energy of oscillations at the AC-side, which are reflected to the DC-side, increasing the overall voltage rating requirements of semiconductors. According to previous studies [10][11][12][16], the oscillations at the AC-side cannot be easily mitigated without added circuit complexity or extra losses introduced by dissipative clamp circuits. However, for relatively low power systems (up to a few kW), added costs due to slight voltage overrating of AC-side devices can be generally tolerated, especially considering the relatively small cost of low-current 900 V and 1200 V SiC MOSFETs. On the other hand, the modulation strategy should ensure that no abrupt change of the current in the AC-side is induced. Particularly, smooth transient at the start of the active state can be provided by an additional pulse applied with the DC-side devices [13][14]. The proposed method is distinguished by arranging the switching sequence such that the reverse current interval of the DC-side devices is embedded with the gating pulse for the active state.

The proposed modulation principle is depicted in Fig. 2 and 3. The AC-side transistors are used to synthesize the sinusoidal current waveform. However, instead of PWM, phase-shift modulation (PSM) is used. Similar to other methods of this group, its advantage is minimal energy circulation at the DC-side, which is particularly beneficial in case the DC-side has relatively low voltage and high current. The duty cycles of the transistors are slightly higher than 0.5 for the AC-side and slightly lower than 0.5 for the DC-side devices. In general, the duty cycles can be kept constant throughout the entire period of the sinusoidal waveform. However, in order to reduce the amount of circulating current, a small variation of the AC-side duty cycle is introduced. The variation is provided in accordance with the instantaneous

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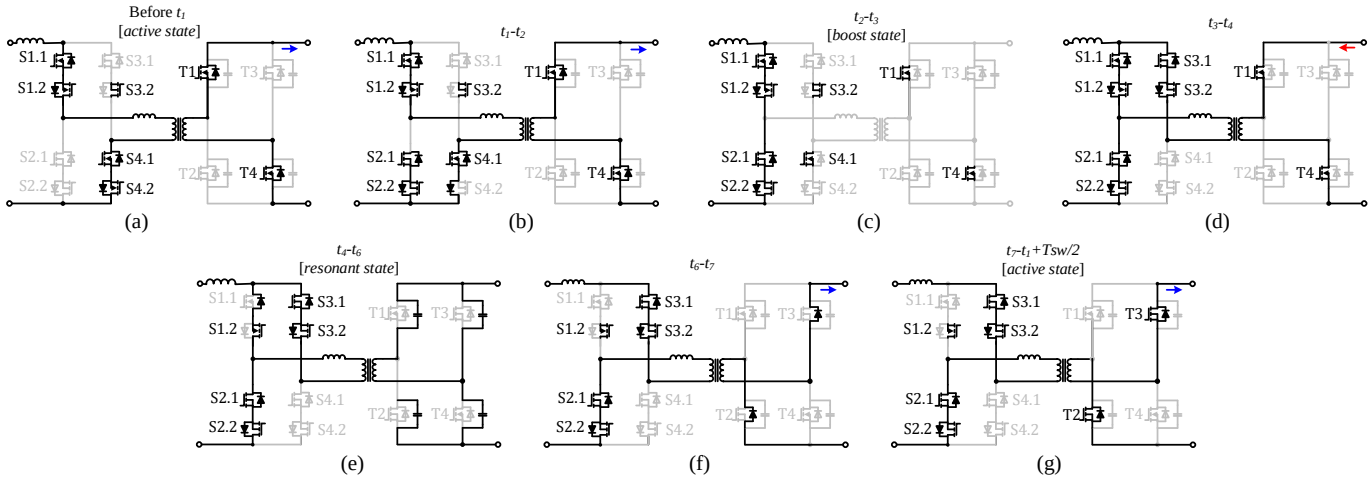

Fig. 2. Equivalent circuits representing the proposed modulation method for one switching half-period.

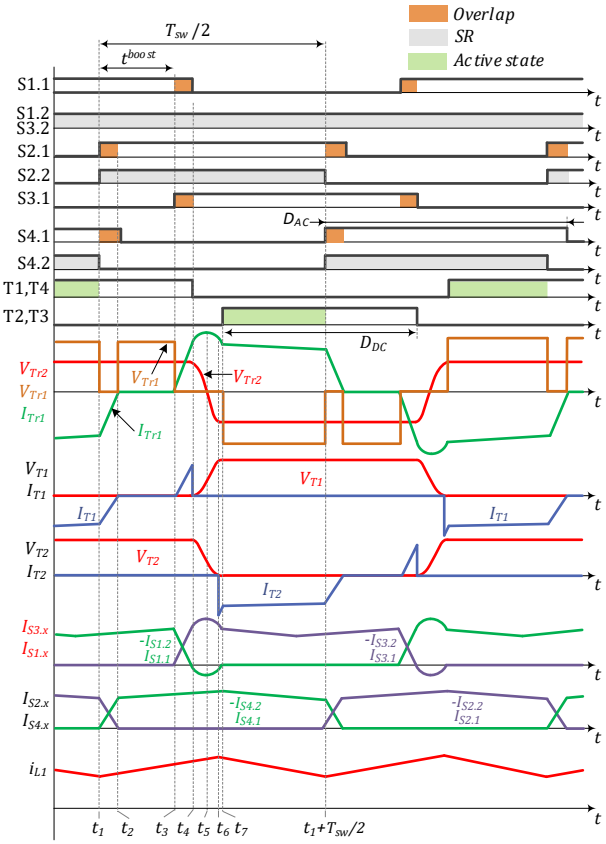

Fig. 3. Generalized modulation principle for one switching period.

value of the sinusoidal input current. The details will be presented in the next section.

It is assumed that the components are lossless and magnetizing inductance is infinitely large. The leakage inductance of the windings is represented by an equivalent series inductance at the AC-side. The DC-side transistors have a lossless snubber capacitor connected in parallel to reduce ringing and *dv/dt* during turn-off. The switching transients are described for the AC-DC power flow when v_{AC}>0 and i_{L1}>0. The transistors S1.2 and S3.2 are kept turned on for the whole duration of the fundamental half-period, while S2.2 and S4.2 operate in the synchronous rectification (SR) mode. The switching intervals distinguished are described below.

Before ***t₁***: S1.1 and S4.1 are turned on. The converter is in the active state, the input filter current i_{L1} decreases and the energy is being transferred to the load (Fig. 2a). The transistors S1.2, S4.2, T1 and T4 operate in the synchronous rectification mode to reduce conduction losses.

t₁-t₂: S2.1 is turned on, starting the transient mode. The current of S2.1 and S2.2 rises, while that of S4.1, S4.2, T1, T4 and the transformer decreases linearly with *di/dt* limited by L_{eq} (Fig. 2b). The input filter current starts to rise, while V_{Tr1} drops to zero.

t₂-t₃: The current of S2.1 and S2.2 reaches the input current level, V_{Tr1} returns to the amplitude value and the transient mode is finished. S1.1, S1.2, S2.1, and S2.2 are conducting and the input filter is energized (Fig. 2c). S1.2 and S2.2 operate in the synchronous rectification mode, while S4.1 can be turned off with ZCS.

t₃-t₄: S3.1 is turned on, starting the next transient mode. The currents of S3.1, S3.2, T1, T4 and the transformer start to rise with *di/dt* limited by L_{eq}, while the currents of S1.1 and S1.2 decrease accordingly (Fig. 2d).

t₄-t₅: The current in the converter circuit continues to rise with the same slope and increases to the value above i_{L1} (Fig. 2e). The current of S1.1 and S1.2 reverses and S1.1 can be turned off with ZCS, together with T1 and T4. The resonant process starts and snubber capacitors C_s start recharging.

t₅-t₆: The resonant process continues. The current in the circuit reaches its peak value at t_5 when the V_{Tr2} voltage crosses zero. Afterwards, the current starts to decline and the voltage V_{Tr1} changes polarity.

t₆-t₇: Snubber capacitors are completely recharged, V_{Tr2} reaches the amplitude value and the body diodes of T2 and T3 become forward biased (Fig. 2f). The S1.1 current reduces back to zero. The current of S3.1, S3.2 and I_{Tr1} becomes equal to the input current, while currents of T2 and T3 reduce to I_{Tr1}/n.

From t_7, the converter operates in the next active state (Fig. 2g). Similar processes are then repeated for another switching half-period.

The operation principle is the same when v_{AC}<0 and i_{L1}<0; in

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this case, the transistors S.2.1 and S4.1 are kept turned on and the gating signals of transistors responsible for the modulation sequence are changed correspondingly.

As it follows from the description of the switching states, the voltage polarity of the voltage at the DC-side changes when the current in the circuit is at the peak value, which is higher than the value of the input current. As a result, the transient time is relatively short even when external snubber capacitors are applied across the DC-side devices. The circulating current flows only through half of the devices at the AC-side, two of which are always in the on-state; therefore, the associated conduction and switching losses are reduced. More details on the operation and design constraints will be given in the following section.

III. Converter Analysis and Design

A. Design Constraints

To implement the proposed modulation method for the HFLC, parasitic parameters of the circuit will be utilized; therefore, several design constraints have to be taken into account.

To achieve ZCS conditions for the AC-side devices, the peak current in the circuit during t_4-t_5 should rise above the instantaneous value of the grid AC current. In this state, the energy is being transferred from the DC-side, and the current rate of rise is limited by the transformer leakage inductance. For the PSM proposed in this paper, this means that the duty cycle of the AC-side transistors should be kept higher than 0.5 by a certain pre-defined margin:

$$D_{AC} > \frac{1}{2} + \frac{2 \cdot n \cdot i_{L1} \cdot L_{eq} \cdot f_{sw}}{V_{DC}}. \quad (1)$$

where i_{L1} is the current of L_1 and L_{eq} is the equivalent circuit inductance reflected to the AC-side winding.

As a result, D_{AC} is strongly dependent on the transformer leakage inductance. Higher values will result in a reduced *di/dt* and allow for an easier and more precise control of the peak current. On the other hand, the duty cycle loss and the energy of oscillations increase, which may lead to the requirement of additional snubber circuits. Likewise, lower L_{eq} values lead to higher *di/dt*, which has a negative impact on proximity losses and may require transformer litz wire strands of thinner diameter to reduce winding losses. Moreover, the i_p value becomes more sensitive to component parameter mismatch and D_{AC} variation.

The equivalent capacitance of DC-side MOSFETs defines the maximum duty cycle D_{DC}. In the following analysis, the capacitances of the DC-side devices are represented by a common equivalent capacitance reflected to the AC-side:

$$C_{eq} = \left(C_{oss} + C_s\right) \cdot n^2. \quad (2)$$

The condition for ZVS is that C_{eq} should be completely recharged prior to the turn-on of the DC-side devices. As was mentioned, in the proposed modulation method, the recharge takes place when the current in the circuit is at the peak value. The duration of the capacitor recharge interval can be estimated by

$$t_{4\text{-}6} = t_{res} = \frac{1}{\pi \cdot f_r} \cdot \left[\frac{\pi}{2} - arctg\left(\frac{n \cdot i_p \cdot Z_r}{V_{DC}}\right)\right], \quad (3)$$

where $Z_r = \sqrt{L_{eq} / C_{eq}}$ and $f_r = 1/\left(2 \cdot \pi \cdot \sqrt{L_{eq} \cdot C_{eq}}\right)$.

During the resonant interval when the transformer DC-side voltage crosses zero, the peak current rises above the i_p value and reaches its maximum at t_5:

$$i'_p = \sqrt{i_p^2 + \left(\frac{V_{DC}}{n \cdot Z_r}\right)^2}, \quad (4)$$

The maximal duty cycle of DC-side devices can be defined by

$$D_{DC} < \frac{1}{2} - t_{res} \cdot f_{sw}. \quad (5)$$

To ensure that the converter is operating as intended, it is required to take into account the minimal duration of the non-active (boost) state:

$$t_{\min}^{boost} \approx \frac{2 \cdot n \cdot L_{eq} \cdot i_p}{V_{DC}} + t_{res} \quad (6)$$

Next, the required transformer turns ratio n can be determined for the minimal DC-side voltage $V_{DC(\min)}$:

$$n = \frac{V_{DC(\min)} \cdot \left(1 - t_{\min}^{boost} \cdot f_{sw}\right)}{V_{AC(\max)}} \quad (7)$$

where $V_{AC(\max)}$ is the amplitude value of the grid sinusoidal voltage.

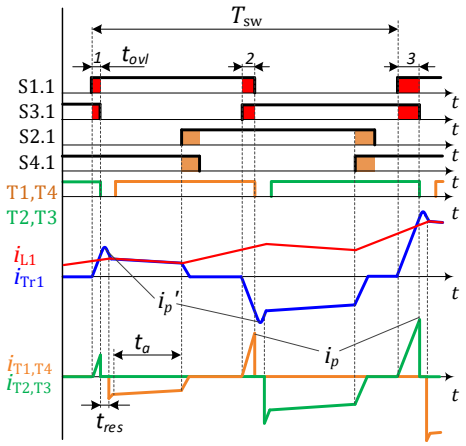

Fig. 4. Generalized representation of the proposed modulation featuring time-variable i_p.

B. Peak current regulation

The analysis in the previous sections has shown that the correct converter operation under the proposed modulation method is associated with a certain amount of energy circulation that is dependent on the value of i_p, which is higher than i_{L1}. However, if the i_p value is kept constant, as in [14], the peak current in the circuit will be unnecessarily high, particularly when the operating point moves away from the sine amplitude value or if the converter is operating with partial load. A small variation of the AC-side duty cycle can

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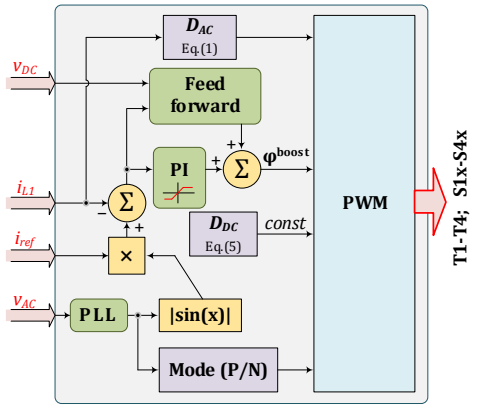

Fig. 5. Simplified control block of the HFLC.

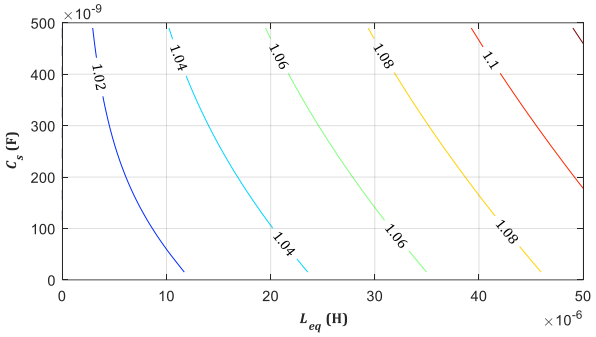

Fig. 6. Minimal ratio $V_{Tr1}/V_{AC(max)}$ for different C_s and L_{eq} values (i_p=i_{L1}).

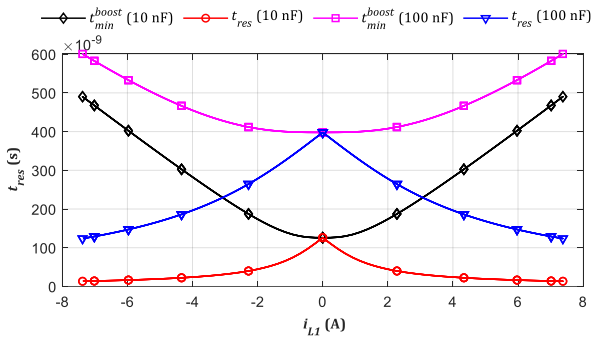

Fig. 7. Duration of t_{min}^{boost} and t_{res} for different C_s values (i_p=i_{L1}, L_{eq}=15μH).

be introduced to adjust the i_p value and make it follow the instantaneous value of i_{L1}. This way, the i_p value will be determined by the varying overlap time t_{ovl}. The idea is illustrated in Fig. 4. As shown in the figure, only the duty cycles of transistors S1.1 and S3.1 (for positive i_{L1} current polarity) need to be adjusted, while the operation of the remaining devices remains unchanged.

Since during t_6-t_7, the peak current reduces back to the value of the input sinusoidal current (with the same *di/dt*), lack of very precise control of i_p would not result in a significant increase in energy circulation. Therefore, on-the-fly control of D_{AC} can be implemented relatively easily, only ensuring that the condition i_p>i_{L1} is satisfied. In this case, the energy circulation and losses would be further reduced. To implement time-varying i_p in the practical system, it is sufficient to know only the recent value of the i_{L1}. Assuming that the leakage inductance is known, the method can be implemented using (1) with the same current sensor utilized for PFC, as high-bandwidth current measurement or detection is not necessary. As a result, the modulation method can tolerate certain component parameter mismatch and inaccuracy in D_{AC} estimation, which can be updated only once in several switching periods. The simplified control block for the realization of the proposed modulation principle in the HFLC is shown in Fig. 5.

C. Component stresses

As was mentioned, HFLC operation in the AC-DC mode is similar to that of a boost converter. Therefore, the steady-state voltage across V_{Tr1} is always higher than the amplitude value of the grid voltage. At the same time, the voltage stress at the AC-side is also influenced by the t_{min}^{boost} value. For the HFLC with the parameters listed in Table I, the resulting characteristics are depicted in Fig. 6. The minimal V_{Tr1} here is increased together with both L_{eq} and C_s. In case time-varying i_p is implemented, according to (6), the first term of the sum increases, while the second decreases together with i_p. As illustrated in Fig. 7, the peak duration is at the maximum value of the AC voltage (and current) where the contribution of t_{res} is minimal. Therefore, it can be concluded that the increase of t_{res} with the implementation of time-varying i_p has only minor effect on the AC-side voltage stress. At the same time, the importance of the design aimed at minimized L_{eq} value is clearly demonstrated.

According to Fig. 3, only half of the AC-side devices exhibit current rise to the i_p value, while the rest follow the i_{L1} sinusoidal wave-shape. Small difference in the operating conditions between the inner and outer AC-side transistors should not affect the choice of the semiconductor switch ratings. To maintain ZVS in the DC-side bridge, the maximal D_{DC} value using (5) should be chosen in accordance with the minimal value of i_p. Assuming that the value of i_p is time-varying and close to the i_{L1} value and the L_{eq} value is relatively small, the rms current in the AC-side transistors can be estimated by

$$i_{AC(\mathrm{rms})}^{sw} = \frac{P_{rated}}{\sqrt{2}\cdot V_{AC}}. \tag{8}$$

Likewise, the rms current in the transformer AC-side is

$$i_{Tr1(\mathrm{rms})} = \frac{\sqrt{6}\cdot P_{rated}}{3\cdot V_{AC}}; \tag{9}$$

and the rms current of the DC-side transistors is

$$i_{DC(\mathrm{rms})}^{sw} = \frac{i_{Tr1(\mathrm{rms})}}{\sqrt{2}\cdot n}. \tag{10}$$

Based on the analysis, with the peak current regulation, the current stresses of HFLC show that during most of the boost state, the current at the DC-side and the transformer are close to zero. The voltage stress on the DC-side semiconductor devices is equal to V_{DC}, while the steady-state voltage stress on the AC-side devices is V_{DC}/n. It should be noticed that in practice, with the HFLC of this type, additional voltage stress occurs due to ringing between the parasitic capacitances on the AC-side switches and L_{eq}.

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D. Transformer design considerations

The analysis above shows that the transformer with a low value of leakage inductance is required in order to reduce the HFLC duty cycle loss and component stresses. One of the possibilities is to apply a planar transformer, which has been reported to achieve low leakage inductance values [17]. On the other hand, these transformers have a pronounced trade-off between the leakage inductance and stray capacitance [18], with both being undesirable for the HFLC [19]. Another method is to utilize fractional-turn designs, as in [20]. Despite the possibility of utilizing a standard core, the winding layout of such design is quite specific and may bring additional manufacturing costs. Moreover, the designs mentioned are generally associated with a relatively low number of turns, which leads to a relatively small magnetizing inductance. Since the magnetizing current is not utilized for ZVS with the proposed algorithm, reduced magnetizing inductance will result in increased energy circulation, without bringing positive benefits.

For the experimental prototype, the transformer was realized using the standard ETD59 core. The conventional interleaving technique was applied, with a layer of secondary winding located between the two layers of primary (low current) winding (P|S|P). The parameters of the transformer are listed in Table I.

IV. Experimental Verification

The proposed modulation method was verified with 230 V_{AC}/48 V_{DC} experimental HFLC prototype. The Si MOSFETs with the voltage rating of 80 V are used at the DC-side, while the AC-side uses 900 V SiC MOSFETs. The prototype uses natural convection heatsinks and its main components are listed in Table I. Synchronous rectification was applied to the corresponding AC-side devices to reduce conduction losses.

TABLE I
SPECIFICATIONS OF THE CONVERTER PROTOTYPE

Parameter	Symbol	Value
DC-side voltage	V_{DC}	48 V
AC-side voltage	V_{AC}	230 V
Switching frequency	f_{sw}	50 kHz
Transformer turns ratio	n	6/58
Transformer leakage inductance	L_{eq}	16.7 µH
Transformer leakage inductance	L_m	17 mH
Rated power	P_{rated}	1200 W
Input capacitor (DC-side)	C_{DC}	6×2500 µF (63 V)
Snubber capacitors (DC-side)	C_s	100 nF
Parasitic capacitance of AC switches	C_p	20 pF
Input inductor (AC-side)	$L1$	2.5 mH
DC-side transistors	T1-T4	IPB017N08N5
AC-side transistors	S1.x-S4.x	C3M0280090D
Microcontroller	-	TMS320F28379

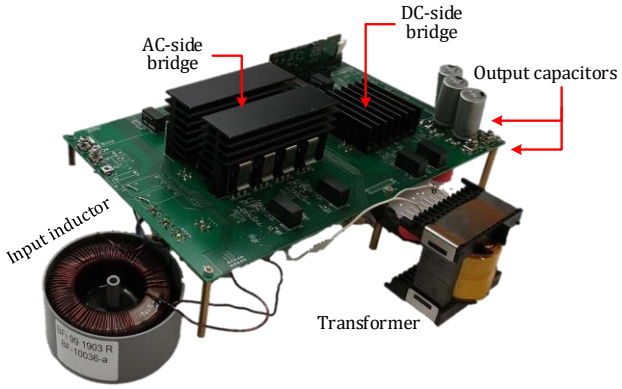
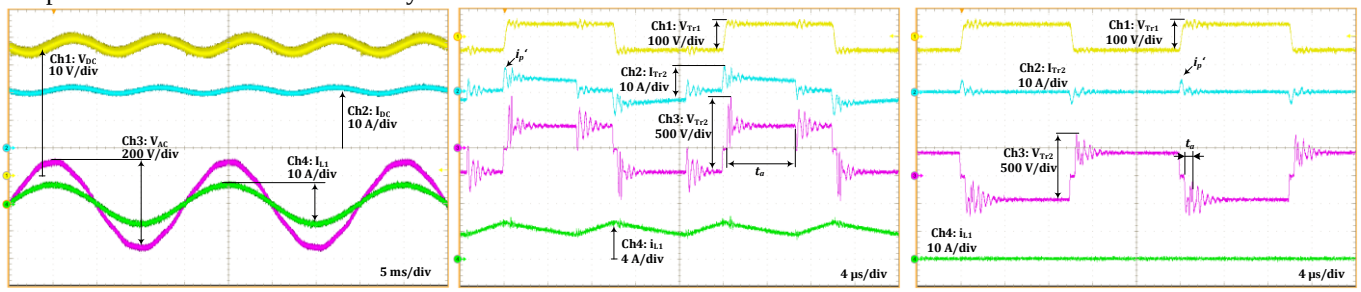
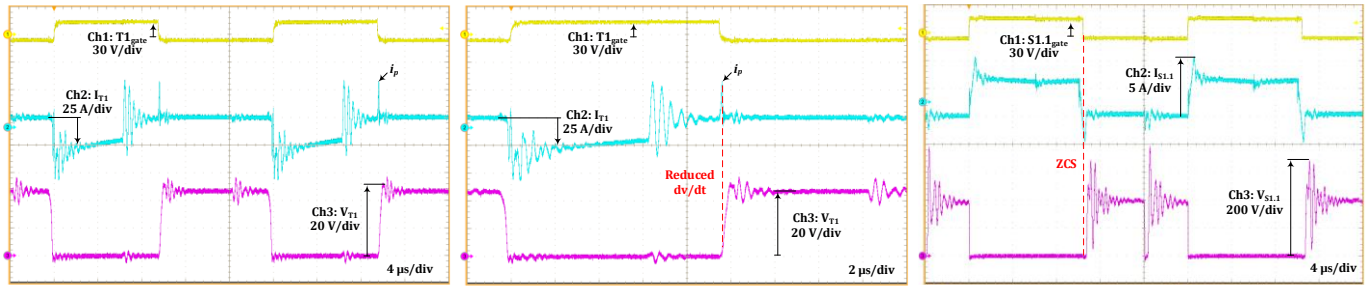


Fig. 8. Photo of the HFLC prototype.



(a) (b) (c)

Fig. 9. Input/output voltages and currents (a); transformer waveforms when i_{L1} is at average level (b) and close to zero (c).



(a) (b) (c)

Fig. 10. Switching transients: T1 at average current (a), zoomed in T1 turn-off process (b), S1.1 during positive half-period of i_{L1} (c).

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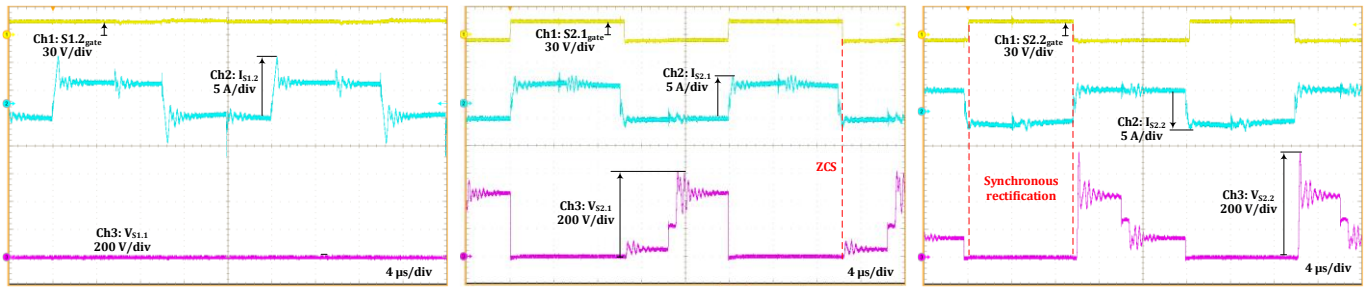

(a) (b) (c)

Fig. 11. Switching transients during the positive-half-period: S1.2 (a), S2.1 (b) and S2.2 (c).

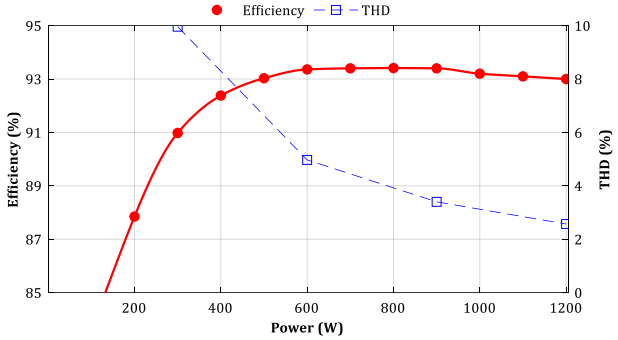

Fig. 12. Power stage efficiency and estimated THD of the experimental HFLC in the AC-DC mode.

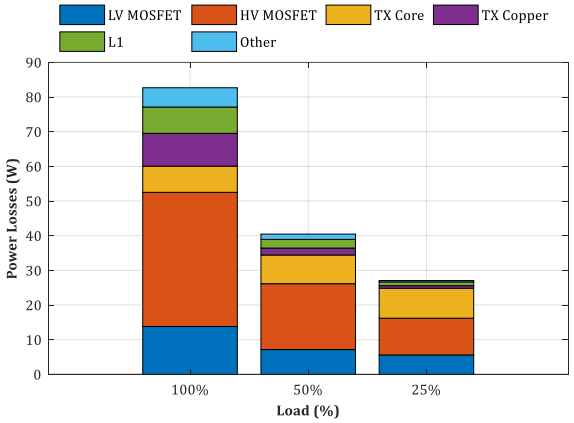

Fig. 13. Estimated power loss breakdown at different loads.

The input/output voltage and current waveforms of the HFLC sourcing sinusoidal current from the grid are shown in Fig. 9a. The transformer waveforms are depicted in Fig. 9b and 16c. When operating with near zero current, only minor current circulation occurs to recharge the snubber capacitors across the DC-side transistors. The ringing in the primary is damped and only a small voltage distortion can be seen at the DC-side. The current peak occurs at the beginning of the active state during the voltage polarity reversal at the transformer secondary. The experimental waveforms demonstrating the transistor switching transients are presented in Fig. 10 and 11. Transistor T1 mostly operates in the SR mode and only close to the end of the turn-on interval, a short current with reverse polarity (i_p) appears across the device (Fig. 10a). After removal of the gate signal, the snubber capacitor across the device starts to charge with the reduced *dv/dt* (Fig. 10b). The ZCS of the S1.1 transistor is demonstrated in Fig. 10c. Transistor S1.2 is constantly turned on during the positive half-period, thus only small on-state voltage appears across the device (Fig. 11a). The current across the bottom devices has no circulating component (i_p): S2.1 operates with ZCS (Fig. 11b), while S2.2 operates in the SR mode. The power stage efficiency at the rated power was at 93.0% (Fig. 12). The estimated power loss breakdown of the converter power stage is depicted in Fig. 13. The other losses account for losses in the PCB and interconnections. The losses in measurement and auxiliary circuits of around 5 W are not included, as these circuits have not been optimized. The voltage ringing with the peak amplitude of around 800 V can be observed across the AC side devices, which is nearly twice the steady-state value. As was mentioned, damping of these oscillations requires extra snubber/clamping circuits or topology modifications, such as the solutions presented in [10][11][12][21]. On the other hand, with the wide availability of 900 V SiC MOSFETs, such voltages can be tolerated without adding extra circuit complexity.

V. Discussion and Conclusions

Despite the concept of the HFLC was proposed a while ago, it has not received sufficient industrial adoption. In addition to

TABLE II
Characteristics of Different HFLCs Operating in the AC-DC Mode

Ref.	Modulation Type	Voltage		Power (W)	Frequency (kHz)	AC-side devices at grid frequency	Specifics
		AC (V_{rms})	DC (V_{DC})				
[14]	DC-side	21.3	120	60	50	2	DC-side devices operate at double frequency; high circulating current $i_p > i_{ac(max)}$
[10]		120	300	1200	50	2	Use external flyback snubber for enabling AC-DC power flow/mitigation of voltage spike
[11]	AC-side	110	35…50	260	25	0	
[8]		240	400	1200	54	4	Hard switched; snubber required
[12]		230	34	320	25/50	0	Modified topology with 2 transformers and extra switching leg
Proposed		230	48	1200	50	2	Snubber optional

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relative complexity of voltage overshoots, there was general lack of effective modulation methods for the AC-DC power flow. This has hindered the use of HFLCs as rectifiers or in applications where continuous bidirectional operation was required. Many of the existing solutions have operating conditions for the AC-DC mode that differ from those in the DC-AC mode, or require additional auxiliary circuits. As a result, the performance of both of the modes was different. Several reported modulation methods are compared in Table II. The presented AC-DC PSM method with the time-varying duty cycle and the DC-AC modulation proposed in [9] both feature very similar switching conditions and share several common advantages:

- external auxiliary circuit or snubber is not required and only a few constraints have to be followed;
- operating conditions for DC-side devices are comparable − ZVS and soft turn-off with reduced *dv/dt*;
- DC-side ZVS with constant duty cycle is ensured without relying on the transformer magnetizing inductance; no signal swapping or double switching frequency of DC-side transistors is required;
- ZCS of the AC-side devices with two inner transistors is operating at the fundamental frequency;
- benefits of the AC-side modulation are attributed − no current is present in the transformer during the boost state with small overall energy circulation.

At the same time, resulting from the switching mode analysis, it can be concluded that the HFLC operation with the proposed modulation method is very highly influenced by the equivalent inductance value. Minimal transformer leakage inductance has to be provided in the design. Moreover, the performance is sensitive to parameter mismatch; therefore, it is required to minimize components parameter variation, especially for the transformer. Due to relatively high currents, only NP0/C0G type capacitors are suitable as DC-side snubbers. Despite the problem of voltage overshoot being mitigated, the parasitic oscillations due to transformer leakage inductance and the parasitic capacitance of AC-side devices still remain. It will increase the voltage stress to 1.7…2 times the V_{DC}/n value. These oscillations occur regardless of the modulation method applied and have been addressed by several solutions, which typically use auxiliary snubber circuits. Alternatively, the design with minimal values of parasitic elements and slightly voltage overrated semiconductors may prove more cost-efficient, particularly for relatively low power HFLCs.

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