Doctoral theses at NTNU, 2022:59

Andreas Giannakis

Design of High-Performance Solid-State Circuit Breakers for LVDC and MVDC Applications

Doctoral thesis

NTNU
Norwegian University of Science and Technology
Thesis for the Degree of
Philosophiae Doctor
Faculty of Information Technology and Electrical Engineering
Department of Electric Power Engineering

NTNU
Norwegian University of
Science and Technology

Andreas Giannakis

Design of High-Performance Solid-State Circuit Breakers for LVDC and MVDC Applications

Thesis for the Degree of Philosophiae Doctor

Trondheim, February 2022

Norwegian University of Science and Technology
Faculty of Information Technology and Electrical Engineering
Department of Electric Power Engineering

NTNU
Norwegian University of
Science and Technology

NTNU
Norwegian University of Science and Technology

Thesis for the Degree of Philosophiae Doctor

Faculty of Information Technology and Electrical Engineering
Department of Electric Power Engineering

ISBN 978-82-326-5896-1 (printed ver.)
ISBN 2978-82-326-6016-2 (electronic ver.)
ISSN 1503-8181 (printed ver.)
ISSN 2703-8084 (online ver.)

Doctoral theses at NTNU, 2022:59

Printed by NTNU Grafisk senter

Abstract

Today, the emerging technology of LVDC and MVDC grids is under extensive research. These grids ease the integration of distributed electricity generation systems and offer several advantages over the AC counterparts, such as lower transmission losses at the same voltage level. However, the lack of a high-performance protection scheme against DC short-circuits is currently the main showstopper for their further development. Three main circuit breaker topologies have been proposed for the fault clearance in DC grids. Among them, the solid-state breaker exhibits the highest speed of breaking operations at a cost of high conduction losses caused in power semiconductor devices. This PhD thesis investigates primarily the design of solid-state DC breakers with the aim of minimizing their conduction losses. For this purpose, the conducting performance of several commercial Silicon and SiC semiconductor technologies with blocking voltage in the range of $1200-1700V$ have been extensively evaluated. Experimental results revealed that the normally-ON SiC JFETs achieved the lowest conduction losses for medium-power LVDC and MVDC solid-state breakers. On the other hand, at high-power MVDC applications, three high-voltage power semiconductor devices are identified. It has been shown that the IGCT-based breakers exhibit the lowest conduction losses. However, to avoid complicated gate driver designs utilized in IGCTs, the use of the gate voltage-controlled IGBTs for high-power solid-state breakers is imposed.

Additionally, this PhD thesis proposes the concept of applying the maximum gate voltage (overdrive) to the active power semiconductor devices used in solid-state breakers in order to minimize the conduction power losses. Especially in SiC MOSFETs and in normally-ON SiC JFETs, the forward voltage drop is reduced significantly compared to IGBT-based semiconductor technologies. In particular, experimental results showed that the normally-ON SiC JFET achieves a conduction loss reduction up to 33% at 55% of normalized current when overdriving.

Three overvoltage suppression configurations used in solid-state breakers for $700-1800V_{DC}$ applications have been experimentally evaluated in terms of electro-thermal performance and passive components requirements. The feasibility and the application-oriented usability of MOVs as an overvoltage suppression configuration for medium-power solid-state LVDC and MVDC breakers has been demonstrated. In addition, the applicability of using both RCD snubber circuits and MOVs as an overvoltage suppression configuration for high-power MVDC solid-state breakers is also revealed.

The voltage level of an MVDC grid can be significantly higher than the blocking voltage of a high-voltage semiconductor device. This imposes the need for

series-connecting a high number of devices for the breaker design. However, this practice introduces design challenges, such as uneven voltage distribution among the devices during the breaking operation. A hybrid method for designing a solid-state MVDC breaker employing series-connected IGBTs with minimum snubber capacitances requirements is proposed. This method is based on the combination of RCD snubber circuits and a gate coupled transformer. The proposed method minimizes the snubber capacitances by 60% compared to a reference configuration which only consists of RCD snubber circuits, when a gate signal propagation delay of $1\mu s$ between two series-connected IGBTs is introduced. Finally, in a $3kV_{DC}$ study, experimental results showed that by keeping the same snubber capacitance, the voltage difference between two IGBTs was measured to be $380V$ without the use of the gate coupled transformer. On the other hand, in the proposed scheme, the corresponding voltage difference was reduced to $60V$.

Finally, the design of an automatic and self-powered solid-state breaker using normally-ON SiC JFETs suitable for a $700V_{DC}$ grid is proposed. This breaker exhibits low conduction losses and it also eliminates the need for external auxiliary circuits used for fault sensing and gate-driver supply. The effectiveness of the breaker has been experimentally validated by interrupting a fault current of $33A$ within $330\mu s$.

Acknowledgements

First and foremost, I have to thank my parents, Evangelos and Anna and my brother, Konstantinos for providing me with unfailing support and continuous encouragement throughout my years of study and through the process of researching and writing this thesis. My thoughts also go to my beloved grandmother, Tasoula, who passed away recently, and who had always been supportive to me and to my personal goals. This accomplishment would not have been possible without them.

I must also express my very profound gratitude to my main supervisor, professor Dimosthenis Peftitsis. Without his assistance and dedicated involvement in every step throughout the PhD process, this thesis would have never been accomplished. Our technical and social discussions as well as his lab guidance have made me a more mature and complete person and a more experienced engineer. Dimos has been not only a great supervisor, but also a mentor and a great friend to me.

I have spent all my PhD time at NTNU, in Trondheim, Norway. During these four years, I have been part of a friendly and warm atmosphere in the Electric Power Engineering department. I also had the pleasure to meet and spend time with many colleagues. Funny stories, jokes, "teasing" each other, as well as technical and philosophical discussions during the coffee breaks have made my PhD journey not only more entertaining, but also more productive. For this, I need to thank many of my colleagues that I can now call them friends. It is, Aravinda, Atousa, Augusto, Babak, Dan El, Daniel, Erick, Gard, Gilbert, Ole-Christian, Rahgbendra, Reza, Santiago, Spyros, Subhadra, Tobias and Yoga. I also wish to show appreciation to the technical and administrative staff at the department who have been very helpful to me throughout the PhD duration.

The football practices have always been the best "therapy" to recover and forget sad and frustrating moments that normally happen during the PhD time. I therefore need to thank all members of the football team at the department, called "Power Challengers" for providing me many enjoyable moments.

Finally, I wish to extend my special thanks to a few more friends. It is their company which made my stay in Trondheim during the PhD time more pleasant. To Michalis V., Doc, George, Spyros, Lina, Stefanos, Artemis, Michalis S., Thomais, and Panos. Thank you all for the great memories. And to Hanne who supported my PhD journey to reach the final destination with her love, her company and her encouragement. Tusen takk.

Abbreviations

ASP	Automatic and Self-Powered
BIGT	Bi-mode Insulated Gate Transistor
BiMOSFET	Bipolar Metal-Oxide Semiconductor Field Effect Transistor
DUT	Device Under Test
FS	Field-Stop
GDU	Gate Drive Unit
GTO	Gate Turn-OFF
HVAC	High-Voltage Alternating Current
HVDC	High-Voltage Direct Current
IEC	International Electrotechnical Commission
IEEE	Institute of Electrical and Electronics Engineers
IGBT	Insulated Gate Bipolar Transistor
IGCT	Integrated Gate Commutated Thyristor
JFET	Junction Field Effect Transistor
LVDC	Low-Voltage Direct Current
MMC	Modular Multilevel Converter
MMC-FB	Modular Multilevel Converter with full bridge sub-modules
MMC-HB	Modular Multilevel Converter with half bridge sub-modules
MOSFET	Metal-Oxide Semiconductor Field Effect Transistor
MOV	Metal-Oxide Varistor
MVAC	Medium-Voltage Alternating Current
MVDC	Medium-Voltage Direct Current
NPC	Neutral-Point Clamped

NPT	Non-Punch-Through
PT	Punch-Through
RCD	Resistor-Capacitor-Diode
SiC	Silicon Carbide
SM	Sub-modules
VSC	Voltage Source Converter

Contents

List of Tables

List of Figures

Chapter 1

Introduction

1.1 Background

The urgent need for decarbonization of the environment is imposed by the low-carbon emission strategies adopted by several countries worldwide [1]. Decarbonization of the electricity sector necessitates the transformation of the existing electric power grid through the ever-increasing integration of renewable energy sources (RES) and the electrification of transportation sector. Grid transformation will be enabled by two key technologies, namely multi-terminal transmission and distribution grids and power electronic converters, which must exhibit the highest ever efficiency, power flow flexibility and supply reliability.

Today, with the tremendous technological development of high-voltage and high-power semiconductor devices, design of high-power electronic converters operating with medium and high-voltages and reaching record efficiencies becomes feasible [2, 3, 4, 5, 6]. Power converters are the catalyst that pave the way towards the development of Low-Voltage Direct Current (LVDC) and Medium-Voltage Direct Current (MVDC) grids. LVDC and MVDC grids ease the integration of RES and utility-scale battery storage dealing with intermittency of RES, as well as the electrification of DC loads such as large-scale charging infrastructure, by minimizing the required electrical energy conversion stages compared to Alternating Current (AC) counterparts. Besides, DC grids exhibit lower transmission and distribution losses than AC grids at the same voltage level [7]. However, the lack of a high-performance short-circuit protection schemes in LVDC and MVDC grids is currently the main showstopper for their further development.

In AC grids, short-circuit faults are cleared by using the state-of-the-art mechanical AC breakers technology. However, this technology is not suitable for clearing DC short-circuit faults due to the absence of current zero crossing, which in AC breaker is the necessary condition to extinguish the fault current. During the last decade,

several LVDC and MVDC circuit breakers have been proposed. A promising DC circuit breaker technology is the solid-state breakers. Solid-state breakers exhibit the shortest fault clearance times and require the least maintenance compared to other DC breaker topologies. Nevertheless, the main design challenge of the solid-state breakers is the high conduction power losses caused in the employed power semiconductor devices. In addition, the development of an application-oriented overvoltage suppression circuit for LVDC and MVDC breakers is also missing. Furthermore, the voltage level of an MVDC grid necessitates the use of multiple series-connected power semiconductor devices, which imposes design challenges related to the even voltage distribution among the devices during the breaking operation. Finally, the fast and efficient coordination between the circuit breaker and the fault detection circuit should also be considered when designing a solid-state breaker. A possible solution to this challenge is the development of an automatic breaker, which detects and interrupts the fault current without the need of external fault detection circuit.

1.2 Objectives and scope of the thesis

1.2.1 Objectives of the thesis and research questions

This PhD project was funded by the Faculty of Information Technology and Electrical Engineering at the Norwegian University of Science and Technology, NTNU. The title of the research project was "Power electronics for DC circuit breakers". The primary objective of the project is **"to advance the design and performance of solid-state circuit breakers for LVDC and MVDC applications by delivering novel concepts and methodologies for breakers design and operation."** From the beginning, two main research questions regarding the main objective were raised; *(i) are the solid-state breakers a feasible protection solution against DC short-circuits that will ease the development of LVDC and MVDC grids? and (ii) what are the design and operating challenges of the solid-state DC breakers?*

Several secondary objectives were also defined during the PhD work. These objectives are listed as follow.

- To deliver LVDC and MVDC solid-state breakers exhibiting the lowest conduction losses.
- To assess the state-of-the-art power semiconductor technologies used in solid-state breakers for minimizing conduction losses.
- To design and evaluate application-oriented overvoltage suppression configurations for LVDC and MVDC solid-state breakers.
- To design low-footprint overvoltage suppression configurations for MVDC solid-state breakers.
- To develop a self-triggered solid-state DC breaker.

During the PhD work and towards the accomplishment of these objectives, additional research questions were raised. Among others; *(i) can the Silicon Carbide (SiC) power semiconductor devices be utilized in the design of the future solid-state DC breakers in order to minimize the conduction losses? (ii) what is the significance of the overvoltage suppression circuits on the performance and the size of the breaker? (iii) what are the design challenges of a solid-state breaker that requires multiple series-connected semiconductor devices? and (iv) what are the advantages of a self-triggered solid-state breaker?*

The main direction of this PhD thesis is to complete the defined objectives by finding answers to the research questions presented above.

1.2.2 Scope of the thesis

The scope of this PhD thesis is to demonstrate the use of solid-state circuit breakers in future LVDC and MVDC grids as a feasible solution. In general, solid-state breakers exhibit fast operation at a cost of high conduction losses. Thus, the optimal design of solid-state breakers for achieving high efficiency has been the main focus of this thesis. The performance evaluation of several Silicon and SiC semiconductor device technologies for the design of such breakers in terms of conduction losses has been conducted. In addition, the concept of overdriving active power semiconductor devices in order to improve their conducting performance by reducing conduction losses has also been proposed and investigated.

Apart from the conduction losses in a breaker design, the overvoltage suppression circuits can also be critical. The applicability and usability of three overvoltages suppression configurations used in LVDC and MVDC solid-state breakers has also been assessed with the focus on minimizing the electrical and thermal stress of the breaker itself and of other grid components.

Besides that, the design of a compact solid-state MVDC breaker is also within the scope of this PhD thesis. A hybrid overvoltage suppression scheme for MVDC solid-state breakers employing series-connected Insulated Gate Bipolar Transistor (IGBT)s for reducing the snubber capacitances requirements is proposed. The minimized snubber circuits lead to lower weight and smaller volume of the overall breaker design and thus, the entire solid-state breaker becomes more compact.

Finally, the development of an automatic and self-powered solid-state DC breaker eliminating the need for fault detection circuit and exhibiting low conduction losses is also in the scope of this PhD thesis. This has been assessed by designing a breaker using normally-ON SiC Junction Field Effect Transistor (JFET)s and coupled inductors, which feeds the gate with the required negative voltage during a breaking operation.

1.3 Thesis outline

Chapter 1 introduces the topic of the thesis. In addition, it presents the scope and the contributions of the PhD thesis.

Chapter 2 presents the protection challenges against short-circuits in LVDC and MVDC grids focusing on the need for developing high-performance solid-state circuit breakers.

Chapter 3 analyses several Silicon and SiC power semiconductor device technologies that can be used in solid-state LVDC and MVDC breakers for medium-power and high-power grids. Additionally, the impact of overdriving the active devices on the conduction losses is presented via experiments.

Chapter 4 presents three overvoltage suppression configurations for semiconductor devices used in solid-state LVDC and MVDC breakers, as well as their application-specific usability. The advantages and disadvantages of each configuration are analyzed via simulations and experiments.

Chapter 5 proposes a hybrid method to mitigate voltage imbalances among series-connected IGBTs used in an MVDC solid-state breaker during a short-circuit clearance operation. This method includes Resistor-Capacitor-Diode (RCD) snubber circuits and a magnetically coupled gate transformer aiming at minimizing the snubber capacitance requirements. Additionally, simulations and experimental results are also included to validate the proposed method.

Chapter 6 presents an automatic and self-powered solid-state breaker concept for $700V_{DC}$ grids, using normally-ON SiC JFETs. This concept eliminates both fault detection circuit and external auxiliary power supply, and it also achieves low conduction losses. The proposed breaker has been validated through simulations and experiments.

Chapter 7 summarizes the main conclusions of the thesis. It also presents future research directions related to the topic of this PhD thesis.

1.4 Research contributions

The main contributions of this PhD thesis can be summarized as follow.

- Demonstration and validation of the benefits of using solid-state breakers for LVDC and MVDC grids.
- Identify the normally-ON SiC JFETs as the best-performing power semiconductor technology enabling the lowest conduction losses for the design of medium-power LVDC and MVDC solid-state breakers.

- Develop an overdriving operating methodology for Silicon and SiC power semiconductor technologies to minimize the conduction losses.
- Demonstrate the feasibility and the application-oriented usability of Metal-Oxide Varistor (MOV)s as an overvoltage suppression configuration for medium-power solid-state LVDC and MVDC breakers.
- Demonstrate the applicability of using both RCD snubber circuits and MOVs as an overvoltage suppression configuration for high-power MVDC solid-state breakers.
- Design of a compact solid-state MVDC breaker employing series-connected IGBTs with minimum snubber capacitances requirements.
- Design of an automatic and self-powered solid-state breaker using normally-ON SiC JFETs, exhibiting low conduction losses and eliminating the need for external auxiliary circuits.

The contributions are further explained in the beginning of each Chapter. The scientific findings from this PhD thesis have been published in four journal articles and six conference papers. These can be found under "List of Publications" below. Additionally, two more conference papers have been published during the PhD work, and these are listed under "Other Publications".

List of Publications

[P1] **A. Giannakis** and D. Peftitsis, "Design Considerations of Power Semiconductor Devices Employed in VSCs Under Short-Circuit Fault Conditions in MVDC Distribution Grids," 2018 20th European Conference on Power Electronics and Applications (EPE'18 ECCE Europe), 2018, pp. P.1-P.11.

[P2] **A. Giannakis** and D. Peftitsis, "MVDC Distribution Grids and Potential Applications: Future Trends and Protection Challenges," 2018 20th European Conference on Power Electronics and Applications (EPE'18 ECCE Europe), 2018, pp. P.1-P.9.

[P3] **A. Giannakis** and D. Peftitsis, "Electro-thermal Design of a Solid-State MVDC Circuit Breaker," 2019 10th International Conference on Power Electronics and ECCE Asia (ICPE 2019 - ECCE Asia), 2019, pp. 1-8, doi: 10.23919/ICPE2019-ECCEAsia42246.2019.8797031.

[P4] **A. Giannakis** and D. Peftitsis, "Performance evaluation of high power semiconductor devices employed in solid-state circuit breakers for MVDC grids," 2019 21st European Conference on Power Electronics and Applications (EPE '19 ECCE Europe), 2019, pp. P.1-P.10, doi: 10.23919/EPE.2019.8915533.

[P5] **A. Giannakis** and D. Peftitsis, "Performance Evaluation and Limitations of Overvoltage Suppression Circuits for Low- and Medium-Voltage DC Solid-State Breakers," in IEEE Open Journal of Power Electronics, vol. 2, pp. 277-289, 2021, doi: 10.1109/OJPEL.2021.3068531.

[P6] **A. Giannakis** and D. Peftitsis, "An Automatic and Self-Powered Solid-State DC breaker with Normally-ON SiC JFETs," PCIM Europe digital days 2021; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management, pp. 1-7.

[P7] **A. Giannakis** and D. Peftitsis, "Voltage Balancing Considerations for Series-Connected IGBTs in MV Solid-State DC Breakers," 2021 IEEE 12th Energy Conversion Congress & Exposition - Asia (ECCE-Asia), 2021, pp. 580-585, doi: 10.1109/ECCE-Asia49820.2021.9479127.

[P8] **Giannakis, A**, Peftitsis, D. A universal automatic and self-powered gate driver power supply for normally-ON SiC JFETs. IET Power Electron. 2021; 14: 1820– 1833. https://doi.org/10.1049/pel2.12151

[P9] **A. Giannakis** and D. Peftitsis, "Overvoltage Suppression Scheme for Minimized Snubber Requirements in MVDC Solid-State Breakers with Series-Connected IGBTs," submitted in IEEE Journal of Emerging and Selected Topics in Power Electronics. (Accepted under major revision)

[P10] **A. Giannakis** and D. Peftitsis, "Comparative Evaluation of Silicon and SiC Power Semiconductors for Solid-State DC Breakers," submitted in IEEE Transactions on Power Electronics. (Accepted under major revision)

Other Publications

[O1] S. J. K. Berg, **A. Giannakis** and D. Peftitsis, "Analytical design considerations for MVDC solid-state circuit breakers," 2019 21st European Conference on Power Electronics and Applications (EPE '19 ECCE Europe), 2019, pp. 1-10, doi: 10.23919/EPE.2019.8915142.

[O2] T. N. Ubostad, **A. Giannakis**, G. L. Rodal, D. A. Phillips and D. Peftitsis, "Reduction of Parasitic Inductance and Thermal Management in a Multi-chip SiC Half-Bridge Module," PCIM Europe digital days 2021; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management, 2021, pp. 1-7.

Chapter 2

Protection challenges in LVDC and MVDC power grids

This Chapter presents the protection challenges in DC power grids. Initially, a short introduction to LVDC and MVDC power grids is given. Then, a short-circuit fault in a DC power line along with its impact on grid components is analyzed. In addition, the basic DC circuit breaker concepts found in literature are briefly discussed. Simulation results of three such breaker concepts are presented. Lastly, the impact of a short-circuit in a DC line on the electrical and thermal stress of power semiconductors in various Voltage Source Converter (VSC)s is also investigated.

Contributions

A comparative evaluation of three main DC circuit breakers via simulations has been presented. The superior performance of solid-state DC breakers over mechanical (with active resonance circuit) and hybrid ones in terms of short clearance time and low peak fault current has been revealed [P2]. Additionally, the impact of a short-circuit in an MVDC power line on the design of four VSCs has been investigated [P1]. The simulation results showed that the long reaction time of mechanical breakers connected to the AC side leads to significantly high short-circuit current flowing through the antiparallel diodes of the VSCs. They also revealed that the use of solid-state DC breakers decreases drastically the fault current. This Chapter summarizes the content of three publications [P1, P2, O1].

2.1 LVDC and MVDC power grids

Today, even though electric power is transmitted by means of both High-Voltage Direct Current (HVDC) and High-Voltage Alternating Current (HVAC) power grids, the power distribution is only performed using Medium-Voltage Alternating Current (MVAC) systems. The utilization of low-frequency and reliable transformers facilitates the voltage conversion from a high level to a lower one, and vice versa. Therefore, the electric power can be generated, distributed and transmitted efficiently at various AC voltage levels, minimizing the losses at the conversion stages. However, the expansion of distributed generation, as well as the increased demand of DC loads have imposed the need for developing more DC power grids, not only for power transmission, but also for power distribution operating at LVDC and MVDC. Additionally, the liberalization of the energy market has also pave the way for integration of more LVDC and MVDC systems into the existed power grid. The benefits of transmitting electric power through DC grids over AC counterparts are as follow:

- Higher efficiency of power transmission and distribution under the same voltage levels [7]
- No need for frequency synchronization which leads to easier integration of multiple energy sources
- No reactive power and thus, no need for reactive power compensation

Furthermore, a decisive factor for the envisaged expansion of LVDC and MVDC grids is the advancement in high-power semiconductors technology. The main reason is the need for designing efficient high-voltage high-power electronic converters which will be used for the required voltage conversions. Today, the improvement of the semiconductor technology seems able to facilitate such a paradigm shift towards DC distribution grids, designing power electronic converters that minimize the power losses [2, 3, 4, 5, 6].

On the other hand, several challenges may appear when DC grids are developed. The higher investment and installation cost of power converters used in DC applications compared to the transformers in AC counterparts remain a significant drawback. Additionally, the development of a high-performance protection scheme against short-circuits slows down the expansion of more DC grids today. Last but not least, the lack of specific standardization related to the operation and safety (human safety, grounding rules, insulation requirements) of MVDC grids is also an issue that needs to be addressed soon [P2]. However, for the electrification of electric ships using MVDC, standards have been established, i.e. Institute of Electrical

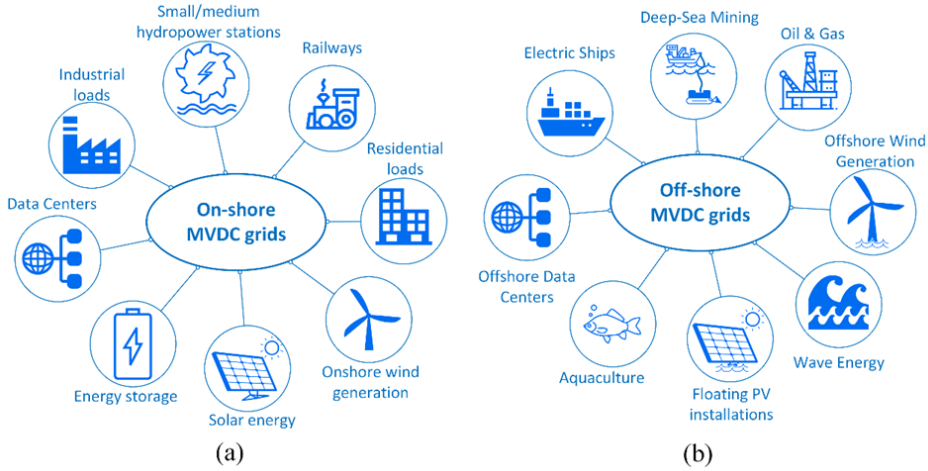


Figure 2.1: Potential MVDC grid applications for: (a) onshore and (b) offshore power grids.

and Electronics Engineers (IEEE) standard 1709-2010 [8]. Among others, IEEE recommends that MVDC starts above $1kV$ and up to and including $35kV$. In particular, this framework defines recommended voltage levels at $1.5kV$, $3kV$, $6kV$, $12kV$, $18kV$, $24kV$ or $30kV$. On the other hand, for HVDC and LVDC power grids, both the International Electrotechnical Commission (IEC) and IEEE have established several standards and regulations [9, 10, 11]. According to IEC 60038, the LVDC is defined up to $1.5kV$, which leads to a "grey" zone for voltage levels between $1kV$ to $1.5kV$ taking into consideration the IEEE standard 1709-2010 as mentioned above. Therefore, a common standardization handbook regarding the division among LVDC, MVDC and HVDC is clearly lacking.

2.1.1 Potential applications of LVDC and MVDC power grids

The integration of renewable energy sources to the grid can be eased by utilizing DC power due to the nature of these sources. For example, photovoltaic (PV) panels generate DC power leading to the need for developing DC collection grids instead of the current trend of AC counterparts [12]. On top of that, there are plenty of other onshore and offshore applications that can be eased by using DC distribution grids as they can be seen in Fig. 2.1. Both LVDC and MVDC concepts can be used in all these applications depending always on the power and voltage requirements of each case.

Offshore wind power can benefit from utilizing DC grids instead of AC counterparts, achieving higher efficiency [13], as well as minimizing the required equip-

ment (i.e. power converters and high-frequency transformers) compared to the bulky low-frequency transformers used in AC systems [14, 15]. In addition to that, electric ships can be electrified with LVDC or MVDC distribution systems [8, 16, 17]. The advantages will be higher fuel efficiency, lower weight, minimized footprint of the electric equipment, as well as higher control flexibility in comparison with electric vessels electrified with LVAC or MVAC power grids [18]. As mentioned before, a framework related to the on board power distribution of the future electric vessels based on MVDC system has been already established [8], paving the way for further electric ships development.

A microgrid is defined as a grid-connected power cluster of distributed generation, energy storage systems and loads integrated into a unity. LVDC and MVDC microgrids are currently trend solutions to several applications and they are advantageous over AC counterparts in terms of efficiency and mostly of simply integration of various energy sources [19, 20]. Moreover, electric transportation can also benefit from DC electrification. In particular, electric trains could potentially increase their performance by minimizing the power losses associated with the conversion stages, as well as with the lines/cables by utilizing DC supply instead of the state-of-the-art AC. In [21], a comparison between AC and DC electrification of a railway revealed that at elevated power, i.e. $10MW$ with voltage rating at $10kV$, the DC case exhibits better performance compared to AC counterparts.

Besides these, LVDC and MVDC distribution grids might be beneficial for electrification of subsea loads. The main advantages of such grids over AC counterparts are the lower losses of the power distribution, and the smaller weight and thus lower cost of the required cables [22] in DC transmission. An example of an MVDC power distribution for subsea application is given in [23]. Specifically, the considered distribution grid exhibits an efficiency of 90% at power and voltage ratings of $20kW$ and $10kV$ respectively. Additionally, another subsea application electrified with DC voltage at $4.6kV$ is presented in [24], emphasizing on the design of a Modular Multilevel Converter (MMC) aiming at reduced number of active switches, as well as reduced cost.

Data centers have gained great attention in the last decades due to the increased demand of data processing and storage [25]. In addition to that, in [26] an entirely underwater server farm is investigated, revealing the increased popularity of data centers. Although both AC and DC power grids have been considered for the electrification of the loads in data centers, only the latter one seems more promising solution for achieving higher efficiencies [27, 28] minimizing the required conversion stages.

In [17], a potential connection of offshore wind farm with oil-drilling operations

supplied by MVDC distribution grid is suggested. Besides the technical benefits of DC grids that have been mentioned several times before, this idea of integrated wind power and oil and gas rigs, may lead to new business opportunities, not only for the oil companies, but also for the grid operators.

Several other applications that an electrification through LVDC and MVDC power distribution systems would offer various advantages compared to AC counterparts are DC homes [29], university campuses [30] and mine sites [31]. Last but not least, an increase of electrification in aviation application has been shown during the last years [32, 33, 34]. Towards the direction of all electric aircraft, the future on board DC distribution systems seem to gain more attention than the corresponding AC systems due to mostly the presence of high energy density batteries and fuel cells which operate with DC power [34]. The voltage level of such a system can vary between $500V$ up to $4kV$ depending on the percentage of electrification of the aircraft, as well as the size of it. Lastly, in [33], a comparative study for a $3kV$ and $20MW$ aircraft powered by either AC or DC voltage is presented. The DC case exhibited higher efficiency, as well as it lowered the total weight of the propulsion system, power supply system, protection and distribution system compared to AC case.

2.2 Short-circuit current in DC grids

For a better understanding of the short-circuits in DC lines, the simplified DC grid depicted in Fig. 2.2 will be considered and analyzed. It includes an ideal DC voltage source, V_{DC}, connected in series with a resistive load, R_{load}. Additionally, a certain line impedance, consisting of a resistive part, R_{line} and an inductive part, L_{line} represent the line modelling. Prior the fault incident, the line current, i_{line} flows from the source to the load. Assuming constant load and that the line resistance is significantly lower than the load resistance (i.e. $R_{load} >> R_{line}$), the line current will be constant and be given by the following equation.

$$I_{line} = \frac{V_{DC}}{R_{load}} \tag{2.1}$$

Assuming now that a short-circuit occurs as seen in Fig. 2.2. The line current will exponentially start increasing according to the following expression.

$$i_{line(t)} = \frac{V_{DC}}{R_{line}} + (\frac{V_{DC}}{R_{load}} - \frac{V_{DC}}{R_{line}})e^{-\frac{R_{line}}{L_{line}}t} \tag{2.2}$$

It can be seen from this equation that the rise of the fault current depends on the line impedance. The line resistance relies mostly on the line length and it is inverse

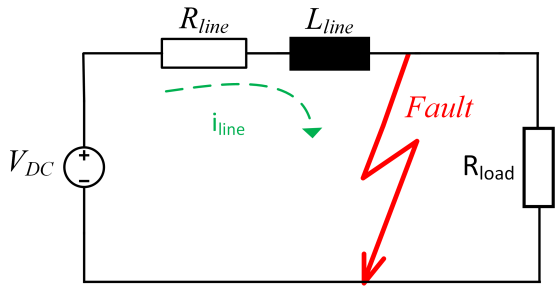


Figure 2.2: A simplified DC grid when a short-circuit incident occurs.

proportional to its cross section area, which eventually is related to the load current. The higher the line resistance is, the higher the power losses caused in the line. A minimum value for it is therefore required, keeping the cross section area of the line within some acceptable limits (including cost, weight). On the other hand, the line inductance which normally dominates in DC grids, can play a significant role for the short-circuit current increase in these grids. By keeping only the line inductance, L_{line} and neglecting the line resistance R_{line}, the fault line current will be given according to the following formula.

$$\frac{di_{line(t)}}{dt} = \frac{V_{DC}}{L_{line}} => i_{line(t)} = I_{line} + \frac{V_{DC}}{L_{line}}t \tag{2.3}$$

In contrast with the AC counterparts, the line inductance in DC systems is normally very low due to the absence of low frequency transformers and hence absence of their leakage inductances. Additionally, the anticipated short lines in LVDC and MVDC distribution systems will also lead to lower line inductances compared to long lines in HVDC systems. Therefore, according to (2.3), it is apparent that the short-circuit current in an LVDC or MVDC grid can reach significantly high values in a very short time due to the inherent low line inductances. As a result, current limiting inductors are installed in DC lines, providing smoother short-circuit current rise.

2.2.1 Protection strategies in DC grids

A protection scheme against short-circuits in an AC power grid utilizes mechanical breakers. Although the breaker opens the contacts when a fault is detected, the fault is not cleared immediately. An electric arc will develop between the two contacts and the fault current will keep flowing. However, due to the alternating nature of the current in these grids, after some milliseconds, the short-circuit current eventually will cross the zero point. During that time instant, the electric

arc between the two contacts of the breaker extinguishes. Thus, the short-circuit current is interrupted and the fault is cleared.

On the contrary, a short-circuit current in a DC grid never crosses the zero point. Thus, mechanical breakers cannot clear such faults. Although several other protection methods have been proposed in literature [35], *a lack of an efficient and cost effective protection device against short-circuits especially in LVDC and MVDC grids is identified.* Today, two different approaches can be applied in DC systems when a fault occurs, namely, power converter-based protection and protection based on circuit breakers. In the first approach, the power converters which are connected to the DC grid protect the system by isolating and clearing the fault. Such converters are, DC/DC boost converters, dual active bridge (DAB) converters, thyristor-based rectifiers, MMC with full bridge etc. However, when power converters which do not have current interruption capability are connected to a DC grid, then circuit breakers must be used for the grid protection. Although the first approach does not require additional components, it suffers from selectivity since it disconnects the entire DC grid connected through the converter. For instance, when a multi-terminal DC grid is considered, a potential fault in the DC line would disconnect the entire grid if a converter-based protection scheme would be implemented. On the other hand, a coordination between circuit breakers can provide selectivity, isolating only the faulted part of the system, at a cost of higher investment cost, as well as increase of the conduction power losses caused in the breaker. Further analysis on circuit breakers will follow in the next Subsection.

A. Protection devices for HVDC grids

Today, a feasible protection solution against short-circuits for HVDC grids is the use of the mature technology of mechanical breakers similar to AC grids. They are connected in both AC sides that the HVDC system is connected to, and hence, they can clear and isolate a short-circuit in the HVDC line. In addition to the high line inductances associated with the long power lines in a HVDC system, bulky reactors are connected to the DC line in order to limit the fault current rise. Furthermore, ABB has recently commercialized a hybrid HVDC circuit breaker [36]. The latter can be a feasible solution especially when multi-terminal HVDC systems are considered, leading to a required protection selectivity.

B. Protection devices for LVDC and MVDC grids

The protection devices connected in LVDC and MVDC grids differ significantly compared to HVDC counterparts. The main reason is the different protection requirements for each case. The space requirement for HVDC applications is not normally restricted, and thus bulky reactors can be used to limit the anticipated

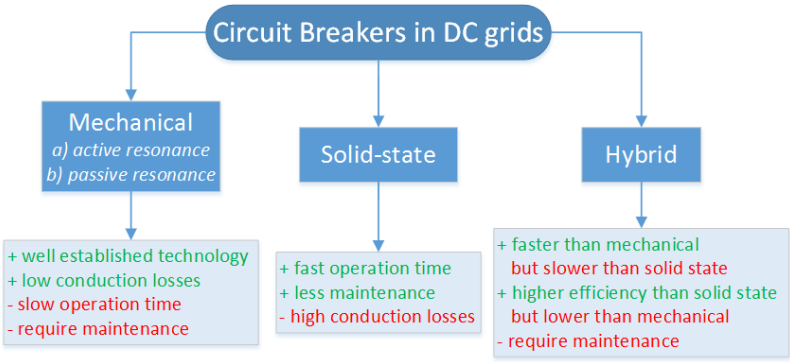


Figure 2.3: The advantages and disadvantages of the three DC circuit breaker types.

fault currents. On the other hand, several LVDC and MVDC applications are utilizing short power lines, as well as they require compactness. Therefore, in such an application, not only the use of bulky reactors becomes impractical, but also the short lines will cause high short-circuit currents in a very short time. *The absence of AC sides in these applications along with the rapid increase of the fault current impose the development of DC circuit breakers capable to interrupt the fault current quickly, before it becomes very high and catastrophic for the equipment.* Finally, several multi-terminal LVDC and MVDC power grids (mostly MVDC) are anticipated to be designed and operate in the near future. Thus, *a protection scheme based on coordination of DC circuit breakers and not on power converters should be considered for providing selectivity, isolating only the faulted lines.*

2.3 Circuit breakers for LVDC and MVDC grids

Several DC breaker concepts have been proposed in literature. They can be categorized into three types as shown in Fig. 2.3; (i) mechanical breakers with either active or passive resonance circuit, (ii) solid-state breakers, and (iii) hybrid breakers. The first type exhibits the highest efficiency by minimizing the conduction losses due to the low Ohmic part of the mechanical breaker. However, the high demand for maintenance, as well as the long fault clearance times are the main drawbacks of this breaker. On the other hand, the solid-state breaker achieves the fastest operation time at a cost of high power losses, which are associated with the power semiconductor devices. A further analysis on the various semiconductor technologies than can be employed in such a breaker will follow in Chapter 3. Finally, the hybrid DC circuit breaker is an intermediate solution, which provides shorter fault clearance times compared to mechanical counterparts, and also lower losses compared to solid-state breakers. The main advantages and disadvantages of the three DC circuit breaker types are summarized in Fig. 2.3.

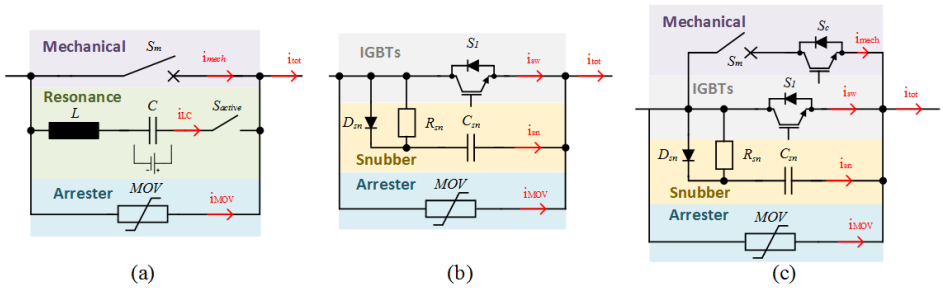


Figure 2.4: Schematic diagrams of the main DC circuit breaker types: (a) mechanical breaker with active resonance, (b) solid-state circuit breaker, and (c) hybrid breaker.

2.3.1 Mechanical breakers with resonance circuit

The successful fault clearance in a mechanical breaker relies on the electric arc extinguishment when the fault current crosses the zero point. In a DC grid though, this does not happen naturally. An artificial zero crossing point should be created through a resonance circuit (or current injection circuit). Two types can be found, namely mechanical breaker with either passive or active resonance circuits. These types rely on an AC current injection from an LC circuit to the mechanical breaker which will eventually force the total current to cross zero. In case of the mechanical breaker with passive resonance, the LC tank is connected in parallel to the main breaker branch. Once a short-circuit occurs, the voltage rise across the breaker will activate the LC tank, and an oscillating current will be generated. However, this automatic current injection depends initially on the voltage rise across the mechanical breaker and the short-circuit current and therefore, a specific design of both inductor and capacitor in the LC tank must be considered. Additionally, the lack of an active trigger mechanism in the breaker makes this breaker less popular. On the contrary, an active switch can be connected in series with the LC tank and thus overcome the previous challenge. The latter breaker technology is called mechanical breaker with active resonance. A simple schematic diagram of such a breaker can be seen in Fig. 2.4(a). The LC tank is controlled by the active switch, S_{active}, (e.g. thyristors) and the capacitor must be pre-charged through an external circuit (not shown in Fig. 2.4(a)). Once a fault occurs, S_{active} is activated, and the generated oscillating current by the LC branch, i_{LC}, is added to the fault line current i_{tot}. This creates the required zero current crossings for the current that flows through the mechanical breaker i_{mech}. Then, the mechanical breaker is able to extinguish the generated arc and interrupt the fault current. Finally, an MOV (or surge arrester) should also be connected in parallel to the main breaker branch as shown in Fig. 2.4(a). The purpose is to suppress the overvoltage across the breaker when this exceeds a certain voltage limit, as well as to absorb the energy stored in the inductive elements of the DC line.

2.3.2 Solid-state DC circuit breakers

Several solid-state breaker topologies employing power semiconductors can be found in literature. They can be categorized into two groups: (i) self-triggered solid-state breakers and, (ii) externally triggered. In the first category, the utilized power semiconductor devices are mostly thyristors and/or JFETs. A typical example of such a breaker is the Z-source solid-state breaker [37]. A self-triggered breaker concept based on JFETs is also proposed in this thesis (given in Chapter 6). **A more detailed analysis on the various semiconductor technologies that can be utilized in a solid-state breaker will follow in Chapter 3.** The majority of solid-state breakers that have been proposed by various researchers is externally triggered. Among others, it is a typical interrupting topology as shown in Fig. 2.4(b), which will be the main focus of this thesis.

The interrupting breaker consists of three branches, namely, active switch branch, snubber circuit branch, and MOV branch. In this analysis, IGBTs have been considered as active switches, while RCD snubber circuits provide a controlled voltage increase across the devices. The operating principle of such a breaker is as follow. The IGBTs carry the line current under normal operation. Once a short-circuit occurs, the line current, i_{tot} increases and a fault detection circuit gives a command to the IGBTs to turn-OFF. The line current is then commutated from the IGBTs to the snubber circuit. Finally, similar to the mechanical breaker, an MOV should be connected in parallel to the main branch in order to provide overvoltage protection and to dissipate the magnetic energy stored in the DC line. **A further analysis on different overvoltage suppression configurations employed in solid-state DC breakers, as well as their operating principles will be presented in Chapter 4.**

2.3.3 Hybrid DC circuit breakers

A basic hybrid breaker type includes four branches as shown in Fig. 2.4(c). A low-voltage active switch (e.g. IGBTs) is connected in series with a mechanical breaker in the conduction branch, while the other three branches are similar to the solid-state breaker. When a fault occurs, the mechanical breaker starts to separate its contacts. Once the Ohmic resistance of the mechanical breaker reaches a certain value, the low-voltage switches turn-OFF. At the same time, the main IGBTs have been turned-ON. Thus, the fault current is forced to flow through these IGBTs, which are responsible for the short-circuit current interruption. The last operating stages of a hybrid breaker are identical to a solid-state breaker.

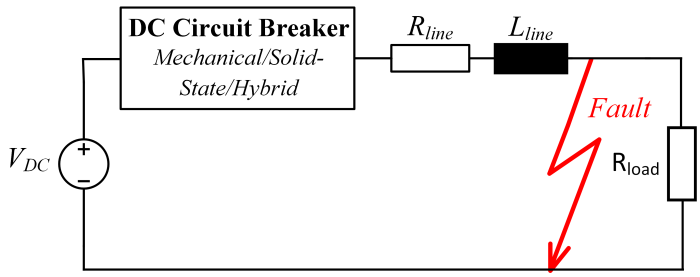


Figure 2.5: Modelling of a simplified MVDC grid with circuit breakers.

2.4 Comparative study among mechanical breaker with active resonance circuit, solid-state breaker and hybrid breaker

A simplified MVDC grid (Fig. 2.5) along with the three investigated breaker types have been modelled using Matlab/Simulink. The grid parameters, namely the line resistance and inductance prior the fault position, are set to $R_{line} = 0\Omega$ and $L_{line} = 1mH$ respectively. A constant DC voltage source has been considered for the grid modelling and a constant resistance for the load. They are set to $V_{DC} = 15kV$ and $R_{load} = 10\Omega$, which lead to a nominal load current of $1.5kA$. The clamping voltage of the MOV has been set to 50% higher than the DC voltage of the grid. A pole-to-pole short-circuit occurs at the time instant $t_{sc} = 100msec$. When the fault current exceeds 2 times the nominal value (i.e. $3kA$) the circuit breaker is triggered.

A. Modelling and simulation results of the mechanical breaker with active resonance circuit

A short analysis on the operating principle of a mechanical breaker with active current injection has been presented earlier. The modelled DC grid is shown in Fig. 2.5, and the mechanical breaker is illustrated in Fig. 2.4(a). The ON-state resistance of the mechanical switch is set to $0.1m\Omega$. The resonant frequency of the LC tank has been chosen to be $500Hz$, and the capacitor is pre-charged at $5kV$ taking into account both the short-circuit current rise and the DC voltage. The inductance is set to $L = 4.29\mu H$ and the capacitor value was calculated to be $C = 23.3mF$. Based on these two values, the injected current from the LC tank (i_{LC}) to the mechanical breaker will force the total current ($i_{tot} = i_{LC} + i_{mech}$) to cross the zero point at least three times in order the fault current to be safely interrupted. If the current rise slope is relatively high, the developed electric arc may be maintained at the first zero crossing point. Therefore, it is recommended that this type of breaker is designed in such a way, that the fault current crosses

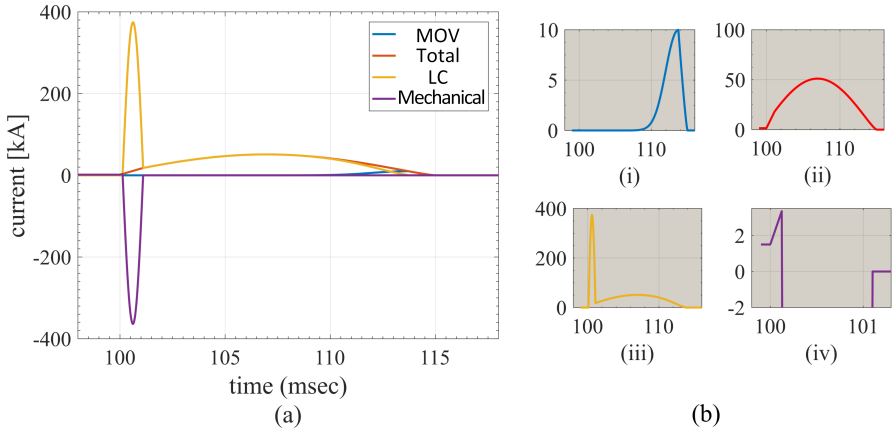


Figure 2.6: Simulation results of: (a) the MOV current (blue line), fault line current (red line), LC tank current (yellow line) and mechanical current (purple line) in a breaking operation when mechanical breaker with active resonance circuit is employed in a $15kV_{DC}$ grid, and (b) the corresponding magnified values.

zero more than one time. It should also be mentioned that the Cassie arc model has been used for the modelling of the developed arc in the mechanical breaker [38].

The simulation results are shown in Fig. 2.6. In particular, the currents that flow through the line, the mechanical breaker, the LC tank, and the MOV during a short-circuit incident are illustrated. Fig. 2.6(b) shows the same currents, but magnified. Fig. 2.6(b.iv) reveals that that the mechanical breaker current i_{mech} crosses zero twice before it is interrupted. Additionally, the peak short-circuit current that flows through the DC power line (marked with red line in Fig. 2.6) reaches almost $50kA$, and it is interrupted after approximately $15msec$. The excessive line current leads to the need for over-dimensioning the whole electrical equipment which is connected to the DC system (e.g. VSCs, DC/DC converters) in order to avoid severe damages.

B. Modelling and simulation results of the solid-state circuit breaker

The next investigated breaker type is the interrupting solid-state DC breaker as it can be seen in Fig. 2.4(b). Five series-connected IGBTs rated at $4.5kV$ and $3kA$ [39] are considered in order the breaker to withstand the MVDC voltage level. Besides that, the passive components of the RCD snubber circuits, which are parallel-connected to every IGBT have been calculated to be $C_{sn} = 25\mu F$ and $R_{sn} = 5\Omega$. *This breaker type is the main focus of this thesis, and therefore, a more detailed analysis follows in the next Chapters. A brief introduction to solid-state breakers and their beneficial performance over other type of breakers is the main focus of this part of the thesis.*

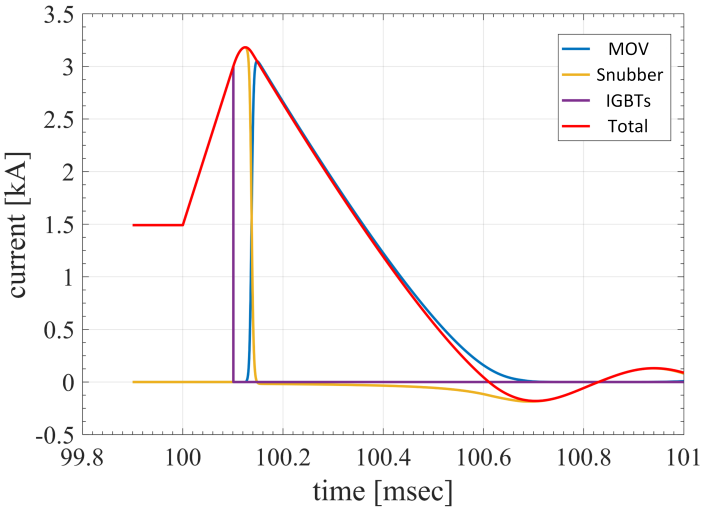


Figure 2.7: Simulation results of the MOV current (blue line), snubber current (yellow line), IGBTs current (purple line) and fault line current (red line) in a breaking operation when solid-state breaker is employed in a $15kV_{DC}$ grid.

The performance of a solid-state breaker clearing a short-circuit current in a $15kV$ DC system is shown in Fig. 2.7. The current commutation in the various branches can be clearly observed. Initially, the line current i_{tot} equals the IGBT current i_{sw}. When the fault current reaches $3kA$, a command is given to the IGBTs to turn-OFF. At that point, the current is commutated from the IGBTs to the snubber capacitors through the snubber diodes (i_{sn} with yellow line in Fig. 2.7). Then, the fault current keeps rising by charging the snubber capacitors until their voltages reach the clamping voltage of the MOV. The peak fault line current reaches $3.2kA$ at that point, then it is commutated to the MOV branch (i.e. i_{MOV}) and it starts decreasing. The fault is finally cleared after approximately $0.6msec$.

C. Modelling and simulation results of the hybrid circuit breaker

Fig. 2.8 illustrates a short-circuit clearance in the considered MVDC grid by using a typical hybrid DC breaker (Fig. 2.4(c)). Initially, the fault current flows through the mechanical breaker i_{mech}, and once it reaches the threshold value, i.e. $3kA$, a command is given to it to start the contact separation. At the same time, the main IGBTs turn-ON. Then, after approximately $1msec$, the Ohmic resistance between the two contacts becomes sufficiently high, and the low-voltage switch turns-OFF. This forces the current to be commutated to the main IGBTs as shown with yellow line in Fig. 2.8. At that point, the fault current reaches $17.5kA$ and a few microseconds later, it is commutated to the snubber capacitors similar to

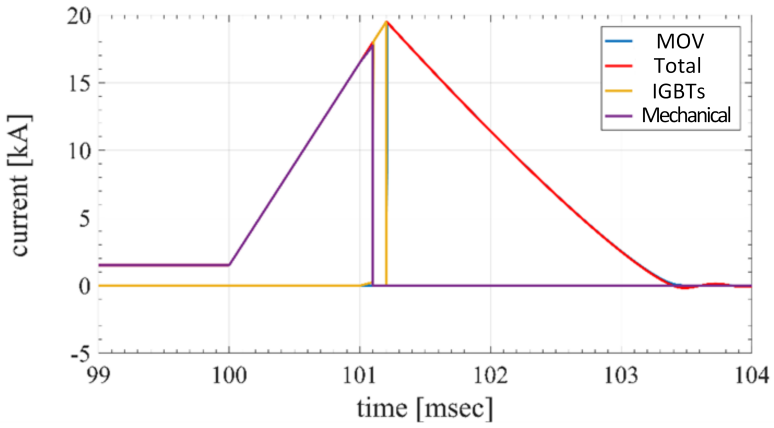


Figure 2.8: Simulation results of the MOV current (blue line), fault line current (red line), IGBTs current (yellow line) and mechanical breaker current (purple line) in a breaking operation when hybrid breaker is employed in a $15kV_{DC}$ grid.

the solid-state breaker operation. The snubber capacitors are being charged for approximately $0.2msec$ causing the fault current to reach a peak value of almost $20kA$. Then, the MOV is activated and the fault current flows through it as shown in Fig. 2.8 with blue line. Finally, the fault is fully cleared in less than $3.5msec$.

D. Performance comparison of the three DC circuit breakers

In this part of the thesis, a performance comparison among the three DC circuit breaker types during a short-circuit clearance is presented. The evaluated criteria are; (i) the peak fault line current, $I_{faul,peak}$, (ii) the short-circuit clearance time, t_{cl}, (iii) the energy dissipation of the MOV, E_{dis} and, (iv) the conduction losses, P_l of each breaker during nominal operation.

Firstly, Fig. 2.9 shows the short-circuit current and the voltage across each breaker during a short-circuit clearance process. It can be seen that the mechanical breaker exhibits the highest fault current and requires the longest time to clear the fault compared to the other two breakers. The numerical values for the peak fault line currents and the short-circuit clearance times are summarized in Table 2.1. In addition, Fig. 2.9(b) shows that the voltages across each breaker are clamped approximately at the same values due to the presence of the MOV. The residual energy dissipation of the MOV in each breaker can also be seen in Table 2.1. This energy becomes the lowest when solid-state breakers are used, which also means that the design of the MOV has the lowest requirements in such a breaker. On the other hand, Table 2.1 reveals that the solid-state breaker exhibits the highest conduction losses caused in the power semiconductor devices. In particular, the

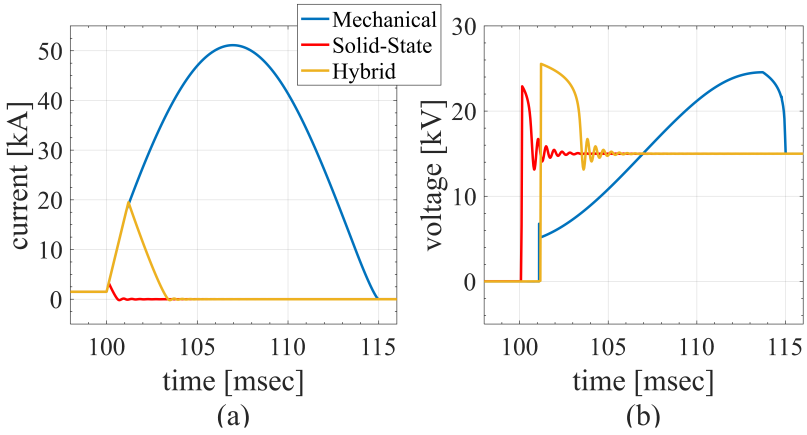


Figure 2.9: Performance comparison of the three investigated breaker types during a short-circuit clearance process with respect to: (a) short-circuit current, and (b) transient voltage across each breaker.

conduction losses in such a breaker are hundred times higher compared to the mechanical breaker losses, and almost four times higher compared to the hybrid breaker. Besides the low-efficiency, the requirements for better cooling systems also becomes critical in case of solid-state breakers.

2.4.1 Impact of the short-circuit current on the design of VSCs

In the previous study, an ideal voltage source was considered for the DC grid modelling. However, in several actual applications, DC grids will interface with AC grids via VSCs. In such hybrid grids, two protection strategies against short-circuits in the DC lines can be applied; (i) use of mechanical breakers connected to the AC side, and (ii) use of DC breakers connected to the DC lines. These strategies are illustrated in Fig. 2.10. In this study, solid-state DC breakers have been considered for the DC breakers in the second strategy.

Table 2.1: Summary of the performance comparison of the three investigated breakers

Circuit breaker type	$I_{fault,peak}$ $[kA]$	t_{cl} $[msec]$	E_{dis} $[kJ]$	P_l $[kW]$
Mechanical with active resonance circuit	51.1	15	645	0.23
Solid-state	3.18	0.6	1.4	30
Hybrid	19.5	3.4	246	8.3

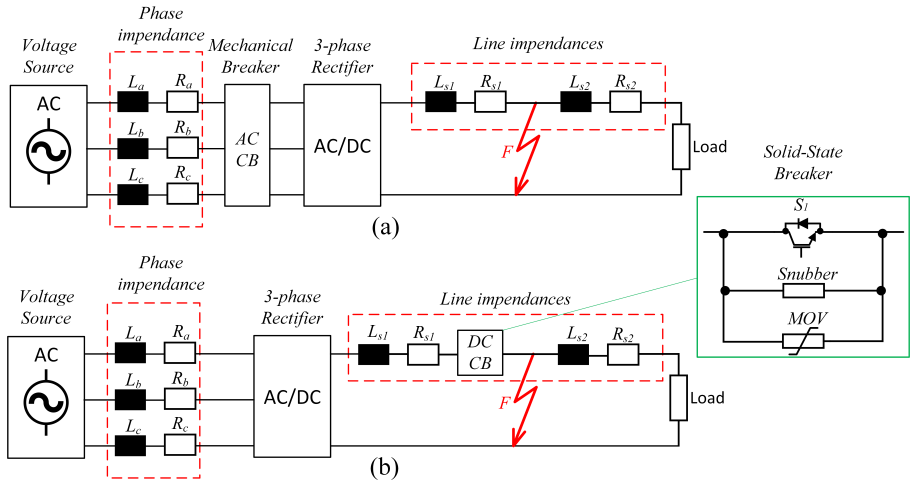


Figure 2.10: Schematic diagrams of the two DC grid configurations under study: (a) protection using an AC circuit breaker on the AC side, and (b) protection using a solid-state DC breaker on the DC side.

Four VSCs have been considered for the AC/DC conversion which are shown in Fig. 2.11. In particular, a two-level VSC, a three-level Neutral-Point Clamped (NPC) converter, an Modular Multilevel Converter with half bridge sub-modules (MMC-HB), and an Modular Multilevel Converter with full bridge sub-modules (MMC-FB). The first three topologies employ antiparallel diodes at each switch position, and thus, if a short-circuit occurs in the DC line, the fault current will flow through these diodes even if the switches turn-OFF, and eventually stress them. This leads to the need for overdimensioning these diodes in order to avoid extensive thermal stress. The MMC-FB topology utilizes antiparallel diodes similar to the other topologies as seen in Fig. 2.11(c.ii), but if the controlled switches turn-OFF, there will be no path for the fault current through the diodes. Therefore, in this VSC topology, the use of circuit breakers is not necessary. The evaluation criteria in this study are the peak short-circuit line current and the fault clearance times, as well as the current and thermal stress of the antiparallel diodes employed in VSCs.

Simulation results

Fig. 2.10 shows the two grids that have been modelled. The grid parameters are given in Table 2.2. Three VSC topologies have been considered by employing either mechanical breakers connected to AC side or DC solid-state breakers, and for the fourth VSC topology, i.e. MMC-FB, a breakerless grid was considered.

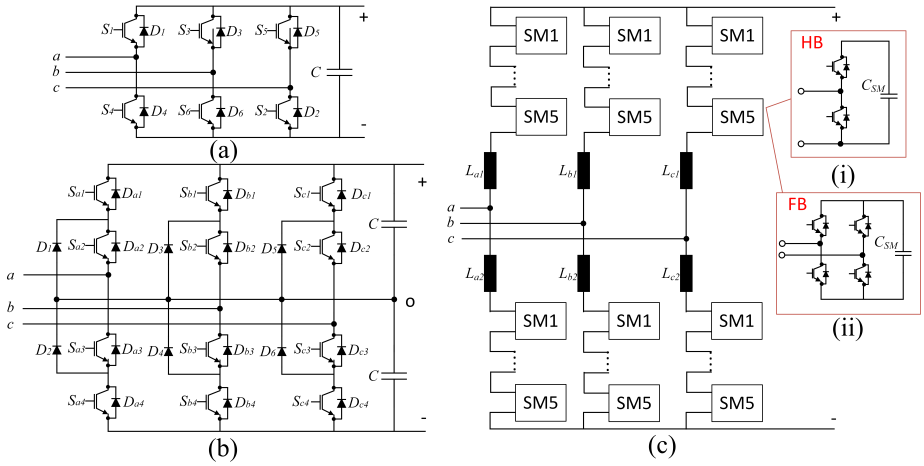


Figure 2.11: Schematic diagrams of the basic types of active rectifiers: (a) 2-level VSC, (b) 3-level NPC and (c) MMC consisting of (i) HBs and (ii) FBs.

For the two MMC-based topologies, five Sub-modules (SM) have been used. Both the mechanical and the solid-state breakers have been designed according to the analysis presented in Subsection 2.3.

The simulation results when a short-circuit is cleared using mechanical breakers in AC side or solid-state DC circuit breakers are summarized in Tables 2.3 and 2.4. It can be seen that the mechanical breakers exhibit a slower operation than the solid-state breakers causing extremely higher short-circuit currents that flow through the antiparallel diodes. In particular, when a 2-level VSC is employed for the AC/DC connection and mechanical breaker is considered, the fault line current reaches $140kA$, it is cleared within $28msec$ and the diode current becomes $35.3kA$. On the other hand, when a solid-state breaker is connected in the DC lines, the peak

Table 2.2: Parameters of the investigated hybrid grid

Parameter	Symbol	Value	unit
AC Voltage - Line to Line RMS value	V_{LL}	12.25	kV
DC voltage	V_{DC}	15	kV
Phase inductance	$L_{a,b,c}$	3.255	mH
Phase resistance	$R_{a,b,c}$	3	$m\Omega$
Line inductances prior and beyond the fault point	$L_{s1,s2}$	0.174	mH
Line resistance prior and beyond the fault point	$R_{s1,s2}$	45	$m\Omega$
Load	P_L	22.5	MW
Threshold current for fault detection	I_{th}	3	kA

fault line current equals $3.9kA$, and the antiparallel diodes carry a significantly lower current, i.e. $1.58kA$. The thermal stress of the diodes which is given by the load integral of the diodes current, is also minimized in the solid-state breaker-based protection approach as shown in Tables 2.3 and 2.4. Similar results for the two approaches can be observed when a 3-level NPC topology is considered for the AC/DC connection.

A MMC-HB topology includes several capacitors (one capacitor per SM as shown in Fig. 2.11(c.i)). When a short-circuit occurs, all the controllable switches turn-OFF, and hence the fault current fed by the AC voltage source will flow through the antiparallel diodes. The latter leads to low short-circuit current rise and hence, the use of the slow mechanical breakers in AC side is becoming less problematic. Specifically, Table 2.3 shows that the peak fault line current reaches $4.6kA$, the current through the diodes is $3.2kA$, their load integral becomes $0.32kA^2sec$ at a cost of long fault clearance time, i.e. $758msec$. On the other hand, the use of a solid-state DC breaker reduces these values even more. In particular, the peak fault current is approximately $3kA$, the diodes are stressed with $2.6kA$ and thermally with $0.02kA^2sec$ while the fault current is interrupted within $5.3msec$ (Table 2.4).

Last but not least, if the MMC-FB topology is used to interface AC to DC grids, a breakerless protection against short-circuits can be applied. That means the converter will turn-OFF all the switches and therefore, there will be no current path to feed the faulty point. The peak short-circuit current reaches $3kA$, which is the threshold current for fault detection, the current that flows through the diodes is $2.6kA$, and the short-circuit is cleared in $3.7msec$. On the other hand, the full bridge configuration requires twice the number of switches compared to half bridge counterparts, and therefore, it is more costly. This approach also suffers from selectivity as it has been already mentioned previously, and thus, it is not always feasible.

Table 2.3: Simulation results during a short-circuit in the DC line in case of using mechanical breakers in AC side for the fault clearance

VSC type	Peak short-circuit line current $[kA]$	Clearance time $[msec]$	Peak diodes current $[kA]$	Load integral of diodes $[kA^2sec]$
2-level VSC	140.1	27.97	35.3	2.6
3-level NPC	140.1	27.35	35.43	2.6
MMC-HB	4.63	758	3.21	0.32
MMC-FB*	3	3.7	2.62	0.01

* breakerless

Table 2.4: Simulation results during a short-circuit in the DC line in case of using solid-state DC circuit breakers for the fault clearance

VSC type	Peak short-circuit line current $[kA]$	Clearance time $[msec]$	Peak diodes current $[kA]$	Load integral of diodes $[kA^2sec]$
2-level VSC	3.91	0.152	1.58	0.01
3-level NPC	3.91	0.152	1.58	0.01
MMC-HB	3.01	5.3	2.63	0.02
MMC-FB*	3	3.7	2.62	0.01

* breakerless

2.5 Conclusions

This Chapter presented the protection challenges against short-circuits occurring in the emerging technology of LVDC and MVDC power grids. Several application areas utilizing such grids have been identified and presented. The operating principles of three major DC circuit breaker concepts have also been discussed. A typical mechanical breaker with an active resonance circuit LC, a solid-state breaker, and a hybrid breaker have been analyzed in depth. A short-circuit incident in a $15kV$ DC grid has been modelled and simulated by means of Matlab/Simulink. All three investigated breakers have been evaluated not only on the fault clearing performance, but also on their conducting performance. The superior performance of the solid-state breakers exhibiting the lowest peak short-circuit current and the shortest fault clearance time has been shown. On the other hand, the high conduction losses caused in the high-power semiconductor devices used in a solid-state breaker has also been revealed.

Last but not least, the impact of a short-circuit current in a DC line on the current and thermal stress of antiparallel diodes found in four VSCs has been investigated. The simulations showed that the diodes' stress is minimized in case of a 2-level VSC, a 3-level NPC converter and a MMC-HB converter when solid-state breakers are used. In addition, a breakerless protection strategy based on MMC-FB converters was also studied. In that case, the converter can turn-OFF and interrupt the short-circuit current before the latter becomes high enough. However, this VSC topology requires a large number of switches compared to other topologies, as well as it suffers from selectivity. This means that it cannot isolate only the faulty line, but it de-energizes all the power lines that are connected to that when a fault occurs. This is not feasible when multi-terminal power grids need to be considered.

Based on the findings of this Chapter, the solid-state breakers seem the most promising solution for the protection of LVDC and MVDC grids. The design and operating challenges of those breakers will therefore be tackled in this PhD thesis.

Chapter 3

Power semiconductor devices for solid-state DC breakers

This Chapter presents the various commercially available power semiconductor technologies that can be used in solid-state circuit breakers for LVDC and MVDC applications. At first, a comparison among several Silicon and SiC semiconductor device technologies suitable for medium-power DC grids is presented. Experimental results are included in order to evaluate the conduction losses of the investigated semiconductors for various operating conditions. Additionally, a study on reducing the conduction losses caused in the power semiconductor devices by applying the maximum gate voltage is also experimentally presented. Lastly, a solid-state breaker connected to a high-power MVDC system is considered, and a performance evaluation of three semiconductor technologies in terms of conduction losses via simulations is given. This Chapter is based on papers [P4, P10].

Contributions

Several studies for evaluating and comparing different semiconductor devices have been presented in literature. However, the majority of these studies aims to evaluate the performance at switch-mode power converter applications [40, 41]. A lack of a comparative evaluation among different semiconductors employed in solid-state DC breakers is therefore identified [P4]. The first contribution of this Chapter is the experimental evaluation of several power semiconductor technologies that can be found commercially, in terms of conduction losses under two cases. Firstly, for a medium-power DC breaker design utilizing Silicon or SiC

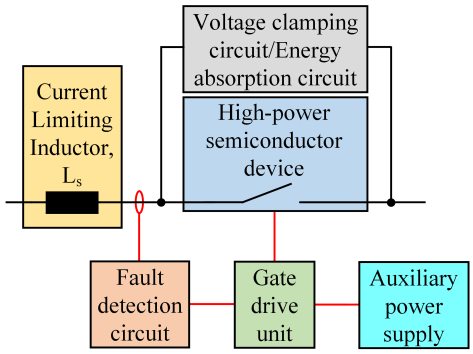


Figure 3.1: Block diagram showing the main components of a typical interrupting solid-state DC circuit breaker.

power semiconductor devices [P10] with blocking voltage in the range of $1200 - 1700V$. Secondly, for a high-power MVDC solid-state breaker design requiring high-voltage and high-power semiconductor modules or press-packs [P4]. The second contribution presented in this Chapter is the study of applying the maximum gate voltage in the semiconductors and its impact on the reduction of the conduction losses [P10].

3.1 Background

Fig. 3.1 shows a typical structure of an interrupting solid-state DC circuit breaker comprising a current limiting inductor, L_s, power semiconductor devices, as well as voltage clamping circuits and energy absorption circuits. In addition, auxiliary circuits for fault detection, as well as for supplying the required power to the gate of the semiconductor devices are also required.

Several challenges may arise when designing a solid-state DC breaker with respect to these key components. Firstly, the choice of the power semiconductor devices is crucial. As mentioned earlier, the today's barrier for the development of solid-state DC breakers is mostly related to the high conduction losses in the semiconductor devices. Therefore, these losses must be minimized by choosing the proper semiconductor technology and chip area for a given current. Besides that, the design of an overvoltage suppression circuit for switch protection leads to various challenges as well. A comparative study on that has been presented in [P5] for DC grid voltages up to $1500V$, while in [42] a similar study was presented at a lower DC voltage, i.e. $400V$. Further analysis on that will follow in Chapter 4. Last but not least, design challenges may also arise in the Gate Drive Unit (GDU)s, as well as in the fault detection and trip electronic circuits [43].

The majority of the semiconductor industries manufacture high-voltage power semiconductor devices that are suitable for switch-mode power converters. Therefore, they aim not only to minimize the forward voltage drop of the semiconductors while keeping the same breakdown voltage capability, but also to achieve low switching losses at elevated switching frequencies. The latter though, is not critical when semiconductors are employed in solid-state breakers. On the contrary, the minimization of the forward voltage drop should be set as the main design goal for such an application.

3.1.1 Paradigm shift towards SiC-based power semiconductor devices

At high blocking voltage, and high current densities, semiconductor device technologies based on minority-carriers (bipolar devices) seem to achieve a better performance in terms of keeping low conduction losses compared to majority-carrier counterparts (unipolar devices). IGBTs, and thyristor-based power devices are among those semiconductor technologies that may be used for the design of the future solid-state DC circuit breakers not only due to their high efficiency but also due to their robustness. On the other hand, the SiC technology has already initiated a new era in the fabrication of majority-based semiconductor devices leading towards the development of switches with lower ON-state resistances compared to Silicon counterparts at the same voltage ratings. The advantageous material properties of SiC over Silicon are summarized in Table 3.1 [44].

In particular, the almost ten times higher critical electric field of SiC may push towards the development of single-chip switches operating at higher breakdown voltages compared to the today's state-of-the-art Silicon counterparts. The critical electric field determines the ionisation and avalanche breakdown of a device. The breakdown voltage on the other hand, relies on the critical electric field, as well as on the drift zone width, i.e. the main part of the device thickness. Therefore, by keeping the same drift thickness, a SiC-based device can operate at ten times

Table 3.1: Silicon vs SiC material properties

Parameter	Unit	Silicon	4H-SiC
Energy band-gap, E_g	eV	1.12	3.26
Intrinsic carrier concentration, n_i	cm_{-3}	$1.4 \cdot 10^{10}$	$8.2 \cdot 10^{-9}$
Critical electric field, E_{crit}	MV/cm	0.23	2.2
Electron mobility, μ_n	$cm^2/V \cdot s$	1400	950
Relative permittivity, ϵ_r	$-$	11.8	9.7
Thermal conductivity, λ	$W/cm \cdot K$	1.5	3.8
BFoM: $\epsilon_r \cdot \mu_n \cdot E_{crit}^3$	rel. to Si	1	500

higher voltage level. On top of that, the required doping in the drift zone becomes, according to Poisson equation, much higher compared to Silicon power devices [44]. Therefore, in majority-carrier devices where there is no conductivity modulation, the ON-state resistance can be seen as a function of the relative permittivity, electron mobility and critical electric field. The combination of these is given be the so called Baliga's figure of merit (BFoM) as it can be seen in Table 3.1. The BFoM for the SiC is 500 times the Silicon, which theoretically means that a SiC-based majority-carrier semiconductor device can be fabricated with the same chip size as a Silicon-based device, but operating at 500 higher breakdown voltage. However, this is only a theoretical value, but in reality other parameters, such as loss density and packaging of modules, play an important role to secure a reliable operation of semiconductor devices and thus, a much smaller factor should be finally considered. Additionally, the wider band-gap along with the low intrinsic carrier concentration of SiC can reduce significantly the leakage currents in devices fabricated by such a material. As a result, the SiC-based power devices can operate at higher temperatures. Lastly, the thermal conductivity is also higher for SiC compared to Silicon, leading to higher temperature endurance of SiC-based semiconductor devices.

It can, therefore, be clear that SiC-based power devices may be a suitable technology for the design of solid-state breakers in the near future. Besides the superior performance in terms of low forward voltage drop, the potential fabrication of SiC-based switches capable to operate at high breakdown voltages leads to the use of fewer series-connected devices for the development of MVDC solid-state circuit breakers. Thus, the design complexity can be reduced. Further analysis on the design challenges of series-connected devices will be presented in Chapter 5.

3.1.2 Desired characteristics of power devices employed in solid-state DC circuit breakers

Even if the SiC-based devices seem suitable candidates for realization of solid-state breakers, there is still a lack of a particular semiconductor device technology for such an application. In that case, the desired characteristics of these devices are the following.

1. **Maximum turn-OFF current capability**. Several high-power DC applications require semiconductor devices employed in breakers that are capable of carrying high currents under nominal operation, as well as to turn-OFF by the gate at even higher currents.

2. **Forward voltage drop**. The main challenge in the design of solid-state circuit breakers is the high conduction losses of the power semiconductors.

Therefore, a switch exhibiting minimized conduction losses would be a perfect candidate for a breaker realization.

3. **Heat dissipation capability**. The thermal performance of a semiconductor is generally crucial for every kind of applications and especially for breaker operations due to the anticipated high short-circuit currents [P3]. The power dissipation within the chip of a device operating at high current can be extremely high leading to device failures. Therefore, the thermal impedance of such a switch should be kept as low as possible in order to avoid thermal breakdowns. Except of the intrinsic thermal characteristics of a power device, the cooling system is also as a vital component of such a device. The proper cooling system design of a power semiconductor device allows it to operate at lower junction temperature and hence, the forward voltage can drop significantly considering a positive temperature coefficient.

4. **Robustness**. The word robustness of a power device includes several parameters. Among others, the immunity of the device to rapid change of both current during a short-circuit (di/dt) and voltage during the turn-OFF of the switch (dv/dt). In other words, the devices intended to be employed in breakers should be insusceptible to the anticipated high derivatives assuring a reliable operation. As an example, they should not be false triggered when a high dv/dt is applied across the device terminals. A feasible solution to that is the use of passive snubber circuits or advanced active gate drivers. Lastly, a well-designed device packaging which minimizes the stray inductances found within the module can also play an important role leading to increased robustness of the switch.

5. **Characteristics in series connection**. When a switch must withstand voltage levels higher than $4kV$ (e.g. MVDC grids), a series-connection of several devices is required. However, voltage imbalances among the series-connected devices may occur due to several reasons that are explained in detail in the Chapter 5. Therefore, a particular attention must be paid when designing these devices in order to ease their series-connection, such as device parameters spread.

6. **Characteristics in parallel connection**. MVDC applications may require high currents. However, if the needed current is higher that the maximum current that a device can supply to the load, then several devices must be parallel-connected in order to share the load current. The devices must have positive and possibly equal temperature coefficients, so they can evenly distribute the load current.

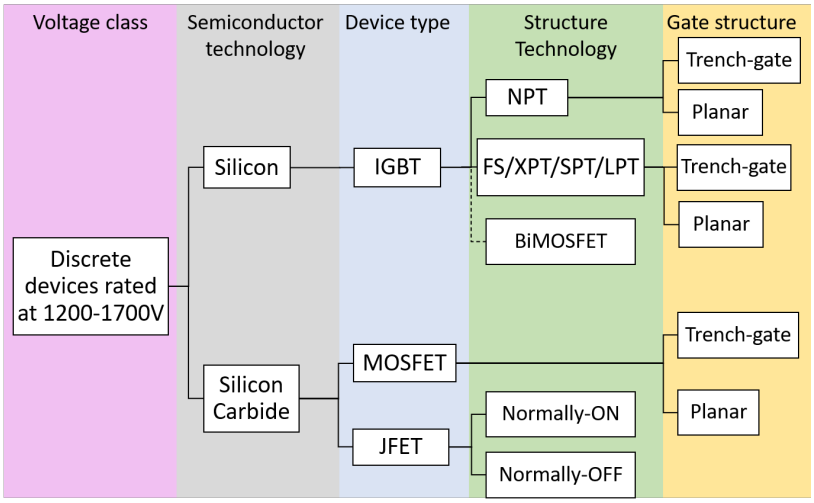


Figure 3.2: Commercially available Silicon and SiC power semiconductor device technologies in the voltage class of $1200 - 1700V$.

3.2 Silicon and SiC semiconductor device technologies for medium-power solid-state DC breakers

In this section, various Silicon and SiC semiconductor device technologies in the voltage classes of 1200 and $1700V$ are investigated. They are suitable for designing solid-state DC circuit breakers connected to power grids with maximum voltage ratings of $1200V$ when single devices are required. On the other hand, a series connection of multiple devices can lead to the design of breakers rated at much higher voltages than $1200V$. However, this would impose several design and operating challenges for the breaker. Further analysis on the series-connected devices follows in Chapter 5.

3.2.1 Commercially available Silicon and SiC power semiconductor device technologies in the voltage class of 1200-1700V

Several power semiconductor technologies can be found in market in the voltage range of $1200 - 1700V$. They are fabricated either with Silicon or SiC and they can be classified into two categories depending on the type of the charge carriers. Firstly, the bipolar or minority-carriers based devices and secondly, the unipolar or majority-carriers based devices. Each semiconductor category includes several devices' types. An overview of all these power semiconductor devices in the voltage class of $1200 - 1700V$ can be seen in Fig. 3.2. They are categor-

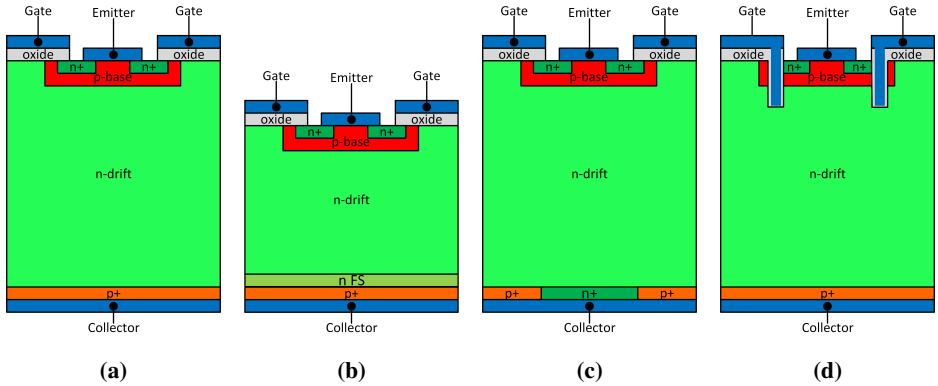


Figure 3.3: Typical Silicon IGBT structures: (a) NPT IGBT, (b) FS/XPT/SPT/LPT IGBT, (c) BiMOSFET, and (d) NPT IGBT with trench-gate.

ized based on the semiconductor material technology, the device type, the structure technology, as well as the gate structure. Three main device types have been identified, i.e. Silicon IGBT, SiC Metal-Oxide Semiconductor Field Effect Transistor (MOSFET) and SiC JFET. A short description of each type follows.

A. Silicon Insulated Gate Bipolar Transistors

IGBTs have gained momentum compared to other semiconductor devices. Several reasons have led towards their popularity, such as their ruggedness at high blocking voltages [45]. Several Silicon IGBT structures can be identified in semiconductor market. Firstly, the Punch-Through (PT) IGBT, which is fabricated by creating an n-epitaxial drift layer and a thin high-doped n+ buffer layer on top of a thick high-doped p+ substrate. However, they can be only found at low blocking voltage, and since the focus of this Chapter is on devices rated at $1200 - 1700V$, they will not be investigated further. Another IGBT-based device is the Non-Punch-Through (NPT) IGBT. The typical structure of such a device is illustrated in Fig. 3.3(a). In contrast to a PT device, the NPT IGBT structure has a thinner p+ substrate, as well as a thicker n-epitaxial drift layer and thus, it can withstand higher blocking voltages. Additionally, the n+ buffer layer has been removed. Moreover, it can achieve better switching performance compared to PT IGBT counterparts, minimizing the switching losses [45]. The next IGBT-based structure is the Field-Stop (FS) IGBT. A typical structure of such a device is depicted in Fig. 3.3(b). Two main difference can be seen compared to NPT counterparts. Firstly, the thinner drift region, which leads to lower ON-state resistance, and secondly, the use of an additional thin n- buffer layer on top of the p+ substrate. The latter leads to a trapezoidal electric field distribution within the drift region and hence, the forward

voltage drops significantly. It must be mentioned that slightly different structures are being fabricated by various semiconductor manufacturers, keeping though the same operating principle as described above. Therefore, several names indicating the same semiconductor structure can be identified in the corresponding market. Examples of such names besides the FS, are, soft-punch-through (SPT), light-punch-through (LPT), or extreme light-punch-through (XPT) IGBT. Lastly, IXYS has designed and fabricated a reverse conducting IGBT, called Bipolar Metal-Oxide Semiconductor Field Effect Transistor (BiMOSFET). A typical structure of a BiMOSFET is shown in Fig. 3.3(c). It is similar to a NPT IGBT structure, with one main difference, i.e. an n+ collector-short pattern [46]. BiMOSFET is an ideal semiconductor device for parallel connection due to the positive voltage temperature coefficient of both the saturation voltage and the forward voltage drop of its intrinsic diode. They can be found in semiconductor market in voltage class of $1600 - 3600V$.

The gate structure of a power semiconductor device can play an important role on both switching and conducting performance of the device. Even if trench-gate devices have been designed and fabricated at low-voltages during the last decades, only recently semiconductor manufacturers have managed to fabricate medium-voltage IGBTs based on trench-gate. The structural difference can be seen in Fig. 3.3(d), where a NPT IGBT with trench-gate has been considered. The trench-gate structure aims at enhancing the amount of carriers in the top region of the IGBT chip during the conduction [45]. Therefore, the conductivity modulation efficiency near the emitter region becomes higher compared to a planar-gate IGBT. The benefit of such a device is the low forward voltage drop [47, 45]. Although all the abovementioned IGBT structures can be designed with a trench-gate cell, only the NPT IGBT has been fabricated and can be found in semiconductor market with this gate technology. They are designed for blocking voltages up to $1200V$.

Last but not least, SiC-based IGBTs have been fabricated and researched. However, they face several manufacturing challenges and thus, they have not been commercially available. One of these challenges is the required highly resistive p-substrate of a SiC n-channel IGBT, which can cause significantly high conduction losses [48].

B. Silicon Carbide Metal-Oxide Semiconductor Field Effect Transistors

The most promising semiconductor device that can replace the Silicon IGBT is the SiC MOSFET [49]. One of the main reasons is that both devices have voltage-controlled gates which can ease the direct replacement. Besides the different material used, the structural difference between a SiC MOSFET and a PT IGBT is that the first device does not have the p+ substrate. The SiC MOSFETs are de-

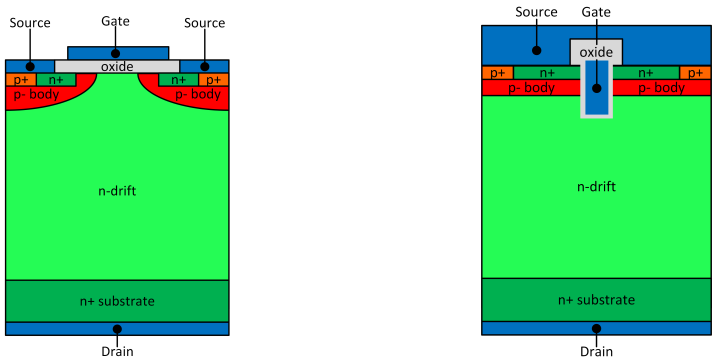


Figure 3.4: Typical SiC MOSFET structures with: (a) planar-gate, and (b) trench-gate technology.

signed and fabricated for blocking voltages up to few kV, and therefore they might be suitable for MVDC solid-state breakers [50]. Fig. 3.4 shows the two typical SiC MOSFET structures that can be found in semiconductor market at the voltage range of $1200 - 1700V$ [51]. In particular, a planar-gate SiC MOSFET is shown in Fig. 3.4(a), and a trench-gate counterparts in Fig. 3.4(b). The latter device exhibits lower conduction and switching losses [52], as well as it can withstand short-circuits for longer times compared to the planar-gate SiC MOSFETs [53].

C. Silicon Carbide Junction Field Effect Transistors

The last semiconductor category includes the majority-carrier device, called JFET. Today, the main semiconductor material used to fabricate high-power JFETs is SiC. Besides the advantageous performance of SiC over Silicon counterparts as it has been explained earlier, the absence of a gate-oxide layer in SiC JFET makes this technology more reliable for long-term and high-temperature operation [54]. SiC JFETs have been used for medium-power solid-state breakers [55, 56], and therefore, they will be considered in this thesis.

Two JFET types can be identified as shown in Fig. 3.2. Firstly, the normally-ON or depletion mode SiC JFET and secondly, the normally-OFF or enhancement mode SiC JFET [54]. The main structures of the two types can be seen in Fig. 3.5. The enhancement JFET is a normally-OFF device and it requires a significant gate current in order to be kept in ON-state [56]. The current driven nature of normally-OFF SiC JFET causes high power losses in the gate circuit. Additionally, the strong gate depletion-region overlap of a normally-OFF device leads to lower current conducting capability and higher specific ON-state resistance compared to

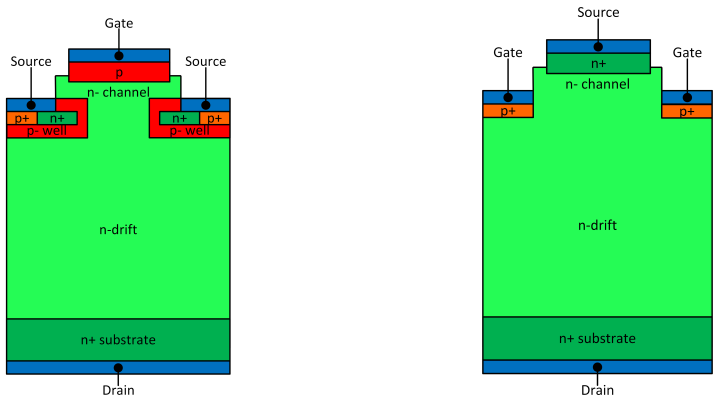


Figure 3.5: Typical SiC JFET structures: (a) depletion mode (normally-ON), and (b) enhancement mode (normally-OFF).

normally-ON counterparts [57]. Therefore, the normally-OFF SiC JFET will not be further investigated. On the other hand, Fig. 3.5(a) reveals the normally-ON nature of the depletion mode JFET. This feature makes this device a suitable candidate for solid-state breaker realization. They can be found in semiconductor market with blocking voltages up to $1700V$. Additionally, $3.3kV$ and $6.5kV$ normally-ON SiC JFET have also been studied and might become available for circuit breaker applications.

3.2.2 Comparative evaluation at nominal gate voltage

For the $1200V$ voltage class, nine power semiconductor devices (Table 3.2) from seven semiconductor technologies are evaluated in terms of normalized forward voltage drop. In addition, six devices from six semiconductor technologies at rated voltage of $1700V$ are also evaluated (Table 3.3).

Table 3.2: Design characteristics and rated current of $1200V$-class semiconductor devices

Semiconductor device	Structure technology	Gate structure	Current rating at $T_c = 25^oC$	Nominal gate voltage	Maximum gate voltage	Symbol
Silicon IGBT	NPT	Planar	60A	15	20	D_1
Silicon IGBT	NPT	Trench	50A	15	20	D_2
Silicon IGBT	XPT	Planar	84A	15	20	D_3
Silicon IGBT	FS	Trench	50A	15	20	D_{4a}
Silicon IGBT	FS	Trench	50A	15	20	D_{4b}
SiC MOSFET	-	Planar	63A	15	18	D_{5a}
SiC MOSFET	-	Planar	65A	20	22	D_{5b}
SiC MOSFET	-	Trench	55A	18	22	D_6
SiC JFET	Normally-ON	-	63A	0	2	D_7

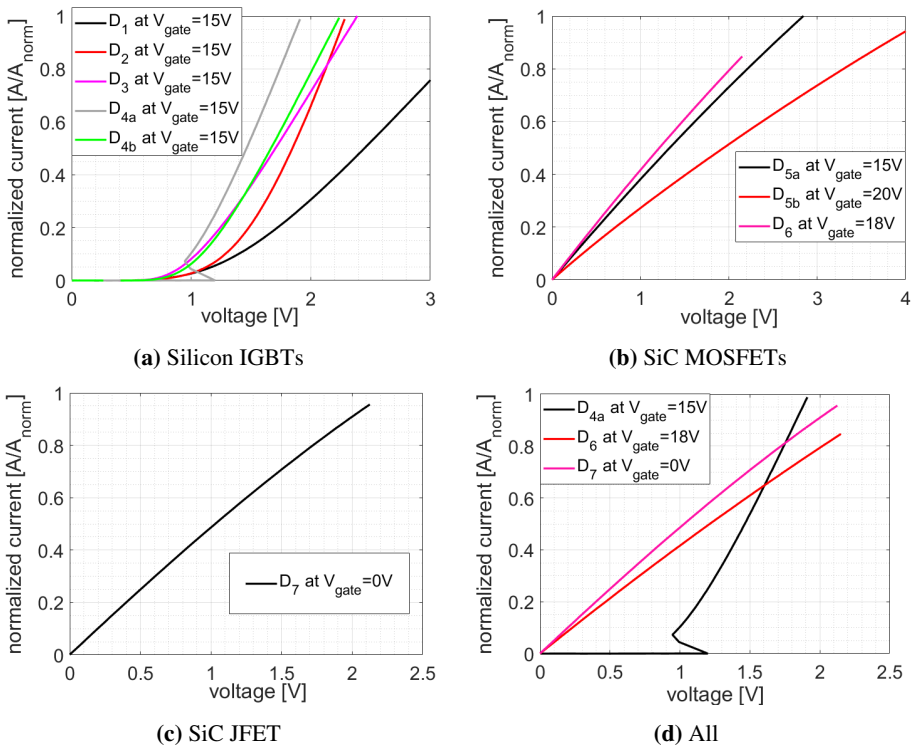
Table 3.3: Design characteristics and rated current of $1700V$-class semiconductor devices

Semiconductor device	Structure technology	Gate structure	Current rating at $T_c = 25^oC$	Nominal gate voltage	Maximum gate voltage	Symbol
Silicon IGBT	NPT	Planar	50A	15	20	D_8
Silicon IGBT	XPT	Planar	58A	15	20	D_9
Silicon IGBT	BiMOSFET	Planar	60A	15	20	D_{10}
SiC MOSFET	-	Planar	40A	20	22	D_{11}
SiC MOSFET	-	Trench	3.7A	18	22	D_{12}
SiC JFET	Normally-ON	-	273A	0	2	D_{13}

The B1505A Power Device Analyzer from Keysight Technologies has been used for measuring the forward voltage drop of the investigated devices at room temperature (25^oC) for a wide range of currents. However, even if the devices are rated in the same voltage classes, their current ratings differ as shown in Tables 3.2 and 3.3. Therefore, a more fair comparison is to use normalized currents in the IV characteristics and using the rated currents as the basis for each device. Lastly, five samples have been investigated for each device, and the results below show the average values of the measurements.

A. Power semiconductor devices rated at 1200V

The IV characteristics of the investigated power semiconductor devices when a nominal gate voltage is applied are depicted in Fig. 3.6. In particular, Fig. 3.6(a) shows the comparative results for the IGBT-based devices. It can be seen that the D_{4a} device, i.e. FS Silicon IGBT with trench-gate achieves the lowest forward voltage drop for almost the entire normalized current range. On the other hand, D_1, i.e. NPT Silicon IGBT with planar-gate structure achieved the highest forward voltage drop for the entire current range. The corresponding results with respect to the three investigated SiC MOSFETs are shown in Fig. 3.6(b). The SiC MOSFET with trench-gate, D_6 achieved the best performance in terms of minimizing the forward voltage drop for the entire normalized current range. Additionally, Fig. 3.6(c) shows the IV characteristic of the normally-ON SiC JFET. Finally, the comparative results of the three best semiconductor technologies are shown in Fig. 3.6(d). It can be seen that the normally-ON SiC JFET, D_7 exhibits the lowest forward voltage drop for the current range up to 80%, while the Silicon FS IGBT with trench-cell, D_{4a} achieved a better performance for the current range of 80-100%. This occurs due to the high injection of the minority carriers (holes) from the collector p+ region into the n-drift region which causes a reduction of the drift region resistivity of the IGBTs at high currents. The increased number of carriers at high current levels causes lower forward voltage drop across the IGBTs (conductivity modulation).



(a) Silicon IGBTs

(b) SiC MOSFETs

(c) SiC JFET

(d) All

Figure 3.6: IV characteristics at nominal gate voltages for all the investigated $1200V$ power semiconductor devices at room temperature (25^oC).

B. Power semiconductor devices rated at 1700V

A similar comparative study among the six $1700V$-class power semiconductor devices shown in Table 3.3 is presented below. The IV characteristic curves of the six devices are shown in Fig. 3.7. The superior performance of the normally-ON SiC JFET (D_{13}) in terms of the lowest forward voltage drop for the entire normalized current range is observed. Besides that, it can be seen that the SiC MOSFETs (D_{11} and D_{12}) achieve a better performance at low currents compared to IGBT-based counterparts (D_8-D_{10}). On the other hand, the NPT Silicon IGBT with planar-gate (D_8) and the BiMOSFET (D_{10}) perform better at high currents compared to MOSFET-based devices. This occurs due to the presence of conductivity modulation of the IGBT-based devices as explained previously. On the other hand, the forward voltage drop in MOSFETs relies on the resistivity of the channel in the body region and the resistivity of the drift region (see Fig. 3.4). These resistivities are independent to the drain-source current and thus, the MOSFET-based devices exhibit similar performance at low and high currents.

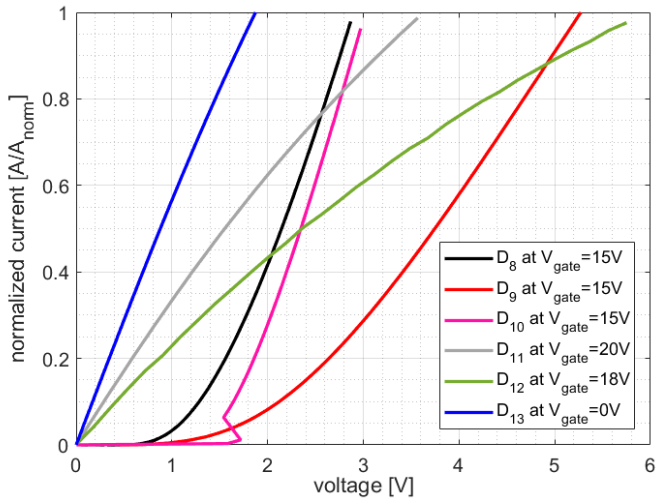
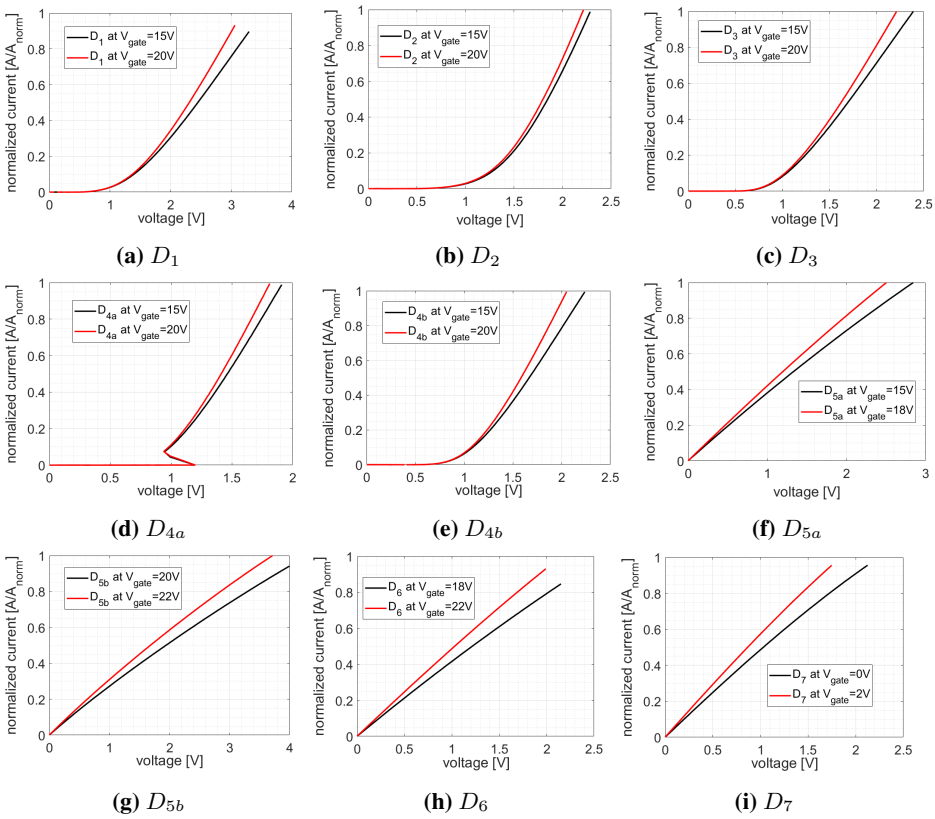


Figure 3.7: IV characteristic of power semiconductor devices rated at $1700V$ at room temperature (25^oC) under nominal gate voltages.

3.2.3 Comparative evaluation at maximum gate voltage

Among others, the forward voltage drop and hence the conduction losses of a power semiconductor device depend on the gate voltage, V_{gate}. When a higher voltage is applied to the gate (overdrive), the forward voltage drop decreases due to the higher carrier injection into the channel. This is valid for all investigated power device technologies. However, the gate voltage cannot be significantly higher than the nominal gate voltage value. It is limited by the thickness and characteristics of the gate-oxide layer in IGBTs and MOSFETs and by the gate current in JFETs. The maximum gate voltage is defined as the voltage that can be applied continuously to the gate of each device ensuring long-term reliability. The value of this maximum gate voltage is normally given in the datasheet of each device. Furthermore, the less critical switching operation in semiconductors employed in solid-state breakers can lead to the use of high gate resistances, which will cause slow switching speed and thus lower overvoltages in the gate loop. Therefore, the maximum voltage can be applied to the gate of semiconductors utilized in breakers without causing degradation in the gate-oxide layer. In this part of the thesis, the reduction of the forward voltage drop by applying the maximum gate voltage compared to the nominal gate voltage for all investigated devices is presented. The maximum gate voltage values have been taken from the datasheets of each device and they are shown in Tables 3.2 and 3.3 for the $1200V$-class and $1700V$-class devices respectively.



(a) D_1 **(b)** D_2 **(c)** D_3

(d) D_{4a} **(e)** D_{4b} **(f)** D_{5a}

(g) D_{5b} **(h)** D_6 **(i)** D_7

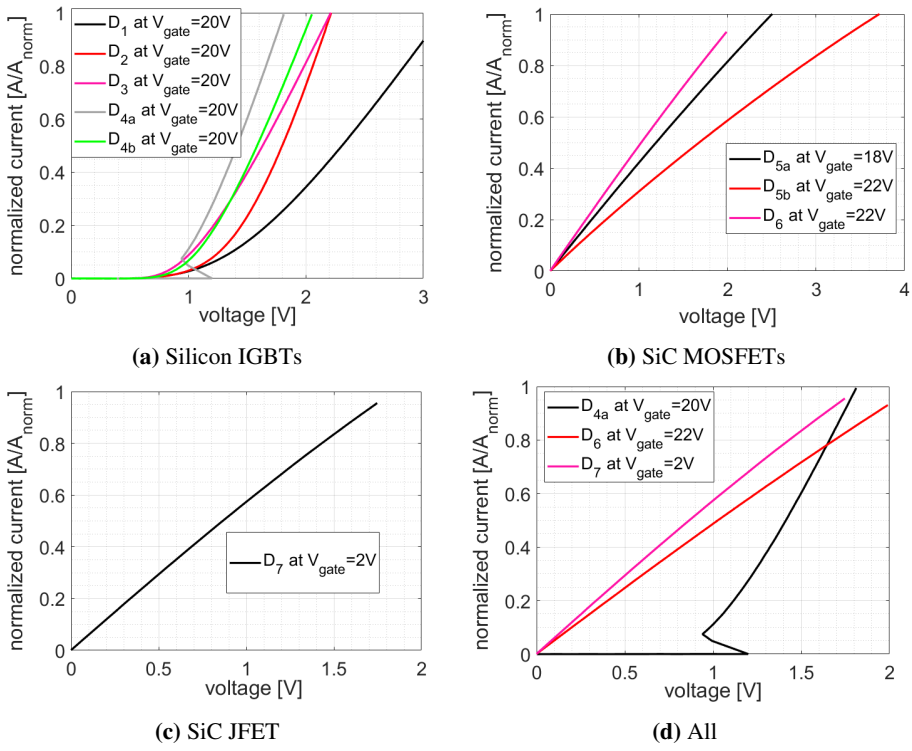
Figure 3.8: IV characteristic at nominal and maximum gate voltages for all investigated $1200V$-class power semiconductor devices.

A. Power semiconductor devices rated at 1200V

The impact of applying maximum gate voltage on the forward voltage drop reduction for all $1200V$-class semiconductor devices can be seen in Fig. 3.8. Even if the voltage reduction is not high in case of IGBT-based devices (D_1-D_{4b}), the corresponding reduction in case of SiC MOSFETs (D_{5a}-D_6) and SiC JFET (D_7) becomes significantly higher. The reason is the high carrier injection (electrons) from the gate to the channel via the source or emitter of each device. This causes a decrease of the resistivity of this channel, which plays more important role in the forward voltage drop of MOSFETs and JFETs compared to the corresponding voltage of IGBTs. The IGBTs experience an additional forward voltage drop due to the "pn" junction between the p+collector and n-drift regions, which cannot be found in unipolar devices, such as MOSFETs and JFETs. Therefore, the resistance of the channel in the IGBTs forward voltage becomes less important. The voltage

reduction when the maximum voltage is applied to the gate of each device at 80% of nominal current is as follows: 8.7% in D_1, 3.3% in D_2, 5.7% in D_3, 4.6% in D_{4a}, 6.5% in D_{4b}, 10% in D_{5a}, 14.5% in D_{5b}, 15% in D_6 and 17% in D_7.

A comparative study has also been conducted among all the $1200V$-class devices when the maximum gate voltage is applied and shown in Fig. 3.9. It can be clearly observed that the normally-ON SiC JFET, D_7 has achieved the best performance with respect to the minimum forward voltage drop at maximum gate voltage for the entire normalized current range. This differs slightly from the findings of the previous investigation when nominal gate voltages were applied to the devices. In the latter case, the Silicon FS IGBT with trench-cell exhibited lower conduction losses compared to the normally-ON SiC JFET for normalized current range of 80-100%. This means that the impact of applying the maximum gate voltage in JFET on its forward voltage drop is more significant compared to IGBTs as explained previously.



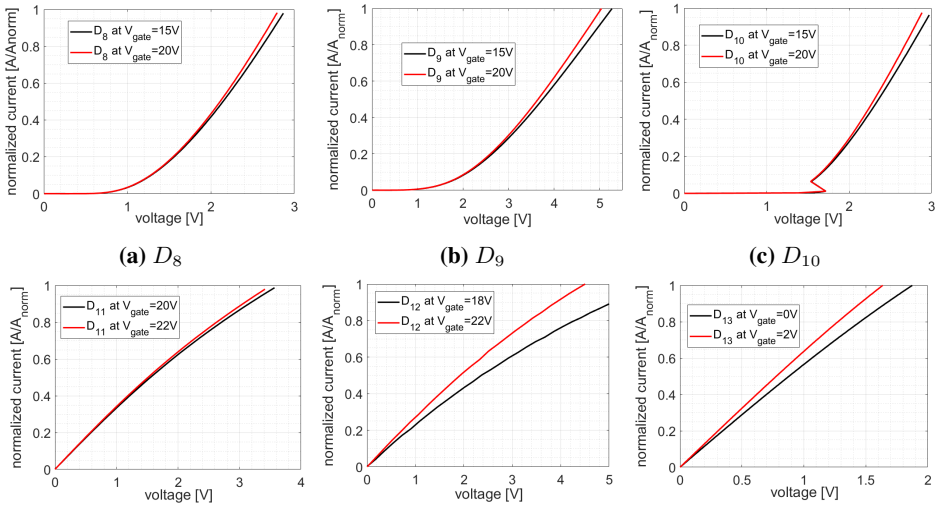
(a) Silicon IGBTs

(b) SiC MOSFETs

(c) SiC JFET

(d) All

Figure 3.9: IV characteristic at maximum gate voltages for all investigated $1200V$-class power semiconductor devices.



(a) D_8 **(b)** D_9 **(c)** D_{10}

(d) D_{11} **(e)** D_{12} **(f)** D_{13}

Figure 3.10: IV characteristic at nominal and maximum gate voltages for all investigated $1700V$ power semiconductor devices.

B. Power semiconductor devices rated at 1700V

A study to evaluate the impact of overdriving the $1700V$-class semiconductor devices on the forward voltage drop reduction has also been performed. In particular, Fig. 3.10 reveals that the IGBT-based devices (D_8-D_{10}) achieved a small forward voltage drop reduction by applying maximum gate voltage, while the SiC MOSFET with trench-gate (D_{12}) and the normally-ON SiC JFET (D_{13}) minimized their forward voltage drop significantly. These results are similar with the corresponding results of the $1200V$-class devices. Specifically, at 80% of normalized current, the reduction of the forward voltage drop for every investigated $1700V$-class power device when applying maximum gate voltage is as follows: 2.3% in D_8, 4.2% in D_9, 2.9% in D_{10}, 3.7% in D_{11}, 20% in D_{12} and lastly, 11.7% in D_{13}.

Finally, Fig. 3.11 shows the superior performance of the normally-ON SiC JFET in case of overdriving. Besides that and similar to the case with nominal gate voltage, it can be clearly seen that at low normalized currents, the SiC MOSFET-based devices achieve better performance compared to IGBT-based counterparts, while the latter devices manage to achieve lower forward voltage drop at high currents due to the high injection of minority carriers from the p+collector region into the n-drift region (conductivity modulation).

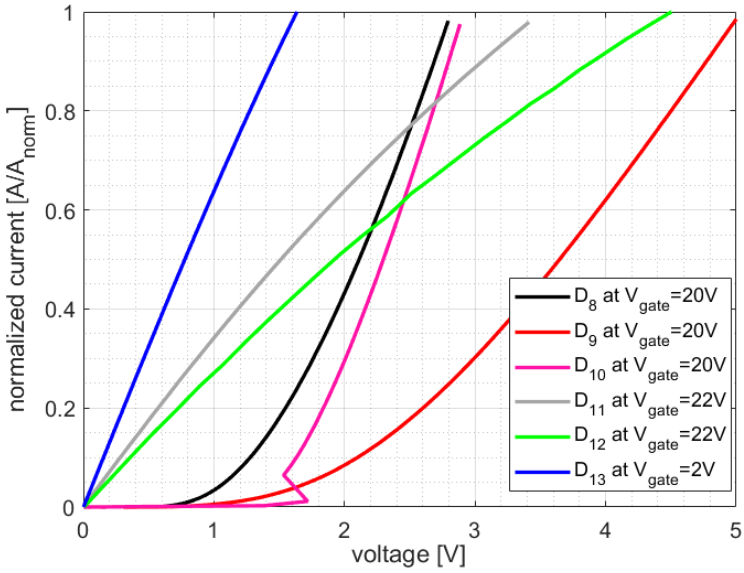


Figure 3.11: IV characteristic at maximum gate voltages for all investigated $1700V$-class power semiconductor devices.

3.2.4 Overdrive operation at high temperatures

The previous studies were conducted by using an IV curve tracer at room temperature (25^oC). However, when a power semiconductor device conducts current, the associated losses will cause a temperature rise in the die. This will also lead to even higher conduction losses due to the positive temperature coefficient of the device's forward voltage drop. Thus, a more fair comparison of the investigated semiconductor devices is by measuring their forward voltage drop at high junction temperatures.

The schematic diagram of the DC test circuit used for these experiments is shown in Fig. 3.12. A photograph of the experimental setup is illustrated in Fig. 3.13, in which a DC power source (ETSystem LAB/HP/E2020) has been used to supply the DC test current, I_{test}. In addition to that, a high-resolution voltmeter (Fluke 8842A) has been used to measure the forward voltage drop of the Device Under Test (DUT). The DUT is mounted on the surface of an aluminium heatsink with a fan (Fischer Elektronik, LA 21/200 24V). This cooling system has been kept constant for the entire set of experiments in order to provide the same heatsink thermal resistance. Finally, the case temperature of the DUT is measured using a K-type thermocouple (Amprobe TMD-50).

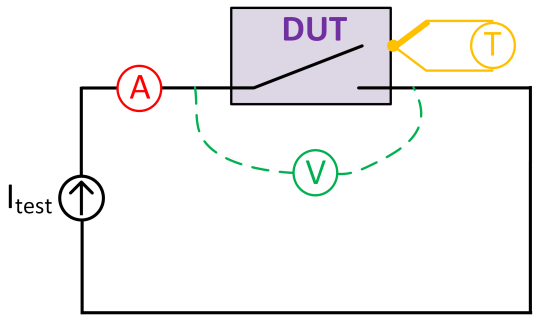


Figure 3.12: Schematic diagram of the test circuit for measuring the forward voltage drop across the DUT, and the DUT's case temperature for various I_{test}.

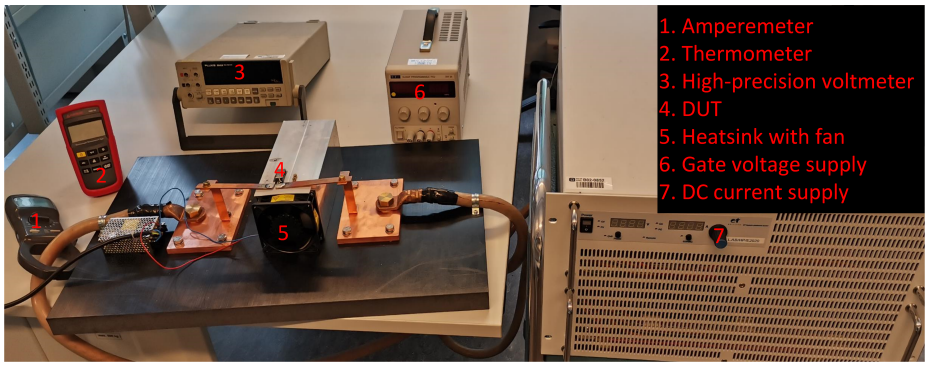
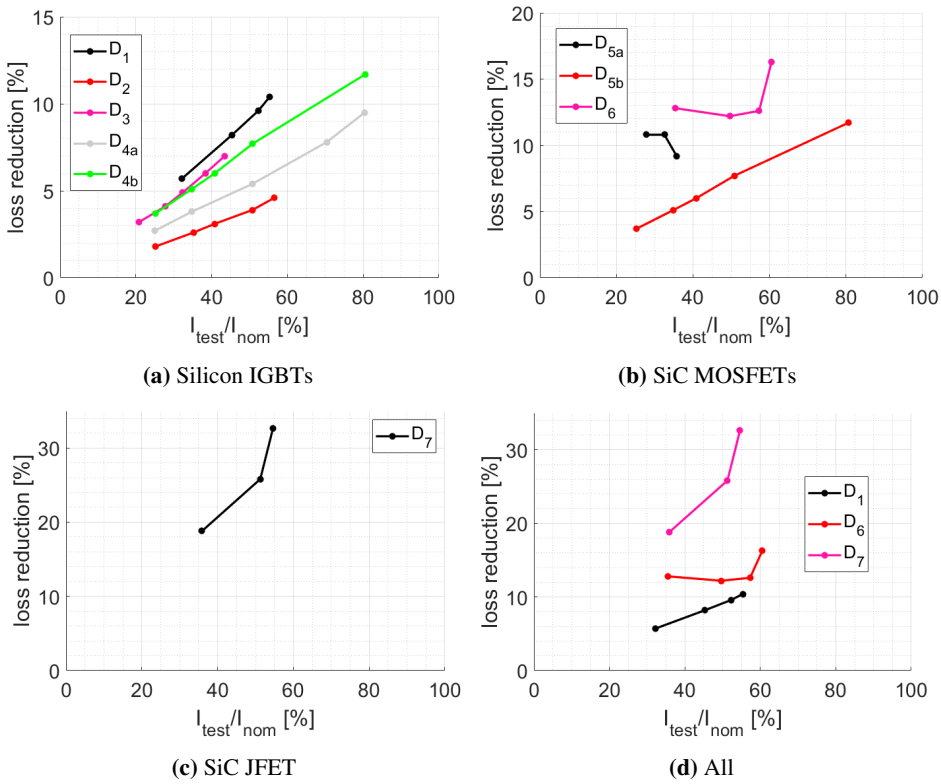


Figure 3.13: Photograph of the experimental test setup.

A. Power semiconductor devices rated at 1200V

The benefit of overdriving the power semiconductor devices at high junction temperatures in terms of conduction loss reduction compared to a case with nominal gate voltage, can be seen in Fig. 3.14. In particular, the reduction can be approximately 10% in case of Silicon FS IGBT with trench-gate (D_{4a} and D_{4b}) at 80% of nominal collector current. Additionally, in case of SiC MOSFETs, the reduction of the conduction losses can reach up to 17% for a 60% normalized drain current (D_6). Lastly, the normally-ON SiC JFET achieves again the best performance, minimizing the conduction losses up to 33% at 55% of normalized current when $2V$ is applied to the gate-source terminals.

It should also be mentioned that the conduction loss reduction becomes higher at elevated normalized currents for all $1200V$-class devices (except D_{5a}), revealing the advantageous overdrive concept. This occurs due to the more significant reduction of the junction temperatures of these devices when the maximum gate voltage



(a) Silicon IGBTs

(b) SiC MOSFETs

(c) SiC JFET

(d) All

Figure 3.14: Conduction loss reduction when applying maximum gate voltages at elevated junction temperatures for all $1200V$-class DUTs at various I_{test}.

is applied at high currents compared to the corresponding temperature reduction at low currents (see Table 3.4). The decrease of the junction temperature causes reduction of the devices' forward voltage drop and thus, the conduction loss reduction becomes more significant. This phenomenon is not obvious at D_{5a} because the maximum test current I_{test} in this device was set to only 36% of normalized current, leading the junction temperature of the device to be lower compared to all other cases (approximately 80^oC). Therefore, the impact of overdriving D_{5a} on the conduction losses at high current or at high junction temperature is not revealed. The maximum current I_{test} is the current value that it has been used in the test, before a thermal runnaway occurs in the DUT.

The numerical results of this experimental investigation are summarized in Table 3.4. This table shows the conduction losses, as well as the junction temperatures T_j of the semiconductor power devices under the maximum test current, I_{test} by applying the nominal and the maximum gate voltage. Besides the conduction

Table 3.4: Impact of the overdrive on the conduction loss and junction temperature of the $1200V$-class devices at maximum DC test current

Device test	V_{gate}	I_{test} $[A]$	I_{test}/I_{nom} $[\%]$	losses $[W]$	T_j $[^oC]$
D_1	Nominal	33.2	55	103.1	136.5
	Maximum	33.2	55	92.4	124.4
D_2	Nominal	28.3	57	63.2	112.7
	Maximum	28.3	57	60.3	108.5
D_3	Nominal	36.5	44	69.5	119.8
	Maximum	36.5	44	64.6	113.4
D_{4a}	Nominal	40.2	80	90.5	113
	Maximum	40.2	80	81.9	105.3
D_{4b}	Nominal	40.3	80	119.5	120.1
	Maximum	40.3	80	105.5	108.4
D_{5a}	Nominal	22.5	36	32.7	85.4
	Maximum	22.5	36	29.7	80.2
D_{5b}	Nominal	23.2	36	47.6	100.9
	Maximum	23.2	36	42	91.4
D_6	Nominal	33.3	61	88.6	105
	Maximum	33.3	61	74.2	92.4
D_7	Nominal	34.4	55	76.2	88.8
	Maximum	34.4	55	51.4	68.9

loss reduction, the reduction of the junction temperature when the maximum gate voltage is applied, is also observed. This could potentially soften the cooling requirements if a semiconductor device is overdriven leading to smaller and less costly cooling systems.

B. Power semiconductor devices rated at 1700V

The impact of overdriving the six $1700V$-class power semiconductor devices at high junction temperatures on the conduction loss reduction is shown in Fig. 3.15. The normally-ON SiC JFET, D_{13} exhibits the highest conduction loss reduction when the maximum voltage is applied to the gate. In particular, the loss reduction reaches almost 23% at 31% of normalized current. On the other hand, the IGBT-based semiconductor devices (D_8-D_{10}) achieve a significantly lower loss reduction. This reduction is approximately 5% at around 40% of normalized current. In addition to that, the SiC MOSFET with trench-gate structure D_{12}, managed to reduce the forward voltage drop and thus the conduction losses at almost 15% for

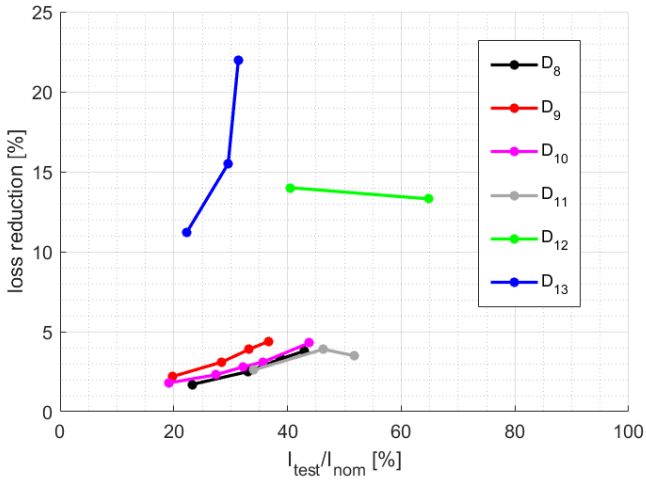


Figure 3.15: Conduction loss reduction when applying maximum gate voltages at elevated junction temperatures for all $1700V$-class DUTs at various I_{test}.

Table 3.5: Impact of the overdrive on the conduction loss and junction temperature of the $1700V$-class devices at maximum DC test current

Device test	V_{gate}	I_{test} $[A]$	I_{test}/I_{nom} $[\%]$	losses $[W]$	T_j $[^oC]$
D_8	Nominal	21.5	43	56.6	128.3
	Maximum	21.5	43	54.4	124
D_9	Nominal	21.3	37	103	136
	Maximum	21.3	37	98.6	131.6
D_{10}	Nominal	26.3	44	77.7	137.8
	Maximum	26.3	44	74.4	133.2
D_{11}	Nominal	20.7	52	46.7	88.7
	Maximum	20.7	52	45	86.4
D_{12}	Nominal	2.4	65	10.5	80.5
	Maximum	2.4	65	9.1	73.4
D_{13}	Nominal	85.6	31	97.7	83.8
	Maximum	85.6	31	76.2	70

a normalized current range of $40 - 60\%$. Finally, the numerical results for conduction losses, as well as the junction temperatures of the DUTs at both voltage gate conditions (nominal and overdrive) at the maximum test current can be seen in Table 3.5.

3.3 Semiconductor device technologies for high-power MVDC solid-state breakers

An MVDC power grid usually operates at a voltage level that is between $1kV$ to $35kV$ [8] or even up to $70kV$ [58]. Therefore, the use of multiple series-connected devices for the breaker design is required. However, this will introduce challenges with respect to transient voltage imbalances during turn-OFF process which will be analyzed in Chapter 5. As a result, semiconductor devices rated at the highest possible blocking voltage must be considered for such MVDC applications in order to minimize the required number of series-connected devices. In addition to that, the power ratings of such grids can be up to several MW, and thus, a high load current will be anticipated. Therefore, high-voltage semiconductor devices encapsulated in modules or press-packs must be employed in solid-state breakers for high-power MVDC grids.

Several potential candidates for solid-state breakers design can be found in the semiconductor market. First of all, thyristors can be utilized in a solid-state breaker due to their inherent advantage of low conduction losses and high breakdown voltages [59]. However, their main drawback is the lack of controllable turn-OFF, and thus, they can be used only along with addition circuits (e.g. passive component that will create resonance) that will force the thyristors to turn-OFF when a fault occurs. A few alternatives to thyristors have been manufactured providing a controllable turn-OFF and, keeping at the same time the low conduction losses of the thyristors. Two such devices are the Gate Turn-OFF (GTO) thyristor [59] and the Integrated Gate Commutated Thyristor (IGCT) [60]. Besides thyristor-based devices, multiple NPT IGBT chips can also form modules and press-packs providing high-voltage and high turn-OFF current capabilities [45]. Furthermore, a new advanced high-voltage high-power device has been commercialized recently, the so called Bi-mode Insulated Gate Transistor (BIGT) [61]. It integrates an IGBT with a reverse conducting-(RC-) IGBT into a single chip. Apart from the commercially available devices, several other have been developed by researchers but have not become commercial yet. The super Gate Turn-OFF (sGTO) [62] and the Emitter Turn-OFF (ETO) [63] are such devices that can be utilized in high-power solid-state MVDC circuit breakers.

Even if the SiC technology has progress significantly the last decades, there is still lack of a commercial high-voltage and high-current SiC-device capable to be used in high-power MVDC breakers. However, high-voltage SiC devices are still under extensive investigation by the research community and thus, a SiC-module with voltage and current ratings similar to the today's state-of-the-art Silicon IGBTs will be foreseen in the close future.

3.3.1 Commercially available high-voltage and high-power semiconductor devices

Based on the brief analysis above, it is apparent that three high-voltage and high-power devices can be used in MVDC solid-state breakers. These are the NPT IGBTs, the BIGTs, and the IGCTs. A short description of each device follows.

- **NPT IGBT:** The structure of a NPT IGBT has been previously explained in detail. Herein, a focus on different semiconductor packaging technologies, and mostly on the press-pack technology is given. A single IGBT chip is normally integrated into a "TO" package. On the other hand, when a switch realization requires higher breakdown voltage and current, then several chips must be connected in parallel and in series. The packaging of such a switch can be done by two technologies, i.e. module packaging and press-pack technology. Even if the first packaging can be found in semiconductor market with higher voltage ratings (up to $6.5kV$ with $1kA$), the last type is a favorable device when a high-voltage application requires high current (up to $4.5kV$ with $3kA$). The main advantages of the press-pack packaging are: (i) high thermal cycling capability, (ii) double-side cooling, (iii) high power density, (iv) ease of laying out in series and finally (v) short-circuit failure mode. Moreover, the turn-OFF current capability is normally defined at two times the nominal current, which means that a $4.5kV$ press-pack IGBT can interrupt a $6kA$ current securely. It should be finally mentioned that the positive temperature coefficient of the forward voltage of the IGBTs eases their parallel connection if required.
- **BIGT:** This new semiconductor device not only eliminates the need for external anti-parallel diode for achieving reverse conduction capability, but also increases the active silicon area compared to both IGBT and RC-IGBT. Therefore, a low forward voltage drop can be achieved leading to low conduction losses. Additionally, the larger active area provides better thermal performance of this device. ABB has patented the BIGT, and it can be found in market with voltage and current ratings up to $5.2kV$ and $2.1kA$ in press-pack technology. Lastly, BIGTs also have a positive temperature coefficient.
- **IGCT:** This is a current-controlled minority-carrier device. It is a thyristor-based device that exhibits low conduction losses similar to thyristor, but it can also turn-OFF from the gate by draining a negative current pulse in the range of the anode current. The main structural difference of IGCTs compared to GTOs is the integrated gate. Additionally, they require shorter storage time compared to GTOs at a cost of high gate current.

Three high-voltage high-power press-pack IGCT-based devices are manufactured by ABB. The first type is an asymmetric IGCT, which can block and conduct only in forward direction. The second type is a reverse blocking IGCT, which blocks in both directions, and the last type is a reverse conducting IGCT which conducts in both ways, but it blocks only in forward direction [64]. They can be found in market with blocking voltage capabilities up to $6.5kV$, whereas the current rating can be up to $4kA$. Even if researchers have shown that IGCTs can interrupt sufficiently a much higher current than the nominal value, it is recommended to not exceed significantly this value when turns-OFF. Similar to IGBTs and BIGTs, IGCTs also have positive temperature coefficient that eases the parallel connection.

3.3.2 Modelling and simulation of a high-power solid-state MVDC breaker

A performance evaluation of three solid-state breakers employing IGBTs, BIGTs and IGCTs has been conducted. The evaluation criteria are the conduction power losses for various power and voltage levels of an MVDC grid, as well as the responses of the breakers in case of a short-circuit occurrence. The simplified DC grid shown in Fig. 2.5 has been modelled using PLECS and Matlab/Simulink. The first simulation software has been used for the steady-state analysis, while the transient analysis during a short-circuit clearance was carried out through Matlab. The solid-state breaker shown in Fig. 2.4(b) has been used for the breaker modelling. In addition, a current limiting inductor L_s, has been connected in series with the breaker as illustrated in Fig. 3.1. The DC grid parameters used are: $L_{line} = 1\mu H$, $R_{line} = 1m\Omega$ and, $L_s = 150\mu H$. The DC voltage and load current have been set to $3kV$ and $1.5kA$ respectively as a "base" case. The parameters of the three investigated high-power semiconductor devices are summarized in Table 3.6.

3.3.3 Steady-state simulation results

The thermal simulation models for the three devices have been provided by the semiconductors manufacturer. These models include the devices thermal characteristics which are required for the simulation of the conduction loss and the junction temperature. Several voltage and power levels of an MVDC grid have been considered for the present evaluation. Fig. 3.16 shows the conduction losses, as well as the anticipated junction temperature of each device for various load currents in a $3kV$ DC grid. The examined range for the load current starts from $0.5kA$ to $3.75kA$. As observed, when the current becomes higher than $2kA$, two devices must be connected in parallel in order to share the load current for all switches.

The conduction losses are kept the lowest among the three devices for the entire investigated current range when IGCTs are employed in the breaker. In particular,

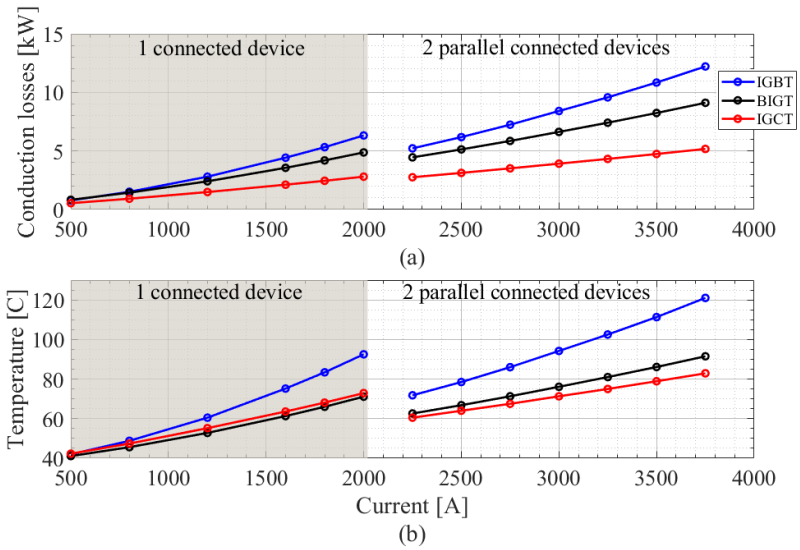


Figure 3.16: Steady-state results for the three investigated semiconductor press-pack devices employed in a $3kV$ solid-state DC breaker for various load currents with respect to: (a) conduction power losses, and (b) junction temperature.

for a load current of $3kA$ and two parallel-connected IGCTs, the total conduction losses are approximately $4kW$, while in case of IGBTs and BIGTs, the corresponding losses become $8kW$ and $6.5kW$ respectively. As a consequence of the

Table 3.6: Parameters of the investigated high-power semiconductor devices employed in a solid-state MVDC breaker

	IGBT	BIGT	IGCT
Manufacturer	ABB	ABB	ABB
Model	5SNA2000K450300	5SJA3000L520300	5SHY35L4522
Blocking voltage	$4.5kV$	$5.2kV$	$4.5kV$
Maximum turn-OFF current	$4kA$	$6kA$	$4kA$
Forward voltage ($4kA$, 125^oC)	$5.1V$	$3.6V$	$2V$
Thermal resistance junction to case	$4K/kW$	$2.1K/kW$	$8.5K/kW$
Packaging dimensions	247x237.3x28.8	237x250x31.5	439x173x41 150x150x411*

* without GDU

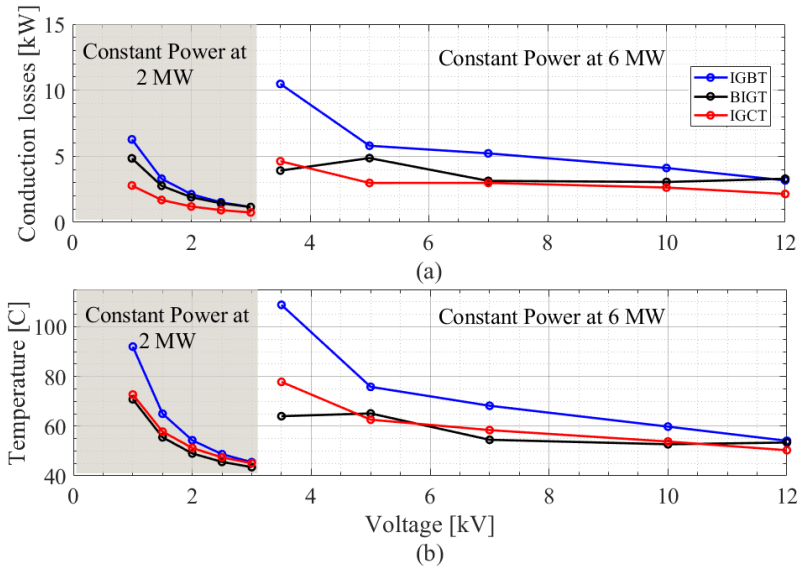


Figure 3.17: Steady-state results for the three investigated semiconductor press-pack devices employed in a solid-state breaker for various DC voltage levels and two load demands with respect to: (a) conduction power losses, and (b) junction temperature.

low conduction losses and hence dissipated energy, the junction temperature of the IGCTs also remains very low. On the other hand, the IGBTs exhibit the worst performance in terms of conduction losses and junction temperature. However, the increased complexity of the GDU in IGCTs due to the required high gate current during the turn-OFF makes these devices less suitable compared to the voltage-controlled IGBTs.

MVDC grids can be in the voltage range of $1-60kV$. In the second study presented below, this range has been examined under three different power loads, i.e. $2MW$ for the voltage range $1-3kV$, $6MW$ for $3.5-12kV$, and $25MW$ for the voltage range $15-60kV$. The simulation results are shown in Fig. 3.17 for the first two load cases and in Fig. 3.18 for the third case. Series connection of multiple device has also been considered when necessary. On the other hand, a parallel connection of two or more switches is not required in any case. Almost in the entire investigated voltage range, the IGCTs achieve the lowest conduction losses compared to IGBTs and BIGTs. There is only one case, where the BIGTs perform better than IGCTs. That is when the voltage is set to $3.5kV$ and the load power is $6MW$. The reason for that is that two IGCTs need to be connected in series when employed in a breaker configuration to block the $3.5kV$, while one single BIGT is sufficient in the other case. The use of a single BIGT reduces the conduction losses significantly.

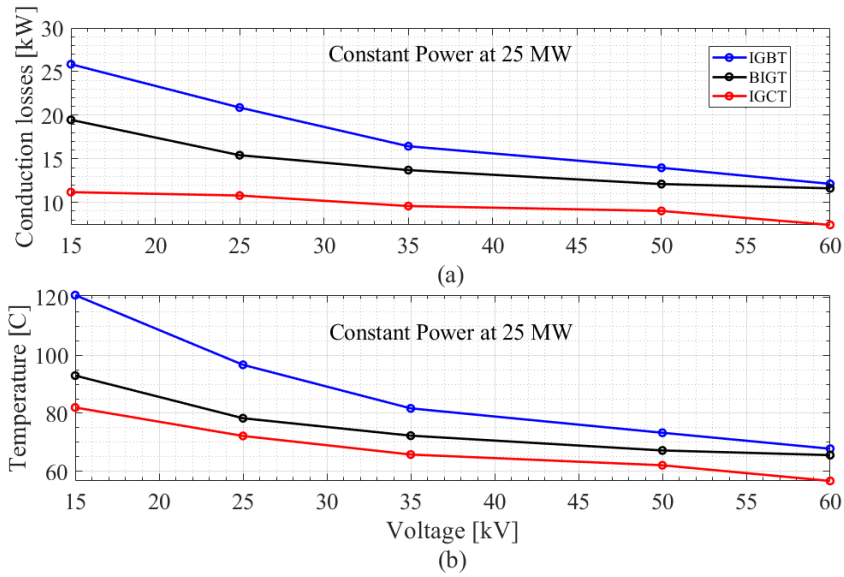


Figure 3.18: Steady-state results for the three investigated semiconductor press-pack devices employed in a solid-state breaker for various DC voltage levels and $25MW$ load power with respect to: (a) conduction power losses, and (b) junction temperature.

3.3.4 Dynamic simulation results

The previous study was related to the thermo-electrical performance of three high-power semiconductor devices during nominal operation in MVDC solid-state breakers. A dynamic comparative study during a short-circuit clearance has also been examined and simulated using Matlab/Simulink. The "base" case for the DC grid, i.e. $3kV$ and $1.5kA$ is adopted in this analysis. The devices models included in Simulink have been modified and adapted to the actual devices using their datasheet parameters. The threshold current for breaker tripping is set to $3kA$. Fig. 3.19(a) illustrates the short-circuit line current in the three cases. The BIGT-based breaker achieves slightly lower fault current compared to the other two device cases. This is mainly due to the shortest required time delay for turning-OFF of the BIGT compared to the IGBT and IGCT. The highest fault current is observed in IGCT-based breaker, i.e. $3538A$, while in case of BIGT-based breaker, the current reaches $3479A$. Finally, in IGBT-based case, the peak fault current is $3512A$. It can be clearly concluded that the differences in the fault currents are not of great importance when designing a high-power solid-state MVDC circuit breaker. Finally, similar results can also be seen for the switch currents and voltages, as depicted in Fig. 3.19(b) and 3.19(c) respectively.

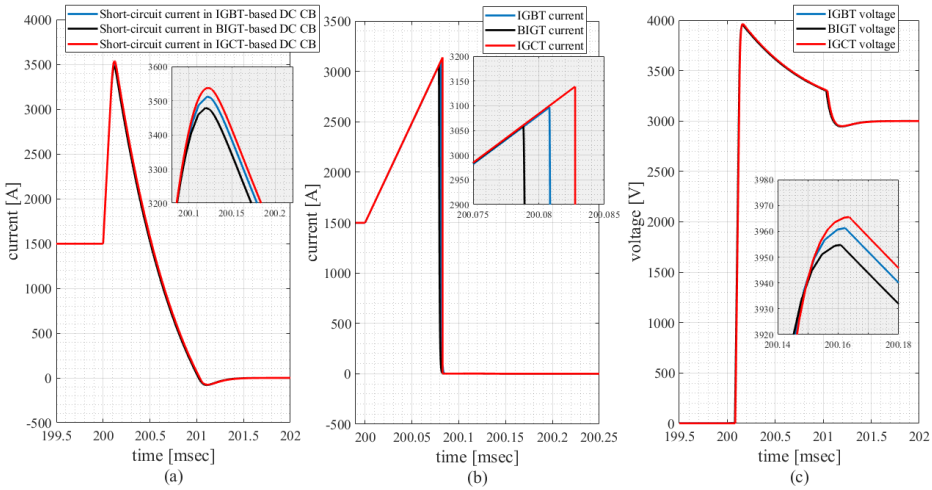


Figure 3.19: Dynamic results for the three investigated solid-state breakers in a $3kV$ DC power grid employing IGBTs, BIGTs and IGCTs during a fault incident with respect to: (a) short-circuit line current, (b) switch current, and (c) switch voltage.

3.4 Conclusions

A comparative evaluation of several Silicon and SiC semiconductor device technologies has been presented and discussed in this Chapter. The targeted application is solid-state circuit breakers for LVDC and MVDC power grids. Initially, the desired characteristics of a power semiconductor device intended to be used in solid-state breakers were analyzed briefly, emphasizing mostly on the need for reducing its forward voltage drop. This leads to the increase of the solid-state breakers efficiency, which is currently the major showstopper for their development.

Two cases have been studied. The first is related to power semiconductor devices rated in the voltage class of $1200 - 1700V$. They can be employed in medium-power solid-state breakers rated up to approximately $1200V_{DC}$. Several semiconductor device technologies have been considered and investigated. Among them, the state-of-the-art Silicon IGBT-based devices, the SiC MOSFETs and the normally-ON SiC JFET. Two studies were experimentally conducted, one at room temperature and one at elevated junction temperatures. In both experiments, the normally-ON SiC JFET achieved the best performance almost for the entire current range by exhibiting the lowest forward voltage drop, for both voltage classes. Additionally, the impact of applying the maximum voltage to the gate of the investigated devices on the forward voltage drop reduction has also been examined. The performance of all devices has improved by lowering the forward voltage drop

when overdriving. Especially the normally-ON SiC JFET achieved a conduction loss reduction up to 33% at 55% of normalized current.

The second case includes high-voltage high-power semiconductor devices in press-pack technology. The considered high-power solid-state breakers have been rated up to $60kV_{DC}$ by employing three semiconductor device types, i.e. IGBT, BIGT and IGCT. The simulations reveal the superior performance of the IGCT in terms of exhibiting the lowest conduction losses for almost all investigated operating points. Specifically, in a $35kV_{DC}$ and $25MW$ grid, the conduction losses in case of IGCT-based breaker were $9.5kW$, while in IGBT and BIGT cases the corresponding losses were $16kW$ and $14kW$ respectively. However, the required high gate current during the turn-OFF of the IGCTs remains a crucial issue in these devices in contrast with the voltage-controlled IGBTs.

Chapter 4

Overvoltage suppression configurations for LVDC and MVDC solid-state breakers

In this Chapter, the interrupting solid-state circuit breaker for LVDC and MVDC applications is analyzed. The design principles of this breaker are described in the beginning of the Chapter. Additionally, the design, operation and performance of three overvoltage suppression configurations are presented. The performance of the three configurations has been assessed through simulations and experiments. The evaluated criteria are the current and voltage stress of the semiconductors used in the breakers during a fault clearance operation, as well as their requirements for passive components.

Contributions

Several attempts have been presented in literature to analyze the overvoltage suppression circuits employed in semiconductor devices. However, they mainly aim to operate in switch-mode power converters or in low-voltage DC solid-state breakers (up to $400V$). The main contribution of this Chapter is to analyze such circuits that are used in medium-power and high-power solid-state circuit breakers rated at $700 - 1800V_{DC}$ voltage. It has been revealed that the suitability of each configuration depends on the application design and operating constraints. The content of this Chapter summarizes the work presented in [P5], and it also contains additional information.

4.1 Design principles of a solid-state DC circuit breaker

A schematic diagram of the interrupting solid-state circuit breaker for LVDC and MVDC grids is shown in Fig. 3.1. It consists of three main power components, i.e. a current limiting inductor L_s, power semiconductor devices and overvoltage suppression circuits. The role of the current limiting inductor, L_s is to limit the rapid increase of the short-circuit current while the power semiconductor devices interrupt the fault current. In Chapter 3, the power semiconductor devices suitable for solid-state breakers have been analyzed. Lastly, the overvoltage suppression circuits protect the power semiconductor devices from breakdown and simultaneously, dissipate the residual magnetic energy stored in the current limiting inductor and in DC line.

4.1.1 Current limiting inductor

The low-inductive lines in LVDC and MVDC power grids can lead to high short-circuit currents within a short time period and, thus, the current limiting inductor is necessary. Considering the maximum allowable current, $I_{sc_{max}}$, the threshold current that trips the breaker, I_{thres} and time delays due to sensing, coordination and communication, t_{delay}, the following expression for L_s must be fulfilled:

$$L_s \geq \frac{V_{DC}}{\frac{I_{sc_{max}} - I_{thres}}{t_{delay}}} \tag{4.1}$$

where, V_{DC} is the nominal DC grid voltage. The specific values for both $I_{sc_{max}}$ and I_{thres} are normally defined by the grid operators. Additionally, t_{delay} might have a crucial impact on the choice of current limiting inductor especially in multi-terminal LVDC and MVDC power grids [65, 66]. This occurs due to the more sophisticated protection strategies applied to such grids, which impose long coordination and communication times.

4.1.2 Overvoltage suppression circuit

The overvoltage protection of the power semiconductor devices must also be ensured when designing a solid-state breaker. The high di/dt during the switch-OFF process along with all the inductive components in an LVDC or an MVDC grid will cause an overvoltage across the switches. Besides the overvoltage protection, an energy absorption component, such as an MOV, must also be employed in the breaker for dissipating the residual energy of the grid. The focus of this Chapter is to investigate the performance of three main overvoltage suppression configurations that can be used in solid-state breakers for LVDC and MVDC applications.

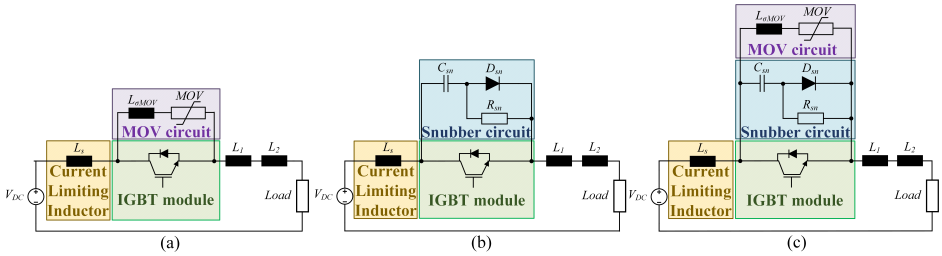


Figure 4.1: The three investigated configurations: (a) CON1, (b) CON2, and (c) CON3.

4.2 Circuit analysis of three overvoltage suppression configurations employed in solid-state DC breakers

The three investigated overvoltage suppression configurations that can be utilized in solid-state breakers are shown in Fig. 4.1. The first configuration (CON1) only contains an MOV as shown in Fig. 4.1(a). Fig. 4.1(b) depicts the second overvoltage suppression configuration (CON2). It employs an RCD snubber circuit connected in parallel to the semiconductor device. Finally, the use of both MOV and RCD snubber circuit as an overvoltage suppression circuit gives the third configuration (CON3) illustrated in Fig. 4.1(c). The operating principles of each topology are presented below. For this investigation, IGBTs have been used as semiconductors and the stray inductance in the MOV path, $L_{\sigma MOV}$, has also been taken into account.

4.2.1 CON1: Solid-state DC circuit breaker with MOV

The CON1 is the simplest topology. The MOV is connected in parallel to the main switches, and it clamps the voltage across the semiconductor devices. Additionally, the MOV dissipates the magnetic energy stored in the DC line and in the current limiting inductor. Fig. 4.2 shows the four operating stages during a fault clearance for the solid-state breaker employing CON1. Stage 1 shows the conducting operation of the circuit breaker prior to a short-circuit. At the time instant t_f, a short-circuit occurs in the DC line. After that point, the DC current rises and when the fault is detected, a command is given to the IGBT to turn-OFF (at t_{open}). Then, both the IGBT voltage and the short-circuit current increase until the first reaches the clamping voltage of the MOV. At that point, the MOV is activated and the current commutates from the IGBT to the MOV. The time instant that denotes the zero IGBT current crossing is t_{off}. After that, the fault current flows through the MOV and steadily decreases until all stored energy in the DC line and the current limiting inductor is dissipated. The last stage normally is the longest, especially when the inductances are very high (in the range of few hundreds μH).

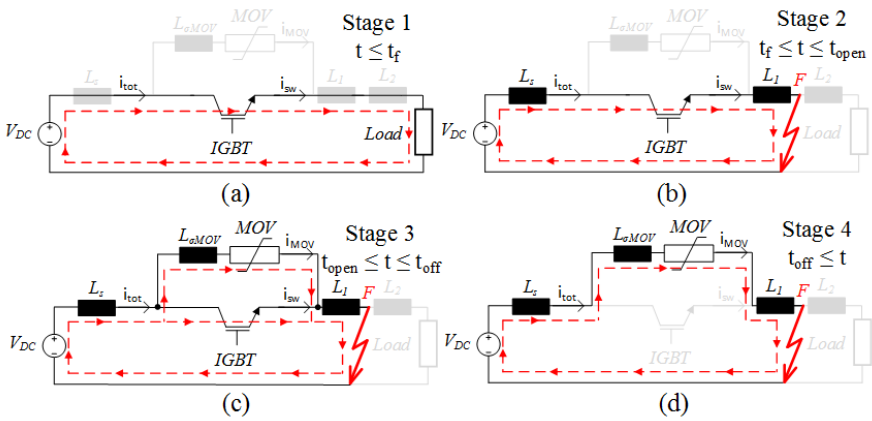


Figure 4.2: Schematic diagrams of the discrete operating stages of the solid-state DC circuit breaker using CON1.

4.2.2 CON2: Solid-state DC circuit breaker with RCD snubber circuit

In the second investigated voltage suppression configuration, CON2, an RCD snubber circuit is connected in parallel to the IGBT. In that case, when the switch turns-OFF, the short-circuit current commutates to the snubber branch, charging the capacitor C_{sn} through the diode D_{sn}. The voltage across the IGBT is controlled by means of the snubber capacitance depending also on the value of the instantaneous fault current. The snubber capacitor is discharged through the snubber resistance R_{sn}.

Five operating stages can be identified in this configuration (Fig. 4.3). The first stage refers to the DC grid operation prior the fault incident at time instant t_f. During that stage, the line current flows through the IGBT. After the fault incident, the line current increases. When the short-circuit current reaches the threshold value I_{thres}, a tripping command is given to the IGBT to start the turn-OFF process at time instant t_{open}. During the IGBT turn-OFF process, the fault current is commutated from the IGBT to the RCD snubber circuit and thus, the snubber capacitor starts charging. Stage four starts when the IGBT's current crosses the zero point at time instant t_{off}. During that stage, the fault current keeps increasing and charging the snubber capacitor. This stage lasts until the inductive energy stored in the DC line and in the current limiting inductor is completely transferred to the snubber capacitor. This occurs at time instant t_{ch}. The last operating stage includes the discharging of the snubber capacitor through the snubber resistor to the DC grid. The design principles of the snubber components follows in Chapter 4.3.

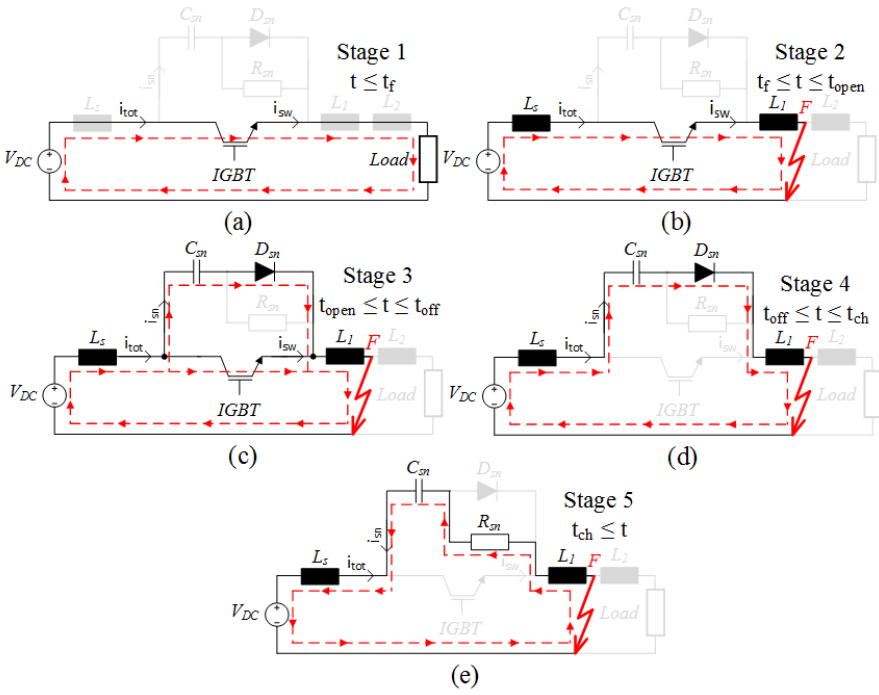


Figure 4.3: Schematic diagrams of the discrete operating stages of the solid-state DC circuit breaker using CON2.

4.2.3 CON3: Solid-state DC circuit breaker with MOV and RCD snubber circuit

The third overvoltage suppression configuration, CON3, is based on a combination of an RCD snubber circuit and an MOV. The main operating principle is that the snubber capacitor controls the voltage rise across the semiconductor device during the turn-OFF and then, the MOV clamps the voltage and protects the IGBT. Seven operating stages can be identified in that configuration as shown in Fig. 4.4. The first three stages are similar to CON2. The fourth stage starts at the time instant t_{off} and lasts until the voltage across the snubber capacitor reaches the clamping voltage of the MOV. This occurs at t_{MOVi} which initiates the next operating stage as illustrated in Fig. 4.4(e). During that time interval, the fault line current is the sum of both snubber and MOV currents. The current through the snubber capacitor decreases until it reaches zero at the time instant $t_{isn=0}$, which denotes the end of the stage five. In the next stage, the capacitor starts discharging feeding current back to the source through the snubber resistor, whereas the rest of fault current flows in the MOV path. The discharging of the snubber capacitor causes the

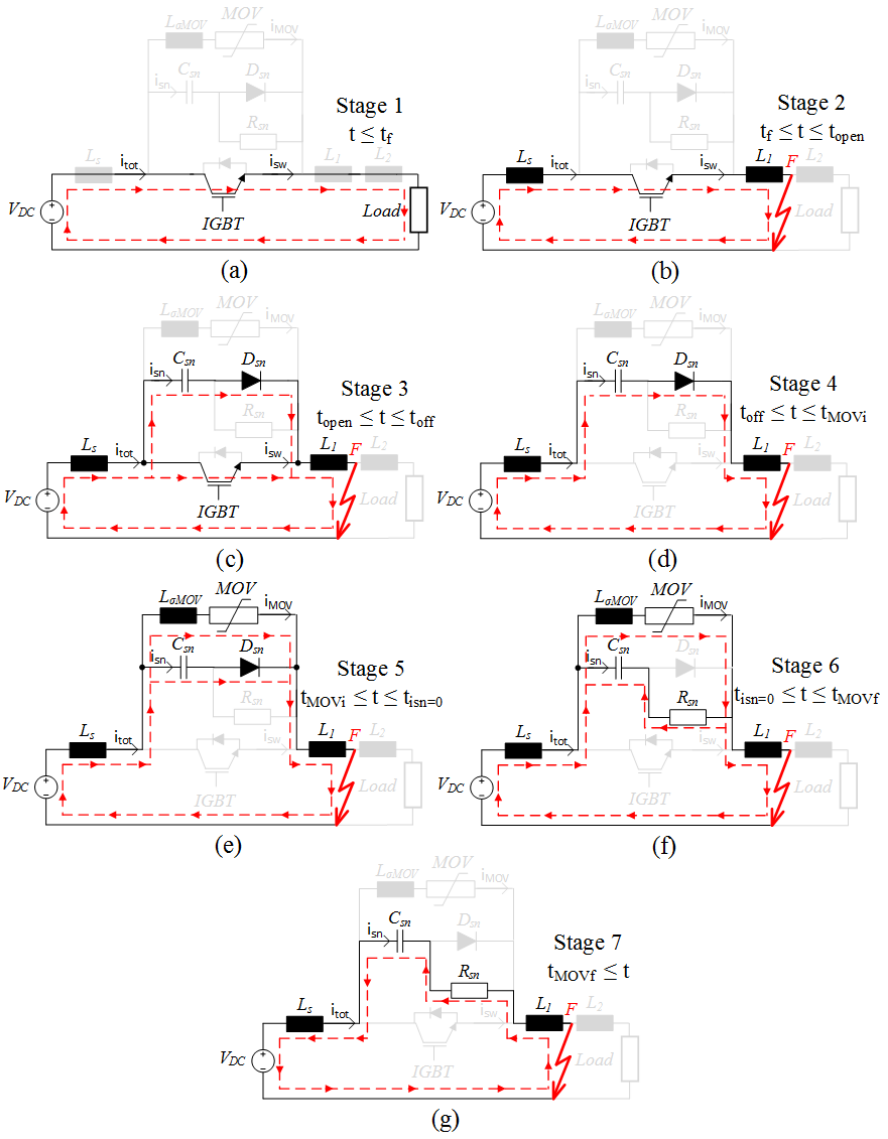


Figure 4.4: Schematic diagrams of the discrete operating stages of the solid-state DC circuit breaker using CON3.

voltage across the MOV to drop below the clamping value, and hence, the MOV current stops flowing. This occurs at the time instant t_{MOVf}. The last operating stage of CON3, is similar to the corresponding last stage of CON2 and involves the discharging of the snubber capacitor.

4.3 Design principles of the three overvoltage suppression configurations

In this part of the thesis, the design principles of CON1, CON2 and CON3 are discussed. For all three cases, IGBTs have been considered as the power semiconductor devices for the solid-state breaker. In the analysis below, the forward voltage drop of snubber diodes and IGBTs has been neglected.

4.3.1 Design principles of CON1

The schematic diagram of CON1 is shown in Fig. 4.1(a). At first, the current limiting inductor L_s should be designed according to (4.1). The design of the MOV must meet various criteria. A typical voltage-current characteristic curve of a MOV can be seen in Fig. 4.5. The four operating areas and the most important values are emphasized. Initially, it is the normal operation region, which is determined by a DC voltage, V_{DC}, where the leakage current remains low. The second region is called leakage current region and it is determined by the leakage current. This area extends until the leakage current reaches $1mA$. After that point, the MOV's current starts increasing drastically with a small rise of the voltage. Once the voltage reaches the clamping voltage V_{cl}, the transient operating region ends. At that point, the current is defined as I_{pk}. The last region, i.e. surge current region, starts once the voltage becomes higher than the MOV clamping voltage.

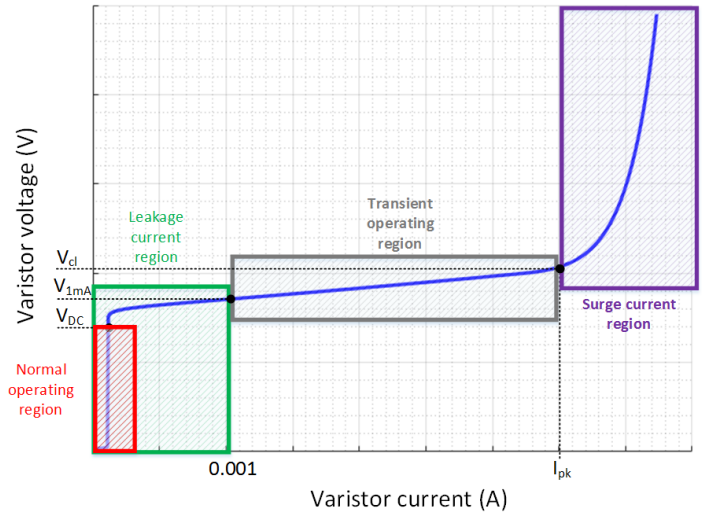


Figure 4.5: Characteristic curve of an MOV.

The choice of an MOV for CON1 should be made by considering all previous parameters. Initially, the normal operating region must be ensured for the MOV when the breaker is OFF. This implies that the V_{DC} should be higher than the DC voltage of the grid. Furthermore, the clamping voltage must be chosen such that it will keep the voltage across the semiconductor device below its blocking voltage V_{bl}. In other words, V_{cl} must be significantly lower than V_{bl} of the IGBTs. The clamping voltage is referring to a specific current I_{pk} and therefore, this must also be chosen to be in the same range with the anticipated fault current. The last two parameters that need to be considered are the peak pulse current of an MOV and the MOV's pulse energy dissipation capability at given currents. It must be ensured that the anticipated fault current will not be higher than the peak pulse current, and that the energy dissipation in the MOV will be within the given energy limit.

CON1 is a simple circuit, but it has several drawbacks. Firstly, the stray inductance in the MOV path $L_{\sigma MOV}$ can cause high voltage spikes which eventually can be catastrophic for the semiconductor devices [67]. This occurs due to the high di/dt during the current commutation from the switch to the MOV. Therefore, the device will experience a voltage higher than the clamping voltage of the MOV that is equal to $L_{\sigma MOV} \cdot di/dt$. One solution to that is to reduce di/dt, which can be done by means of tuning the gate drive circuit of the IGBT. However, this reduction leads to longer current falling times, and thus, the power dissipation in the device during turn-OFF will increase significantly. This might cause thermal damages to the semiconductor device. Finally, possible ringing between the MOV stray inductance and devices' stray capacitances may also occur leading to undesired triggering of the switch.

4.3.2 Design principles of CON2

The second investigated overvoltage suppression configuration CON2 is shown in Fig. 4.1(b). The snubber circuit is used for the protection of the semiconductor devices from overvoltage, as well as for the energy dissipation which is stored mostly in the current limiting inductor. The use of a snubber capacitor connected in parallel to the IGBT aims at controlling the voltage rise across the device, dv_{sw}/dt. This also minimizes the thermal stress of the switches due to the soft switching process. The snubber capacitance C_{sn} must be chosen based on both the dv_{sw}/dt criterion and the value of the peak line current. The higher the snubber capacitance is, the lower the dv_{sw}/dt becomes according to the following equation.

$$I_{sn} = C_{sn}\frac{dv_{sw}}{dt} \tag{4.2}$$

where I_{sn} is the commutation current from the IGBT path to the snubber circuit.

However, the increase of the capacitance results in longer time for the snubber capacitor to be fully charged and hence, the line short-circuit current increases further. The snubber capacitance C_{sn} will be then given based on the energy conservation law, as follows.

$$C_{sn} = \frac{L_s I_{sc_{max}}^2}{(V_{sn_{max}} - V_{DC})^2} \tag{4.3}$$

where, $V_{sn_{max}}$ and V_{DC} are the snubber capacitor voltage and the voltage of the DC grid respectively and $I_{sc_{max}}$ is the peak short-circuit current. Besides the snubber capacitance, the snubber resistance must also be chosen properly. This resistance provides a discharging path to the snubber capacitor as shown in Fig. 4.3(e). Therefore, it can be designed in order to damp any oscillations between the snubber capacitor C_{sn} and the current limiting inductor L_s [O1]. The following criterion then must be met.

$$R_{sn} \geq 2\sqrt{\frac{L_s}{C_{sn}}} \tag{4.4}$$

If the snubber resistance becomes significantly higher than this, it will take longer time for the snubber capacitor to be fully discharged. The result is that the breaker will not be able to reclose shortly after its turning-OFF operation, which might be required in several cases (e.g. temporary fault incident, deactivation of a line in a multi-terminal DC grid etc). At last, although the snubber circuit introduces stray inductance in the MOV path similarly to CON1, the impact of this inductance on the IGBTs overvoltage is negligible due to the presence of the snubber capacitor. Additionally, the snubber diode should have high surge current capability.

4.3.3 Design principles of CON3

The last investigated overvoltage suppression configuration CON3 is a combination of the two previous configurations. It consists of an RCD snubber circuit and an MOV as shown in Fig. 4.1(c). The snubber circuit provides soft switching of the semiconductor devices by controlling the voltage rise during the turn-OFF process similar to CON2. However, the magnetic energy stored in the current limiting inductor is no longer needed to be fully dissipated in the snubber capacitor, but this can be done in the MOV. This leads to the use of lower snubber capacitance compared to CON2. The only criterion that should be fulfilled is the du_{sw}/dt, and therefore the required capacitance must be given by (4.2). On the other hand, the impact of the stray inductance in the MOV path on the voltage across the semiconductor devices is minimized in CON3 compared to CON1. The reason is that

the fault current is not commutated directly from the semiconductor devices to the MOV as in CON1, but it commutates firstly to the snubber circuit and then to the MOV. This leads to smoother current commutation to the MOV and therefore, the anticipated voltage spike due to the MOV stray inductance is kept low.

Besides the snubber capacitance, the snubber resistance, as well as the snubber diode must be designed similarly to CON2. Additionally, the MOV must be chosen according to Fig. 4.5 in the same manner as described in the CON1. A summary of the advantages and disadvantages of the three investigated overvoltage configurations are summarized in Table 4.1.

4.4 Performance evaluation of the three overvoltage suppression circuits

The performance of the three overvoltage suppression configurations, CON1, CON2 and CON3 has been assessed by using simulations and experiments. The simulation study has been performed using high-power solid-state circuit breakers for MVDC grids, while the experimental validation was conducted on a down-scaled prototype for medium-power LVDC and MVDC breakers. Matlab/Simulink has been used for the modelling and simulation studies. The evaluation criteria are the requirements for passive components, as well as the performance during a breaking operation of each overvoltage suppression configuration. This performance concerns the short-circuit current, the switch voltage and the fault clearance time.

4.4.1 Simulation results for high-power MVDC solid-state breakers

The DC grid utilizing CON1, CON2 and CON3 is illustrated in Fig. 4.1. The DC voltage has been set to $1.8kV$, and the rest of parameters can be seen in Table 4.2. The threshold current I_{thres} is the current that trips the breaker and the turn-OFF

Table 4.1: Comparative evaluation of CON1, CON2 and CON3

Configuration	Advantages	Disadvantages
CON1	Simple circuit Short fault clearance time	High voltage spike due to MOV stray inductance Possible ringings between stray inductances and capacitances Thermal stress of the switch No dv_{sw}/dt control
CON2	No thermal stress of the switch dv_{sw}/dt control No ringings	High total short-circuit current Long fault clearance time Need for high snubber capacitance Need for snubber resistor during the snubber capacitor discharge Need for diode with high surge current capability
CON3	No thermal stress of the switch dv_{sw}/dt control Low voltage spikes Need for low snubber capacitance	Long fault clearance time Need for snubber resistor during the snubber capacitor discharge Need for diode with high surge current capability Possible ringings between stray inductances and capacitances

Table 4.2: Parameters of the simulated $1.8kV_{DC}$ grid and the utilized MOV

Parameter	Symbol	Value	unit
Load current	I_{load}	500	A
Line inductances	L_1, L_2	0.1	μH
Threshold current	I_{thres}	1	kA
Turn-OFF delay	t_{delay}	2	μs
Maximum allowable current	$I_{sc_{max}}$	1.2	kA
Voltage of MOV at $1mA$ DC current	V_{1mA}	1.95	kV
Clamping voltage of MOV	V_{cl}	2	kV
MOV current at V_{cl}	I_{pk}	200	A
MOV stray inductance	$L_{\sigma MOV}$	500	nH

Table 4.3: Comparative results of CON1, CON2 and CON3 with respect to the passive components requirements

Configuration	L_s $[\mu H]$	C_{sn} $[\mu F]$	$P_{R_{sn}}$ $[kW]$	$\int I^2 dt$ $[A^2 s]$	E_{mov} $[J]$
CON1	34.2	-	-	-	282
CON2	34.2	100	1500	954	-
CON3	34.2	10	14	31.5	433

delay time t_{delay} is the time delay due to communication, sensing etc, which has been set to $2\mu s$ [65]. Additionally, the maximum allowable current $I_{SC_{max}}$ is the current that L_s must be designed for according to (4.1). A $4.5kV$ and $1.3kA$ IGBT (ABB 5SNA1300K450300) has been considered for the modelling in all cases.

The first comparison is related to the required passive components of each configuration. According to the previous analysis and considering the parameters shown in Table 4.2, the requirements for passive components in the three configurations are summarized in Table 4.3. The current limiting inductor has been designed in the similar manner for all configurations, and therefore it is equal. On the other hand, it can be clearly seen that the snubber capacitance in CON3 is ten times lower compared to CON2. Additionally, the power requirements for the snubber resistor, as well as the snubber diode are higher in CON2 than in CON3. The main reason for that is the anticipated higher short-circuit current, which will be presented below. Finally, the energy dissipation in MOV in CON1 is lower compared to CON3 due to the lower short-circuit current in CON1.

The various currents of the DC grid during the short-circuit clearance interval and the switch voltage in CON1 are illustrated in Fig. 4.6. The total current (Fig.

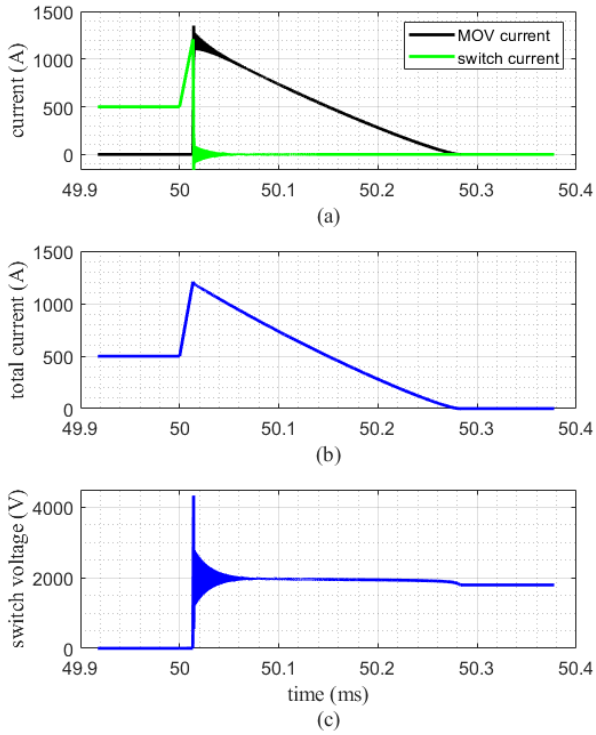


Figure 4.6: Simulation results for the CON1 during the short-circuit: (a) MOV and switch currents, (b) total short-circuit current, and (c) switch voltage.

4.6(b)) equals the sum of the switch current (green line in Fig. 4.6(a)) and the MOV current (black line in Fig. 4.6(a)). The oscillations caused by the stray inductances (mostly by $L_{\sigma MOV}$) and the IGBT stray capacitances can be seen. These oscillations might accidentally retrigger the IGBT and thus, a sophisticated gate driver design must be made. The use of active Miller clamp circuits in the GDU is an example of such a sophisticated driver. The high peak overvoltage can also be observed in Fig. 4.6(c), which is caused by the rapid IGBT current decrease during turn-OFF along with the $L_{\sigma MOV}$.

Fig. 4.7 depicts the various currents and switch voltage in CON2. Similarly to the previous case, the total current (Fig. 4.7(b)) equals initially the switch current (green line in Fig. 4.7(a)) and later the snubber current (red line in Fig. 4.7(a)). The long clearance time and the high peak fault current can be clearly observed. On the other hand, the voltage rise is smoother compared to CON1.

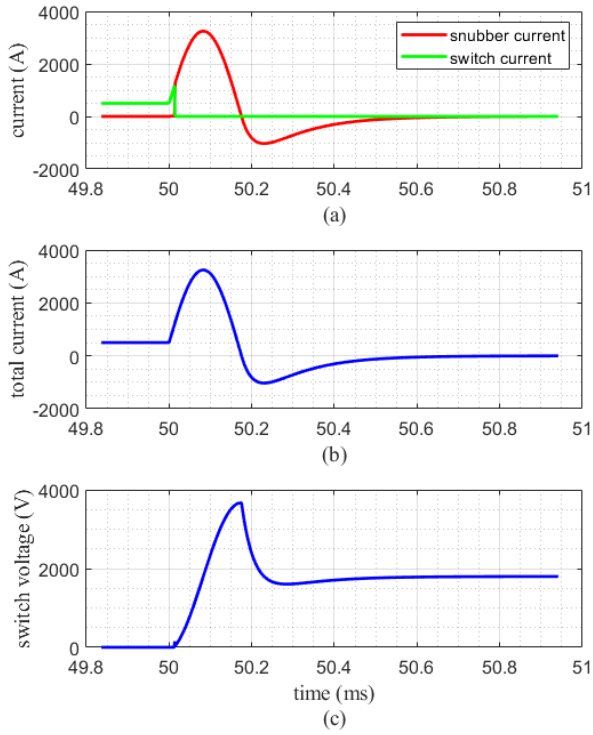


Figure 4.7: Simulation results for the CON2 during the short-circuit: (a) snubber and switch currents, (b) total short-circuit current, and (c) switch voltage.

The results for the last overvoltage suppression configuration, CON3, are shown in Fig. 4.8. The current commutates initially from the switch to the snubber circuit and later to the MOV branch as illustrated in Fig. 4.8(a). Furthermore, the rate of voltage rise remains low and the fault is cleared within less than $0.5ms$.

The numerical results of the electrical performance of the three overvoltage configurations during a fault clearance are summarized in Table 4.4. The short-circuit current reached the highest value in CON2 due to the high snubber capacitance. This current is approximately $3.3kA$, while in case of CON1 and CON3, the corresponding current reached $1209A$ and $1543A$, respectively. Additionally, CON1 exhibits the highest switch voltage, as well as the highest switch voltage rise during turn-OFF. In particular, the voltage reached around $4.3kV$ and the dv_{sw}/dt was $8kV/\mu s$. Finally, the lack of a snubber capacitor in CON1 led to the shortest fault clearance time that equals $280\mu s$.

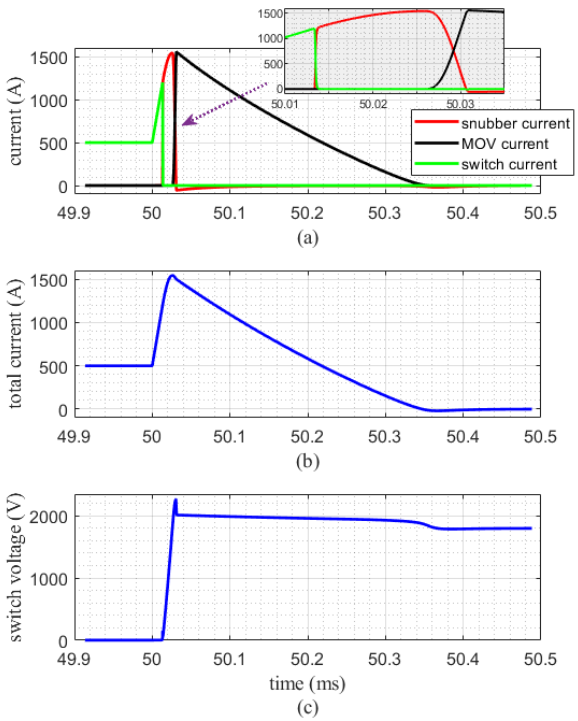


Figure 4.8: Simulation results for the CON3 during the short-circuit: (a) snubber, MOV and switch currents, (b) total short-circuit current, and (c) switch voltage.

Table 4.4: Simulation results of CON1, CON2 and CON3 during breaking operation

Configuration	$I_{sc_{peak}}$ $[A]$	$V_{sw_{peak}}$ $[V]$	dv_{sw}/dt $[V/\mu s]$	t_{cl} $[ms]$
CON1	1209	4332	8000	0.280
CON2	3246	3667	32	1.031
CON3	1543	2265	150	0.475

Impact of $L_{\sigma MOV}$ on the performance of CON1, CON2 and CON3

The impact of $L_{\sigma MOV}$ on the switch peak voltage in the three simulated cases is shown in Fig. 4.9. It is observed that in CON1, when $L_{\sigma MOV}$ increases from $100nH$ to $700nH$, the switch voltage rises drastically from $2850V$ to $4850V$. On the other hand, in CON3, the corresponding switch voltage increase for the same $L_{\sigma MOV}$ change, is much lower, i.e. from $2110V$ to $2330V$. It can be concluded that in MVDC applications, where the space requirements are more strict (to ensure sufficient voltage isolation), CON1 might not be a feasible solution.

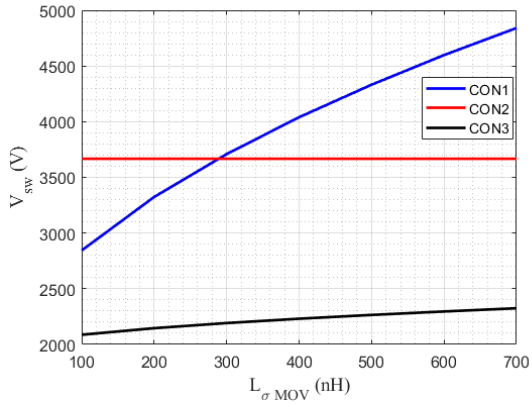


Figure 4.9: Impact of the MOV stray inductance on the switch peak voltage for all the investigated configurations.

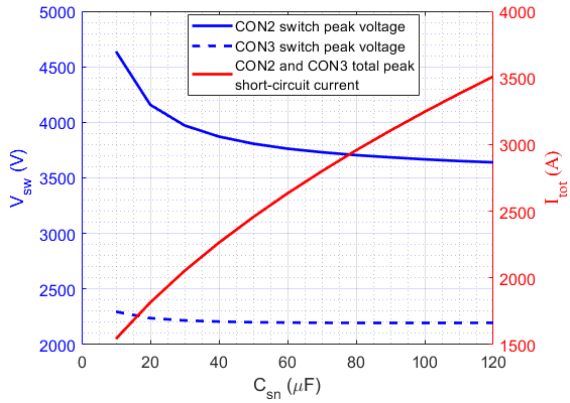


Figure 4.10: Impact of the snubber capacitance on the switch peak voltage and total peak short-circuit current.

Impact of C_{sn} on the performance of CON1, CON2 and CON3

Except of CON1, the two other overvoltage suppression configurations include snubber circuits. The impact of the snubber capacitance on the peak switch voltage, and on the fault current is shown in Fig. 4.10. It can be seen that in CON2, the switch peak voltage is kept low at high snubber capacitances at a cost of high short-circuit current. On the other hand, the snubber capacitance in CON3 can be significantly lower, achieving at the same time low fault current. This draws the conclusion that the CON2 is not a feasible solution in LVDC and MVDC applications where sensitive to high current equipment is connected (e.g. VSCs).

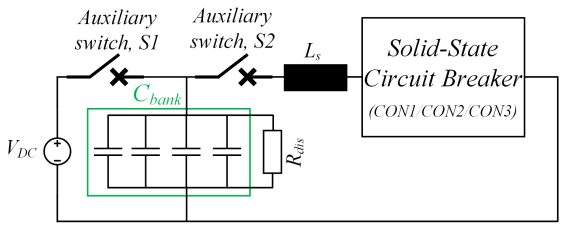


Figure 4.11: Schematic diagram of the test circuit.

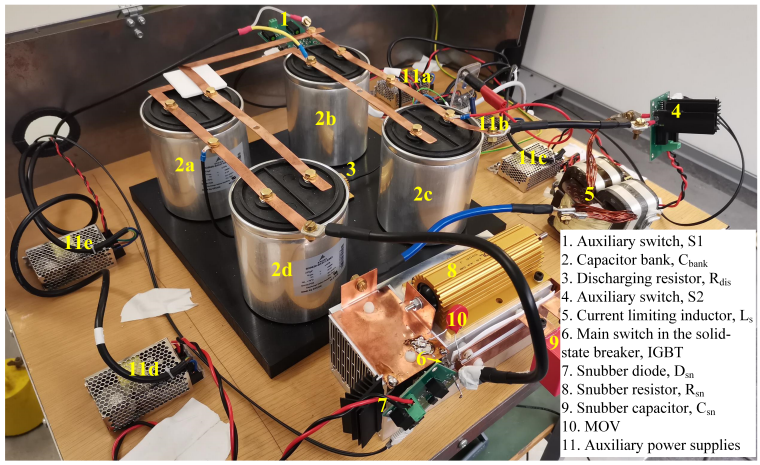


Figure 4.12: Photograph of the experimental solid-state breaker prototype using CON3.

4.4.2 Experimental results for medium-power LVDC and MVDC solid-state breakers

A down-scaled experimental prototype was built in order to validate the theoretical and simulation findings from the comparative evaluation of the three overvoltage suppression configurations. The schematic diagram of the test circuit is illustrated in Fig. 4.11. A photograph of the lab prototype is depicted in Fig. 4.12. Although the solid-state breaker depicted in this photo employes CON3, the test setup is easily reconfigurable and can accommodate CON1 and CON2. Two auxiliary switches S_1 and S_2 have been used. The first one, S_1, controls the charge of the capacitor bank C_{bank} which is fed by a DC voltage source V_{DC}. The second auxiliary switch S_2 is used to block the charging of the snubber capacitor before the breaker operation. The performed test is a single-pulse test, where proper pulses are provided to the gates of the two auxiliary switches and the main switch of the solid-state breaker. The time duration of the pulse given to S_2 determines the desired turn-OFF current of the breaker. This time duration has been set to $20\mu s$ for

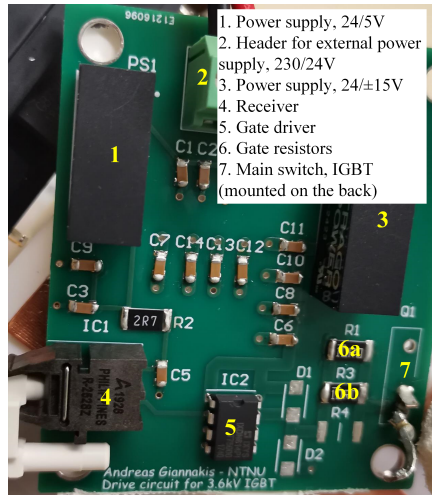


Figure 4.13: Photograph of the gate drive unit.

all investigations. On top of that, three high-voltage and medium-power IGBTs encapsulated in discrete packaging technology, rated at $3.6kV$ and $50A$ (IXYS IXBX50N360HV, technology of BiMOSFET) have been used for the realization of the two auxiliary switches, as well as for the main switch employed in the solid-state breaker. Fig. 4.13 shows the GDU which has been designed to drive the IGBT in the main switch. In addition, two more GDUs, of a similar design have been used to drive the auxiliary switches S_1 and S_2. The parameters of the GDU can be found in Table 4.5. In addition, the design and operating parameters of the test circuit and the lab prototype are summarized in Table 4.6. The solid-state breaker operation employing the three overvoltage configurations have been tested under three input voltages, V_{DC}. In particular, $700V$ has been initially used to represent LVDC solid-state breakers, and then $1100V$ and $1500V$ were considered to represent MVDC breakers.

Table 4.5: Design parameters of the gate drive unit

Parameter/Component	Value
Power supply, $24/5V$	Traco, TMR 3-2411
Power supply, $24/\pm 15V$	Traco, TMR 3-2423
External power supply, $230/24V$	Traco, TXM 015-124
Gate driver	IXYS, IXDN614PI
Receiver	Broadcom/Avago, HFBR-2528Z
Gate resistors, R_{g1}, R_{g2}	10Ω

Table 4.6: Parameters of the experimental setup

Parameter/Component	Value
Auxiliary switches, S_1, S_2	IXYS, IXBX50N360HV
Input voltage, V_{DC}	$700 - 1500V$
Capacitor bank, C_{bank}	$860\mu F$
Discharge resistor, R_{dis}	$47k\Omega$
Current limiting inductor, L_s	$660\mu H$
Main switch in solid-state CB, IGBT	IXYS, IXBX50N360HV
Snubber diode, D_{sn}	GeneSiC, GB25MPS17-247
Snubber resistor, R_{sn}	500Ω
Snubber capacitor, C_{sn}	$0.15 - 2\mu F$
Metal-Oxide Varistor, MOV	V1000LA160BP

Experimental results employing CON1

The switching performance of the solid-state breaker employing CON1 when the DC voltage was set to $1500V$ is illustrated in Fig. 4.14. This figure shows the line current (purple line), the main switch current (green line), the MOV current (light blue line), and the main switch voltage (blue line) during a fault clearance process. The switch voltage reaches $2.18kV$ at peak line current of $44A$. The voltage rise during the IGBT's turn-OFF has been measured to be $13.5kV/\mu s$. This can cause oscillations due to the switch stray capacitances, and eventually switch mistriger-rings. However, the used IGBT encapsulated in discrete packaging leads to lower stray capacitances compared to high-power modules and therefore, a mistriggering is less likely to occur. Additionally, it should be noted that the considered IGBTs exhibit long current falling times, and hence the impact of the stray inductance in the MOV path cannot be seen in the results. In contrast to them, the high-power semiconductor modules can achieve one or even two orders of magnitude higher turn-OFF speed, and then the impact of the MOV stray inductance on the switch voltage is being severe as shown in the simulations. Moreover, the thermal stress of the main IGBT in terms of switching energy during the breaking operation has been measured to be $41mJ$. Finally, the solid-state breaker managed to interrupt the line current within $130\mu s$ from the time instant that the main IGBT has received the command to turn-OFF.

Table 4.7 summarizes the experimental results for the three investigated voltage levels when CON1 is employed in the solid-state breaker. Since the pulse duration of the S_2 remains constant, it is observed that the turn-OFF currents change proportional to the DC voltage.

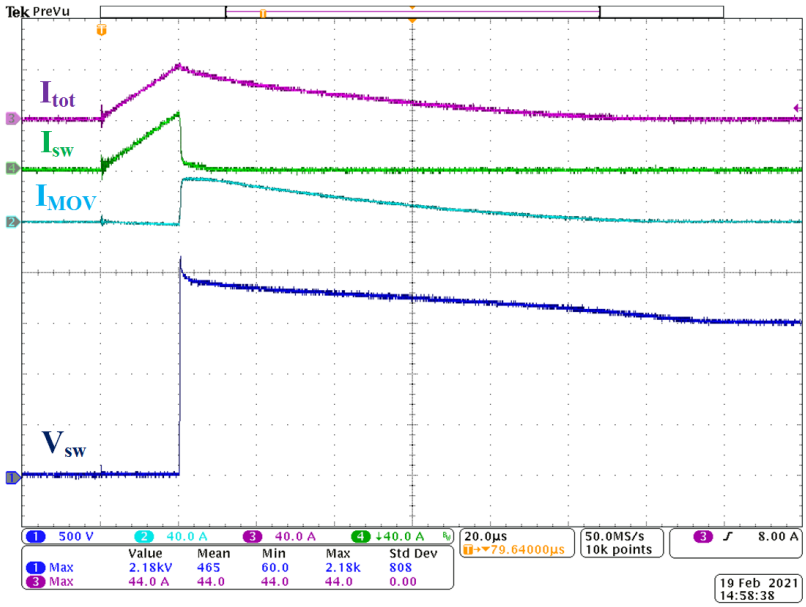


Figure 4.14: Experimental results for the CON1 at $1500V_{DC}$ and $44A$ turn-OFF current. Measured line current (purple line, 40A/div), IGBT current (green line, 40A/div), MOV current (light blue line, 40A/div), and IGBT voltage (blue line, 500V/div), (time base $20\mu s$/div).

Table 4.7: Experimental results for CON1

V_{DC} $[V]$	$V_{sw_{peak}}$ $[kV]$	$I_{tot_{peak}}$ $[A]$	dv_{sw}/dt $[kV/\mu s]$	E_{sw} $[mJ]$	t_{cl} $[\mu s]$
700	2.04	21.2	7.5	16.8	16
1100	2.10	33.2	11	21	31
1500	2.18	44	13.5	41	130

Experimental results employing CON2

The experimental results when CON2 is used are shown in Figs. 4.15-4.18. Fig. 4.15 illustrates the line current (purple line), switch current (green line), snubber capacitor current (light blue line) and the switch voltage (blue line) during a breaker operation. The snubber capacitance and the DC voltage have been set to $1\mu F$ and $1500V$, respectively. As observed, the switch voltage rises slowly due to the presence of the capacitor, and it reaches a peak value of $3.25kV$, which is close to the blocking voltage of the employed IGBT. This also leads to high line current, which equals $71.2A$. In addition, the line current crosses the zero point $65\mu s$

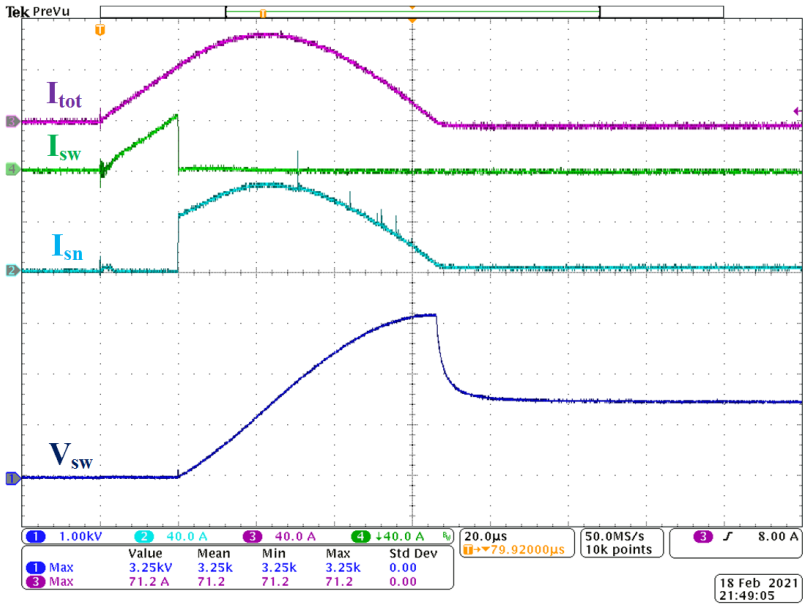


Figure 4.15: Experimental results for the CON2 at $1500V_{DC}$ and $71.2A$ turn-OFF current with $C_{sn} = 1\mu F$. Measured line current (purple line, 40A/div), IGBT current (green line, 40A/div), snubber capacitor current (light blue line, 40A/div), and IGBT voltage (blue line, 1kV/div), (time base 20μs/div).

after the pulse in S_2 which denotes the beginning of the short-circuit fault. Then, the snubber capacitor discharges and feeds power back to the capacitor bank. The fault clearance time is considered as the time instant that the current crosses the zero point for the first time. Finally, the IGBT in the breaker experiences almost zero switching energy due to the snubber capacitor and thus the soft switching.

The impact of the snubber capacitance on the switch voltage, as well as on the line current during a breaker operation has also been investigated experimentally. Figs. 4.16, 4.17 and 4.18 show this impact for the three DC voltage levels, i.e. $V_{DC} = 700V$, $V_{DC} = 1100V$ and $V_{DC} = 1500V$. It can be seen that the increase of the snubber capacitance leads to a significant line current rise, whereas the switch voltage drops. However, after a certain capacitance value, the voltage drop is no longer significant. This holds true almost for all three investigated voltage levels. The difference is that in the case with $V_{DC} = 1500V$, when the snubber capacitance increases from $1.5\mu F$ to $2\mu F$, the switch voltage slightly rises instead of decreasing. The reason is the high current leading to high magnetic energy stored in the current limiting inductor, which eventually must be dissipated in the snubber capacitor.

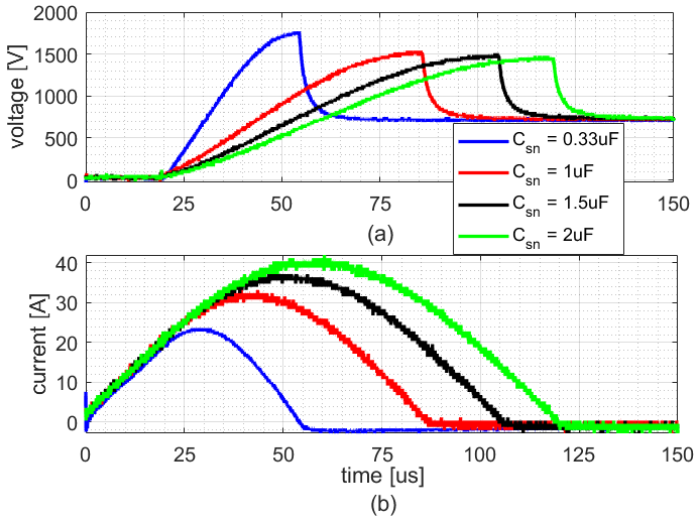


Figure 4.16: Experimental results for CON2 at $700V_{DC}$ with several snubber capacitances: (a) switch voltage, and (b) line current.

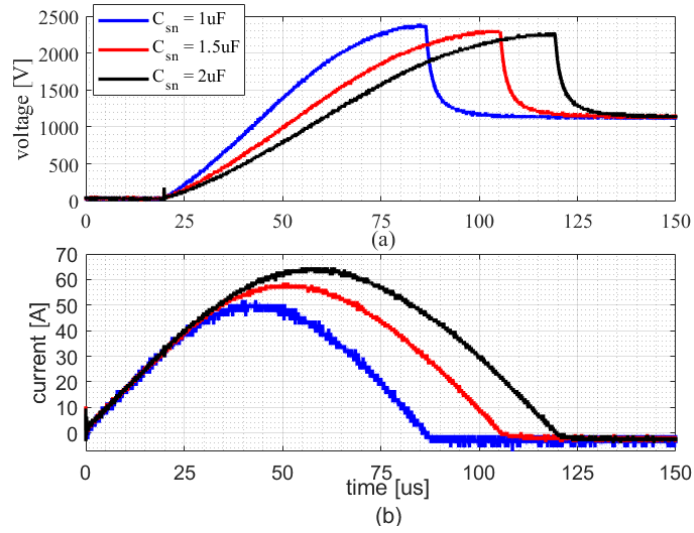


Figure 4.17: Experimental results for CON2 at $1100V_{DC}$ with several snubber capacitances: (a) switch voltage, and (b) line current.

Table 4.8 summarizes the experimental results for the three voltage levels, as well as for all the considered snubber capacitances in case of CON2. It is revealed that the choice of the snubber capacitance is critical, and therefore it must be selected

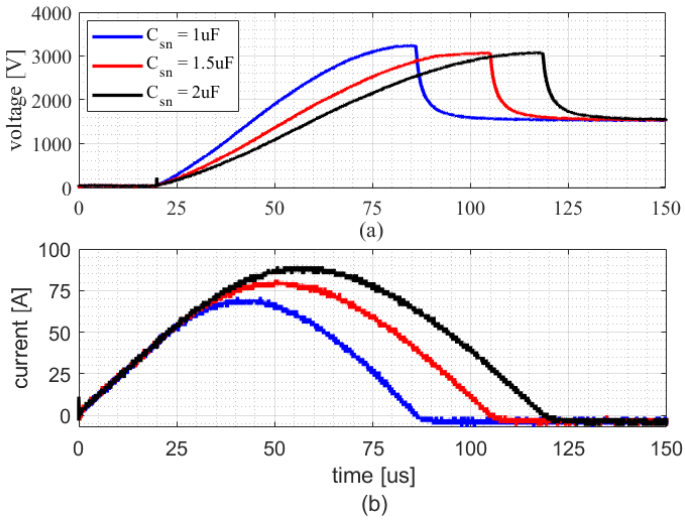


Figure 4.18: Experimental results for CON2 at $1500V_{DC}$ with several snubber capacitances: (a) switch voltage, and (b) line current.

according to the design and operating constraints of the specific application. For example, if the line current should be well limited, then the minimum snubber capacitance must be used and thus semiconductor devices with higher blocking voltages must be chosen. This increases the forward voltage of the devices causing higher conduction losses. On the other hand, if the losses of the semiconductors should be kept low, then a high snubber capacitance must be chosen. This imposes

Table 4.8: Experimental results for CON2

V_{DC} $[V]$	C_{sn} $[\mu F]$	$V_{sw_{peak}}$ $[kV]$	$I_{tot_{peak}}$ $[A]$	dv_{sw}/dt $[V/\mu s]$	E_{sw} $[mJ]$	t_{cl} $[\mu s]$
700	0.33	1.77	23.6	70	~ 0	35
700	1	1.54	33.2	33	~ 0	65
700	1.5	1.51	38	24	~ 0	85
700	2	1.48	42	20	~ 0	100
1100	1	2.40	52	50	~ 0	65
1100	1.5	2.31	58.8	39	~ 0	85
1100	2	2.28	64.8	32	~ 0	100
1500	1	3.25	71.2	70	~ 0	65
1500	1.5	3.09	81.6	61	~ 0	85
1500	2	3.10	89.6	45	~ 0	100

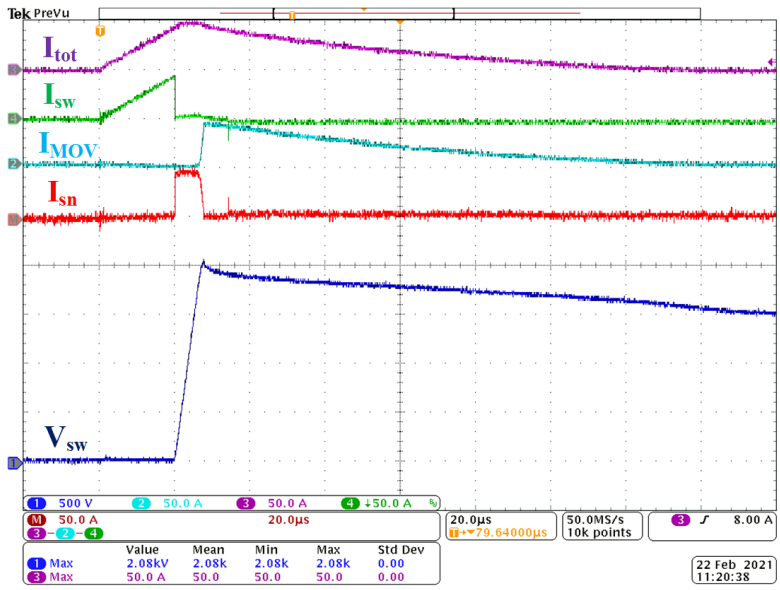


Figure 4.19: Experimental results for the CON3 at $1500V_{DC}$ and $50A$ turn-OFF current with $C_{sn} = 0.15\mu F$. Measured line current (purple line, 50A/div), IGBT current (green line, 50A/div), MOV current (light blue line, 50A/div), and IGBT voltage (blue line, 500V/div), (time base 20μs/div).

the use of semiconductor devices with lower blocking voltage capabilities. In that case though, the fault line current might reach very high values.

Experimental results employing CON3

For the performance evaluation of the solid-state breaker employing CON3, similar investigations with CON2 have been performed. Fig. 4.19 shows the experimental results when the DC voltage is set to $1500V$ and the snubber capacitance is equal to $C_{sn} = 0.15\mu F$. The switch voltage and the line current reached $2.08kV$ and $50A$ respectively. The rate of the switch voltage rise is also limited to $325V/\mu s$, which is significantly lower than CON1. Additionally, the switching energy is almost zero due to the presence of the snubber capacitor. Finally, the line current crosses the zero point for the first time $135\mu s$ after the activation of the single-pulse test. Similarly to CON2, the negative residual current that discharges the snubber capacitor is not taken into account for the fault clearance time.

Three snubber capacitors have been tested showing the impact of the capacitance on the line current, and switch voltage during a breaker operation. The snubber capacitances that have been used are $0.15\mu F$, $0.33\mu F$, and $1\mu F$. Figs. 4.20, 4.21 and 4.22 show the experimental results of the switch voltage and line current in

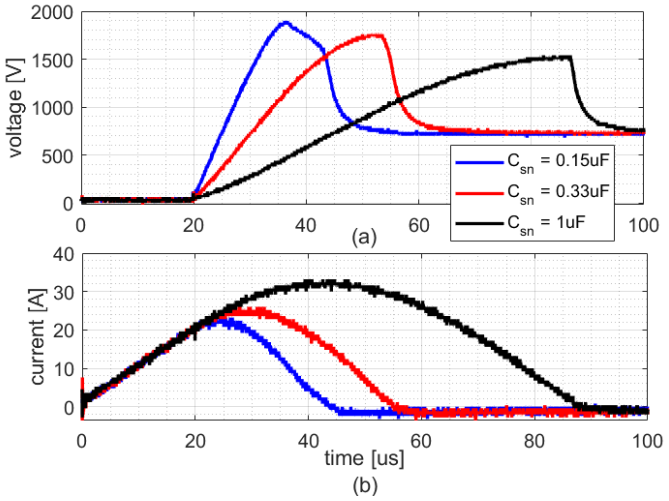


Figure 4.20: Experimental results for CON3 at $700V_{DC}$ with several snubber capacitances: (a) switch voltage, and (b) line current.

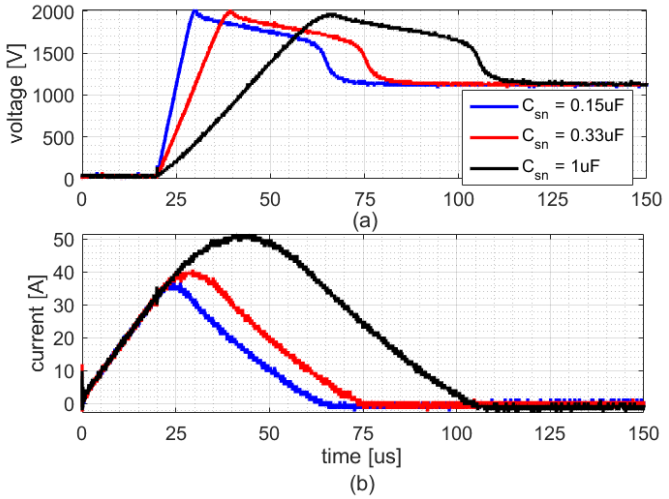


Figure 4.21: Experimental results for CON3 at $1100V_{DC}$ with several snubber capacitances: (a) switch voltage, and (b) line current.

case of $V_{DC} = 700V$, $V_{DC} = 1100V$, and $V_{DC} = 1500V$, respectively. It can be seen that the lowest snubber capacitance exhibits the best performance since the switch peak voltage remains constant due to the MOV activation for all considered capacitances, whereas the line current is kept the lowest at $0.15\mu F$. This

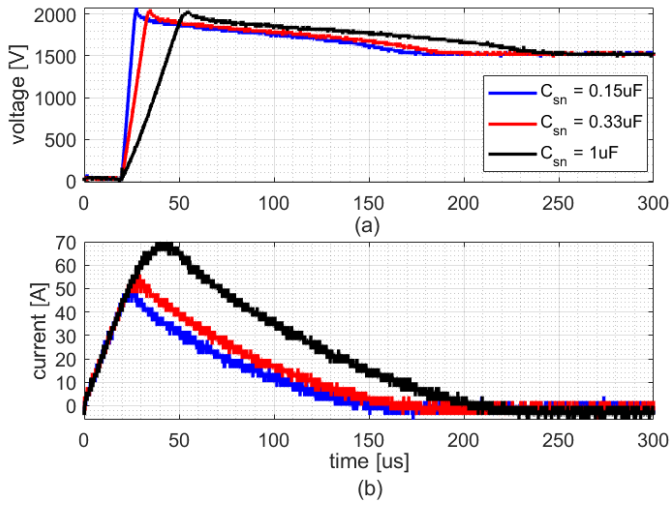


Figure 4.22: Experimental results for CON3 at $1500V_{DC}$ with several snubber capacitances: (a) switch voltage, and (b) line current.

conclusion can be clearly seen in cases of $V_{DC} = 1100V$, and $V_{DC} = 1500V$. In the $V_{DC} = 700V$ case, the MOV is not activated for any of the snubber capacitances and therefore, the performance is similar with CON2. Finally, the minimum snubber capacitance is limited by two factors; firstly the dv_{sw}/dt requirement, and secondly it should be high enough in order the switch current to be fully commutated to the snubber branch when the IGBT turns-OFF. The numerical results from the experimental investigations for all cases are summarized in Table 4.9.

Table 4.9: Experimental results for CON3

V_{DC} $[V]$	C_{sn} $[\mu F]$	$V_{sw_{peak}}$ $[kV]$	$I_{tot_{peak}}$ $[A]$	dv_{sw}/dt $[V/\mu s]$	E_{sw} $[mJ]$	t_{cl} $[\mu s]$
700	0.15	1.90	23.2	145	~ 0	23
700	0.33	1.76	26	75	~ 0	34
700	1	1.54	33.2	32	~ 0	68
1100	0.15	2.02	36.8	235	~ 0	40
1100	0.33	2.02	40.8	120	~ 0	52
1100	1	1.98	51.6	51	~ 0	83
1500	0.15	2.08	50	325	~ 0	135
1500	0.33	2.06	56	168	~ 0	150
1500	1	2.04	70	70	~ 0	183

4.5 Conclusions

This Chapter has presented three possible overvoltage suppression configurations for power semiconductor devices employed in solid-state breakers. Such circuits also dissipate the magnetic energy stored in the DC line and in the current limiting inductor during a fault clearing process. The first configuration, CON1, consists of an MOV branch connected in parallel to the main switch, the second one, CON2 employs an RCD snubber circuit and the last one, CON3 contains both MOV and RCD snubber circuit. The evaluation criteria were the passive components requirements, as well as the electrical performance of the three configurations by means of both simulations and experiments.

Even if CON1 requires only one passive element, the simulations in a $1.8kV_{DC}$ and $500A$ solid-state breaker revealed that this configuration is prone to switch overvoltages due to the MOV stray inductance. Additionally, the switch employed in the breaker with CON1 exhibited high switching energy during the breaker operation which can lead to thermal damages of the semiconductors. On the other hand, the simulation studies showed that CON3 can minimize not only the snubber capacitance compared to CON2, but also the switch voltage and the fault line current. The cost of the better performance of CON3 compared to CON1 is the higher requirements for passive components. Additionally, it has been verified that CON3 is immune to the stray inductance in the MOV path. Lastly, although CON2 managed to keep the switch voltage within acceptable limits, the high required snubber capacitance led to extremely high fault currents, as well as long fault clearance times.

The choice of the overvoltage configuration is critical and it must be made according to the design and operating constraints of the application that the solid-state breaker will be used. The factors that need to be considered are the cost, the circuit complexity, the load sensitivity, and the conduction losses. If the cost is of concern for the breaker's design, CON1 is the most suitable solution. On the other hand, if the conduction losses should be minimized, then CON3 may be used because it achieves the lowest peak switch voltage during a breaking operation. This imposes the use of semiconductor devices with lower blocking voltage capability, and thus, the forward voltage of these devices decreases, which causes lower conduction losses.

A down-scaled medium-power LVDC and MVDC solid-state breaker prototype employing the three overvoltage suppression configurations has been built and tested. The experimental results of the three circuits validated the findings from the simulation studies in three DC voltage levels, i.e. $700V$, $1100V$, and $1500V$.

Chapter 5

Series connection of IGBTs in solid-state MVDC breakers

This Chapter studies the voltage imbalances among series-connected IGBTs employed in MVDC solid-state circuit breakers. A hybrid method for voltage imbalance mitigation among series-connected IGBTs in such a breaker is proposed and analyzed. The aim of this method is the minimization of the required snubber capacitances by utilizing a magnetically coupled GDU for the IGBTs. The effectiveness of the proposed method is validated by simulations and experimental results.

Contributions

Several methods to mitigate voltage imbalances in series-connected IGBTs have been proposed in literature [68, 47, 69]. However, they mostly aim at switch-mode converters and thus, different design challenges may arise in case of solid-state breakers. The main contribution of this Chapter is a hybrid concept for the dynamic voltage-balancing for series-connected IGBTs employed in a solid-state MVDC breaker. The proposed method consists of RCD snubber circuits and a gate driver with an integrated gate current balancing scheme based on mutually coupled magnetic inductors. The goal of the proposed scheme is the minimization of the required bulky snubber components keeping the switch peak voltage low when the breaker turns-OFF, at a cost of a more complex gate drive circuit design. The minimization of the snubber circuits leads to minimization of the total volume, cost and weight of the breaker which becomes critical to weight-sensitive applications. The content of this Chapter summarizes two publications [P7, P9].

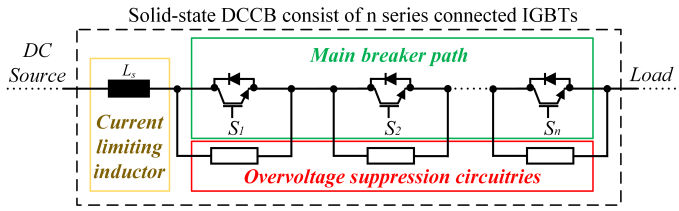


Figure 5.1: Basic schematic circuit of an interrupting solid-state MVDC breaker.

5.1 Voltage imbalances among series-connected IGBTs

An MVDC grid usually operates at a voltage level that is between $1kV$ to $35kV$ [8] or even up to $70kV$ [58]. However, the highest breakdown voltage of a single commercial high-voltage IGBT module equals $6.5kV$. Therefore, series connection of several IGBTs might be required for designing a solid-state MVDC breaker as shown in Fig. 5.1. This increases the circuit design and operating complexity. A critical design challenge of series-connected IGBTs is the balancing of the blocking voltages during the turn-OFF process (dynamic balance) and during the OFF-state (static balance) [70]. The dynamic imbalance normally occurs due to either IGBT device parameters spread (e.g. threshold voltage and stray capacitances) or possible gate drive delays among the series-connected IGBTs. These voltage imbalances might also lead to device failures, i.e. overvoltages. Additionally, the static voltage imbalances are normally caused due to differences in the semiconductors characteristics, such as leakage resistance. These voltage mismatches in series-connected IGBTs may be mitigated easily by connecting high-value resistors R_s, in parallel to the semiconductors. The value of this resistor should be approximately 10% of the OFF-state resistance of the IGBTs [71].

This Chapter focuses on mitigating transient voltage mismatches among series-connected IGBTs when unsynchronized gate voltages are fed to the devices during a turn-OFF process. The early turned-OFF IGBT is expected to experience the highest voltage among the other series-connected devices. The gate signal delays can occur for several reasons, such as uneven stray inductances in gate loops due to the physical layout design of the GDUs. Besides that, possible communication or coordination time delays may occur and affect the gate signal delays, which will eventually cause voltage imbalances during a breaking operation.

5.2 Voltage-balancing methods for series-connected IGBTs

The proposed solutions for voltage balancing in series-connected IGBTs can be classified into three categories; (i) passive snubber circuits, (ii) active gate control circuits and (iii) voltage clamping circuits. Passive snubber circuits are robust, but

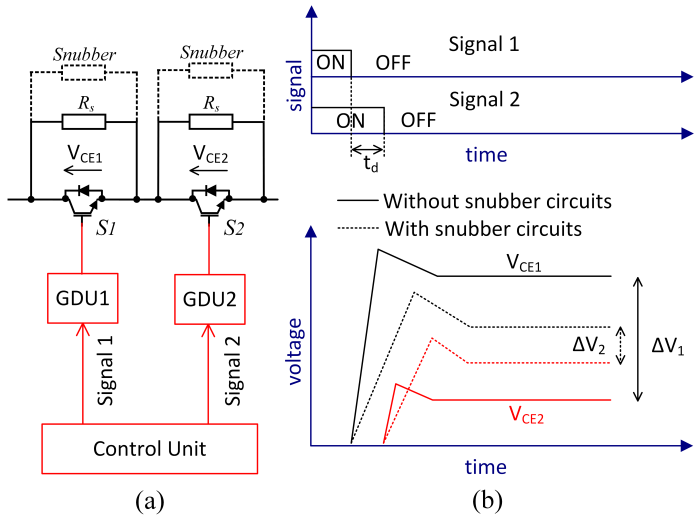


Figure 5.2: Block diagrams showing: (a) two series-connected IGBTs with GDUs, static resistances and snubber circuits, and (b) gate signals of the two IGBTs along with their voltages with and without snubber circuits.

their design is bulky and costly. Active gate control circuits can share the voltage among the devices sufficiently at a cost of increased complexity and thus the reliability is decreased. In particular, they require high-speed and high-precision electronic circuitries, such as sensors in order to detect voltage differences of the devices during the turn-OFF process. Finally, voltage clamping circuits require several additional components, such as high-voltage Zener diodes and capacitors and therefore, the complexity, as well as the volume, weight and cost of the system increase. Their performance however, can be robust and accurate. The three solutions for dynamic voltage balancing are analyzed below.

5.2.1 Passive snubber circuits

Passive snubber circuits use capacitors in order to provide smooth voltage rise during the turn-OFF of the IGBTs. Besides the bulky and costly use of snubber capacitors, they also cause increased line currents, as well as long IGBTs turn-OFF times which eventually limit the switching frequency of the devices. However, the last drawback is not critical when the semiconductors are employed in solid-state breakers, due to the less frequent breaking operation.

The most common snubber circuit is the RCD configuration, which has also been analyzed as an overvoltage suppression scheme in Chapter 4. Fig. 5.2(a) shows two series-connected IGBTs S_1 and S_2 with static resistances R_s, and snubber circuits along with their GDUs. Additionally, in Fig. 5.2(b) the gate signals, as well

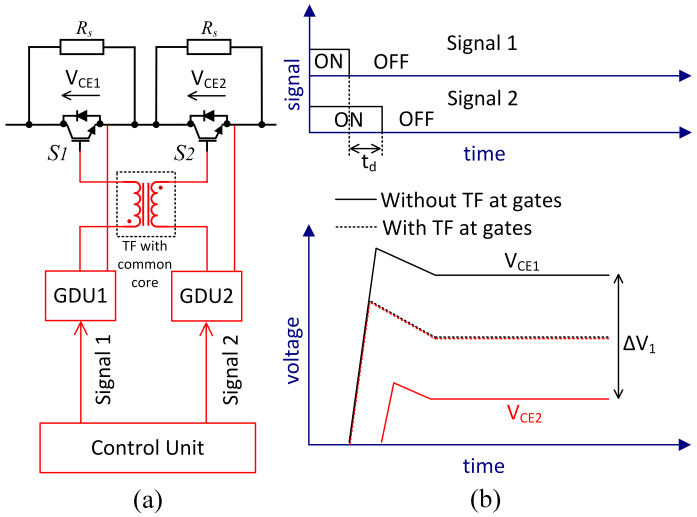


Figure 5.3: Block diagrams showing: (a) two series-connected IGBTs with magnetically coupled GDUs and static resistances and (b) gate signals of the two IGBTs along with their voltages with and without the gate coupled transformer.

as the collector-emitter voltages of the two switches V_{CE1} and V_{CE2} are depicted. It can be seen that a small gate propagation delay t_d has been introduced. In particular, signal 2 is delayed compared to signal 1 by t_d which leads to a delayed turn-OFF of S_2. The impact of the snubber circuits use on the IGBTs voltages is observed in the bottom waveforms in Fig. 5.2(b). The solid lines show the case without snubber circuits, and the dashed lines reveal the voltage imbalance mitigation by means of using the snubber circuits. In the first case, the early turned-OFF IGBT experiences a voltage of V_{CE1} and the voltage difference between the two switches is ΔV_1. However, when snubber circuits are employed, the corresponding difference decreases to ΔV_2. The higher the snubber capacitances are, the lower the voltage difference among the switches becomes for a given gate signal propagation delay. However, the high value capacitors cause high line currents as presented in Chapter 4, as well as they increase the cost, weight and the volume of the solid-state breaker.

5.2.2 Active gate control circuits

The challenge of eliminating bulky high-power passive components in snubber circuits can be tackled by driving the series-connected IGBTs using more sophisticated GDUs. Sasagawa et al. in [69] have proposed a robust active gate control method, namely gate-balancing core technique, as shown in Fig. 5.3(a). The output stages of the individual GDUs are magnetically coupled on a mutual core,

(transformer, TF, shown in Fig. 5.3) with the purpose of eliminating possible gate voltage propagation delays to the IGBTs. Fig. 5.3(b) shows the impact of the common core method. A balanced voltage sharing can be achieved (dashed lines), eliminating the voltage difference ΔV_1 between the two IGBTs. The robustness and the low cost and size are the key characteristic of this method, while a small slow down of the switching behavior can be seen as a drawback. Even though this might be crucial for the switch realization in a power electronics converter (i.e. slower switching results in higher switching losses), for a breaker design the switching speed of the power semiconductor devices is not a critical characteristic for the overall breaker performance. Therefore, the active gate control method with the core type for voltage-balancing in a solid-state breaker can be considered as a possible solution to voltage imbalance mitigation among series-connected IGBTs.

5.2.3 Voltage clamping circuits

The last voltage sharing method for series-connected high-power semiconductor devices is based on voltage clamping circuits. Several configurations have been proposed [72] and their majority utilizes high-power, high-voltage Zener diodes and high-voltage capacitors, connected normally between the gate and the collector terminals. The main idea of these concepts is that the device voltage is clamped at a certain level in order to prevent device breakdown. Although some proposed configurations are simple topologies and require few components, the main drawback is the additional high-voltage components used, which increase the cost and size and decrease the operating stability of the entire switch.

5.3 Proposed hybrid method for even voltage distribution in series-connected IGBTs for MVDC solid-state breakers

The use of snubber circuits for the voltage imbalance mitigation among series-connected IGBTs is a robust solution as explained previously at a cost of high line current, as well as of being bulky. Additionally, the use of a gate coupled transformer has been proven to enable an even voltage distribution among series-connected IGBTs at a cost of long turn-OFF times.

The proposed hybrid voltage-balancing method is based on the combination of RCD snubber circuits, MOV, and the gate coupled transformer. In this way, the required snubber capacitances are minimized and hence, they become less bulky, as well as less costly. The main reason for the snubber capacitance minimization is that the snubber circuits are used only for the current commutation and dv/dt control when the IGBTs turn-OFF. On the contrary, the even voltage distribution among the series-connected devices is achieved via the gate coupled transformer. The proposed scheme for voltage imbalance mitigation in a solid-state DC breaker

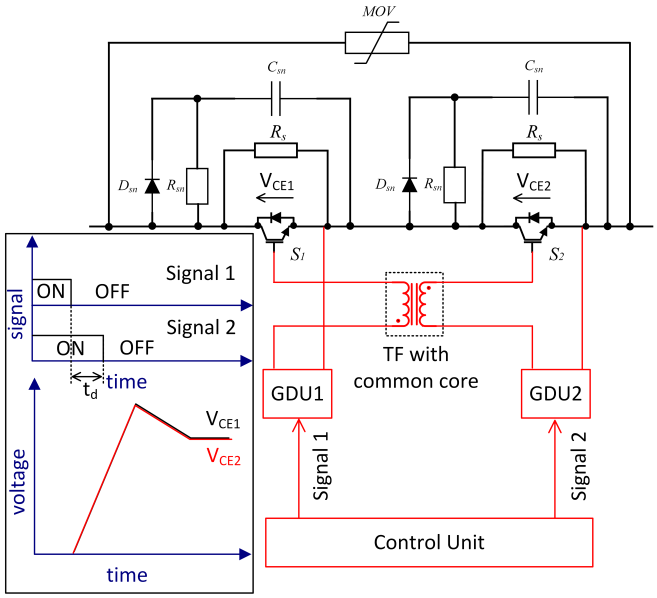


Figure 5.4: Schematic diagram of the proposed hybrid voltage-balancing scheme employed in a solid-state MVDC breaker comprising two series-connected IGBTs.

comprising two series-connected IGBTs is shown in Fig. 5.4. The anticipated voltages across an early and a late turned-OFF IGBTs (V_{CE1} and V_{CE2} respectively) during a breaking operation can also be seen in the same figure.

5.3.1 Design of the proposed hybrid voltage-balancing method

The minimization of the snubber capacitance results in minimization of the line current, as well as to the smaller size of the snubber circuit. Three configurations will be presented with respect to the required snubber capacitances and their expected breaking performance in order to emphasize the impact of the proposed method. The following parameters and limitations have been considered for all cases.

- Current limiting inductor, L_s has been designed using (4.1)
- Forward voltage of the snubber diode has been neglected. In addition to that, the equivalent series resistance of the snubber capacitor has also been neglected
- The rate of rise of the switch voltage during turn-OFF has been set as $\frac{dv}{dt}_{ref} \leq 500kV/ms$

- Gate signal propagation delay, t_d is in the range of $200 - 1000ns$
- MOV stray inductance, $L_{\sigma MOV}$ is in the range of $400 - 1000nH$
- Varistor clamping voltage, $V_{MOV} = 1.5 \cdot V_{DC}$
- Number of series-connected IGBTs is given by $N_s = \frac{V_{DC}}{2kV}$, where $2kV$ has been considered for the blocking voltage of each IGBT, V_{CEbl}. In particular, IGBT modules with voltage and current ratings of $4.5kV$ and $1300A$ have been considered.
- Maximum accepted voltage difference between the delayed IGBT(s) and the early turned-OFF IGBT(s) during the turn-OFF is $\Delta V_{CEref} \leq 10\% V_{CEbl} = 200V$
- Maximum load current equals $400A$, the threshold current is equal to $800A$ and the maximum allowable short-circuit current flowing through the IGBTs in the breaker is $I_{max} = 960A$
- Current falling time t_{fall} of the IGBT is set to $0.5\mu s$ at $960A$ of turn-OFF current

A. Configuration with RCD snubber circuit (RCD_{ref})

RCD snubbers control the voltage rise across the IGBTs during turn-OFF providing also a smooth fault current commutation to MOV. This leads to low di/dt and thus low switch overvoltage due to the stray inductance in the MOV path. Rearranging (4.2), the minimum required snubber capacitance for a given dv_{sw}/dt_{ref} is as follows.

$$C_{sn1} \geq \frac{I_{max}}{\frac{dv_{sw}}{dt}_{ref}} \tag{5.1}$$

Additionally, in series-connected IGBTs, the snubber circuits must also ensure an even voltage distribution during a breaker operation. According to this criterion, the required snubber capacitance for a given ΔV_{CEref} and t_d is the following.

$$C_{sn2} \geq \frac{I_{max}}{\frac{\Delta V_{CEref}}{t_d}} \tag{5.2}$$

It can be concluded that the maximum value of C_{sn1} and C_{sn2} must be considered for the design of the snubber capacitor in order to fulfill all the preset requirements. It can be seen that for almost the entire range of the given design parameters, (5.2) provides the highest minimum required capacitance (C_{sn2}). Therefore, the first investigated configuration, RCD_{ref} includes RCD snubber circuits where the capacitances are calculated based on the criteria analyzed above. The switch peak voltage of the early turned-OFF IGBT is then given by the following equation, taken into account the equivalent circuit shown in Fig. 4.4(f).

$$V_{CEpeak} = (V_{MOV} + \omega_{LC} L_{\sigma MOV} I_{max} + I_{max} R_{MOV} + \\ + I_{max} \frac{t_d}{C_{sn}}) \frac{1}{N_s} \tag{5.3}$$

with

$$\omega_{LC} = \frac{1}{\sqrt{L_{\sigma MOV} \frac{C_{sn}}{N_s}}} \tag{5.4}$$

where R_{MOV} is the resistance of the MOV.

B. Configuration with RCD snubber circuit and gate coupled transformer (Proposed configuration)

In the proposed configuration, the RCD snubber circuit is only used for controlling the voltage rise across the IGBTs during the turn-OFF and therefore, (5.1) should be considered. On the other hand, a possible gate signal propagation delay which causes uneven voltage distribution among the series-connected IGBTs can be dealt with the use of a gate coupled transformer, as shown in Fig. 5.4. The design of this transformer with respect to the magnetizing inductance L_m and the leakage inductance L_{leak} should fulfill the following criteria [69]:

$$L_m \geq \frac{t_d^2}{0.02 C_{ies}} \tag{5.5}$$

$$L_{leak} \leq \frac{R_g^2 C_{ies}}{1.96} \tag{5.6}$$

where C_{ies} is the input stray capacitance of an IGBT and R_g is the gate resistance.

Similar to the RCD_{ref} configuration, the peak voltage V_{CEpeak} of the early turned-OFF IGBT in the proposed method is as follows.

$$V_{CEpeak} = \frac{V_{MOV} + \omega_{LC} L_{\sigma MOV} I_{max} + I_{max} R_{MOV}}{N_s} \tag{5.7}$$

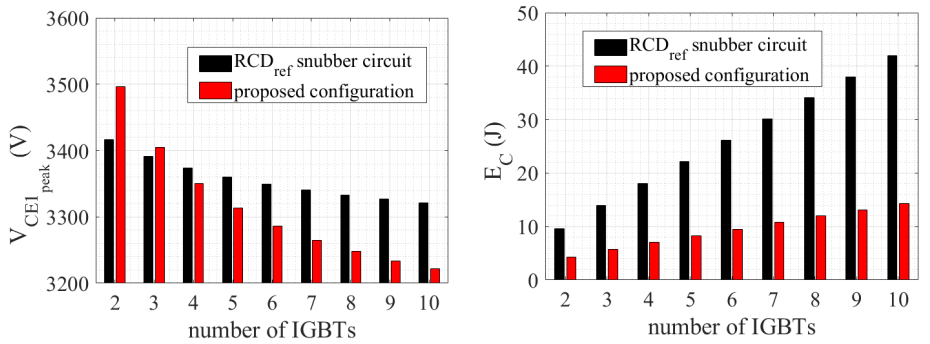
C. Comparative study between RCD_{ref} and proposed configurations

The impact of the proposed method for an even voltage distribution among series-connected IGBTs on the design requirements, as well as on the electrical performance is shown in Fig. 5.5. This figure shows the peak voltages of the early-turned-OFF IGBT, and the required energy storage capability of snubber capacitors for different number of series-connected IGBTs in both investigated configurations, i.e. RCD_{ref} and proposed. The snubber capacitances for the two configurations were calculated using (5.2) and (5.1). The worst-case scenarios at the given parameters have been considered for these calculations. These are $L\sigma_{MOV} = 1\mu H$, $\Delta V_{CEref} = 200V$, $I_{max} = 960A$ and $t_d = 1\mu s$. Therefore, for the RCD_{ref} configuration, the snubber capacitances have been calculated to be $4.8\mu F$, while in the proposed configuration, they are equal to $1.95\mu F$, leading to 60% capacitance reduction.

From Fig. 5.5(a), it can be seen that when the number of series-connected IGBTs is either 2 or 3, the switch peak voltage of the early turned-OFF device in RCD_{ref} is lower than in the proposed configuration. The cost is the higher line current during the breaker operation as it will be explained below. On the other hand, when the number of IGBTs increases, the switch voltage in the proposed method becomes lower than in RCD_{ref}.

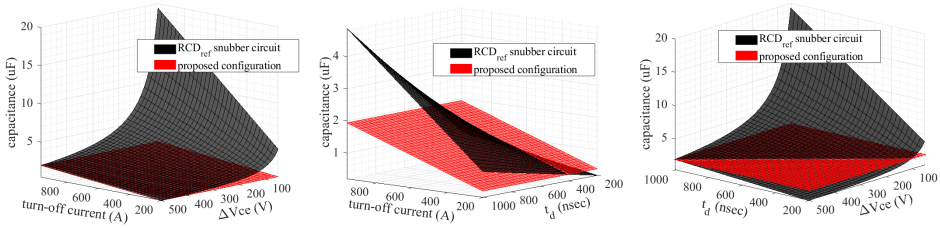
In Fig. 5.5(b), the total energy storage capability of all the snubber capacitors in both investigated configurations as a function of the number of series-connected IGBTs is illustrated. This along with the snubber capacitances are good indices for the capacitor size in terms of weight, volume and cost. The proposed method managed to reduce the energy storage capability compared to the RCD_{ref} configuration for the entire investigated number of IGBTs.

The previous analysis has considered the worst-case scenario with respect to $L\sigma_{MOV}$, ΔV_{CE}, I_{max} and t_d. The impact of the three last design parameters on the snubber capacitances choice in the RCD_{ref} and proposed configurations has also been investigated. Fig. 5.6(a) shows the required snubber capacitances in both configurations as a function of turn-OFF current and ΔV_{CE} at $V_{DC} = 4kV$ and $N_s = 2$. The minimization of the snubber capacitances in the proposed scheme



(a) **(b)**

Figure 5.5: Comparison between RCD_{ref} and the proposed configuration in terms of: (a) peak voltage of the early turned-OFF IGBT, and (b) total energy storage capability of snubber capacitors with respect to the number of series-connected IGBTs.



(a) **(b)** **(c)**

Figure 5.6: Comparison between RCD_{ref} and the proposed configurations for the required C_{sn} with respect to: (a) I_{max} and ΔV_{CE}, (b) I_{max} and t_d, and (c) t_d and ΔV_{CE}.

can be clearly seen for the entire investigated current and voltage difference ranges, especially when the desired ΔV_{CE} is kept low. Additionally, Figs . 5.6(b) and 5.6(c) show the required capacitances as a function of turn-OFF current, t_d and ΔV_{CE}. The increase of the gate signal propagation delay causes a higher snubber capacitance difference between the two investigated configurations. The reason is that in RCD_{ref} configuration, the snubber capacitance is proportional to t_d, while in the proposed scheme, the choice of C_{sn} is decoupled from t_d. It can be seen that when t_d is kept low (i.e. $< 400ns$), the proposed scheme does not minimize the snubber capacitance. However, the design of a solid-state breaker employing series-connected IGBTs should always consider the worst-case scenario, which means the longest possible t_d.

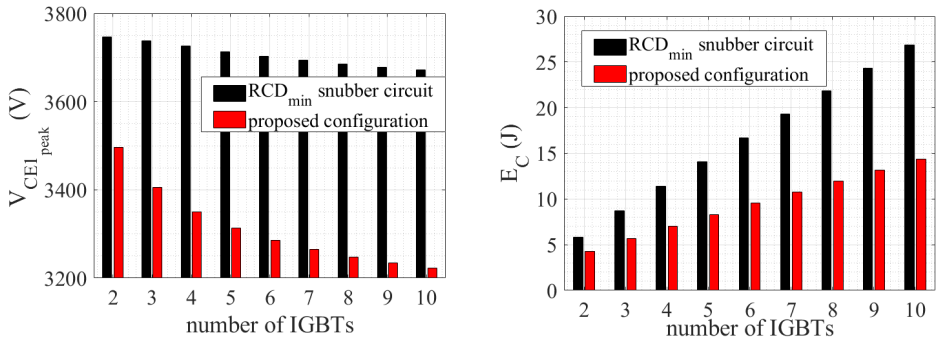


Figure 5.7: Comparison between RCD_{min} and the proposed configuration in terms of: (a) peak voltage of the early turned-OFF IGBT, and (b) total energy storage capability of snubber capacitors with respect to the number of series-connected IGBTs.

D. Case study with minimum RCD snubber circuit (RCD_{min}) and its comparison with the proposed configuration

The impact of the proposed configuration on the electrical performance of the solid-state breaker that utilizes several series-connected IGBTs can also be seen through the following investigation. Assuming a configuration with only RCD snubber circuits for the even voltage distribution among the IGBTs, similar to the first case, but this requires the same capacitances as the proposed one. This can be called as RCD_{min} configuration. According to the previous analyses, the snubber capacitances are calculated to be $1.95\mu F$ considering the worst-case scenario in the given parameters. In this investigation, the voltage stress of the early turned-OFF IGBTs in the proposed and the RCD_{min} configuration can be compared.

The results of such a comparison are shown in Fig. 5.7. It can be seen that the proposed configuration minimizes the peak voltage of the early turned-OFF IGBT for all N_s values. Specifically, when $N_s = 2$, the switch voltage in the proposed configuration is reduced by $250V$ compared to RCD_{min}, while in case of $N_s = 10$, the peak voltage drops even further, up to $450V$. Similarly, Fig. 5.7(b) reveals that the total energy storage capability of the snubber capacitors in the proposed configuration is also reduced compared to RCD_{min}.

E. Impact of the gate signal propagation delay on the early turned-OFF IGBT peak voltage

The design of the RCD snubber circuits should consider the longest possible gate signal propagation delay t_d that may occur among the series-connected IGBTs.

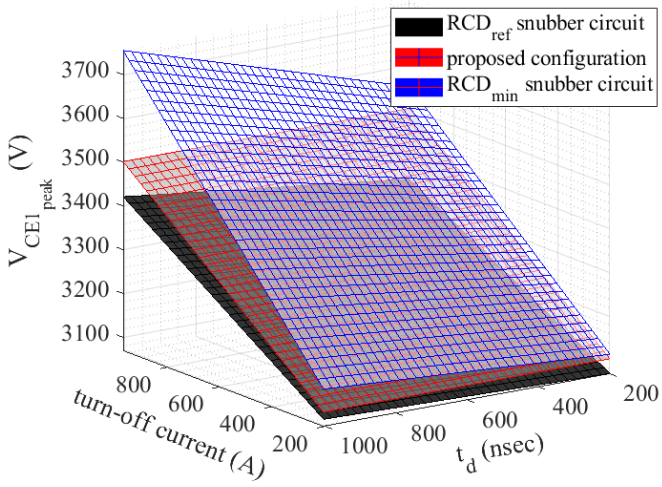


Figure 5.8: Peak voltage of the early turned-OFF IGBT with respect to I_{max} and t_d at $4kV_{DC}$ in case of RCD_{ref} (black), proposed configuration (red), and RCD_{min} (blue).

This part of the thesis examines the impact of the t_d on the peak voltage of the early turned-OFF IGBT for different turn-OFF currents in the three investigated configurations. For this case study, V_{DC} was set to $4kV$ leading to the use of two series-connected IGBTs. Moreover, the snubber capacitances were calculated and set to $4.8\mu F$ for the RCD_{ref} configuration and $1.95\mu F$ for the proposed and the RCD_{min} configurations. Fig. 5.8 shows the peak voltage of the early turned-OFF IGBT for the three configurations as a function of t_d and I_{max}. It can be seen that $V_{CE1peak}$ reaches $3.75kV$ in RCD_{min} at $I_{max} = 1000A$ and $t_d = 1\mu s$. On the other hand, in the proposed configuration, $V_{CE1peak}$ reaches approximately $3.5kV$ and in RCD_{ref} it becomes equal to $3.41kV$ at a cost of much higher snubber capacitance. Lastly, at low I_{max} (i.e. lower than $300A$), the three configurations exhibit similar performance even if t_d becomes long, e.g. $1\mu s$.

F. Impact of the MOV stray inductance on the early turned-OFF IGBT peak voltage

The impact of $L_{\sigma MOV}$ on the peak voltage of an early turned-OFF IGBT utilized in a breaker comprising two series-connected devices has also been investigated. The grid parameters are the same as in the previous analysis, i.e. $V_{DC} = 4kV$ leading to $N_s = 2$. The snubber capacitances are calculated to be $4.8\mu F$ for the RCD_{ref} and $1.95\mu F$ for the proposed and the RCD_{min} configurations. Additionally, $1\mu s$ has been introduced as a signal gate propagation delay between the two IGBTs. The peak voltage of the early turned-OFF IGBT with respect to several $L_{\sigma MOV}$ values and various turn-OFF currents is shown in Fig. 5.9. It can be observed

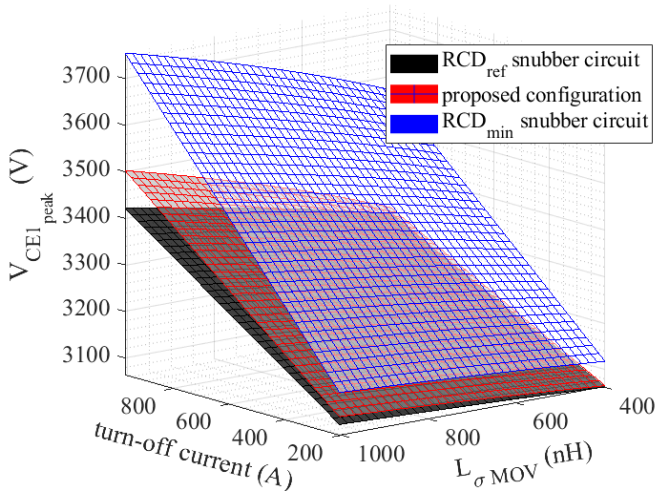


Figure 5.9: Peak voltage of the early turned-OFF IGBT with respect to I_{max} and $L_{\sigma MOV}$ at $4kV_{DC}$ in case of RCD_{ref} (black), proposed configuration (red), and RCD_{min} (blue).

that the proposed scheme keeps the early turned-OFF IGBT voltage below $3.5kV$ for the entire investigated range of $L_{\sigma MOV}$. This performance is slightly worse compared to the performance of the RCD_{ref} configuration, in which though, the snubber capacitances are almost 2.5 times higher than in the proposed one. Besides that, the line current also becomes significantly higher in case of higher snubber capacitances as explained in Chapter 4.

5.3.2 Simulation results

Matlab/Simulink has been used for the modelling of the investigated solid-state circuit breaker connected in an MVDC grid as shown in Fig. 5.10. The design and operating parameters of the DC grid and the breaker are summarized in Table 5.1. Two case studies have been examined. In the first study, the DC voltage was set to $4kV$ and therefore two series-connected IGBTs were utilized in the breaker configuration. In the second case study, five IGBTs were considered in a $10kV$ DC grid. IGBTs with blocking voltage of $4.5kV$ and current rating of $1300A$ have been used and modelled in Matlab/Simulink taking into account the datasheet of the device (ABB 5SNA1300K450300) and adjusting the IGBT device model in Simulink. The snubber capacitances have been calculated to be $4.8\mu F$ for RCD_{ref} and $1.95\mu F$ for the proposed and the RCD_{min} configurations.

Fig. 5.11 shows simulation results of the gate signals of two solid-state DC breaker configurations when $V_{DC} = 4kV$. In particular, Fig. 5.11(a) is referring to both

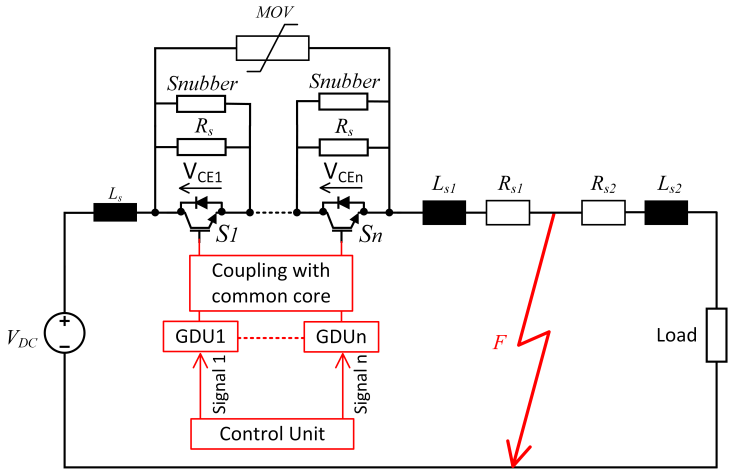


Figure 5.10: Schematic diagram of the investigated MVDC power grid with the proposed voltage-balancing configuration employed in a solid-state breaker.

Table 5.1: Design and operating parameters of the DC power grid

Parameter	Symbol	Value	unit
DC voltage	V_{DC}	4/10	kV
Number of series-connected IGBTs	N_s	2/5	
Load current	I_{load}	400	A
Current limiting inductance	L_s	98/243	μH
Line inductances	L_1, L_2	0.1	μH
Maximum turn-OFF current of IGBTs	I_{max}	960	A
Clamping voltage of MOV	V_{MOV}	6/15	kV
MOV stray inductance	$L_{\sigma MOV}$	1	μH
Gate signal propagation delay	t_d	1	μs

RCD snubber configurations (i.e. RCD_{ref} and RCD_{min}) and shows the generated signals for two switches with $1\mu s$ gate signal propagation delay and the corresponding gate-emitter voltages. The signal delay can also be observed in the gate voltages. On the other hand, the proposed configuration synchronizes the gate-emitter voltages mitigating the dynamic voltage imbalance between the two IGBTs as shown in Fig. 5.11(b).

The synchronized gate voltages of the two series-connected IGBTs lead to an even distribution of the emitter-collector voltages (Fig. 5.12(c)). On the other hand, in case of unsynchronized gate voltages, the voltage across the early turned-OFF IGBT (S1) experiences higher voltage than the late turned-OFF counterpart (S2)

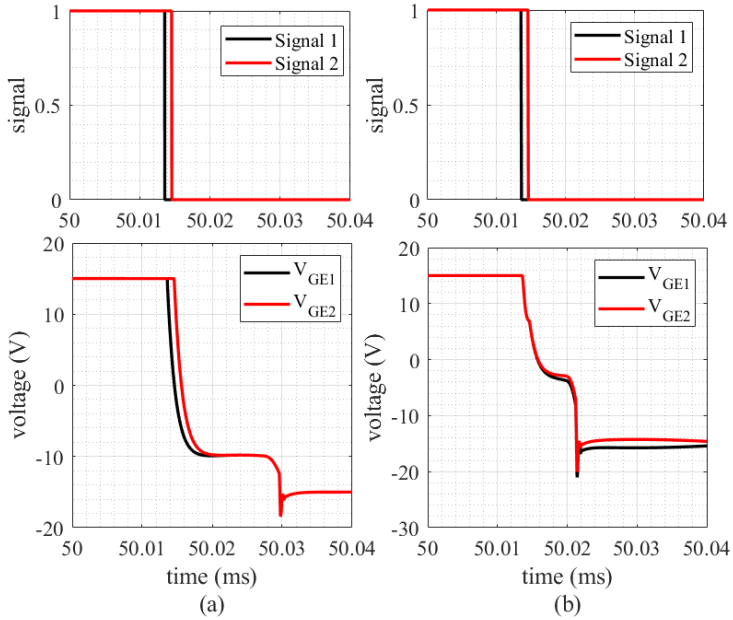


Figure 5.11: Simulation results showing two gate signals with a propagation delay of $1\mu s$ between each other and the corresponding gate-emitter voltages for S1 and S2 in case of: (a) RCD snubber configurations (RCD_{ref} and RCD_{min}) and (b) proposed configuration.

(see Figs. 5.12(a) and 5.12(b)). The numerical results are summarized in Table 5.2. It can be seen that in RCD_{ref}, the peak voltage of the early turned-OFF IGBT achieves the lowest voltage during a breaking operation compared to the other two investigated configurations. This occurs due to the highest snubber capacitances used in RCD_{ref} configuration. Additionally, the latter also leads to high short-circuit current, as well as to longer fault clearance times (Fig. 5.13). The numerical results can be seen in Table 5.2. Last but not least, a second case study, in which the DC voltage has been set to $10kV$ and five IGBTs are series-connected has also been investigated. The simulation results can be found in Table 5.2. They reveal a performance similar to the previous case study with $V_{DC} = 4kV$. The proposed configuration manages to minimize the peak voltage of the early turned-OFF IGBT, as well it keeps the short-circuit current at the lowest value. In particular, the peak voltage reaches $3310V$ and the fault current becomes equal to $1060A$ in case of the proposed configuration. In RCD_{ref} configuration, the corresponding values for the voltage and current are $3370V$ and $1170A$ respectively. Finally, when the RCD_{min} configuration is used, the voltage across the early turned-OFF IGBT becomes equal to $3730V$, and the fault current reaches $1060A$.

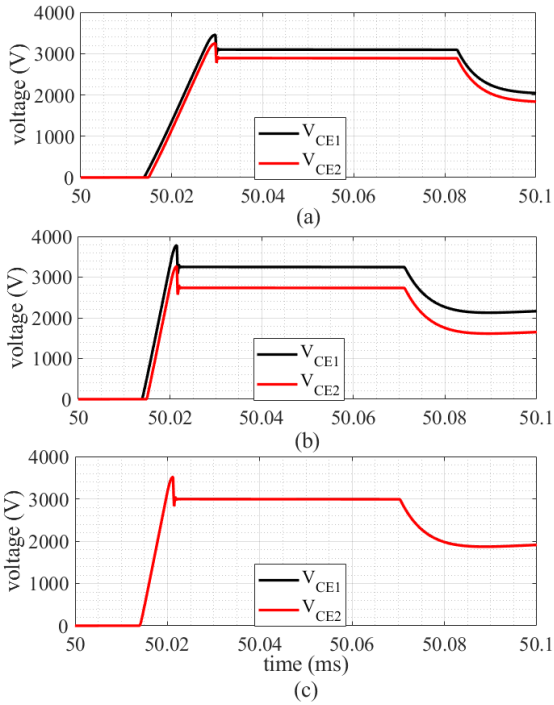


Figure 5.12: Simulation results showing the voltages of the early turned-OFF IGBT (S1 with black) and the late turned-OFF IGBT (S2 with red) during a breaking operation in: (a) RCD_{ref}, (b) RCD_{min}, and (c) proposed configurations.

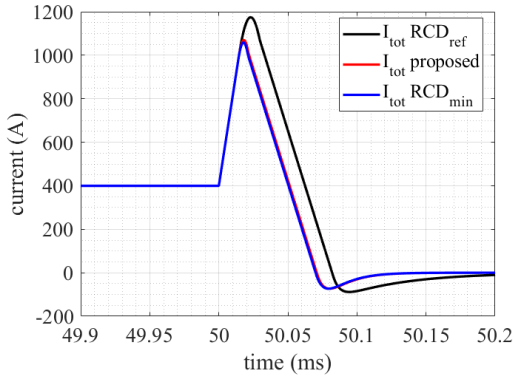


Figure 5.13: Simulation results for the line fault currents in case of RCD_{ref} (black), proposed (red) and RCD_{min} (blue) configurations during a breaking operation.

Table 5.2: Simulation results for the investigated cases with $t_d = 1\mu s$

V_{DC} $[kV]$	N_s	Case	C_{sn} $[\mu F]$	$V_{CE1_{peak}}$ $[V]$	$I_{tot_{peak}}$ $[A]$	t_{cl} $[\mu s]$
4	2	RCD_{ref}	4.8	3415	1170	200
		Proposed	1.95	3485	1060	120
		RCD_{min}	1.95	3750	1060	120
10	5	RCD_{ref}	4.8	3370	1170	250
		Proposed	1.95	3310	1060	140
		RCD_{min}	1.95	3730	1060	140

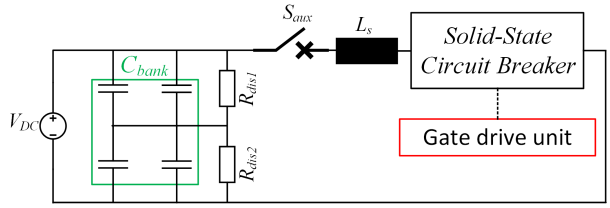


Figure 5.14: Schematic diagram of the test circuit.

5.4 Experimental results

The performance of the proposed scheme has been experimentally validated in a down-scaled laboratory prototype of a solid-state circuit breaker rated at $3kV_{DC}$ and $50A$. The test circuit is shown in Fig. 5.14, in which single-pulse tests have been conducted. A photograph of the experimental setup is illustrated in Fig. 5.15, and the design parameters are summarized in Table 5.3.

Two $3.6kV/50A$ IGBTs (IXYS, IXBX50N360HV) have been used in the solid-state breaker prototype. In addition, two GDUs have been designed and tested. The first is a conventional unit in which two unsynchronized signals are generated and sent to the gate terminals of the two IGBTs. The second unit is based on the proposed method and thus, it includes the gate coupled transformer as shown in Fig. 5.16. The design parameters of the proposed and the conventional GDUs can be found in Table 5.4. Several experiments at various operating scenarios have been performed and the corresponding investigations are presented below. Snubber capacitances of $0.15\mu F$, $0.33\mu F$ and $1\mu F$ have been tested at two DC voltage levels, i.e. $1500V$ and $3000V$ by employing the two GDUs. In the first voltage test, a single MOV with $V_{1mA} = 1600V$ was used and in case of $3000V$, two similar MOVs were connected in series in order to withstand the DC voltage. Finally, for these tests, a gate signal propagation delay of $1\mu s$ has been considered.

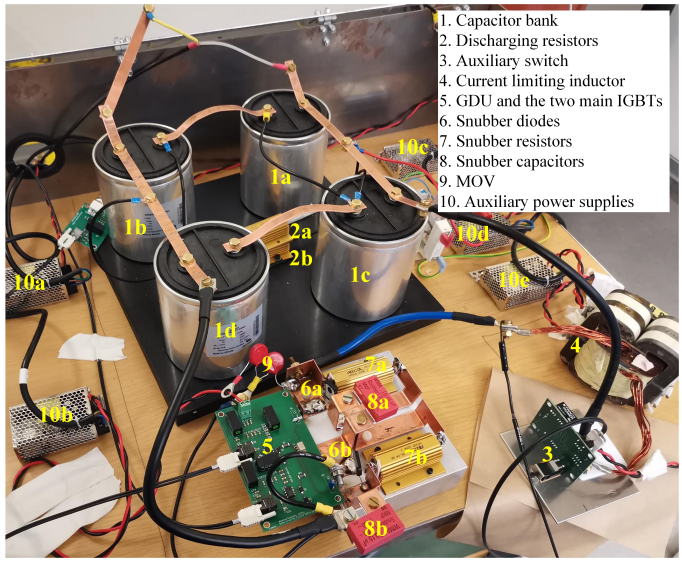


Figure 5.15: Photograph of the experimental setup.

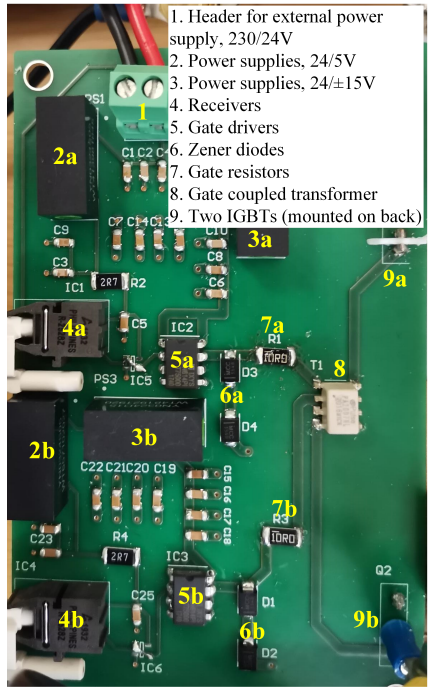


Figure 5.16: Photograph of the proposed gate drive unit.

Table 5.3: Parameters of the experimental setup

Parameter/Component	Value
Input voltage, V_{DC}	1500/3000 V
Main switches, IGBTs	IXYS, IXBX50N360HV
Auxiliary switch, S_{aux}	IXYS, IXBX50N360HV
Capacitor bank, C_{bank}	EPCOS/TDK, 4xB25620B1217K983
Discharge resistors, $R_{dis1,2}$	$47k\Omega$
Current limiting inductor L_s	$660\mu H$
Snubber diodes, $D_{sn1,2}$	GeneSiC, GB25MPS17-247
Snubber resistors, $R_{sn1,2}$	220Ω
Snubber capacitors, $C_{sn1,2}$	WIMA, $0.15 - 1\mu F$
Metal-Oxide Varistor, MOV	Littelfuse, 2xV1000LA160BP

Table 5.4: Design parameters of the gate drive units

Parameter/Component	Value
Power supplies, $24/5V$	Traco, TMR 3-2411
Power supplies, $24/\pm 15V$	Traco, TMR 3-2423
External power supply, $230/24V$	Traco, TXM 015-124
Gate drivers	IXYS, IXDN614PI
Receivers	Broadcom/Avago, HFBR-2528Z
Gate resistors, R_{g1}, R_{g2}	Bourns, CR2512AFX-10R0EAS
Zener diodes	MCC, SMBJ5354B
Gate balancing magnetic core	Pulse Electronics, PA2007NL

5.4.1 Experimental results at $V_{DC} = 1500V$

The first set of experiments relates to the RCD_{ref} configuration along with the conventional gate drive unit at a voltage of $1500V_{DC}$. Two pulse lengths have been used for the solid-state breaker testing in order to achieve two turn-OFF currents. The oscillograms for the first investigation showing the line current (I_{tot}), breaker voltage (V_{BR}), and voltages across the early and late turned-OFF IGBTs (V_{CE1} and V_{CE1} respectively) are shown in Fig. 5.17. In this case, the snubber capacitances have been set to $0.15\mu F$ and the pulse duration at $20\mu s$. The peak voltage of the early turned-OFF IGBT reached $1340V$, while the late turned-OFF IGBT experienced $300V$ lower voltage, i.e. $1040V$. Additionally, the turn-OFF current reached $46A$. However, when the snubber capacitances increase to $1\mu F$, the voltage difference between the two IGBTs is minimized significantly as shown in Fig. 5.18. In particular, $V_{CE1peak} = 1180V$ and $V_{CE2peak} = 1080V$ lead-

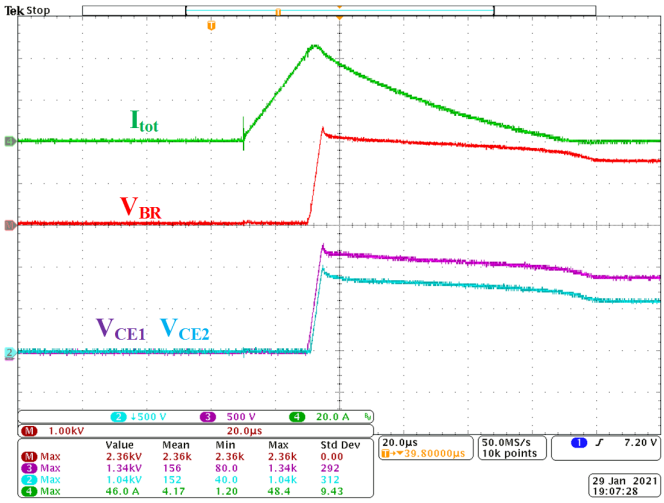


Figure 5.17: Experimental results for the RCD_{ref} configuration at $1500V_{DC}$ and $46A$ turn-OFF current with $C_{sn} = 0.15\mu F$ and $t_d = 1\mu s$. Measured line current (green line, 20A/div), early turned-OFF IGBT voltage (purple line, 500V/div), late turned-OFF IGBT voltage (light blue line, 500V/div), and total breaker voltage (red line, 1kV/div) (time base 20μs/div).

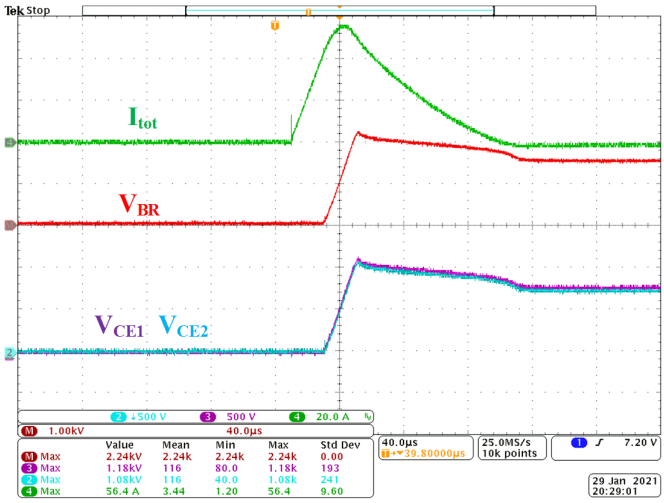


Figure 5.18: Experimental results for the RCD_{ref} configuration at $1500V_{DC}$ and $56.4A$ turn-OFF current with $C_{sn} = 1\mu F$ and $t_d = 1\mu s$. Measured line current (green line, 20A/div), early turned-OFF IGBT voltage (purple line, 500V/div), late turned-OFF IGBT voltage (light blue line, 500V/div), and total breaker voltage (red line, 1kV/div) (time base 40μs/div).

ing to $100V$ difference, which is one third of the value corresponding to the case with lower snubber capacitances. On the other hand, the increase of the snubber capacitances is also associated with higher line current. For the same pulse duration between the two cases, the line current increased from $46A$ to $56.4A$ with the rise of the snubber capacitances. The numerical results for all experimental investigations in case of RCD_{ref} configuration can be found in Table 5.5.

The second set of experiments was conducted at $1500V_{DC}$ using the proposed scheme. Fig. 5.19 reveals that the use of the minimum snubber capacitance, i.e. $0.15\mu F$ can be sufficient for the voltage balancing among the two series-connected IGBTs when a gate signal propagation delay of $1\mu s$ is introduced. In particular, the early and the late turned-OFF IGBTs experience the same voltage of $1140V$ at a peak current of $46.8A$. The numerical results of various experiments are shown in Table 5.6. It can be seen that the voltage is evenly distributed between the two IGBTs in all investigations when the proposed configuration is employed.

Table 5.5: Experimental results for the RCD_{ref} configuration at $V_{DC} = 1500V$ with $1\mu s$ gate signal propagation delay

C_{sn} $[\mu F]$	Pulse duration $[\mu s]$	$V_{CE1_{peak}}$ $[V]$	$V_{CE2_{peak}}$ $[V]$	$I_{tot_{peak}}$ $[A]$
0.15	10	1220	1020	26.8
0.15	20	1340	1040	46
0.33	10	1160	1060	31.6
0.33	20	1240	1080	48.4
1	10	1140	1080	43.6
1	20	1180	1080	56.4

Table 5.6: Experimental results for the proposed scheme at $V_{DC} = 1500V$ with $1\mu s$ gate signal propagation delay

C_{sn} $[\mu F]$	Pulse duration $[\mu s]$	$V_{CE1_{peak}}$ $[V]$	$V_{CE2_{peak}}$ $[V]$	$I_{tot_{peak}}$ $[A]$
0.15	10	1080	1080	27
0.15	20	1140	1140	46.8
0.33	10	1080	1070	31.2
0.33	20	1110	1110	48.8
1	10	1060	1060	44
1	20	1090	1090	58

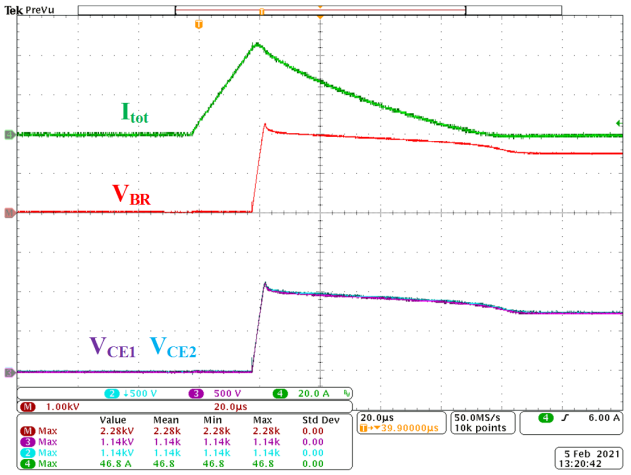


Figure 5.19: Experimental results for the proposed configuration at $1500V_{DC}$ and $46.8A$ turn-OFF current with $C_{sn} = 0.15\mu F$ and $t_d = 1\mu s$. Measured line current (green line, 20A/div), early turned-OFF IGBT voltage (purple line, 500V/div), late turned-OFF IGBT voltage (light blue line, 500V/div), and total breaker voltage (red line, 1kV/div) (time base 20μs/div).

5.4.2 Experimental results at $V_{DC} = 3000V$

The last set of experiments concerns solid-state breakers rated at $3000V_{DC}$. Both investigated GDUs have been tested with snubber capacitances of $0.15\mu F$. The experimental results in case of RCD_{ref} configuration with the conventional GDU are depicted in Fig. 5.20. This figure shows that the peak voltage of the IGBT that turns-OFF $1\mu s$ sooner reaches $2410V$, while the second IGBT experiences a peak voltage of $2030V$, leading to a voltage difference of $380V$. The turn-OFF current reached $55.2A$. On the other hand, when the gate coupled transformer is used, the voltage is distributed more evenly in the two IGBTs, with a voltage difference of $60V$, at a turn-OFF current of $54.4A$ (Fig. 5.21). Such difference might be due to mismatches between the device parameters spread of the considered IGBTs. The numerical results for the two investigated cases are included in Table 5.7.

Table 5.7: Experimental results for the RCD_{ref} and the proposed configurations at $V_{DC} = 3000V$ with $1\mu s$ gate signal propagation delay

C_{sn} $[\mu F]$	Configuration	$V_{CE1_{peak}}$ $[V]$	$V_{CE2_{peak}}$ $[V]$	$I_{tot_{peak}}$ $[A]$
0.15	RCD_{ref}	2410	2030	55.2
0.15	proposed	2150	2210	54.4

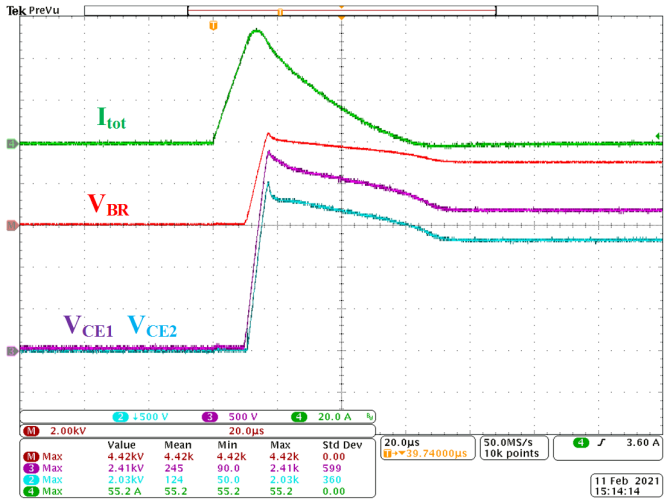


Figure 5.20: Experimental results for the RCD_{ref} configuration at $3000V_{DC}$ and $55.2A$ turn-OFF current with $C_{sn} = 0.15\mu F$ and $t_d = 1\mu s$. Measured line current (green line, 20A/div), early turned-OFF IGBT voltage (purple line, 500V/div), late turned-OFF IGBT voltage (light blue line, 500V/div), and total breaker voltage (red line, 2kV/div) (time base 20μs/div).

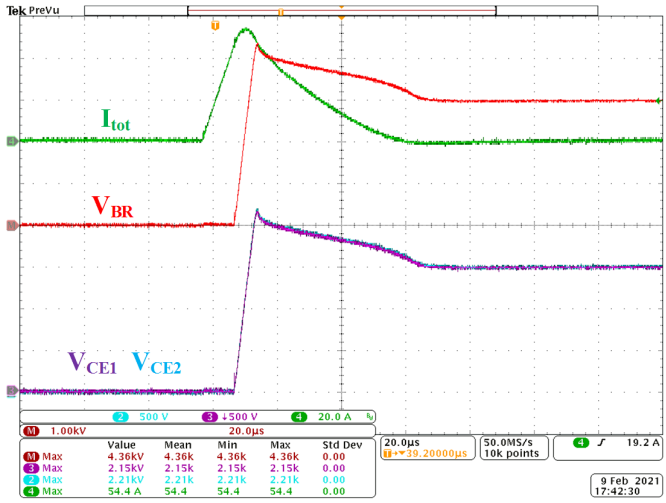


Figure 5.21: Experimental results for the proposed scheme at $3000V_{DC}$ and $54.4A$ turn-OFF current with $C_{sn} = 0.15\mu F$ and $t_d = 1\mu s$. Measured line current (green line, 20A/div), early turned-OFF IGBT voltage (purple line, 500V/div), late turned-OFF IGBT voltage (light blue line, 500V/div), and total breaker voltage (red line, 1kV/div) (time base 20μs/div).

5.5 Conclusions

This Chapter has presented and analyzed the design challenges of series-connected IGBTs employed in solid-state MVDC breakers. A hybrid method to mitigate the voltage imbalances among series-connected IGBTs has been proposed. This method is based on an RCD snubber circuit and a gate coupled transformer, with the aim to minimize the required snubber capacitances. The latter leads to smaller, lighter and less costly snubber circuit as well as to lower short-circuit current drawn from the DC line. The performance of the proposed hybrid configuration was validated by means of simulations and experiments.

Three configurations have been considered in two simulation studies with respect to the rated MVDC voltage of the examined solid-state breaker, i.e. $4kV_{DC}$ with two series-connected IGBTs and $10kV_{DC}$ with five IGBTs. In both cases, the proposed configuration achieved the mitigation of the voltage imbalance among the devices when a gate signal delay of $1\mu s$ among them was introduced. Moreover, with the proposed scheme, the short-circuit current is kept low by minimizing the snubber capacitances at 60% compared to a reference configuration RCD_{ref}.

The feasibility of the proposed scheme has also been verified experimentally. A down-scaled laboratory prototype of a solid-state MVDC breaker employing two series-connected IGBTs and RCD snubber circuits has been designed, built and tested. Additionally, two gate drive units, one conventional and one with the gate coupled transformer have also been designed. Two voltage levels have been considered; $1500V_{DC}$ and $3000V_{DC}$. Snubber capacitances in the range of $0.15\mu F$-$1\mu F$ were used for the RCD circuit design, while a $1\mu s$ gate signal propagation delay between the two IGBTs was introduced. A comparison between the proposed configuration and the conventional RCD_{ref} was performed. In particular, in case of $1500V_{DC}$ and $46A$ turn-OFF current with snubber capacitances of $0.15\mu F$, the voltage difference between the early and the late turned-OFF IGBTs was measured to be $300V$ when the conventional gate drive units were employed. On the other hand and under the same testing conditions, the two IGBTs share equally the voltage during a breaking operation when the proposed scheme is used. Finally, in the $3000V_{DC}$ study, similar experimental results were achieved. In particular, in case of RCD_{ref}, the voltage difference between the two IGBTs was measured to be $380V$, while in the proposed scheme, it was reduced to $60V$.

Chapter 6

An automatic and self-powered solid-state DC circuit breaker based on normally-ON SiC JFETs

In this Chapter, an Automatic and Self-Powered (ASP) solid-state DC circuit breaker employing normally-ON SiC JFETs is proposed. Initially, the concept description and the operating principle of the breaker are given. Then, simulation results under several operating conditions will follow. Finally, a laboratory prototype of the proposed concept will be presented under various design and operating scenarios in order to validate the effectiveness of the breaker.

Contributions

The majority of the proposed solid-state DC breakers requires fault detection schemes in order to be activated and thus to interrupt the fault line current. Additionally, the solid-state breakers employ IGBTs or SiC MOSFETs as the main high-power semiconductor devices. On the other hand, there are a few concepts which are based on either thyristors or normally-ON SiC JFETs. The main contribution of this Chapter is the presentation of an ASP solid-state breaker used in 700_{DC} grids based on normally-ON SiC JFET. This concept neither requires external gate power supply nor fault detection circuit, and it exhibits the lowest conduction losses due to the use of normally-ON SiC JFETs as shown in Chapter 3. In literature, various solid-state breaker concepts based on normally-ON SiC JFETs have been proposed. However, they rely on the voltage drop across the device, while

in this proposed concept, the gate of the JFET is magnetically coupled with the DC line via two mutually coupled inductors. Therefore, the JFET and hence the breaker is activated and turns-OFF under a rising fault current causing a voltage across the primary winding of the coupled inductors. As a result, the induced voltage on the secondary winding turns-OFF the JFET. This Chapter summarizes the content of two publications [P6, P8].

6.1 Background

From Chapter 3, it has been revealed that the normally-ON SiC JFETs can minimize the conduction losses of solid-state breakers employing devices with blocking voltage in the range of $1200 - 1700V_{DC}$. Besides the low conduction losses, the normally-ON nature of such devices eliminates the need for continuous gate power supply in order to keep the device ON. On the other hand, the turn-OFF process of a SiC JFET requires a negative gate voltage, and therefore a power supply in the gate must be present.

Furthermore, a fault detection circuit should normally be connected in a DC grid as shown in Fig. 3.1. This circuit detects short-circuits and then, it sends a turn-OFF signal to the GDU of the power semiconductor device. Several methods to detect a short-circuit in a DC grid have been proposed. However, they rely on electronic devices, sensors etc. which increases the design and operating complexity and thus, the response and safe operation of the entire protection system decreases.

The proposed solid-state DC breaker which employes normally-ON SiC JFET eliminates the need for an external power supply for the gate driver by using the magnetic energy stored in the coupled inductors connected to the DC line. These coupled inductors supply the required negative voltage in the gate-source terminals of the JFET when a rapid increase of the line current occurs (e.g. during a short-circuit). Therefore, the JFET starts to turn-OFF and hence the breaker can clear the fault. From these, it can be concluded that the proposed breaker does not only exhibit low conduction losses due to the use of SiC JFETs, but also it is an ASP breaker concept. This breaker can be considered for medium-power applications rated at $700V_{DC}$ by utilizing the commercial $1200V$-class SiC JFETs. The proposed breaker can also be used at applications with requirements for higher voltages than $700V_{DC}$, when high-voltage SiC JFETs will become available in semiconductor market. The circuit analysis, as well as the operating principle of the proposed concept follow.

6.2 Operating principle of the proposed ASP solid-state breaker with normally-ON SiC JFET

The proposed solid-state DC circuit breaker connected in a simplified DC grid is shown in Fig. 6.1. The breaker contains high-power and low-power components. The high-power components are; a residual mechanical switch, a current limiting inductor, L_s, two mutually coupled inductors L_1 and L_2, the normally-ON SiC JFET and an MOV which is used for overvoltage suppression and residual energy absorption. The residual mechanical switch is used to provide galvanic isolation to the faulty lines, while L_s limits the short-circuit current rise. Additionally, the two mutually coupled inductors are used in order to provide the required power to the GDU. On the other hand, the low-power components are; a damping resistor R_d, and the ASP gate driver of the SiC JFET. The ASP circuit is composed of a full-bridge diode rectifier D_b, a capacitor C_{dc}, one Zener-diode regulator D_{zn} along with a parallel capacitor C_n, and a series-connected leakage resistor R_{leak}, which limits the current through the Zener diode. A gate resistor R_g must also be used for the damping of possible oscillations when the MOV is deactivated. Under a short-circuit condition, the line current rises sharply leading to a voltage drop across L_1. This induces a voltage in L_2, which is rectified and then feeds energy to C_{dc}. This capacitor supplies the required negative voltage to the gate of the JFET, and thus the device turns-OFF. The voltage across C_{dc} must exceed the pinch-OFF voltage of the JFET (normally $-6V$) which is required for the turn-OFF taking into consideration also the possible voltage drop across R_{leak}.

The theoretical performance of the proposed solid-state DC breaker during a short-circuit condition is illustrated in Fig. 6.2. A line-to-line short-circuit occurs at t_1, leading to a rapid increase of the line current i_{L1} as shown on the top waveform in Fig. 6.2. During the same time period, the DC voltage V_{DC} will appear across the current limiting inductor L_s, as well as across the primary side of the mutually coupled inductors, i.e. L_1. This voltage, V_{L1+}, is given as:

$$u_{\mathrm{L1(t_1-t_2)}} = V_{\mathrm{L1+}} = \frac{L_1}{L_1 + L_s} \cdot V_{DC} \tag{6.1}$$

The voltage on the primary side induces a voltage across the secondary side L_2, V_{L2+}, which is proportional to the turns number N_1 and N_2. The voltage $u_{L2(t_1-t_2)}$ is therefore, given as follows.

$$u_{\mathrm{L2(t_1-t_2)}} = V_{\mathrm{L2+}} = \frac{N_2}{N_1} \cdot V_{L1+}, \tag{6.2}$$

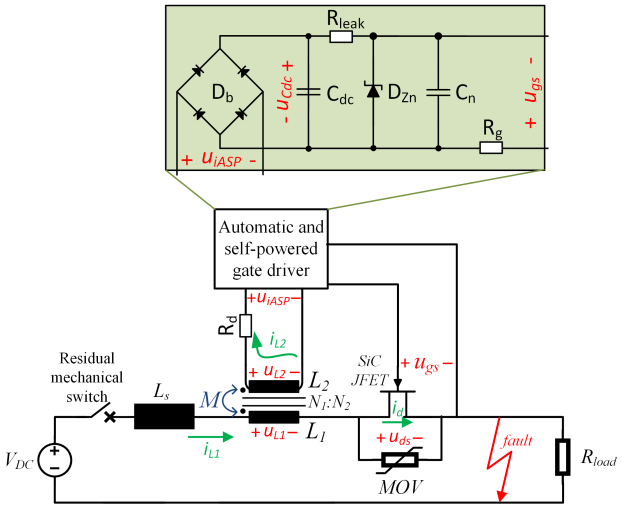


Figure 6.1: Schematic diagram of the solid-state DC breaker employing a normally-ON SiC JFET with the ASP gate driver.

The induced voltage on the secondary winding will generate a current i_{L2}, which eventually feeds the diode rectifier D_b and thus, charges C_{dc} at a certain level V_{Cdc} as shown in Fig. 6.2. The damping resistor R_d which is used to damp possible oscillations between C_{dc} and L_2 dissipates some energy and therefore, V_{Cdc} is expected to be slightly lower than V_{L2+}. During the same time interval $t_1 - t_2$, the gate-source voltage of the normally-ON SiC JFET becomes negative, following the inverse voltage of C_{dc}. The time instant t_2 initiates the second operating stage. At that moment, the gate-source voltage reaches the pinch-OFF voltage, V_{pi} of the JFET, and thus, the drain-source voltage, u_{ds} starts increasing. During the same time, the voltages across L_1 and hence across L_2 decrease. This stage ends when u_{ds} is clamped at V_{MOV}, which occurs at time instant t_3. After that point, the fault current is commutated to the MOV branch, and thus, it starts decreasing from a maximum value of I_{SCmax} to zero. The time instant t_4 denotes the fault line current interruption. The drain-source voltage u_{ds}, as well as the voltages of the coupled inductors V_{L1-} and V_{L2-} during the time interval $t_3 - t_4$ are as follow.

$$u_{\mathrm{ds(t_3-t_4)}} = V_{\mathrm{MOV}} \tag{6.3}$$

$$u_{\mathrm{L1(t_3-t_4)}} = V_{\mathrm{L1-}} = \frac{L_1}{L_1 + L_s} \cdot (V_{MOV} - V_{dc}) \tag{6.4}$$

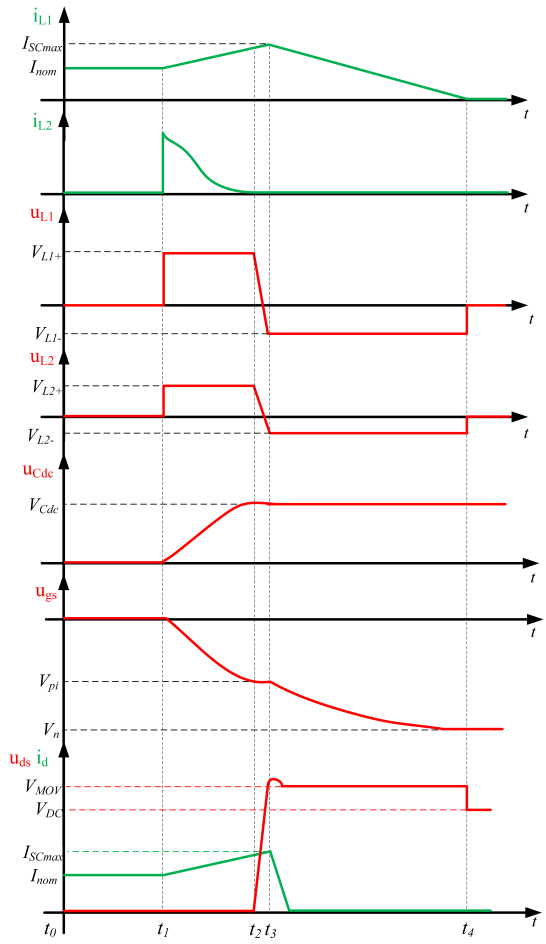


Figure 6.2: Theoretical performance of the proposed DC breaker.

$$u_{\mathrm{L2(t_3-t_4)}} = V_{\mathrm{L2-}} = \frac{N_2}{N_1} \cdot V_{L1-} \tag{6.5}$$

After the fault current interruption at t_4, the MOV is deactivated, and thus the voltage across the JFET becomes equal to V_{DC}, while the voltages across the coupled inductors become zero. C_{dc} keeps the voltage at V_{Cdc} for a certain time period, which depends on the value of C_{dc}, and the Zener diode D_{zn} clamps the gate-source voltage at V_n as shown in Fig. 6.2. The residual mechanical switch should activate and galvanically isolate the faulty part of the grid before the u_{Cdc} drops at V_{pi} of the JFET, which can cause accidental retrigerring of the JFET.

6.3 Design considerations of the proposed ASP solid-state breaker with normally-ON SiC JFET

There are several challenges when designing the proposed breaker. The turns-ratio of the mutually coupled inductors N_1/N_2, as well as the ratio of the primary side inductance L_1 to the current limiting inductance L_s are of great importance. Additionally, C_{dc} must be chosen that to ensure the required supply of a negative gate voltage V_n to the normally-ON SiC JFET in order to turn-OFF safely. The following criterion must be therefore met:

$$V_{\mathrm{Cdc}} \geq V_n + V_{Rleak}, \tag{6.6}$$

where V_{Rleak} is the voltage drop across the R_{leak}. As mentioned above, V_{Cdc} is slightly lower than V_{L2+} which is given by (6.2). This equation along with (6.1) must be considered for choosing the turns-ratio N_1/N_2, as well as for L_1 and L_s. It must be mentioned that V_{DC} is expected to be in the range of $700V$ and V_n is lower than $30V$ in absolute value. Therefore, it can be concluded that L_s must be chosen to be significantly higher than L_1, and thus, it can be designed based on (4.1). The latter expression can be rearranged as follow.

$$L_s \geq \frac{V_{dc}}{\frac{I_{SCmax}-I_{nom}}{t_{delay}}} \tag{6.7}$$

where I_{nom} is the nominal line current. Additionally, the delay time t_{delay} includes the charging time of C_{dc}, as well as the turn-OFF delay time of the JFET which depends on both gate resistance and gate-source capacitance. Furthermore, R_d damps possible oscillations between L_2 and C_{dc} and hence, the following criterion must be met.

$$R_d > 2\sqrt{\frac{L_2}{C_{dc}}} \tag{6.8}$$

Last but not least, the charging time of C_{dc} should also be considered since it indicates the turn-OFF process of the normally-ON SiC JFET and hence the anticipated peak fault current I_{SCmax} drawn from the grid. It can be concluded that several design parameters such as L_s, L_1, L_2, C_{dc} and R_d need to be considered when designing the proposed ASP solid-state breaker according to the parameters and requirements set by the grid operators, e.g. V_{DC}, I_{SCmax} etc.

6.4 Simulation results

The proposed ASP solid-state breaker with normally-ON SiC JFETs (Fig. 6.1) was modelled and simulated using LTspice. The simulation parameters of the $700V_{DC}$ grid and the breaker are shown in Table 6.1. The SiC JFET used for the modelling and simulation is a $1200V/63A$ device having an ON-state resistance of $35m\Omega$ at room temperature (UnitedSiC, UJ3N120035K3S).

The simulated gate-source voltage of the JFET is shown in Fig. 6.3(a). The short-circuit occurs at the time point $t = 100\mu s$, leading to the charging of C_{dc}, and hence, to a decrease of the gate-source voltage. This voltage reaches the pinch-OFF voltage of the JFET after approximately $4\mu s$, and then, the drain-source voltage of the JFET starts increasing as illustrated in Fig. 6.3(b). Once this voltage becomes equal to the clamping voltage of the MOV, the line current commutates from the switch branch to the MOV path. This can be clearly seen in Fig. 6.4. At the same time, the gate-source voltage becomes more negative than the pinch-OFF voltage, until it is clamped from the Zener diode at $-30V$. Fig. 6.4 also shows that the fault line current reaches a peak value of approximately $80A$ and it is interrupted within $51\mu s$ from the fault occurrence.

The impact of C_{dc} on the electrical performance of the breaker has also been investigated as shown in Fig. 6.5. Four capacitance values, i.e. $0.1\mu F$, $0.3\mu F$, $0.5\mu F$ and $0.7\mu F$ were considered. From Fig. 6.5, it is revealed that the increase of the capacitance extends the required time for the gate-source voltage to reach the pinch-OFF value. This occurs due to the slow charging speed of a capacitor

Table 6.1: Design and operating parameters of the DC power grid

Parameter/Component	Symbol	Value
DC grid voltage	V_{DC}	700 V
Current limiting inductor	L_s	100 μH
Primary winding	L_1	10 μH
Secondary winding	L_2	10 μH
Coupling coefficient	c	0.95
Turns-ratio	$N1/N2$	1:1
DC capacitance in ASP	$\mathrm{C_{dc}}$	0.1 μF
Zener diode	V_n	-30V
Clamping voltage of MOV	V_{MOV}	900 V
Damping resistance	R_d	20 Ω
Nominal line current	I_{nom}	35 A
Maximum allowable fault current	I_{SCmax}	80 A

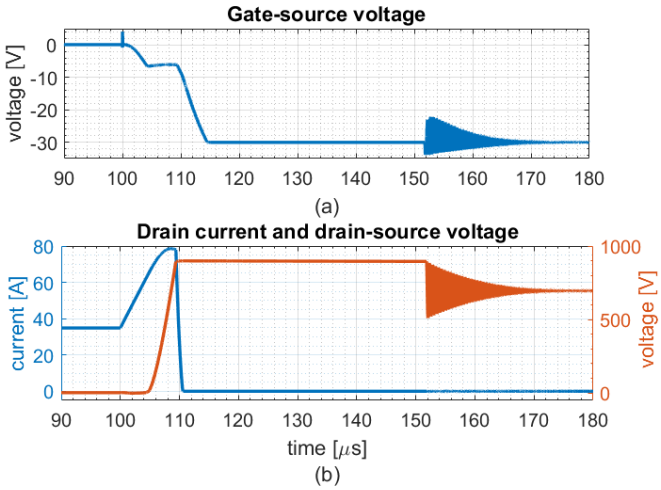


Figure 6.3: Simulation results showing: (a) the gate-source voltage, and (b) the drain-source voltage and the drain current of the SiC JFET under a short-circuit condition.

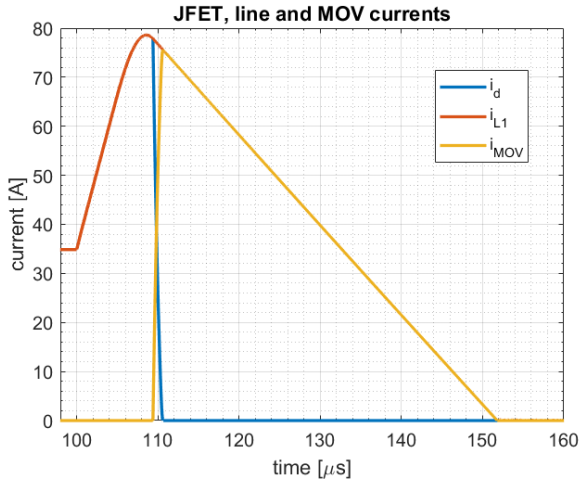


Figure 6.4: Simulation results showing the drain current of the SiC JFET, the fault line current and the current through MOV under a short-circuit condition.

having higher value. As a result, the line current rises further with the increase of C_{dc}. In particular, at $C_{dc} = 0.7\mu F$, it is found that the peak fault current reaches approximately $130A$, while in case of $0.1\mu F$, the corresponding current becomes $80A$. Therefore, the proper choice of C_{dc} is critical, defining among others the maximum short-circuit current.

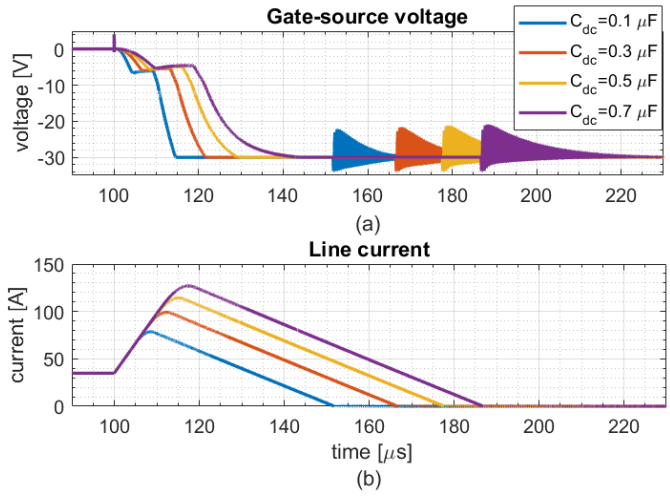


Figure 6.5: Simulation results showing: (a) the gate-source voltage of the SiC JFET, and (b) the fault line current for different values of C_{dc}.

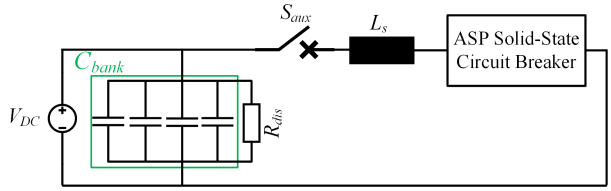


Figure 6.6: Schematic diagram of the test circuit.

6.5 Experimental results

The performance of the ASP solid-state DC breaker employing normally-ON SiC JFET has also been tested experimentally. Fig. 6.6 shows the schematic diagram of the test circuit. A photograph of the $700V_{DC}$ experimental test circuit along with the proposed solid-state breaker is illustrated in Fig. 6.7. A closer view of the ASP GDU, the normally-ON SiC JFET, and the coupled inductors are shown in Fig. 6.8. The design parameters for the coupled inductors are given in Table 6.2. For the experimental investigation, the same $1200V/63A$ normally-ON SiC JFET with the simulation study has been used (UJ3N120035K3S). In the test circuit, a $3600V/50A$ IGBT (IXBX50N360HV) has been used for the implementation of the auxiliary switch S_{aux}. The turn-ON of S_{aux} initiates the single-pulse test, while the turn-OFF isolates the JFET from the source, which must be ensured in a certain time, prior the discharge of the C_{dc}. The parameters of the experimental setup are shown in Table 6.3.

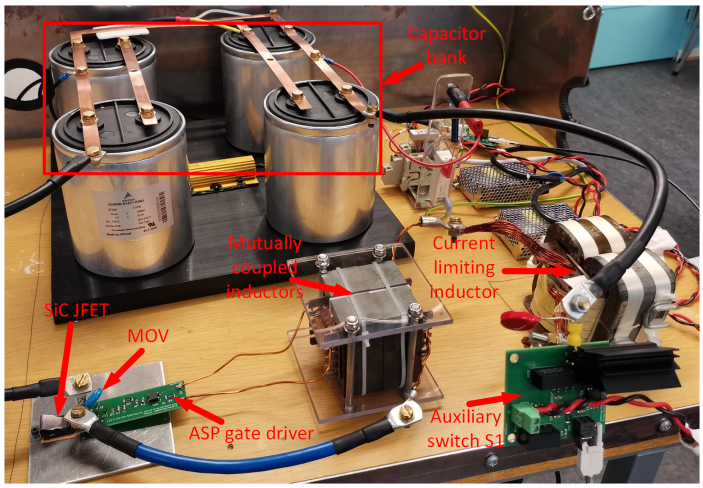
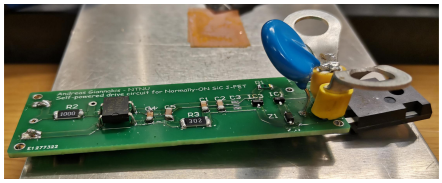
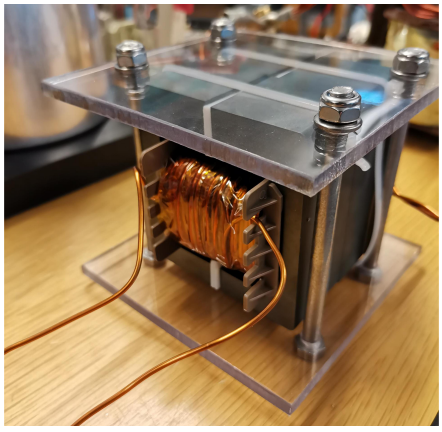


Figure 6.7: Photograph of the experimental solid-state DC breaker prototype employing the ASP gate driver.



(a)



(b)

Figure 6.8: (a) The automatic and self-powered gate driver, and (b) the coupled inductors.

Table 6.2: Design parameters of the coupled inductors

Parameter/Component	Value
Core type	4xE71/33/32
Core material	Ferrite N87
Saturation induction of the core, B_{sat}	0.32 T
Number of turns, $\mathrm{N_1}$	9
Air-gap, l_g	3.15 mm
Relative permeability, μ_r	1680
Cross-section area of the core A_c	1366 $\mathrm{mm^2}$

Table 6.3: Parameters of the experimental setup (power circuit and gate driver)

Parameter/Component	Value
Input voltage, V_{DC}	700 V
Main switch SiC JFET	UnitedSiC, UJ3N120035K3S
Auxiliary switch, S_{aux}	IXYS, IXBX50N360HV
Capacitor bank, C_{bank}	EPCOS/TDK, 4 x B25620B1217K983
Discharge resistor, R_{dis}	$47k\Omega$
Current limiting inductor L_s	$660\mu H$
Metal-oxide varistor MOV	Bourns MOV-14D621K
$\mathrm{L_1}$,$\mathrm{L_2}$	36 μH
Turns-ratio, N_1/N_2	1:1
Diode rectifier, $\mathrm{D_b}$	ON Semiconductor DF06M
$\mathrm{C_{dc}}$	0.1-1 μF
V_n	-30 V
V_p	5 V
R_{leak}	3 kΩ
IC-driver	IXYS IXDN614PI
Damping resistor, $\mathrm{R_d}$	20 Ω
Gate resistor, $\mathrm{R_g}$	50 Ω

The first set of experimental results is illustrated in Fig. 6.9. The value of C_{dc} has been set to $0.1\mu F$. The ASP solid-state breaker interrupts the line current I_{L1} within $260\mu s$ after the fault occurrence. This current reaches a peak value of $23.8A$ as shown in Fig. 6.9 with purple line. Once the line current starts rising, the gate-source voltage V_{gs} decreases and reaches the pinch-OFF voltage of the JFET after approximately $8\mu s$ as it can be seen in Fig. 6.9 with light blue line. At that instant time, the voltage across the JFET, V_{ds}, starts increasing and at a certain point, it is clamped from the MOV at $848V$. The MOV activation forces

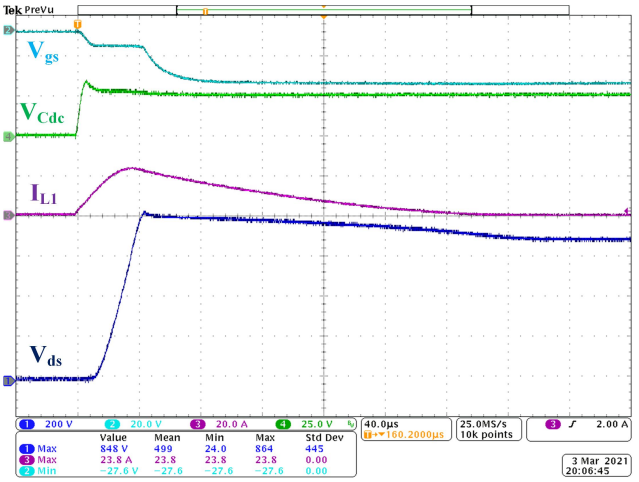


Figure 6.9: Experimental results for the solid-state DC breaker with $C_{dc} = 0.1\mu F$. Measured line current (purple line, 20A/div), C_{dc} voltage (green line, 25V/div), SiC JFET gate-source voltage (light blue line, 20V/div), and SiC JFET drain-source voltage (blue line, 200V/div), (time base 40μs/div).

the line current to commutate from the JFET path to the MOV leading to a current decrease and eventually to a current interruption.

The second set of experimental results, in which the capacitance C_{dc} has been set to $1\mu F$ is shown in Fig. 6.10. The line current reaches a peak value of $33A$, and it is interrupted within a time interval of $330\mu s$. Similar to the previous case, the voltage across the JFET is clamped at approximately $864V$ from the MOV.

The impact of C_{dc} on the performance of the proposed solid-state breaker has been assessed using four capacitance values, i.e. $0.1\mu F$, $0.43\mu F$, $0.76\mu F$ and $1\mu F$ (Figs. 6.11-6.13). The performance evaluation of the breaker concerns the line current, and the fault clearance time. Fig. 6.11 shows the gate-source voltage u_{gs} of the normally-ON SiC JFET and the voltage across C_{dc} for the four investigated cases. It is observed that the increase of the capacitance results in longer charging times for C_{dc} and thus, a longer time is required for u_{gs} to reach the pinch-OFF voltage. The turn-OFF process of the JFET is therefore delayed, leading towards higher line currents, as shown in Fig. 6.12. Besides the higher line currents, the increase of the capacitance C_{dc} causes longer fault clearance times. Finally, the voltage across the JFET in all four investigated cases exhibits similar performance due to the presence of the MOV, which clamps V_{ds} at approximately $850V$. The numerical results of the peak line current, peak switch voltage, and clearance time for all cases can be found in Table 6.4. It is apparent that the clearance time

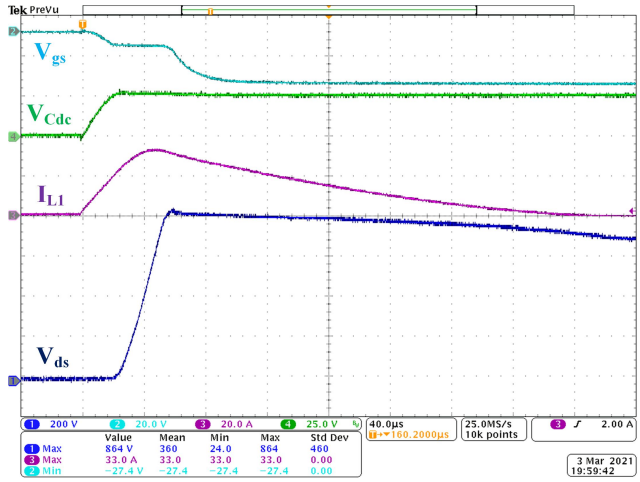


Figure 6.10: Experimental results for the solid-state DC breaker with $C_{dc} = 1\mu F$. Measured line current (purple line, 20A/div), C_{dc} voltage (green line, 25V/div), SiC JFET gate-source voltage (light blue line, 20V/div), and SiC JFET drain-source voltage (blue line, 200V/div), (time base 40μs/div).

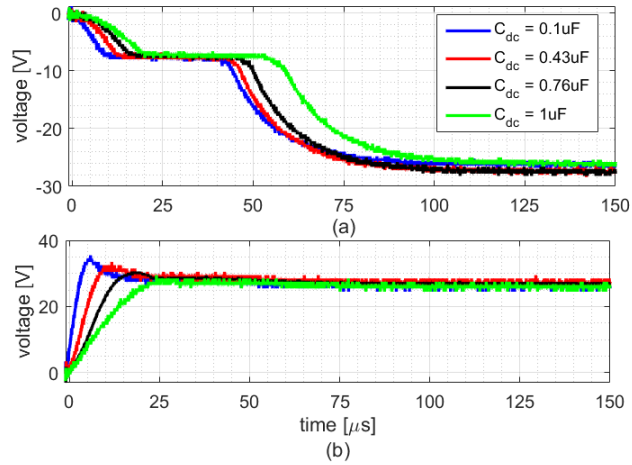


Figure 6.11: Experimental results showing: (a) gate-source voltage u_{gs} of the SiC JFET and (b) voltage of C_{dc}, u_{Cdc} for various C_{dc} values.

depends on the magnetic energy stored in the current limiting inductor. The higher the inductance is, the higher the energy is stored and hence, the longer the fault clearance time becomes. The use of higher L_s in the experimental setup compared to the simulation studies has led to longer fault clearance times in the experimental investigations.

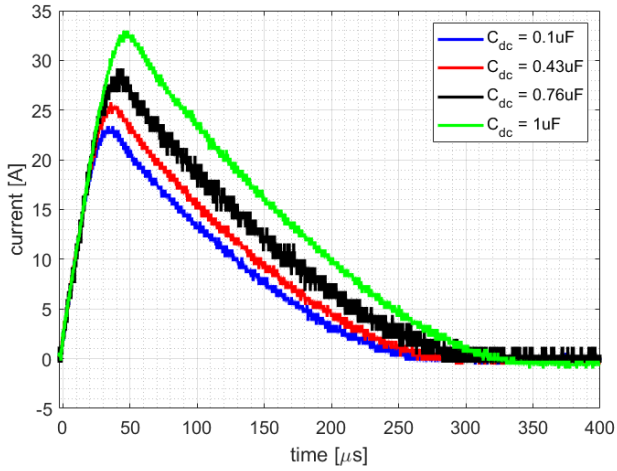


Figure 6.12: Experimental results showing the line current i_{L1} for various C_{dc} values.

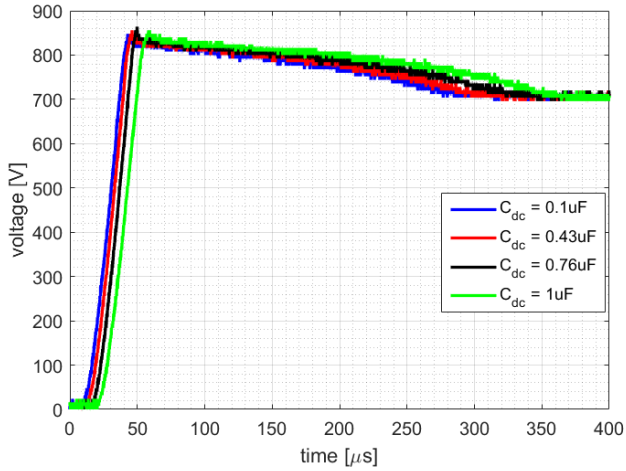


Figure 6.13: Experimental results showing the drain-source voltage u_{ds} of the SiC JFET for various C_{dc} values.

Table 6.4: Numerical experimental results for various C_{dc} values

$C_{dc}[\mu F]$	0.1	0.43	0.76	1
line current [A]	23.8	25.8	28.6	33
switch voltage [V]	848	848	856	864
clearance time [μs]	260	270	290	330

6.6 Conclusions

In this Chapter, an ASP solid-state circuit breaker rated at $700V_{DC}$ which employes normally-ON SiC JFETs has been proposed. The main benefits of this breaker topology are the low conduction losses associated with the use of SiC JFETs, the elimination of fault detection circuits, and the elimination of need for external gate power supply. The breaking operation relies on magnetically coupled inductors, in which the primary side is connected to the high-power DC grid, while the secondary side feeds the gate of the JFET via a diode rectifier, a capacitor C_{dc} and a Zener diode. The design and operating principles of the proposed breaker concept have been presented in details.

At first, the performance of the ASP solid-state breaker has been validated through simulations. A simplified $700V_{DC}$ grid with a nominal load of $35A$ has been modeled and simulated using LTspice. The breaker was able to interrupt a short-circuit current of $80A$ within $51\mu s$. Additionally, the impact of the capacitance choice C_{dc} on the breaker performance in terms of peak fault current and fault clearance time has been investigated. For a higher C_{dc} values, the short-circuit current becomes higher which also leads to longer clearance times.

Last but not least, a $700V_{DC}$ laboratory prototype of the proposed breaker concept was designed and constructed. The breaker is able to interrupt currents in the range of $23.8-33A$ within $260-330\mu s$ by employing several values for C_{dc} in the range of $0.1 - 1\mu F$. The latter means that the capacitance defines the threshold current that trips the breaker, and therefore, C_{dc} should be chosen wisely.

Chapter 7

Conclusions

One showstopper towards the development of LVDC and MVDC grids is the lack of high-performance protection schemes against short-circuit faults. Today, challenges such as high conduction power losses, electrical and thermal impact of breakers' design and operation on the grid components, fast clearing process of faults, as well as low-weight and low-volume breaker designs are imposed.

This PhD thesis proposes innovative concepts to tackle these design and operating challenges of solid-state circuit breakers for LVDC and MVDC grids. The research findings of this thesis concern ways of decreasing conduction power losses of existing power semiconductor technologies for designing the most efficient solid-state circuit breaker for LVDC and MVDC grids. In addition, the thesis proposes a way to minimize the volume and the weight of MVDC breakers when series-connected IGBTs should be used. Finally, a high-efficient, automatic and self-powered solid-state circuit breaker for LVDC grids has also been proposed.

Three main circuit breaker types for LVDC and MVDC grids have been identified. These are the mechanical with active resonance circuit, solid-state breakers and hybrid breakers. The solid-state breaker achieves high speed operation which leads to low short-circuit currents and thus to minimized current and thermal stress of the VSCs connected to the DC grid. Additionally, the volume of solid-state breakers is small and require less maintenance compared to the other two breaker types at a cost of high conduction losses. The proper choice of the breaker type relies mostly on the application area, the sensitivity of equipment, and the protection requirements set by the grid operators. Several LVDC and MVDC applications introduce space restrictions, as well as they require high speed breaking operations in order to isolate the faulty DC lines shortly after the short-circuit incident. It is

clear that under such constraints, the solid-state DC breakers should be considered.

The main drawback of the solid-state DC breakers is the high conduction losses caused in the power semiconductor devices. Several Silicon and SiC semiconductor device technologies have been assessed in terms of conduction power losses. It has been shown that the normally-ON SiC JFETs exhibit the lowest conduction losses in the blocking voltage range of $1200-1700V$ among several Silicon IGBTs and SiC MOSFETs technologies. The thesis also proposes a way to decrease the conduction losses by applying the maximum gate voltage to the semiconductors. The normally-ON SiC JFETs achieved a conduction loss reduction up to 33% at 55% of normalized current when the gate voltage was set to $2V$. Additionally, at high-power applications when high-power modules and press-packs are used, fewer semiconductor devices can be found as suitable candidates for solid-state DC breakers. It has been shown that the IGCTs reduce the conduction losses by more than 40% compared to IGBTs for a grid with $35kV$ of DC voltage and $25MW$ of power. However, the increased design complexity of the gate circuit in IGCTs necessitates the use of the voltage-controlled IGBTs for high-power solid-state breakers.

Besides the semiconductor devices utilized in a typical solid-state breaker, there are other power components that comprise such a breaker. The overvoltage suppression and energy absorption circuits are crucial components of the breakers. The use of RCD snubber circuits and MOV are the most common topologies to suppress the voltage across the switch during the turn-OFF switching. It has been revealed that the use of only MOV can be sufficient at low-power and medium-power applications. However, at high-power applications, such a breaker is prone to switch overvoltages due to the MOV stray inductance. Furthermore, the anticipated high switching energy during the breaker operation at high-power applications can lead to thermal damages to the switch. Additionally, when RCD snubber circuits are utilized, the required snubber capacitance can be high enough, leading not only to high snubber cost and volume, but also to extremely high short-circuit currents. On the other hand, the simulation and the experimental results showed that if both RCD snubber circuit and MOV are utilized in a breaker, the switch voltage, as well as the fault current are minimized at a cost of additional passive components. In addition, the required snubber capacitance is also minimized compared to the case with only RCD snubber circuit. Finally, it has been revealed that the impact of the stray inductance in the MOV path on the switch overvoltage is negligible in the case of using simultaneously RCD snubber circuit and MOV, which makes this configuration more suitable for high-power MVDC applications.

Design of solid-state breakers for MVDC necessitates the series connection of multiple semiconductor devices. The possible gate signal delays among the series-

connected IGBTs may lead to uneven voltage distribution during a breaking operation. This thesis has proposed a hybrid voltage balancing method consisting of RCD snubber circuits and a gate coupled transformer, aiming at minimizing the required snubber capacitances. This eventually leads to smaller, lighter and less costly snubber circuits. The simulations have shown that the proposed method achieved an even voltage distribution between five series-connected IGBTs during a breaking operation in a $10kV_{DC}$ grid, minimizing the snubber capacitances by 60%. Finally, it has experimentally been shown that the proposed method achieved a $60V$ voltage difference between an early turned-OFF IGBT and a late by $1\mu s$ turned-OFF IGBT in a $3kV_{DC}$ grid compared to a $380V$ voltage difference when only RCD snubber circuits were used.

Finally, an automatic and self-powered solid-state circuit breaker rated at $700V_{DC}$ which employes normally-ON SiC JFETs has also been proposed. The low conduction losses of the normally-ON SiC JFETs, and the elimination of both external gate power supply and fault detection circuit are the main advantages of this breaker concept. The proposed breaker utilizes coupled inductors, whose the primary winding is series-connected to the DC line and the secondary winding feeds the gate of a normally-ON SiC JFET via a low-voltage ASP gate driver. From experiments using a $1200V/63A$ normally-ON SiC JFET, the proposed breaker interrupted a short-circuit current of $33A$ in $330\mu s$.

7.1 Future work

The solid-state DC circuit breakers have been investigated extensively the last years due to the rapid development of LVDC and MVDC power grids. This thesis has proposed innovative concepts for tackling crucial design and operating challenges of LVDC and MVDC solid-state circuit breakers. However, there are remaining challenges when designing and operating a solid-state breaker that were not addressed in this thesis. The prospective topics for future research related to the contributions of this thesis are as follow.

- **Advanced gate drive circuits for semiconductor devices used in solid-state LVDC and MVDC breakers.** Even if the gate driver of a semiconductor device employed in solid-state breakers can be generally simple, there are advanced gate drive concepts that can be used in coordination with snubber circuits. An adaptive gate drive concept could potentially decrease the requirements for snubber circuits further.
- **Cooling system design for high-power semiconductor devices used in solid-state breakers.** The main challenge of solid-state DC breakers is the high conduction losses caused in the high-power semiconductor devices.

One key parameter that has a high impact on the conduction losses is the device junction temperature. Therefore, the design of a low-cost and low-weight cooling system that enables efficient heat dissipation is of great importance.

- **Design of ultra-fast solid-state DC breakers for multi-terminal DC grids.** Multi-terminal DC grids are under extensive research the last years due to the ever increasing penetration of renewable energy resources. One key factor when designing such a grid is the protection strategy that the grid operators will follow in case of employing the ultra-fast solid-state DC breakers. The coordination strategy of the breakers is not only critical to ensure the fast disconnection of the faulty lines, but should also be considered for the optimal electrical and thermal design of breakers. Thus, the breakers will be able to withstand fault currents during the fault clearance process.

- **Design of a high-power semiconductor device that is being utilized in solid-state breakers.** This aspect is related to the fabrication of semiconductor devices exhibiting the lowest conduction losses at a cost of increased switching times. This practice, however, is not utilized today in the semiconductors industry due to their utilization in switch-mode power converters, requiring simultaneously low conduction and switching losses.

- **Development of application-specific design and operating guidelines for solid-state DC breakers.** Such applications can be, electrified aviation, vessels, data centers, utility-scale battery energy storage, and photovoltaic solar generation. Different criteria for the design of solid-state breakers are imposed in the various application areas. Therefore, a more application-oriented design and operating guidelines for solid-state DC breakers could be an interesting topic for future research in order to optimal tune the design and operation of the breakers.

Bibliography

[1] G. Luderer, M. Pehl, A. Arvesen, T. Gibon, B. L. Bodirsky, H. S. de Boer, O. Fricko, M. Hejazi, F. Humpenöder, G. Iyer, S. Mima, I. Mouratiadou, R. C. Pietzcker, A. Popp, M. van den Berg, D. van Vuuren, and E. G. Hertwich, "Environmental co-benefits and adverse side-effects of alternative power sector decarbonization strategies," *Nature Communications 2019 10:1*, vol. 10, pp. 1–13, 11 2019.

[2] L. Shu, W. Chen, G. Ning, W. Cao, J. Mei, J. Zhao, C. Liu, and G. He, "A Resonant ZVZCS DC-DC Converter with Two Uneven Transformers for MVDC Collection System of Offshore Wind Farms," *IEEE Transactions on Industrial Electronics*, vol. 0046, no. c, pp. 1–1, 2017.

[3] S. Moury and J. Lam, "Modular isolated high frequency medium voltage (MV) step-up resonant DC / DC converters with high- gain rectifier for wind energy systems," in *2015 IEEE Energy Conversion Congress and Exposition (ECCE)*, pp. 4789–4796, 2015.

[4] M. Hossain, N. Rahim, and J. a. Selvaraj, "Recent progress and development on power DC-DC converter topology, control, design and applications: A review," *Renewable and Sustainable Energy Reviews*, vol. 81, no. July 2017, pp. 205–230, 2018.

[5] Y.-C. Liu, M.-C. Chen, C.-Y. Yang, K. A. Kim, and H.-J. Chiu, "High-Efficiency Isolated Photovoltaic Microinverter Using Wide-Band Gap Switches for Standalone and Grid-Tied Applications," *Energies 2018, Vol. 11, Page 569*, vol. 11, p. 569, 3 2018.

[6] M. A. Bahmani, T. Thiringer, and M. Kharezy, "Design methodology and optimization of a medium-frequency transformer for high-power DC-DC ap-

plications," *IEEE Transactions on Industry Applications*, vol. 52, pp. 4225–4233, 9 2016.

[7] F. Wang, Yunqing Pei, D. Boroyevich, R. Burgos, and Khai Ngo, "Ac vs. dc distribution for off-shore power delivery," in *2008 34th Annual Conference of IEEE Industrial Electronics*, pp. 2113–2118, IEEE, 11 2008.

[8] IEEE Std. 1709-2010, "IEEE Recommended Practice for 1 kV to 35 kV Medium-Voltage DC Power Systems on Ships," *DC Power Systems on Ships Working Group of the IEEE Industry Applications Society Petroleum & Chemical Industry (IAS/PCI) Committee*, vol. 1, no. November, pp. 1–54, 2010.

[9] "IEEE 1378-1997 - IEEE Guide for Commissioning High-Voltage Direct-Current (HVDC) Converter Stations and Associated Transmission Systems."

[10] "IEEE 1898-2016 - IEEE Standard for High-Voltage Direct-Current (HVDC) Composite Post Insulators."

[11] "IEC 60898-3:2019 | IEC Webstore | water management, smart city, LVDC."

[12] H. Jeong, H. Lee, Y. C. Liu, and K. A. Kim, "Review of Differential Power Processing Converter Techniques for Photovoltaic Applications," *IEEE Transactions on Energy Conversion*, vol. 34, pp. 351–360, 3 2019.

[13] W. Chen, A. Q. Huang, C. Li, G. Wang, and W. Gu, "Analysis and Comparison of Medium Voltage High Power DC/DC Converters for Offshore Wind Energy Systems," *IEEE Transactions on Power Electronics*, vol. 28, pp. 2014–2023, 4 2013.

[14] M. Stieneker, Nurhan Rizqy Averous, N. Soltau, H. Stagge, and R. W. De Doncker, "Analysis of wind turbines connected to medium-voltage DC grids," in *2014 16th European Conference on Power Electronics and Applications*, pp. 1–10, IEEE, 8 2014.

[15] M. A. Bahmani, T. Thiringer, A. Rabiei, and T. Abdulahovic, "Comparative Study of a Multi-MW High-Power Density DC Transformer with an Optimized High-Frequency Magnetics in All-DC Offshore Wind Farm," *IEEE Transactions on Power Delivery*, vol. 31, pp. 857–866, 4 2016.

[16] H. Li and D. Boroyevich, "Guest Editorial Special Issue on Emerging Electric Ship MVDC Power Technology," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 5, no. 1, pp. 1–4, 2017.

[17] G. F. Reed, B. M. Grainger, A. R. Sparacino, and Z. H. Mao, "Ship to grid: Medium-voltage dc concepts in theory and practice," *IEEE Power and Energy Magazine*, vol. 10, no. 6, pp. 70–79, 2012.

[18] Z. Jin, G. Sulligoi, R. Cuzner, L. Meng, J. C. Vasquez, and J. M. Guerrero, "Next-Generation Shipboard DC Power System: Introduction Smart Grid and dc Microgrid Technologies into Maritime Electrical Netowrks," *IEEE Electrification Magazine*, vol. 4, pp. 45–57, 6 2016.

[19] X. Guo, L. Wang, Y. Zhao, G. Wang, G. Liu, and Q. Zhong, "Reliability-Oriented Selection for Grid-Connected Converters: A Low Voltage Direct Current Microgrid Case Study," *IEEE Access*, vol. 8, pp. 205836–205847, 11 2020.

[20] M. Monadi, C. Koch-Ciobotaru, A. Luna, J. Ignacio Candela, and P. Rodriguez, "Multi-terminal medium voltage DC grids fault location and isolation," *IET Generation, Transmission & Distribution*, vol. 10, no. 14, pp. 3517–3528, 2016.

[21] A. Hinz, M. Stieneker, and R. W. De Doncker, "Impact and opportunities of medium-voltage DC grids in urban railway systems," *2016 18th European Conference on Power Electronics and Applications, EPE 2016 ECCE Europe*, 2016.

[22] G. F. Reed, B. M. Grainger, A. R. Sparacino, E. J. Taylor, M. J. Korytowski, and Z.-H. Mao, "Medium Voltage DC Technology Developments, Applications, and Trends," *CIGRE*, no. Grid of the Future Symposium, 2012.

[23] N. R. Butler, R. C. Myer, J. E. Petry, S. S. Normand, D. M. Robinson, M. P. J. Gaudreau, and W. J. Beckman, "Undersea MVDC power distribution," *Proceedings of the 2010 IEEE International Power Modulator and High Voltage Conference, IPMHVC 2010*, pp. 294–297, 2010.

[24] G. J. M. De Sousa and M. L. Heldwein, "Three-phase unidirectional modular multilevel converter," *2013 15th European Conference on Power Electronics and Applications, EPE 2013*, no. Dcc, 2013.

[25] H. I. Bahari and S. S. M. Shariff, "Review on data center issues and challenges: Towards the Green Data Center," in *2016 6th IEEE International Conference on Control System, Computing and Engineering (ICCSCE)*, pp. 129–134, IEEE, 2016.

[26] B. Cutler, S. Fowers, J. Kramer, and E. Peterson, "Dunking the data center," *IEEE Spectrum*, vol. 54, pp. 26–31, 3 2017.

[27] G. Allee and W. Tschudi, "Edison redux: 380 Vdc brings reliability and efficiency to sustainable data centers," *IEEE Power and Energy Magazine*, vol. 10, no. 6, pp. 50–59, 2012.

[28] D. Gerber, V. Vossos, W. Feng, A. Khandekar, C. Marnay, and B. Nordman, "A simulation based comparison of AC and DC power distribution networks in buildings," *2017 IEEE 2nd International Conference on Direct Current Microgrids, ICDCM 2017*, pp. 588–595, 2017.

[29] M. Stieneker and R. W. D. Doncker, "Medium-Voltage DC Distribution Grids in Urban Areas," *2016 IEEE 7th International Symposium on Power Electronics for Distributed Generation Systems (PEDG)*, pp. 0–6, 2016.

[30] F. Mura and R. W. De Doncker, "Design aspects of a medium-voltage direct current (MVDC) grid for a university campus," *8th International Conference on Power Electronics - ECCE Asia: "Green World with Power Electronics", ICPE 2011-ECCE Asia*, no. Mvdc, pp. 2359–2366, 2011.

[31] C. Yuan, M. a. Haj-ahmed, and M. Illindala, "Protection Strategies for Medium Voltage Direct Current Microgrid at a Remote Area Mine Site," *IEEE Transactions on Industry Applications*, vol. 9994, no. c, pp. 1–1, 2015.

[32] G. Buticchi, M. Liserre, and K. Al-Haddad, "On-Board Microgrids for the More Electric Aircraft," *IEEE Transactions on Industrial Electronics*, vol. 66, pp. 5585–5587, 7 2019.

[33] T. C. Cano, A. Rodrmguez, D. G. Lamar, I. Castro, L. Albiol-Tendillo, Y. F. Khalil, and P. Kshirsagar, "Future of Electrical Aircraft Energy Power Systems: An architecture review.," *IEEE Transactions on Transportation Electrification*, 2021.

[34] H. Schefer, L. Fauth, T. H. Kopp, R. Mallwitz, J. Friebe, and M. Kurrat, "Discussion on Electric Power Supply Systems for All Electric Aircraft," *IEEE Access*, vol. 8, pp. 84188–84216, 2020.

[35] M. Monadi, M. Amin Zamani, J. Ignacio Candela, A. Luna, and P. Rodriguez, "Protection of AC and DC distribution systems Embedding distributed energy resources: A comparative review and analysis," *Renewable and Sustainable Energy Reviews*, vol. 51, pp. 1578–1593, 11 2015.

[36] M. Callavik, A. Blomberg, J. Häfner, and B. Jacobson, "The hybrid HVDC breaker An innovation breakthrough enabling reliable HVDC grids," *ABB Review*, vol. Tech. Rep., no. 2, 2012.

[37] A. H. Chang, B. R. Sennett, A. T. Avestruz, S. B. Leeb, and J. L. Kirtley, "Analysis and Design of DC System Protection Using Z-Source Circuit Breaker," *IEEE Transactions on Power Electronics*, vol. 31, no. 2, pp. 1036–1049, 2016.

[38] L. Yuan, L. Sun, and H. Wu, "Simulation of Fault Arc Using Conventional Arc Models," *Energy and Power Engineering*, vol. 05, pp. 833–837, 6 2013.

[39] ABB, "5SNA 3000K452300," tech. rep., 2017.

[40] M. G. Aghdam and T. Thiringer, "Comparison of SiC and Si power semiconductor devices to be used in 2.5 kw dc/dc converter," *Proceedings of the International Conference on Power Electronics and Drive Systems*, pp. 1035–1040, 2009.

[41] J. Biela, M. Schweizer, S. Waffler, and J. W. Kolar, "SiC versus Si - Evaluation of potentials for performance improvement of inverter and DCDC converter systems by SiC power semiconductors," *IEEE Transactions on Industrial Electronics*, vol. 58, no. 7, pp. 2872–2882, 2011.

[42] F. Liu, W. Liu, X. Zha, H. Yang, and K. Feng, "Solid-state circuit breaker snubber design for transient overvoltage suppression at bus fault interruption in low-voltage DC microgrid," *IEEE Transactions on Power Electronics*, vol. 32, pp. 3007–3021, 4 2017.

[43] M. Monadi, C. Gavriluta, A. Luna, I. Candela, and P. Rodriguez, "Centralized Protection Strategy for Medium Voltage DC Microgrids," *IEEE Transactions on Power Delivery*, vol. 32, no. 1, pp. 1–1, 2016.

[44] N. Kaminski, "State of the art and the future of wide band-gap devices | IEEE Conference Publication | IEEE Xplore," in *2009 13th European Conference on Power Electronics and Applications*, 2009.

[45] N. Iwamuro and T. Laska, "IGBT history, state-of-the-art, and future prospects," *IEEE Transactions on Electron Devices*, vol. 64, no. 3, pp. 741–752, 2017.

[46] S. Hazra, A. De, L. Cheng, J. Palmour, M. Schupbach, B. A. Hull, S. Allen, and S. Bhattacharya, "High Switching Performance of 1700-V, 50-A SiC Power MOSFET over Si IGBT/BiMOSFET for Advanced Power Conversion Applications," *IEEE Transactions on Power Electronics*, vol. 31, pp. 4742–4754, 7 2016.

[47] C. Abbate, G. Busatto, and F. Iannuzzo, "High-voltage, high-performance switch using series-connected IGBTs," *IEEE Transactions on Power Electronics*, vol. 25, no. 9, pp. 2450–2459, 2010.

[48] D. Peftitsis, G. Tolstoy, A. Antonopoulos, J. Rabkowski, J. K. Lim, M. Bakowski, L. Ängquist, and H. P. Nee, "High-power modular multilevel converters with SiC JFETs," *IEEE Transactions on Power Electronics*, vol. 27, no. 1, pp. 28–36, 2012.

[49] X. She, A. Q. Huang, O. Lucia, and B. Ozpineci, "Review of Silicon Carbide Power Devices and Their Applications," *IEEE Transactions on Industrial Electronics*, vol. 64, no. 10, pp. 1–1, 2017.

[50] Y. Ren, X. Yang, F. Zhang, K. Wang, W. Chen, L. Wang, and Y. Pei, "A Compact Gate Control and Voltage-Balancing Circuit for Series-Connected SiC MOSFETs and Its Application in a DC Breaker," *IEEE Transactions on Industrial Electronics*, vol. 64, pp. 8299–8309, 10 2017.

[51] J. Millan, P. Godignon, X. Perpina, A. Perez-Tomas, and J. Rebollo, "A Survey of Wide Bandgap Power Semiconductor Devices," *IEEE Transactions on Power Electronics*, vol. 29, no. 5, pp. 2155–2163, 2014.

[52] S. Anwar, Z. J. Wang, and M. Chinthavali, "Characterization and Comparison of Trench and Planar Silicon Carbide (SiC) MOSFET at Different Temperatures," *2018 IEEE Transportation and Electrification Conference and Expo, ITEC 2018*, pp. 956–960, 8 2018.

[53] D. Pappis, L. de Menezes, and P. Zacharias, "Comparison of the short circuit capability of planar and trench sic mosfets," in *PCIM Europe 2017; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management*, pp. 1–9, 2017.

[54] S. Chen, A. Liu, J. He, S. Bai, and K. Sheng, "Design and Application of High-Voltage SiC JFET and Its Power Modules," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 4, no. 3, pp. 780–789, 2016.

[55] Z. Miao, G. Sabui, A. M. Roshandeh, and Z. J. Shen, "Design and Analysis of DC Solid-State Circuit Breakers Using SiC JFETs," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 4, no. 3, pp. 863–873, 2016.

[56] Z. J. Shen, G. Sabui, Z. Miao, and Z. Shuai, "Wide-bandgap solid-state circuit breakers for DC power systems: Device and circuit considerations," *IEEE Transactions on Electron Devices*, vol. 62, no. 2, pp. 294–300, 2015.

[57] V. Veliadis, H. Hearne, E. J. Stewart, H. C. Ha, M. Snook, T. McNutt, R. Howell, A. Lelis, and C. Scozzie, "Investigation of the suitability of 1200-V normally-off recessed-implanted-gate SIC VJFETs for efficient power-switching applications," *IEEE Electron Device Letters*, vol. 30, no. 7, pp. 736–738, 2009.

[58] G. Bathurst, G. Hwang, and L. Tejwani, "MVDC - The New Technology for Distribution Networks," in *11th IET International Conference on AC and DC Power Transmission*, pp. 027 (5 .)–027 (5 .), Institution of Engineering and Technology, 2015.

[59] A. Q. Huang, "Power Semiconductor Devicesfor Smart Grid and Renewable Energy Systems," *Proceedings of the IEEE*, pp. 1–29, 2017.

[60] M. Arnold, A. Antoniazzi, M. Rahimo, D. Pessina, and U. Vemulapati, "Reverse blocking IGCT optimised for 1 kV DC bi-directional solid state circuit breaker," *IET Power Electronics*, vol. 8, pp. 2308–2314, 12 2015.

[61] M. Rahimo, A. Kopta, U. Schlapbach, J. Vobecky, R. Schnell, and S. Klaka, "The Bi-mode Insulated Gate Transistor (BIGT) a potential technology for higher power applications," in *2009 21st International Symposium on Power Semiconductor Devices & IC's*, pp. 283–286, IEEE, 6 2009.

[62] K. Lawson, S. B. Bayne, S. Lacouture, L. Cheng, H. O'brien, A. Ogunniyi, and C. Scozzie, "Safe operating area and long-term reliability of 9-kV silicon carbide PNPN super gate turn-off thyristors," *IEEE Electron Device Letters*, vol. 35, no. 8, pp. 862–864, 2014.

[63] X. Song, A. Q. Huang, M. C. Lee, and C. Peng, "Theoretical and Experimental Study of 22 kV SiC Emitter Turn-OFF (ETO) Thyristor," *IEEE Transactions on Power Electronics*, vol. 32, no. 8, pp. 6381–6393, 2017.

[64] F. Agostini, U. Vemulapati, D. Torresin, M. Arnold, M. Rahimo, A. Antoniazzi, L. Raciti, D. Pessina, and H. Suryanarayana, "1MW bi-directional DC solid state circuit breaker based on air cooled reverse blocking-IGCT," in *2015 IEEE Electric Ship Technologies Symposium (ESTS)*, pp. 287–292, IEEE, 6 2015.

[65] K. A. Saleh, A. Hooshyar, and E. F. El-Saadany, "Ultra-high-speed travelling-wave-based protection scheme for medium-voltage DC microgrids," *IEEE Transactions on Smart Grid*, vol. 10, pp. 1440–1451, 3 2019.

[66] W. Li, A. Monti, and F. Ponci, "Fault detection and classification in medium voltage dc shipboard power systems with wavelets and artificial neural networks," *IEEE Transactions on Instrumentation and Measurement*, vol. 63, pp. 2651–2665, 11 2014.

[67] Z. Dongye, L. Qi, K. Liu, X. Wei, F. Lu, and X. Cui, "Overvoltage Estimation by Stray Inductances During Turn-Off of a 500 kV/25 kA DC Circuit Breaker," *IEEE Transactions on Power Electronics*, pp. 1–1, 12 2020.

[68] R. Withanage and N. Shammas, "Series connection of Insulated Gate Bipolar Transistors (IGBTs)," *IEEE Transactions on Power Electronics*, vol. 27, no. 4, pp. 2204–2212, 2012.

[69] K. Sasagawa, Y. Abe, and K. Matsuse, "Voltage-balancing method for IGBTs connected in series," *IEEE Transactions on Industry Applications*, vol. 40, pp. 1025–1030, 7 2004.

[70] X. Yang, J. Zhang, W. He, Z. Long, and P. R. Palmer, "Physical Investigation into Effective Voltage Balancing by Temporary Clamp Technique for the Series Connection of IGBTs," *IEEE Transactions on Power Electronics*, vol. 33, pp. 248–258, 1 2018.

[71] L. Feng, R. Gou, F. Zhuo, X. Yang, and F. Zhang, "Development of a 10kV solid-state DC circuit breaker based on press-pack IGBT for VSC-HVDC system," in *2016 IEEE 8th International Power Electronics and Motion Control Conference, IPEMC-ECCE Asia 2016*, pp. 2371–2377, Institute of Electrical and Electronics Engineers Inc., 7 2016.

[72] S. Yu, T. Lu, Z. Zhao, and S. Ji, "Behavior model for series connected high voltage IGBTs," in *IEEE Transportation Electrification Conference and Expo, ITEC Asia-Pacific 2014 - Conference Proceedings*, Institute of Electrical and Electronics Engineers Inc., 10 2014.

ISBN 978-82-326-5896-1 (printed ver.)
ISBN 2978-82-326-6016-2 (electronic ver.)
ISSN 1503-8181 (printed ver.)
ISSN 2703-8084 (online ver.)

NTNU

Norwegian University of
Science and Technology