Master's thesis

NTNU
Norwegian University of Science and Technology
Faculty of Information Technology and Electrical Engineering
Department of Electronic Systems

Solveig Skavnes

Design and Implementation of a Magnetic Energy Harvesting System for Low Primary Current Applications

Master's thesis in Electronic Systems Design and Innovation
Supervisor: Snorre Aunet
Co-supervisor: Øystein Moldsvor, Anders Ivar Hagen
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Abstract

Energy harvesting is the act of exploiting small amounts of ambient energy to power a low power system, like a sensor node. This can be done from the magnetic fields originating from an AC current, I_P, flowing through a power cable. The aim of this thesis is a system that is able to deliver 3.3 V to charge a battery, while I_P is under 1 A. The system should work for I_Ps under 1 A, since this will allow it to charge a battery a lot of the time even if the cable it is connected to is not carrying high AC currents. A magnetic energy harvesting system can consist of a current transformer (CT), a rectifier and a DC/DC converter. Such a system is designed, simulated using SPICE and implemented using components on a breadboard. The different sub-systems are tested individually and together. Five different commercial CTs are tested. Three different rectifiers are designed and tested, and two DC/DC converters are tested. This makes a total of 30 sub-system configurations, of which three fulfil the requirement of working at $I_P < 1\ A$. The combination of sub-systems that manages to deliver 3.3 V to a battery on the lowest I_P is the combination of a CT with a 1:2000 turn ratio, a schottky diode rectifier and a high input resistance DC/DC converter. This system delivers 3.3 V to an attached battery at $I_P = 0.5$ A. It is tested and verified that the three sub-system configurations that work at $I_P < 1\ A$ continue to work up to $I_P = 16$ A. A commercial energy harvesting system with a combined rectifier and DC/DC is tested with the five CTs under the same conditions as a comparison. This is the LTC3331, and together with the best performing CT, it requires $I_P = 5$ A to deliver 3.3 V to a battery, making the commercial solution significantly worse than the system designed in this thesis.

Samandrag

Energihausting er å utnytte små mengder omkringliggjande energi for å drive eit lavenergisystem, slik som for eksempel ei sensornode. Dette kan gjerast frå magnetfelta som kjem frå ein vekselstraum, I_P, som går gjennom ei leidning. Målet med masteroppgåva er å utvikle eit system som klarer å levere 3,3 V ut for å lade eit batteri, mens I_P er under 1 A. Systemet burde fungere for $I_P$ar under 1 A, sidan dette mogleggjer at systemet kan lade eit batteri mykje av tida, sjølv om det ikkje går høge vekselstraumar gjennom leidninga. Eit magnetisk energihaustingssystem kan bestå av ein straumtransformator (engelsk: Current Transformer) eller CT, ein likerettar og ein DC/DC-omformar. Eit slikt system er designa, simulert ved bruk av SPICE og implementert ved å bruke komponentar på eit breadboard. Dei ulike undersystema er testa individuelt og saman. Fem ulike CTar er testa. Tre ulike likerettarar er designa og testa, og to ulike DC/DC-omformarar er testa. Dette blir totalt 30 undersystemkonfigurasjonar, kor tre av dei oppfyller kravet om å fungere ved $I_P < 1\ A$. Den kombinasjonen av undersystem som klarar å levere 3,3 V ut med den lavaste I_P inn er kombinasjonen av ein CT med 1:2000 vindingsforhold, ein likerettar basert på schottkydioder og ein DC/DC-omformar som har ein høg inngangsmotstand. Dette systemet leverer 3,3 V ut ved $I_P = 0{,}5$ A. Dei tre undersystemkonfigurasjonane som oppfyller kravet er alle saman testa og verifisert at dei fungerer opp til $I_P = 16$ A. Eit kommersielt energihaustingssystem med kombinert likerettar og DC/DC-omformar er testa som ei samanlikning, med dei same fem CTane testa tidlegare. Dette systemet er LTC3331 og saman med ein CT med 1:2000 viklingsforhold treng dette systemet $I_P = 5$ A for å levere 3,3 V ut, noko som er signifikant dårlegare enn det beste systemet som er designa og testa i denne masteroppgåva.

Preface

This master thesis is written as a part of the study program Electronic Systems Design and Innovation. The program is part of the Department of Electronic Systems (IES) at the Norwegian University of Science and Technology (NTNU) in Trondheim, Norway. The thesis is finished in June of 2021.

The original project was set forth by Disruptive Technologies. A thank you is sent to them for help on the project, as well as procuring the necessary components and hardware for the testing phase. Thank you to my supervisor Øystein Moldsvor from Disruptive Technologies, and Snorre Aunet and Anders Ivar Hagen from IES at NTNU. Their contributions are much appreciated.

A special thanks is sent to my fellow master students for fruitful discussions and company on long study nights.

In the autumn of 2020 a related project to this thesis was conducted. The title of the project report was "Investigation of Coil Geometries for Energy Harvesting of Magnetic Fields from 50 Hz Household Power Cables". The project mostly focused on different coil geometries for optimal energy harvesting from magnetic fields, and not on the circuitry for exploiting the energy to charge a battery. The coils developed are not used in this thesis, as commercially available coils were considered superior. It is a report on a related subject, but with a scope that is very different, and is therefore not very relevant. The work presented in this thesis is entirely work done in the spring semester of 2021.

A note should be taken if one wants to print this master thesis, that it should be printed in colour. This is because many of the figures rely on colours that can be hard to distinguish if printed in black and white.

Contents

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Abbreviations

AC	Alternating Current
AC/DC	AC to DC converter, also called rectifier
CT	Current Transformer
DC	Direct Current
DC/DC	DC to DC converter
DWCT	Dual Wire Current Transformer
EH	Energy Harvesting
GUI	Graphical User Interface
IoT	Internet of Things
KCL	Kirchoffs Current Law
MF	Magnetic Fields
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
NMOS	N-type Metal Oxide Semiconductor
PCB	Printed Circuit Board
PMOS	P-type Metal Oxide Semiconductor
RMS	Root Mean Square
TR	Turn Ratio
WSN	Wireless Sensor Network

1 Introduction

Both Wireless Sensor Networks (WSN) and the Internet of Things (IoT) bring endless possibilities for small wireless sensors to exist everywhere. With them, come several more wireless sensors nodes. These nodes can be very useful for different applications. Used correctly they can even lower power consumption of common households [1].

All such sensor nodes have one problem in common, they need power in order to work. Even though many such sensor nodes can use a very low amount of power, they still make use of batteries, which at some point either need to be changed for the sensor node to keep working, or the whole sensor node becomes useless and will be thrown away. As these sensor nodes become increasingly more common they will also generate more and more waste. In addition, such nodes can have many purposes, and be placed many inconvenient places, making changing their batteries a difficult and time consuming task.

A way to avoid this problem of battery changing is to recharge the batteries little by little where they are, while they are in use, with energy that is already present around them. This concept of exploiting small amounts of ambient energy to charge a battery, or to power a sensor node, is called Energy Harvesting (EH). According to [2], page 541 "[...] energy harvesting can be defined as the collection of local naturally available energy for local use. Most often it involves small systems with tiny amounts of power, in the range from nanowatts to hundreds of milliwatts."

In principle, one can harvest energy from a wide variety of sources. This includes solar power, wind power, temperature differences, mechanical movement and more [3]. Figure 1.1, based on a figure from [2], shows one way of partitioning energy harvesting into different categories.

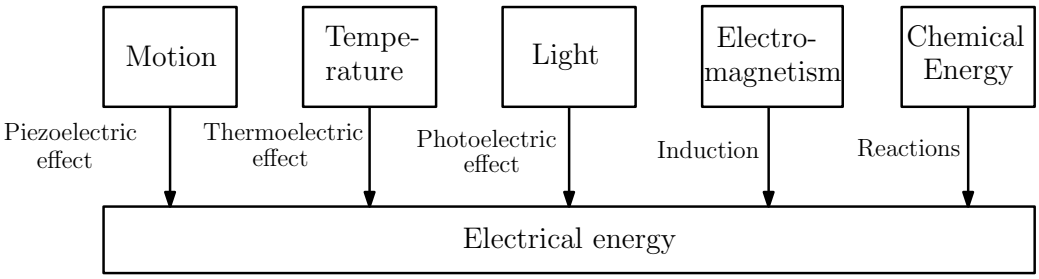


Figure 1.1: Some categories of energy and how to harvest them.

The focus of this paper will be on the category of Electromagnetic radiation, or more specifically, Magnetic Fields (MF) that originate from Alternating Current (AC) flowing through wires. As shown in Figure 1.1, induction can be used to turn electromagnetic radiation into electrical energy, which again can be used to charge a battery.

The use of energy harvesting to power wireless sensor nodes, like the ones used in IoT, is not a new idea. Many have tried this before, including [4]. They used light, changes in temperature, motion and electromagnetic fields to power wireless sensor nodes. The use of energy harvesting from magnetic fields is not as widespread. While some have worked with this in the past, like [5] and [6], most solutions are big and chunky, and require large primary currents to work. For applications requiring mounting EH systems on common household wires, it is desirable to have a system that can work on currents that are as low as possible, seeing as a lot of the time the currents flowing through such wires are low.

This thesis looks into using magnetic energy harvesting on common household wires

that carry AC currents at a frequency of 50 Hz. 50 Hz is chosen because it is the frequency of the power grid in Europe [7]. These kinds of currents are often in the range of 0-16 A, depending on the fuse. In Figure 1.2, an EH system converts magnetic energy, originating from a primary current I_P, into a DC voltage V_{Bat}, that can either power a sensor node directly, or be used to charge a battery.

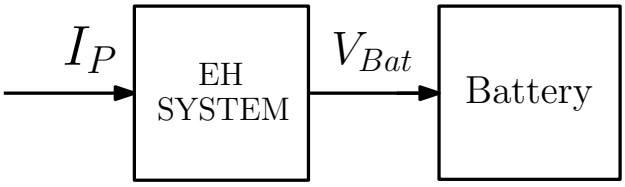


Figure 1.2: A block diagram of the energy harvesting system that converts magnetic energy from the primary current I_P into a DC voltage V_{Bat} that can charge a battery.

Energy harvesting of magnetic fields allows for energy harvesting in places where other, more common sources are unavailable. For instance if one wants to place sensors in walls of public buildings like schools, hospitals, offices or malls to monitor temperatures, humidity or power usage, there is no sunlight available for solar panels, no wind or no movement for piezoelectric elements. Using the alternating magnetic fields originating from the electric wires present in such areas, allow for extended life for sensor nodes placed there.

Charging batteries with energy from wires makes the available energy very dependent on the amount of current flowing through the wires at any given moment. There is no guarantee that there will be large currents flowing in the wire, so to make the system function as much of the time as possible, it is beneficial to optimise the system to charge a battery with as low primary currents as possible.

Electromagnetic induction [8] can be used to convert a magnetic field into an electric one. For this to be possible, the magnetic field needs to be alternating. Alternating magnetic fields are located around all electrical wires carrying an alternating current. Close to these wires a Current Transformer (CT) can use the magnetic fields to transform the primary current I_P into a smaller secondary current I_S. When connected to a load, this current produces an alternating voltage V_{AC}.

Because batteries and electronic circuits in general tend to run on Direct Current (DC), an AC to DC converter (AC/DC) or rectifier is needed to convert V_{AC} into V_{DC}. After the conversion to a direct voltage V_{DC}, the voltage has to be DC/DC converted to reach the level V_{Bat} required to charge a battery.

The EH system can therefore be broken down into three sub-systems as shown in Figure 1.3. In this figure a primary current I_P flows in an electrical wire. Then the CT converts this into a AC current that gives the voltage V_{AC} when connected to the rectifier circuit. The rectifier circuit transforms the alternating voltage into a DC voltage V_{DC}, that the DC/DC converter converts to the required voltage level V_{Bat} that a battery needs to be charged.

Figure 1.3: A block diagram of the magnetic energy harvesting system that contains a CT, a rectifier and a DC/DC converter.

Problem description

The problem that this thesis focuses on is how to design a magnetic energy harvesting system that can charge a 3.3 V battery. The aim is to have a system that can work with a primary current I_P being under 1 A. The reason for this is as follows: At any given time, one can not know how much current is flowing in a common household wire. If a house has 16 A fuses, the maximum current that can flow in a wires connected to that fuse is 16 A. However, most of the time the current flowing in the wire will be less than that. The current flowing at any given time is dependent on what it is being used for. This can be something that requires a lot of power, like a cooking plate, or it can be something that requires almost no power at all, like a light bulb. If it is desired to charge a battery with energy from a magnetic field that may often be very small, it would be beneficial to have an EH system that can work on those very small fields. Then the system can continuously charge the battery little by little as the sensor node is using it, and not depend on the current flowing in the wire having to be large. If the EH system can charge a battery when I_P is less than 1 A, it is considered likely that the system will be working most of, or at least a lot of, the time. This is of course only true if the system works for all currents up to the fuse current, which in this thesis is assumed to be 16 A.

The EH system will comprise of a CT, a rectifier and a DC/DC converter. For the CT and DC/DC converter there are many commercial solutions out there. Therefore the focus of this thesis will lie on looking into a rectifier that can work with an available CT and DC/DC converter, as well as mapping the requirements the different sub-systems need to meet when connected to each other for the whole system to work as often as possible. The number of amperes out of the system, or the power out from it, is not the most crucial part of the system, as many wireless sensor nodes use very little current. If the system can deliver 3.3 V out as much of the time as possible, there is no need for a high power output. It is considered that having a system that works on I_P less than 1 A will result in a system that works more of the time. Therefore the aim of the thesis is to design and implement a system that achieves this.

Problem scope

The scope of this thesis is to simulate, build and test the different sub-systems individually, as well as together, to investigate the different requirements the sub-systems need to meet to make a complete system that can deliver 3.3 V out to a battery with an I_P under 1 A.

It is not in the scope of this thesis to look into how to make an finished industrial product that can be easily installed by a consumer. The goal is simply to prove that energy harvesting of magnetic field from I_P that is lower than 1 A is possible.

Thesis structure

The structure of this thesis is as follows. After Section 1 - Introduction, Section 2 - Theoretical Background follows. It will describe all the necessary background theory needed to understand the rest of the work as well as showing an overview of related work. Then, Section 3 - Methodology describes the methodology used, and how the systems are simulated, implemented and tested. Section 4 - Results describes the results of the tests and simulations conducted, and Section 5 - Discussion discusses them. Section 6 - Conclusion concludes, before Section 7 - Future Work explains what future work needs to be done to improve the system. At the very end, the Appendices are placed, containing supplementary information, netlists and figures.

2 Theoretical Background

This section will present all the information it is necessary to know before going into the methodology and the implementation of the system.

2.1 Related work

This section will look into a selection of papers that are relevant to the work in this thesis. Many papers have been written that are relevant to magnetic energy harvesting. A selection of them will be presented in this section, with highlights of why they are relevant, and why they are insufficient for the problem described under Problem description.

[9] discusses a system for energy harvesting that is completely input powered. It is comprised of an AC/DC converter and a DC/DC converter. A problem with the system in this paper is that it is not primarily made for magnetic energy harvesting, and thus is not optimised for low input voltages. The system in the paper needs at least 0.6 V amplitude in to work, and at least 1 V to work optimally. It is also only tested with a voltage generator as source, and not an actual energy harvester.

[6] describes a full system for magnetic energy harvesting and power monitoring combined. It is designed to be mounted on a wire carrying AC current, without having to destroy the wire in any way to install the system. The energy harvesting part of the system contains a CT, a rectifier and a DC/DC converter. The harvested energy is used to charge a battery, which again powers the sensor and transceiver functionality. The system is tested at primary currents down to 4 A. The problem with this system is that it is not made with a commercial CT. Instead they use a custom Dual Wire Current Transformer (DWCT). This DWCT is hard and expensive to manufacture.

[10] focuses on active rectification, and the advantages this has over passive rectification. It discusses different ways to achieve active rectification. The paper contains several circuit diagrams of different solutions for rectifiers for use with energy harvesters. This includes one they call a passive rectifier that is based on MOSFET transistors, and an active rectifier that includes an active diode. The paper does however not test the rectifiers together with energy harvester circuits, even though it is stated that the intended application is electromagnetic harvesting, nor is the rectified voltage boosted to a level a battery can use.

[5] does harvest magnetic energy from AC current going through a wire, using a CT. They argue that adding a switch plus a capacitor helps increasing the amount of power one can harvest, because that keeps the CT out of saturation. They propose a promising system, but do not test it on primary currents lower than 10 A. The final output from their system is not a 3.3 V DC voltage.

[11] describes a system designed to replace 3.3V battery using magnetic energy harvesting. This is a system trying to accomplish the same goal as this thesis, but have a different starting point. They do not assume that the magnetic fields they want to harvest from are originating from a wire carrying AC current, but rather that there are stray magnetic fields present that can be harvested. The fields they are using have a magnetic flux density of minimum 200 μT, which is not something that would be present in an environment other than in specific factories using heavy machinery. This means that the coil that they use as the first step in their EH system, is not usable in the case that this thesis examines. However, the rest of the system is very similar. They have a rectifier and a DC/DC converter. The rectifier is a diode bridge rectifier, and the DC/DC converter is a step down converter, since the voltages they get from their coil in the case of 200 μT present are much higher than the ones originating from a 1 A AC current.

Comparisons

For an easier overview, the key elements of the systems presented in the papers [9], [6], [10], [5] and [11] are presented in Table 1.

Table 1: Key elements of magnetic energy harvesting systems in the relevant papers.

Article	**[9]**	**[6]**	**[10]**	**[5]**	**[11]**
Published	2011	2015	2014	2017	2017
Energy source	Vibrational energy	Magnetic fields	Electro-magnetism	MF from AC	Stray magnetic fields
EH component	NaN	DWCT	NaN	CT	Brooks coil
Tested on	1 V-3 V	4 A-10 A	0.8 V-2 V	10 A	350 μT
P out	3.9 mW	1.89 mW	13.6 mW	792 mW	104 mW
V out	3 V	2.2 V-4.7 V	0.5 V	6 V, peak	3.3 V
R Load	2 kΩ	NaN	40 Ω	20 Ω	100 Ω
Rectifier component	MOSFETs	MOSFETs	MOSFETs	Diodes	Diodes
Min. req. to work	0.6 V	4 A	0.8 V	NaN	200 μT
Implementation	0.5 μm CMOS	0.25 μm CMOS	PCB	Breadboard	Veroboard
Efficiency	60 %	82 %	95 %	NaN	49 %

To summarise; some previous papers have worked on making a magnetic energy harvesting system. None of the ones mentioned here focus on optimising for low primary currents to charge a battery. Many also use CTs that are not commercially available, and that can be difficult and expensive to manufacture.

This thesis will therefore try to answer these questions: What are the basic relations one needs to consider when designing a energy harvesting system? What are the most important attributes of the different sub-systems? And what is needed to have magnetic energy harvesting system that works on sub 1 A primary currents?

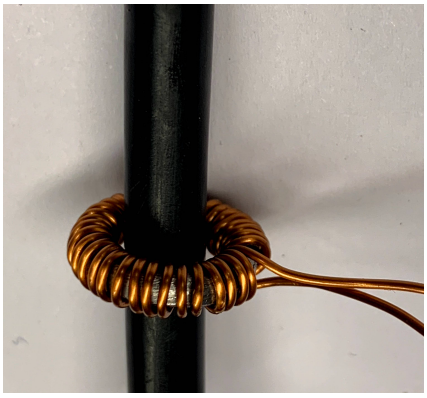
2.2 Theory

This section is an overview of the theory that is necessary to understand the rest of the work in this paper. It is organised so that each sub-system in the EH system has its own sub-section that explains the theory needed to understand them. In addition there is a sub-section explaining what to expect when the different parts are put together as one.

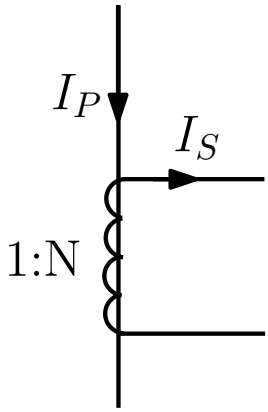
2.2.1 Current Transformers

The first sub-system of the EH system is the Current Transformer, or the CT. This is the step that exploits the physics of electromagnetic induction to transform a primary current I_P in a wire into a smaller secondary current I_S that the EH system can use to power a battery or a sensor node.

Figure 2.1 shows a typical CT located around a wire as both a picture and a circuit symbol. Figure 2.1a shows a picture of a CT located around a wire. The picture is of one of the CTs created in the project mentioned in Preface. Figure 2.1b shows how I_P is flowing in the primary wire, and how I_S is flowing from the output wires of the CT. N is the number of windings in the CT, and 1:N is the Turn Ratio (TR).



(a) Picture of a toroidal shaped CT with a high permeability core located around a wire.



(b) Circuit symbol of a CT.

Figure 2.1: A CT located around a wire as both a picture (a) and a circuit symbol (b).

The electromagnetic induction that induces the current I_S is described by two equations: The Maxwell Faraday equation (1) [12] and Ampère's law (2) [12]. Together these two laws explain why the current I_S has to be an AC current. Ampère's law describes how a changing electric field $\frac{\partial \mathbf{E}}{\partial t}$ and a current source $\mathbf{J}$ both can create a changing magnetic field. The equation also contains the constants for magnetic permeability in vacuum μ_0 and electric permittivity in vacuum ϵ_0. The Maxwell Faraday equation then states that a changing magnetic flux density, $\frac{\partial \mathbf{B}}{\partial t}$, creates a curled electric field around it, $\nabla \times \mathbf{E}$. It is this changing electric field that in turn creates the AC current I_S. It is therefore not possible for I_S to be a DC current.

$$\nabla \times \mathbf{E} = -\frac{\partial \mathbf{B}}{\partial t} \tag{1}$$

$$\nabla \times \mathbf{B} = \mu_0 \mathbf{J} + \mu_0 \epsilon_0 \frac{\partial \mathbf{E}}{\partial t} \tag{2}$$

The CT can be modeled as an equivalent circuit. Figure 2.2 shows a circuit model of a CT based on [13].

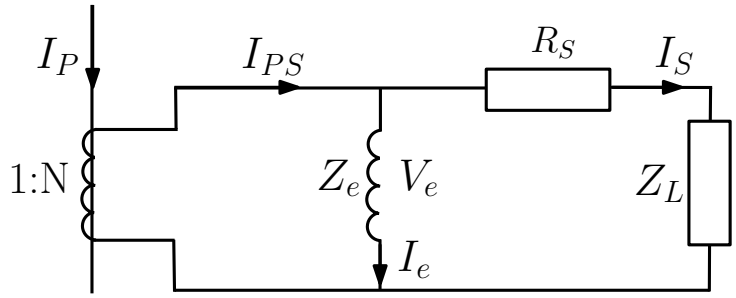


Figure 2.2: CT equivalent circuit model.

The symbols in this figure are:

- I_P - Primary current
- I_{PS} - Ideal secondary current
- I_S - Secondary current
- I_e - Excitation current
- Z_e - Excitation impedance
- V_e - Excitation voltage
- R_S - Secondary winding resistance
- Z_L - Load impedance

Kirchoffs Current Law (KCL) [14] states that the following must be true: $I_S = I_{PS} - I_e$. That means that the secondary current is equal to the ideal secondary current minus the excitation current I_e.

There are also many equations describing a CT as a transformer. A Current Transformer's Turn Ratio (TR) is defined as in Equation (3) [15].

$$TR = \frac{N_P}{N_S} = \frac{I_{PS}}{I_P} \tag{3}$$

Here, N_P is the number of primary windings, and N_S is the number of secondary windings. In a CT N_P is usually 1. This means that one can write the secondary current as a function of the turn ratio, primary current and excitation current:

$$I_S = I_P \cdot TR - I_e \tag{4}$$

The ratio between the inductance on the primary side L_P and the inductance on the secondary side L_S has a square relationship to the TR. This is shown in Equation (5) [16].

$$\frac{L_P}{L_S} = TR^2 = \left(\frac{N_P}{N_S}\right)^2 \tag{5}$$

The excitation impedance Z_e in Figure 2.2 is not constant as I_P changes. In a real CT, the magnetic flux density to the magnetic field strength is a hysteresis curve, meaning that at some point the CT saturates [17]. This can be modeled in the CT model by adjusting the size of Z_e so that I_e become very large at high I_P (when the core is saturated), making I_S very small. The exact physics behind this is not in the scope of this thesis to describe, but more information on the physics CT saturation can be found in [17].

2.2.2 DC/DC converter

After the signal has been rectified, it will not necessarily be at the right level to charge a battery. Given a low I_P, V_{DC} might also be low. At high I_Ps V_{DC} might be too high. If the desired level of V_{bat} is 3.3 V, it is necessary to have a DC/DC converter to transfer the voltage to that level. There are many commercially available converters that can do this job. A hypothesis is put forward that the most important characteristic of a DC/DC converter to be used in this EH system should be

- Being able to deliver 3.3 V output with the input voltage being as low as possible.

In addition, the input impedance should be in the same range as the output impedance of the rectifier, to ensure maximal power transfer, as stated by the maximum power transfer theorem [18]. As many datasheets do not state the input impedance explicitly, it is not simple to just buy a DC/DC converter with perfect input impedance.

2.2.3 Rectifiers

As previously stated, in its nature, I_S is an AC current, making an AC voltage when connected to a load. In order to charge a battery, a DC voltage is needed. It is therefore necessary for the EH system to include a rectifier. The types of rectifier that different papers previously have used is listed in section 2.1, Table 1. There are primarily two types that have been used; diode bridge rectifiers and MOSFET based rectifiers. Both these types will be discussed here.

Diode bridge rectifier

A common way to rectify single phase signals is using a using a full-wave diode bridge rectifier [19]. A circuit diagram of such a rectifier is shown in Figure 2.3.

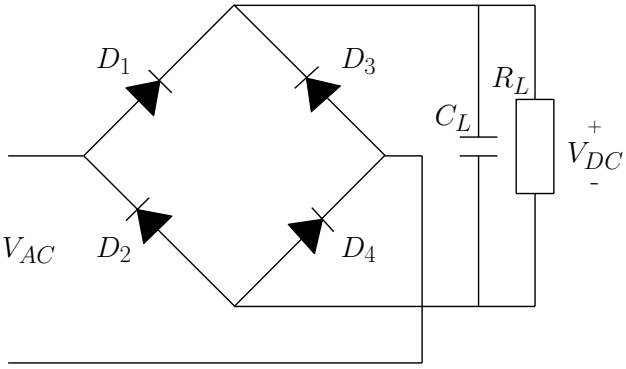


Figure 2.3: Circuit diagram of standard diode bridge rectifier with load. V_{DC} is a DC voltage if the load is large enough.

The rectifier in Figure 2.3 consists of four identical diodes, D_1, D_2, D_3 and D_4. A load is connected to the rectifier, consisting of a resistor R_L and a capacitor C_L. The input signal V_{AC} becomes rectified to the output signal V_{DC}. Depending on the polarity of the voltage at any given time, the current will either flow through D_1 and D_4 or D_3 and D_2. If the load is small, the voltage at the output will be a strictly positive version of the input, but if the load is large, the voltage at the output will be a DC voltage.

A diode bridge rectifier can be realised using many different kinds of diodes. Standard silicon diodes have a voltage drop of ≈ 0.7 V [20]. To have a lower voltage drop, one can use schottky diodes instead. The voltage drop of a schottky diode is dependent on the metal used [21], but they generally have a lower voltage drop than silicon diodes, and it can be as low as ≈ 0.2 V. In the configuration of the full wave rectifier bridge, there are always two diodes in series, meaning that the total voltage drop gets doubled. This voltage drop is problematic when the available voltage from the CT is small.

MOSFET rectifier

The voltage available from the CTs can be small for small I_P, meaning the voltage drop over the rectifier should be as small as possible for the system to work with I_P being as low as possible. One method to achieve lower voltage drop than what is possible with diodes, is to use MOSFET transistors.

[10] describe a rectifying circuit using MOSFET transistors. [10] is the basis for the MOSFET rectifier in this thesis. The schematic used in this thesis is shown in Figure 2.4. The rectifier consists of two NMOS transistors and two PMOS transistors (the abbreviations MOSFET, PMOS and NMOS are explained under Abbreviations at the beginning of this thesis). In addition there is a load connected to the rectifier, consisting of a resistor R_L and a capacitor C_L.

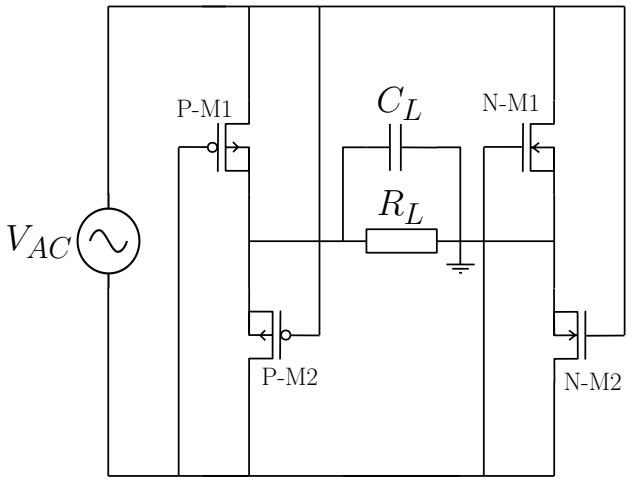


Figure 2.4: Circuit diagram of a rectifier using MOSFET transistors.

The transistors P-M1 and P-M2 are PMOS transistors, and the transistors N-M1 and N-M2 are NMOS transistors.

The transistors are used as switches, and are switching between being in cut-off and in triode. Triode region means $V_{GS} > V_{th}$ and $V_{DS} \leq V_{eff}$. $V_{eff} = V_{GS} - V_{th}$ [21]. V_{GS} is the gate source voltage, V_{DS} is the drain source voltage, and V_{th} is the threshold voltage, meaning the minimum level V_{GS} needs to be for the transistor to turn on.

The rectifier should be able to rectify voltages with as low amplitudes as possible. To achieve this, the transistors in question should have a threshold voltage that is as low as possible, as the switches will not close until the voltage V_{GS} is larger than the threshold voltage. If the threshold voltage is very low ($V_{th} \approx 0$) one can assume that $V_{GS} > V_{th}$ when $V_{GS} > 0$. That also means $V_{eff} \approx V_{GS}$, and $V_{GS} > V_{DS}$.

In the case of using the circuit in Figure 2.4 to rectify an AC signal, small signal analysis is not valid, because the signals are not small. Still, the small signal resistance of the transistors can give an indication of the drain source resistance in question, and the order of magnitude of the in and output resistance of the entire rectifier. The small signal resistance of the NMOS transistors is given in Equation (6) [21]. For the PMOS transistors it is similar, but instead of μ_n it includes μ_p.

$$r_{ds} = \frac{1}{\mu_n C_{ox} \left(\frac{W}{L}\right) V_{eff}} \tag{6}$$

Here, μ_n is the electron mobility, C_{ox} is the oxide layer capacitance and $\frac{W}{L}$ is the ratio between the width and the length of the transistor. r_{ds} is inversely proportional to the voltage V_{eff}. If V_{th} becomes smaller, V_{eff} will get larger for the same V_{GS}. This means that if $V_{th} \approx 0$, r_{ds} must be high.

Figure 2.5 shows the circuit diagram of a MOSFET based rectifier where the transistors are represented by switches. The names of the transistors are kept for continuity. All switches are open if the voltage is 0 V.

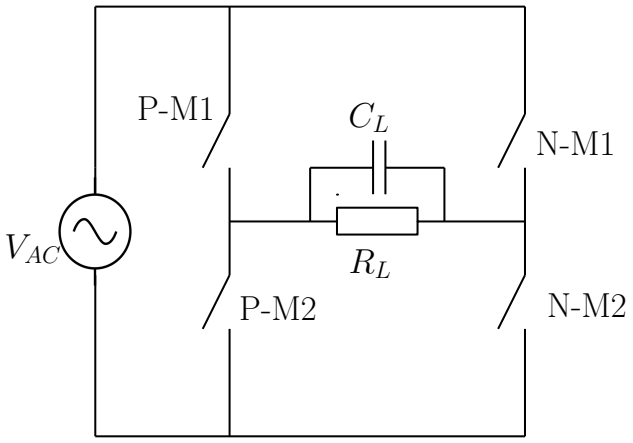
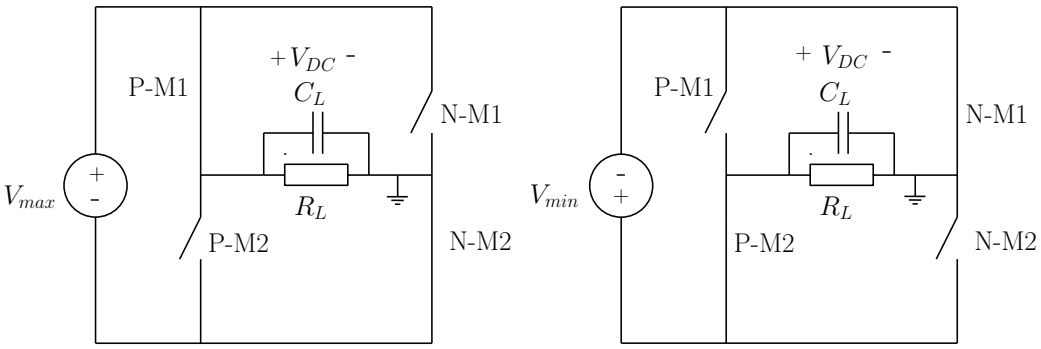


Figure 2.5: Circuit diagram of a MOSFET rectifier where the transistors are represented by switches. If the voltage is 0 V, none of the switches are closed, and no current is flowing.

Figure 2.6 also shows a circuit diagram of a MOSFET based rectifier where the transistors are represented by switches. Figure 2.6a shows the case in the moment when V_{AC} is at its largest. It is illustrated by having the voltage source be a DC source named V_{max}. In this moment the switches P-M1 and N-M2 are closed, allowing current to run. This results in a voltage over the load, V_{DC}. There is a voltage drop over the switches P-M1 and N-M2 in this case, which is dependent on the ON resistance of the transistors. This resistance is not shown in the circuit diagram. As is the case with the diode bridge rectifier, there will be a voltage drop over the rectifier, and it is desired that this voltage drop be as low as possible. Figure 2.6b shows the opposite case of Figure 2.6a. In this case the voltage is on its lowest value, represented by a DC source V_{min}. Now, P-M2 and N-M1 are the ones that are closed, while P-M1 and P-M2 are open. The on resistance is not shown here either. As is evident from the figure, the change in direction of the input current does not cause a change in the polarity of the voltage V_{DC}.



(a) When the voltage in is sufficiently positive, the switches P-M1 and N-M2 are closed, allowing current to run.

(b) When the voltage in is sufficiently negative, the switches P-M2 and N-M1 are closed, allowing current to run.

Figure 2.6: Circuit diagrams of a MOSFET rectifier where the transistors are represented by switches for different voltages.

Even though these figures show the cases of V_{max} and V_{min}, the situation will be the same for all voltages larger than the threshold voltage of the transistors V_{th}. When the load capacitor C_L is large, the period when the voltage below the threshold will not cause the voltage V_{DC} to drop to zero, but rather it will slowly decline. When the load is large enough, V_{DC} will be a DC voltage.

Transistors for use in a rectifier like this one should have a low threshold voltage and a low ON resistance. The switching speed is not very important, as the commercial switching frequency of AC current is 50 Hz as previously stated.

2.2.4 Energy Harvesting System

The entire EH system consists of the previously discussed sub-systems. A block diagram of the EH system is shown in Figure 2.7. In this figure, I_P is the primary current going to the CT, which is the current in the cable that the CT is connected to. V_{AC} is the voltage that results from I_S being connected to a load. V_{DC} is the rectified voltage coming from the rectifier. The DC/DC converter then converts this voltage up to the required voltage V_{Bat} that can charge a battery. The focus in this thesis is to achieve $V_{Bat} = 3.3$ V with $I_P < 1$ A.

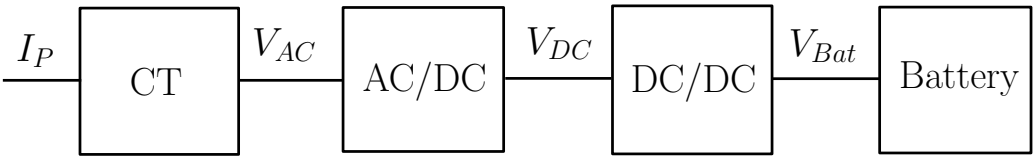


Figure 2.7: A block diagram showing the sub-systems of the energy harvesting system together with a battery and the signals that connect them.

Normally, wireless sensor nodes are powered by batteries. An ideal EH system would be able to replace the need of having a battery. However, the energy coming from a magnetic field surrounding a cable can be very unstable, and varying in magnitude. It is dependent on the current in the cable, which varies by how much power is used at any given moment. Therefore, it is beneficial to keep a battery in the system, but to use the energy from the magnetic fields to recharge the battery, so that the battery would not need to be changed as often.

A relevant metric for any EH system is efficiency. It states how much of the available energy is exploited and converted to usable energy.

Efficiency, η is defined as the relation between the power out P_{out} over the power in P_{in} as is shown in Equation (7) [19].

$$\eta = \frac{P_{out}}{P_{in}} \tag{7}$$

Here, the power P is defined by the voltage V, current I and/or resistance R as shown in Equation (8) [14].

$$P = IV = \frac{V^2}{R} = I^2 R \tag{8}$$

If the voltage in question is an AC voltage, the voltage in the power equation is the Root Mean Square (RMS) voltage that is included in the equation.

The RMS voltage V_{RMS} for a periodic signal V is given in Equation (9) [14]. Here T is the period of the signal, and t_1 is the moment in time when one starts to look at the signal.

$$V_{RMS} = \sqrt{\frac{1}{T}\int_{t_1}^{t_1+T} V^2(t)dt} \tag{9}$$

AC current, or voltage, is ideally sinusoidally shaped. When it is perfectly sinusoidally shaped, Equation (9) can be used to calculate V_{RMS}. For a sinusoidal signal $V = Asin(\omega t + \phi)$, V_{RMS} can be found by dividing the amplitude by $\sqrt{2}$ [14]. This means that the efficiency of a rectifier, where the input voltage is AC and the output voltage is DC, can be given as in Equation (10).

$$\eta = \frac{\sqrt{2}V_{DC}^2 R_{in}}{V_{AC,amplitude}^2 R_{out}} \tag{10}$$

The input resistance R_{in} and output resistance R_{out} of the rectifier is a part of this equation. For the rectifiers discussed here, this is dependent on the resistance of the diodes used or the drain source resistance r_{ds} of the MOSFETs. Both of these are metrics that are dependent on the voltage over and current through them at any given time. A datasheet of the components used can be used to determine these resistances at different currents and voltages. For the DC/DC converter the datasheet does not necessarily state what the input resistance is, but the equivalent input resistance under specific preconditions can be found experimentally. The equivalent input resistance when the system is off, $R_{in,off}$, can be found by measuring with a multimeter between the input pin and the ground pin of the DC/DC. The equivalent input resistance while on $R_{in,on}$ can be found by connecting the input in series to a known resistance R_{known} and a known voltage V_{known}, and measuring the voltage $V_{measured}$ between the two. Then a simple voltage dividing between R_{known} and the DC/DC is used to determine the equivalent input resistance under these prerequisites. Equation (11) shows this.

$$R_{in,on} = R_{known}\frac{V_{measured}}{V_{known} - V_{measured}} \tag{11}$$

It can be a problem that the DC/DC converter has a very low input impedance, while the output impedance of the rectifier is much higher. That would mean that only a small amount of the voltage would be transferred from the rectifier to the DC/DC. This would lead to the system having a very low efficiency. In order to avoid the problem of impedance matching of the input of the DC/DC and the output of the rectifier, a switch, SW and a large capacitor C_1 can be added to the system. This is shown in Figure 2.8. When the switch is open the voltage V_{DC1} charges the capacitor C_1, while the voltage V_{DC2} is zero. When C_1 is fully charged, the switch closes and the charge that is stored in C_1 will discharge to the DC/DC converter, giving it a little time to turn on. Then it can open and closed repeatedly to turn the DC/DC converter on for short amounts of time.

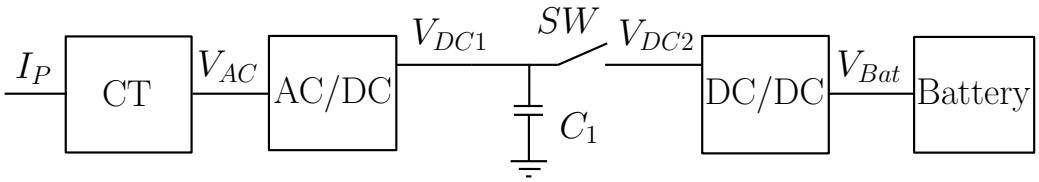


Figure 2.8: A block diagram showing the sub-systems of the energy harvesting system together with a battery and the signals that connect them. Switch and capacitor added to the block diagram.

The formula showing the voltage of the capacitor C_1 is given in Equation (12) [14].

$$V_c(t) = V_F + (V_I - V_F)e^{\frac{-t}{\tau}} \tag{12}$$

Here, $V_c(t)$ is the capacitor voltage, V_F is the final voltage over the capacitor, V_I is the initial voltage and the time constant τ is given in Equation (13).

$$\tau = RC \tag{13}$$

R in this equation is the resistance [Ω] and C is the capacitance [F]. The capacitor is charged 63% after the time τ has passed, and is considered fully charged after 5τ.

Figure 2.9 shows the full circuit with a diode bridge and a CT model. The circuit is split in two to be easier to read. V_{DC1} in the upper half is connected to V_{DC1} in the lower half.

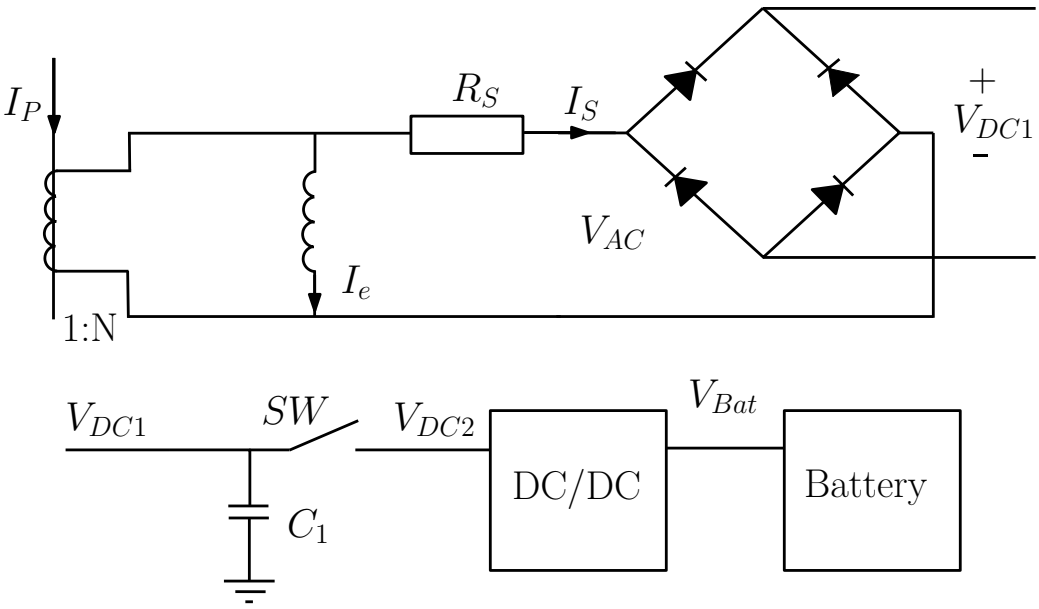


Figure 2.9: The full circuit diagram of the EH system. Here shown with a diode bridge rectifier.

3 Methodology

The chosen method to design, optimise and test the energy harvesting system is a combination of simulations in the program LTspice[1] [22], and physical implementation and testing with a selection of physical components.

3.1 Simulations

The design method of the EH system is mainly simulation in a SPICE software called LTspice. There are multiple advantages to design circuits using simulations, versus using physical components to test different solutions immediately. It is faster, easier, and cheaper than physical implementation. Simulating allows for faster iterations. A simulation takes much shorter time than actually connecting many physical components together. When something needs to change, a simple parameter can be changed with a lot less effort than for instance having to buy a new component. This makes it a cheaper method, as well as allowing for fast testing of the impact different parameters have on the system as a whole. In addition, it allows for assuming some parts of the system as ideal, and look at other parts of the system isolated. However, all kinds of simulations include some assumptions and simplifications that make them imperfect. Special care has to be taken to make sure the simulations are accurate enough to be useful.

The program LTspice is chosen as a simulation program for multiple reasons. First, it is a SPICE based program that is good for simulating analogue circuitry. It has a Graphical User Interface (GUI) that makes it simple to use. It is also a free software that is widely used for this purpose.

The different parts of the EH system are simulated individually before they are put together as a full system.

3.1.1 Current Transformers

An equivalent circuit model of a CT is modeled in LTspice. The model is based on the circuit in Figure 2.2. The model used in this thesis use a constant inductance for Z_e, in stead of a varying impedance, for simplicity. Therefore the model contains no information about nonlinearities like the saturation of the core of the CT, and is thus very inaccurate. Still, it is simulated to give an indication on what behaviour to expect of a CT. Figure 3.1 shows the circuit modeled in LTspice. The relationship between L1 and L2 is found using Equation (5). The K statement is a coupling factor that is set to 1 to signify ideal transfer from L1 to L2. K = 0 means no current gets transferred. The resulting netlist can be found under Listing 1 in Appendix A. Another CT with a different TR is shown in Figure 3.2. This is the model used in the simulation of the full system that will be shown later.

[1] Version: LTspice XVII for OS X

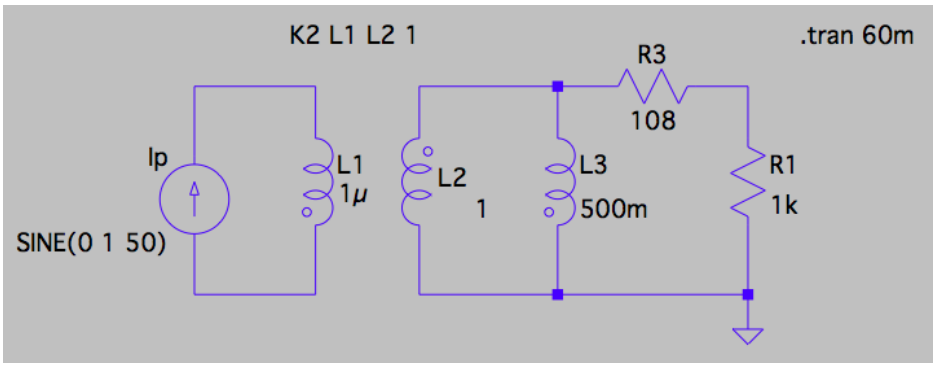


Figure 3.1: An equivalent circuit model of a different CT simulated in LTspice.

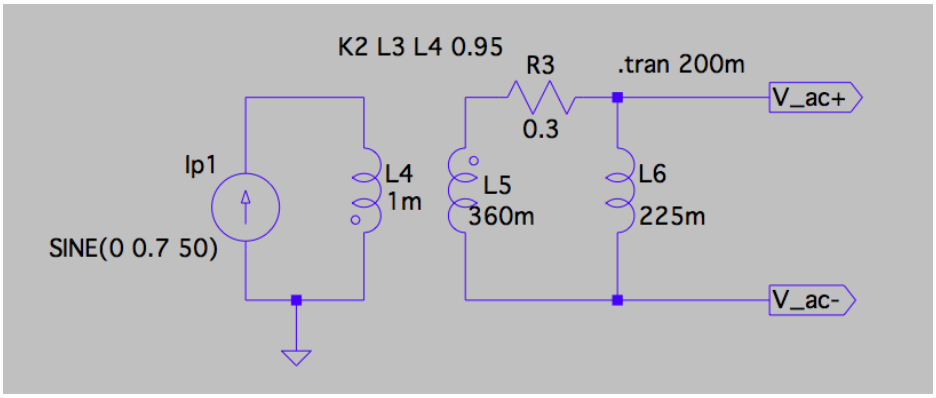


Figure 3.2: An equivalent circuit model of a CT simulated in LTspice.

3.1.2 DC/DC converters

According to the hypothesis put forward in Section 2.2.2, the most important characteristic of the DC/DC converter is that it should be able to deliver $V_{Bat} = 3.3$ V with an input voltage that is as low as possible, seeing as the goal is for the system to work with an I_P that is as low as possible. LTC3108 [23] from Linear Technologies promises to be able to deliver 3.3 V on its output with the input voltage being as low as 20 mV. Therefore this circuit is investigated as a possible DC/DC converter in the EH system. Since Linear Technologies is the same company that makes LTspice, the LTC3108 is a component in the standard LTspice library and can be used for simulations. It is connected to a test circuitry as shown in Figure 3.3. This circuit is based on the evaluation board schematic for DC1582B [24], and the jump wires are connected to produce a 3.3 V output voltage. The SPICE netlist for this circuit is listed in Listing 5 in Appendix A. This circuit is from now on called DC/DC1.

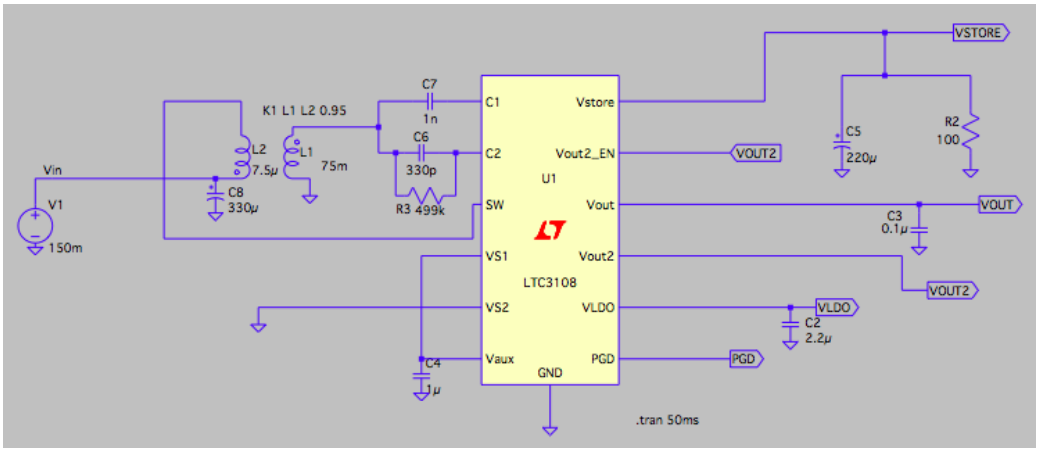


Figure 3.3: The simulated circuit of DC/DC1 with connections as specified in the data sheet for the evaluation board DC1582B.

LTC3331 [25] is another DC/DC converter. It is hereby named DC/DC2. This DC/DC converter is very different from DC/DC1, since it has a much higher voltage threshold on the input, with 3 V instead of 20 mV. It also has a much higher equivalent input on resistance. It is included to see what effect this change has on the system as a whole. It is simulated with connections as specified in the datasheet of the evaluation board DC2151A [26]. The spice netlist for this simulation is shown in Appendix A, Listing 6.

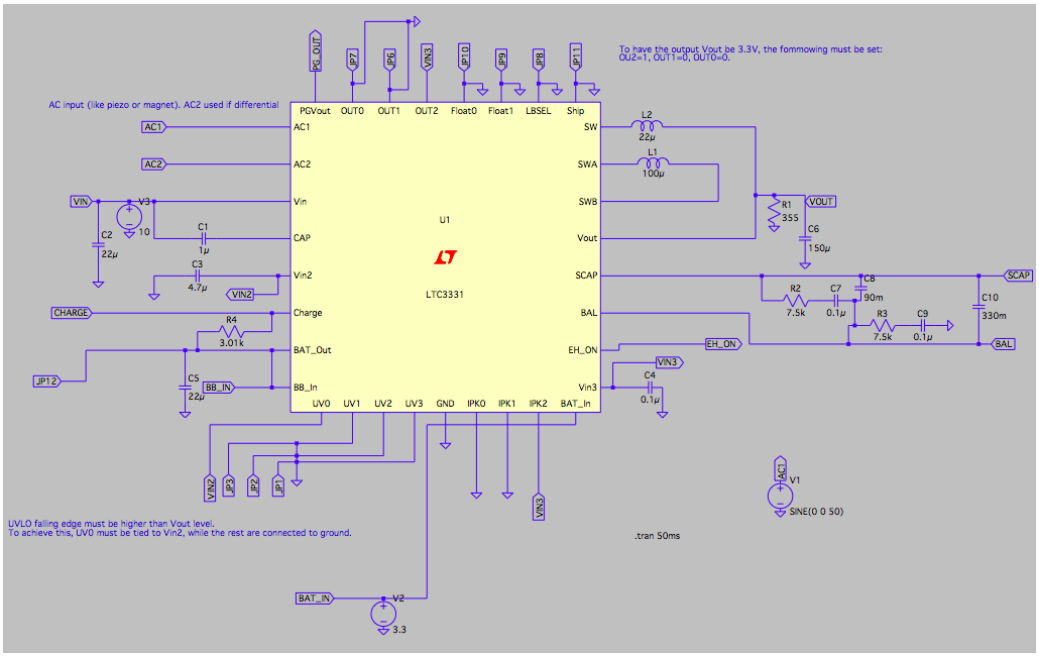


Figure 3.4: LTspice model of DC/DC2 with connection as specified in the datasheet of the evaluation board DC2151A.

Table 2 shows an overview of the two DC/DCs that are used in this thesis, their given name and some important input characteristics. Both are capable of delivering 3.3 V on their output. The input voltage range is stated in the datasheets, and the equivalent input resistance Rin, on are found using Equation (11).

Table 2: Overview of DC/DCs

Name	Chip	Evaluation board	Input voltage range	$R_{in,on}$
DC/DC1	LTC3108	DC1582B	20 mV-400 mV	3 Ω
DC/DC2	LTC3331	DC2151A	3 V-19 V	36 kΩ

3.1.3 Rectifiers

The rectifier is the part of the system that needs to connect the CT and the DC/DC converter. When designing the rectifier for the EH system, characteristics of both the CT and the DC/DC needs to be taken into account. In previous papers on this topic, different rectifiers have been used for this purpose. In order to evaluate which is the best rectification method, three different rectifiers are simulated. The three rectifiers are:

- Rect1: Diode based full wave rectifier using silicon diodes.
- Rect2: Diode based full wave rectifier using schottky diodes.
- Rect3: MOSFET transistor based rectifier.

For a more detailed description of the different rectifiers that are simulated, see Table 3. The name is the given name in this thesis, the type is the type of rectifier as described in Section 2.2. The component type is the type of component that the rectifier is implemented or simulated with, and the main components column state the company given name of the exact component used in the implementation. The V_{th} is the threshold voltage of the transistors or the forward voltage drop of the diodes, according to the respective datasheets. The actual voltage drop might differ from these values. All rectifiers are simulated with an ideal voltage source. The signal in is a sinusoidal signal of 50 Hz. They are also simulated with a load that is representing the DC/DC converters.

Table 3: Overview of rectifiers in this thesis

Name	Type	Component type	Main components	V_{th}
Rect1	Full wave rectifier	Silicon diodes	1N4007	1.1 V
Rect2	Full wave rectifier	Schottky diodes	1N5819	0.6 V
Rect3	MOSFET rectifier	PMOS/NMOS	ALD310700/ALD110800	0.02 V

Rect1: Silicon diode based rectifier

Rect1 is a full wave rectifier based on a diode bridge architecture like described in Section 2.2.3. The model is simulated using diodes of the type 1N4007 [27]. The SPICE model of this component is from [28]. The circuit that is simulated in LTspice is shown in Figure 3.5. The resulting netlist can be found under Listing 2 in Appindix A. The simulation includes an ideal AC voltage source in place of the CT, and a load of 12 Ω and 300 μF. This load is chosen because it is the same as the input impedance of the DC/DC converter DC/DC1 while off.

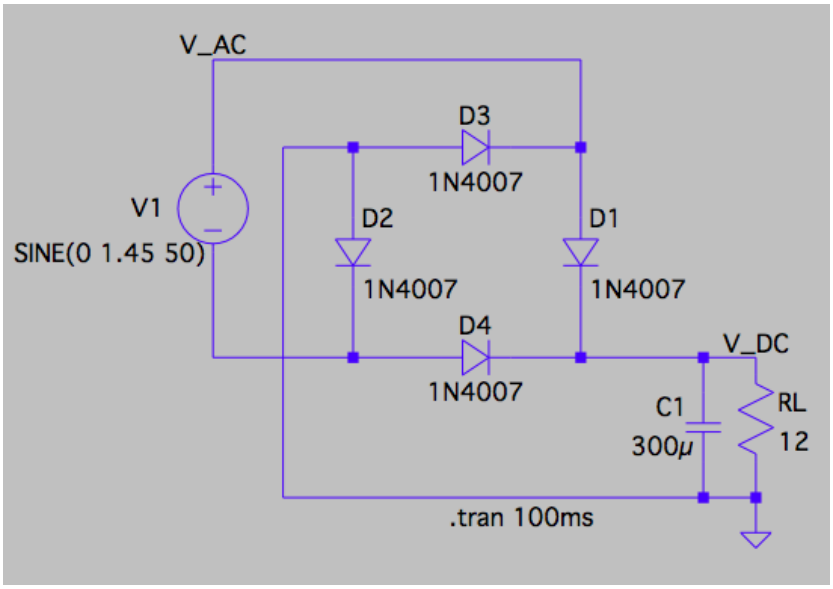


Figure 3.5: The simulated circuit of the Rect1 simulated in LTspice. The simulation includes an AC voltage source in place of a CT and a load in place of a DC/DC converter.

Rect2: Schottky diode based rectifier

Rect2 is simulated in a similar way to Rect1. The source and load are similar. Schottky diodes of the type 1N5819 [29] are in the original library of LTspice and are used to simulate Rect2. The simulated circuit is shown in Figure 3.6. The resulting netlist can be found under Listing 3 in Appindix A.

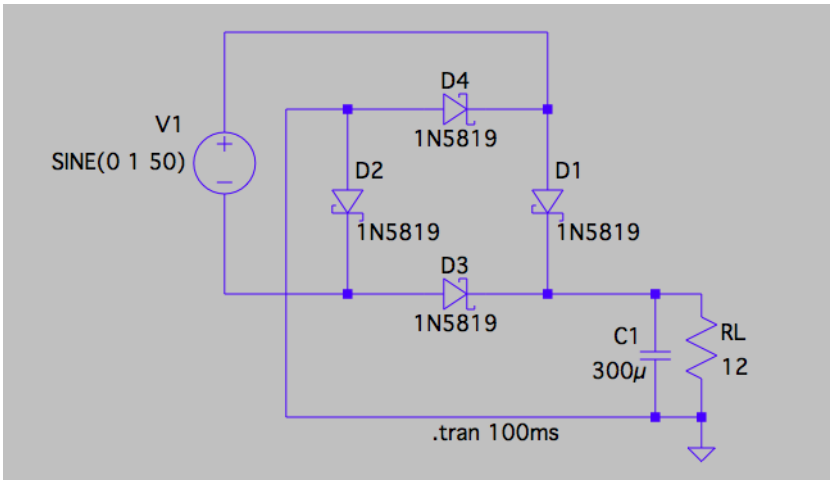


Figure 3.6: The simulated circuit of the Rect2 simulated in LTspice. The simulation includes an AC voltage source in place of a CT and a load in place of a DC/DC converter.

Rect3: MOSFET based rectifier

Rect3 is simulated like the circuit diagram in Figure 2.4. In order for this rectifier to work on as low input voltages as possible, the threshold voltages of the transistors needs to be as low as possible. Therefore the transistors ALD310700 [30] (PMOS) and ALD110800 [31] (NMOS) have been chosen to implement this rectifier, as they are advertised as "zero-threshold transistors". These transistors do not have a LTspice model, and therefore the simulations of Rect3 are done using transistor models that have been fetched from [32] that are augmented to better fit the specifications of the datasheets of ALD310700 and ALD110800. For PMOS the 2SJ49C transistor model is chosen, and the transistor model 2SK134 is chosen for NMOS. These are chosen because they offer the lowest threshold voltage of the transistors available in the library. The simulated circuit is shown in Figure 3.7. The SPICE netlist is listed in Listing 4 in Appendix A. The circuit is simulated with an ideal AC voltage source in place of a CT as a source, and a load that consists of a resistor and a capacitor to represent DC/DC1 while on.

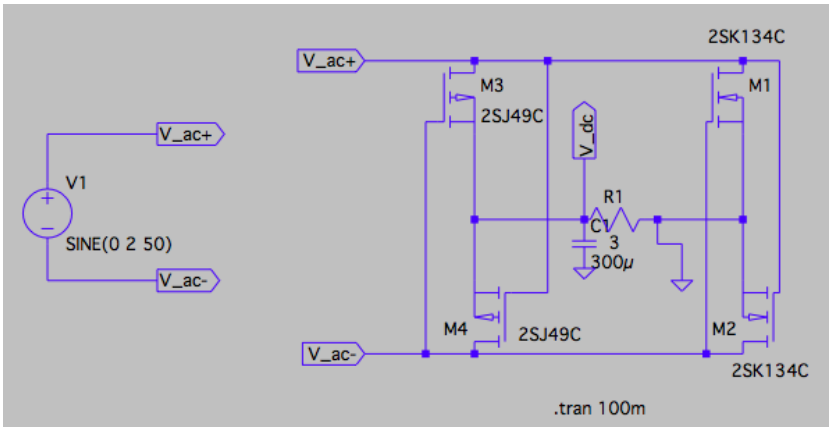


Figure 3.7: The MOSFET based rectifier circuit Rect3 simulated in LTspice. An AC voltage source is the source of the circuit, and a resistor and capacitor are the load.

3.1.4 Full system

The aforementioned sub-systems have been put together and simulated as one system. The final simulated circuit is shown in Figure 3.8. In this figure Rect2 is the rectifier used, and DC/DC1 is the DC/DC converter used. The CT model is the model from Figure 3.2. This simulation can show how the different sub-systems behave together, when the sources and loads are no longer ideal. It allows for optimisations of the full system based on how the different sub-systems behave together.

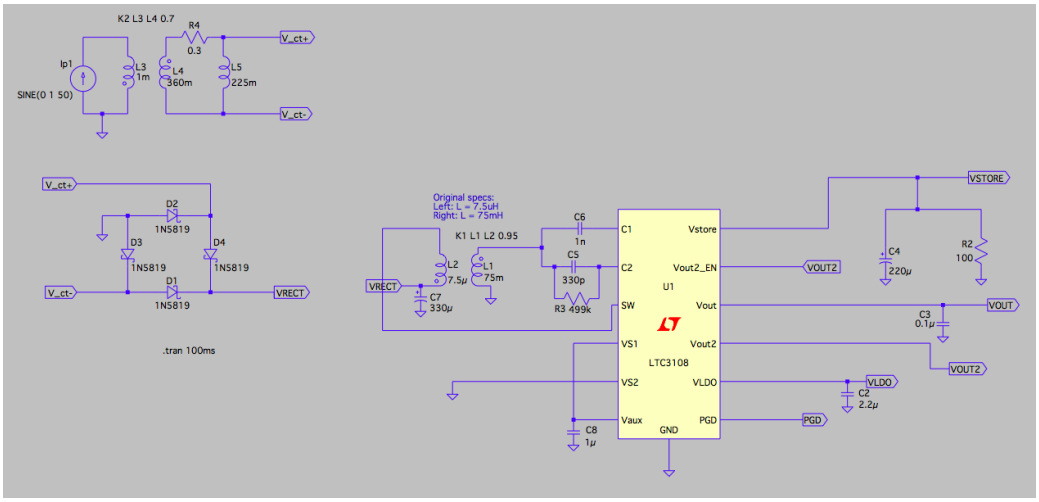


Figure 3.8: Full simulated system with a CT model, Rect2 and DC/DC1.

As a comparison, a commercial energy harvesting system is simulated. LTC3331 is simulated as DC/DC2 in Section 3.1.2, but is actually an EH system with an integrated rectifier. It has the possibility to charge a connected battery with either a DC voltage, AC voltage, or a combination, as an input signal. Using the system as a DC/DC converter involves adding a DC voltage to the input Vin. Using it as a combined system involves adding an AC voltage at AC1 or AC2. The AC1 and AC2 inputs can be used in combination with the DC input Vin. The circuit simulated in LTspice is the same as when it is used as a DC/DC converter, shown in Figure 3.4. The only difference is what input is used.

3.2 Implementation

Simulating circuits can be useful while designing, but ultimately a simulation can never be 100% accurate with all the imperfections present in the real world. Therefore the system is implemented using physical components to be tested in a real world setting. This can help validate the results from the simulations, and can help uncover weaknesses in the system that the simulations are unable to uncover.

In this thesis the different components are connected together using wires and a breadboard, and tested using oscilloscopes and multimeters.

3.2.1 Current Transformers

A choice is made to use commercial CTs as the first step of the magnetic energy harvesting system. The reason for this is that it is cheaper and easier than to make a custom CT. To find out what CTs would be ideal for this particular system, five different CTs are chosen. The different CTs are chosen because they have different properties that it can be interesting to look into the effect of. All of them have a different maximum current ratings, and two and two have the same TR, but it is combined with different current ratings, and different secondary winding resistance, making the five of them span a wide range of possibilities. This way it is possible to look at the impact of different parameters on the system as a whole.

The different CTs are tested to map their properties. The primary side is connected to a wire that had a steady, controllable current flowing through it. The secondary side is connected to a known resistance and an oscilloscope to look at the change in output voltage with changing primary current or changing load resistance.

The five different CTs tested are named from CT0 to CT4. Their properties are listed in Table 4. The CT name is the name of the CTs given from the manufacturer, TR is the Turn Ratio, Current rating is the rating given by the manufacturer, and Resistance is the secondary winding resistance, which has been measured on the individual CTs. The physical CTs are depicted in Figure 3.9.

Table 4: Overview of the CTs that are tested.

CT	CT name	TR	Current rating	Resistance [Ω]
CT0	TCC176	1:60	60 A : 1 A	0.3
CT1	SCT006	1:2000	10 A : 5 mA	485
CT2	SCT006	1:1000	20 A : 20 mA	108
CT3	XHSCT-T-10	1:1000	16 A : 16 mA	41
CT4	AKH_0.66 K-Ø10	1:2000	40 A : 20 mA	164

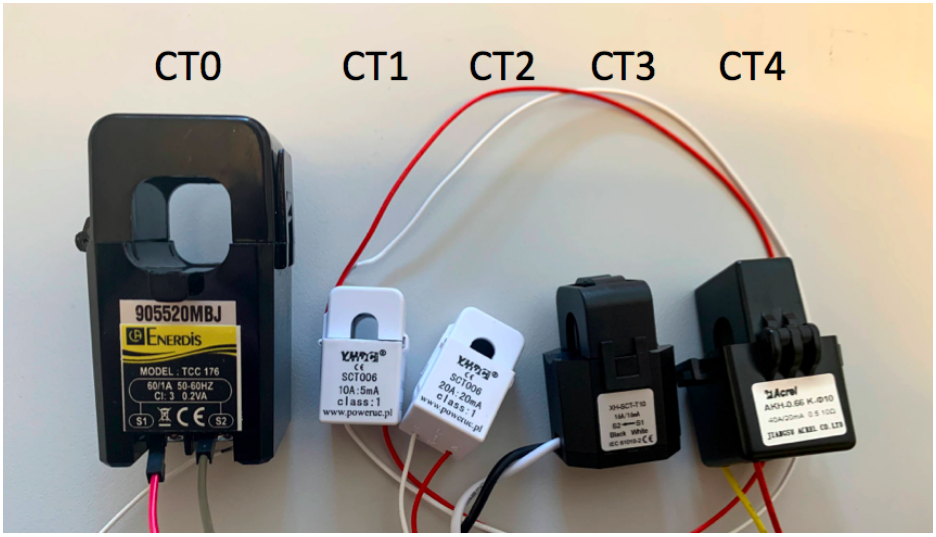


Figure 3.9: Pictures of the different CTs used in this thesis.

The setup of the testing of the CTs is shown in Figure 3.10. Here a CT is connected to a wire carrying I_P on the primary end, and a load resistance on the secondary end. A clamp ampere meter is used to measure I_P, and an oscilloscope is used to measure the resulting voltage V_{AC}. The load resistance is varied for the same I_P to look at the effect different load resistances has, and I_P is varied for the same load resistance to look at the effect different I_Ps have on the voltage V_{AC}.

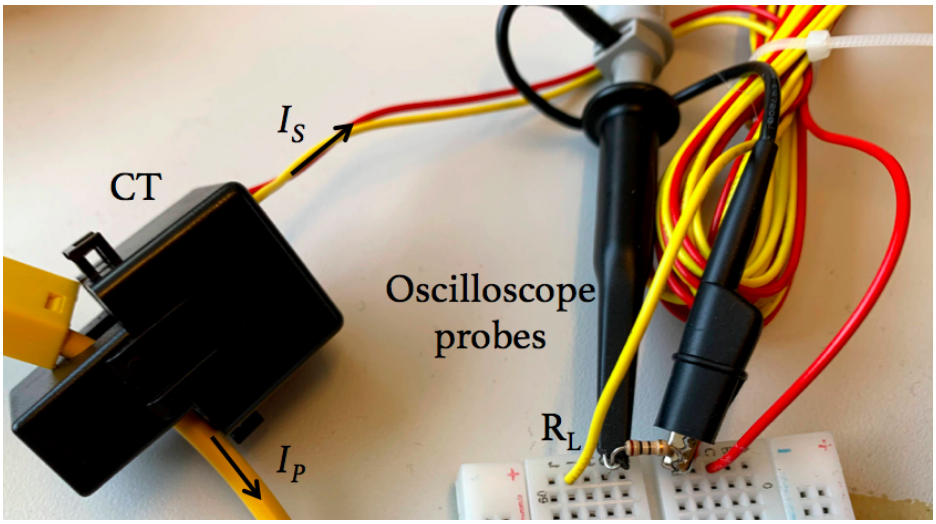


Figure 3.10: The test setup for testing a CT with a load.

3.2.2 DC/DC converters

DC/DC1 is tested while on the evaluation board DC1582B. The evaluation board is tested to look at the input resistance and to see if the threshold voltage for the circuit to deliver 3.3 V out is the same as is promised in the datasheet. This is also done on DC/DC2.

3.2.3 Rectifiers

The three rectifiers Rect1, Rect2 and Rect3 are implemented and tested. They are implemented with the components listed in Table 3. The components are mounted on a breadboard and tested using a wave generator and oscilloscope called DIGILENT Analog Discovery 2 [33] from Analog Devices. It was connected to a laptop running the WaveForms 2015 software[2] [34]. They are connected to loads that are similar to the simulated loads mentioned in Section 3.1.3. Figure 3.11 shows how the three rectifiers are implemented. (a) shows Rect1, (b) shows Rect2 and (c) shows Rect3.

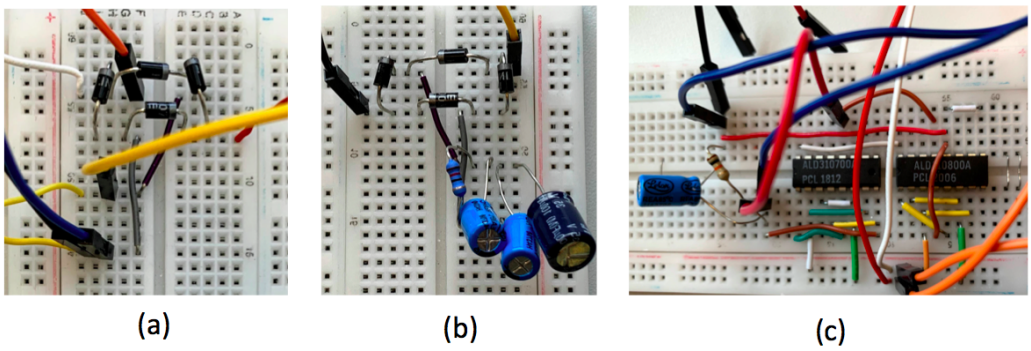


Figure 3.11: Pictures of the implemented rectifiers with loads. (a) shows Rect1 with yellow wires going to the left to a DC/DC converter, (b) shows Rect2 with 12 Ω and 300 μF and (c) shows Rect3 with 10 kΩ and 100 μF.

3.2.4 Full system

The different sub-system are connected together and tested. Figure 3.12 shows the full system connected together. The signal/power flow in the system generally goes from right to left. The different parts of the the test setup and the sub-systems present are marked on the picture. The test setup includes an oscilloscope, a clamp meter and a setup to get a variable primary current in the range of 0-16 A. The current source setup consists of a variac, or auto transformer [35], a large current transformer and some wires. The variac is connected to the power grid that has has a voltage of 230 V. The variac has a wheel to enable smooth transforming of voltage. This transfers the voltage down. The two outputs of the variac are connected to the primary side of a large current transformer to transform the voltage further down, but the current up. The two wires on the secondary side of the current transformer are connected together with a wire with a measured resistance of about 0.6 Ω. This is the wire carrying I_P that CT0-CT4 are connected to. The current flowing through that wire is continuously monitored using a clamp meter.

[2]Version: 3.4.7

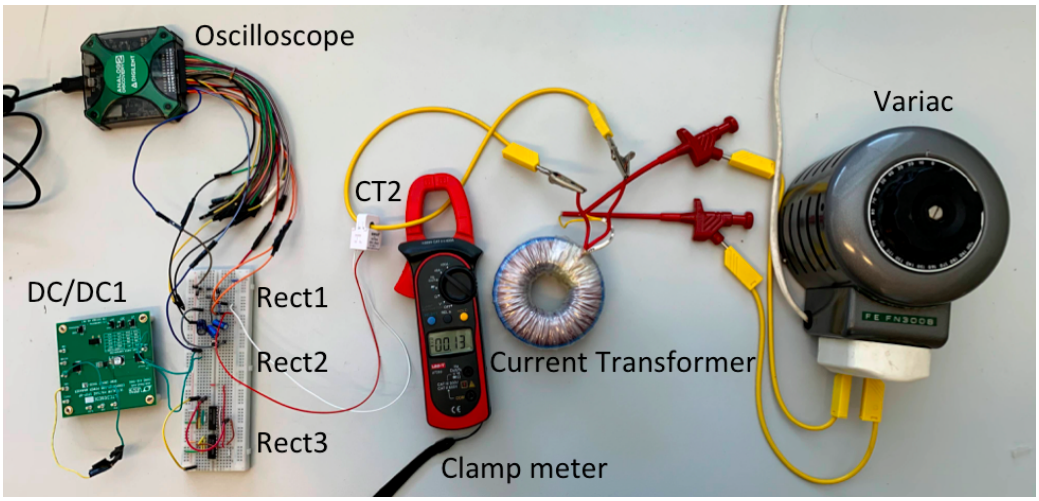


Figure 3.12: The different parts of the energy harvesting system connected together with oscilloscope and source.

The full system is tested with the two DC/DCs, three different rectifiers and the five different CTs. I_P is varied in all cases to see how low it can be before the system stops working. All measurements are done more than once, at different dates, to try to minimise the possibility of wrong test setup or other factors leading to wrong measurements. The waveforms are produced by exporting oscilloscope datapoints and plotting them in Matlab[3] [36].

The capacitor and switch mentioned in section 2.2.4 are implemented in between the rectifier and the DC/DC converter. The system is tested with and without these two components to see if it can improve the overall performance.

The combined commercial EH system LTC3331 is tested together with all the different CTs at the input AC1 to see if the combined rectifier and DC/DC system is better or worse than the rectifiers designed in this thesis with a separate DC/DC converter.

For a full overview of all the equipment, components and software used in this thesis, see Appendix B.

[3]Version: R2016a (9.0.0.341360), maci64

4 Results

Selected waveforms from the simulations and measurements from the implemented system are described in this section. The results are also presented as graphs and tables showing important aspects of the performance of the system.

4.1 Simulations

The results from the simulations are described in this section.

4.1.1 Current Transformers

When the CT equivalent circuit from Figure 3.1 is simplified to have a coupling factor of 1, no secondary winding resistance, no I_e and 1 Ω RL, $I_P = 1$ A does result in $I_S = 1$ mA as is predicted by Equation (4). When all of the above is added, an $I_P = 1$ A results in an I_S of 1 mA for 10 Ω. The voltage over the load is 120mV. Increasing R_L to 1 kΩ increases the output voltage to 300 mV, and decreases I_S to 280 μA. This is shown in Figure 4.1. It shows waveforms of I_{ps} (light blue), I_S (pink) and the output voltage (blue). I_P is set to 1 A.

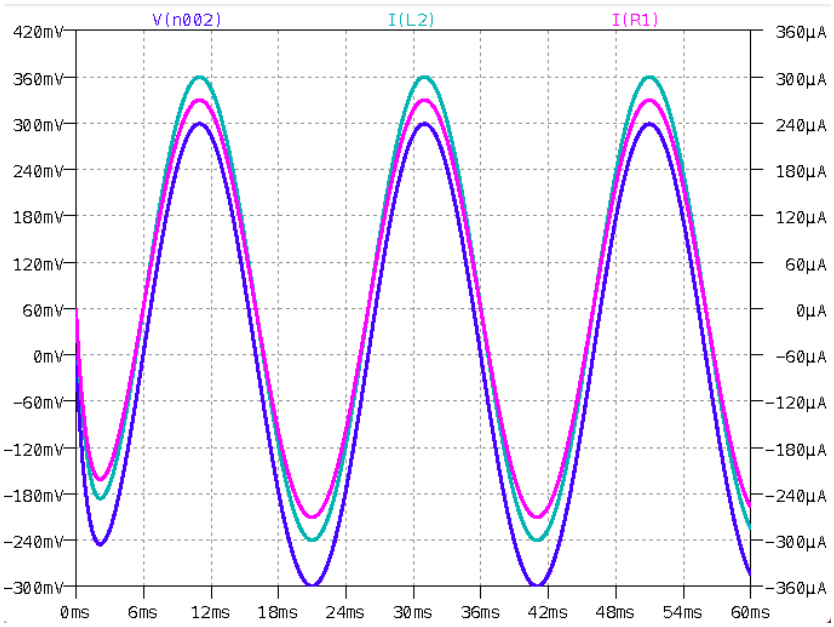


Figure 4.1: Waveforms of I_{ps} (light blue), I_S (pink) and output voltage (blue).

4.1.2 DC/DC converters

The DC/DC converter DC/DC1 is simulated with the connections specified in Section 3.1.2. The resulting transient is shown in Figure 4.2. The green signal is V_{DC} and the blue signal is V_{Bat}. V_{DC} is 150 mV, and is set to this as t = 0 ms. V_{Bat} is zero until 30 ms, where it starts rising. After a few ms it reaches 3.3 V. The time delay is due to the large capacitor at the input of the DC1582B. The lower the input voltage on the input, the longer time it takes for DC/DC1 to turn on.

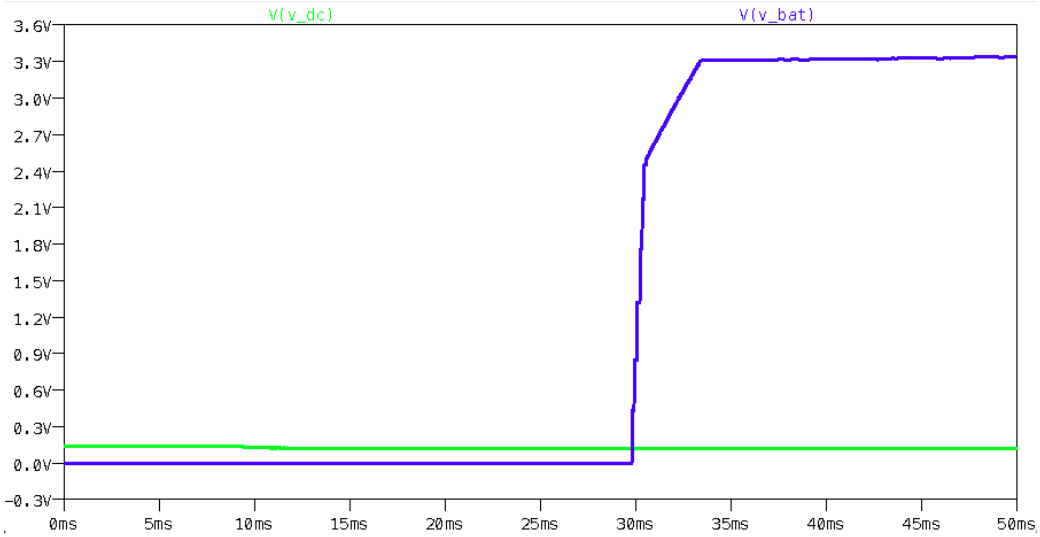


Figure 4.2: The simulated transient plot of V_{DC} (green) on the input of DC/DC1 and V_{Bat} (blue) on the output of DC/DC1.

If one looks closely on V_{DC} in Figure 4.2 at around 10 ms one can see that there is something that happens there, but it is not possible to see on this scale. Figure 4.3 shows a magnified version of Figure 4.2 around this area. Here, it is evident that V_{DC} drops from 140 mV to $\approx$ 117 mV at 10 ms. This behaviour is the result of the input resistance of DC/DC1 changing from 12 Ω when it is off, to 3 Ω when it is on.

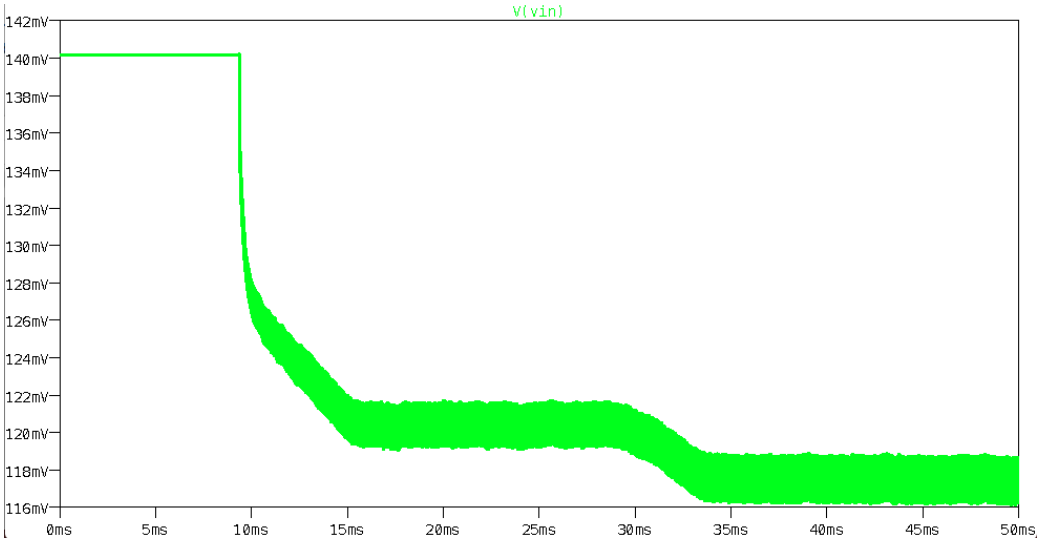


Figure 4.3: The transient plot of V_{DC} on the input of DC/DC1 in the moment when DC/DC1 turns on.

DC/DC2 is also simulated. The resulting simulated transient is shown in Figure 4.4. The DC input of LTC3331 "vin" (green) corresponds to V_{DC} and is set to 7.5 V. The AC

input option AC1 (blue) is set to float, and default to half of Vin. This input option can be used to use LTC3331 as a EH system with integrated rectifier. Vout (red) corresponds to V_{Bat} and goes high after 4 ms. These are much higher voltages than DC/DC1 needs to turn on. The system did not give vout = 3.3 V for lower voltages than this in these simulations. The time delay is lower for DC/DC2 than for DC/DC1 because it has a 22 μF capacitor on the input in stead of a 330 μF capacitor which the DC/DC1 has.

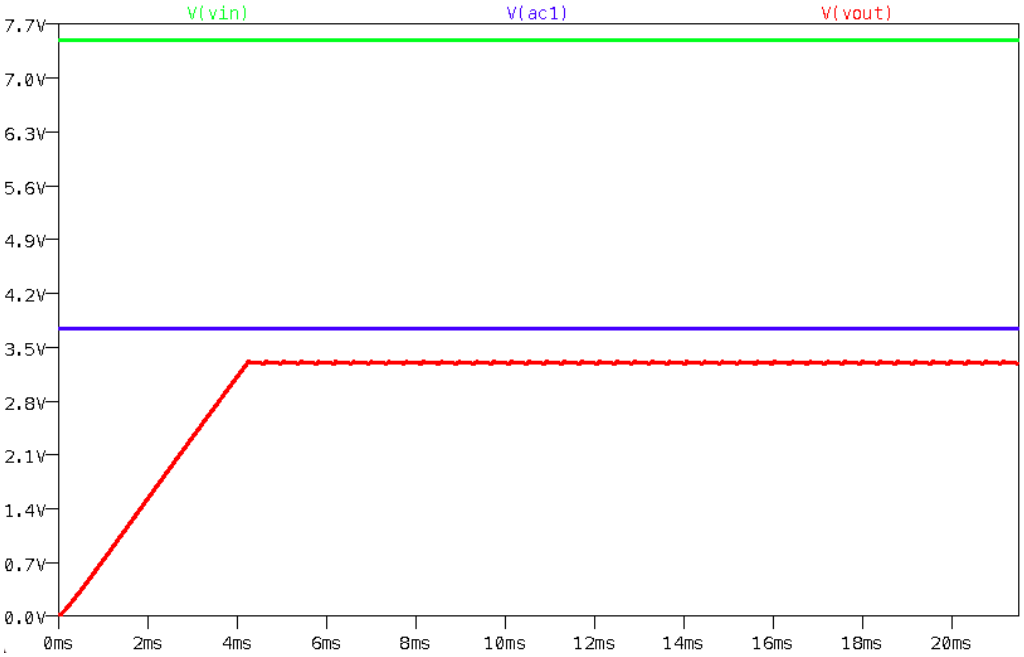


Figure 4.4: V_{DC} (Vin), Vac1 (blue) and V_{Bat} (vout) on DC/DC2. The input in on AC1 (blue) was set to be floating and V_{DC} (green) was set to 7.5V. V_{Bat} goes high at about 4 ms.

4.1.3 Rectifiers

The three aforementioned rectifiers are simulated. The resulting simulated waveform for Rect1 is shown in Figure 4.5. In this simulation, the load of the circuit is set to be 12 Ω and 300 μF. The signal in on Rect1 is the V_{AC} signal (green), which here is set to be 50 Hz and have a 2 V amplitude. The signal out of Rect1 is V_{DC} (blue). The shape of this signal is not a DC signal, but rather a rectified version of the AC signal that is strictly positive. It also has a lower amplitude, and the shape is clearly influences by the exponential charge and discharge of the capacitive part of the load. This is due to the low load resistance, which makes the time constant of the load lower than the period of the signal it self. The signal V_{DC} has an average value of about 275 mV.

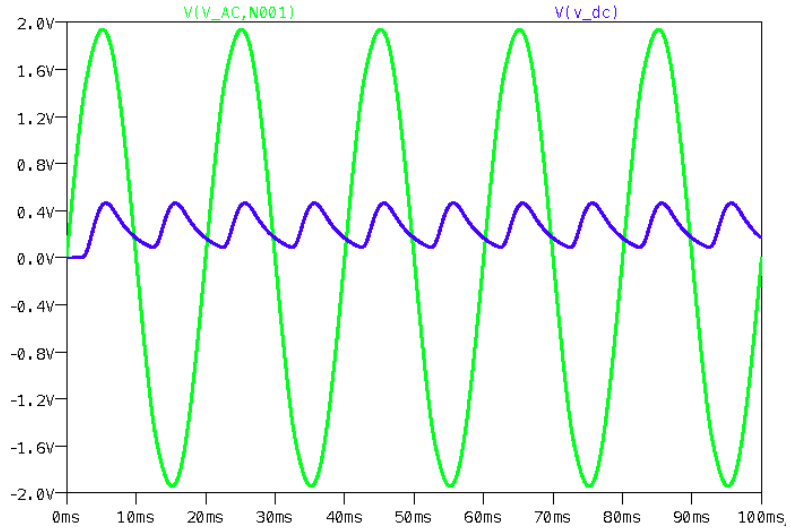


Figure 4.5: The signals V_{AC} (green) and V_{DC} (blue) from the simulation of Rect1 with a load of 12 Ω and 300 μF.

Appendix C shows similar plots for Rect2 and Rect3 in Figure C.1 and Figure C.2 respectively.

Simulated waveform of V_{AC} (green) and V_{DC} (blue) for Rect2 with 2 V sinusoidal signal in and 36 kΩ and 22 μF load can be seen in Figure 4.6. This load corresponds to the input impedance of DC/DC2, while on. This higher load resistance results in a more DC shaped signal even though the load capacitance is smaller. Similar plots for Rect1 and Rect3 can be found in Figure C.3 and Figure C.4 in Appendix C.

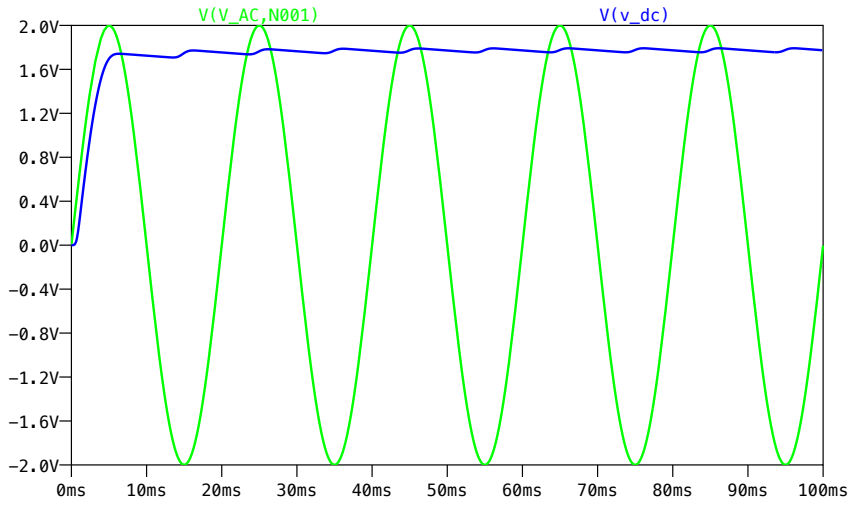


Figure 4.6: Waveform of V_{AC} (green) and V_{DC} (blue) for Rect2. V_{AC} has a 2 V amplitude, and a frequency of 50 Hz. The load is 36 kΩ and 22 μF.

The input resistance of DC/DC1 is 3 Ω. Therefore the rectifiers have been simulated with 3 Ω as a load together with the 300 μF capacitor. The resulting V_{DC} versus V_{AC} for the different rectifiers is shown in Figure 4.7. In this figure it is Rect2 that shows the best performance. It makes DC/DC1 turn on at the lowest V_{AC}, and consistently has a higher V_{DC} for the same V_{AC}. Figure C.5 in Appendix C shows the same plot as Figure 4.7, but with 12 Ω instead of 3 Ω, as this is the resistance of DC/DC1 while off.

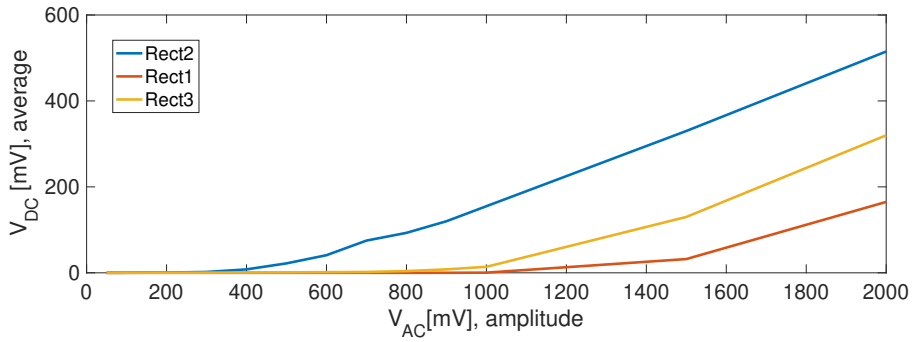


Figure 4.7: V_{DC} versus V_{AC} for the rectifiers Rect1, Rect2 and Rect3 simulated with 3 Ω and 300 μF as a load.

4.1.4 Full system

The complete energy harvesting system is simulated with Rect2 and DC/DC1, as these have shown to be the most promising. The transient of this simulation is shown in Figure 4.8. In this figure, V_{AC} (green) have an amplitude of about 500 mV, the signal V_{DC} have an average value of about 27 mV and the signal V_{Bat} reaches 3.3 V after 93 ms.

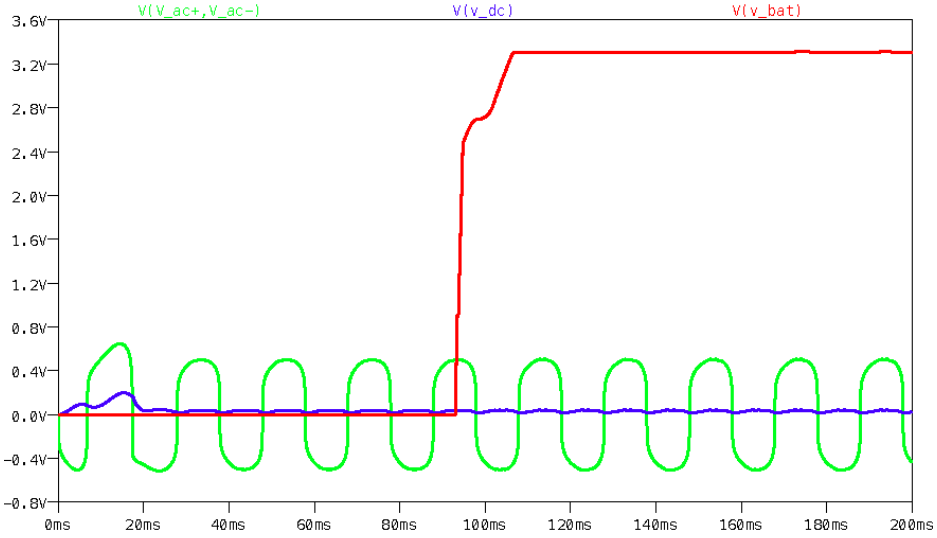


Figure 4.8: The simulated transient plot of the signals V_{AC} (green), V_{DC} (blue) and V_{Bat} (red). The system consists of a CT equivalent model, Rect2 and DC/DC1. The input to the system is $I_P = 0.7$ A

Similar figures for Rect1 and Rect3 together with DC/DC1 can be found in Appendix C, Figure C.6 and Figure C.7.

The full EH system is also simulated with DC/DC2. Figure 4.9 shows V_{AC}, V_{DC} and V_{Bat} for a simulated system consisting of a CT model, Rect2 and DC/DC2. $I_P = 6$ A. This configuration needs a higher I_P than a configuration with DC/DC1.

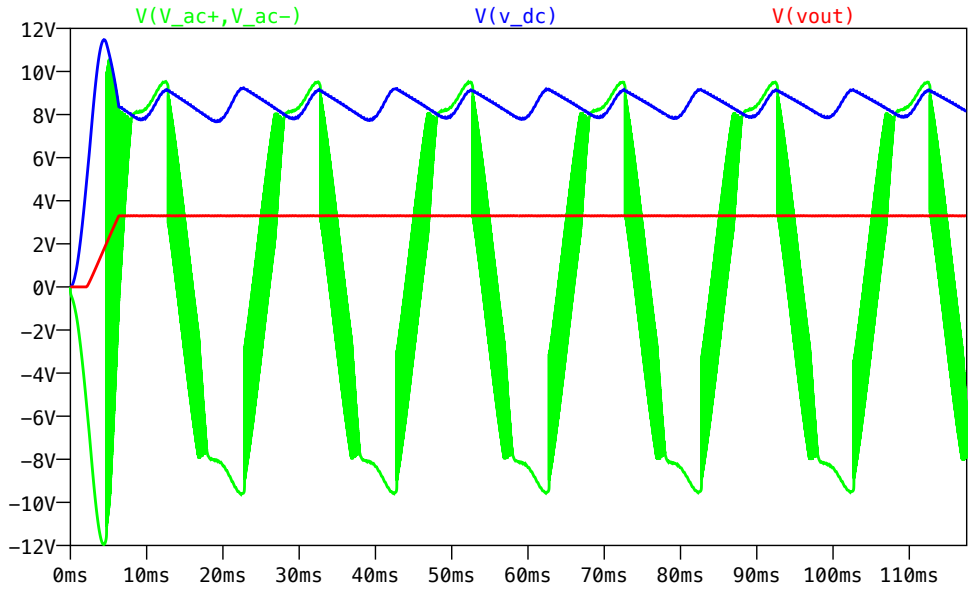


Figure 4.9: Waveforms of V_{AC}, V_{DC} and V_{Bat} for a simulated system consisting of a CT model, Rect2 and DC/DC2. $I_P = 6$A.

LTC3331 is also simulated as a combined rectifier and DC/DC converter, and not just as DC/DC2. It generally needs very high input voltages to work. Figure 4.10 shows some of the signals simulated for LTC3331 with a sinusoidal input voltage on AC1 with a 10 V amplitude, while the DC input Vin is set to float. The output voltage V_{Bat} (red) reaches 3.3 V after about 6 ms. If the input amplitude is decreased to 7.5 V, the output is no longer a constant 3.3 V signal, but decreases to 2.5 V in between the peaks of the sinusoidal signal. If the input signal is a 7.5 V DC signal on Vin however, the output voltage is stably 3.3 V, as is shown in Figure 4.4 in Section 4.1.2. In Figure 4.11, both the AC and DC inputs are used together. AC1 is set to a sinusoidal voltage with a 3 V amplitude and Vin is set to a DC voltage of 10 V. The output voltage V_{Bat} goes to 3.3 V after about 4 ms in this case, which is a little faster than when only AC1 was used as input, but not faster than when the input is only DC (shown in Figure 4.4).

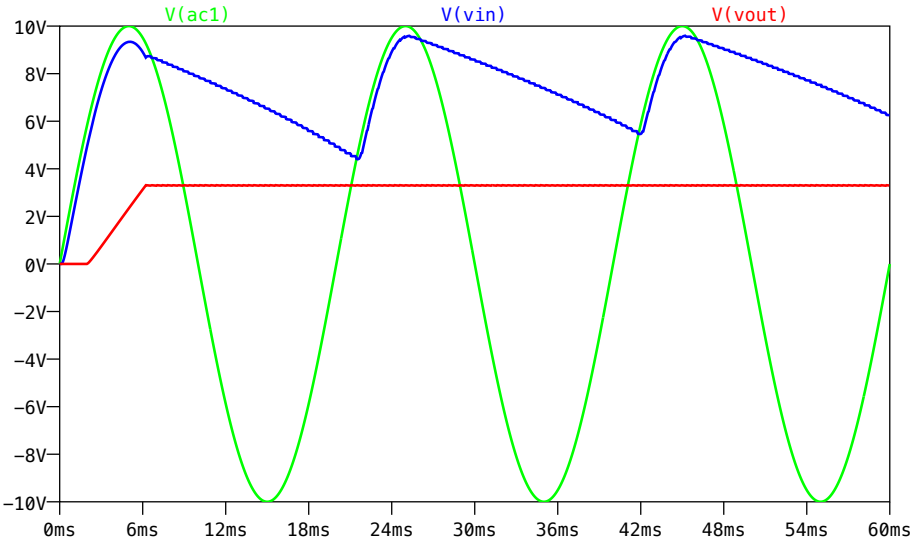


Figure 4.10: Some of the signals in and out for LTC3331 as a combined system. The input in on AC1 (green) was set to be a sinusoidal signal with an amplitude of 10V. Vin (blue) was set to float and Vout (red) is V_{Bat}.

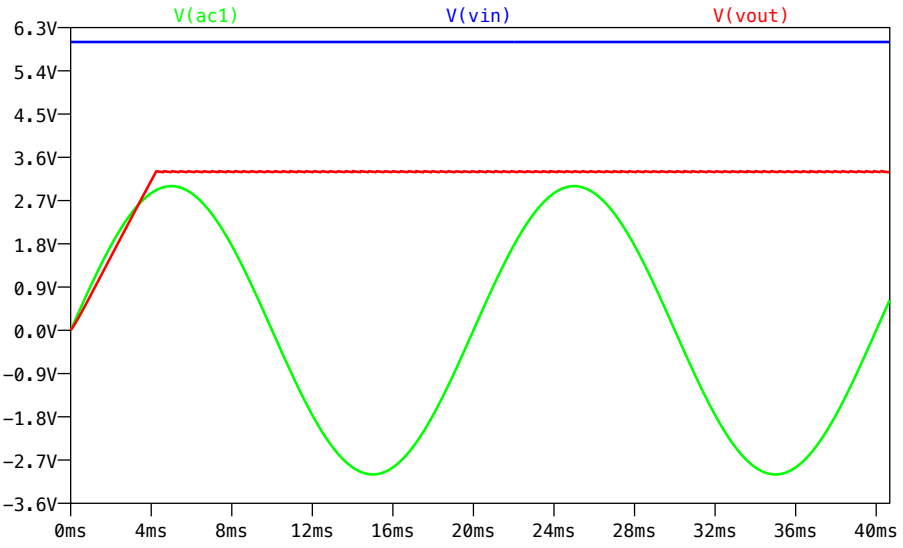


Figure 4.11: Some of the signals in and out for LTC3331 as a combined system. The input in on AC1 (green) was set to be a sinusoidal signal with an amplitude of 3V, while Vin (blue) is set to 6V. Vout is V_{Bat} and reaches 3.3 V after about 6 ms.

4.2 Measurements

This section will present the results of the measurements done on the physical implementation of the energy harvesting system.

4.2.1 Current Transformers

An example waveform is shown in Figure 4.12. The waveform are almost sine shaped.

Figure 4.12 shows the waveform results from CT2 being connected to a wire carrying $I_P = 5$A, and a load resistance of 3 Ω. The current flowing through the load resistance in this case is 6.4 mA.

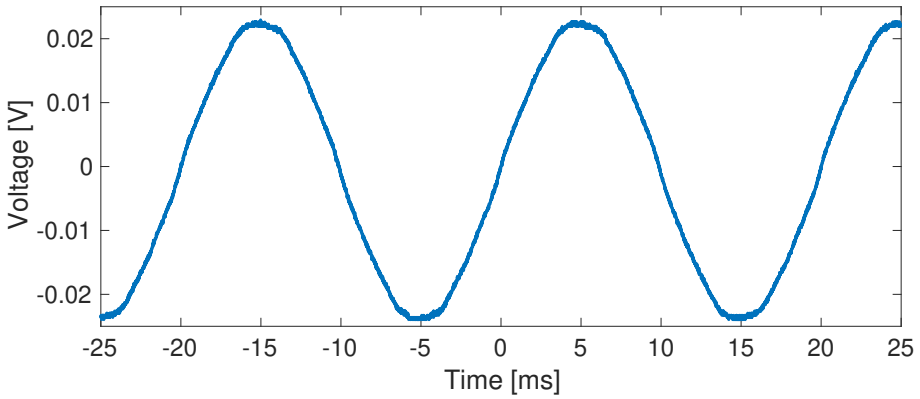


Figure 4.12: Waveform of the CT2 at 5A with 3 Ω load resistance.

Figure 4.13 shows how the different CTs output voltage changes with different load resistances for the same primary current of 1 A. Underneath the CT name the TR of the CT is stated. As the secondary voltage increases very much for the larger resistances, Figure 4.14 shows the same plot, but without the four largest resistance values, for increased readability. In Figure 4.13 CT0 looks like it is outputting a lot lower voltages compared to the other CTs. Figure 4.14 shows that for low resistances (lower than approximately 150 Ω) CT0 is actually better than the others. This is because the lower amount of secondary windings in CT0 results in a lower secondary windings resistance, meaning that more of the voltage gets transferred to the load if the load is low, than for the CTs that has a higher secondary winding resistance.

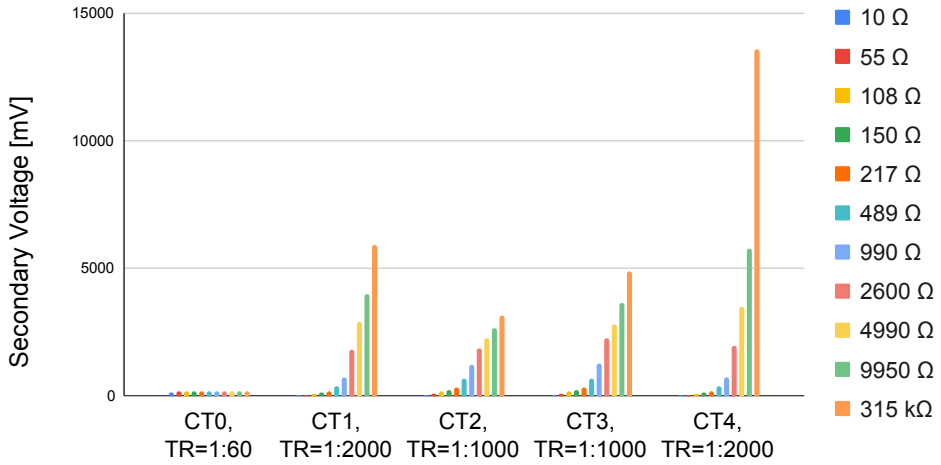


Figure 4.13: Secondary voltage vs load resistance for each of the five CTs. The primary current I_P was kept constant at 1 A.

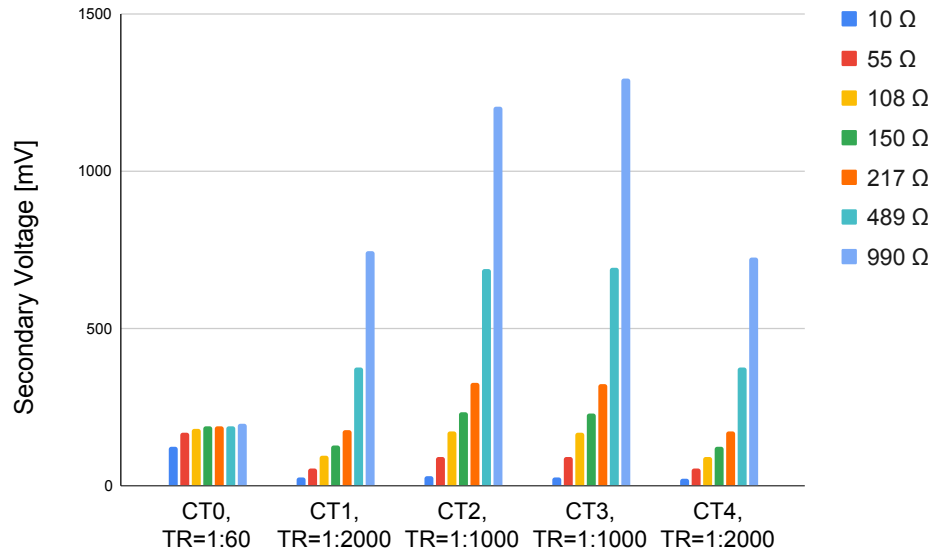


Figure 4.14: Secondary voltage versus load resistance for each of the five CTs. Fewer of the resistance values are shown, for increased readability. The primary current I_P was kept constant at 1 A.

Figure 4.15 shows how the different CTs output voltage changes with different primary currents for the same load resistance of 10 Ω. The crosses in the plot are the actual data points measured, while the lines between them are added for better readability. This figure confirms that the trend visible for low loads in Figure 4.14 are also valid for higher values for I_P as long as the load resistance is kept low.

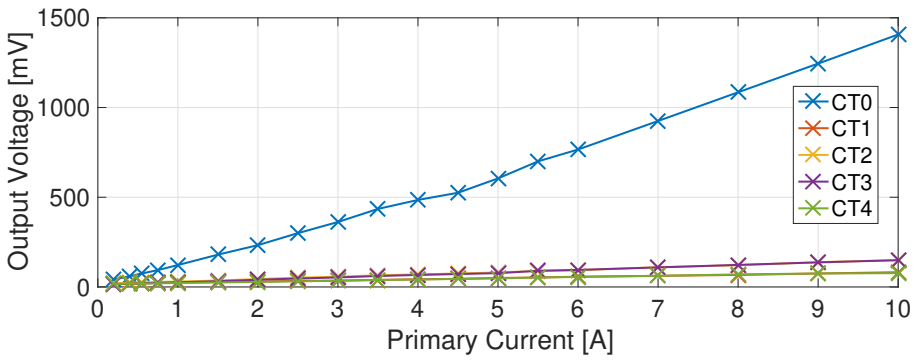


Figure 4.15: Output voltage vs primary current for each of the five CTs. The load resistance was kept constant at 10 Ω.

In Figure 4.15 it is hard to distinguish CT1 through CT4. Therefore the same figure, without CT0, is shown in Figure C.8 in Appendix C. Here, it is evident that CT1 and CT4 are the worst performing CTs for low loads. The CTs are grouped together by TR, suggesting that I_S is indeed most dependant on TR in this case as is stated by Equation (4).

4.2.2 DC/DC converters

A typical transient plot of the DC/DC1 is shown in Figure 4.16. Here, a signal generator generated 400 mV DC in on DC/DC1. This signal was measured as V_{DC} and is shown in the figure. It is measured to be approximately 50 mV, which is much lower than the 400 mV it is set to be.

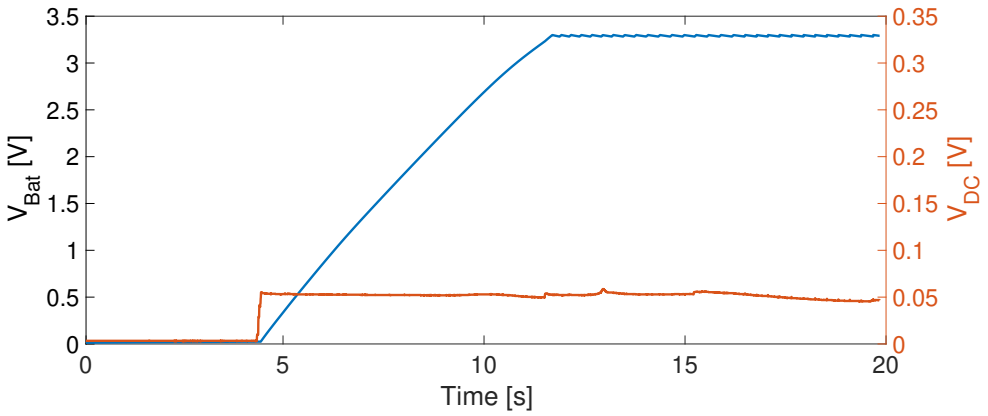


Figure 4.16: Transient plot of the DC/DC1 with an input signal V_{DC} that is 0 V until slightly before 5 s where it is changed to 50 mV.

Figure 4.17 shows a transient of the input (orange) and output (blue) of DC/DC1 when the input voltage is close to the limit of what the DC/DC1 can operate at. At first the input signal from the generator is set to be 100 mV. V_{DC} is then measured to be about 17 mV. As one can see from the figure, this makes the signal V_{Bat} increase,

but then decrease again. At between t = 100 s and t = 150 s the input signal from the generator is changed to 200 mV. The measured V_{DC} increases to about 22 mV, and V_{Bat} reaches 3.3 V after some time.

In addition DC/DC1 is tested to identify some important characteristics. The input DC resistance is measured to be 12 Ω, and a cold start requires a 45 mV DC voltage in to deliver 3.3 V out. When the DC/DC converter turns on the input resistance changes to 3 Ω, and the required voltage to deliver 3.3 V out drops to 20 mV.

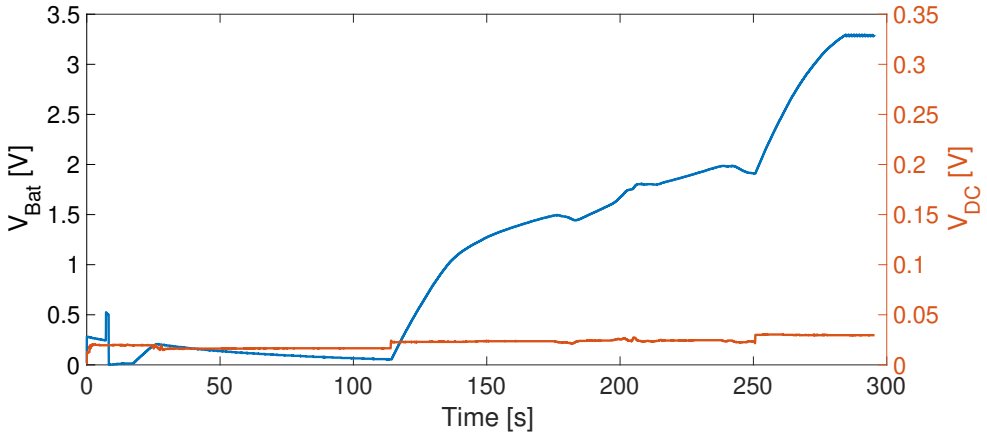


Figure 4.17: Transient plot of DC/DC1 with an input signal V_{DC} = 17 mV, and then it was changed to 22 mV at between t = 100 s and t = 150 s.

The input resistance of DC/DC2 is measured to 20 MΩ when it is off, and 36 kΩ when it is on. There is a 22 μF capacitor between the input pin and ground. Figure 4.18 shows the transient of DC/DC2 with the input voltage V_{DC} going from 0 V to 4 V at t ≈ 60 ms. It is evident that the respons time of DC/DC2 is significantly faster than that of DC/DC1. Also the voltage needed to turn it on is much higher. The evaluation board DC21551A states that the DC/DC converter part of LTC3331 should work with input voltages of between 3 V and 19 V. It is tested with both 3 V and 3.5 V in, and neither voltage level managed to get DC/DC2 to deliver 3.3 V out.

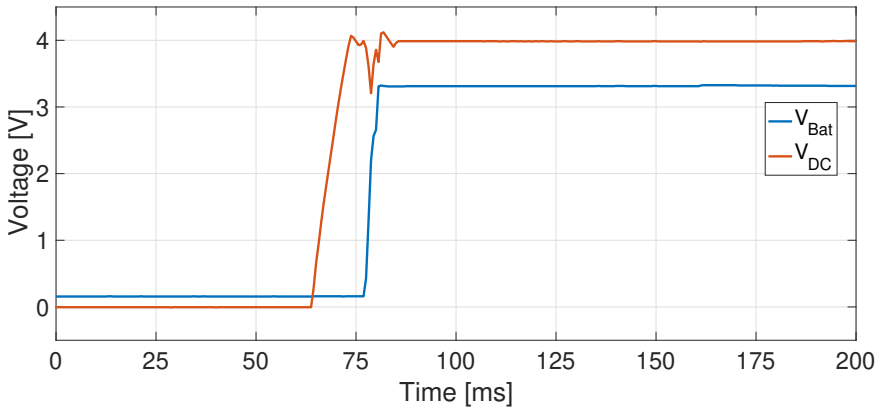


Figure 4.18: Transient plot of DC/DC2 with an input signal $V_{DC} = 0$ V, and then it is changed to 4 V at t $\approx$ 60 ms.

4.2.3 Rectifiers

The waveform of the different rectifiers is dependant on several factors, like if the input is a CT or a voltage source, the magnitude of the signal in and the load.

Without a load the resulting output of a rectifier will not be a DC signal, but a strictly positive version of V_{AC}.

An example waveform of this case is shown in Figure 4.19. Here, Rect2 is used as to show the example. The input signal, shown in blue, to Rect2 is a sinusoidal voltage from a voltage source with 500 mV amplitude and a 50 Hz frequency. The resulting output signal, in orange, is a strictly positive version of the input.

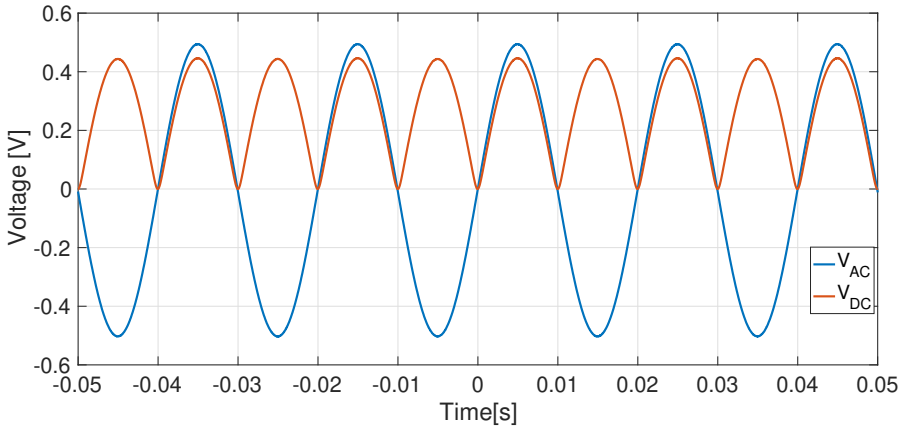


Figure 4.19: Output voltage (orange) and V_{AC} (blue) for Rect2 with a no load connected.

By adding a capacitor to the output, the output signal is smoothed out by the capacitance, and the same circuit as before produces a DC voltage instead, as shown in Figure 4.20.

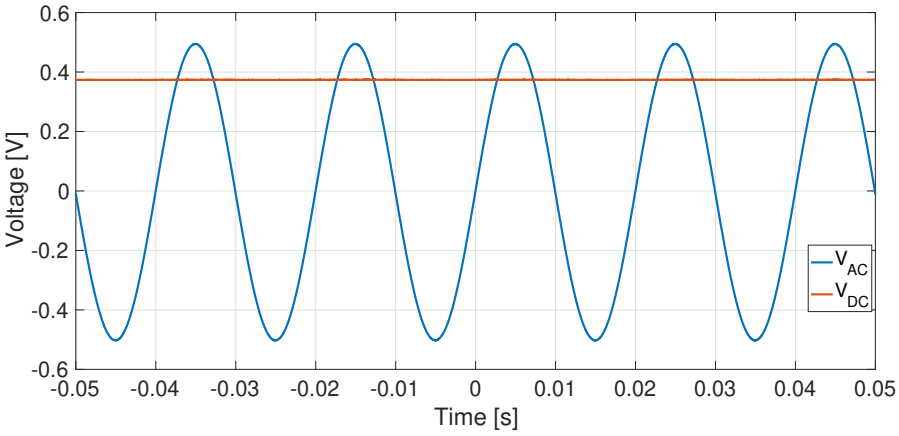


Figure 4.20: V_{DC} (orange) and V_{AC} (blue) for Rect2 with a 300 μF load capacitor connected.

Figure 4.21 shows the output of Rect2, V_{DC} (orange), and the input, V_{AC} (blue), when the rectifier is connected to a load of 12 Ω, which is equal to the DC resistance measured on the input of DC/DC1 when it is not on. This is a relatively small load resistance from the rectifier, that results in the output voltage V_{DC} being much lower than V_{DC} is in Figure 4.20.

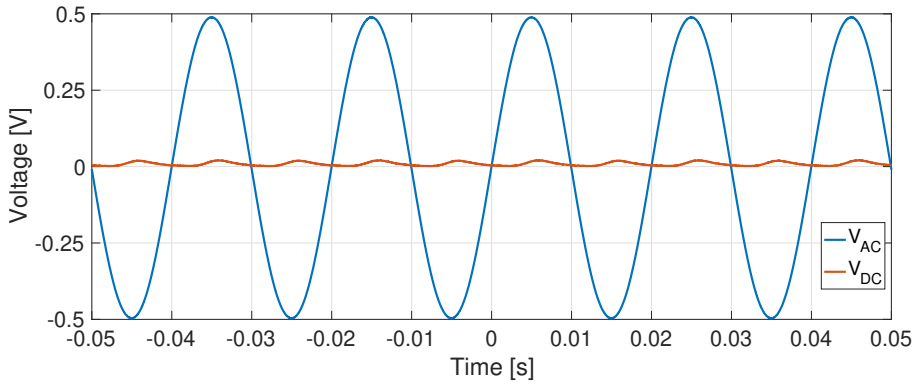


Figure 4.21: V_{DC} (orange) and V_{AC} (blue) for Rect2 with a load of 12 Ω.

In Figure 4.22 Rect2 is tested with different load resistances, and different values of V_{AC} to investigate the impact this has on the signal V_{DC}. The DC/DC2 and the "No resistance" lines are more or less overlapping for all V_{AC}.

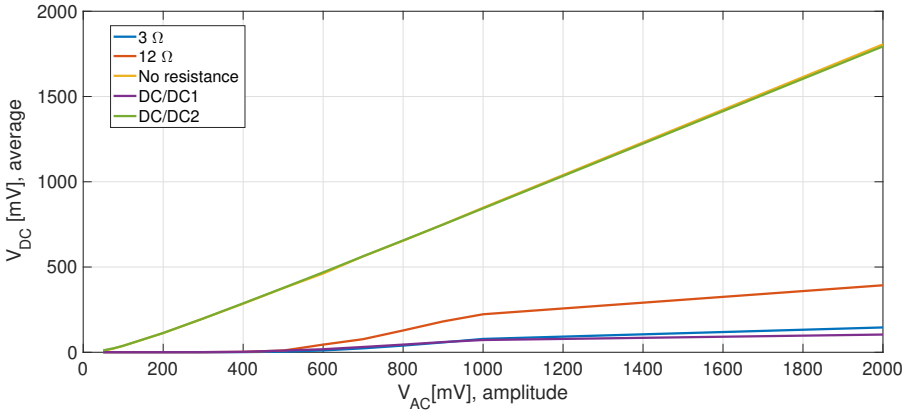


Figure 4.22: Measured V_{DC} at Rect2 for different load resistances at different values of V_{AC}.

Figure 4.23 shows V_{DC} in orange and V_{AC} in blue for Rect1 with a DC/DC1 as a load and a 2 V, 50 Hz V_{AC} from a voltage source.

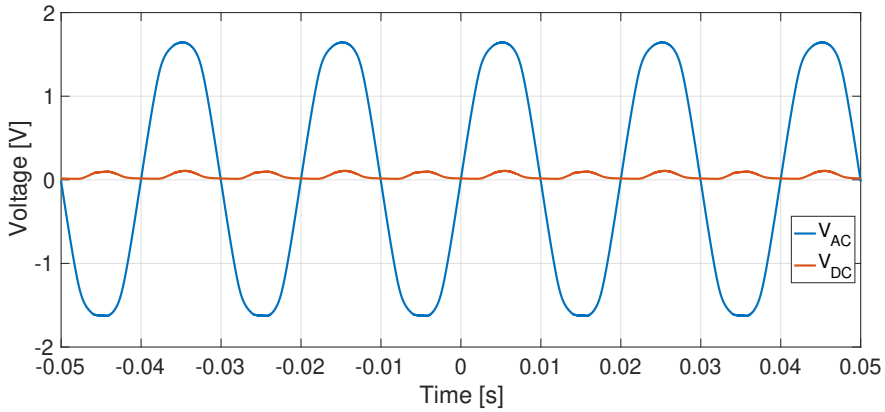


Figure 4.23: V_{DC} (orange) and V_{AC} (blue) for Rect1 with DC/DC1 as a load.

Rect1 is also tested with different load resistances and different values of V_{AC} to look at the resulting values of V_{DC} this gives. This is shown in Figure 4.24.

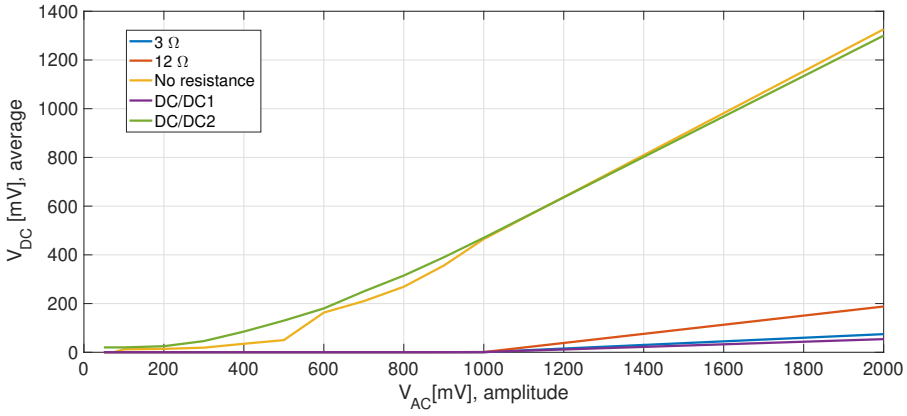


Figure 4.24: Measured V_{DC} for different load resistances and different values of V_{AC} on Rect1.

Figure 4.25 shows the waveforms of V_{DC} in orange and V_{AC} in blue when Rect3 was connected to CT2 as source and a load of 10 kΩ and 100 μF. The current I_P was 0.5 A.

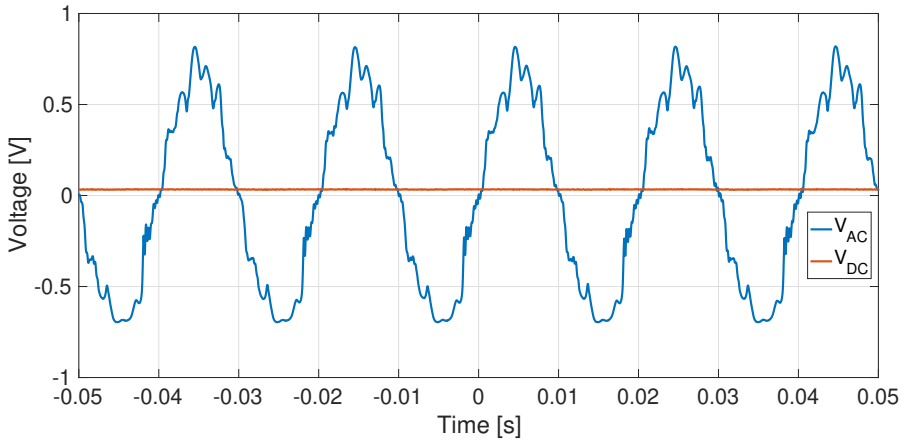


Figure 4.25: Measured V_{DC} (orange) and V_{AC} (blue) for Rect3 with CT2 as source and a load of 100 μF and 10 kΩ.

Figure 4.26 shows the difference in output voltage from the transistor based rectifier with 10 kΩ, 12 Ω and DC/DC2 as a load. With the 12 Ω load, the output voltage of the transistor based rectifier is 0, no matter the primary current. With 10 kΩ the system started to get a lower output after about $I_P = 0.5$ A, and with the DC/DC2 the system stopped working after $I_P = 1.7$ A, where it started to output 16 mV.

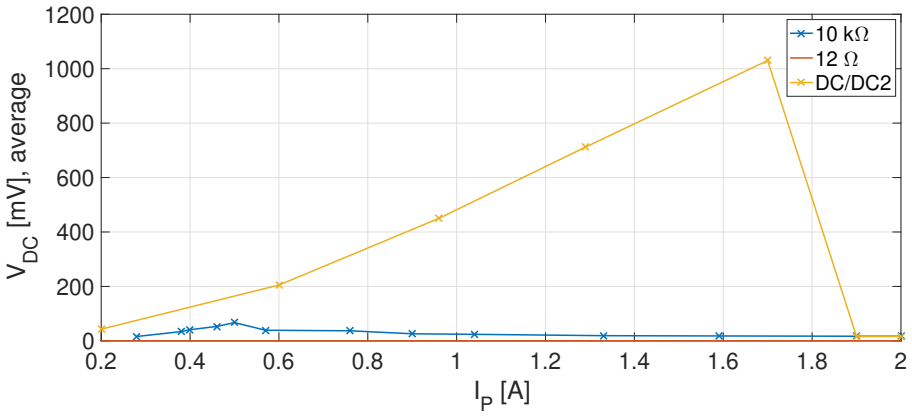


Figure 4.26: V_{DC} versus I_P for Rect3 with CT2 as source and a load of 10 kΩ (blue), 12 Ω (red) and DC/DC2 (yellow).

4.2.4 Full system

The whole energy harvesting system is tested by putting the different parts together to one system. First the system is presented with DC/DC1, and then with DC/DC2.

DC/DC1

First, the full system is tested with the DC/DC1. The different rectifiers produce different results, and are presented individually. The different CTs were tested together with this, but only CT2 gave interesting results when combined with the rest of the system, and therefore all results presented in this section is using CT2 as a source. The others generally only gave 0 V out of the rectifiers for the currents tested ($<$ 16 A). In order to overcome the problem of the difference in input impedance of the DC/DC1 and the output impedance of the rectifiers, a switch and a capacitor is added. This switch and capacitor and their placements is shown in Figure 2.9.

The system is tested using Rect2 with CT2 and DC/DC1. Figure 4.27 shows V_{AC} in blue, and V_{DC} in orange. In this case the switch is open. V_{DC} is a DC signal, but V_{AC} is not a sinusoidal signal. These waveforms are produced when $I_P = 5$ A. The resulting waveforms for the same system with the same I_P but when the switch is closed ais shown in Figure 4.28. Also here V_{AC} is blue and V_{DC} is orange. The amplitude of V_{AC} becomes much smaller when the switch closes, and V_{DC} drops from almost 6 V when the switch was open, to 26 mV. This is just enough to turn DC/DC1 on, and produce $V_{Bat} = 3.3$ V.

The waveform for Rect1 when the switch is down can be found in Appendix C in Figure C.9.

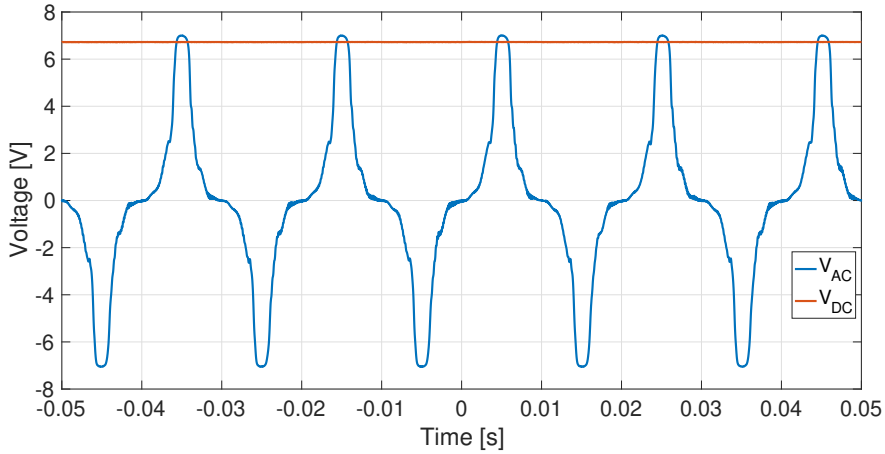


Figure 4.27: Waveform of V_{AC} (blue) and V_{DC} (orange) for Rect2 with CT2, capacitor, switch and DC/DC1. Switch is open and $I_P = 5$ A.

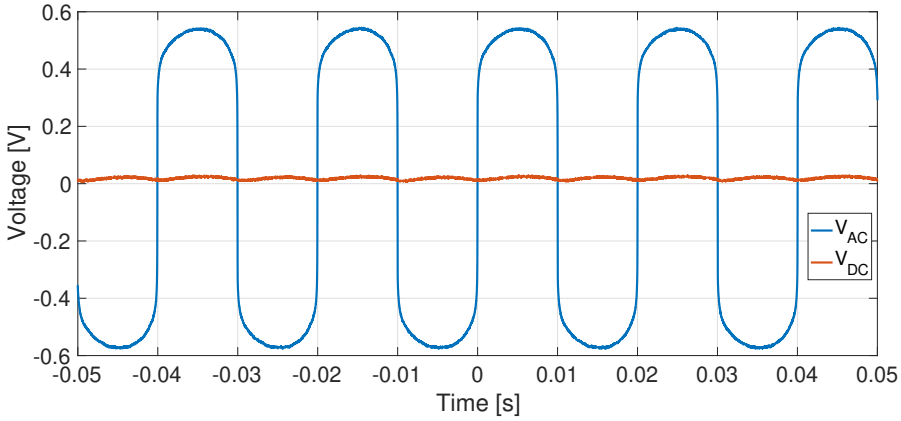


Figure 4.28: Waveform of V_{AC} (blue) and V_{DC} (orange) for Rect2 with CT2, capacitor, switch and DC/DC1. $I_P = 5$ A and switch is closed.

DC/DC2

The system is also tested with DC/DC2. The system is tested first with CT2, which is the same as for the DC/DC1. The switch and capacitor configuration was not needed for DC/DC2 as the input resistance of the DC/DC2 is high enough by itself to get a sufficient power transfer.

Figures 4.29 and Figure 4.30 shows waveforms of V_{AC} (blue) and V_{DC} (orange) for the system CT2, Rect1, DC/DC2. In the case of Figure 4.29 I_P is 3.3 A, and DC/DC2 is off. In Figure 4.30 I_P is 4.1 A, and the DC/DC2 is turned on and delivers 3.3 V out. The shape of the waveform changes when DC/DC2 is turned on.

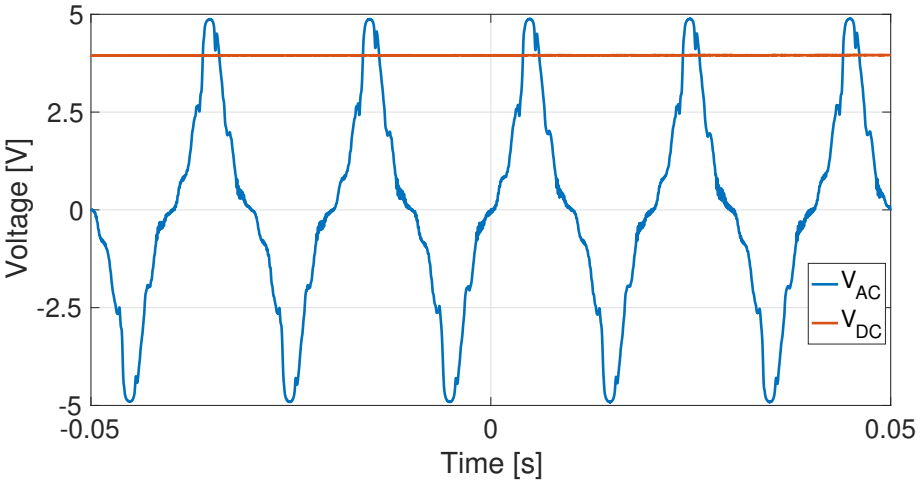


Figure 4.29: V_{AC} (blue) and V_{DC} (orange) measured on Rect1, with CT2 as a source, and DC/DC2 as a load. DC/DC2 was turned off. $I_P = 3.3$ A.

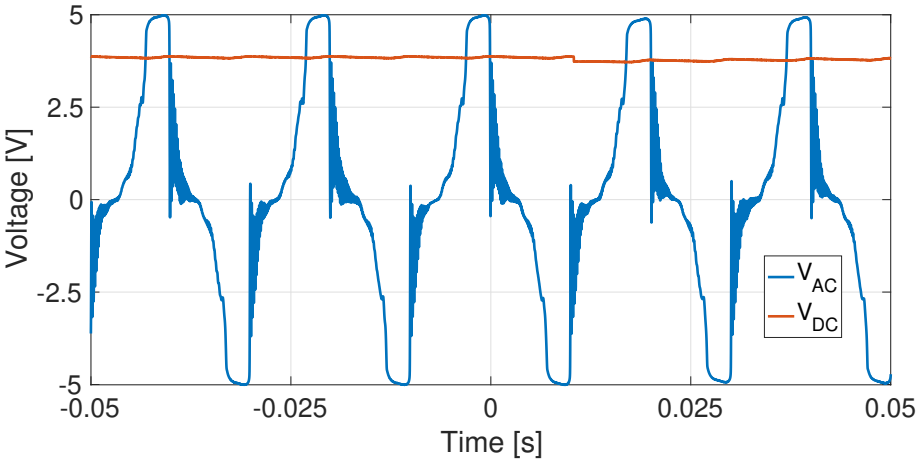


Figure 4.30: V_{AC} (blue) and V_{DC} (orange) measured on Rect1, with CT2 as a source, and DC/DC2 as a load. DC/DC2 was turned on. $I_P = 4.1$ A.

Figure 4.31 shows V_{AC} (blue) and V_{DC} (orange) for the system consisting of CT2, Rect2 and DC/DC2. $I_P = 3.9$ A, and DC/DC2 delivers 3.3 V out.

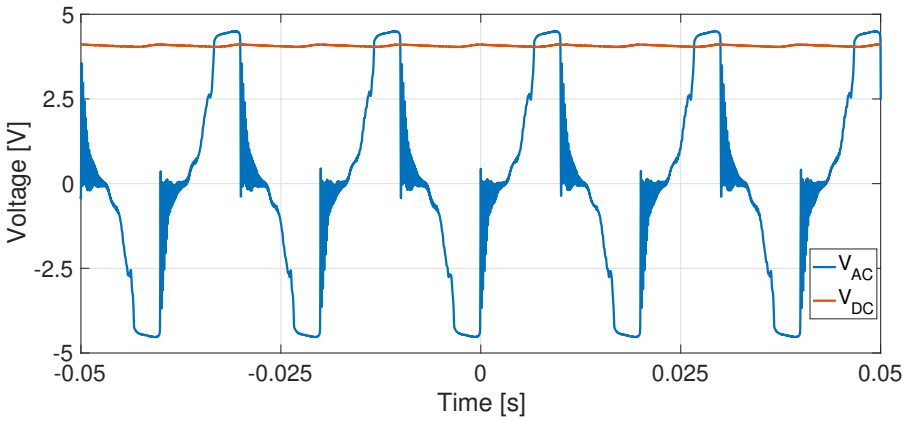


Figure 4.31: V_{AC} (blue) and V_{DC} (orange) measured on Rect2, with CT2 as a source, and DC/DC2 as a load. DC/DC2 was turned on. $I_P = 3.9$ A.

Figure 4.32 shows V_{AC} in blue and V_{DC} in orange. The system tested consists of CT2, Rect3 and DC/DC2. Here $I_P = 0.13$ A, and the rectifier is still rectifying the voltage, even though the amplitude of V_{AC} is only 0.2 V. This is lower than the forward voltage of the schottky diodes 1N5819, making Rect3 the rectifier that is capable of working at the lowest voltage levels of the ones tested in this thesis. V_{DC} is approximately 50 mV.

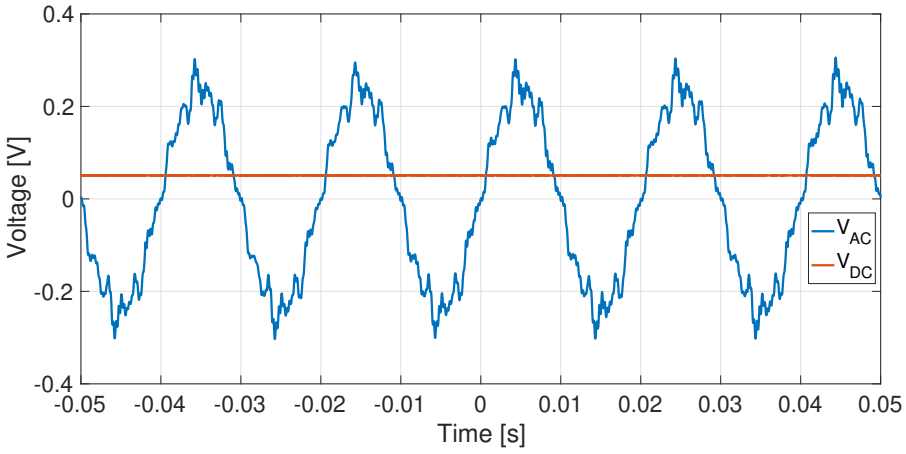


Figure 4.32: V_{AC} (blue) and V_{DC} (orange) measured on Rect3, with CT2 as a source, and DC/DC2 as a load. The switch is open during the measurement. $I_P = 0.13$ A.

All the rectifiers are tested with all the CTs. Generally CT4 has proved to be the best one. This is different from a system with DC/DC1, for which CT2 was the best. Figure 4.33shows V_{AC} (blue) and V_{DC} (orange) for a system consisting of CT4, Rect1 and DC/DC2.

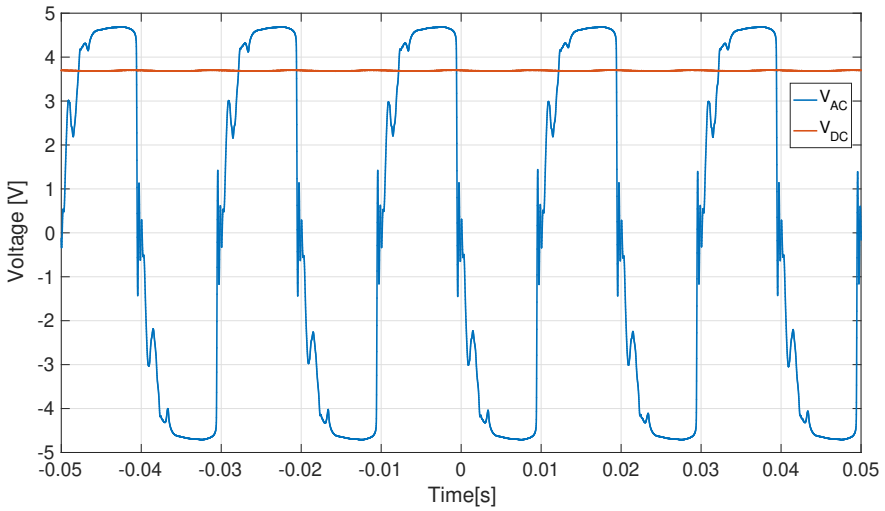


Figure 4.33: Waveform showing V_{AC} (blue) and V_{DC} (orange) produced by the combination of CT4, Rect1 and DC/DC2 with $I_P = 0.75$ A.

Figure 4.34 shows V_{AC} (blue) and V_{DC} (orange) for a system consisting of CT4, Rect2 and DC/DC2. Of all the combinations tested in this thesis, this combination proved to be able to deliver $V_{Bat} = 3.3$ V for the lowest I_P, namely 0.5 A.

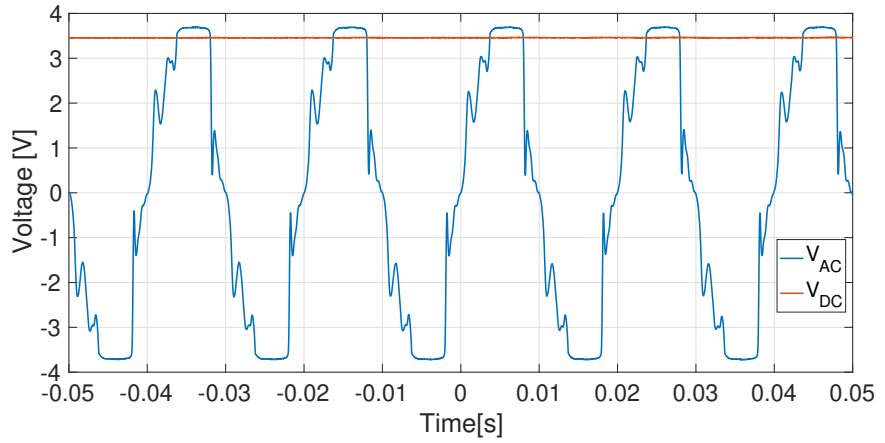


Figure 4.34: Waveform showing V_{AC} (blue) and V_{DC} (orange) produced by the combination of CT4, Rect2 and DC/DC2 with $I_P = 0.5$ A.

Rect3 did not manage to deliver a V_{DC} to DC/DC2 so that $V_{Bat} = 3.3$ V at any point. Using DC/DC2 as a load does however make the rectifier work with very low I_Ps. It was tested with all CTs as a source, and for all the CTs it worked and produced a DC voltage out at I_P being just 80 mA. This is the lowest I_P possible to generate with the resolution of the variac. Figure 4.35 shows V_{DC} for each of the five CTs at $I_P = 80$ mA. With CT4 connected, Rect3 produced a 496 mV DC voltage when $I_P = 80$ mA. The waveform for this case is shown in Figure 4.36. Here, V_{AC} is orange and V_{DC} is blue.

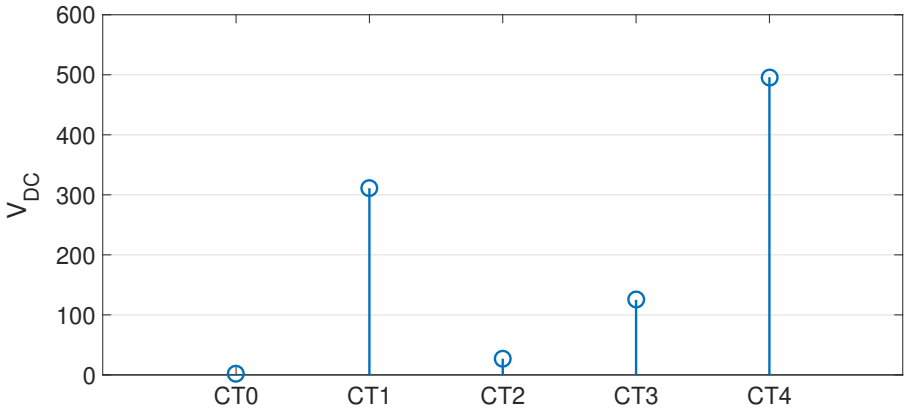


Figure 4.35: V_{DC} for each of the five CTs connected to Rect3 with $I_P = 0.08$ A.

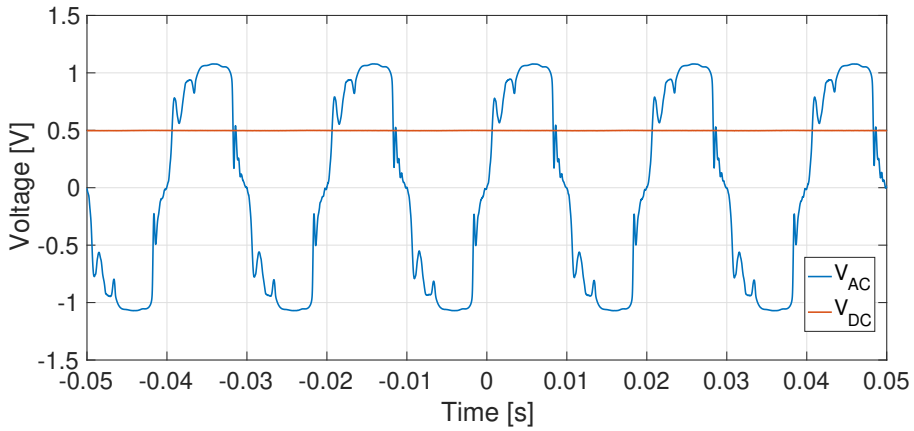


Figure 4.36: Waveform showing V_{AC} (orange) and V_{DC} (blue) produced by the combination of CT4, Rect3 and DC/DC2 with $I_P = 0.08$ A.

The problem with this rectifier is that after I_P becomes high enough (different value for different CTs), V_{DC} suddenly drops to about 15 mV. Figure 4.37 shows V_{AC} (blue) and V_{DC} (orange) for a system consisting of CT2, Rect3 and DC/DC2 when $I_P = 1.9$ A. This is the point when I_P is just high enough to make V_{DC} drop to 16 mV. This is lower than when $I_P = 0.13$ A in Figure 4.32. In addition to V_{DC} being lower that in Figure 4.32 it is also apparent that the shape of V_{AC} is very different. This change in shape occurs at the same time as the drop in V_{DC} and happens just as abruptly.

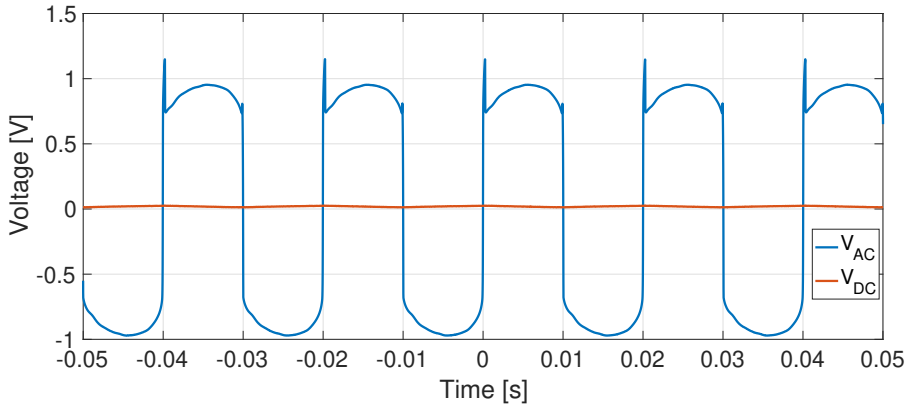


Figure 4.37: V_{AC} (blue) and V_{DC} (orange) measured on Rect3, with CT2 as a source, and DC/DC2 as a load. I_P = 1.9 A.

Overview

For a simpler overview of all the different system configurations tested, all configurations are shown in Table 5. It presents the lowest I_P that made the DC/DC converter deliver V_{Bat} = 3.3 V for all system configurations. The table contains three different colours, green, blue and white, as well as different gradients within the same colour. Green is used to denote that the configuration in question manages to deliver V_{Bat} = 3.3 V for $I_P < 1$ A, which is the goal of this thesis. Blue means that the system configuration in question delivers V_{Bat} = 3.3 V out, but only for $I_P > 1$ A. White signifies that V_{Bat} did not reach 3.3 V for any I_P up to 16 A, which is the highest I_P tested. Darker colour gradient means that 3.3 V out is achieved with a lower I_P. Table 5a shows the results for the systems made using DC/DC1 as a DC/DC converter, while Table 5b shows the results for the systems implemented using DC/DC2 as a DC/DC converter.

Table 5: Compiled results of different sub-system configurations. The number denotes the lowest I_P [A] that turns the DC/DC on and delivers V_{Bat} = 3.3V. Green signifies that the system configuration meets the requirement. White means the configuration never produced V_{Bat} = 3.3 V out, and blue signifies that the configuration works, but do not meet the requirements. (a) shows the results of configurations using DC/DC1, while (b) shows the results from configurations containing DC/DC2.

(a) DC/DC1

	Rect1	Rect2	Rect3
CT0	-	-	-
CT1	-	-	-
CT2	7	5	-
CT3	-	-	-
CT4	-	-	-

(b) DC/DC2

	Rect1	Rect2	Rect3
CT0	-	-	-
CT1	1.6	1.0	-
CT2	4.3	3.7	-
CT3	1.3	1.2	-
CT4	0.8	0.5	-

From Table 5 one can see that the best result is achieved with the combination of CT4, Rect2 and DC/DC2. This combination manages to give an output of 3.3 V to the battery with I_P = 0.5 A. This is lower than the 1 A goal set in the beginning. Other

combinations that also give 3.3 V out at sub 1 A I_P are CT1, Rect2 and DC/DC2 and CT4, Rect1 and DC/DC2.

To make sure the system can handle up to 16 A, which can be expected in common household cables, the best performing sub-system configuration is tested with $I_P = 16$ A. This is shown in Figure 4.38.

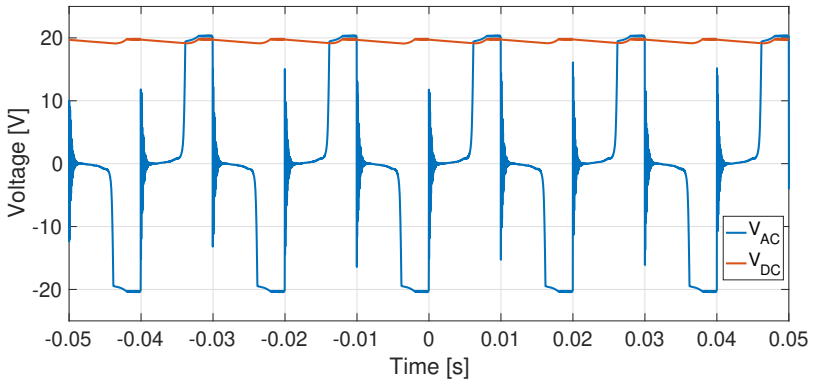


Figure 4.38: Waveform showing V_{AC} (blue) and V_{DC} (orange) produced by the combination of CT4, Rect2 and DC/DC2 with $I_P = 16$ A.

The two other sub-system configurations that produced $V_{Bat} = 3.3$ V at $I_P < 1$ A are also tested up to $I_P = 16$ A, and those resulting waveforms can be found in Appendix C. The resulting waveform from the sub-system configuration consisting of CT4, Rect1 and DC/DC2 can be found in Figure C.10, while Figure C.11 shows the resulting waveform from the combination of CT1, Rect2 and DC/DC2.

The commercial system LTC3331 is tested as a combined rectifier and DC/DC, with a battery connected to the evaluation board DC2151A, and the jumpers set to "charge". All CTs are tested as an input on AC1, and the CTs that manages to turn LTC3331 on with the lowest I_P are CT2 and CT4. For both these CTs LTC3331 needs $I_P = 5$ A to produce 3.3 V on the output. Figure 4.39 shows the waveform when I_P is 5 A.

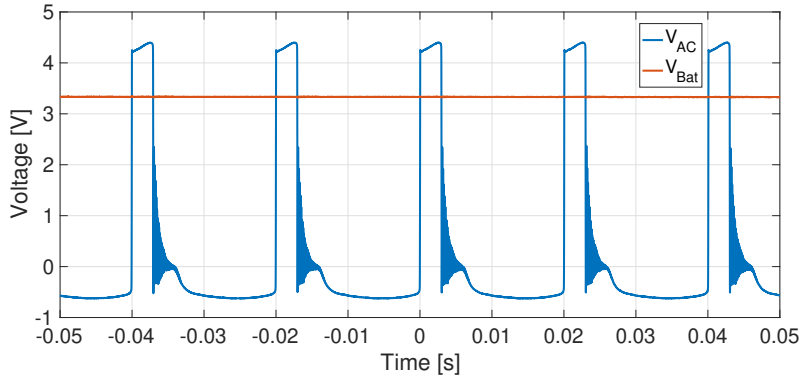


Figure 4.39: Waveform showing V_{AC} (blue) and V_{Bat} (orange) when the AC1 input of LTC3331 is used with CT4 and $I_P = 5$ A.

5 Discussion

This sections will discuss the different results from Section 4.

5.1 CTs

The initial simulation of a CT in Section 4.1.1 does show that the I_P and I_S relationship is in accordance with Equation (4). The changing of parameters to make the model less ideal, by including I_e does however not increase the accuracy of the model. Often, what happens when going from simulations to physical measurements is that the actual measurement is worse than the ideal calculated value, due to different kinds of loss. Here, the measured value is larger than what the ideal equation predicts, which means that something is happening that is not accounted for in the original theory. A hypothesis as to why this is, is that the CT has a high permeability core that enhances the magnetic field that is present around I_P, so that the induced I_S becomes larger than the one predicted by the equations used in the SPICE model.

Looking at the different CTs in Figure 3.9 one can see that they have different sizes. Comparing the sizes to the current ratings in Table 4 it is obvious that the physically larger CTs CT0 and CT4, are also the ones that can handle the largest currents before saturating. This is also consistent with [17], that states that larger CTs saturate on larger currents.

Figure 4.13 and Figure 4.14 show the output voltage of the different CTs for different load resistances. There is a clear difference between CT0 and the rest of the CTs. CT0 has a much lower amount of secondary windings than any of the other CTs, as well as a lower secondary winding resistance. This results in higher load resistances not making the secondary voltage any higher for CT0, which is the case for the other CTs.

Looking at Figure 4.14 it is evident that the TR of the CT influences the secondary voltage, as is predicted in Equation (4), where I_S is dependant of TR. CT2 and CT3 both have a TR of 1:1000, while CT1 and CT4 have a TR of 1:2000. In Figure 4.14 CT1 and CT4 have almost identical Secondary voltages for each load resistance. The same goes for CT2 and CT3.

However, Figure 4.13 shows that for higher load resistances this is no longer true. Here, CT4 starts having larger secondary voltages than CT1, and CT3 has higher secondary voltages than CT2, for the same load resistance. This can be explained by looking at the secondary winding resistances of the CTs in Table 4. Here, it can be seen that CT1 has a higher secondary winding resistance than CT4, and that CT2 has a higher secondary winding resistance that CT3. Looking at the system of CT in series with the load resistance as a voltage divider, it makes sense that in the case where the CT has a lower secondary winding resistance for the same TR lets more of the voltage transfer to the load, than for the CTs that have a higher secondary winding resistance.

These observations do not hold true for CT0, which is very different from the others. CT0 has a TR of 1:60 and a secondary winding resistance of 0.3 Ω. For very low load resistances, up to and including 108 Ω, CT0 is indeed the CT that provides the highest secondary voltage. To understand why after this point, it is not any more, it can be helpful to look at Figure 2.2. For all the measurements, I_P is constantly 1 A. I_{PS} is proportional to I_P and is also constant. As the load resistance increases above than 108 Ω, the secondary voltage no longer increases with it. According to Ohms law, this means that I_S must become smaller as the load resistance increases for the secondary voltage to be close to constant. If I_S decreases, I_e increases when I_{PS} is constant, according to KCL. As stated in Section 2.2, Z_e is an impedance that can change [17], and thus explain this behaviour.

Figure 4.15 shows that for a low load resistance of 10 Ω CT0 produces a higher voltage for all I_P than any of the other CTs. This indicates that the CT does not saturate for higher I_Ps as [17] predicts, since it is physically large. It is the high load resistances that makes the CT stop producing higher voltages.

5.2 DC/DC converters

The hypothesis in Section 2.2.2 states that the most important characteristic of the DC/DC converter is that it should be able to work with the input voltage being as low as possible. This hypothesis has been disproved. Although DC/DC1 has the ability to transfer voltages as low as 20 mV up to 3.3 V, it is not a suitable DC/DC converter for this system. The DC/DC1 has a very low input resistance. It is so low that no matter which one of the rectifiers it is connected to, the power transfer to the rectifier becomes very small, since the input impedance is much smaller than the output impedance of the rectifiers.

DC/DC2 was considered a bad choice at first due to the fact that it needs 3 V in to work. The simulations indicate that it needs a 4 V input voltage to deliver $V_{Bat} = 3.3$ V. It turned out that the fact that it has an equivalent on resistance of 36 kΩ, which is much higher than the output resistance of any of the rectifiers, is much more important for the over all performance of the system. Figure 4.22 and Figure 4.24 show that the performance of Rect1 and to is the same when DC/DC2 is connected to them, as when no resistance is connected to them. This is the reason that all three sub-system configurations that fulfil the requirements use DC/DC2.

A DC/DC converter that combines high input resistance with a low threshold voltage would be ideal. There are signs that there probably exists a trade off between the threshold voltage needed to achieve 3.3 V out and the input impedance, due to ohms law. The ideal DC/DC converter for such a system would have an input resistance equal to the output impedance of the rectifier (maximum power transfer theorem), meaning that a DC/DC converter with a little lower input impedance and also lower threshold voltage than DC/DC2 would be optimal, but not so low as that of DC/DC1. This would also result in a system with a maximum possible η.

5.3 Rectifiers

Three different rectifiers are presented, simulated and tested in this thesis. Their performance is very varying. The simulated performance is shown in Figure 4.7. In this figure Rect2 is the best rectifier, Rect3 is the second best, and Rect1 is the worst. The measured performance of Rect2 is shown in Figure 4.22, of Rect1 in Figure 4.24 and of Rect3 in Figure 4.26. These figures show that Rect2 is still the best when physically implemented, but now Rect1 is performing better than Rect3. Rect3 gives a rectified voltage out on the lowest I_P of the three, but the voltage is never high enough to actually turn a DC/DC converter on.

It was predicted that Rect2 should have a better performance than Rect1, because it is implemented with the same circuit topology, but with diodes that have a lower forward voltage than Rect1. Rect3 was predicted to work better than both Rect1 and Rect2, because it is implemented with transistors that have a lower threshold voltage than diodes can have. However, it turned out to be the worst performing rectifier over all. There are two main reasons for this. The transistors used are chosen because of their low threshold voltage. That parameter comes at the expense of others. The r_{ds} of the transistors are very high compared to the input impedance of DC/DC1. That means

that even though Figure 4.26 shows that Rect3 is able to deliver a higher V_{DC} than the threshold of DC/DC1 for very low I_P, the input resistance of DC/DC1 forces the voltage so low for all I_P that it never reaches 20 mV. For DC/DC2 there is different problem. The input resistance is much higher, so the problem of matching the impedances disappears. However, as is very apparent in Figure 4.26 the rectifier is not suited for high I_Ps. After some threshold, that is different depending on the load connected, the DC voltage coming from Rect3 suddenly drops to a very low level. This level is about 15 mV. The reason for this is not trivial. A theory is that the transistors are put under a too high voltage, so that they overload. The datasheets state that the maximum voltage the NMOS can handle is ±10 V, while it is ±8 V for the PMOS. The voltages that are present when the sudden voltage drops happen are much lower than these maximum ratings, but the current is not measured, so it might be that the current present causes an overload to happen. A MOSFET based rectifier using transistors that do not overload at low voltages would maybe perform better than Rect1 as is the case in the simulations.

5.4 Full system

Table 5 shows a full overview of the different configurations of sub-systems. Of the 30 combinations tested, only three combinations fulfil the requirement of being able to produce V_{Bat} = 3.3 V at I_P <1 A. Those three are the ones marked in green. It is evident that the three system configurations marked in green have something in common. They all use DC/DC2, and none use Rect3 or CT0. The best configuration uses DC/DC2, CT4 and Rect2. This configuration is able to work at I_P being just 0.5 A. If Rect2 is swapped for Rect1, the minimum I_P needed to produce V_{Bat} = 3.3 V increases from 0.5 A to 0.8 A. The diodes used in Rect1 have a higher threshold voltage than the diodes in Rect2, which is why it needs a slightly higher I_P. If CT4 is swapped for CT1, the minimum I_P needed to produce V_{Bat} = 3.3 V increases to 1 A. The reason why this configuration is marked as sub 1 A is that it was measured to be 0.96 A but for the sake of putting the measurement in the table it was rounded to 1 A. CT1 has the exact same TR as CT4, but has a secondary winding resistance that is significantly higher. The secondary winding resistance of CT4 is 164 Ω while the secondary winding resistance of CT1 is 485 Ω. The lower the secondary winding resistance makes more of the voltage transfer to the rectifier when all else stays the same, making this sub-system configuration slightly better.

DC/DC1 has an input impedance that is so low that the voltage connected to it is driven low even for an actual signal source, as is shown in Figure 4.16, where 400 mV becomes 50 mV when connected to DC/DC1. This is why all of the configurations that contain this DC/DC converter fail to meet the requirements. Also, not a single system that includes CT0 manages to produce 3.3 V out at any point for all the I_Ps tested. As shown in Figure 4.13, this CT is a good choice for very low loads. The DC/DC1 has a low equivalent DC input resistance, and could be such a low load, but since a rectifier must be connected between the two components, this can not be exploited. That be unless a rectifier is found that has an input impedance of 0.3 Ω and an output impedance of 3 Ω. All the rectifiers in this thesis however, has in- and output impedances much higher than this, and thus removes that possibility. The last sub-system that does not work in any case is Rect3. Rect3 is designed to be able to work on as low voltages as possible. Figure 4.35 shows that Rect3 does this very effectively, but as shown in Figure 4.37 it stops working to fast when I_P increases for it to be a useful rectifier.

Waveforms

The three sub-system configurations that manage to deliver $V_{Bat} = 3.3$ V for $I_P < 1$ A are all tested with I_P up to 16 A. This was shown in Figure 4.38, Figure C.10 and Figure C.11. When steadily increasing I_P to 16 A it was observed that the amplitude of V_{AC}, and the level of V_{DC} increased for increasing I_P only up to a point. After this point the levels stayed the same for all I_P up to $I_P = 16$ A. For the two sub-system configurations containing CT4, this point was $I_P = 7$ A, while for the sub-system configuration containing CT1, this point was $I_P = 5$ A. It thus seems that the point where the voltage stops increasing is dependent on which CT is used, and it is likely that this happens due to the saturation of the CT core. The shape of the waveforms of V_{AC} supports the assumption that the CTs are responsible for this behaviour. Comparing the waveforms of V_{AC} to example waveforms of CTs that saturate in [17], the shape is similar. Figure 4.27 has the exact shape that is present when a CT that is connected to a capacitive load is saturated. The shape in Figure 4.38 is not identical to that in Figure 4.27, but contains an additional spike going in the opposite direction after each maximum or minumum. A similar behaviour is also shown in [17], all though the spikes there are not as sharp.

Figure 4.28 shows V_{AC} and V_{DC} for the same system as Figure 4.27. The only difference is whether the switch in the system (shown in Figure 2.9) is closed or open. After some time after the switch is closed, the capacitor present, C_1 is discharged, and the circuit is equivalent to one that just does not have a switch and capacitor in it. That is the circuit that is simulated in Figure 4.8. It is evident that when the switch is closed, which is the case in Figure 4.28, the waveforms of V_{AC} and V_{DC} are very similar in both shape and magnitude of the waveforms of the same signals in the simulated system in Figure 4.8. For the simulated system containing the other diode rectifier, Rect1, shown in Figure C.6 the case is the same that V_{AC} and V_{DC} are very similar to the measured waveforms shown in Figure C.9. The physical implementation of Rect3 never managed to turn DC/DC1 on like the simulated version managed, shown in Figure C.7, but when the transistors are overloaded, like in Figure 4.37 V_{AC} also has a with a similar shape, but with an extra spike. The magnitude of V_{AC} and shape and magnitude of V_{DC} is also similar. The fact that all these simulations coincide so well with the measurements indicate that the shape of V_{AC} and V_{DC} here are inherit to the system configuration. The I_P needed to achieve these waveforms in the two cases is however very different. In the simulated case it is 0.7 A, and in the measured case it is 5 A. The fact that the amplitudes of V_{AC} coincide for the point where DC/DC1 turns on indicate that the simulations are correct, only that the CT model converts I_P to I_S in an incorrect manner.

There are several other shapes of V_{AC} present throughout Section 4.2. Not all the shapes are trivial to explain the reason of, but the shapes are also not really important, as the main goal of the system is to get energy out. The power, in Equation (8), contains the RMS voltage, and Equation (9) shows that the RMS voltage can be calculated for all signal shapes. As long as the rectifier can turn V_{AC} into a DC voltage, the shape of V_{AC} is not a crucial part of the system in the context of this thesis.

5.5 Refuted hypotheses

An assumption was made in the beginning of the project time that the most important factor when designing for low primary current applications would be to use components that have low thresholds for turning on. The impedance matching has turned out to actually be the most important metric. The secondary current coming from the CTs are larger than first anticipated, making the need for low threshold voltage components smaller. The input and output impedances of the different sub-systems on the other hand turned out to be much more different than first anticipated. As the power transfer is dependant on impedance matching, this has turned out to be the most important metric to consider. Unfortunately the input impedance of the DC/DCs and the secondary winding resistance of CTs are not listed in the respective datasheets, making it hard to make a decision on which component to use, without first buying the component and testing it. This also affects the initial hypothesis that the transistors used in Rect3 should have a V_{th} that should be as low as possible. since r_{ds} is dependant on V_{th}, it might be beneficial to get a lower in and output impedance of Rect3, to have transistors with higher V_{th} to get a lower r_{ds}. If transistors with higher V_{th} were used, the rectifier also might be better at handling high I_Ps, and not just stop working at I_Ps much smaller than it should.

A hypothesis was also made that there would be a need for a switch and a capacitor between the rectifier and the DC/DC, to avoid the problem of impedance matching. The capacitor can be charged with the switch open, and then the switch can close so that the accumulated charge can flow to the input of the DC/DC. This concept turned out not to work. The capacitor might have been too small to make a difference against the 300 μF capacitor on the input of DC/DC1. It was not necessary at all on the input of DC/DC2, as the equivalent input resistance in that case was already sufficiently large.

5.6 General

The best performing combination of sub-systems tested in this thesis is CT4, Rect2 and DC/DC2. This system manages to deliver $V_{Bat} = 3.3$ V to a battery at $I_P = 0.5$ A. It was stated in Section 1 that having a system that works at $I_P < 1$ A is considered to mean that the system can work most of the time, when connected to a common power cable with currents maximum reaching 16 A for 16 A fuses. The current flowing to the battery is not measured. The number of amperes flowing to the battery is not considered important here, as the intended use is sensor nodes that already consume very little power.

The main take away is that the most important aspect when designing a magnetic energy harvesting system is the impedance matching between the different sub-systems. The purpose of the EH system is to harvest energy from the magnetic fields present, and to use that energy to charge a battery. It is obvious that a high efficiency for this system is preferable to a low efficiency, even though efficiency has not been the main aspect that the system has been evaluated on. Efficiency, as defined in Equation (7), increases if P_{out} increases. According to the maximum power transfer theorem [18] P_{out} is at its highest when the impedances are matched. Impedance matching between the different sub-systems thus both improves how low I_P the system can harvest from, and the efficiency of the energy harvesting.

The commercial system LTC3331 contains an integrated DC/DC and rectifier. When tested as a combined system together with the CTs in this thesis it performs worse than when it is used as DC/DC2 and is connected to Rect1 or Rect2.

The system is not tested on $I_P >$ than 16 A, since this is a normal fuse current. There is a possibility that it would not work for I_P higher than this, but this has to be tested

if needed. Also, the system is not tested with varying I_Ps for a long period of time (like days). This would have to be done to ensure proper operation while in use in a real life context. Still, there are no indications that the system stops working after some time during all the tests conducted, so it is considered likely that the system would work for long periods of time.

It might be considered a problem that for the system to be mounted on normal household wires, the insulation of such wires would have to be removed. This is because normal wires contain two wires (or three, if there is a separate ground wire) with current going in opposite directions, something that makes the total magnetic field around them zero. To exploit the magnetic field from the AC current present, the CT must be installed on only one of the current carrying wires. It is not impossible to remove the insulation of a part of a wire to install the EH system, but it might be a high threshold for a consumer to install the system. The EH system developed might be best suited for larger buildings, like offices, universities or hospitals, where it might be desirable to put IoT sensors to monitor different parameters like humidity, temperature etc. In such cases someone can be hired to install the systems that has been trained in how to do it without harming the wires within. The system designed in this thesis then would be able to recharge the batteries of such IoT sensors, so that once installed, the sensors could be self-operating for a very long time, without the need for someone to go and change the batteries. This saves work-hours, money, and the waste from all the batteries that would otherwise have been thrown away.

6 Conclusion

A magnetic energy harvesting system is designed, simulated in LTspice and implemented using components on a breadboard. The complete EH system consists of a three sub-systems: A CT, a rectifier and a DC/DC converter. The main goal of the thesis is to make a system that can deliver $V_{Bat} = 3.3$ V to a battery, with the available I_P being under 1 A. Five different commercial CTs are tested, three different rectifiers are designed, simulated and tested and two different commercial DC/DC converters are tested. All 30 combinations of sub-systems are physically tested together to reveal the optimal combination. The best performing EH system consists of CT4, which has TR= 1:2000, Rect2, consisting of schottky diodes, and DC/DC2, that has a high input impedance. The lowest I_P that makes this sub-system configuration deliver $V_{Bat} = 3.3$ V is 0.5 A, which is 0.5 A less than the 1 A requirement. The three sub-system configuration is verified functional up to 16 A. A commercial EH system LTC3331, that consists of a combined rectifier and DC/DC, is tested as a comparison. It can work down to $I_P = 5$ A when combined with CT2 and CT4. This is a lot worse than the performance of the best sub-system configuration in this thesis. CT4 is best suited for the system. This is because is has the lowest secondary winding resistance of the two CTs with the highest number of secondary windings, with a TR of 1:2000. An assumption was made that the best suited DC/DC converter would be one that could work with as low input voltage as possible. This hypothesis is proven wrong. It is more important to match the output impedance of the rectifier and the input impedance of the DC/DC converter. If this impedance is perfectly matched, maximum efficiency is reached. DC/DC2 has an input resistance of 36 kΩ and needs more than 3 V in to work turnes out to be better suited than DC/DC1 that has a 3 Ω input resistance and that can work with a 20 mV input voltage. Rect3 is the rectifier that can work at the lowest I_P of the three rectifiers tested. It rectifies voltage down to the lowest I_P that the resolution of the current source setup allowed for, which was 80 mA. This enables the possibility of having future systems that can charge a battery almost continuously at low I_Ps, if better transistors are used. The system developed does fulfil the requirements sat, and can be used to charge batteries of sensor nodes while they are in use. It can thus help save work-hours, money and waste from potential battery replacement.

7 Future Work

To be able to use the system developed in this thesis in a real life context, some modifications would have to be conducted. The system should be implemented using something other than a breadboard and wires. Maybe a custom PCB would be fitting.

The CTs used in this thesis are commercial CTs intended for single wire power cables. Cables in normal households, and also in places like offices and public buildings are usually dual wire cables, meaning that the current is flowing in opposite directions at the same time. This means that the outermost layer of the insulation of these cables would have to be removed in order to install the CT, making it an intrusive installation. In order to avoid this a Dual Wire Current Transformer, DWCT, could be used, like the one developed by [6]. The reasons why this is not done in this thesis are mentioned in Section 2.1, and are both related to the complexity and cost of making it.

The main goal was to prove that 3.3 V could be provided from the EH-system even at low I_Ps, not to integrate the EH system with a sensor node. Control logic to turn off the EH functionality when the battery is fully charged, and on when the battery needs charging should be added to ensure proper functionality when in use over time.

An argument can be made that the worst performing rectifier in this thesis, Rect3, could become the best performing one if more fitting transistors are chosen. A future work could look into implementing it using higher threshold transistors with lower r_{ds} so as to overcome the problems this rectifier has faced in this thesis.

The DC/DC converters that have been simulated and tested here are two extremes on the scale of high input resistance vs. low threshold voltage. A future work could investigate a DC/DC converter that is a compromise of these two, to see if the performance could be further improved. When choosing a DC/DC converter, special care must be taken to make the input impedance of the DC/DC converter as similar as possible to the output impedance of the rectifier. As the currents available varies with I_P, maybe a microcontroller could be added to the system to continuously change the load resistance so as to gain maximum possible power transfer at any given time.

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Appendix A Spice Netlists

Listing 1: LTspice netlist of the circuit used to simulate the CT equivalent circuit.

```
Version 4
SHEET 1 880 784
WIRE -192 528 -304 528
WIRE 32 528 -96 528
WIRE 80 528 32 528
WIRE 208 528 160 528
WIRE -192 576 -192 528
WIRE -96 576 -96 528
WIRE 32 576 32 528
WIRE 208 576 208 528
WIRE -304 592 -304 528
WIRE -304 720 -304 672
WIRE -192 720 -192 656
WIRE -192 720 -304 720
WIRE -96 720 -96 656
WIRE 32 720 32 656
WIRE 32 720 -96 720
WIRE 208 720 208 656
WIRE 208 720 32 720
WIRE 208 752 208 720
FLAG 208 752 0
SYMBOL current -304 672 R180
WINDOW 0 24 80 Left 2
WINDOW 3 25 1 Left 2
SYMATTR InstName Ip
SYMATTR Value SINE(0 1 50)
SYMBOL ind2 -208 560 R0
WINDOW 3 37 66 Left 2
SYMATTR Value 1u
SYMATTR InstName L1
SYMBOL ind2 -80 672 R180
WINDOW 0 -29 61 Left 2
WINDOW 3 -50 32 Left 2
SYMATTR InstName L2
SYMATTR Value 1
SYMBOL res 176 512 R90
WINDOW 0 0 56 VBottom 2
WINDOW 3 32 56 VTop 2
SYMATTR InstName R3
SYMATTR Value 108
SYMBOL ind2 16 560 R0
SYMATTR InstName L3
SYMATTR Value 500m
SYMATTR SpiceLine Ipk=99m Rser=10000 Cpar=0 mfg="␣␣␣——" pn="␣␣␣——"
SYMATTR Type ind
```

```
SYMBOL res 192 560 R0
SYMATTR InstName R1
SYMATTR Value 1k
TEXT 256 480 Left 2 !.tran 60m
TEXT -352 256 Left 2 ;1/1000 TR -> 1/(1000*1000). L2=1M*L1
TEXT -216 480 Left 2 !K2 L1 L2 1
TEXT 136 264 Left 2 ;RS = 108 ohm
```

Listing 2: LTspice netlist of the circuit used to simulate Rect1.

```
SHEET 1 3100 864
WIRE 864 128 528 128
WIRE 656 208 592 208
WIRE 736 208 656 208
WIRE 864 208 864 128
WIRE 864 208 800 208
WIRE 528 224 528 128
WIRE 656 272 656 208
WIRE 864 272 864 208
WIRE 528 400 528 304
WIRE 656 400 656 336
WIRE 656 400 528 400
WIRE 736 400 656 400
WIRE 864 400 864 336
WIRE 864 400 800 400
WIRE 976 400 864 400
WIRE 1024 400 976 400
WIRE 1024 416 1024 400
WIRE 976 432 976 400
WIRE 592 528 592 208
WIRE 976 528 976 496
WIRE 976 528 592 528
WIRE 1024 528 1024 496
WIRE 1024 528 976 528
WIRE 1024 560 1024 528
FLAG 1024 560 0
FLAG 1024 400 VDC
FLAG 528 128 VAC
SYMBOL voltage 528 208 R0
WINDOW 0 -72 16 Left 2
WINDOW 3 -180 55 Left 2
SYMATTR InstName V1
SYMATTR Value SINE(0 1.45 50)
SYMATTR SpiceLine Rser=1
SYMBOL res 1008 400 R0
SYMATTR InstName RL
SYMATTR Value 12
SYMBOL cap 960 432 R0
WINDOW 0 -27 12 Left 2
WINDOW 3 -50 48 Left 2
SYMATTR InstName C1
SYMATTR Value 300u
SYMBOL diode 848 272 R0
SYMATTR InstName D1
SYMATTR Value 1N4007
SYMBOL diode 640 272 R0
SYMATTR InstName D2
```

```
SYMATTR Value 1N4007
SYMBOL diode 736 224 R270
WINDOW 0 32 32 VTop 2
WINDOW 3 0 32 VBottom 2
SYMATTR InstName D3
SYMATTR Value 1N4007
SYMBOL diode 736 416 R270
WINDOW 0 32 32 VTop 2
WINDOW 3 0 32 VBottom 2
SYMATTR InstName D4
SYMATTR Value 1N4007
TEXT 744 544 Left 2 !.tran 100ms
TEXT -208 56 Left 2 !.model 1N4007
D(IS=7.02767n RS=0.0341512 N=1.80803 EG=1.05743
XTI=5 BV=1000 IBV=5e-08 CJO=1e-11 VJ=0.7 M=0.5
FC=0.5 TT=1e-07 mfg=OnSemi type=silicon)
```

Listing 3: LTspice netlist of the circuit used to simulate Rect2.

```
SHEET 1 3100 864
WIRE 864 128 528 128
WIRE 656 208 592 208
WIRE 736 208 656 208
WIRE 864 208 864 128
WIRE 864 208 800 208
WIRE 528 224 528 128
WIRE 656 272 656 208
WIRE 864 272 864 208
WIRE 528 400 528 304
WIRE 656 400 656 336
WIRE 656 400 528 400
WIRE 736 400 656 400
WIRE 864 400 864 336
WIRE 864 400 800 400
WIRE 976 400 864 400
WIRE 1024 400 976 400
WIRE 1024 416 1024 400
WIRE 976 432 976 400
WIRE 592 528 592 208
WIRE 976 528 976 496
WIRE 976 528 592 528
WIRE 1024 528 1024 496
WIRE 1024 528 976 528
WIRE 1024 560 1024 528
FLAG 1024 560 0
SYMBOL schottky 736 384 M90
WINDOW 0 0 32 VBottom 2
WINDOW 3 32 32 VTop 2
SYMATTR InstName D3
SYMATTR Value 1N5819
SYMBOL schottky 736 192 M90
WINDOW 0 0 32 VBottom 2
WINDOW 3 32 32 VTop 2
SYMATTR InstName D4
SYMATTR Value 1N5819
SYMBOL schottky 640 272 R0
SYMATTR InstName D2
SYMATTR Value 1N5819
SYMBOL schottky 848 272 R0
SYMATTR InstName D1
SYMATTR Value 1N5819
SYMBOL voltage 528 208 R0
WINDOW 0 -72 16 Left 2
WINDOW 3 -180 55 Left 2
SYMATTR InstName V1
SYMATTR Value SINE(0 2 50)
```

```
SYMATTR SpiceLine Rser=1
SYMBOL res 1008 400 R0
SYMATTR InstName RL
SYMATTR Value 3
SYMBOL cap 960 432 R0
WINDOW 0 -27 12 Left 2
WINDOW 3 -50 48 Left 2
SYMATTR InstName C1
SYMATTR Value 300u
TEXT 744 544 Left 2 !.tran 100ms
```

Listing 4: LTspice netlist of the circuit used to simulate Rect3.

```
Version 4
SHEET 1 2556 1536
WIRE 288 208 144 208
WIRE 384 208 288 208
WIRE 640 208 384 208
WIRE 688 208 640 208
WIRE 240 288 224 288
WIRE -128 304 -272 304
WIRE -272 368 -272 304
WIRE 288 416 288 304
WIRE 432 416 432 336
WIRE 432 416 288 416
WIRE 528 416 512 416
WIRE 640 416 640 304
WIRE 640 416 528 416
WIRE 528 448 528 416
WIRE 560 448 528 448
WIRE -272 496 -272 448
WIRE -128 496 -272 496
WIRE 288 496 288 416
WIRE 560 496 560 448
WIRE 640 496 640 416
WIRE 384 512 384 208
WIRE 384 512 336 512
WIRE 688 512 688 208
WIRE 224 592 224 288
WIRE 224 592 144 592
WIRE 288 592 224 592
WIRE 592 592 592 288
WIRE 592 592 288 592
WIRE 640 592 592 592
FLAG 560 496 0
FLAG 432 336 V_dc
IOPIN 432 336 Out
FLAG 144 208 V_ac+
IOPIN 144 208 In
FLAG 144 592 V_ac-
IOPIN 144 592 In
FLAG -128 304 V_ac+
IOPIN -128 304 Out
FLAG -128 496 V_ac-
IOPIN -128 496 Out
FLAG 432 480 0
SYMBOL nmos 592 208 R0
WINDOW 3 2 -31 Left 2
SYMATTR Value 2SK134C
SYMATTR InstName M1
SYMBOL nmos 688 592 R180
```

```
WINDOW 3 -38 -22 Left 2
SYMATTR Value 2SK134C
SYMATTR InstName M2
SYMBOL pmos 240 208 R0
SYMATTR InstName M3
SYMATTR Value 2SJ49C
SYMBOL pmos 336 592 R180
WINDOW 3 -92 25 Left 2
SYMATTR Value 2SJ49C
SYMATTR InstName M4
SYMBOL cap 416 416 R0
SYMATTR InstName C1
SYMATTR Value 300u
SYMBOL res 528 400 R90
WINDOW 0 0 56 VBottom 2
WINDOW 3 32 56 VTop 2
SYMATTR InstName R1
SYMATTR Value 3
SYMBOL voltage -272 352 R0
SYMATTR InstName V1
SYMATTR Value SINE(0 2 50)
TEXT 392 664 Left 2 !.tran 100m
TEXT -984 -64 Left 2 !.model 2SK134C VDMOS(nchan
Vto=0.02 Kp=0.85 Lambda=0.02 Rs=0.62 Rd=500 Rds=1e7
Cgdmax=100p Cgdmin=5p a=0.25 Cgs=600p Cjo=1080p m=0.7
VJ=2.5 IS=4.0E-06 N=2.4)
TEXT -976 8 Left 2 !.model 2SJ49C VDMOS(pchan Vto=-0.02
Kp=0.6 Lambda=0.1 Rs=0.55 Rd=1.1k Rds=1e7 Cgdmax=215p
Cgdmin=10p a=0.25 Cgs=900p Cjo=1200p m=0.7 VJ=2.5
IS=4.0E-06 N=2.4)
TEXT -968 -96 Left 2 ;NMOS
TEXT -968 -16 Left 2 ;PMOS
```

Listing 5: LTspice netlist of the circuit used to simulate DC/DC1: LTC3108.

```
Version 4
SHEET 1 2556 864
WIRE 2272 112 2048 112
WIRE 2400 112 2272 112
WIRE 2272 192 2272 112
WIRE 2272 192 2192 192
WIRE 2432 192 2272 192
WIRE 1072 240 928 240
WIRE 1392 240 1328 240
WIRE 1520 240 1456 240
WIRE 2048 240 2048 112
WIRE 2048 240 1776 240
WIRE 2432 256 2432 192
WIRE 1328 288 1328 240
WIRE 1328 288 1168 288
WIRE 2192 288 2192 192
WIRE 1072 304 1072 240
WIRE 1168 304 1168 288
WIRE 1328 336 1328 288
WIRE 1360 336 1328 336
WIRE 1376 336 1360 336
WIRE 1472 336 1440 336
WIRE 1520 336 1472 336
WIRE 1984 336 1776 336
WIRE 2192 368 2192 352
WIRE 2432 368 2432 336
WIRE 720 384 688 384
WIRE 1024 384 720 384
WIRE 1072 384 1024 384
WIRE 1200 384 1168 384
WIRE 1200 416 1200 384
WIRE 1360 416 1360 336
WIRE 1376 416 1360 416
WIRE 1472 416 1472 336
WIRE 1472 416 1456 416
WIRE 688 432 688 384
WIRE 1520 432 1504 432
WIRE 2336 432 1776 432
WIRE 2448 432 2336 432
WIRE 2336 448 2336 432
WIRE 928 496 928 240
WIRE 1504 496 1504 432
WIRE 1504 496 928 496
WIRE 1520 528 1408 528
WIRE 2304 528 1776 528
WIRE 2304 592 2304 528
WIRE 2352 592 2304 592
WIRE 1520 624 1104 624
```

```
WIRE 2096 624 1776 624
WIRE 2144 624 2096 624
WIRE 1104 656 1104 624
WIRE 1408 720 1408 528
WIRE 1520 720 1408 720
WIRE 1984 720 1776 720
WIRE 1648 848 1648 768
FLAG 1648 848 0
FLAG 1984 720 PGD
IOPIN 1984 720 Out
FLAG 2144 624 VLDO
IOPIN 2144 624 Out
FLAG 2096 688 0
FLAG 1408 784 0
FLAG 2336 512 0
FLAG 2352 592 VOUT2
IOPIN 2352 592 Out
FLAG 2448 432 VOUT
IOPIN 2448 432 Out
FLAG 2400 112 VSTORE
IOPIN 2400 112 Out
FLAG 2432 368 0
FLAG 1984 336 VOUT2
IOPIN 1984 336 In
FLAG 1104 656 0
FLAG 2192 368 0
FLAG 1200 416 0
FLAG 1024 448 0
FLAG 688 512 0
FLAG 720 384 Vin
SYMBOL PowerProducts/LTC3108 1648 480 R0
SYMATTR InstName U1
SYMBOL cap 2080 624 R0
WINDOW 0 44 28 Left 2
WINDOW 3 44 56 Left 2
SYMATTR InstName C2
SYMATTR Value 2.2u
SYMBOL cap 2320 448 R0
WINDOW 0 -43 6 Left 2
WINDOW 3 -54 29 Left 2
SYMATTR InstName C3
SYMATTR Value 0.1u
SYMBOL cap 1392 720 R0
SYMATTR InstName C4
SYMATTR Value 1u
SYMBOL res 2448 352 R180
WINDOW 0 36 76 Left 2
WINDOW 3 36 40 Left 2
SYMATTR InstName R2
SYMATTR Value 100
```

```
SYMBOL polcap 2176 288 R0
SYMATTR InstName C5
SYMATTR Value 220u
SYMBOL res 1360 432 R270
WINDOW 0 -23 15 VTop 2
WINDOW 3 5 64 VBottom 2
SYMATTR InstName R3
SYMATTR Value 499k
SYMBOL cap 1440 320 R90
WINDOW 0 0 32 VBottom 2
WINDOW 3 32 32 VTop 2
SYMATTR InstName C6
SYMATTR Value 330p
SYMBOL cap 1456 224 R90
WINDOW 0 0 32 VBottom 2
WINDOW 3 32 32 VTop 2
SYMATTR InstName C7
SYMATTR Value 1n
SYMBOL ind2 1184 400 R180
WINDOW 0 -25 67 Left 2
WINDOW 3 -86 39 Left 2
SYMATTR InstName L1
SYMATTR Value 75m
SYMATTR SpiceLine Rser=13.7
SYMBOL ind2 1056 288 R0
SYMATTR InstName L2
SYMATTR Value 7.5u
SYMATTR SpiceLine Rser=0.74
SYMBOL polcap 1008 384 R0
WINDOW 0 40 26 Left 2
WINDOW 3 39 54 Left 2
SYMATTR InstName C8
SYMATTR Value 330u
SYMBOL voltage 688 416 R0
SYMATTR InstName V1
SYMATTR Value 150m
TEXT 1808 832 Left 2 !.tran 50ms
TEXT 1112 256 Left 2 !K1 L1 L2 0.95
```

Listing 6: LTspice netlist of the circuit used to simulate DC/DC2: LTC3331.

```
Version 4
SHEET 1 1992 1344
WIRE 352 -368 240 -368
WIRE 368 -368 352 -368
WIRE 208 -208 208 -240
WIRE 240 -208 240 -368
WIRE 240 -208 208 -208
WIRE 496 -208 496 -240
WIRE 544 -208 496 -208
WIRE 592 -208 592 -240
WIRE 640 -208 592 -208
WIRE 688 -208 688 -240
WIRE 736 -208 688 -208
WIRE 784 -208 784 -240
WIRE 832 -208 784 -208
WIRE 304 -192 304 -240
WIRE 352 -192 352 -368
WIRE 352 -192 304 -192
WIRE 544 -192 544 -208
WIRE 640 -192 640 -208
WIRE 736 -192 736 -208
WIRE 832 -192 832 -208
WIRE 112 -160 112 -240
WIRE 208 -160 208 -208
WIRE 304 -160 304 -192
WIRE 400 -160 400 -240
WIRE 496 -160 496 -208
WIRE 592 -160 592 -208
WIRE 688 -160 688 -208
WIRE 784 -160 784 -208
WIRE 48 -96 -272 -96
WIRE 928 -96 848 -96
WIRE 1248 -96 1008 -96
WIRE 48 0 -272 0
WIRE 944 0 848 0
WIRE 1152 0 1024 0
WIRE 1248 80 1248 -96
WIRE 1296 80 1248 80
WIRE 1376 80 1296 80
WIRE -448 96 -464 96
WIRE -368 96 -448 96
WIRE -304 96 -368 96
WIRE 48 96 -304 96
WIRE 1152 96 1152 0
WIRE 1152 96 848 96
WIRE 1376 96 1376 80
WIRE 1376 160 1376 96
WIRE -448 176 -448 96
```

```
WIRE −304 192 −304 96
WIRE −208 192 −304 192
WIRE 48 192 −144 192
WIRE 1248 192 1248 80
WIRE 1248 192 848 192
WIRE 1376 256 1376 224
WIRE −224 288 −304 288
WIRE 16 288 −160 288
WIRE 48 288 16 288
WIRE 1264 288 848 288
WIRE 1520 288 1264 288
WIRE 1824 288 1520 288
WIRE 1888 288 1824 288
WIRE −448 304 −448 240
WIRE −304 336 −304 288
WIRE 16 336 16 288
WIRE 16 336 −48 336
WIRE 1824 336 1824 288
WIRE 1264 352 1264 288
WIRE 1312 352 1264 352
WIRE 1424 352 1392 352
WIRE 1504 352 1488 352
WIRE 1520 352 1504 352
WIRE 0 384 −464 384
WIRE 48 384 0 384
WIRE 1232 384 848 384
WIRE 1504 416 1504 352
WIRE 1504 416 1488 416
WIRE 1536 416 1504 416
WIRE 1648 416 1616 416
WIRE 1744 416 1712 416
WIRE −144 432 −192 432
WIRE 0 432 0 384
WIRE 0 432 −64 432
WIRE 1120 464 896 464
WIRE 1232 464 1232 384
WIRE 1488 464 1488 416
WIRE 1488 464 1232 464
WIRE 1824 464 1824 400
WIRE 1824 464 1488 464
WIRE 1856 464 1824 464
WIRE −224 480 −480 480
WIRE −192 480 −192 432
WIRE −192 480 −224 480
WIRE 0 480 −192 480
WIRE 48 480 0 480
WIRE 896 480 896 464
WIRE 896 480 848 480
WIRE 992 512 880 512
WIRE −224 544 −224 480
```

```
WIRE −480 560 −480 480
WIRE −480 560 −544 560
WIRE 0 576 0 480
WIRE 0 576 −96 576
WIRE 48 576 0 576
WIRE 880 576 880 512
WIRE 880 576 848 576
WIRE 944 576 880 576
WIRE −224 640 −224 608
WIRE 1008 640 1008 576
WIRE 128 672 128 640
WIRE 128 672 −160 672
WIRE 784 672 784 640
WIRE 784 672 400 672
WIRE 64 720 −112 720
WIRE 208 720 208 640
WIRE 208 720 64 720
WIRE 448 720 448 640
WIRE 64 752 64 720
WIRE 64 752 −48 752
WIRE 288 752 288 640
WIRE 288 752 64 752
WIRE 64 768 64 752
WIRE 64 768 16 768
WIRE 368 768 368 640
WIRE 368 768 64 768
WIRE −160 800 −160 672
WIRE −112 800 −112 720
WIRE −48 800 −48 752
WIRE 16 800 16 768
WIRE 64 816 64 768
WIRE 528 848 528 640
WIRE 608 848 608 640
WIRE 688 848 688 640
WIRE 288 1120 160 1120
WIRE 400 1120 400 672
WIRE 400 1120 288 1120
FLAG 448 720 0
FLAG −464 96 VIN
IOPIN −464 96 In
FLAG −304 336 0
FLAG −448 304 0
FLAG 1008 640 0
FLAG −48 336 VIN2
IOPIN −48 336 Out
FLAG 992 512 VIN3
IOPIN 992 512 Out
FLAG −96 576 BB_IN
IOPIN −96 576 In
FLAG −224 640 0
```

```
FLAG −464 384 CHARGE
IOPIN −464 384 In
FLAG −544 560 JP12
IOPIN −544 560 In
FLAG −272 −96 AC1
IOPIN −272 −96 In
FLAG −272 0 AC2
IOPIN −272 0 In
FLAG 1120 464 EH_ON
IOPIN 1120 464 Out
FLAG 112 −240 PG_OUT
IOPIN 112 −240 Out
FLAG 1376 256 0
FLAG 1888 288 SCAP
IOPIN 1888 288 In
FLAG 1856 464 BAL
IOPIN 1856 464 In
FLAG 1744 416 0
FLAG 688 848 VIN3
IOPIN 688 848 In
FLAG 160 1120 BAT_IN
IOPIN 160 1120 In
FLAG 208 −240 JP7
IOPIN 208 −240 In
FLAG 304 −240 JP6
IOPIN 304 −240 In
FLAG 400 −240 VIN3
IOPIN 400 −240 In
FLAG 496 −240 JP10
IOPIN 496 −240 In
FLAG 592 −240 JP9
IOPIN 592 −240 In
FLAG 688 −240 JP8
IOPIN 688 −240 In
FLAG 784 −240 JP11
IOPIN 784 −240 In
FLAG −160 800 VIN2
IOPIN −160 800 In
FLAG −112 800 JP3
IOPIN −112 800 In
FLAG −48 800 JP2
IOPIN −48 800 In
FLAG 16 800 JP1
IOPIN 16 800 In
FLAG 64 816 0
FLAG 368 −368 0
FLAG 608 848 0
FLAG 528 848 0
FLAG 736 −192 0
FLAG 544 −192 0
```

```
FLAG 640 -192 0
FLAG 832 -192 0
FLAG 1312 896 0
FLAG 1312 816 AC3
IOPIN 1312 816 Out
FLAG 288 1200 0
FLAG -368 176 0
FLAG 1376 96 VOUT
IOPIN 1376 96 In
FLAG 1296 160 0
SYMBOL PowerProducts/LTC3331 448 240 R0
SYMATTR InstName U1
SYMBOL cap -144 176 R90
WINDOW 0 0 32 VBottom 2
WINDOW 3 32 32 VTop 2
SYMATTR InstName C1
SYMATTR Value 1u
SYMBOL cap -464 176 R0
SYMATTR InstName C2
SYMATTR Value 22u
SYMBOL cap -160 272 R90
WINDOW 0 0 32 VBottom 2
WINDOW 3 32 32 VTop 2
SYMATTR InstName C3
SYMATTR Value 4.7u
SYMBOL cap 1008 560 R90
WINDOW 0 0 32 VBottom 2
WINDOW 3 32 32 VTop 2
SYMATTR InstName C4
SYMATTR Value 0.1u
SYMBOL cap -240 544 R0
SYMATTR InstName C5
SYMATTR Value 22u
SYMBOL ind 928 16 R270
WINDOW 0 32 56 VTop 2
WINDOW 3 5 56 VBottom 2
SYMATTR InstName L1
SYMATTR Value 100u
SYMBOL ind 912 -80 R270
WINDOW 0 32 56 VTop 2
WINDOW 3 5 56 VBottom 2
SYMATTR InstName L2
SYMATTR Value 22u
SYMBOL cap 1360 160 R0
SYMATTR InstName C6
SYMATTR Value 150u
SYMBOL res 1408 336 R90
WINDOW 0 0 56 VBottom 2
WINDOW 3 32 56 VTop 2
SYMATTR InstName R2
```

```
SYMATTR Value 7.5k
SYMBOL cap 1488 336 R90
WINDOW 0 0 32 VBottom 2
WINDOW 3 32 32 VTop 2
SYMATTR InstName C7
SYMATTR Value 0.1u
SYMBOL cap 1504 288 R0
SYMATTR InstName C8
SYMATTR Value 90m
SYMBOL res 1632 400 R90
WINDOW 0 0 56 VBottom 2
WINDOW 3 32 56 VTop 2
SYMATTR InstName R3
SYMATTR Value 7.5k
SYMBOL cap 1712 400 R90
WINDOW 0 0 32 VBottom 2
WINDOW 3 32 32 VTop 2
SYMATTR InstName C9
SYMATTR Value 0.1u
SYMBOL cap 1808 336 R0
SYMATTR InstName C10
SYMATTR Value 330m
SYMBOL res -48 416 R90
WINDOW 0 0 56 VBottom 2
WINDOW 3 32 56 VTop 2
SYMATTR InstName R4
SYMATTR Value 3.01k
SYMBOL voltage 1312 800 R0
SYMATTR InstName V1
SYMATTR Value SINE(0 0 50)
SYMBOL voltage 288 1104 R0
SYMATTR InstName V2
SYMATTR Value 3.3
SYMATTR SpiceLine Rser=9999999
SYMBOL voltage -368 80 R0
SYMATTR InstName V3
SYMATTR Value 7.5
SYMBOL res 1280 64 R0
SYMATTR InstName R1
SYMATTR Value 355
TEXT 896 -296 Left 2 ;To have the output Vout be 3.3V,
the following must be set: \nOU2=1, OUT1=0, OUT0=0.
TEXT -680 928 Left 2 ;UVLO falling edge must be higher
than Vout level. \nTo achieve this, UV0 must be tied to Vin2,
while the rest are connected to ground.
TEXT -576 -152 Left 2 ;AC input (like piezo or magnet).
AC2 used if differential
TEXT 936 960 Left 2 !.tran 200ms
```

Appendix B List of equipment and components used

Table 6: List of equipment used in implementation

Equipment	**Name**
Oscilloscope	DIGILENT Analog Discovery 2
Oscilloscope	Agilent Technologies MSO9254A
Clamp Ammeter	UNI-T UT203
Multimeter	Sparkfun VC830L
Breadboard	Standard
Variac	unknown
Big CT	TOREMA VÄXJÖ SWEDEN Transf. No. 7344
Wires	Various

Table 7: List of components used in implementation

Component	**Name**
Silicon diodes	1N4007
Schottky diodes	1N5819
PMOS	ALD310700
NMOS	ALD110800
Resistors	Various
Capacitors	Various
Push button	standard
CT0	TCC176
CT1	SCT006, 1:1000
CT2	SCT006, 1:2000
CT3	XHSCT-T-10
CT4	AKH_0.66 K-Ø10
DC/DC1	LTC3108
DC/DC1 Evaluation board	DC1582B
DC/DC2 & EH circuit	LTC3331
DC/DC2 & EH Evaluation board	DC1582B

Table 8: List of Software used

Software	**Purpose**
LTspice XVII	Circuit simulation
Waveforms 2015	Testing of circuits
Matlab R2016a	Post processing and plotting

Appendix C Additional Figures

Figure C.1 shows the signals V_{AC} in green and V_{DC} in blue for Rect2. V_{AC} is set to have 50 Hz and a 2 V amplitude. The load of the circuit is set to be 12 Ω and 300 μF. This results in the output signal V_{DC} having an average value of about 805 mV. This is almost 3 times higher than the corresponding signal for Rect1.

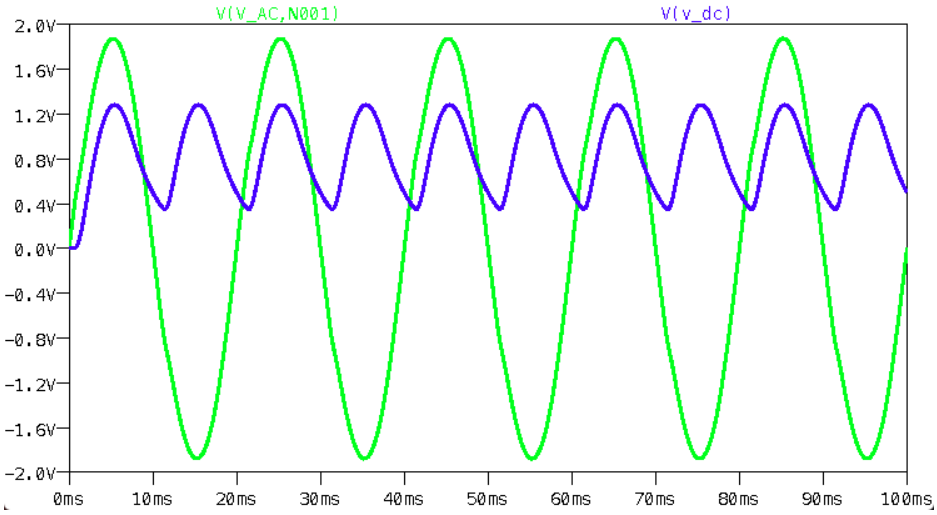

Figure C.1: V_{AC} in green, and V_{DC} in blue for Rect2, with a load of 12 Ω and 300 μF.V_{AC} has a 2 V amplitude, and a frequency of 50 Hz.

Rect3 is simulated with a load of 12 Ω and 300 μF. The resulting waveforms of V_{AC} and V_{DC} for Rect3 are shown in Figure C.2. V_{AC} is shown in green, and is set to have an amplitude of 2 V and a frequency of 50 Hz. The resulting V_{DC} is shown in blue, and has an average value of 480 mV, which is between the corresponding values for Rect1 and Rect2.

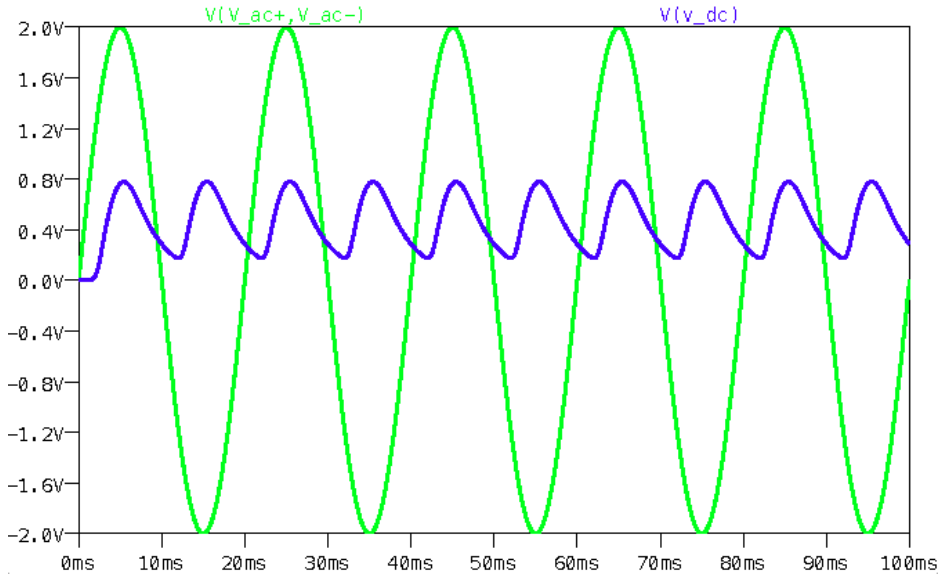

Figure C.2: Waveform of V_{AC} (green) and V_{DC} (blue) for Rect3. V_{AC} has a 2 V amplitude, and a frequency of 50 Hz. The load is 12 Ω and 300 μF.

Figure C.3 shows the simulated waveform of V_{AC} (green) and V_{DC} (blue) for Rect1 with 2V sinusoidal signal in and 36 kΩ and 22 μF load.

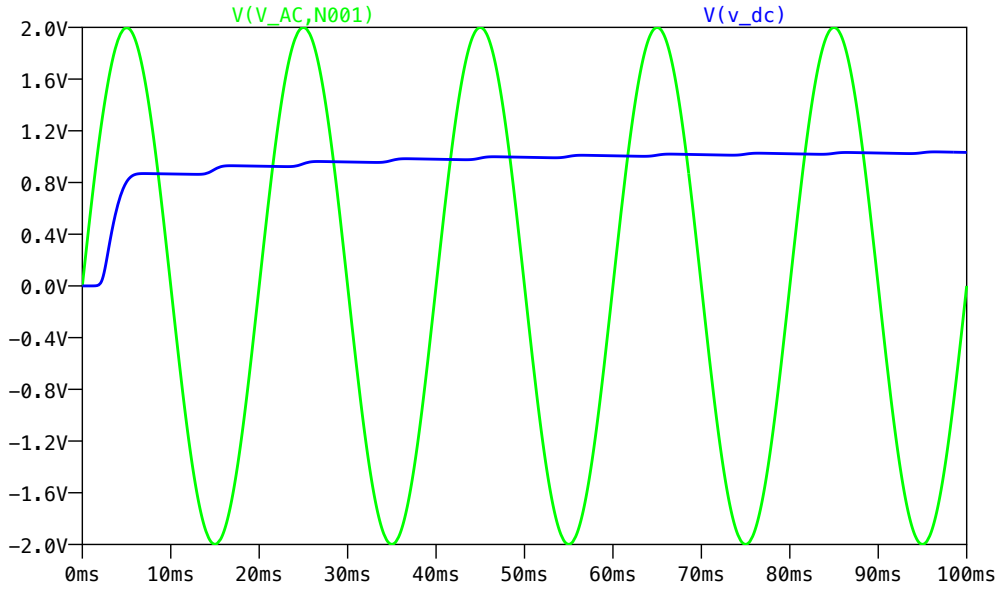

Figure C.3: Waveform of V_{AC} (green) and V_{DC} (blue) for Rect1. V_{AC} has a 2 V amplitude, and a frequency of 50 Hz. The load is 36 kΩ and 22 μF.

Figure C.4 shows the Simulated waveform of V_{AC} (green) and V_{DC} (blue) for Rect3 with 2V sinusoidal signal in and 36 kΩ and 22 μF load.

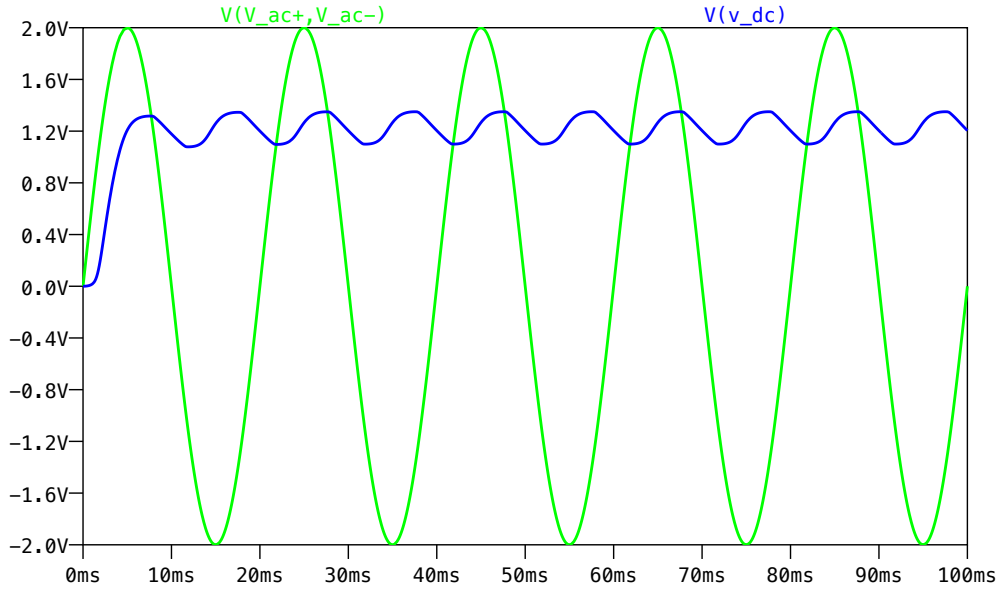

Figure C.4: Waveform of V_{AC} (green) and V_{DC} (blue) for Rect3. V_{AC} has a 2 V amplitude, and a frequency of 50 Hz. The load is 36 kΩ and 22 μF.

Figure C.5 shows the simulated V_{DC} versus V_{AC} for the rectifiers Rect1, Rect2 and Rect3 simulated with 12 Ω and 300 μF as a load.

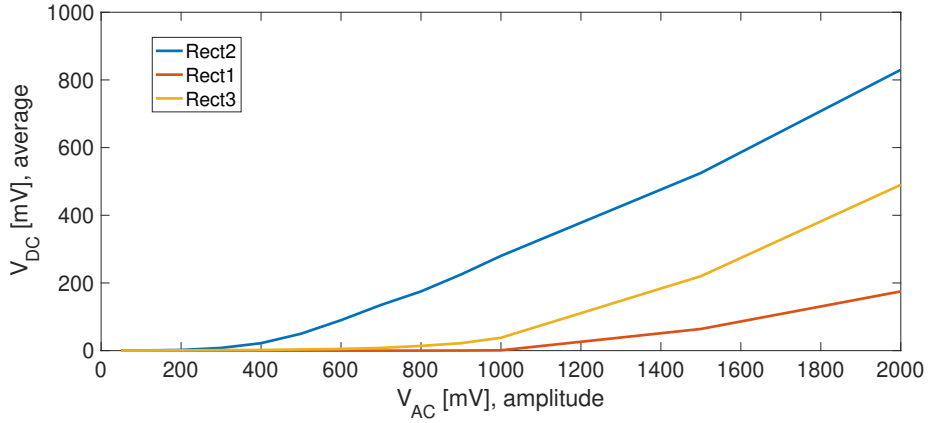

Figure C.5: V_{DC} versus V_{AC} for the rectifiers Rect1, Rect2 and Rect3 simulated with 12 Ω and 300 μF as a load.

The complete energy harvesting system is simulated with Rect1. The transient of this

simulation is shown in Figure C.6. In this figure, V_{AC} (green) has an amplitude of about 1.5 V, the signal V_{DC} has an average value of about 29 mV and the signal V_{Bat} reaches 3.3 V after 76 ms. At a little before 20 ms, the same effect as shown in Figure 4.3 is evident. As the DC/DC1 turns on, its input impedance changes, which affects V_{AC} by forcing it lower because of the lower resistance.

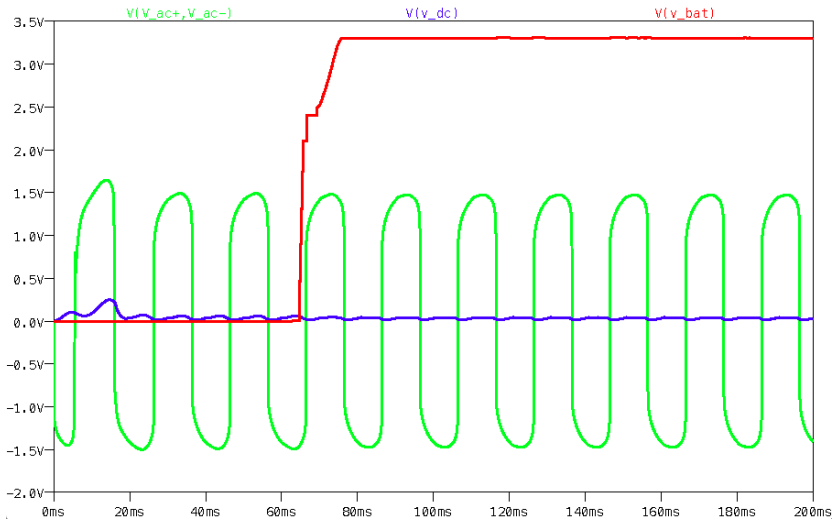

Figure C.6: The simulated transient plot of the signals V_{AC} (green), V_{DC} (blue) and V_{Bat} (red). This is for a complete system with a CT model, Rect1 and DC/DC1. The input to the system is $I_P = 1.5$ A

Figure C.7 shows a transient plot of the entire energy harvesting system with a CT model, Rect3 and DC/DC1. The input to the model is a signal I_P that is set to have an amplitude of 0.7 A and a frequency of 50 Hz. The figure shows that this makes the signal V_{AC} (green) have an amplitude of about 1.2 V, the signal V_{DC} have an average value of about 25 mV and the signal V_{Bat} reaching 3.3 V after 132 ms.

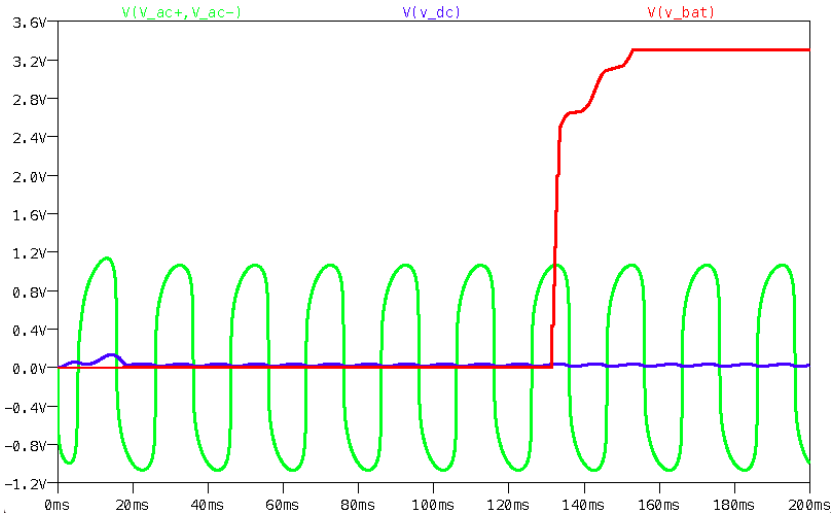

Figure C.7: A transient plot showing the signals V_{AC} (green), V_{DC} (blue) and V_{Bat} (red). This is for a complete system with a CT model, Rect3 and DC/DC1. The input I_P is set to be 700 mA.

Figure C.8 shows V_{AC} versus I_P for CT1-CT4.

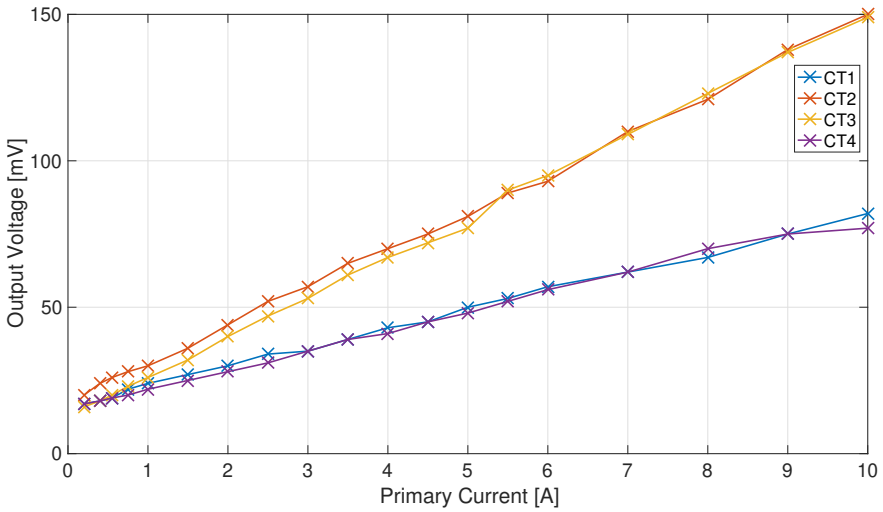

Figure C.8: Output voltage vs primary current for CT1-CT4. The load resistance was kept constant at 10 Ω.

Figure C.9 shows a waveform of V_{AC} (blue) and V_{DC} (orange). This measurement is done on a system consisting of CT2, Rect1, and DC/DC1. In this case $I_P = 8$ A. The lowest I_P that managed to deliver $V_{Bat} = 3.3$ V for Rect1 was 7 A.

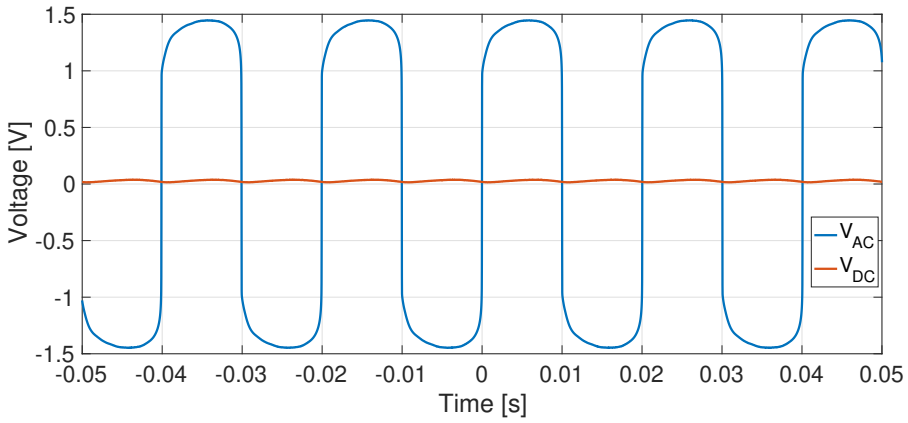

Figure C.9: Measured V_{AC} (blue) and V_{DC} (orange). Measurements done on a system consisting of CT2, Rect1. $I_P = 7$ A.and DC/DC1.

Figure C.10 and Figure C.11 show the EH system working at $I_P = 16$ A. Figure C.10 shows V_{AC} (blue) and V_{DC} (orange) produced by the combination of CT4, Rect1 and DC/DC2. Figure C.11 shows V_{AC} (blue) and V_{DC} (orange) produced by the combination of CT1, Rect2 and DC/DC2.

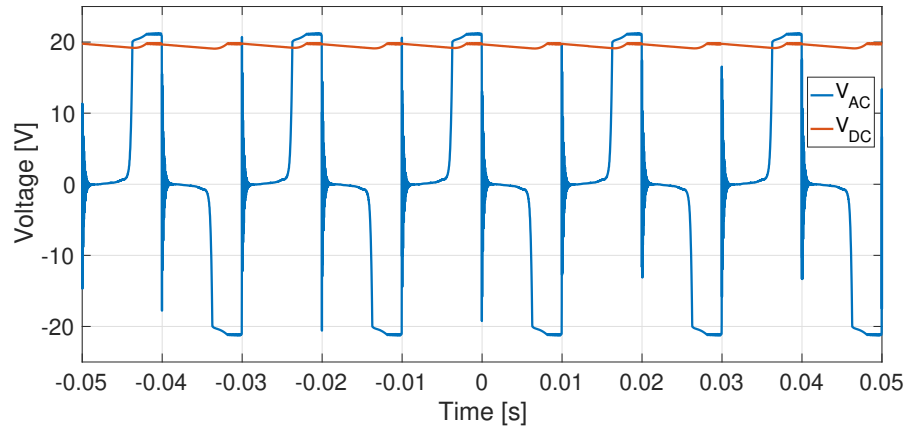

Figure C.10: Waveform showing V_{AC} (blue) and V_{DC} (orange) produced by the combination of CT4, Rect1 and DC/DC2 with $I_P = 16$ A.

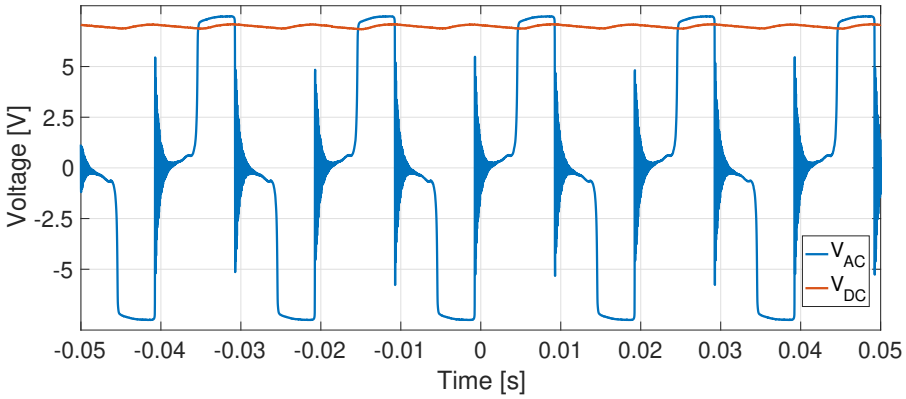

Figure C.11: Waveform showing V_{AC} (blue) and V_{DC} (orange) produced by the combination of CT1, Rect2 and DC/DC2 with $I_P = 16$ A.

Solveig Skavnes

Design and Implementation of a Magnetic Energy Harvesting System

NTNU
Norwegian University of
Science and Technology