Master's thesis

NTNU
Norwegian University of Science and Technology
Faculty of Information Technology and Electrical Engineering
Department of Electric Power Engineering

Thomas Mickelborg

Detection and Protection strategy for a modular HVDC generator

Master's thesis in Energy and the Environment
Supervisor: Pål Keim Olsen
Co-supervisor: Bruce Andrew Mork
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Summary

As an increased portion of the worlds electricity production is being produced by Renewable Energy Sources (RES), an alternative for power distribution over long distances called super grids is proposed by the EU. These are based on high voltage direct current (HVDC) and allows for higher volumes of RES to be transported across large distances. This thesis considers a new concept based on a modular HVDC (ModHVDC) generator that proposes a transformer-less concept with one single conversion step to achieve 100 kV HVDC on the output. This technology aim to be a solution to one of the main innovation gaps in regards to offshore wind power, which is to drive down costs and lower risk related to transmission and distribution of electricity.

This thesis specifically aim to fill some of the knowledge gaps within the field of faults and protection regarding this new concept. The segmented machine introduces some new failure modes that needs to be investigated before a commercial product can be achieved. There is little to no known literature on this topic and thus three predefined research objectives was chosen as a starting point. A simulation model is made in the Simulink environment that models the modHVDC generator with multiple stator segments and corresponding converter modules. Based on the model and circuit analysis, a fault analysis of module-to-module and module-to-ground faults are conducted to investigate the severity of these faults. An overview of the different faults that can occur for this machine and an initial protection strategy is presented. As a part of the protection strategy a bypass solution is proposed for isolating faulty modules and achieve redundant operation.

Due to its simple structure, the simulation model utilizes a designated two-level voltage source topology for each stator segment. However, this topology is vulnerable to DC faults which poses the question of which converter topology that is best suitable for this concept. A literature review is conducted to get an overview of different MMC topologies with focus on their fault handling capabilities. In addition some new experimental methods for achieving DC-fault handling capabilities are described. Although these topologies are not implemented as a part of the simulation model, they act as suggestions for further research.

The proposed protection strategy provides an initial solution based on the investigated failure modes. As there is additional failure modes that needs investigation, the proposal must be seen as an suggestion for further work. However, the results illustrates the need for a current limiting reactor to limit fault current for the applied RLC parameters. Although at the expense of faster voltage rise time on the affected DC-links. This supports the suggestion of applying a fast acting solid state switch in the bypass in order to mitigate the heat dissipation. The results also supports the proposed use of fuses or breakers on the floating DC voltage connections, as this has a considerable and positive impact on bypass heat dissipation.

Sammendrag

Ettersom en økt del av verdens elektrisitetsproduksjon produseres av fornybare energikilder (RES), et nytt alternativ for kraftdistribusjon over lange avstander kalt supernett er foreslått av EU. Disse er basert på likestrøm med med høye spenningsnivåer (HVDC) og gjør det mulig å transportere høyere volum av RES over store avstander. Denne oppgaven vurderer et nytt konsept basert på en modulær HVDC (ModHVDC) generator som foreslår et transformatorfritt konsept med ett enkelt konverteringstrinn for å oppnå 100 kV på utgangen. Denne teknologien tar sikte på å være en løsning på et av de viktigste innovasjonshullene når det gjelder offshore vindkraft, som er å redusere kostnadene og redusere risikoen knyttet til overføring og distribusjon av elektrisitet.

Denne oppgaven tar spesielt sikte på å fylle noen av kunnskapshullene innen feil og beskyttelse med hensyn til dette nye konseptet. Den segmenterte maskinen introduserer noen nye feilsituasjoner som må undersøkes grundig før et kommersielt produkt kan oppnås. Det er lite eller ingen kjent litteratur om dette emnet, og tre valgte forskningsmål ble derfor valgt som utgangspunkt. En simuleringsmodell er laget i Simulink som modellerer modHVDC-generatoren med flere statorsegmenter og tilhørende omformermoduler. Basert på modell- og kretsanalyse blir det utført en feilanalyse av modul-til-modul- og modul-til-jord-feil for å undersøke alvorlighetsgraden av disse feilene. En oversikt over de forskjellige feilene som kan oppstå for denne maskinen og en innledende beskyttelsesstrategi presenteres. Som en del av beskyttelsesstrategien foreslås en bypass-løsning som et alternativ for å isolere defekte moduler og dermed oppnå videre drift av resterende moduler.

På grunn av sin enkle struktur bruker simuleringsmodellen en enkel to-nivå omformer topologi (2L-VSC) for hvert statorsegment. Imidlertid er denne topologien sårbar for DC-feil som stiller spørsmålet om hvilken omformertopologi som er best egnet for dette konseptet. En litteraturstudiet er gjort for å få en oversikt over forskjellige MMC-topologier med fokus på deres evne til å håndtere feil. I tillegg er noen nye eksperimentelle metoder for å oppnå håndtering av DC-feil beskrevet. Selv om disse topologiene ikke er implementert som en del av simuleringsmodellen, fungerer de som forslag til videre forskning.

Den foreslåtte strategien gir en innledende løsning basert på de undersøkte feilmodusene. Siden det er flere feil situasjoner som må utforskes, må forslaget sees på som et forslag til videre arbeid. Resultatene illustrerer imidlertid behovet for en strømbegrensende reaktor for å begrense feilstrøm for de anvendte RLC-parametrene. Skjønt på bekostning av raskere spenningsøkning på berørte DC-koblinger. Dette støtter forslaget om å bruke en hurtigvirkende solid state-bryter i bypass for å redusere varmetapet. Resultatene støtter også den foreslåtte bruken av sikringer eller brytere på de flytende DC-spenningstilkoblingene, da dette har en betydelig og positiv innvirkning på varmetap i bypass resistoren.

Preface

This master thesis concludes my five year long journey in academia. It is an accomplishment which ranks high, and I am very proud to have completed this journey. However, I would not have succeeded without the friends I've made during this period. There have been many highs and lows but in the end I have learned a lot about myself and I'm looking forward to an exciting career in the years to come.

I wish to thank my main supervisor Pål Keim Olsen for providing an interesting topic for my thesis and for being available for rewarding discussions and valuable help undergoing this project. I also wish to thank my co-supervisor Bruce Mork for providing insight to the protection aspect, which is a topic I had little experience with beforehand.

Trondheim, June 14th 2021

Thomas Mickelborg

Abbreviations

IGBT	Insulated Gate Bipolar Transistor
DCCB	Direct Current Circuit Breaker
VSC	Voltage Source Converter
PWM	Pulse Width Modulation
2L-VSC	Two-level Voltage Source Converter
HVDC	High Voltage Direct Current
PMSG	Permanent Magnet Synchronous Generator
ModHVDC	Modular High Voltage Direct Current
VSC	Voltage Source Converter
ODE	Ordinary Differential Equations
RES	Renewable Energy Sources
KCL	Kirchoff's Current Law
KVL	Kirchoff's Voltage Law
IEA	International Energy Agency
MMC	Modular Multilevel Converter
SM	Sub-module
PLL	Phase-Locked-Loop
ESR	Equivalent Series Resistance
FEM	Finite Element Method

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Chapter 1

Introduction

This section aim to provide context to a new and innovative concept based on a modular HVDC generator called modHVDC. The concept could contribute as a solution to some of the innovation gaps when it comes to offshore wind power, which is further elaborated on. The research objectives and questions that will provide the basis for this master thesis are presented. As this thesis is an extension of the specialization project conducted in the previous semester, the background and concept description is the same.

1.1 Background

More and more of the worlds electricity production is being produced by renewable energy sources (RES). In order to facilitate for a further increase in low-carbon energy production, an alternative for power distribution over long distances is proposed by EU. These are called super grids and are meant to interconnect various countries and regions with high voltage DC current. This transmission network would make it possible to trade high volumes of RES across great distances. If HVDC can be achieved on the generator output, economical benefits are introduced as the transformation steps from AC to DC current can be avoided. As fewer transformation steps are introduced, lower investment costs can be achieved. [1–3]

Offshore wind power is one of the renewable technologies that are forecasted to have a significant growth in the coming years and decades. In 2019, the potential for offshore wind power was found to have the potential of generating 18 times the global electricity demand. One of the main innovation gaps with respect to offshore wind power is according to the International Energy Agency (IEA), further cost reduction and lower risk of transmission and distribution of electricity. [4] For offshore applications, AC transmission is not feasible due to the high transmission losses. When the distance is greater than 400–700 km on land, and 50–60 km at sea, DC transmission is cheaper than AC transmission. [5, 6] HVDC generators combined with the above mentioned super grid can be a part of the solution, addressing this innovation gap. However, the concept is in an early stage of development and further research is needed before full-scale version can be realized. [3]

1.2 ModHVDC generator concept

The modHVDC concept introduces a new generator design that proposes a transformerless permanent magnet synchronous machine (PMSG), with one single conversion stage. High voltage DC current is achieved by stacking the converter voltages instead of the generator coil group voltages. By doing this, the need for step-up/down transformers can be eliminated. The overall goal of the project is to see if modular HVDC generators are able to provide a cost-saving and up-scalable DC based solution for RES production. In order to achieve this goal, thorough research in regards to faults and protection are required. [1, 3]

The concept proposes a stator that is divided into segments, and each of these segments are connected to the DC potential of dedicated converters (1M-4M) See Figure 1.2.2. By having a segmented stator with galvanic connection to the converter DC potential, the AC and DC voltage stresses are separated. This leads to a more optimal distribution of voltage stress. As a consequence, the Power-to-weight ratio can be increased compared to state-of-the art machines with the same voltage rating. [1, 3] Figure 1.2.1 illustrates the modular design of the concept.

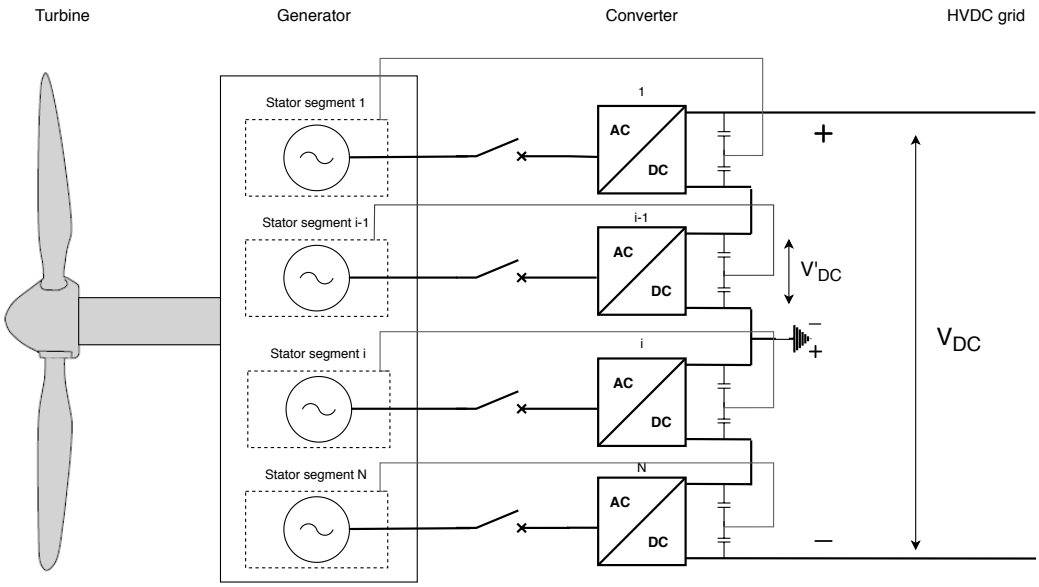


Figure 1.2.1: ModHVDC generator concept, illustrating the segmented stator and modular converter. Each stator segment is connected to the DC potential through copper wires from the segments to the DC side of the converter modules. [1, 7]

The stator is divided into N segments with a defined voltage level. Each segment are connected to a dedicated power converter, which are series connected on the DC side. Each stator winding are confined within a laminated iron stator that floats on the DC voltage potential (See figure 1.2.3). These stator segments are thus connected to the corresponding DC-voltage level of the converter. By doing this, a decoupling of the AC- and DC- field is achieved. DC insulation can withstand higher field stresses than AC insulation, which provides the possibility of reducing the amount of insulation. [3, 7, 8].

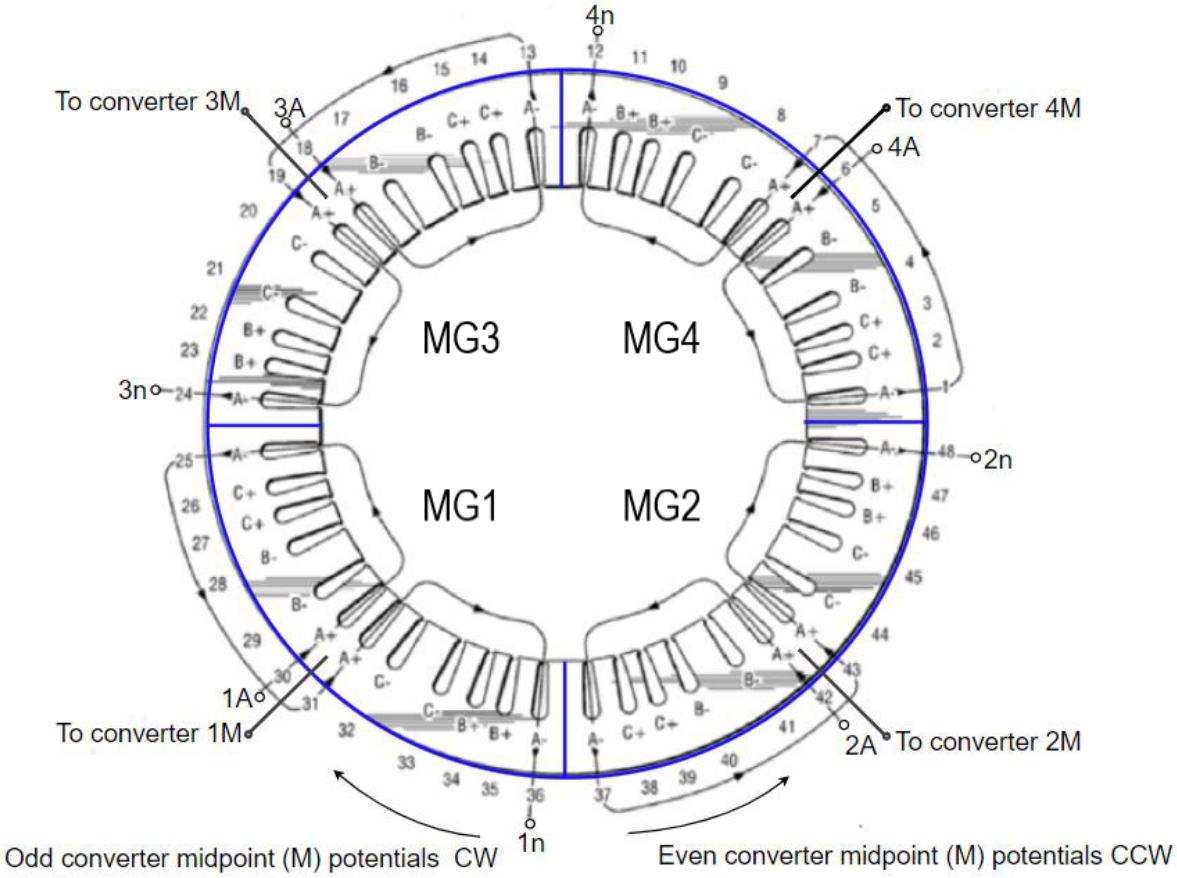


Figure 1.2.2: ModHVDC stator divided into modules (example of 4 modules shown here). Blue (bold) lines are DC voltage insulation. Individual iron core modules are connected to converter midpoints (1M-4M). Phase A connection (A) and neutral end (n) are shown for all module windings. [1, 3]

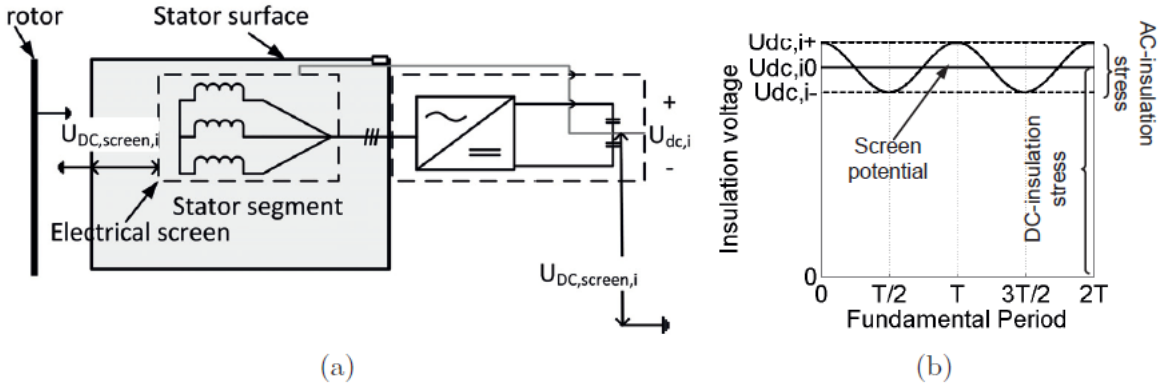


Figure 1.2.3: a) Illustration of electric screen connected to a converter unit on floating DC potential. b) Illustration of the division of the insulation-voltage stress into an AC-field and an DC-field. [3, 8]

ModHVDC Generator in Previous Research

The following paragraphs were written as a part of the specialization project in the previous semester. However, the information is still relevant and thus included in this thesis also.

Several master thesis's from NTNU have been written on different aspects of the modHVDC concept. A master thesis from 2020 [7] emphasized the power electronic converters related to the modHVDC machine and performed a comparison between a three-level neutral-point converter (3L-NPC) and a conventional two-level voltage source converter (2L-VSC). A complete Simulink model was made for the system which have been used for inspiration in this thesis Another thesis from 2020 found in [9], was written with respect to the design aspect of a 16 segmented machine provided relevant information in regards of geometrical parameters. [3]

A doctoral thesis from 2012 [8] conceptualized the modHVDC generator as a 10 MW offshore wind turbine with direct drive and nine stator segments. The power converter used in this thesis was a 2L-VSC and played a important role in providing a detailed description of the system that was helpful for this project. [3]

There is little to none previous literature on fault detection and protection for modular machines. Hence, there are different aspects of the concept that needs to be investigated in detail before it can be applied to a power grid. The research done in this masters thesis aim to fill some of the knowledge gap on faults and protection for modular machines. [3]

1.3 Research objectives

This thesis is an extension of the specialization project conducted in the semester leading up to this thesis and aim to fill some of the knowledge gaps within the field of faults and protection regarding segmented machines. The following objectives constitutes the basis of the thesis:

- Develop a simulation model in Simulink environment that models the modHVDC generator with multiple stator segments and power electronic modules.
- Conduct fault analysis for module-to-module faults and module-to-ground faults to investigate the severity of the corresponding fault currents and voltages that will occur.
- Identify possible faults and propose protection strategy for the modHVDC concept in regards to these, which should inhabit detection, mitigation and handling.

1.4 Limitations

Certain limitations have been set in order to limit the extent of the project. The following limitations should be noted as they will have an impact on the end result:

- Generator modelled as ideal voltage sources.
- The conducted fault analysis is based on steady-state operation and restricted to DC faults. Also the possibility of sequence of faults is not considered.
- Control strategy for the converter modules are limited to Sinusoidal Pulse Width Modulation (SPWM).
- Simple droop control solution which is not dynamically self-adapting.
- Simplified HVDC transmission model where the cable is modelled as a pure resistance, excluding pi-sections and onshore converter modelled as a stiff voltage source.
- Ideal switching components applied as breakers and fuses.

1.5 Structure of the report

Explanation of the content of each of the chapters that constitutes this thesis are presented in this section.

Chapter 1: Introduction to the modHVDC concept and which role the technology can have in future renewable energy systems are presented. The research gaps regarding renewable energy as well as the research objectives and questions that this thesis is based on are presented.

Chapter 2: The background theory regarding the technology that is analyzed in this thesis as well as the theory around the analytical methods that are applied is presented in this chapter.

Chapter 3: Literature review of the state-of-art Multilevel Modular Converters (MMC) in regards to fault handling including relevant protection components that are of special interest for the modHVDC concept are presented.

Chapter 4: The modelling setup applied in the Simulink model is presented. This includes the module structure, converter topology with corresponding control scheme and HVDC transmission model. The content from this chapter end throughout the rest of the thesis is considered as my personal contribution to the modHVDC project.

Chapter 5: Here, overview of potential failure modes are presented. This overview is a direct product from the Specialization project that constitutes the basis for this thesis. Thereafter, based on new work for this thesis, circuit analysis is presented for module-to-ground and module-to-module faults. Specific protection strategies are proposed and DC-link discharge dynamics are analyzed for two proposed DC-link designs for mitigating fault current and to isolate faulty modules and have continued operation of the remaining modules.

Chapter 6: The simulation results are presented with corresponding discussion of the used methods and obtained results.

Chapter 7: Conclusions to the research objectives and questions that this thesis intended to answer.

Chapter 8: Proposed further work that is thought to be a natural next step in regards research of protection strategies for the modHVDC concept.

Appendix: Related attachments that are excluded from the above chapters.

Chapter 2

Background theory and system modeling

This chapter aim to give background to the relevant aspects that are considered in this thesis. Theory regarding the specific converter technology that is applied is presented. Thereafter, some additional background theory regarding how the modeling of the mod-HVDC is done in this thesis are given.

2.1 Two-level voltage source converter

For the purpose of this thesis, the conventional Two-level Voltage Source converter (2L-VSC) is applied in the simulation model as a reference due to its simple structure. The 2L-VSC is a fully controllable converter and the topology is presented in Figure 2.1.1. [3, 7] Note that in the modHVDC model for this thesis, each converter module as illustrated in Figure 1.2.1 is represented by a designated 2L-VSC with the topology shown here.

The converter consists of semiconductor switching devices, called insulated-gate bipolar transistors (IGBTs) with anti-parallel diodes and is commonly used with Pulse-Wide Modulation (PWM) control method in VSC-HVDC projects. [6] This configuration is also utilized in the simulation part of this thesis. The converter consists of six IGBTs with anti parallel diodes, two identical capacitors constitutes the DC-link which splits the DC-bus voltage and forms a neutral point N. [3, 6, 7]

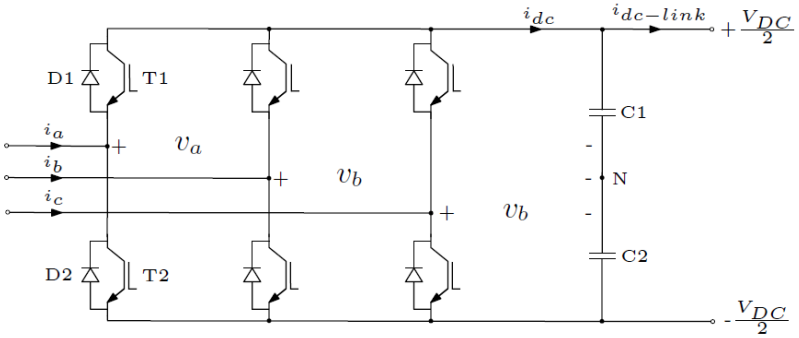


Figure 2.1.1: The 2L-VSC topology, consisting of six IGBTs and anti-parallel diodes. [3, 7]

PWM is a specific control strategy utilized to change between the two possible states that the 2L-VSC can obtain. Two control signals are compared to determine the ON/OFF switching of the IGBTs, the instantaneous magnitude of a triangular waveform and a sinusoidal input reference. If the control signal is greater than the triangular signal the state is 1, else -1. Depending on the state each phase will either have the value $+V_{DC}$ or $-V_{DC}$. [7, 10] Figure 2.1.2 illustrates the SPWM modulation for a 2L-VSC.

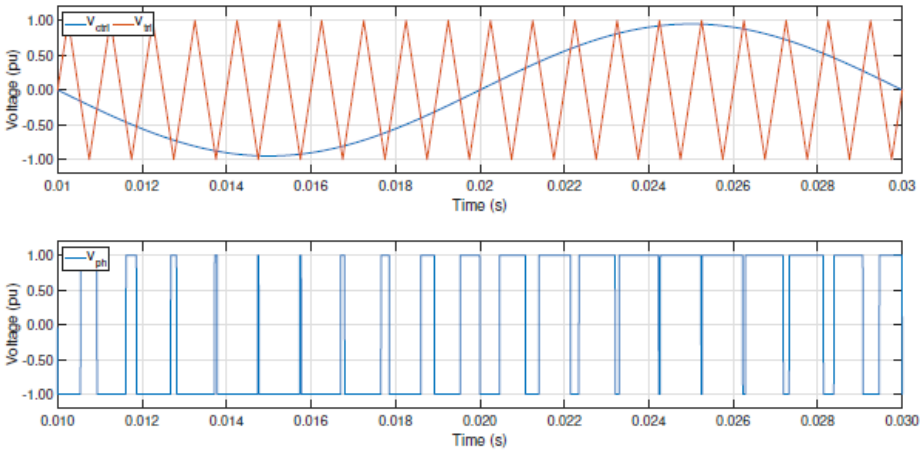


Figure 2.1.2: SPWM for a 2L-VSC [7, 10]

For the different states generated by the PWM scheme, the conduction pattern will be as illustrated in Figure 2.1.3 for phase a. The devices D1 and T2 and T1-D2 (i.e Diode and Thyristor) form pairs that conduct depending on the current direction. Which device in the respective pair that conducts depends on the state (-1 or 1) as shown. [7, 10]

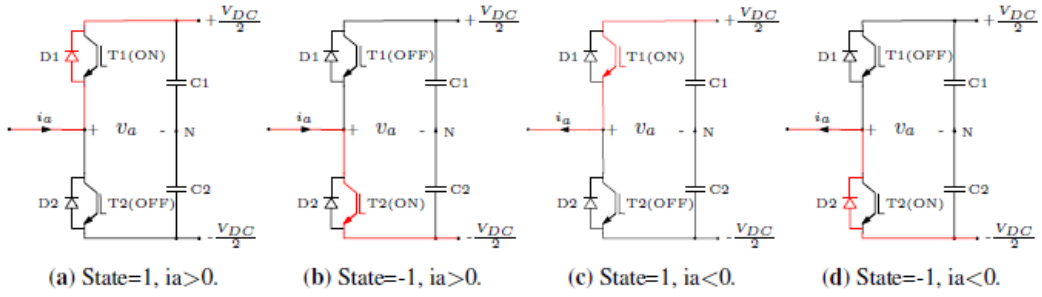


Figure 2.1.3: Conductor pattern in one phase leg of a 2L-VSC [7, 10]

The possible states, voltages and conduction modes are presented in Table 2.1.1.

Table 2.1.1: Possible states, voltages and conduction modes in the 2L-VSC converter. [7, 10]

State	Va	T1	T2
1	Vdc/2	ON	OFF
-1	-Vdc/2	OFF	ON

For a SPWM modulation scheme, the relation between modulation index and inverter voltages are given by Equation 2.1.1 and 2.1.2, respectively. [10]

$$V_d = M_d \frac{V_{DC}}{2} \tag{2.1.1}$$

$$V_q = M_q \frac{V_{DC}}{2} \tag{2.1.2}$$

The conventional Two-level VSC is widely applied in low to medium voltage applications due to its low complexity. However, for high voltage transmission systems the complexity increases due to the low voltage rating of IGBTs. In order to lower the voltage stress on the IGBTs, series connection of multiple IGBTs is needed. [11] An illustration of such series connection is presented in Figure 2.1.4.

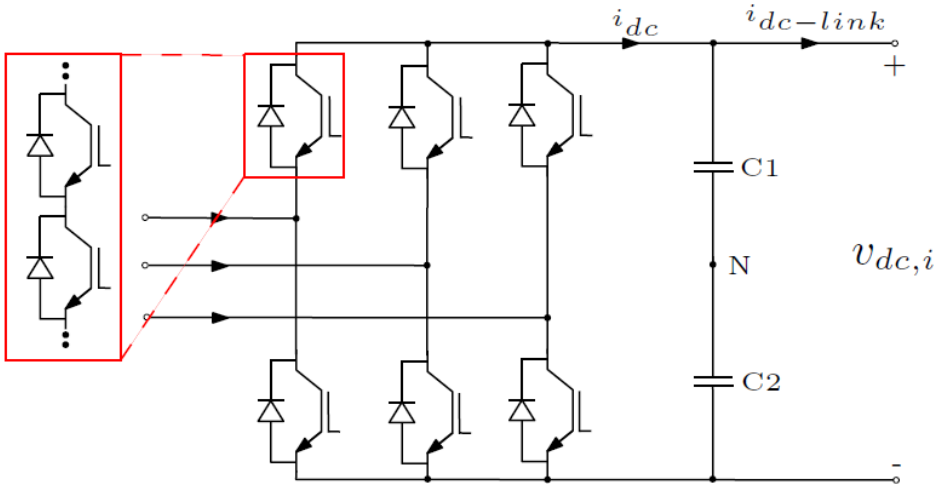


Figure 2.1.4: Illustration of series connection of IGBTs to comply with voltage ratings [7, 11]

This adds to the complexity and introduces the need for accurate switch control to ensure that the branch of IGBTs are able to switch simultaneously. A delay in the switching in one part of the branch can lead to severe damage. The 2L-VSC also has the need for bulky and expensive filtering, which adds to the negatives. With the generator specifications applied for the modHVDC in this work, series connections of IGBTs would be needed. The highest voltage rating for commercial available IGBTs are 6.5 kV. [11] This speaks in favor of the increasingly popular Modular Multilevel Converters (MMC) as the preferred technology for this application. This is a topic investigated in Section 3.1

DC fault handling

The modHVDC concept introduces some new failure modes that can occur on the DC-side of the converter. As a consequence, DC-fault handling capacities of the converters are of special interest in this thesis.

The 2L-VSC is not able to withstand faults originating from the DC side since their freewheeling diodes function as an uncontrolled rectifier bridge, which feed the DC fault, even if the semiconductor switches are turned off. With the AC side contributing to the DC fault, the current passing through the diodes can cause severe damage and destroy the diodes. [12] The 2-VSC during a pole DC fault is illustrated in Figure 2.1.5. The fault current (I_f) is the sum of the contribution from the AC grid (I_{gc}) and the discharge current from the capacitors (I_{dis}).

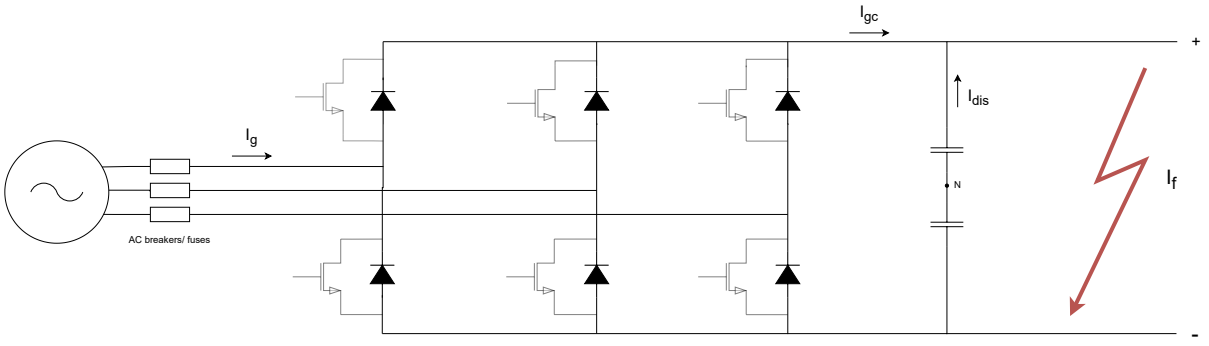


Figure 2.1.5: 2L-VSC rectifier during DC-fault. AC currents are feeding fault due to the freewheeling nature of the diodes. [12]

The diodes used with IGBTs are fast recovery diodes characterized by their low surge current withstand capability. This means that even if fast acting current breakers are used to isolate the AC side, there will be a risk of damaging the diodes before the CB is able to react. [12]

DC-link

The DC-link bus is the central energy storage and transfer element. The capacitors acts as a centralized capacitor bank working as an energy buffer. These should keep the power stable during transients and also satisfy small ripple and small transient over-voltages.[13] The DC capacitor size can be determined by a time constant τ, defined as ratio between the stored energy at the rated direct voltage, and the nominal apparent power of the converter. [14] In 2L-VSC a time constant between 5 ms and 10 ms is considered to be sufficient. [3, 15, 16]

The capacitors are amongst the most fragile power converter components. According to [17], as much as 30% of converter failures can be related to the DC-link capacitors. The paper concluded that the equivalent series resistance (ESR) has a strong influence on the voltage ripple, leading to high risk of failures.

Continued degradation is likely to result in component failure. In the case of a complete loss in ability to function, the component can become an short- or open circuit. Continued degradation causes rising ESR and decrease of capacitance. [17] Table 2.1.2 presents the most common causes of DC-link capacitor failures.

Table 2.1.2: Failure modes related to DC-link capacitors with causes and physics of failure mechanisms. [17]

No.	Capacitor failures		
	Cause	Physics of failure mechanism	Failure mode
1	Overvoltage stress	Increase in internal temperature	Decrease in Capacitance and increase ESR
2	Excess current ripple	Degradation/loss of capacitance of cathode and anode foil	Open-circuit
3	Charging/ discharging cycles	Electrolyte evaporation	Short-circuit
4	Degradation due to nominal operation	Ageing/degradation in the dielectric	-
5	-	Corrosion (electrodes)	-
6	-	Increase in the internal pressure	Open pressure vent

The discharge rate of a capacitor is dependant of its time constant (τ). The time constant of a capacitor is given by Equation 2.1.3. [18]

$$\tau = R \cdot C \tag{2.1.3}$$

The stored energy in a capacitor can be calculated by Equation 2.1.4. Where C is the capacitor capacitance, and V_{DC} is the voltage over it. The resulting energy is given in Joules. [18]

$$E_{cap} = \frac{1}{2} C V_{DC}^2 \tag{2.1.4}$$

The discharge equation for a capacitor yields the rate of discharge over time based on its initial voltage and inherent time constant. The current will have a large peak before decaying over time due to the resistive element. The voltage discharge is given by Equation 2.1.5. [18]

$$U_c = U_0 \cdot e^{\frac{-t}{RC}} \Rightarrow I_c = \frac{U_0}{R} \cdot e^{\frac{-t}{RC}} \tag{2.1.5}$$

The same equation is valid also for the discharge current, only by dividing U_0 on the resistance R to get the current. The discharge curve for capacitors is illustrated in Figure 2.1.6. After five timeconstants (5τ), the capacitor discharges 99.3% of the initial voltage. [18, 19]

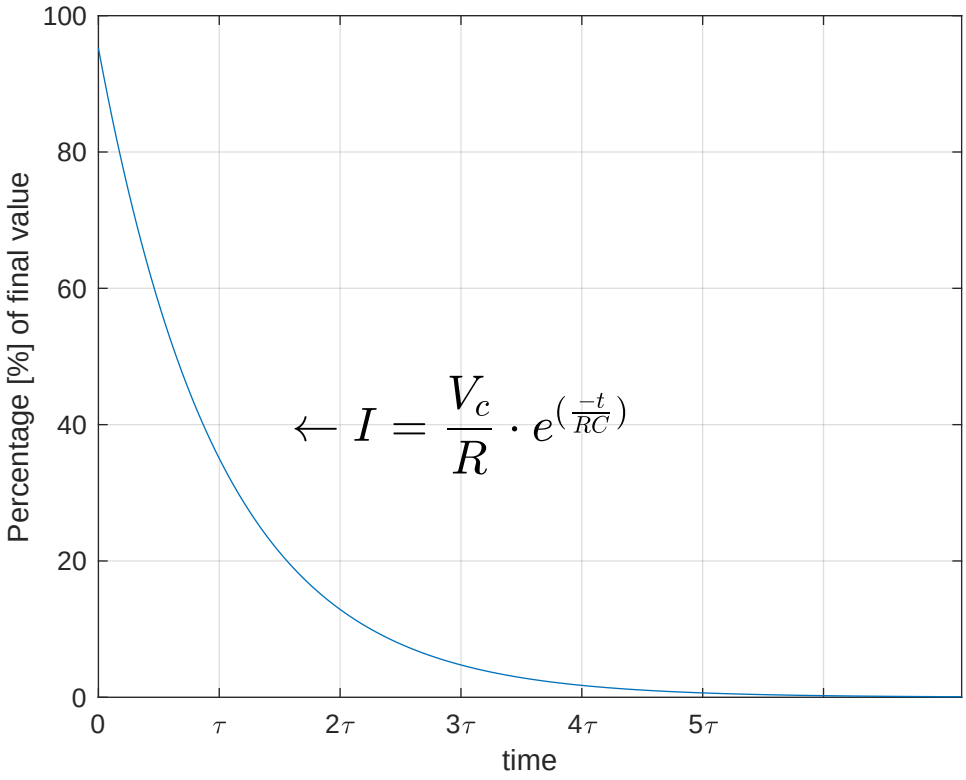


Figure 2.1.6: Discharge curve for capacitors. [18]

2.2 Description of ModHVDC model

In order to stay consistent and relate this thesis to previous research related on the modHVDC concept, the model is based on a 10 MW, 100kV generator system. Nine individual stator segments are chosen (N=9). This means that each converter unit must handle a DC voltage of 11.1 kV and a power rating of 1.1 MW. This voltage level would require series connection of IGBTs. This is not accounted for in the simulations. Hence IGBTs will have a too high voltage distribution compared to the highest rated components that are available.

Model parameters

Table 2.2.1: ModHVDC generator parameters.

Symbol	Parameter	Value	Unit
P_{nom}	Rated power	10	MW
I_{nom}	Rated current	110	A
V_{DC}	DC voltage	100	kV
N	# of segments	9	-

The power is equally distributed between the segments as shown by the simple Equation 2.2.1. The AC side voltage is derived from Equation 2.2.2, and the grid voltage neccesary for having the output power at 10 MW is given from Equation 2.2.3.

$$P_{seg} = \frac{P_{nom}}{N} \tag{2.2.1}$$

$$V_{seg,AC} = \frac{P_{seg}}{\sqrt{3} \cdot I_{nom}} \tag{2.2.2}$$

$$v_{dc,i} = \frac{v_{DC,tot}}{N} \tag{2.2.3}$$

From the equations above the module parameters are derived and listed in Table 2.2.2.

Table 2.2.2: ModHVDC generator parameters.

Symbol	Parameter	Value	Unit
P_{seg}	Rated power	1.11	MW
$V_{seg,DC}$	DC-link voltage	11.11	kV
$V_{seg,AC}$	AC voltage	5.832	kV

Due to the series connection of converter modules is that the DC-side current of the converters must be equal in steady state. If there are any difference, the DC-link capacitors will compensate by either charging or discharging.

$$\frac{dv_{DC,i}}{dt} = i_{DC,i} - i_{DC-link} \tag{2.2.4}$$

Control system

Synchronous Reference Frame Theory

The control system applied for generating the PWM scheme in the Simulink model is based on Synchronous Reference Frame (SRF) theory. It is a commonly used method due to its simplicity, as it only applies algebraic equations. [19]

The method in general applies a direct (d-q) and inverse (d-q) Park transformation in order to transform the three-phase voltage and current into their active (d-) and reactive (q-) components. The d-q components are in a rotating synchronous frame with the positive sequence of the system voltage. The synchronous reference frame system d-q-0 rotates at synchronous speed $\omega_s = 2\pi f_s$. Where ω_s is the angular electrical speed of the rotating magnetic field of the three phase supply. [19, 20]

Clark and Park transformation

Clark transformation converts balanced three-phase quantities into balanced two-phase quadrature quantities (α and β). The equations in matrix form is presented in Equation 2.2.5.

$$\begin{bmatrix} u_\alpha \\ u_\beta \\ u_0 \end{bmatrix} = \frac{2}{3} \begin{bmatrix} \frac{2}{3} & -\frac{1}{3} & -\frac{1}{3} \\ 0 & \frac{1}{\sqrt{3}} & -\frac{1}{\sqrt{3}} \\ \frac{1}{3} & \frac{1}{3} & \frac{1}{3} \end{bmatrix} \cdot \begin{bmatrix} u_a \\ u_b \\ u_c \end{bmatrix} \tag{2.2.5}$$

The three-phase quantities can be transformed into its rotating reference frame quantities (d-q-0) using Park transformation as illustrated in Equation 2.2.6. [19, 21]

$$\begin{bmatrix} u_d \\ u_q \\ u_0 \end{bmatrix} = \frac{2}{3} \begin{bmatrix} cos(\omega t) & cos(\omega t - \frac{2\pi}{3}) & cos(\omega t + \frac{2\pi}{3}) \\ -sin(\omega t) & -sin(\omega t - \frac{2\pi}{3}) & -sin(\omega t + \frac{2\pi}{3}) \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} \cdot \begin{bmatrix} d_a \\ d_b \\ d_c \end{bmatrix} \tag{2.2.6}$$

dq- based Phase Locked Loop (dqPLL)

There exists many types of PLL algorithms. However, as a dq-based PLL is applied in this thesis, only this method is described.

The PLL circuit provides the rotation speed of the rotating reference frame. The phase of the input voltages are acquired as the q-component of the positive sequence voltage tracks a zero reference through a PI controller. As a result, under ideal voltage conditions, ωt becomes equal to the phase angle of the three-phase voltage. This information can be applied to synchronize the on/off switching of power devices such as IGBTs. [22, 23]

Figure 2.2.1 illustrates how the PLL is applied to align the d-axis component with the grid voltage.

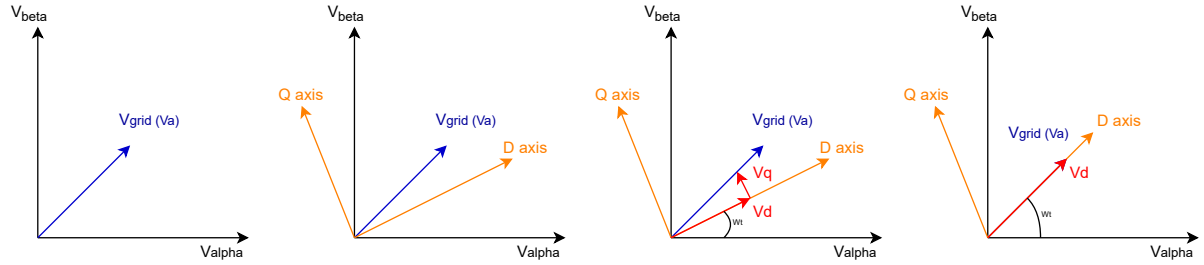


Figure 2.2.1: Applying Phase Locked Loop (PLL) to align D-axis with grid voltage.

A negative in regards to this method is that since the synchronous frame is rotating with the positive angular speed, the method only works accurately for balanced grid faults. [22]

Proportional Integral (PI) controllers

The PI-controller takes as input the difference (error) of the process variable and the reference signal. As the name indicates, there are two separate parameters that dictates the PI-controller algorithm, the proportional and integral. The proportional value determines the reaction to the error, while the integral determines the reaction based on the sum of the recent errors. The process of the converter are adjusted based on the weighted sum of these two actions. [20]

2.3 Fault Protection Components

This section will take a look at component related to protection that is found to be of interest to the proposed protection system of this thesis.

2.3.1 High voltage Fuses

Due to the development in HVDC transmission technology in recent years, more attention is given to the development of breaker technologies that can comply with the very high speed di/dt that can occur during faults. [24]

HVDC fuses

In the case of short-circuit faults in VSCs, the fault current has a very high di/dt due to low inductance in the capacitor discharge loop. This emphasizes the need for specific fuse development for breaking time under 100 µs. A 2019 study investigated fuse interruption under 4000 V DC with low inductance for VSI application. Due to the high speed di/dt results in limited heat dissipation which becomes a challenge with regards to the cooling and current capacity accepted by a single fuse. 3 large rated parallel current fuses were therefor used for the breaking tests as a mean for increasing the heat exchange surface. [24]

AC fuses

In the case of AC-side protection in VSC-HVDC systems, fuses are generally seen as a bad solution. As fuses are a thermal device, it is thus not able to distinguish between temporary or permanent faults. If the fuse were to blow, the system is not able to be restored before the fuse is physically replaced. Conventionally. fuses are used for AC protection, while other DC devices protect the DC line. In such a case, the DC devices will trip before the fuse and the fuses will act as a backup if the DC protection were to fail. [25]

2.3.2 Circuit breakers

AC circuit breakers are a well known and proven technology. But as VSC-HVDC is becoming an increasing part of the energy system, a lot of research is focused on fast acting DC circuit breakers that can handle the high speed di/dt that is proven to be a challenge in these systems.

AC Circuit Breakers (ACCBs)

AC devices for protection purposes has several advantages such as low cost compared to its DC counterparts and mature science. However, these CBs have the longest interruption time, due to mechanical restrictions. The best interrupting time according to [25] is two cycles. Compared to fuses as an AC side protection in VSC-HVDC systems, ACCBs have the possibility of an re-closing cycle to test if the fault is temporary or permanent. In the case of VSC applications, ACCBs are seen as the most cost effective solution for AC side protection. [25]

DC Circuit Breakers (DCCBs)

In order to successfully clear DC faults in HB-based topologies, DCCBs are required. These are expensive due to the fast response time that is required because of the fast rise time of DC fault currents. DCCBs must be able to create a current zero for it to be interrupted, and the stored energy in the network must be dissipated. Some research papers suggests Hybrid HVDC circuit breakers (HCBs) as one of the most suitable CB technology for application in HVDC systems. [6, 26]

One particular technology have caught commercial interest as it can block 9 kA fault current within 5 ms. An DCCB based solution could require large fault limiting reactor to perform fault interruption. A 2018 study investigated a solution with HCB as the main protection in a HVDC transmission system as illustrated in Figure 2.3.1. [26]

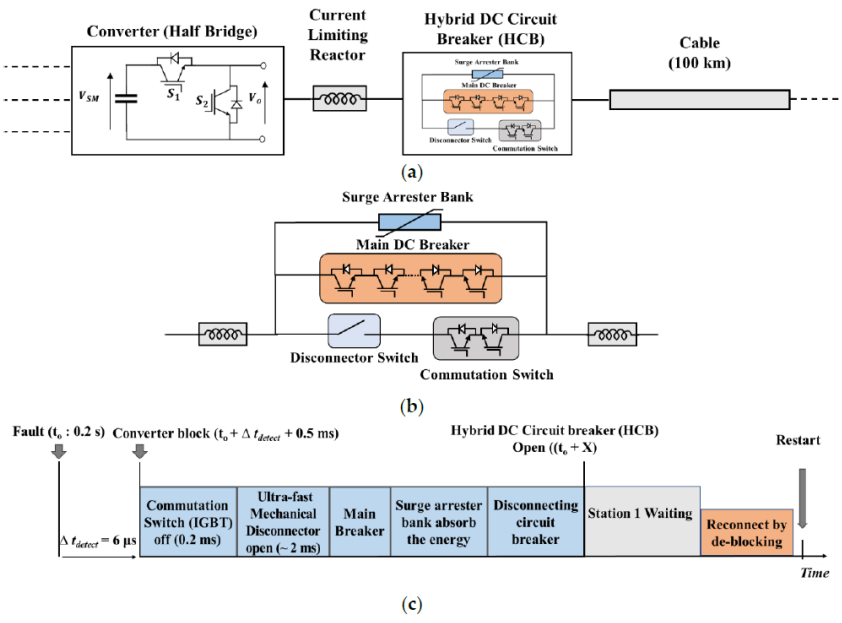


Figure 2.3.1: DC fault handling solution for an HB-MMC based on a hybrid circuit breaker (HCB): (a) configuration; (b) structure of the HCB; (c) fault handling under a DC short-circuit fault. [26]

2.3.3 DC Chopper Resistors

Chopper resistors is a method that have been commonly applied in offshore wind power plants as a mean for fault voltage mitigation in the case of grid faults. In order to uphold overall system stability, the DC-link stored energy can be discharged and dissipated as heat in the chopper resistor. [27] A VSC system with chopper resistor is presented in Figure 2.3.2.

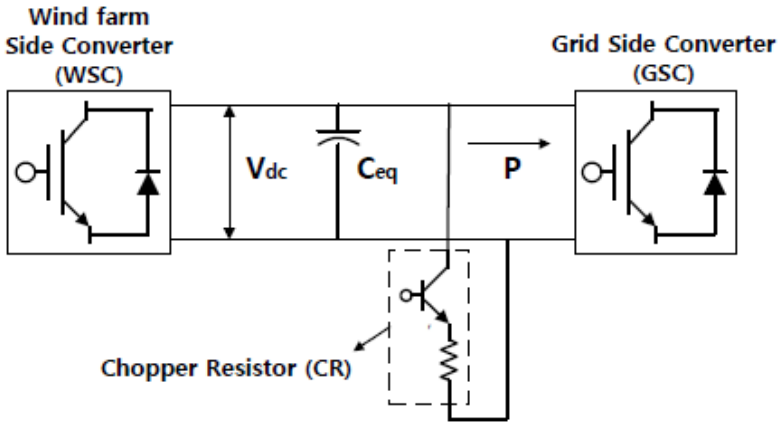


Figure 2.3.2: Illustration of a chopper resistor on the DC-link. [27]

The chopper method is found to be an effective solution in medium voltage systems. However, Some of the downsides is that the related costs is high, specially if the current flowing through it is high as additional cooling may be required. There is also considerable waste of produced energy until the fault is cleared. [27, 28]

Chapter 3

Literature review

This chapter presents an overview of commercially and experimentally tested MMC topologies with focus on their fault handling capabilities. The findings aim to provide insight into possible solutions that may be suitable for the modHVDC concept.

3.1 Converter technology suitable for modHVDC

Previous research have been performed in regards to finding the optimal converter topology for the modHVDC concept. Modular Multilevel converters (MMC) are found to be the most promising in regards of efficiency and reliability. Despite this, the conventional two level topology are applied as a base case for the purpose of this thesis. This section will consequently focus on state-of-art MMC topologies, with a main focus on their fault handling capabilities and the complexity of the different solutions.

When trying to decide upon the optimal converter topology for the modHVDC concept, several aspects should be considered. The segmented stator concept that the modHVDC generator is based on, can be considered as increased complexity as each segment will have a designated converter. This stresses the importance of utilizing converter technology with high reliability and fault handling capabilities. Specially in the case of offshore wind applications, this aspect is important due to the increased cost and effort to perform repairs and maintenance.

The main aspects that should be considered and that constitutes the basis of this literature review is summarized in the listed points below:

- Reliability/ availability
- System complexity/costs
- Fault handling capabilities
- Industrialized realized in MW range

3.2 Modular Multilevel Converters (MMC)

The MMC converters have already been found to be the most promising technology for industrialized realization of the modHVDC generator, based on previous work related to the same concept. [11] This section aim to present an overview of the current state-of-the art MMC technology in order to give an understanding of the main challenges, with focus on the sub-module topologies and its fault handling capabilities.

A research paper from 2013, compared the conventional 2L-VSC against five multilevel topologies. Based on simulations, the paper concluded that the MMC was the most suitable technology due to superior voltage quality, no need for series connection of IGBTs, redundancy possibilities and low filtering demand. [11]

A review of modular multilevel converters with focus on state-of-art sub-module topologies found in [29] was published in October 2020. This paper was at the time of writing the most recent and thorough publication on this subject, and have been a main inspiration when describing the different topologies.

3.2.1 MMC topology

The MMC topology can be illustrated by the generalized configuration presented in Figure 3.2.1. The three-phase MMC comprise of a DC terminal, an AC terminal, and a converting kernel involving three phase legs. Each leg/phase has two symmetric arms referred to as the upper arm and lower arm. The upper arm and lower arm contain a group of identical sub-modules (SM) connected in series together with a inductor to suppress high-frequency components in the arm current. [29, 30]

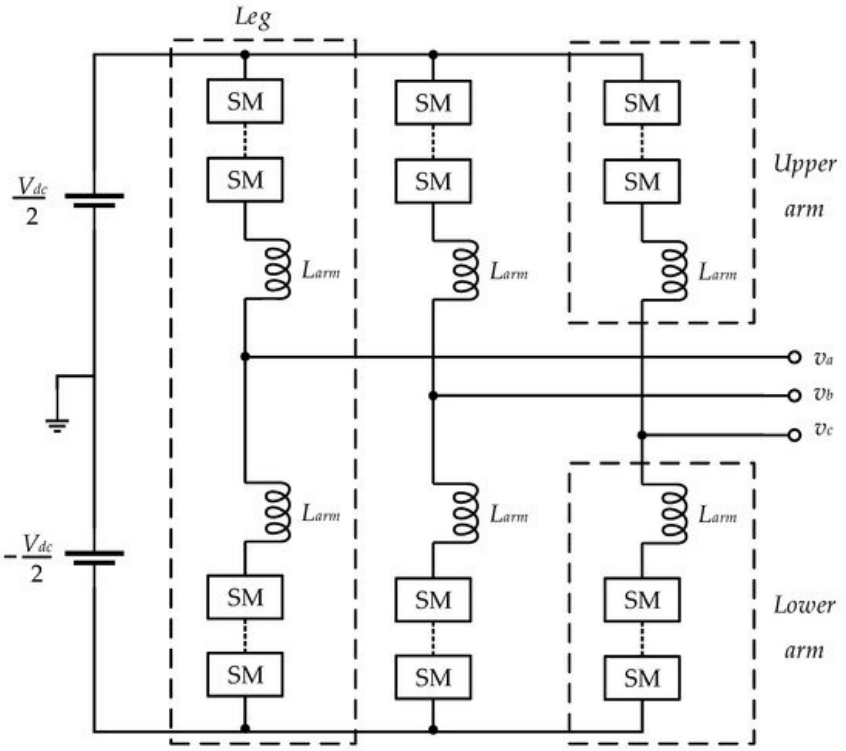


Figure 3.2.1: Generalized configuration of the MMC topology. [29]

The MMC provides a more advanced voltage source converter topology compared to the 2L-VSC presented in Section 2.1. Some similarities regarding fault blocking capabilities is found between the two technologies depending on the specific topology. However, MMC has some clear advantages such as output performance, high modularity, simple scalability, and low voltage and current rating demand for the power switches. The technology is very suitable for medium and high-voltage power conversion systems such as HVDC transmission systems, and can achieve bidirectional power conversion. However, several technical challenges such as modelling, control and protection still limits the practical use. [29, 30] Specially, DC-side fault blocking capability have been an area of significant research in recent years, as the dc fault blocking capability is a major shortcoming of the HBSM-based MMC (HB-MMC) and its handling is found to be the most serious challenge in the implementation of VSC-type DC transmission systems. [26, 31]

3.2.2 Two level sub-module topologies

The performance, cost and fault handling capabilities of the MMC is very much dependant on the sub-module (SM) topology that the MMC is based on. The SM is one of the fundamental components in the MMC and can be categorized into two- or multilevel topologies. A wide range of sub-module topologies have been proposed by researchers in the years after the MMC was first introduced. [29] Some of the most common two-level SMs are presented in Figure 3.2.2.

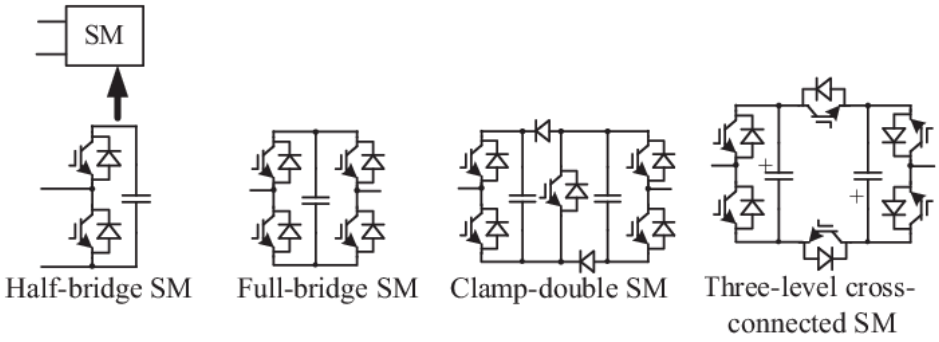


Figure 3.2.2: Commonly applied sub-module configurations. [30]

Half-bridge SM (HBSM)

HBSM based MMCs is widely applied and one of the most popular configurations. The HBSM is the simplest of the sub-module topologies, and have advantages as high-quality output voltages, easy scalability, modularity, much lower switching loss, elimination of dc bus capacitor, and smaller filter size when compared with two or three-level voltage source converters. However, it has some significant drawbacks regarding handling of fault currents. HB-MMC based systems have similar DC-fault characteristics with that of the conventional 2L-VSC described in Section 2.1. [29, 31]

The HBSM has two power switches with anti-parallel diodes and a floating capacitor. The SM voltage is either zero or equal to the capacitor voltage, depending on the switching state. Due to the freewheeling effect of the diodes, fault currents fed from the AC grid can not be blocked in the case of DC-side short circuit fault. [29, 32] The anti-parallel diodes of HBSMs conducts as rectifier bridges after the IGBTs are blocked. For this case, the

fault current continues to be fed from the AC grid until the AC side is isolated by some form of breaker operation. [32] If the fault current is able to flow uninterrupted through the converter, the semiconductor devices will have a great chance of being damaged or destroyed. [31] An illustration of the MMC converter with HB SMs during DC faults is presented in Figure 3.2.3.

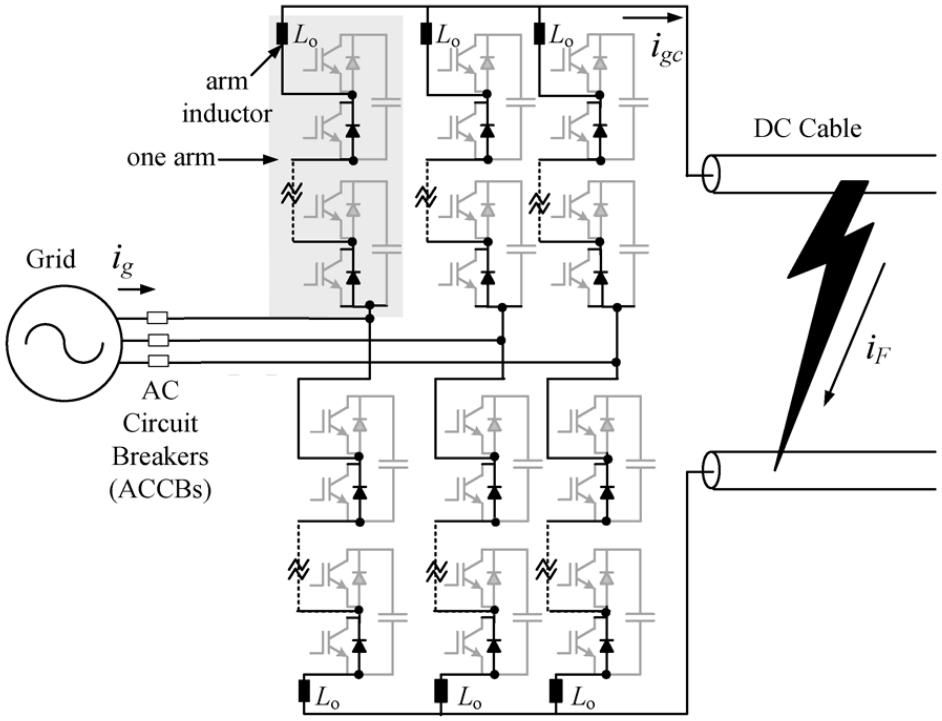


Figure 3.2.3: MMC converter with half-bridge SMs during DC-fault. [12]

Contrary to the 2L-VSC topology presented in Figure 2.1.1, the common DC-link capacitor is not utilized, which is favourable in regards to the discharge current during fault in MMC converters. However, there is still contribution from the AC side as there is no segregation between the AC and DC side during faults. [12]

Two solutions can be implemented to counter the DC fault handling capabilities. These solutions are illustrated in Figure 3.2.4. The first is to introduce a clamp-single sub-module (CSSM) to suppress fault current. CSSM is composed of a HBSM with an additional transistor/diode pair. Two configurations is possible as shown in Figure 3.2.4 a,b). During normal operation, S3 is always conducting. In the case of a DC fault, all transistors are set to OFF to block the fault current. The second solution is to introduce thyristors to the HBSM, either Single- or double thyristors based HBSM as shown in Figure 3.2.4 c,d). The thyristor(s) are connected to the terminal and are always turned off during normal operation. When a DC fault is detected the current is forced to flow through them. [29, 32]

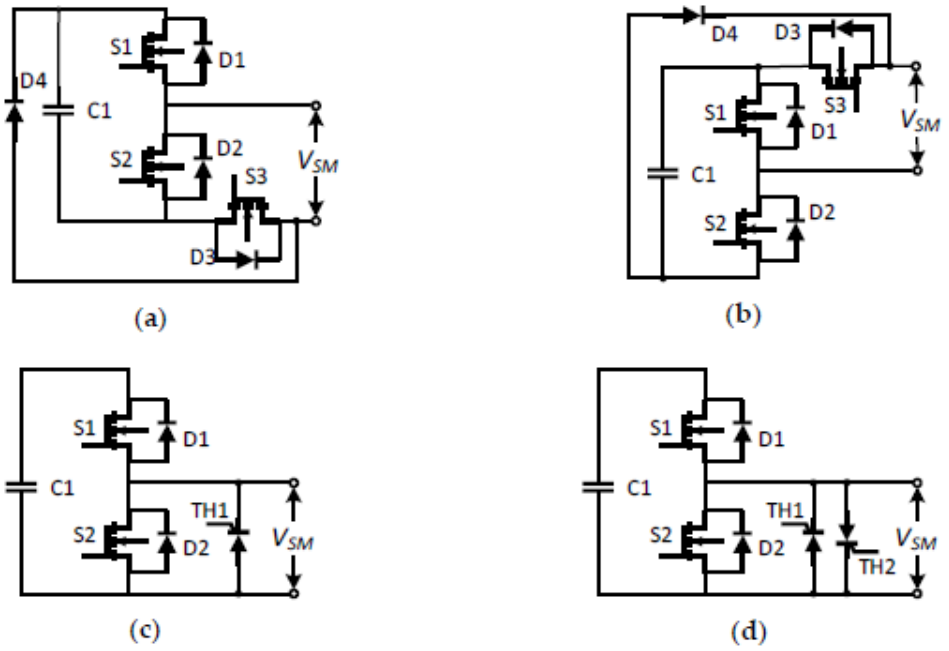


Figure 3.2.4: (a) clamp-single submodule (CSSM) type-1; (b) CSSM type-2; (c) Single-thyristor HBSM; (d) Double-thyristor [29]

Full-bridge SM (FBSM)

The FBSM has two half-bridge legs with one floating capacitor as illustrated in Figure 3.2.2. Each of the two legs has two switches with anti-parallel diodes. the voltage can now have three voltage levels, i.e zero, v_c and -v_c. This enables the SM to counter DC fault current. [29] The FBSM can cut off arm currents in any direction by blocking all of the IGBTs. The complete blocking of the DC fault current occurs when the total voltage of each SM capacitor becomes higher than the maximum peak line-to-line AC voltage. The configuration in FB-MMCs does not allow the discharge of DC side capacitors. FB-MMC does thus not necessarily require either DCCBs or current limiting reactor as oppose to the HB counterpart. However, this topology requires double the number of power components, thus increasing the investment costs. Another drawback regarding the FB topology is that, in order to be able to eliminate faults, the price to be paid is to double the loss of power during normal operation. [5, 26, 30] According to [29], unidirectional topologies in which certain IGBTs are substituted by diodes have been proposed to drive down costs.

Multilevel sub-module topologies

The two commonly applied MMC topologies are the Neutral-point Clamped (NPC) and the Flying Capacitor (FC) topologies. NPCSM contains four IGBT devices with anti-parallel diodes, two clamping diodes, and two capacitors. FCSM differ from NPCSM by not having clamping diodes. Both of them can generate three voltage levels: v_{c1} + v_{c2}, v_{c2} or zero for NPCSM, and v_{c1}, v_{c1} - v_{c2} or v_{c2}, zero for FCSM. [29]

Various other configurations with varying complexity and fault handling capabilities are proposed as alternatives to the NPCSM and FCSM. A list of these multilevel sub-module topologies are presented below:

- Neutral Point Clamped (NPCSM)
- Flying capacitor (FCSM)
- Cascaded (CHBSM)
- Clamp-Double (CDSM)
- Hybrid (HSM)
- Cross-Connected (CCSM)
- Switched Capacitor (SCSM)
- Composite three-level (CSM)

The Clamped-Double SM (CDSM) is one of the configurations that is able to block fault current. This is achieved by implementing two identical HBSMs connected by two extra diodes and an IGBT, which is always on during normal operation. When a DC fault is detected, all the power components are set to OFF to block the current. The CDSM has only half utilization of the capacitor voltage (-v_{c1} or -v_{c2}) when in blocking mode. Hence, by applying one extra IGBT, -2v_c output blocking voltage can be achieved. Higher switching losses are associated with CDSM as all switches work during normal operations. [29]

Hybrid SMs (HSMs) are another configuration that are made to withstand DC fault current. HSMs mainly based on HBSM although different variations can be applied. In Figure REF, a hybrid cell comprised of a HBSM in series with a FBSM is shown. A voltage-balanced HBSM-CDSM hybrid MMC topology was proposed in 2019 by [33]. By adding diodes between sub-modules based on the traditional HBSM-CDSM hybrid topology, DC faults was effectively isolated and the energy was evenly distributed across the capacitance of each sub-module during fault clearing. As a result, when a DC fault occurs on the line, the system can complete the fault current clearing and the system quick restart without disconnecting the AC breaker. [29, 33]

Cross-Connected SM (CCSM) can consist of two HBSMs cross-connected back-to-back via two IGBTs with anti parallel diodes as shown i Figure REF. The CCSM topology can handle DC fault current by turning OFF the cross-connected IGBTs. The drawback is higher power losses as the IGBTs conduct alternately during normal operation. [29]

A new Switched Capacitor SM (SCSM) was proposed by researchers in 2016 [34]. The topology showed to provide operation with DC fault blocking capability, and also achieved voltage balancing with half the number of voltage sensors applied in existing MMC cells. The reduced complexity of the control system ensures higher system reliability, while the DC fault ride-through is achieved by turning OFF all IGBTs. [29, 34]

A Composite three-level SM (CSM) topology introduces three DC fault blocking schemes which includes all-blocked, partly blocked and staged blocking. A CSM was proposed in 2018 by [35], which was found to effectively address the DC fault and achieve capacitor unbalanced charging without changing the independent operation states of the SMs. [29, 35]

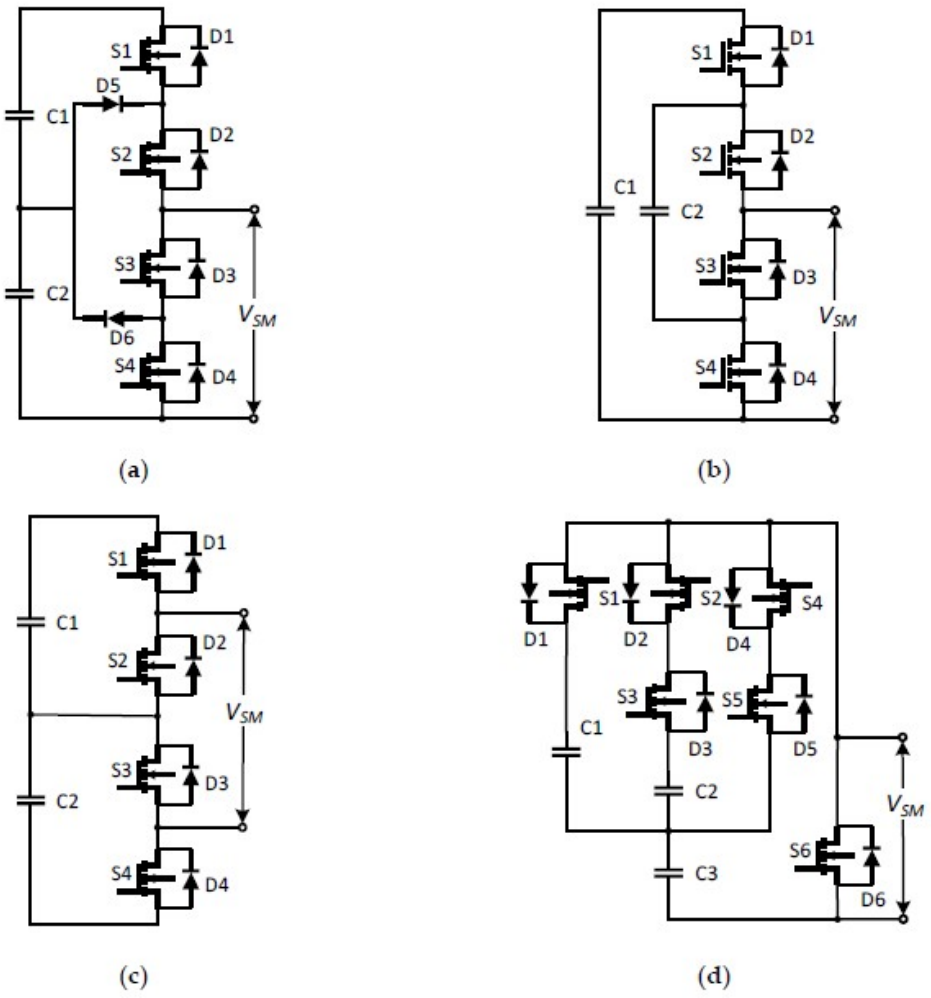


Figure 3.2.5: Multilevel submodule topologies: (a) neutral point clamped submodule (NPCSM); (b) flying capacitor submodule (FCSM); (c) cascaded half-bridge submodule (CHBSM); (d) stacked switched capacitor submodule (SSCSM) [29]

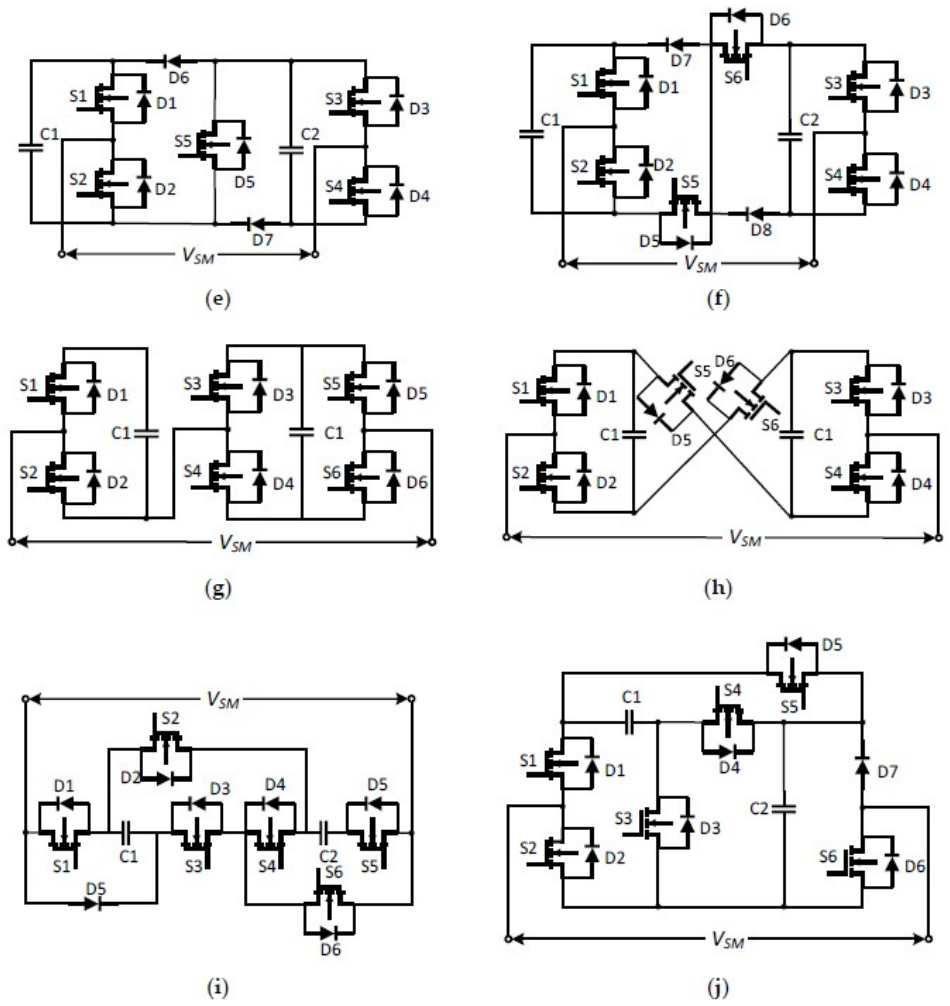


Figure 3.2.6: Multilevel submodule topologies: (e) clamp-double submodule (CDSM) type-I; (f) CDSM type-II; (g) hybrid submodules HSM); (h) cross-connected submodule (CCSM); (i) switched capacitor submodule (SCSM); (j) composite three-level composite three-level submodule (CSM). [29]

The before mentioned sub-module topologies are categorized by performance index as presented in Table 3.2.1. The performance index contains the number of sources, transistors and diodes to give an perspective on the complexity of the topology.

Table 3.2.1: Comparison between various SM topologies. [29]

Performance index	**HBSM**	**FBSM**	**SCSM**	**NPCSM**	**FCSM**	**CDSM**	**HSM**	**CCSM**
No. of sources	1	1	1	2	2	2	2	2
No. of transistors	2	4	3	4	4	5	6	6
No. of diodes	2	4	4	6	4	7	6	6
Max. voltage	v_c	v_c	v_c	$2v_c$	$2v_c$	$2v_c$	$2v_c$	$2v_c$
Bipolar operation	No	Yes	Yes	No	No	Yes	Yes	Yes
DC fault blocking	No	Yes	Yes	No	No	Yes	Yes	Yes
Power losses	Low	High	Low	Moderate	Low	Moderate	Moderate	Moderate
Cost	Low	Moderate	Moderate	High	High	High	High	High
Control complexity	Low	Low	Low	High	high	Low	Low	High

A 2018 study investigated th fault handling capabilities of the two mainstream MMC topologies (HB-MMC and FB-MMC) in combination with adequate protection devices. AC and DC side transient analysis were performed in regards to fault interruption. The results proved that "the fault handling performance of an HB-MMC with a DC circuit breaker is superior due to smaller fault current magnitude, faster interruption time, lower overvoltage magnitude, and lesser stresses on the insulation of the DC grid." [26]

The overall structure of the MMC can contain a combination of different types of sub-modules with various arrangements. This is an active field of research as the hybrid arm/leg architecture is a key factor to achieve acceptable performance i.e adequate system costs, power losses and DC fault blocking capabilities. This is not further elaborated on in this thesis but [29] gives good insight to this topic.

3.2.3 Modifications to improve fault blocking capabilities

DC fault blocking capabilities in MMC converters can be achieved. The first is to have fault-blocking SMs, which are already elaborated on. Another solution which have been implemented in other projects, are AC-side CBs. They are however slow in response. The second solution is to utilize fast DCCBs, but these are limited by their high and relatively high conduction losses. [12] However, hybrid HVDC breakers (HCB) that can cope with the rapid rise of fault current in HVDC grids are catching attention. [26]

1. Fault-blocking SMs
2. DCCBs/ACCBs
3. Converter-embedded device protection

The fault blocking capabilities of the MMC depends on the configuration of the SMs. The blocking capability can be embedded into the MMC by applying fault-blocking SMs that block fault current from flowing through the converter. MMC converters with fault blocking SMs can limit the fault effectively within a few milliseconds. [26] Different SM variations based on either HBSM, FBSM or a combination of the two have been proposed to increase the fault handling capabilities. [26, 29, 31, 32]

IGBT response time/response time of fault blocking converters

In the case of converters with DC fault blocking capabilities, there will be an delay due to detection time and the time it takes for the converter to be fully blocked. The time it takes for the converter to successfully block the fault current (t_{block}) can be described by Equation 3.2.1 where t_0 is the time of fault occurrence, Δt_{detect} is the detection time and x is the time it takes for the SMs to block the current. [26]

$$t_{block} = t_0 + \Delta t_{detect} + x \tag{3.2.1}$$

In [26], the detection time is assumed to be 6 µs, while the time for the SM to successfully block is assumed to be 0.5 ms, which gives $t_{block} = 0.506$ ms.

Experimental Protection Scheme for HVDC Converters Against DC-Side Faults With Current Suppression Capability

A new protection scheme for HVDC converters against DC-side faults with current suppression capability were proposed in 2014 by [12]. The paper proposed a solution to limit the severity of DC side faults by connecting double thyristor switches across the semiconducting devices. "By turning on the thyristors, the AC side current contribution to the DC fault is eliminated and the DC-link current will freely decay to zero." [12]

The proposed solution can be implemented on both conventional 2-level VSC and MMC topologies. [12] It involves employing double-thyristor switches connected across the AC terminals of the HVDC converter, as presented in Figure 3.2.7.

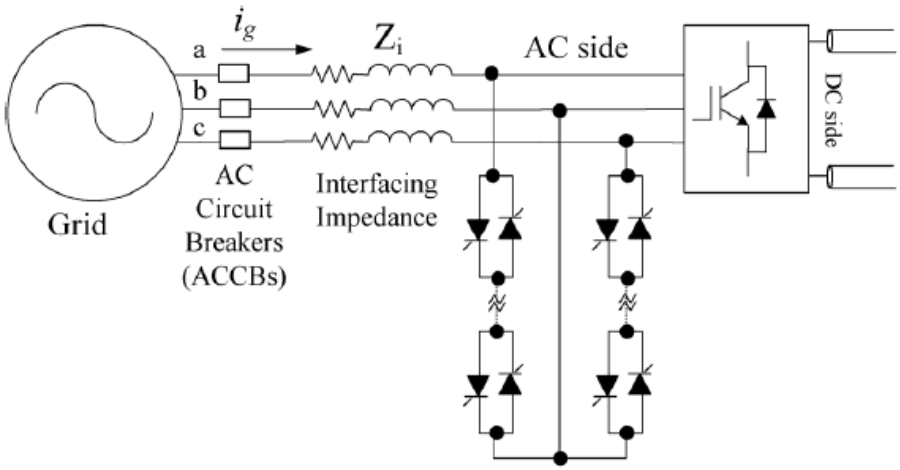
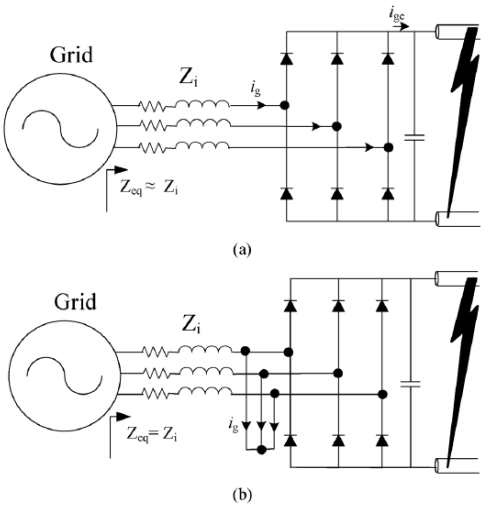
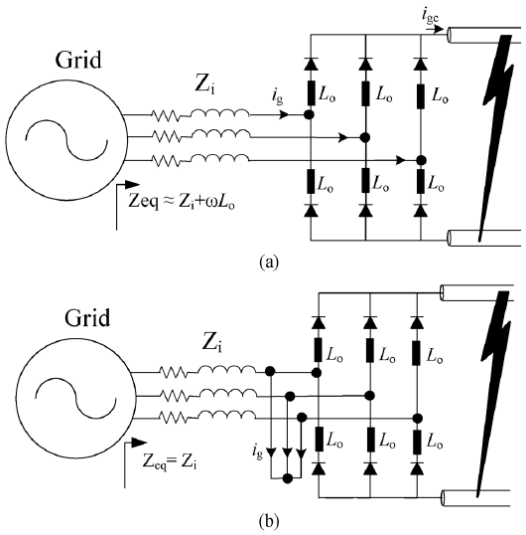


Figure 3.2.7: Experimental protection scheme against the dc-side faults. [12]

During normal operation, the thyristors are turned off such that no current is flowing through them. When a DC fault occurs, the thyristors are turned on to segregate the AC and DC side and thus eliminating the DC side contribution to the fault and allowing the DC-link current to freely decay to zero. The effect of thyristors firing on the equivalent impedance seen by the grid in the case of 2L-VSC and MMC are presented in Figure 3.2.8i and 3.2.8ii, respectively. [12]



(i) Effect of thyristors firing on the equivalent impedance seen by grid for 2L-VSC [12]



(ii) Effect of thyristors firing on the equivalent impedance seen by grid for MMC [12]

In the case of the 2L-VSC, the equivalent impedance seen by the DC side during fault, before and after the thyristor firing is unaffected. As a consequence, the segregation between the AC and DC side is achieved without increasing the magnitude of the AC fault currents. In the case of MMC, the equivalent impedance during DC-side fault after firing the thyristors is lower than its original value, as the arm inductors (L_0) are no longer part of the circuit during faults when utilizing this protection strategy. Since the main function of the arm inductors are to suppress circulating currents and limiting fault currents, and the proposed scheme eliminates the need for fault current limitation, a smaller arm inductor can be sufficient. [12]

The following benefits were found to be achieved with the proposed protection scheme: [12]

- Complete segregation between the AC grid and converter during fault. i.e no current flowing through the freewheeling diodes during fault
- AC currents are not affected by enabling the thyristors
- DC-link current will decay to zero
- Lower dv/dt across thyristors
- Can eliminate the need for expensive and complicated CBs as DC-link current is able to decay freely to zero

Chapter 4

Modelling and Simulations

The content from this chapter end throughout the rest of the thesis is considered as my personal contribution to the thesis and modHVDC project. Detailed description of the Simulink model can be found in Appendix B.

This chapter presents the simulation setup and the overall model structure that are used to obtain the results in Chapter 6. The case study is performed with parameters equal to a nine (N = 9) module machine, that are equally distributed. For simplicity, four modules are applied in the Simulink model as this is adequate for the scope of this thesis. The goal is to investigate module-to-module and module-to-ground faults in regards to fault handling and specifically investigate the feasibility of the proposed bypass solution.

4.1 Simulation setup

The Simulink model is divided into four subsystems, one for each module. When it is referred to "Module" in this thesis, this includes one stator segment and its corresponding converter module. (i.e each stator segment has a dedicated converter) The model is based on the generator setup presented in Figure 4.1.1. As shown, the generator consists of four stator segments, each with a designated converter module that are series connected and equally separated by the ground connection.

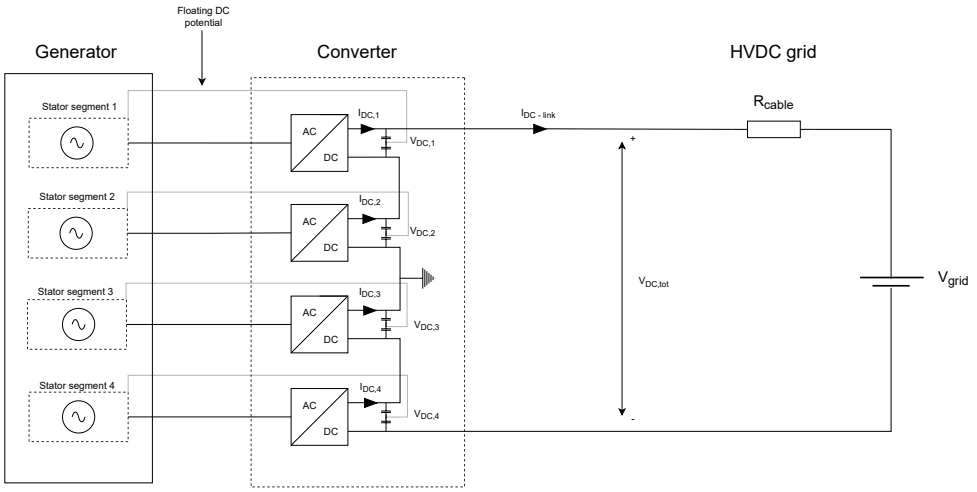


Figure 4.1.1: Model overview illustrating the modHVDC concept with four modules.

4.1.1 Modules

Each of the machine modules are identical in their topology. Figure 4.1.2 illustrates one module, which includes a three-phase source, filter, protection components and a designated 2L-VSC. Each stator segment is modelled as an ideal three-phase sinusoidal voltage source (V_a, V_b, V_c). The three phase source represents the generator windings for one single machine segment. The generator parameters are listed in Table 2.2.1.

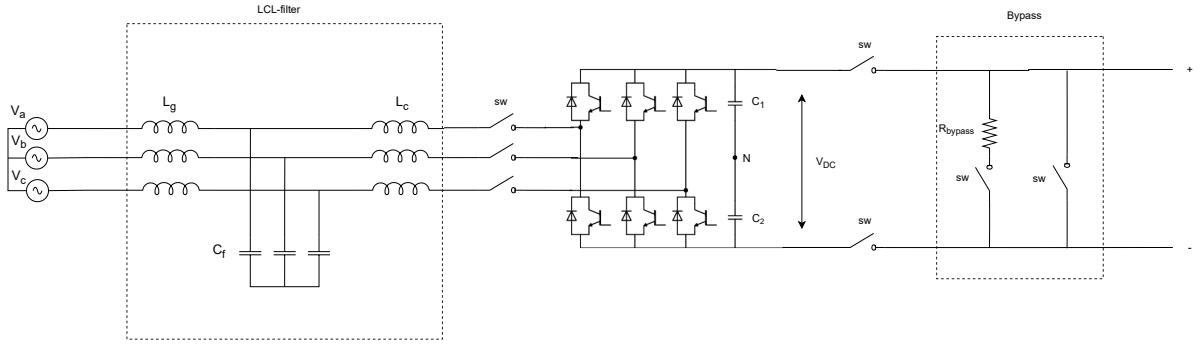


Figure 4.1.2: Block model of one machine segment, consisting of a three-phase source, LCL-filter, converter unit and protection components.

LCL-filter

The filter was implemented to provide sufficient attenuation of current harmonics. The LCL-filter is implemented after the three-phase source. Parameters L_g and L_c represent the generator side and the converter side inductor, respectively, while the parameter C_f represents the filter capacitor. Optimal design of such filters can be a complex procedure involving various constraints, and is seen as out of scope for this thesis. The filter is made with parameters which gives results deemed to be good enough, and is thus not optimized. The filter parameters are listed in Table B.1.4.

Protection components

All protection components (breakers, fuses, switches) are modelled as ideal switches (Sw). The switches representing the fuses on the AC side of the converter are deliberately placed after the LCL-filter in order to avoid stored energy to be discharged, feeding the fault after the switches are opened.

Power Electronic Unit

The converter modules are series connected on the DC-side for achieving HVDC directly from the converter, while the AC side of each module is connected to one generator segment. The switching opeartion of the IGBTs are performed by applying Pulse Width Modulation (PWM). The converter parameters applied in the Simulink model is presented in Table B.1.2.

The model representation of the 2L-VSC is presented in Figure 4.1.3. The topology consist of six IGBTs with anti parallel diodes shown in green, and two DC-link capacitors dividing the voltage equally between them. The gate port of each IGBT are connected to an input block which provides the PWM signals needed for the switching operation.

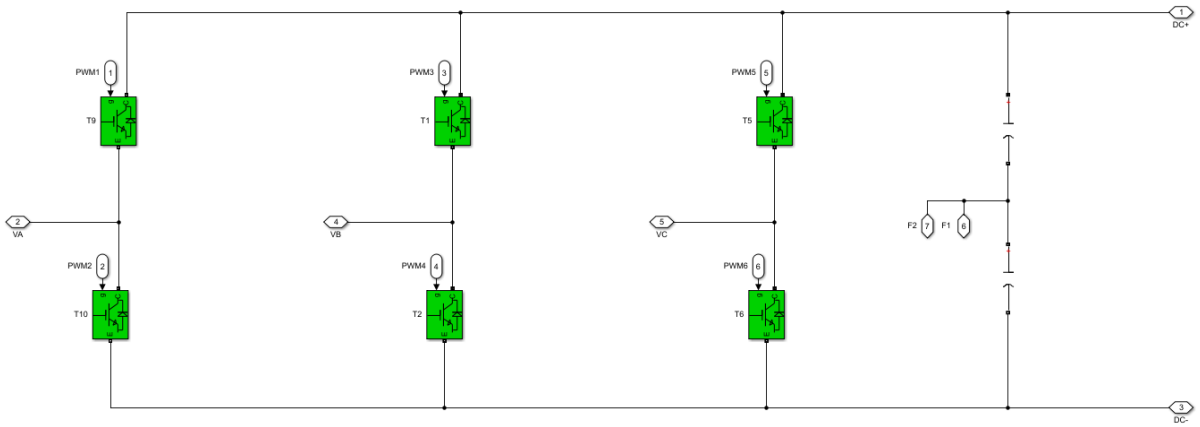


Figure 4.1.3: Model representation of the 2L-VSC consisting of six IGBTs and anti parallel diodes.

Bypass

The proposed bypass solution is designed as a chopper resistor in series with an ideal switch representing an fast acting solid state switch. In parallel with the chopper resistor, an ideal switch is applied to short circuit the module after the stored energy is dissipated in the chopper resistor. The chopper resistor has a value $R_{chop} = 1\ \Omega$ used as a base case if not otherwise is stated.

4.1.2 PWM control scheme

This section will give an explanation of the control scheme for the converter which is presented in Figure 4.1.4. More indepth explanation of the actual Simulink model is attached in Appendix B.

Pulse Width Modulation (PWM) based on synchronous reference frame theory is applied to operate the VSC. Each of the modules have a independent control system which composes of:

- Current controllers
- DC-bus voltage balancing controller
- Droop control

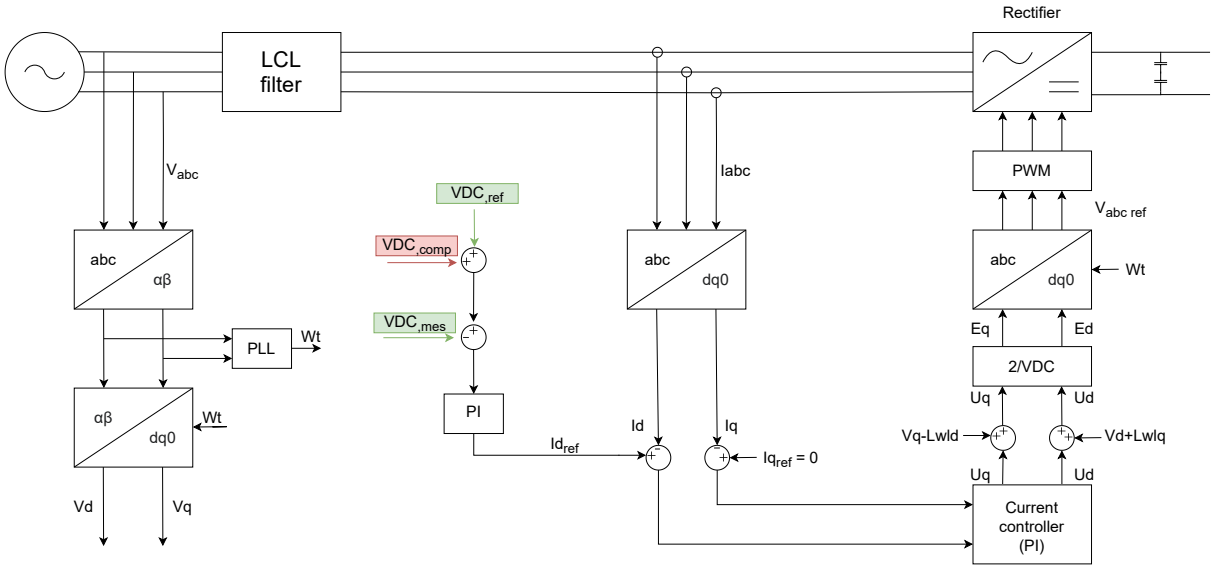


Figure 4.1.4: Control scheme for Pulse Width modulation (PWM).

As shown, the three phase line-to-line voltages are transformed from its abc-values to two-phase alpha and beta values by applying Park transformation. These values are used in the Phase-Locked-Loop (PLL) to obtain ωt. The alpha and beta voltages are then transformed to dq values (V_d and V_q) by performing Clark transformation. The AC current on inverter side is transformed into dq axis components by performing Park transformation.

The reference voltage ($VDC_{,ref}$) is the desired nominal DC voltage output for each converter module. In order for the generator to achieve redundant operation (N-z), the healthy modules must compensate for the loss of voltage potential when a module is isolated from the rest of the system. That is achieved by adding an additional signal ($VDC_{,comp}$). This signal has a zero value during normal operation and is only initiated when a fault is detected. When a fault is detected the signal gradually ramps up to the required voltage level. The sum of the nominal voltage reference and the compensation voltage gives the desired voltage output. The difference between the desired voltage output and the measured voltage ($VDC_{,mes}$) yields the error which is fed to the PI-controller to obtain the correct I_d reference value. The voltage error $V_{DC,err}$ can be described by Equation 4.1.1.

$$V_{DC,err} = V_{DC,ref} + V_{DC,comp} - V_{DC,mes} \tag{4.1.1}$$

Id and Iq is then subtracted from the reference current I_d in order to measure the error. This reference is fed to the PI controller to obtain the d- and q-axis voltages (U_d and U_q). U_d is added to $V_d + L\omega I_q$ to obtain E_q, while U_q is added to $V_q + L\omega I_d$. ω is the angular grid frequency while L is the filter inductor. U_d and U_q are multiplied with 2/VDC to obtain E_d and E_q due to the relations shown in Equations 2.1.1 and 2.1.2, respectively. The voltages E_d and E_q are then transformed to abc-voltages to get the reference for PWM generation, which are fed into the PWM block. Sine PWM (SPWM) scheme with unipolar switching is applied for controlling the switching states of the converter IGBTs.

Droop control/ Voltage compensation

Droop control is employed to ensure the proportional power sharing between the series converters. The voltage compensation $V_{DC,comp}$ must react according to the total voltage drop of the affected modules. As control system design is not the main focus of this thesis, it is assumed that the voltage on the remaining modules increases linearly with a specified slope. This is achieved by adding a ramp function with an saturation limit equal to the required voltage increase, which are added to the voltage reference ($V_{DC,ref}$) from the fault initiation. The slope is defined as shown in Equation 4.1.2 and represents the time it takes for full compensation to be achieved.

$$\frac{dy}{dx} = 0.013 \tag{4.1.2}$$

The voltage compensation that needs to take place during faults depends on the number of modules involved and is calculated with Equation 4.1.3.

$$V_{DC,comp} = \frac{V_{DC,seg} \cdot z}{(N - z)} \tag{4.1.3}$$

4.1.3 HVDC Transmission

The HVDC transmission is simplified for the purpose of this thesis. The cable is represented as a pure resistance (R_{cable}). A stiff grid on the shore side is assumed, holding a constant voltage equal to the desired voltage output. Accurate cable representation is out of scope and thus, the cable model as presented in Figure 4.1.5, is assumed to be sufficient for the intended analysis performed in this thesis.

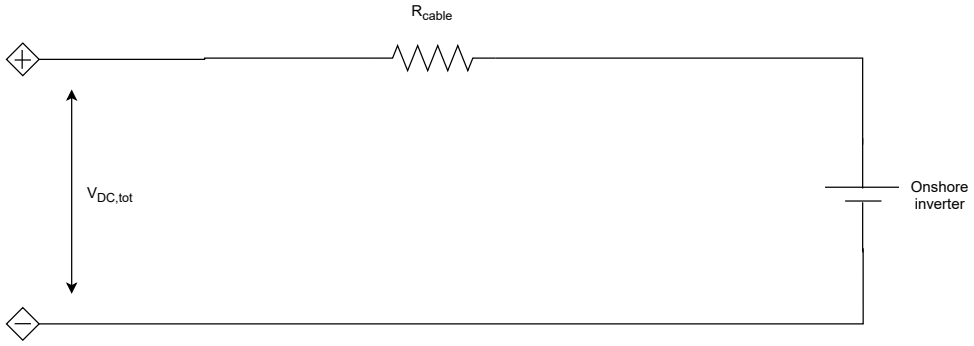


Figure 4.1.5: Simplified HVDC transmission model.

The parameters applied in the HVDC transmission model is listed in Table 4.1.1. The voltage source V_{mmc} has a voltage equal to the total generator output $V_{DC,tot}$ for the model with four modules (N = 4), and the cable resistance is set to 1 Ω.

Table 4.1.1: HVDC transmission parameters.

Parameter	Value	Unit
V_{mmc}	44.4	kV
R_{cable}	1	Ω

4.1.4 Fault initiation

As described in Section 5.1.1, the physical implication of a module-to-module fault is that a connection between the DC-link neutral point of two physically adjacent modules are created. In the Simulink model the fault is initiated by closing an ideal switch which creates the necessary contact. The same logic is applied to initiate module-to-ground faults. Although by closing the switch in this case, a connection between the neutral point of the DC-link of the specific module to ground is created. Subsystems illustrating how the fault initiation is performed in the Simulink model is presented in Figure B.1.4.

4.1.5 Fault parameters

One of the points of investigations performed on the specialization report which was the basis for this masters thesis was to derive the RL fault parameters. [3] These results are used in this thesis and the content of this section previous work, and thus not a part of the work load for this thesis.

When a module fault occur, the current flow through the physical copper connection between the DC-link neutral point and stator iron (floating DC potential). The fault resistance for a module to module fault will consist of the resistance in the stator iron (R_{iron}), resistance in the copper wire (R_{cu}) and the resistance of the arc (R_{arc}). The equivalent resistance can be seen as a series connection as presented in Equation C.0.1. [3]

$$R_{eq} = R_{iron} + R_{cu} + R_{arc} \tag{4.1.4}$$

A FEM (Finite Element Method) model of was created in COMSOL for the specialization project to derive the fault resistance in the iron (R_{iron}) for varying fault locations, fault area and varying number of ground potentials (i.e copper connections to neutral point of DC-link). Figure C.0.2 illustrates the FEM model of two adjacent stator iron sheets. 10 laminated iron sheets per stator segment were assumed, where these are seen as being in parallel as it is assumed that there is an infinite resistance between them.[3]

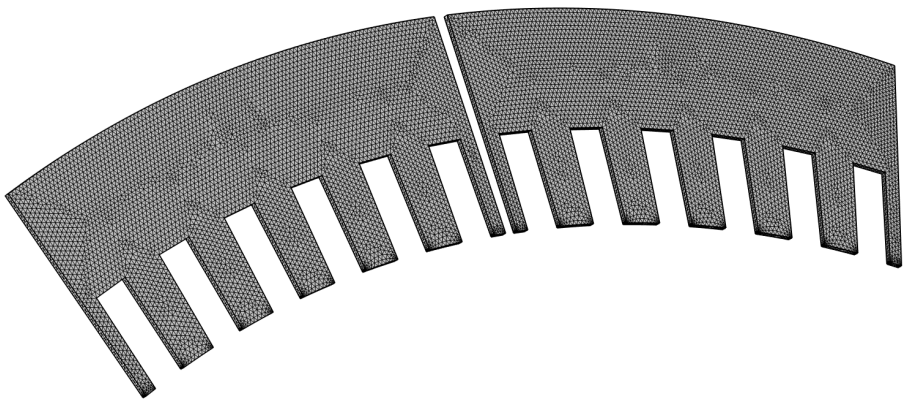


Figure 4.1.6: 3D model of two adjacent stator sheets created in COMSOL. [3]

The copper resistance R_{cu} was derived for a copper length of 5 m and a wire diameter of 5 mm. For the resistance in the arc that will occur between the adjacent modules, Warrington's formula were applied to make an assumption of the resistance, as the resistance is a function of the RMS arc current and thus difficult to derive exactly. [3]

The equivalent inductance (L_{eq}) is assumed to only consist of the self inductance of the copper wires connecting the DC-link and the stator iron. The same wire geometry as for the copper resistance were applied to derive the wire self inductance. The values applied in the simulations for this thesis are listed in Table B.1.5 with more detailed description of fault initiation found in Appendix B.

For a module-to-ground fault the values is assumed to be half of the above given values as this fault only involves one stator module and half the copper length. A more detailed description on how the fault resistance in the iron is derived in COMSOL is attached in Appendix C.

Chapter 5

Faults and Protection Strategies

The modular design of the ModHVDC concept introduces some new failure modes that can occur and thus needs further investigation. [3]

As explained in Section 1.2.1, the stator is divided in modules that are electrically insulated from each other. This introduces the probability of faults (flashover) occurring between these stator modules. Other possibilities are module-to-ground faults and different sequences of faults. There exists no known literature on how to handle these faults and faults originating from the external DC-grid. [3]

Failure modes that needs further investigation is listed below:

- Module-to-module faults
- Module-to-earth faults
- Faults originating from external DC-grid
- Sequence of faults

5.1 Identification of faults

An systematic overview of the different faults that can occur related to the ModHVDC concept was made in the specialization project that represents the basis of this thesis. The content of this section is based on prior work but with modifications and improvements. An overview of the different failure modes that are related to the modules, phases and on the DC-link is presented in Figure 5.1.1. The figure illustrates a stator segment nearest to the positive pole, with corresponding converter module. [3]

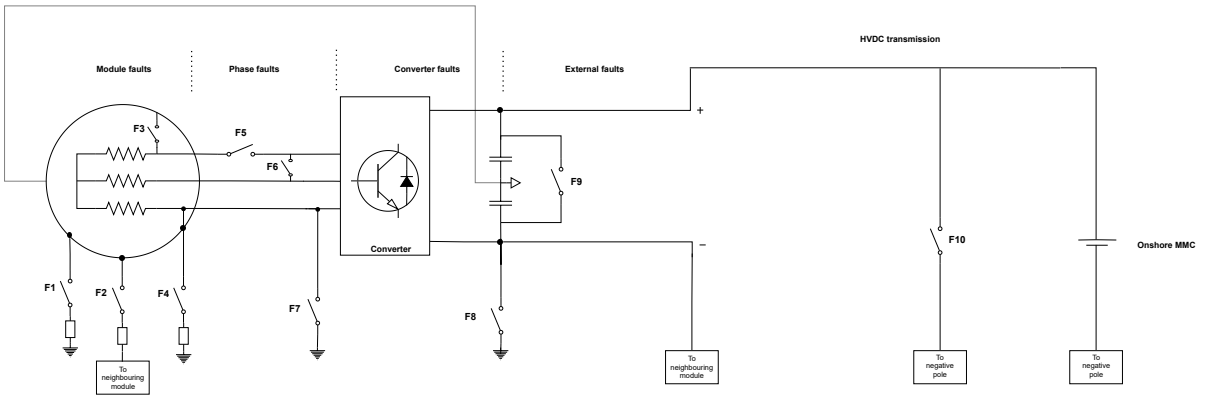


Figure 5.1.1: Overview of the different failure modes that can occur for the modHVDC concept. Illustrated from the perspective of the module nearest to the positive pole. [3]

Three type of faults related to the stator modules are assumed to be probable and must be carefully considered when designing a protection scheme for the modHVDC concept. These are Module-to-ground faults (F1), Module-to-module (F2), Phase-to-module (F3) and a sequence of faults where a short-circuit between the windings and a stator module develops into an earth fault (F4). [3]

Phase faults (AC-side) include phase-open-circuit (F5), Phase-to-phase (F6) and phase-to-ground faults (F7). These faults are not special in regards of the modHVDC concept and are assumed to be handled by conventional methods. [3]

The external faults are earth-fault on DC-bus (Pole-to-ground) (F8), short circuit fault around the DC-link capacitors (F9) and pole-to-pole fault (F10). To accommodate the fault illustration, a nomenclature of the different failure modes shown above are listed in Table 5.1.1.

Table 5.1.1: Overview of the failure modes that can occur in the generator and rectifier. [3]

Nomenclature	Type
F1	Module-to-Earth fault
F2	Module-to-Module fault
F3	Phase-to-module
F4	Phase-segment-earth fault
F5	Phase Open-circuit
F6	Line-to-line short-circuit fault
F7	Single Line to ground fault
F8	Pole-to-Ground fault
F9	DC link capacitor short-circuit fault
F10	Pole-to-Pole fault

5.1.1 Circuit analysis

In this section, an analytical circuit analysis of module-to-ground and module-to-module faults are presented. It must be noted that the analysis is based on a system with the 2L-VSC converter technology which affects the system fault handling capabilities.

Module-to-ground faults

With the series connection of stator modules, the fault current will depend on the discharge current of the involved capacitors and the AC-side contribution. Hence, the fault loop current for a module-to-ground fault will depend on which module to fault occurs on. The ground connection on the DC-side divides the total number of modules. Consequently, if a module-to-ground fault occurs at module 1 as shown in Figure 5.1.2 a), Module 2 and 3 will also contribute to the fault. On the other hand, if the fault occurs at the module 3 as shown in Figure 5.1.2 b), only this module is affected as there is no other modules between itself and the ground connection.

As each module has a physical connection to the neutral point of its DC-link (copper wires), when a module-to-ground fault occurs, a connection between the DC-link and ground is established. The fault loop (light blue) is modelled as an equivalent resistor and inductor to represent the resistive and inductive element of the stator iron and copper wires.

Due to the lack of DC-fault handling capability (freewheeling diodes) of the 2L-VSC, the AC side of the affected modules will feed the fault (dark blue current) until some breaker operation is performed, separating the AC side from the rest of the system. This means that high over-currents will occur on the AC side of all affected modules. Hence, the current to earth depends on the number of affected modules.

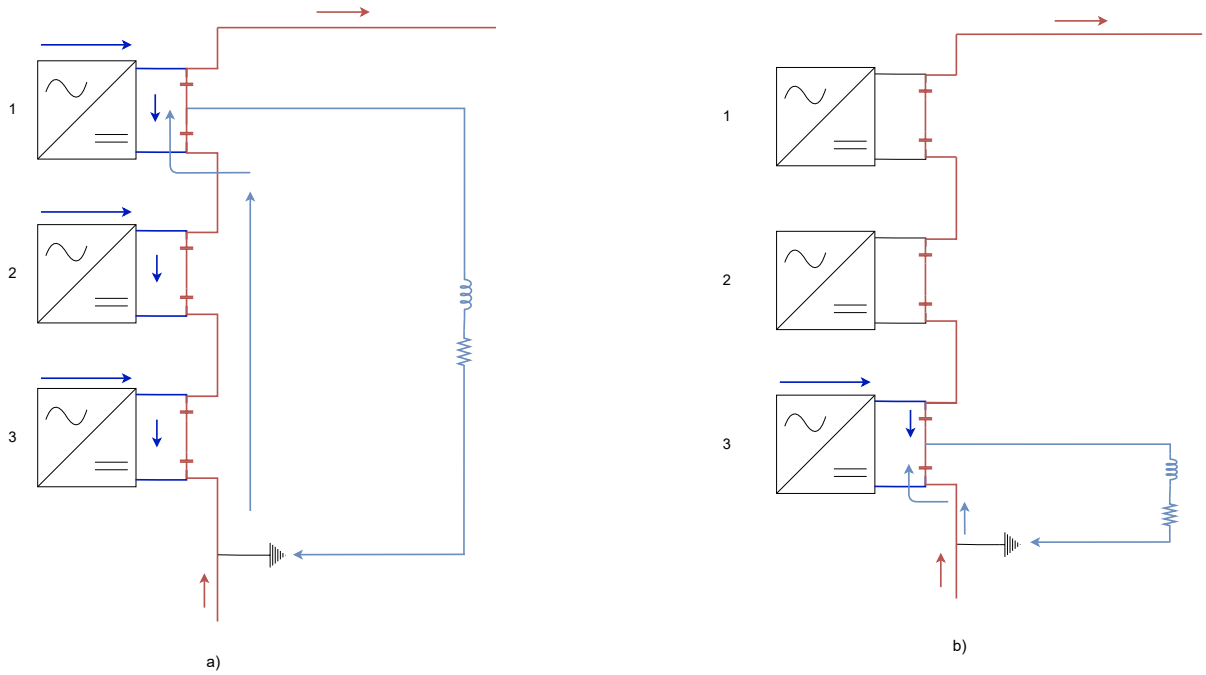


Figure 5.1.2: a) Fault loop when a module-to-ground fault occurs at module 1 with adjacent modules downstream between the earth connection. b) Fault occurs at module 3 with no modules downstream before the earth connection.

When a fault occurs on modules further upstream from the ground potential, the fault voltage consequently increases. This is evident from a) where five DC-link capacitors are involved, whereas in b) only one capacitor is involved. An equation for the total fault voltage in per unit for module-to-ground faults can be generalized as shown in Equation 5.1.1. Where z is the total number of modules involved in the fault.

$$V_{fault,pu} = 1pu \cdot \left(z - \frac{1}{2} \right) \tag{5.1.1}$$

Due to the series connection of modules and the placement of the ground connection (separating the total number of modules), the maximum fault voltage for module-to-ground faults is these faults occurs when $\frac{N}{2}$-modules are involved, where N is the total number of modules. Hence, the maximum voltage potential is given by Equation 5.1.2.

$$V_{fault,max,pu} = 1pu \cdot \left(\frac{N}{2} - \frac{1}{2} \right) \tag{5.1.2}$$

Module-to-module faults

The coarse of a module-to-module ground fault is quite similar to that of a module-to-ground fault. When a short-circuit occurs between two modules, a connection is made between the neutral point of each of the two DC-links through the stator iron and copper wires, creating a closed loop. An illustration is presented in Figure 5.1.3.

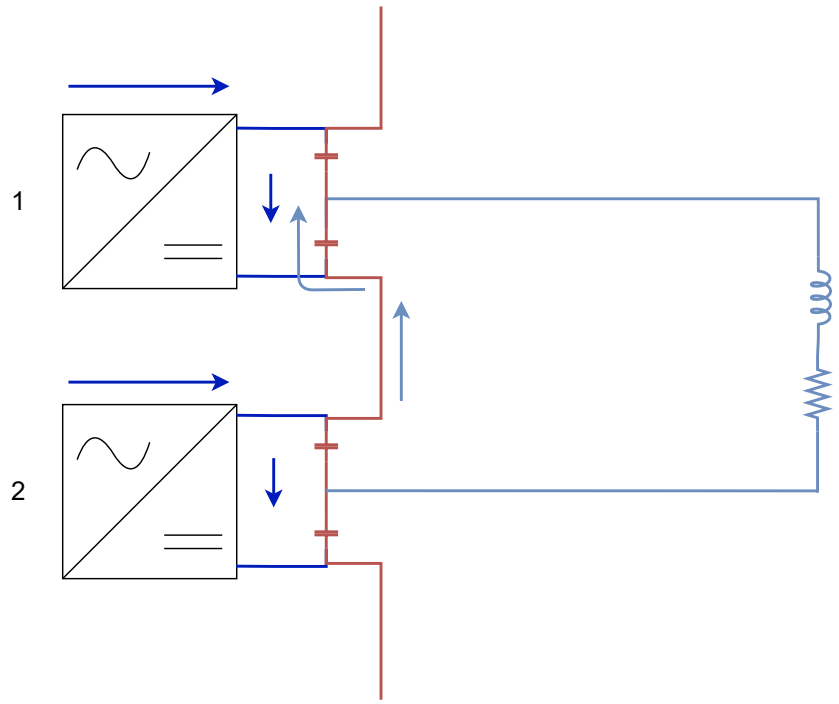


Figure 5.1.3: DC fault loops for a module-to-module fault between two adjacent modules.

In this case, the fault current (I_f) will flow through twice the copper length as it involves two modules. Hence the equivalent resistance and inductance will be double the value compared to a module to ground fault.

Module interleaving

To limit the voltage potential between adjacent modules, a possible solution is to interleave the modules in a order where the integers and odd numbers are separated, as appose to a numerical order from 1-N. An illustration of the system where the order of the modules are interleaved is illustrated in Figure B.1.9. [3]

This method ensures that the voltage potential between physically adjacent modules has a maximum value equal to the DC-link voltage, avoiding the risk of a SC between module 1 and N, where the voltage potential would be equal to the total DC output. Although the interleaving limits the voltage potential, a module-to-module fault with this arrangement results in a minimum of three affected modules. [3]

5.1.2 Summary of fault characteristics

Although there are similarities between module-to-ground (F1) and module-to-module faults (F2), there are also differences that are important to known when planning a protection setup for the machine. The differences are listed in Table 5.1.2 in order to give a summary of the different fault characteristics.

Table 5.1.2: Summary of fault characteristics.

Fault type	**F1**	**F2**
# of affected modules	1 to N/2	3
Max voltage potential	VDC/(N/2)	(VDC/N)*3
Impedance	$Z_g/2$	Z_g

The equivalent impedance seen by the a module-to-ground fault is assumed to be half that of a module-to-module fault as the fault current flow through only one stator segment and half the copper length.

Module-to-ground

The worst case scenario for module-to-ground faults, is that $\frac{N}{2}$-modules needs to be isolated. Then each of the remaining modules must double their voltage output to compensate for the voltage drop caused by the fault.

$$V_{DC,comp} = \frac{V_{DC} \cdot \frac{N}{2}}{\frac{N}{2}} = \underline{V_{DC}} \tag{5.1.3}$$

A significant design aspect is thus that in order to achieve redundant operation in the case of a module-to-ground fault at either pole (i.e module 1 or N), the DC-link of the remaining modules must be able double their voltage output.

Module-to-module

For module-to-module faults the worst case scenario in regards to how much the remaining modules must compensate depends on the total number of modules as the total voltage is evenly distributed among the total number of stator segments as shown in Equation 5.1.4.

$$v_{dc,i} = \frac{v_{DC,tot}}{N} \tag{5.1.4}$$

The amount of voltage increase the remaining modules must compensate with can be calculated by dividing the segment voltage multiplied with the number of affected modules (z) to the number of active modules (N-z) as shown in Equation 5.1.5.

$$V_{DC,comp} = \frac{V_{DC,seg \cdot z}}{(N - z)} \tag{5.1.5}$$

5.1.3 DC-link discharge dynamics

The DC-link capacitors play a vital role in ensuring a stable DC output voltage and mitigating voltage transients. When the bypass switch is closed as described in the previous section, the stored energy in the capacitors is discharged. The physical implications of this stored energy dynamics and how it can be handled are analysed, and specific DC-link designs are investigated.

Two designs are proposed to mitigate fault current i.e dissipate stored energy from capacitors, so that the faulty modules can be safely isolated from the system.

1. Add DC-link series resistors
2. Bypass with "burn off" resistor

Two approaches are applied in the analysis. First the circuit dynamics are analysed analytically, then the dynamics are analyzed by performing system simulations in Simulink. The limiting factor in regards to the proposals is the heat generation that would occur in the added resistors. In order to investigate the proposed designs, the system dynamics during discharge is analysed. It is assumed that the capacitors are fully discharged after 5τ.

By analysing the circuit for a module-to-ground fault after the bypass switch has been closed, two current loops are identified as illustrated in Figure 5.1.4. The green loop is the new current loop established by the closing of the bypass switch. Note that it is assumed that the AC side is separated when bypass is initiated and are thus no longer contributing to the fault. When the fault case involves multiple modules as is shown in 5.1.4 a), the bypass operation must me performed for all the modules involved. In the case of a module-to-module fault, it is assumed that only two adjacent modules are involved, i.e a maximum of three modules has to be isolated (due to interleaving).

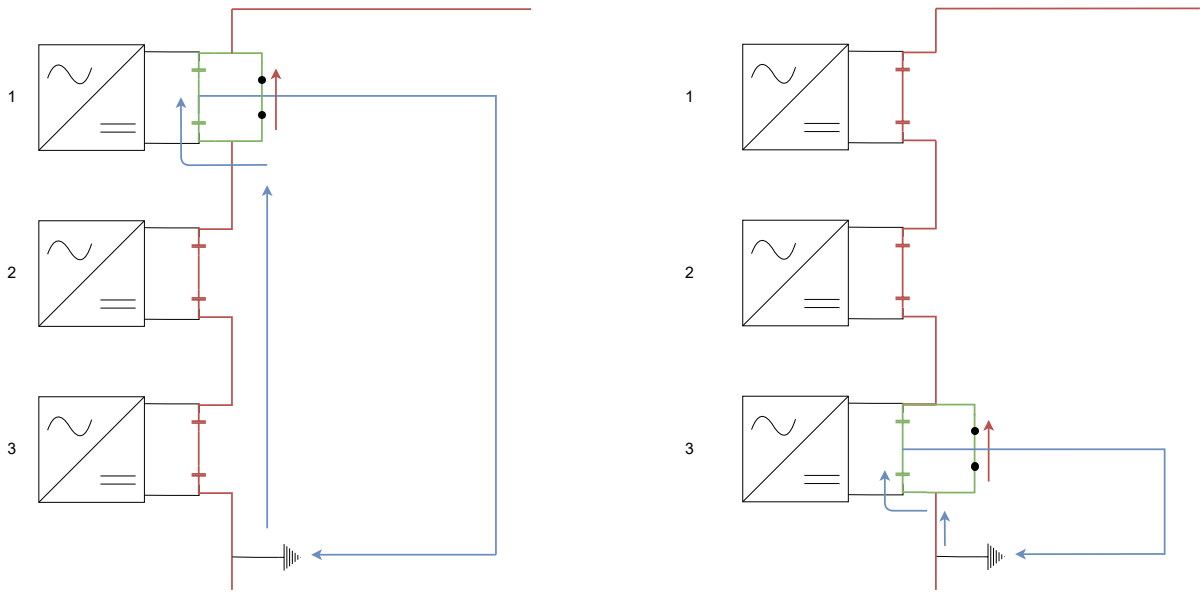


Figure 5.1.4: Current loops after bypass switch is closed. When the bypass is closed a new current loop (green current) is established. The ground fault loop vary depending of the fault location as illustrated here.

The following assumptions constitute the frame of the analytical approach:

1. Fault occurs leading to high AC current feeding fault until fuses blows.
2. Bypass close, creating two closed current loops. Only energy discharged from the capacitors contribute to the green loop, until the energy are burned off in the resistors as heat.
3. DC-link capacitors are the only elements that can store energy, which implies that the energy dissipated as heat in the resistors can not be higher than the amount of stored energy in the affected capacitors at the time of bypass initiation.

Solution 1: DC-link series resistors

The proposed DC-link design with series resistances are presented in Figure 5.1.5. The material dependant series resistance is assumed to be negligible, however the inserted resistance will add to the capacitor ESR. (See Section 2.1)

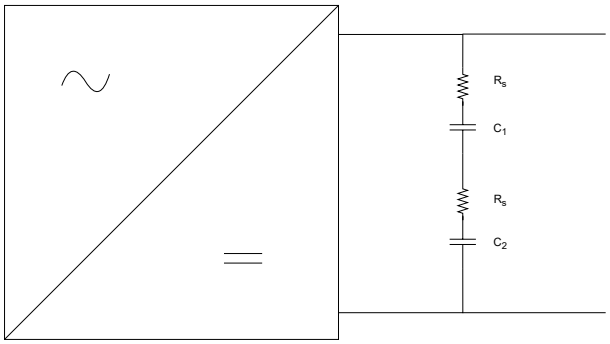


Figure 5.1.5: Proposed DC-link design with series resistances.

By adding the two series resistances (R_s) as shown above, the stored energy will be discharged via these resistances. Consequently resulting in longer discharge time due to higher time constant and heat generation with magnitude depending on resistor size. The two capacitors are in series and hence, the total capacitance is given by equation 5.1.6.

$$C_{tot} = \left(\frac{1}{C_1} + \frac{1}{C_2} \right)^{-1} \tag{5.1.6}$$

The current loops before and after the closing of the bypass switch are illustrated in Figure 5.1.6 a) and b), respectively. When the bypass is closed the green current loop is established and the stored energy in the capacitors is dissipated in the series resistors found in the blue and green current loops.

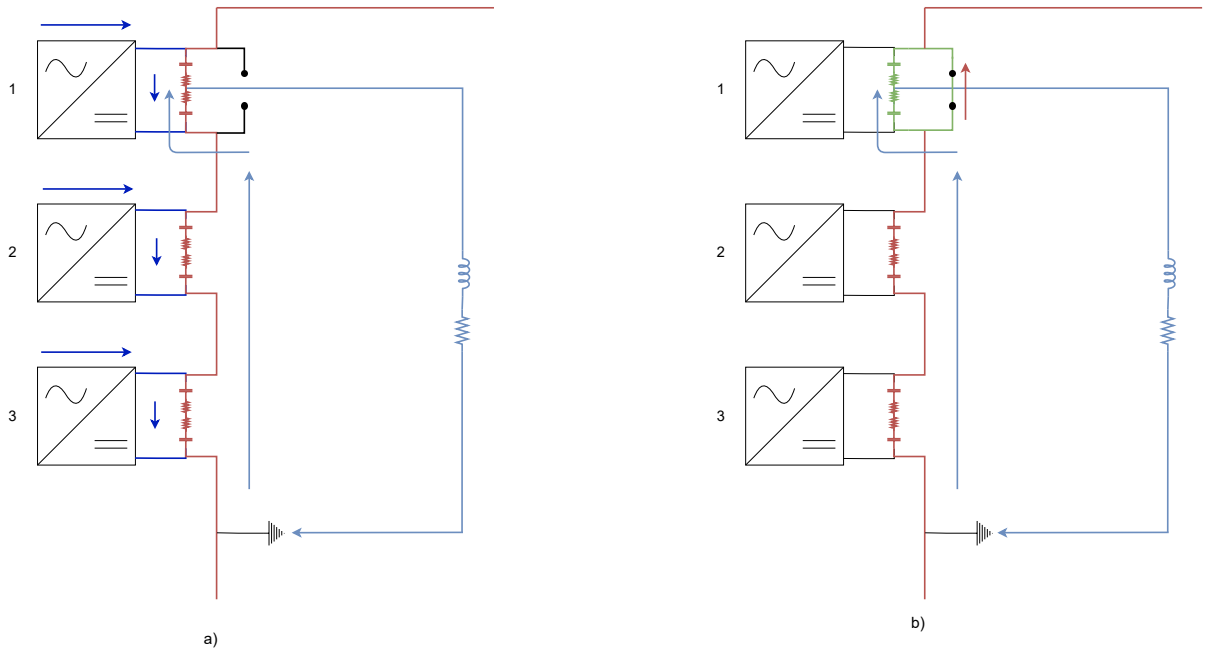


Figure 5.1.6: a) Fault loops for a module-to-ground fault with series resistors before closing bypass switch. b) Fault loops with series resistors after closing bypass switch.

Problems regarding having series resistances in the DC-links:

1. Increasing the time constant. Hence increasing ripple.
2. Additional power loss during normal operation.
3. Increased ambient temperature in DC-link

With two resistors in each DC-link, the total series resistance is thus $2R \cdot N$, where R is the resistance in each resistor and N is the total number of active modules. The active power loss due to the DC-link resistors is found by calculating the I^2R-losses as shown in Equation 5.1.7.

$$P_{loss} = I_{nom}^2 R_{s,tot} = I_{nom}^2 (2R_s \cdot N) \tag{5.1.7}$$

Solution 2: Double bypass

An alternative method of dissipating the stored energy during the fault is to have a power resistor in series with the bypass switch, as illustrated in Figure 5.1.7, to dissipate the excess heat due to the capacitor discharge current. In this case, the bypass needs to have two switches. By first closing switch a), the energy can be dissipated as heat energy in the resistor. The current through the resistor will have contribution from both capacitors and other modules. When the stored energy is dissipated, the resistor must be short-circuited to avoid unnecessary losses, as nominal current will continue to flow through it. This is ensured by closing switch b).

When closing b) it is important to ensure that the DC-link capacitors are fully discharged before short-circuiting the DC-link. When the DC-link is short circuited, the only resistance in the loop are the capacitor ESR which can be very low. By investigating the discharge equation in 5.1.8, it is evident that the combination of low resistance and voltage potential can lead to fast rising and dangerous over-currents.

$$I_c = \frac{U_0}{R} \cdot e^{\frac{-t}{RC}} \tag{5.1.8}$$

The resistor acts as a voltage divider as long as current is flowing through it. Hence, the capacitors can only be discharged to the voltage equal to the voltage drop over the resistor, determined by Ohms law.

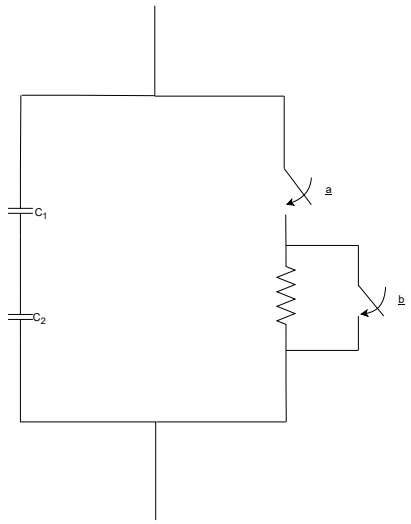


Figure 5.1.7: Bypass switch with parallel resistance for heat dissipation.

The operations of the modified bypass are illustrated in Figure 5.1.8, where in a) both switches are open prior to the AC currents being interrupted. In b) switch a is closed to dissipate the capacitor stored energy. The last operation is shown in c) where the bypass is short circuited after the capacitors are fully discharged, as to avoid high over-currents.

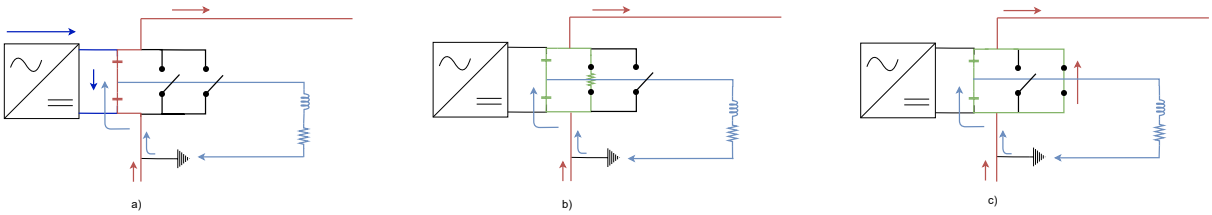


Figure 5.1.8: a) Bypass switches before closing. b) Bypass switch with resistor closes to dissipate capacitor stored energy. c) Bypass is short circuited to avoid unnecessary losses.

The proposed bypass scheme avoids all the negatives related to having series resistances in the DC-link, but at the cost of added complexity to the system. Each converter module will have one extra bypass switch compared to the solution with series resistors in the DC-link. The extra complexity in form of total number of extra switches compared to conventional VSC systems can be generalized as shown in Equation 5.1.9, where N is the total number of converter modules.

$$N_{sw} = 2 \cdot N \tag{5.1.9}$$

5.2 Protection strategy

In this section, a protection strategy for fault detection, mitigation and handling are proposed. The strategy goal is to achieve redundant operation. i.e the system must be able to have continuous operation even if z number of modules are isolated. It is preferred to have a simple and cost effective strategy where passive components are utilized as much as possible. The proposed protection strategy is based on the following characteristics:

- Fault detection
- Fault mitigation
- Fault handling

5.2.1 Proposed protection scheme

The proposed protection scheme constitutes the basis for the simulation model and is presented in Figure 5.2.1, which illustrates protection components related to one stator segment with corresponding converter module (machine segment). The protection strategy is based on that each machine segment is self protected with an independent set of protection.

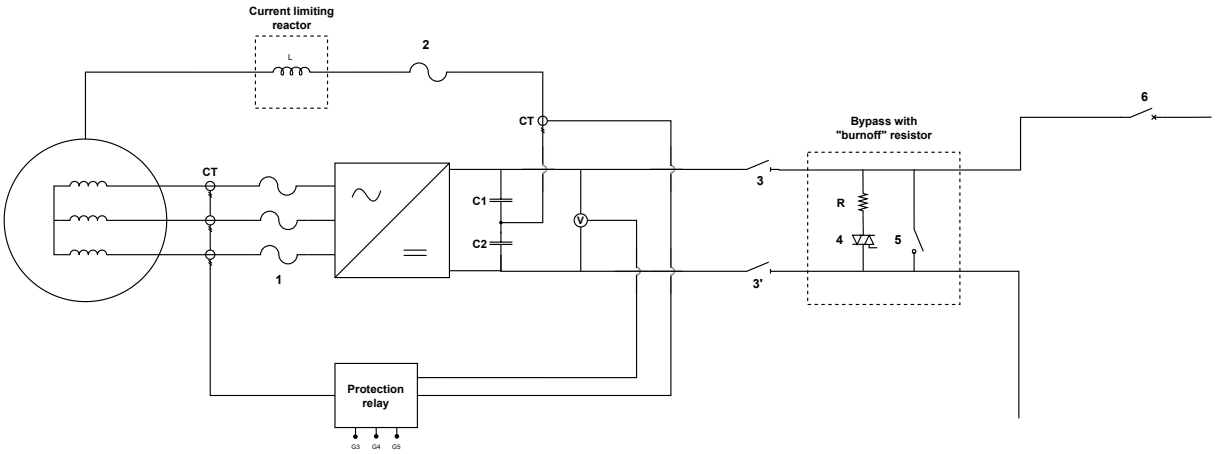


Figure 5.2.1: Proposed arrangement of fuses, breakers and detection components.

5.2.2 Components

In order for the ModHVDC concept to become an competitive option for conventional synchronous machines, the cost is an important aspect. The following points are used as a guideline when suggesting appropiate protection components for the ModHVDC concept.

- Easy and cost effective setup
- High utilization of the power electronics
- High utilization of passive components

Bypass

Based on the circuit analysis of the two proposed bypass solutions, Solution 2 which applies a double bypass is used seen as the most promising solution and thus chosen for further investigation. It is proposed to use a fast acting solid state switch in series with the chopper resistor in order to be able to quickly isolate the faulty module. When the capacitor stored energy is dissipated in the chopper resistor (5) is closed for a full short circuit of the module, creating a new path for the nominal current. After some time the isolator switches (3,3') are opened for a complete isolation of the faulty module.

Detection

The protection philosophy is based on AC- and DC-side overvoltage and over current measurement. Based on the circuit analysis for the investigated failure modes in Section 5.1.1 the following methods of fault detection are proposed:

1. Measure the current through the floating DC potential wires
2. Measure AC currents
3. Measure the voltage over the DC-link capacitors

As in the event of either a module-to-module or module-to-ground fault, the fault current will take the path through the copper wires that gives a physical connection between the DC link and the stator segments, it is suggested to monitor the current flow in each of the floating potential wires for each module. Since such faults also will results in high overcurrents on the AC side, monitoring the AC-side currents is proposed to function as AC-side protection and to validate the before mentioned failure modes. If both CTs detects overcurrents, the fault is validated and the proper action can be taken (i.e initiation of bypass).

It is suggested to monitor the voltage of the DC-link capacitors so that any over/under-voltage can be detected. These values can be fed into a relay which can avoid bypass initiation if the voltage is at unacceptable values (i.e stored energy over acceptable values). Note that the suggestions assumes that the resistor in the proposed bypass solution is able to handle the current heat dissipation that will occur during these faults.

Current limiting reactor

A current limiting reactor is proposed to be placed on the copper wires connecting the stator segment and DC-link neutral point. This proposal is based on limiting fault current peak and di/dt to levels that do not cause damage to the generator.

Switches and breakers

The initial proposal for the protection scheme is done with the cost aspect of the concept in mind. Passive components and components with medium to high response times are assumed to be the most cost effective options. The proposal is done before any simulations have been performed. The feasibility of the proposal is discussed in Section 6.4, based on the literature review and simulation results. The proposed breaker and switching technologies are categorized by their response times, with a rating of high, medium or low. These are listed in Table 5.2.1.

Table 5.2.1: Response time for the breaker technologies applied in Scheme 1.

	High	**Medium**	**Low**
AC side fuses (1)		X	
DC fuse (2)	X		
DC isolator switch (3)			X
Solid state switch (4)	X		
Switch (5)	X		
Hybrid DC circuit breaker (6)		X	

Due to the low inductance value in fault circuit, a current limiting reactor in series with the floating DC potential wires on each of the modules is proposed to limit the rise time and magnitude of the fault current and at the same time lower the requirements of the DC fuse technology. The DC circuit breaker (5) is proposed to act as an backup if isolation of the faulty module should fail (i.e failure of bypass initiation (4)).

Switching sequence

The protection system must be able to handle faults such that components are not damaged by over voltages or currents. The DC-link capacitors are seen as critical components which must be protected from possible breakdowns. Keeping the voltage over them within certain limits is therefor a key goal when performing simulations of the protection scheme.

Chapter 6

Results and Discussion

This section presents the results obtained from the simulations model. Due to the theoretical analysis on bypass design, given in Section 5.1.1, the preferred method for further analysis is to apply the bypass solution with chopper resistor to dissipate stored energy in the capacitors during faults. Simulations with series resistances in the DC-links is also performed and these results can be found in Appendix B.2

The goal of the protection scheme is to ensure that the modules that are affected of a fault are isolated without having dangerously high over- currents and voltages that could increase the risk of unnecessary damage. An crucial aspect of the bypass solution is that the resistor must be able to handle the current (i.e heat dissipation) that will occur during switch on time.

The following aspects are investigated in regards to fault voltage and current, with the main goal to investigate the feasibility of the proposed bypass solution:

1. Optimal breaker response times
2. Optimal breaker sequence
3. Current limiting components

As there is significant uncertainties regarding the applied parameters, the results aim to highlight and give understanding of different aspects that need to be considered when designing the protection scheme and bypass solution.

6.1 Normal operation

Figure 6.1.1 illustrates the AC- and DC-side voltages and currents during normal operation for one stator segment. During startup there is a transient step response, before stationary values are obtained at steady state, which occurs after around 150 - 200 ms. Hence, it is shown that the applied controllers are able to achieve and maintain the required DC output. As the four modules are series connected and identical in their topology, the dynamics during normal operation is also identical.

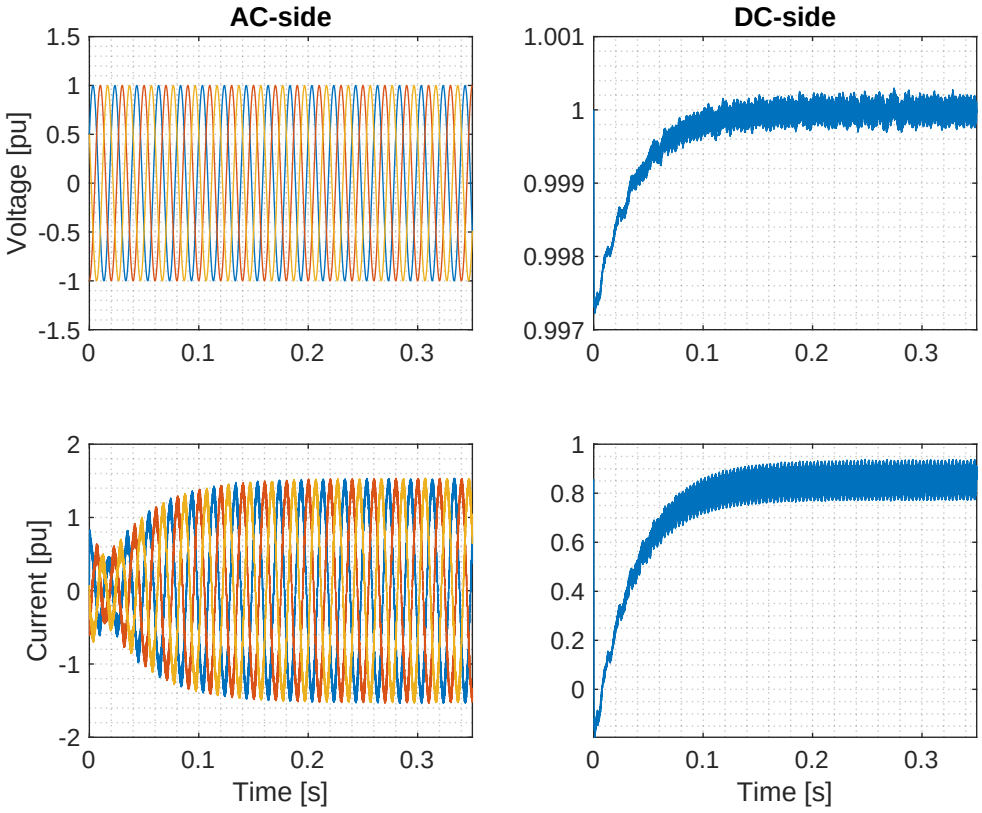


Figure 6.1.1: AC- and DC-side voltages and currents for one stator module.

The AC-side voltages are measured at the generator terminal (i.e adjacent to the voltage sources), the AC side currents are measured to the left of the LCL-filter. DC side current is measured at the positive pole of the DC-link, while the DC voltage is measured over the respective DC-link. The Simulink model of the stator module where this is illustrated is presented in Figure B.1.2.

6.2 Module-to-Ground Faults (F2)

All faults are initiated at steady state. Hence, analysis of faults during startup are not performed. The fault parameters are listed in Table B.1.5. As the goal of the protection scheme is to isolate the faulty module without exceeding dangerous over-currents and voltages, these parameters are investigated in this Section.

For module-to-ground faults, two scenarios are investigated. In Scenario 1, the fault occurs at Module 1 (i.e closest to positive pole) while in Scenario 2, the fault occurs at Module 2 (i.e nearest to the ground connection). These two cases represents the worst and best case for this fault type, respectively.

6.2.1 Module-to-ground fault @ module 1

A module-to-ground fault is initiated @ module 1 at t=0.2s.

Voltage considerations

Figure 6.2.1 illustrates the DC-link voltages at modules 1-4 during a module-to-ground fault ride through. As the ground point equally separates the four modules, both module 1 and 2 must be isolated for this fault situation. The results show that there is a significant voltage drop on Module 1 and Module 2, while there is an increase on Module 3 and Modul 4, immediately after fault initiation. Within the first 2.5 ms, the highest voltage occurs on Module 1 with a maximum value of 1.8 pu.

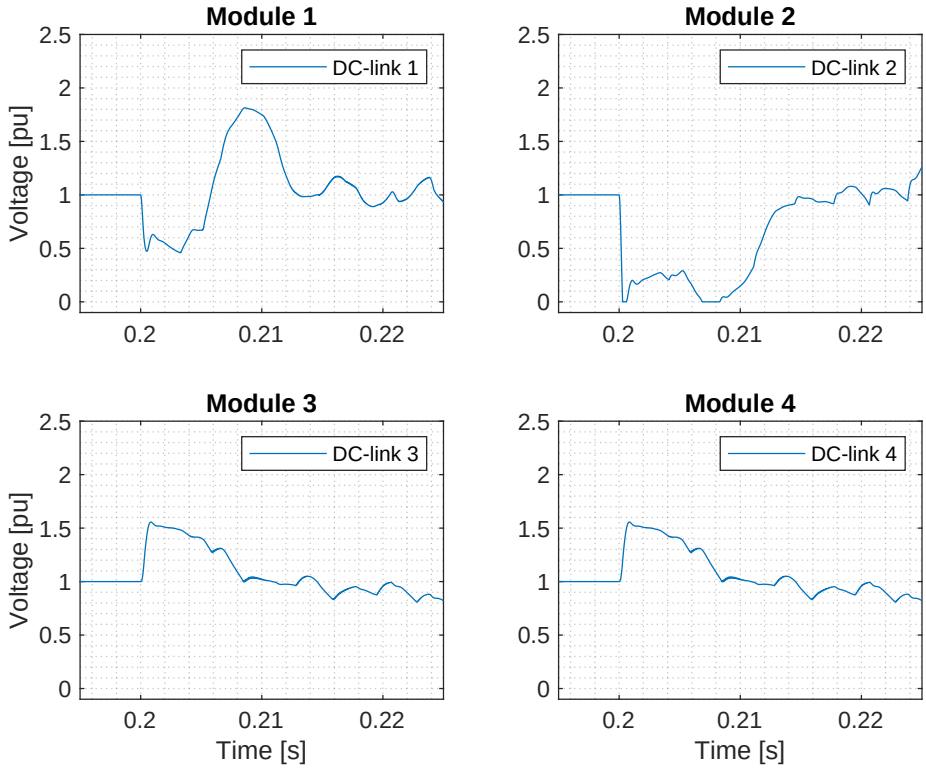


Figure 6.2.1: Total DC-link voltage for modules 1-4, when a module-to-ground fault occurs at module 1.

The voltage course on the modules is as expected as there will be an high fault current seen by Module 1 and 2, which result in a voltage drop on their respective DC-links. The remaining modules increases the voltage to uphold the system voltage balance. To mitigate the capacitor stored energy that needs to be dissipated in the bypass resistor to a maximum of 1 pu, the bypass operation must be initiated when the voltage on Module 1 and Module 2 are below 1 pu. As shown, the optimal breaker response time is not equal for the two modules. As the stored energy in the capacitors is a function of the voltage squared (see Equation 2.1.4), the difference in stored energy between the voltage minimum and voltage maximum at Module 1 is considerable. The minimum stored energy in the DC-link capacitors at this module during the first 22 ms of the fault is around 23 kJ while the highest is around 300 kJ.

Table 6.2.1: Minimum an maximum stored energy in the DC-link capacitors at Module 1 during the first 22 ms of the fault.

Parameter	value	Unit
E_{min}	23	kJ
E_{max}	300 (+1200 %)	kJ

The fault current (I_f) that flows through the stator module to ground during the first 5 ms of the fault is illustrated in Figure 6.2.2. The initial current reaches a peak value of 389 pu within the first 0.2 ms after fault initiation. This current is highly dependant on the RL (R_{eq} and L_{eq}) parameters seen by the fault. The course of the fault current is thus the result of applying the parameters given in Table B.1.5

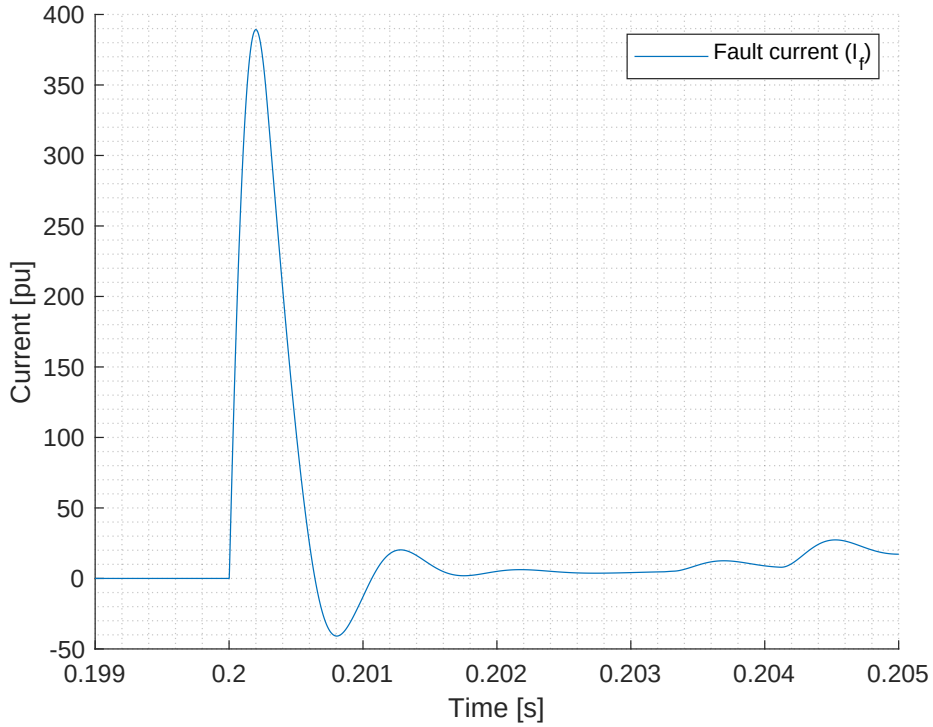


Figure 6.2.2: The initial fault current (I_f) flowing through stator module to ground.

6.2.2 Protection scheme

In the following simulations, it is assumed that the optimal response time for the chopper resistor to be initiated is 2.5 ms after fault initiation, as the DC-link voltage is well below 1 pu for both modules at this time instant. The simulations are performed for varying response times for the AC-side breaking operation.

With the proposed protection sequence, the DC-link voltages will develop as illustrated in Figure 6.2.3, for varying AC fuses response times. The DC-link voltages at Module 1 and 2 reaches zero value within 150 - 200 ms, and in the same time frame, Module 3 and 4 are able to compensate for the voltage drop and stabilizes at 2 pu.

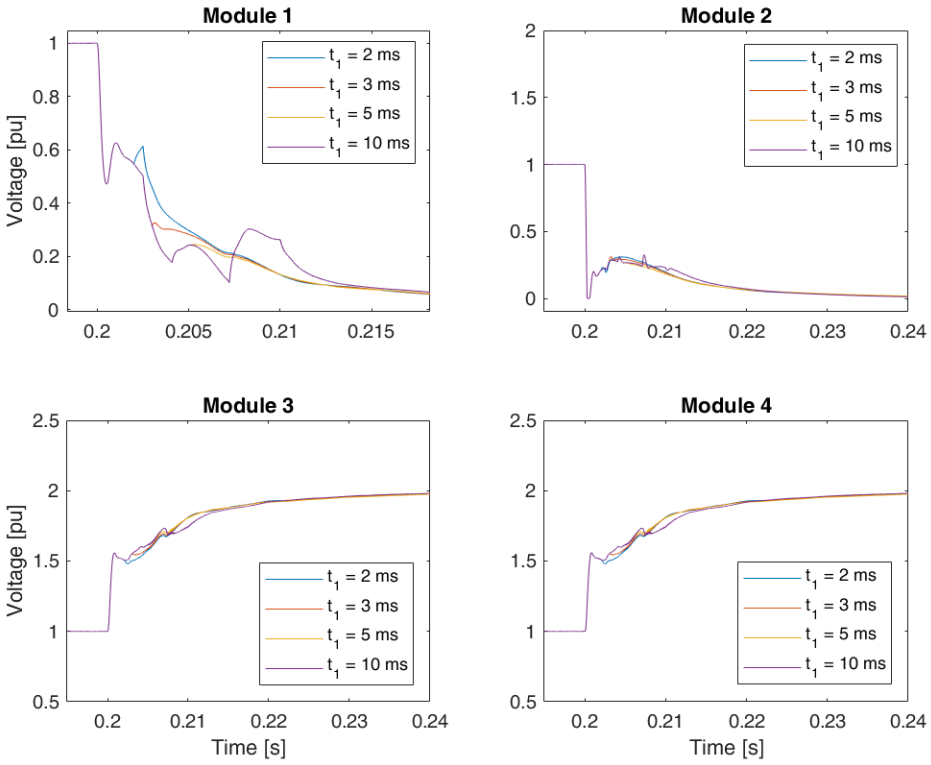


Figure 6.2.3: Total DC-link voltage for modules 1-4, when a module-to-ground fault at Module 1 is cleared with the proposed protection scheme.

The results show only minor differences on the DC-link voltages for varying AC breaking response times. However, small changes in voltages can have significant impact on the stored energy and thus the required heat dissipation.

Bypass heat dissipation

The current through the bypass resistors at the affected modules when the bypass switch is closed, will flow as illustrated in Figure 6.2.4. The initial current peak is governed by the discharge equation for capacitors, elaborated on in Section 2.1. A very high speed initial di/dt occurs due to the low inductance current path. The current has been plotted for different AC-side response times. Ideally, the current through the bypass resistor should be mitigated such that the energy dissipated in the resistor is equal to the stored capacitor energy in the time of bypass closing - Which implies low contribution from the AC-side. If the AC side is able to feed the fault, additional current spikes can occur as shown. However, a long response time did not lead to the highest current peak.

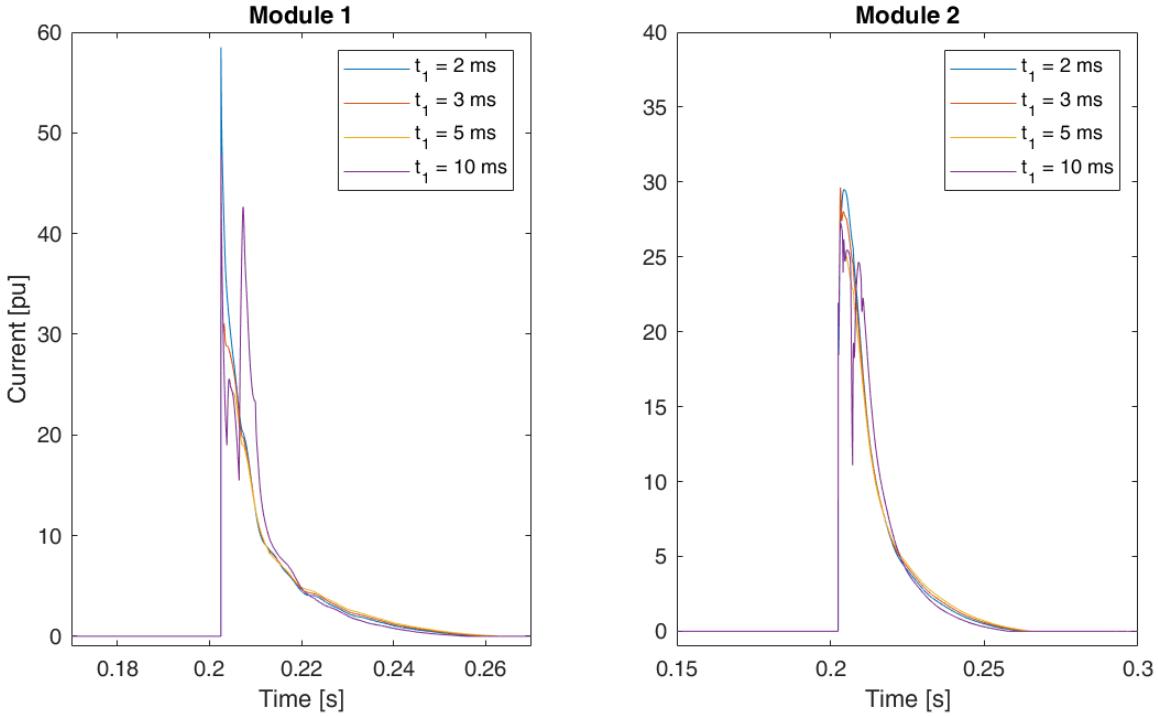


Figure 6.2.4: Current through the bypass resistor of Module 1 and 2.

As shown, the highest current peak occurs for $t_1 = 2$ ms, which is 0.5 ms before the bypass initiation. It can be observed when examining the plot that with lower response time, the current gets closer to the shape of the discharge curve for the capacitors. The time constant stays constant for all situations, as the resistance is consistent. (i.e the discharge time is equal) The corresponding heat dissipation for the different switching operations is presented in Table 6.2.2.

Table 6.2.2: Heat dissipation in bypass resistor during switch on time given in kJ and current peaks given in pu.

	Module 1		Module 2	
Response time	**Heat dissipation [kJ]**	**Current peak [pu]**	**Heat dissipation [kJ]**	**Current peak [pu]**
2 ms	87.0	58.5	87.4	29.5
3 ms	70.1	47.9	83.2	29.6
5 ms	61.2	47.9	74.6	27.3
10 ms	96.7	47.9	86.3	27.3

The highest heat dissipation occurs at Module 1 for an AC-side response time of 10 ms. In this case the aggregated heat dissipation during the fault is 96.7 kJ. This equals a constant power in the resistor of 9.67 kW as shown in Equation 6.2.1.

$$\frac{96.7kJ}{10s} = \underline{9.67kW} \tag{6.2.1}$$

Effect of fault fuse on bypass heat dissipation

The effect of adding additional fuses on the copper connections to break fault current, on the bypass current is investigated. These fuses (t_2) are set to break at the same time as the AC fuses (t_1). The new values for heat dissipation and current peaks are presented in Table 6.2.3, with change in percent.

Table 6.2.3: Heat dissipation and current peak values in bypass resistor during switch on time, given in kJ and pu respectively. Change in percent compared to the results in Table 6.2.2 are shown.

	Module 1		**Module 2**	
Response time	**Heat dissipation [kJ]**	**Current peak [pu]**	**Heat dissipation [kJ]**	**Current peak [pu]**
2 ms	79.8 (-8.3 %)	61.7	56.3 (-35.6 %)	29.5
3 ms	62.9 (-10.3 %)	47.9	54.4 (-34.6 %)	27.5
5 ms	55.9 (-8.7 %)	47.9	52.9 (-29.1 %)	27.3
10 ms	92.3 (-4.6 %)	47.9	67.6 (-21.7 %)	27.3

The heat dissipation in the bypass resistor is significantly reduced when DC fuses on the copper connection are applied. The impact is most predominant on Module 2, as a maximum of 35.6 % reduction is shown, as appose to a maximum of 10.3 % reduction on Module 1. The bypass current peaks are virtually the same for all cases. This makes sense as the current peak is governed by the capacitor discharge equation.

The worst case still occurs on Module 1 for a AC-side response time of 10 ms, and is the case with the least decrease (-4.6%). The heat loss in this case equals a 10 second constant power loss in the resistor as shown in Equation 6.2.2.

$$\frac{92.3kJ}{10s} = \underline{9.23kW} \tag{6.2.2}$$

Current limiting reactor

As an option for decreasing the initial current peak that flows through the stator modules, due to its high speed di/dt and large magnitude, a fault limiting reactor is added in series with the floating DC potential connection as proposed and illustrated in Figure 5.2.1. The current limiting reactor is added in addition to the DC fuse. The results illustrates the effect of this combination.

The simulations are performed with a response time for both DC and AC fuses of 5 ms, with inductance values $L_r = 0$ H, $L_r = 1$ mH and $L_r = 1$ H, respectively. The effect of heat dissipation and current peaks in the bypass is presented in Table 6.2.4.

Table 6.2.4: Heat dissipation and current peak values in bypass resistor with current limiting reactor, given in kJ and pu respectively.

	Module 1		Module 2	
Inductance [H]	**Heat dissipation [kJ]**	**Current peak [pu]**	**Heat dissipation [kJ]**	**Current peak [pu]**
-	55.9	47.9	52.9	27.3
1 mH	50.8	28.4	93.5	51.6
10 mH	60.4	87.9	21.3	19.0
1 H	82.0	95	80.6	94.5

What is shown from these results is that mitigating the fault current that flow through the stator modules does not necessarily decrease the energy dissipation or current peaks in the bypass. For $L_r = 1$ mH, the heat dissipation on Module 1 decreases, while it is significantly increased on Module 2. For $L_r = 10$ mH, the opposite is true. If the inductive element is large enough, this would lead to a low fault current and consequently a low voltage drop on the DC-links, immediately after the fault. Hence, the stored energy will be higher. It is found that with an inductive element of 1 H, the heat dissipation and voltage peaks are equal to the discharge energy from fully charged capacitors. Figure 6.2.5 illustrates the fault current flowing through the stator segments for varying inductive values.

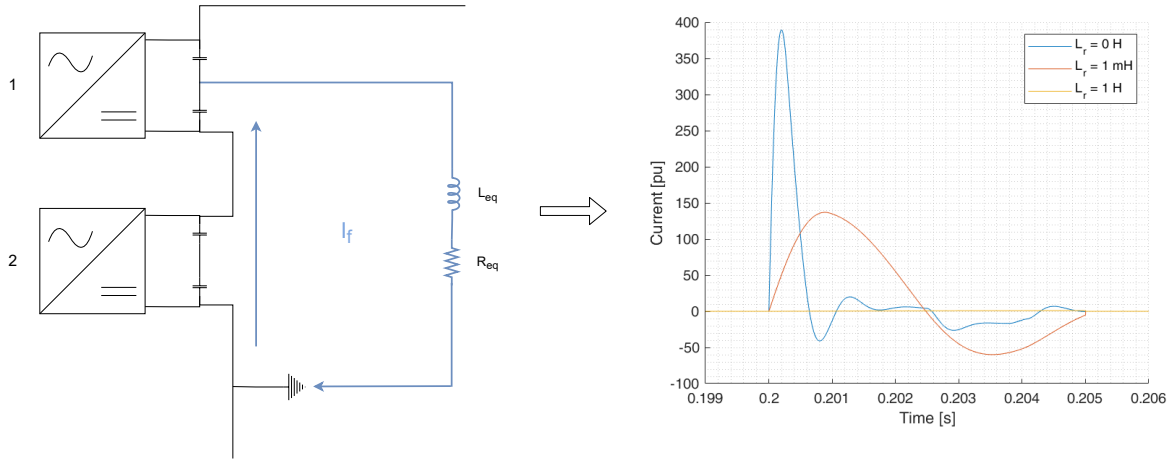


Figure 6.2.5: Fault current flowing through the stator segments for varying inductive values.

The high fault current results in a voltage drop on the affected DC-links. This is favourable in regards to mitigating the energy dissipation in the bypass, but creates problems in regards to fault current and related damage potential to the generator itself. Adding an inductive element as described, will in practice be the same as increasing the equivalent inductance (L_{eq}), described in Section 4.1.5. There is significant uncertainty in regards to the equivalent inductance value that is applied. The fault current can effectively be mitigated with an inductive element as shown, although due to the low or non existent voltage drop on the DC-links faster response times are required to decrease heat dissipation. In all cases shown in Table 6.2.4, the heat dissipation is below 100 kJ, with the worst case being 93.5 kJ. If DCCBs were to be considered instead of a fuse based solution, the current limiting reactor would play an important role to limit the stress on the DCCBs, which is assumed to be required to achieve fault interruption.

Bypass resistor size

Figure 6.2.6 illustrates the change in energy dissipation and current peak in the bypass resistor on Module 1 and 2 during the fault situation. Both energy and current are effectively mitigated by increasing the resistance. However, as the resistance increases there will build up an higher voltage potential over the resistor which caused instabilities for values above 10 Ω. By increasing the resistor value from 1 - 10 Ω, the heat dissipation is decreased by 66.5 % on Module 1 and 62.7 % on Module 2. The current peak is decreased by 85.1 % and 86.6 % on Module 1 and 2, respectively.

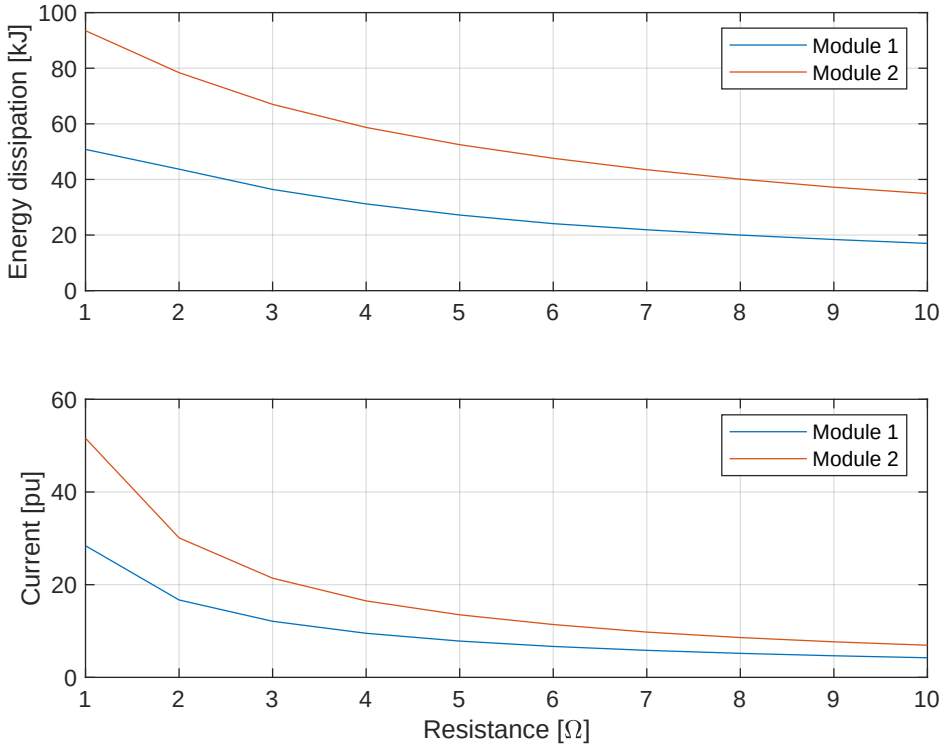


Figure 6.2.6: Effect of varying bypass resistance on energy dissipation and current peak in the bypass resistor on Module 1 and 2.

6.2.3 Module-to-ground fault @ varying locations

Module-to-ground faults occurring at modules nearest to either pole is the worst case scenario for this type of fault. As the voltage potential between the fault location and ground increases when occurring further upstream (or downstream) from ground, the fault current will increase approximately linearly as the change in RL parameters seen by the fault is only minor and the voltage doubles in value for each segment from ground. The simulation model is based on four modules with voltage rating corresponding to a machine with a total of nine (N = 9) modules. This implies that the maximum fault current for a 10 MW, nine segmented machine would be twice as much as the peak value found in the previous simulations, assuming the same parameters seen by the fault. If the equivalent parameters (R_{eq}, L_{eq}) applied in the simulation model is near realistic values, then this show the importance of having a current limiting reactor as a part of the generator concept. The fault current for varying number of involved modules are presented in Figure 6.2.7.

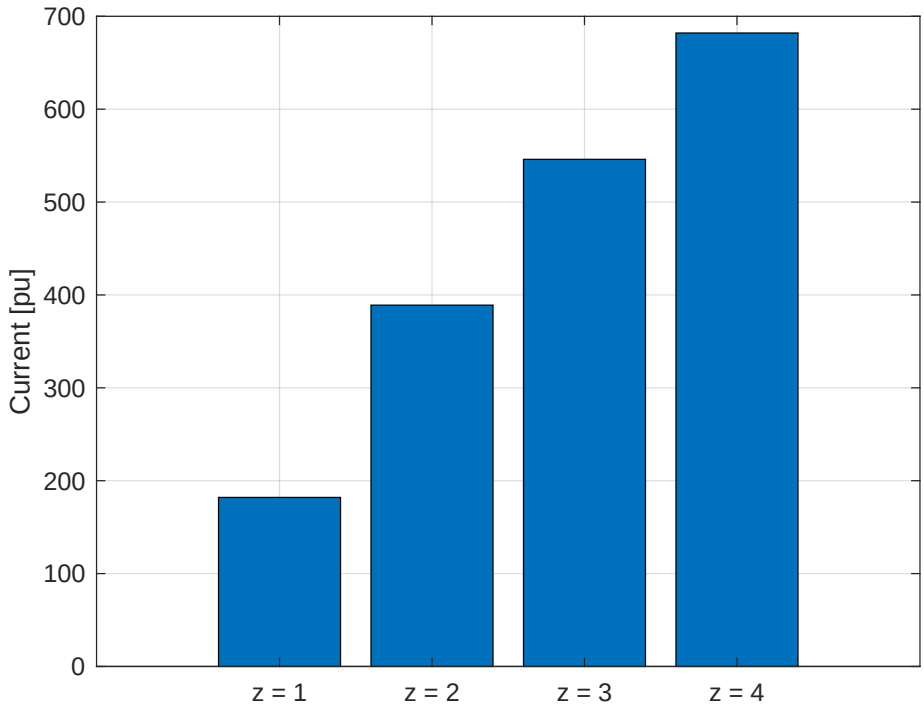


Figure 6.2.7: Fault current (I_f) for increasing number of involved modules for module-to-ground faults.

6.3 Module-to-Module Faults (F2)

A module-to-module fault is initiated at t = 0.2s between Module 1 and Module 3. Due to interleaving, these modules are physically adjacent to each other. All parameters are equal to the parameters used for module-to-ground simulations. The main difference between module-to-module and module-to-ground faults is the impedance seen by the fault and the voltage potential.

Voltage considerations

Figure 6.3.1 illustrates the DC-link voltages on the four modules during the initial 2 ms of the fault, without any protection. As this fault creates a connection between the neutral point of the DC-link on Module 1 and Module 3, they see the same fault, and consequently have the same voltage course. Module 2 is electrically adjacent to Module 1 and 3, and will as a result of the high fault current, experience a instant voltage drop. Voltage on Module 4 is increasing to uphold system voltage balance. It can be seen that the voltage increase on Module 4 is comparable to the aggregated voltage drop on Module 1-3.

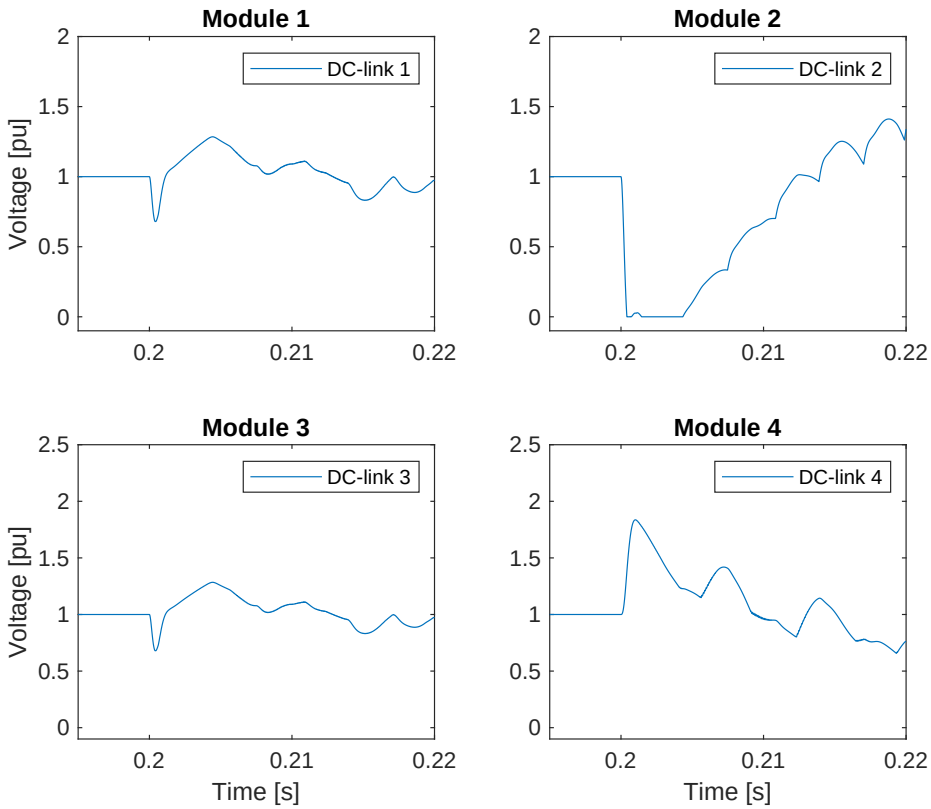


Figure 6.3.1: DC-link voltages on the four modules during the initial 2 ms of the fault, without any protection.

For this failure mode, the initial voltage drop on module 1 and 3 reaches values above 1 pu within 1 ms. Thus, the optimal response time for the bypass operation in this case would be within this time frame. Module 2 has a much more significant voltage drop as both DC-link capacitors are within the fault loop, as a consequence the voltage over both capacitors drop, compared to 1 and 3 where only the capacitors within the fault loop experiences a voltage drop, while the outer capacitors has a voltage increase.

The fault current (I_f) for this fault is compared to the module-to-ground fault current in Figure 6.3.2. The fault current peak in the case of module-to-module faults is 22 % lower and has less transient response. This has to do with the RLC parameters seen by the fault. For module-to-module faults, the current pass through twice the copper length and pass through two stator segments, which increases both the fault resistance and inductance. Based on previously elaborations, this affects the DC-link voltage during the fault and contributes to a lower initial voltage drop.

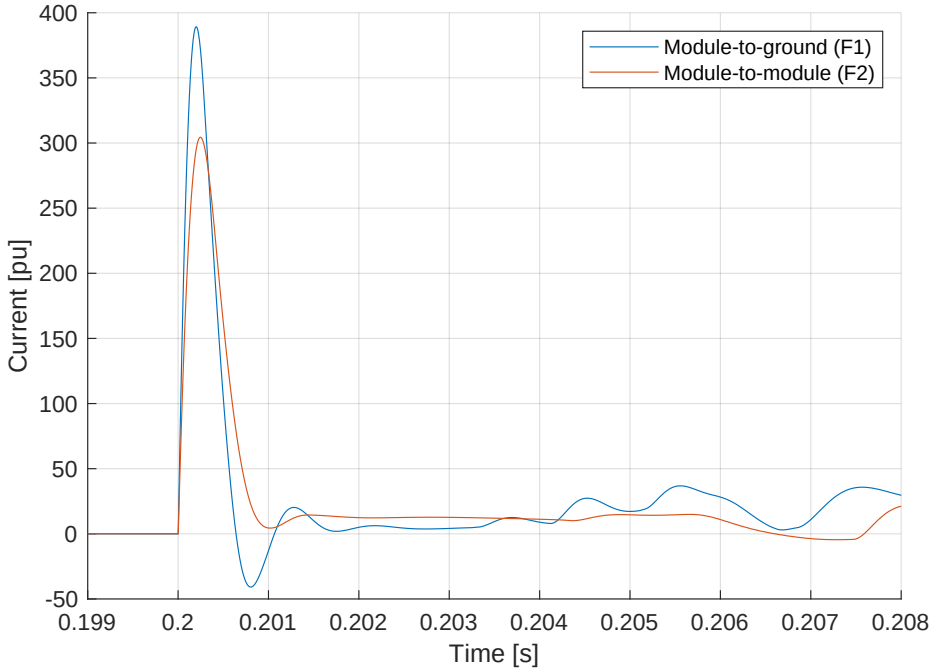


Figure 6.3.2: Comparison of fault current (I_f) between module-to-ground and module-to-module faults.

Due to the interleaving method that is proposed to limit the voltage potential between physically adjacent modules, the voltage potential seen by a module-to-module fault between Module 1 and 3 as shown here (2 pu) will be the worst case scenario for a 100 kV machine with 9 (N = 9) stator segments. Module 1 and 2 are also physically adjacent to each other with this method. A fault between these modules will only have half the voltage potential (1 pu) and as a consequence have a lower fault current than what is illustrated above.

With protection

In the following simulations, the first bypass switching operation is set to have a response time of 2.5 ms, while the AC and DC fuses for the affected module (Module 1, 2 and 3) are set to have a response time of 5 ms. The protection sequence is illustrated in Figure 6.3.3.

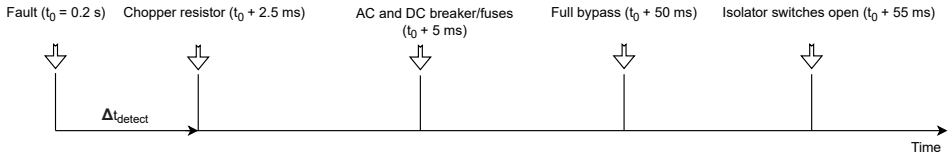


Figure 6.3.3: Protection sequence with AC side breaker and fault current breaker operations being the priority action.

Current limiting reactor is not implemented in these initial simulations. Figure 6.3.4 illustrates the DC-link voltages after the fault when this protection strategy is applied. The plots show the first 25 ms after the fault. Affected modules are isolated (1-3), while Module 4 must compensate by increasing its output to 4 pu. Note that in an actual machine there would be more stator modules, and thus a 3 pu voltage increase on a single module would not be realistic. However, the results show that the control system works as intended.

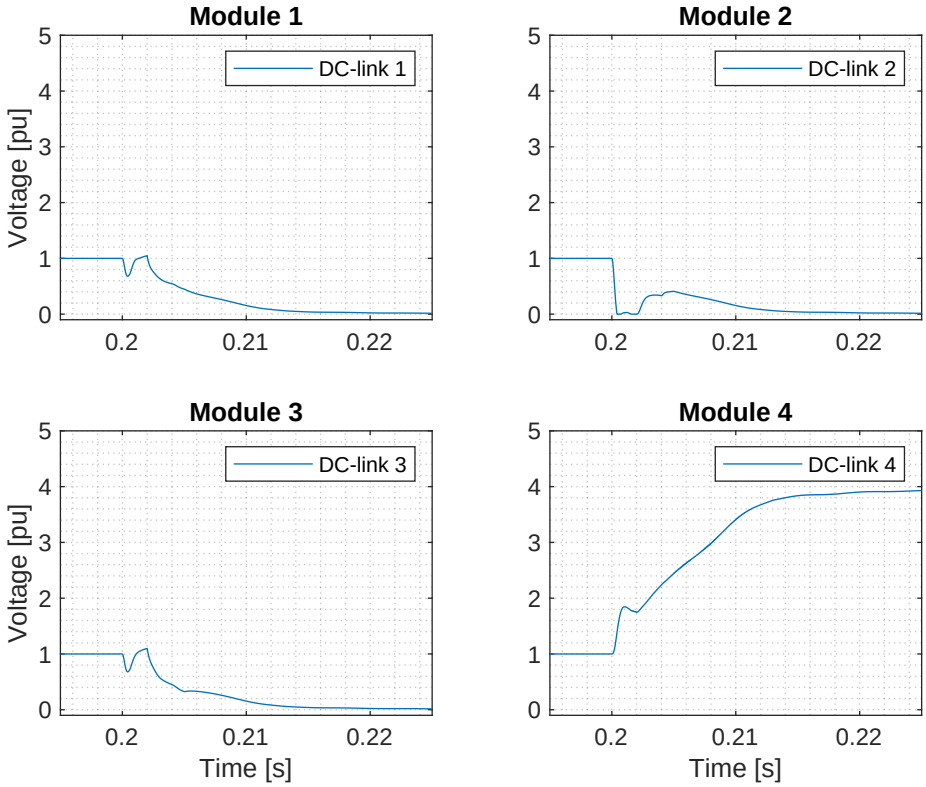


Figure 6.3.4: DC-link voltages after module-to-module fault between Module 1 and Module 3 with protection. Affected modules are isolated (1-3), while Module 4 must compensate by increasing its output to 4 pu.

The heat dissipation and current peak that occurs in the bypass resistor on the affected modules (1-3) are listed in Table 6.3.1. Both heat loss and current peak are identical for Module 1 and 3, respectively. As the fault creates a connection between the neutral point of these two modules, the DC-link voltage course will be the same, as also the fault current will be equally distributed among the two. This means that the stored energy in both DC-links at the bypass closing time is the same, hence equal discharge.

Table 6.3.1: Heat dissipation and current peaks in the bypass resistor during module-to-module fault on Module 1 and 3 without current limiting reactor.

Module	Heat dissipation [kJ]	Current peak [pu]
1	173.6	105.0
2	95.2	42.9
3	173.6	105.0

If the voltages presented in Figure 6.3.1 are compared to the response times that are implemented, it is evident that the bypass on Module 2 will experience less heat dissipation and lower peak current as the DC-link voltage is much lower at the bypass initiation. Compared to the case where a Module-to-ground fault occurs at Module 1, one extra capacitor is involved in the fault, which contributes to a higher heat loss. The heat loss is considerable higher for this module-to-module fault. According to the results in Table 6.3.1, the chopper resistors must handle a aggregated heat loss of 173.6 kJ which equals a constant power loss of 17.4 kW for 10 seconds. The aggregated heat loss in this case is 442.4 kJ.

When adding a 1 mH inductive element also in this case, the results listed in Table 6.3.2 is obtained. The heat dissipation on Module 1 and 3 are reduced by 23.6 % while it is increased by 40.8 % on Module 2. The fault current is reduced to 118 pu, which results in a lower dv/dt on all modules, hence the even heat dissipation shown. The aggregated heat loss in this case is 399.1 kJ.

Table 6.3.2: Heat dissipation and current peaks in the chopper resistor during module-to-module fault between Module 1 and 3 with current limiting reactor.

Module	Heat dissipation [kJ]	Current peak [pu]
1	132.5 (-23.7 %)	77.7 (-26.0 %)
2	134.0 (+40.8 %)	65.5 (+34.5 %)
3	132.6 (-23.6 %)	77.7 (-26.0 %)

On this fault situation, an increase in bypass resistor size caused instability problems. This is assumed to be a consequence of the simple droop control solution that is implemented. However, based on the clear impact shown in Figure 6.2.6 for module-to-ground faults, an similar impact would be achievable also in this situation. Aggregated heat dissipation for all three modules is thus assumed to be mitigated to values well below 100 kJ.

6.4 Proposed protection scheme

The simulation results highlights aspects that need to be considered when designing a protection scheme for the modHVDC concept. However, there are still failure modes that have not been investigated, such as a sequence of faults (F4), which is assumed to be an even worse case then the failure modes that are investigated in this thesis. Thus, a complete and final protection strategy is not presented, but rather an initial proposal based on the investigated failure modes.

Different response times have been investigated for AC-side breaker components and bypass have been tested. The proposed use of fuses have not been validated as a solution that will provide the required protection. It is assumed that the use of fuses as the AC-side protection will require a converter topology that is able to block DC-faults, so that the fuses are applied as secondary protection.

Proposed bypass solution

The following factors are the main aspects to consider when mitigating the bypass heat dissipation:

1. DC-link voltage at bypass initiation
2. Current contribution

Based on the results the initial voltage drop on affected modules during faults, caused by the initial fault current can be exploited to mitigate heat dissipation. Since the stored energy in the capacitors increases exponentially with the DC-link voltage, even a small increase in voltage gives significant increase in heat dissipation. However, since the fault current has such a fast rising di/dt with high magnitude, fault limiting reactors are assumed to be required to avoid generator damage. This will cause over voltages on the DC-links to occur much faster and it it assumed that fast acting breakers with response times in micro seconds instead of milliseconds for the bypass would be necessary to mitigate the heat dissipation close to 1 pu. Design aspects that can be done to mitigate the stored energy is to ensure that the capacitors are not larger than what is required. In regards to the proposed bypass solution, a higher number of stator modules would be favourable, to decrease the voltage potential over the respective modules.

The goal of achieving a system that are able to have redundant operation increases the DC-link requirements. For module-to-module faults the maximum number of modules that will be isolated is three ($z = 3$), due to the interleaving method. Thus, the voltage increase on the remaining modules depends on the total number of modules that the generator is designed for. In the case of module-to-ground faults, irrespective of the total number of modules, a fault at either module nearest to one of the poles would mean that the remaining modules must be able to double their voltage output. This also increases the converter requirements due to the relatively low voltage rating of IGBTs. As described in Section 2.1, the required IGBT voltage rating for the machine parameters in this thesis would require undesirable series connection of converter IGBTs, if the 2L-VSC technology where to be used. Hence, to achieve a system with redundancy the number of IGBT would likely need to be doubled, depending on the voltage rating of the specific IGBTs used. However, this problem is not an issue if MMC converters were to be used.

The considerations above is done with the main focus on mitigating the bypass heat dissipation. An important aspect of the DC-link capacitors is their vulnerability to high $\mathrm{d}v/\mathrm{d}t$ stress. It is shown that the fault current and DC-link voltage stress during faults can be effectively limited by adding an inductive element in the copper connections between DC-link and stator modules, but at the cost of increased heat dissipation in the proposed bypass. Depending amount of heat dissipation that can be allowed, fuses may not be feasible as breaker technology with higher response times may be required.

It is assumed that the feasibility of having chopper resistors as suggested, is only limited by the design aspect. As elaborated on in Section 2.3.3, chopper resistor is related to high costs, specially if additional cooling components is required. Depending on the number of modules, the total volume of the bypass solution could be significant. Also the aggregated heat dissipation must be considered in regards to physical placement of the bypass as high ambient temperature can have negative effects on other components such as DC-link capacitors. In order to fully understand the feasibility of the solution, these aspects must be further investigated. Although specific resistor components are not proposed in this work, the heat dissipation and current peaks in the resistor is mitigated to levels which are assumed to be manageable.

6.5 Control strategy

As the ModHVDC concept is a new system, there is no standard expected control solution for the concept. The proposed control system that is implemented in the model is not necessarily assumed to be the optimal solution as that aspect were not investigated.

One aspect of the system that proved to be challenging during this work was the droop control. When assuming a stiff network on the load side, the system must be able to react to voltage change that might occur, and at a sufficient rate, in order to avoid severe instabilities. The required response depends on several aspects. In the case of module faults, the response depends on both the specific type of fault and number of modules that are involved and needs to be isolated. The remaining modules must increase their voltage output near the same rate as the voltage decrease on the ones that are isolated. The protection sequence and switching response time has an effect on the voltage course and achieving the required response proved to be challenging in regards to module-to-module faults. As the implemented method increases the voltage output to the required level with a fixed rate, it is not able to react to sudden changes that can occur in the period before the modules are successfully isolated, and steady state is achieved. For some protection strategies, severe instabilities did occur which made it impossible to evaluate their feasibility. It is assumed that with an ideal droop control solution these problems would be solved.

The stiff network represented by the grid voltage source becomes the governing source for the system as a whole. When a fault occurs, the stiff voltage source forces the modules to react in order to keep the system voltage balance. At the instant of either of the investigated faults, the generator (AC-side) is forced to ramp up the current and significant transients occurs before achieving steady state again. The current magnitude that occurs reaches values far higher (>30 pu) than what the generator would be able to deliver in reality. This is a consequence of modelling the generator as ideal voltage sources. This will affect the values in terms of magnitudes and transition time. If it is assumed that the

generator currents only would reach magnitudes of 1.1-1.2 pu, then the fault current is mitigated to some extent, thus yielding a lower voltage drop on the DC-link. As a result, this is not necessarily beneficial in regards to the bypass heat dissipation. The transition time from fault occurrence to steady state are achieved is assumed to be quicker. However, the strongest influence is the discharge current from the capacitors in regards to bypass heat dissipation. The smallest heat dissipation does not occur in cases where the AC-side is isolated in the time frame before currents are able to reach unrealistic values. Hence, this issue is still valid for realistic AC-side fault currents. The possibility to implement a way to make the currents saturate at a given value was a solution that was investigated, although an acceptable solution were not found. However, the results points out important aspects and issues that needs further investigation in regards to protection going forward. Figure 6.5.1 illustrates the AC side overcurrent that occurs due to the use of ideal voltage sources. It is shown that the current reaches over 30 pu during the first 50 ms after fault initiation.

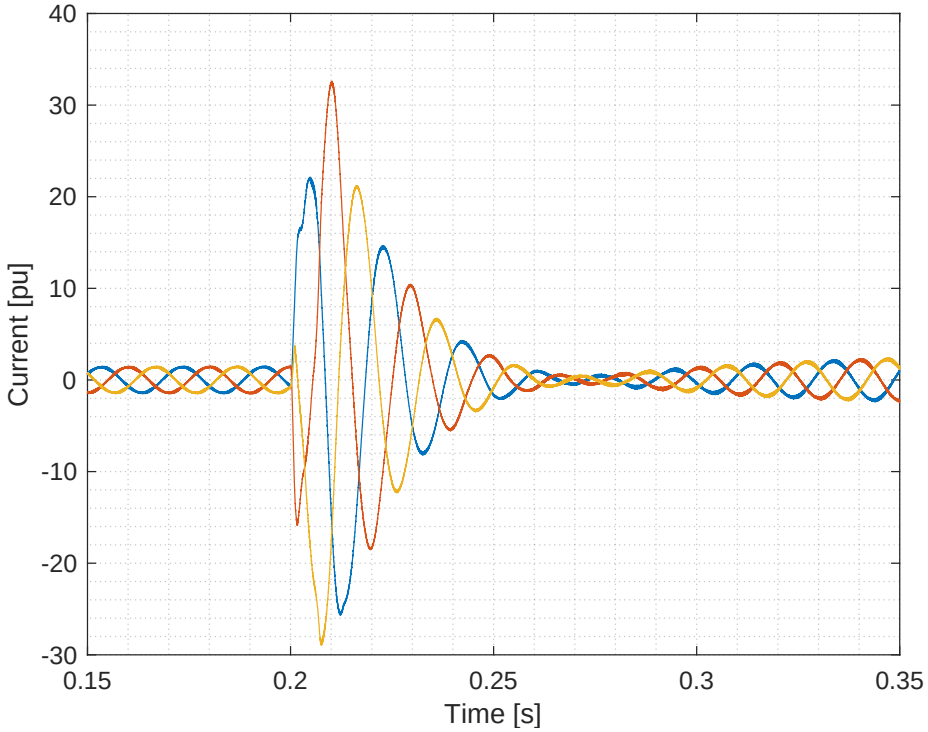


Figure 6.5.1: Illustration of AC-side overcurrent occurring from $t_{fault} = 0.2$ to new steady state operation due to the use of ideal voltage sources for representing the generator.

6.6 Complete shutdown with use of DCCBs

The considerable bypass heat generation and the added complexity and costs that the solution poses are not in favour of this being an optimal solution. To achieve redundant operation for all fault situations would also be an design challenge as components such as DC-link capacitors and converter semiconductor devices must handle the stress of having to potentially double the voltage. If the protection system is able to differentiate between module- and ground faults, then a solution could be to have a complete shutdown for ground faults, while selectivity is achieved for module-to-module faults.

6.7 If MMC technology where applied

As elaborated on in Section 3.1, converters with fault blocking capabilities can have a response time of a few milliseconds. The simulation results could therefor be directly transferred to a case where an MMC converter topology is assumed in contrary to the 2L-VSC topology that the simulations in this thesis is based on. Then the AC side fuses are instead seen as the blocking IGBTs with their respective blocking response time. By utilizing a power converter topology whit DC fault blocking capabilities, one can avoid relaying on fuses or breakers on the AC side for these fault situations. This would avoid the negatives elaborated on in Section 2.3, such as slow response times and the inability to achieve a system restart before replacing the blowm fuses.

An issue that has been highlighted by the findings of this research is that the common DC-link capacitors on the output poses issues in the case of fault situations and the proposed bypass solution, due to significant heat dissipation, added complexity and overall system costs. When deciding upon an optimal converter topology, the solution of choice should inhabit DC-fault blocking capabilities and a topology that do not have common DC-link capacitors, as this would eliminate some of the issues highlighted here.

A lot of research in regards to optimal MMC topologies for HVDC transmission applications have been and are still ongoing. Many of the topologies elaborated on in Section 3.1 have not been tested in real applications and are only theoretically validated. However, to comply with the aim to achieve an cost-effective solution and relatively low complexity, two solutions from the literature review stands out as good candidates for further research in regards to the modHVDC concept. The combination of MMC converter based on half-bridge SMs with the back-to-back thyristor based protection scheme elaborated on in Section 3.2.3 seems like a promising solution that should be further investigated due to low power loss, costs and control complexity of the HB-SMs. The second is to apply Clamp-single SMs which enables HB-structure to achieve DC fault handling capabilities with relatively small added complexity.

The complete protection strategy for the modHVDC concept will depend on several factors such as the type of converter topology used. Thus if an MMC topology where to be applied, this will affect the total protection complexity as different SMs can require different protective solutions.

Chapter 7

Conclusion

This thesis is based on three research objectives which aims to be an foundation into further research regarding detection and protection strategies for the ModHVDC concept. The first objective was to develop a simulation model in the Simulink environment which describes the modHVDC machine with multiple stator segments and corresponding converter modules. Although there is little basis of comparison, the model have been discussed with several professors and considering the stated limitations used, the model is regarded as sufficient for these initial investigations, but the limitations should be prioritized for future work. The use of ideal voltage sources to represent the generator is considered the limitation with the largest impact.

The second research objective was to conduct fault analysis for module-to-module and module-to-ground faults, which were analysed analytically in Section 5.1.1 and from simulations in Section 6. The implications of these fault situations have been highlighted in regards to corresponding over currents and voltages. The results suggests that the natural fault impedance seen by these faults are low, leading to high over currents with high di/dt that can cause severe damage to the generator. Also, the module-to-ground fault is found to be the most severe of the two, depending on fault location.

The third and last research objective was to identify possible faults and propose a protection strategy for the modHVDC concept. A preliminary proposal consisting of detection and breaker components is presented in Section 5.2. The protection strategy is implemented in the simulation model and different breaker sequences and fault mitigating components are tested and presented in Section 6. The main goal was to achieve redundant operation by implementing a bypass solution which isolates the faulty modules while achieving continuous operation of the remaining modules. This was successfully achieved.

The proposed protection strategy provides an initial solution based on the investigated failure modes. As there is additional failure modes that needs investigation, the proposal must be seen as an suggestion for further work. However, the results illustrates the need for a current limiting reactor to limit fault current for the applied RLC parameters. Although at the expense of faster voltage rise time on the affected DC-links. This supports the suggestion of applying a fast acting solid state switch in the bypass in order to mitigate the heat dissipation. The results also supports the proposed use of fuses or breakers on the floating DC voltage connections, as this has a considerable and positive impact on bypass heat dissipation.

Chapter 8

Further work

Due to Covid-19 related restrictions, a lab scale realisation of the model was not done in regards to this thesis. However, this should be a natural next step for further investigation. There are a lot of uncertainties and assumptions in this thesis that should be further investigated and addressed by implementing a lab scale model. Further investigation of the RLC parameters seen by faults in a physical system is required to be able to propose specific protection components. As commercial applied and tested grid resistors relevant for the purpose of the proposed bypass solution were not found when doing research for this thesis, additional research should be performed to conclude on the feasibility of the solution.

The stated limitations that were made in this thesis can act as guidelines for what should be included in further research. In regards to improving the simulation model, this includes applying wind speed and mechanical model instead of modelling the generator as ideal voltage sources which yields inaccurate results as elaborated on in the discussion. An accurate HVDC transmission model should be included, specially if investigating external DC grid faults. Moreover, future work focus on droop control strategies and control strategies overall, as these are aspects that impacts the results in this thesis to an significant extent. In regards to faults, an aspect that was not investigated in this thesis is the possibility to have a sequence of faults, where one fault leads to another and thus having an cascading effect. This could lead to much more severe implications and is recommended to be investigated in further analysis.

In regards to detection of faults and relay settings, only type of measurement and its placement are considered. Thus, a natural next step would be to quantify the detection thresholds and define the pickup settings of the protection relays.

The results quantified the aggregated heat dissipated during the two fault situations. In this regard the next step could be to find out if there exists specific chopper resistor components that are able to dissipate that amount of heat with the corresponding current impulses that occurs during bypass initiation.

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Appendix A

Model parameters

A.1 Per unit system

Table A.1.1: Per unit system on AC-side.

Parameter	Expression	Value	Unit
Voltage	$V_b = \sqrt{\frac{2}{3}} Vac_{seg}$	4.76	kV
Current	$I_b = \sqrt{2} \cdot I_{nom}$	155.6	A
Apparent power	$S_b = \frac{S_{nom}}{N}$	$\frac{10}{N}$	MVA
Active power	$P_b = S_b$	$\frac{10}{N}$	MW
System frequency	$f_b = f_{nom}$	50	Hz
Angular frequency	$\Omega_b = 2\pi f_b$	188.3	rad/s
Impedance	$Z_b = \frac{V_b}{Ib}$	37.5	Ω
Capacitance	$C_b = 1$	1.5e-3	F

Table A.1.2: Per unit system on DC-side.

Parameter	Expression	Value	Unit
Voltage	$Vb_{dc} = Vdc_{seg}$	$\frac{V_{dc}}{N}$	kV
Current	$Ib_{dc} = \frac{3}{4} I_b$	116.7	A
Active power	$Pb_{dc} = S_b$	$\frac{10}{N}$	MW
Capacitance	$Cb_{dc} = C_b$	1.53e-3	F

Appendix B

Simulink model

MathWorks MATLAB-based graphical modeling software Simulink is applied for all aspects of the modeling, simulation and analysis. The model only accounts for the electrical aspect of the generator system. Hence, the mechanical aspect i.e rotor torque and speed are not included.

B.1 Simulation setup

The simulation parameters used in SImulink are listed in Table B.1.1.

Table B.1.1: Simulation and solver parameters.

Symbol	Parameter	Value	Unit
-	Simulation type	Discrete	-
-	Sample time	1	µs
-	Discrete solver	Tustin/Backward Euler	-

Figure B.1.2 illustrates the overall system model with for stator modules, and subsystems for HVDC transmission and fault initiation.

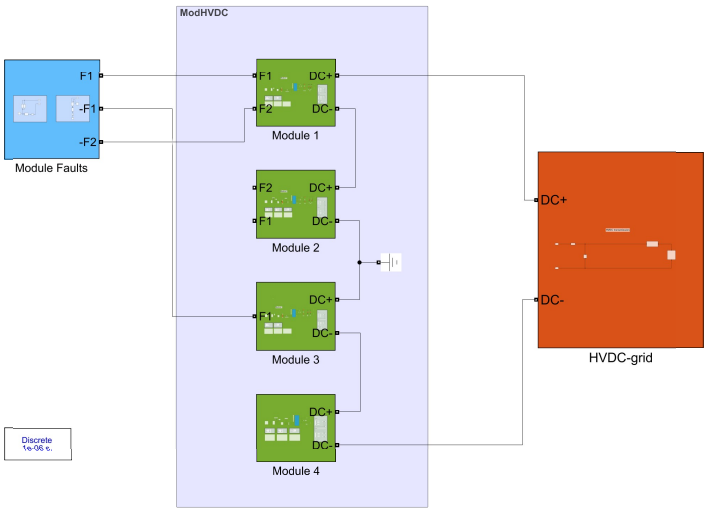

Figure B.1.1: Overall structure of the Simulink model, consisting of four identical stator modules and substructires for HVDC-transmission and fault initiation.

Each stator module are identical in their topology and the simulink model representing them are presented in Figure B.1.2. Each module includes the generator windings represented by the ideal three-phase source, LCL-filter, current and voltage measurement, designated converter module and ideal switches for protection components.

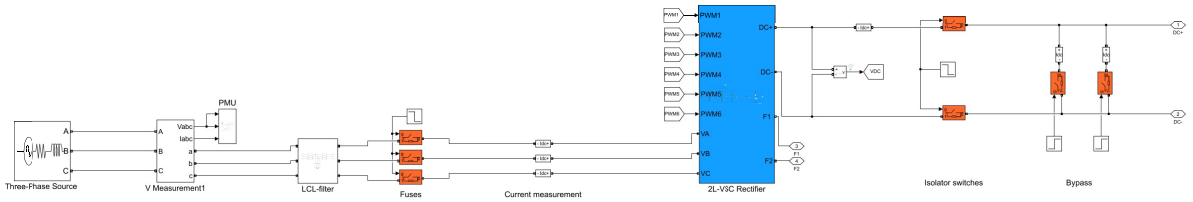

Figure B.1.2: Simulink model of one stator module. This includes the generator windings represented by the ideal three-phase source, LCL-filter, current and voltage measurement, designated converter module and ideal switches for protection components.

The Simulink model representing the 2L-VSC modules is illustrated in Figure B.1.3, where the green blocks represents each of the six IGBTs. The model also includes voltage and current measurement blocks and DC-link with double capacitor splitting the voltage (Capacitor 1 and capacitor 2). Ideal switch (orange) represents the DC fuse on the copper connection between DC-link neutral and stator iron. F1 and F2 are floating connections to the fault subsystems.

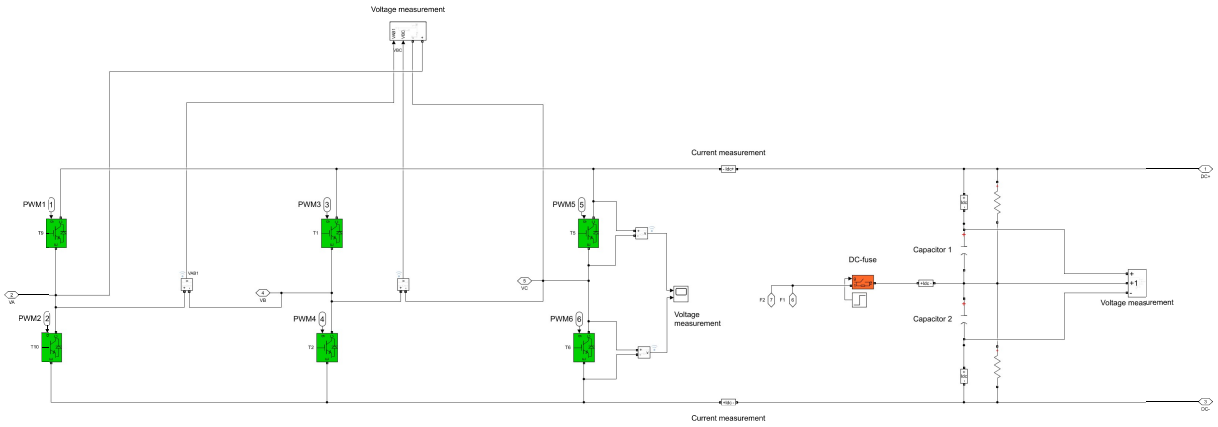

Figure B.1.3: Simulink model of converter modules

The converter parameters are listed in Table B.1.2.

Table B.1.2: Converter parameters.

Symbol	Parameter	Value	Unit
C	DC-bus capacitance	1.5	mF
f_{sw}	Switching frequency	10	kHz
R_S	Snubber resistance	1	MΩ
C_S	Snubber capacitance	inf	F

DC-link

The DC-link parameters used as a base case are listed in Table B.1.3.

Table B.1.3: DC-link parameters.

Parameter	Expression	Value
Capacitance	$C_{DC-link}$	5.6 mF
Initial voltage	$V_{initial}$	5.56 kV
Series resistance	R_s	1 mΩ
Parallel resistance	R_p	1 GΩ

LCL-filter

The LCL-filter is not fine tuned, as this is out of scope for this thesis and do not have impact on the results that are of interest. The applied filter parameters are listed in Table B.1.4.

Table B.1.4: LCL-filter parameters.

Parameter	Value	Unit
Inductors (L1)	500	µF
Inductors (L2)	500	µF
Capacitors (Cf)	100	µH

Fault initiation

Figure B.1.4 illustrates the subsystems used for initiating module-to-module and module-to-ground faults.

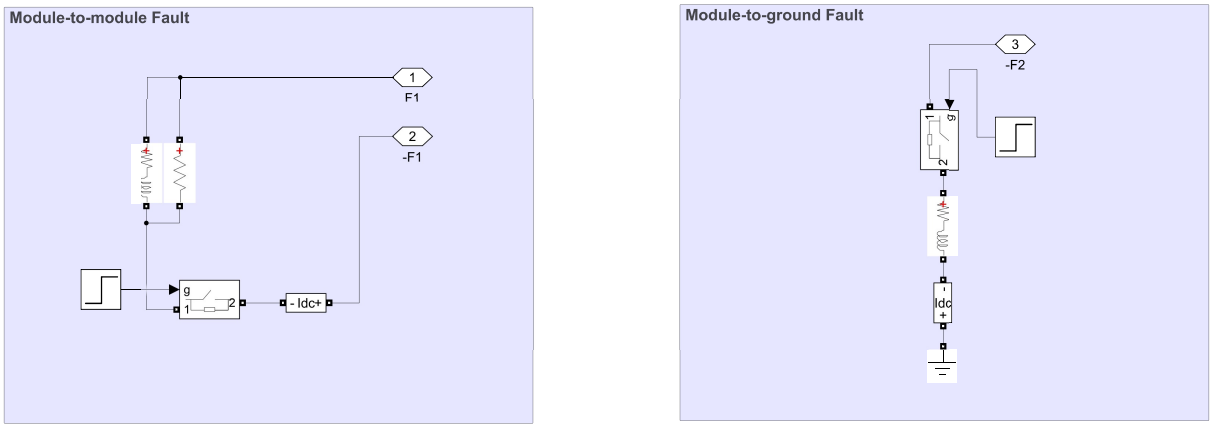

Figure B.1.4: Sub-model of fault initiation in Simulink.

RL-parameters (R_{eq} and L_{eq}) for a module-to-module fault are listed in Table B.1.5. The values used for module-to-ground faults are the same parameters divided by two.

Table B.1.5: RL-parameters seen by fault a module-to-module fault (F1). [3]

Parameter	Value	Unit
R_{eq}	0.2530	Ω
L_{eq}	75.0	µH

Transformation steps

The block diagram for performing the transformation steps from abc to alpha/beta reference frame (Clark transformation) and dq reference frame (Park transformation) are presented in Figure B.1.5.

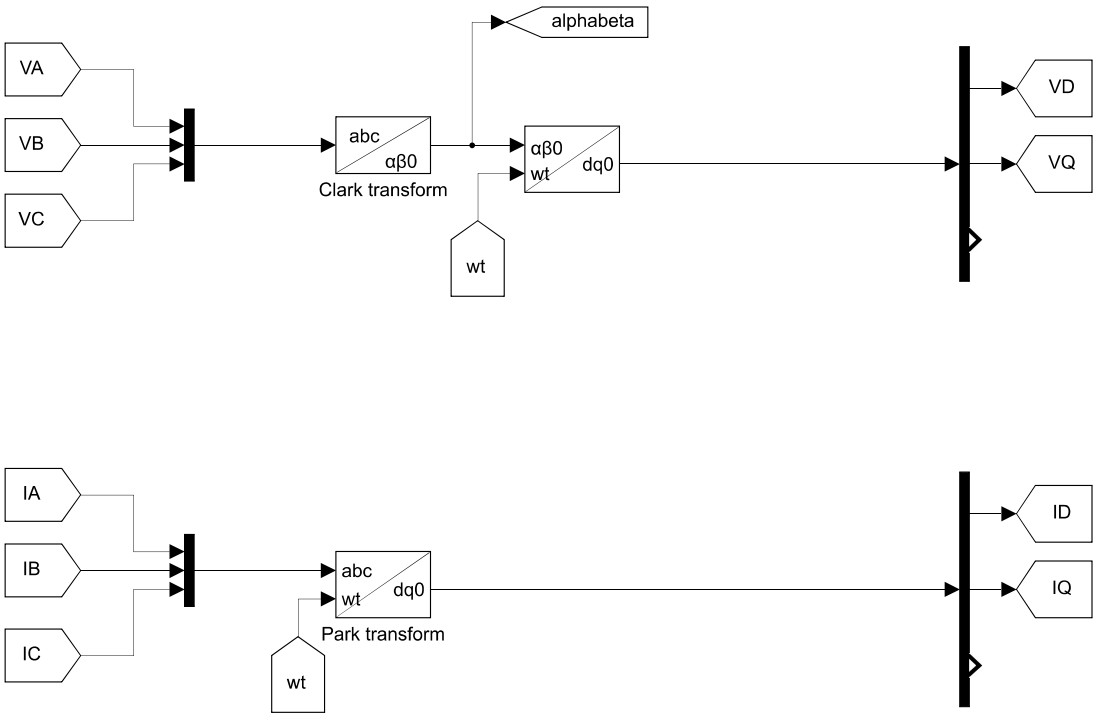

Figure B.1.5: Current transformation steps.

Phase Locked Loop (PLL)

Figure B.1.6 illustrates the block diagram for the PLL used to obtain ωt. The two phase alpha and beta values obtained from the Clark transformation illustrated in Figure B.1.5 are input signals to the PLL.

The PLL is needed to obtain a reference signal that is in phase with the actual voltage. The two phase alpha and beta values are transformed into its the dq reference frame, although only the q-axis component is of interest here. By setting the q-axis reference to zero, it is ensured that the d-axis component is align with the grid voltage. This is illustrated in Figure 2.2.1. The Pi controller keeps Vq equal to zero, while the integrator block is applied to extract the ωt value. A closed loop is created by feeding the output back into the transformation block at the beginning of the block diagram.

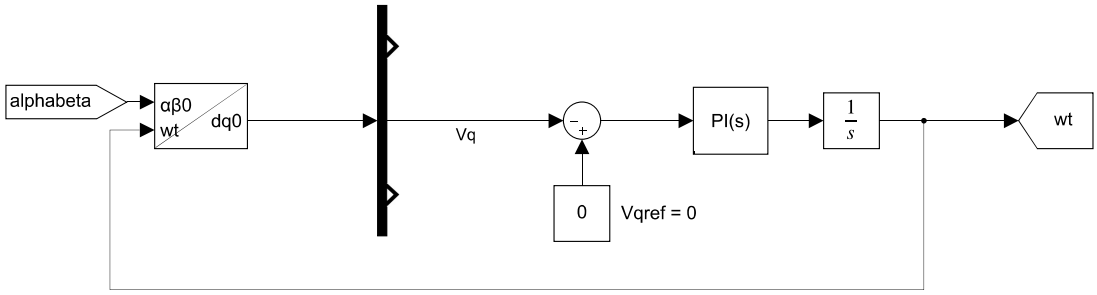

Figure B.1.6: Phase-Locked-Loop for obtaining ωt.

The applied PI-controller parameters are listed in Table B.1.6. The two

Table B.1.6: PI-controller parameters.

Parameter	Value
Proportional gain (Kp)	10
Integral gain (Ki)	50 000

Control

The block diagram that represents the DC-bus voltage controller, i addition to the d- and q-axis current controllers is illustrated in Figure B.1.7. These controllers are used to obtain the abc voltage reference signals for PWM generation.

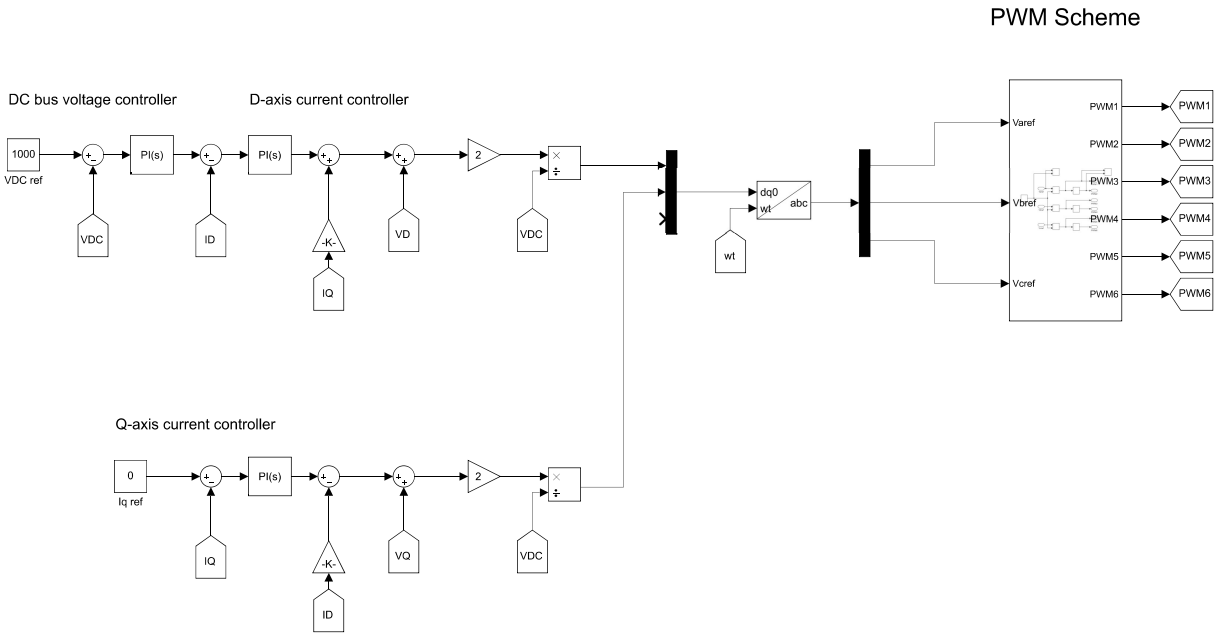

Figure B.1.7: Voltage and current controllers for obtaining voltage reference for PWM generation.

Table B.1.7: PI-parameters for DC bus and current controllers.

Parameter	DC bus	D-axis current	Q-axis current
Proportional gain (Kp)	0.5	25	25
Integral gain (Ki)	200	500	500

PWM scheme

PWM scheme is created by comparing an triangular carrier signal to the abc voltage reference signals, which generates a binary signal (1 or 0) to the gate of the IGBTs. The reference for phase a is used to generate the PWM signal to the two IGBTs in the first phase leg. If the triangular signal is higher or equal to the reference, IGBT1 is activated and IGBT2 is closed, and vice versa. the same logic is valid for the two other converter phase legs.

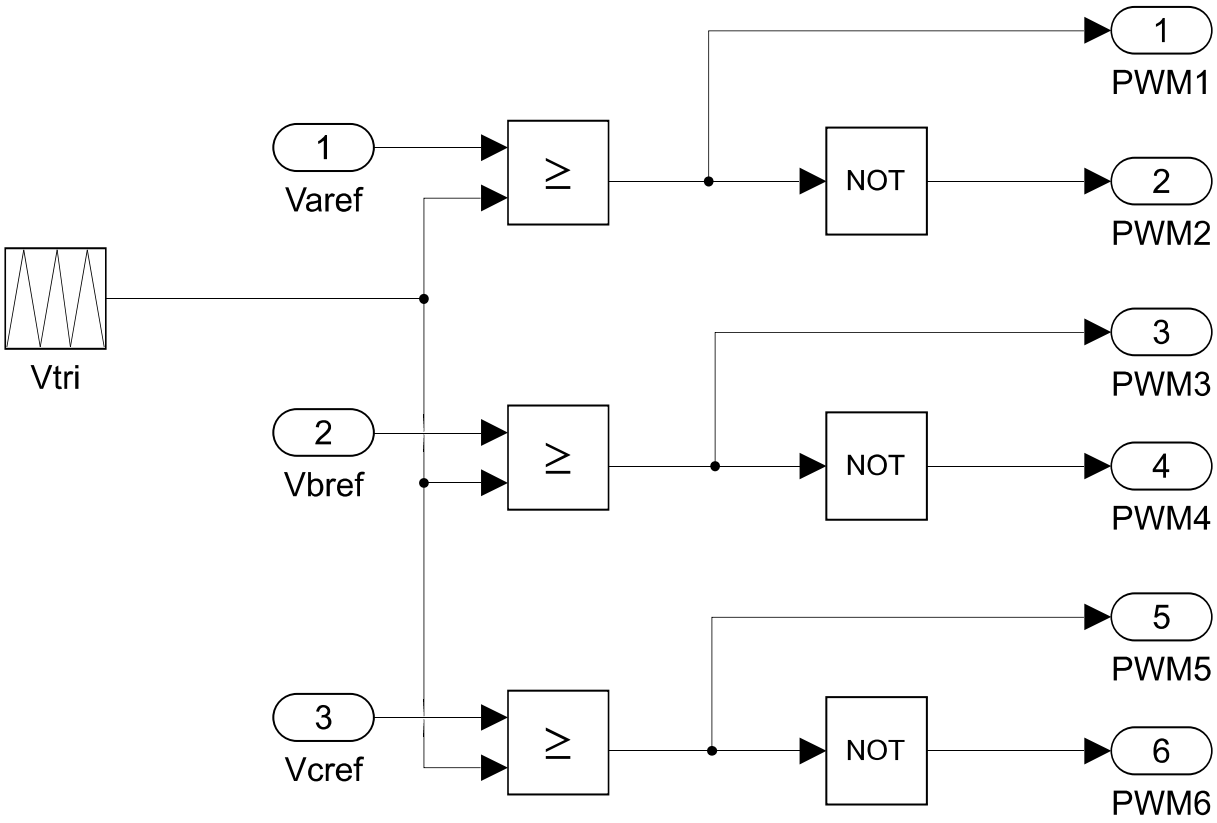

Figure B.1.8: PWM scheme for controlling the switching states of the converter IGBTs.

Interleaving

An illustration of the system with interleaved modules are presented in Figure B.1.9. The integer and odd numbers are separated as shown, in order to limit the voltage potential between adjacent modules.

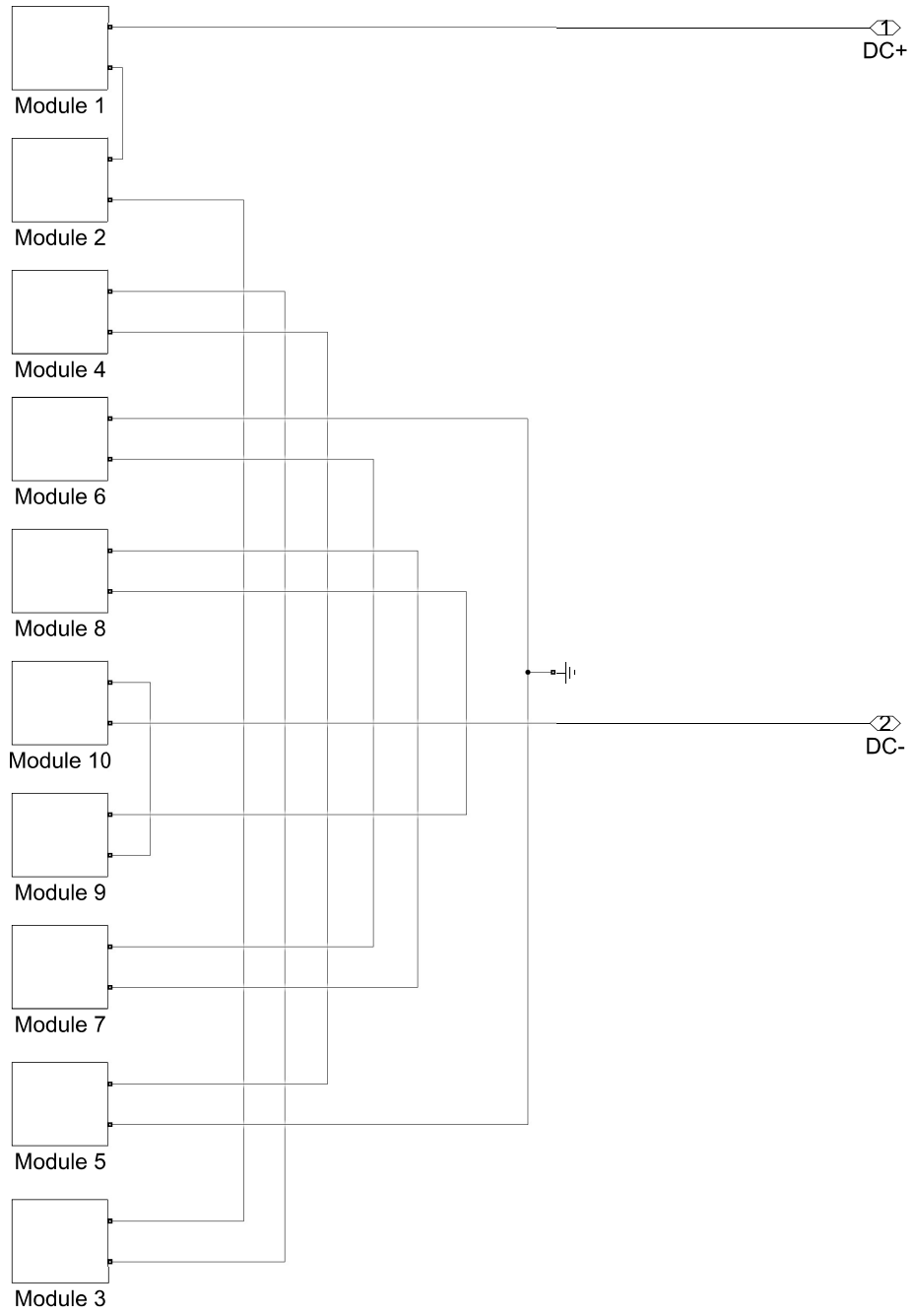

Figure B.1.9: Illustration of module interleaving to limit the voltage potential between adjacent modules.

B.2 Solution 1: DC-link W/series resistances

As elaborated on in Section 5.2, closing the bypass switch will lead to high over-currents. One solution to mitigate the over-current could be to design the DC-link with tuned series resistances.

Increased series resistance was shown to increase voltage ripple, which is inherently undesirable. By calculating the integral of the I^2R-loss curve, the heat loss in kJ was found. The simulations illustrated that by increasing the series resistance, the DC-side current was significantly reduced. However, at the cost of increased heat loss. The amount of fault current reduction depends on the maximum allowable heat dissipation in the DC-link and voltage ripple limit. The effect on fault current peak, heat dissipation and voltage ripple for module-to-ground fault is presented in Table B.2.1.

Table B.2.1: Effect of increased series resistance on heat dissipation during a module-to-ground fault and general voltage ripple.

Series resistance [Ω]	**Current peak [pu]**	**Heat dissipation [kJ]**	**Voltage ripple** [%]
10 $\mu\Omega$	7.23e4	0.92	0.03
25 $m\Omega$	877	24.1	0.10
50 $m\Omega$	444	31.3	0.23
100 $m\Omega$	224	43.7	0.45
200 $m\Omega$	127	59.6	0.91
300 $m\Omega$	95.5	69.1	1.41

By applying a limit on the acceptable voltage ripple of 1 %, the maximum series resistance is limited to around 0.2 Ω. The heat dissipation in one of the two series resistances is then around 60 kJ. The total heat dissipation in the DC-link adds to about 120 kJ in total. This is an considerable amount, and can be seen as a constant power of 12 kW for 10 seconds as shown in Equation B.2.1.

$$\frac{120kJ}{10s} = \underline{12kW} \tag{B.2.1}$$

B.3 MATLAB script

```
1
2
3  %% Master thesis - modHVDC model
4
5  % clc, clear all
6  format long
7  %%
8
9  Ts = 1e-6; %1e-6
10
11
12 %% Electrical parameters
13
14 N        = 9;                % Number of active modules
15 Pnom     = 10e6;             % Nominal power [W]
16 Pseg     = Pnom/N;           % Power per segment
17 VDC      = 100e3;            % Total DC output voltage
18 VDC_seg  = VDC/N;
19 Inom     = 110;              % Nominal RMS current
20 fnom     = 50;
21
22
23 Ls = 16.58e-9; % 9          % Source inductance
24 Rs = 0.8929e-3; %e-3        % Source resistance
25
26
27
28 Vac_seg     = Pseg/(sqrt(3)*Inom);  % AC-side line-line voltage
29 Vline_rms   = Vac_seg/sqrt(2);
30
31 % Base values
32 % AC-Side
33 Vb_ac  = Vac_seg;
34 Ib     = sqrt(2)*Inom;
35 Sb     = (2/3)*Ib*Vb_ac;
36 Pb     = Sb;
37 fb     = fnom;
38 wb=2*pi*fb;
39 Zb=Vb_ac/Ib;                  %AC impedance base (ohm)
40 Lb=Zb/wb;                    %AC inductance base value (H)
41
42 % DC-Side
43 Ib_dc  = (3/4)*Ib;
44 Vb_dc  = VDC_seg;
45 Vb     = Vb_dc;
46
```

```
47 xs=0.33;                          %PMSM armature inductance (pu).
       Value from S.Gjerde
48 rs=0.02;                          %PMSM stator resistance (pu).
       Value from S.Gjerde
49 % Rs=rs*Zb;
50 % Xs=xs*Zb;
51 % Ls=Xs/wb;
52 % ls=Ls/Lb;
53
54 % Module fault parameters
55 R_eq     = 0.2530;
56 L_eq     = 7.5e-5;
57
58
59 % HVDC transmission line
60 R_load = 1; %333;
61 hvdc_currents    = out.hvdc_current.Data(:,1);
62
63 %% Filter parameters
64
65 L1 = 5*500e-6;     %4.5*
66 L2 = 5*500e-6;     %5.59*e-6
67 Cf = 5*100e-6;
68 Rf = 0.000001;
69
70
71
72 %% Fault initiation
73
74 F1 = 100;    % Module-to-module fault
75 F2 = 0.2;    % module to ground fault
76 F3 = 100;    % DC pole-to-pole fault
77 F4 = 100;    % DC pole-to-ground fault
78
79
80 %% DC-link design
81
82 R_p       = 1e6;
83 R_s       = 1e-5; %.0251e-3
84 R_bypass = 1+1;
85
86 C_dclink        = 1.5e-3;    %5.6e-3
87 C_init          = VDC_seg/2;
88
89 Vdclink = VDC_seg;
90 %% Protection schemes
91
92 % Module 1
```

```
93
94  fuses1          = F2 + 5e-6; %10e-3
95  res_bypass      = F2 + 2.5e-3;
96  bypass1         = F2 + 100e-3; %0.02;
97  DCLB1           = F2 + 100e-3;%0.05;
98
99  % Module 2
100 fuses2          = F2 + 5e-6; %10e-3;
101 res_bypass2     = F2 + 2.5e-3;
102 bypass2         = F2 + 100e-3; %0.02;
103 DCLB2           = F2 + 100e-3; %0.05;
104
105 % Module 3
106 fuses3          = F1 + 5e-3; %10e-3
107 res_bypass3     = F1 + 2.5e-3;
108 bypass3         = F1 + 100e-3; %0.02;
109 DCLB3           = F1 + 100e-3;%0.05;
110
111 fault_fuse      = F2 + 5e-3;
112 fault_fuse2     = F1 + 5e-3;
113
114
115 thy_prot = F1 + 1e-3;
116 %% Droop control
117
118 z = 2;                  %
119 active = 4-z;
120
121 tdroop1 = F1;
122 tdroop2 = F1;
123 tdroop3 = F2;
124 tdroop4 = F2;
125
126
127 upper    = (VDC_seg*z)/active;
128
129 dy       = upper;
130 dx       = 0.013; % 0.013
131 slope    = dy/dx;
132
133
134 %% Current limiter
135
136 limit = inf;
137
138 %% Simulink
139
140 sim('Three_modules_test.slx')
```

```
141
142
143 %% Plot
144
145 % AC-Side
146 % Module 1
147 V_a                    = out.AC_voltages.Data(:,1);
148 V_b                    = out.AC_voltages.Data(:,2);
149 V_c                    = out.AC_voltages.Data(:,3);
150 t                      = out.AC_voltages.Time;
151
152 I_a                    = out.AC_currents.Data(:,1);
153 I_b                    = out.AC_currents.Data(:,2);
154 I_c                    = out.AC_currents.Data(:,3);
155
156 %Module 2
157 V_a2                    = out.AC_voltages_mod2.Data(:,1);
158 V_b2                    = out.AC_voltages_mod2.Data(:,2);
159 V_c2                    = out.AC_voltages_mod2.Data(:,3);
160 t2                      = out.AC_voltages_mod2.Time;
161
162 I_a2                    = out.AC_currents_mod2.Data(:,1);
163 I_b2                    = out.AC_currents_mod2.Data(:,2);
164 I_c2                    = out.AC_currents_mod2.Data(:,3);
165
166 % DC-Side
167 DC_v                   = out.DC_volt.Data(:,1);
168 DC_I                   = out.DC_curr.Data(:,1);
169
170 DC_v2                   = out.DC_volt_mod2.Data(:,1);
171 DC_I2                   = out.DC_curr_mod2.Data(:,1);
172
173 % DC-link capacitors
174
175 Vc1_mod1               = out.vc1_mod1.data(:,1);
176 Vc2_mod1               = out.vc2_mod1.data(:,1);
177 sum_mod1               = out.sum_VC_mod1.data(:,1);
178
179 Vc1_mod2               = out.vc1_mod2.data(:,1);
180 Vc2_mod2               = out.vc2_mod2.data(:,1);
181 sum_mod2               = out.sum_VC_mod2.data(:,1);
182
183 Vc1_mod3               = out.vc1_mod3.data(:,1);
184 Vc2_mod3               = out.vc2_mod3.data(:,1);
185 sum_mod3               = out.sum_VC_mod3.data(:,1);
186
187
188 Vc1_mod4               = out.vc1_mod4.data(:,1);
```

```
189 Vc2_mod4                = out.vc2_mod4.data(:,1);
190 sum_mod4                = out.sum_VC_mod4.data(:,1);
191
192
193 % Bypass
194
195 kJ1      = out.bypass_resistor_kJ1.data(:,1);
196 curr1    = out.bypass_resistor_current1.data(:,1);
197
198 kJ2      = out.bypass_resistor_kJ2.data(:,1);
199 curr2    = out.bypass_resistor_current2.data(:,1);
200
201 kJ3      = out.bypass_resistor_kJ3.data(:,1);
202 curr3    = out.bypass_resistor_current3.data(:,1);
203
204 t_b      = out.bypass_resistor_kJ2.Time;
205
206 % HVDC transmission
207
208 HVDC_transm = out.HVDC_VOLT_SUM.data(:,1);
209
210
211 % fault current
212
213 faultcurrent                                    = out.faultcurrent.
    data(:,1);
214 [MAXfaultcurrent, index_faultcurrent]       = max(faultcurrent
    *(-1));
```

Appendix C

Fault Parameters

This appendix presents some of the work done in the specialization project leading up to this thesis, where the fault resistances in the stator iron R_{iron}, and arcing resistance R_{arc} is derived.[3]

Fault Resistance

The fault resistance for a module to module fault will consist of the resistance in the stator iron (R_{iron}), resistance in the copper wire (R_{cu}) and the resistance of the arc (R_{arc}). The equivalent resistance can be seen as a series connection and was found with Equation C.0.1.[3]

$$R_{eq} = R_{iron} + R_{cu} + R_{arc} \tag{C.0.1}$$

The stator core is assumed to be laminated with an infinitely large resistance between them, thus if two ore more sheets are involved in the fault, the current path will be in parallel. With an increased number of laminations involved in the fault, a lower total resistance is seen by the circuit. The fault resistance will vary dependant on the location and magnitude of the fault. In the moment of fault occurrence, a closed loop between the modules via the DC potential wires is created. Hence, the placement of the DC-potential connection on the module will affect the length of the current path and thus the fault resistance. An in-depth investigation of this can be found in Section C.[3]

Arc resistance

The arcing resistance have been calculated based on two versions of Warrington's formula. given in Equation C.0.2 and C.0.3, respectively. The arc length is proportional to the fault resistance. The resistance is plotted for varying currents in the range of 100 - 10000 A, for a width between the segments equal to 1 cm. The arc resistance is presented in Figure C.0.1, where it can be seen that the resistance is non-linear. [3]

$$R_w = \frac{28688.5}{I^{1.4}} L \tag{C.0.2}$$

$$R_{arc} = \frac{2\sqrt{2}}{\pi} \frac{E_a L}{I} \tag{C.0.3}$$

Where:

E_a = Voltage gradient of the arc
L = Arc length
I = RMS value of the arc current.

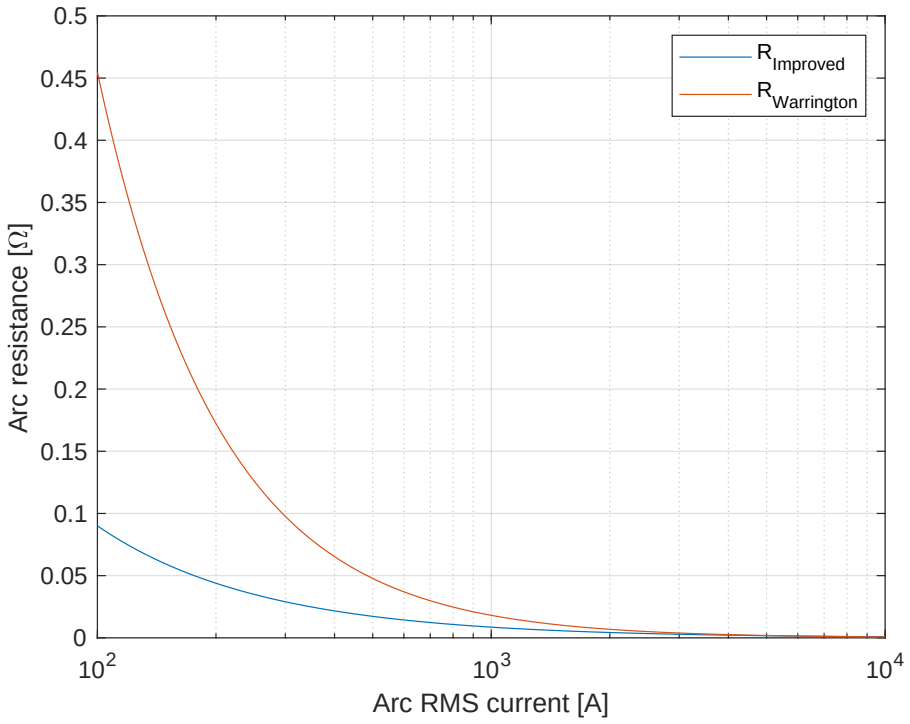

Figure C.0.1: Arc resistance for varying currents based on Warrington's formula and a arc length of 1 cm. [3]

Resistance in stator iron

In order to calculate the fault resistance in the stator iron, a 3D model of two adjacent segment sheets was created in COMSOL Multiphysics. The goal of this analysis was to examine the impact of varying fault area, location and to investigate the difference in fault resistance when one or two ground connections per segment is applied. [3] An illustration of the 3D model is presented in Figure C.0.2.

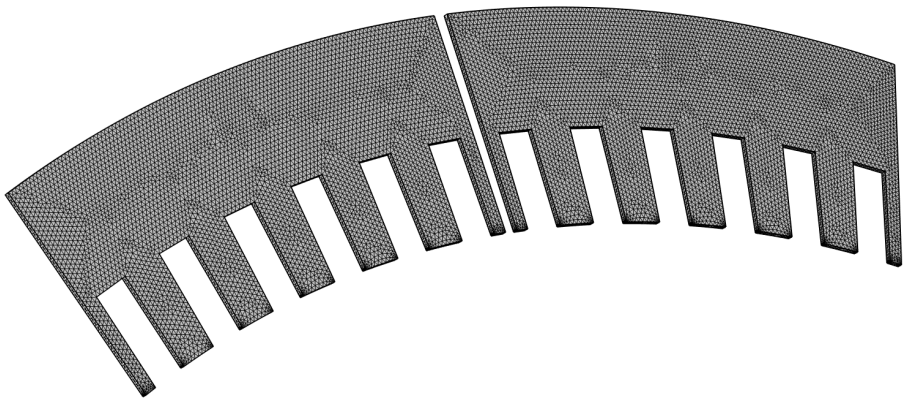

Figure C.0.2: 3D model of two adjacent stator sheets created in COMSOL. [3]

The geometry used for this analysis is based on [9]. This geometry is for a geared machine with 16 stator segments.

Table C.0.1: Geometric parameters of the stator segments. [3]

Parameter	Value	Unit
Stator height	0.2127	[m]
Stator sheet width	0.0050	[m]
Outer arc length	0.5768	[m]

The voltage potential is set to 1 kV at the terminal. In order to calculate the resistance a volume integration of the losses was performed in COMSOL. Equation C.0.4 was then applied in order to calculate the total fault resistance. [3]

$$P = U^2 \cdot R \Rightarrow R = \frac{U^2}{P} \tag{C.0.4}$$

Varying Fault Area

In the event of a module-to-module fault situation (flashover between modules), the area of the fault inception is not known. The size and placement of the terminal (fault area) will affect the current path and thus also the fault resistance, as will be shown. [3]

Figure C.0.3 illustrates the difference in current density for the base case (left) and the with an 100% increase in fault area (right). The current density is given in [A/mm^2]. It can be seen that the current density is lower for higher fault area and is illustrated with more blue colors. [3]

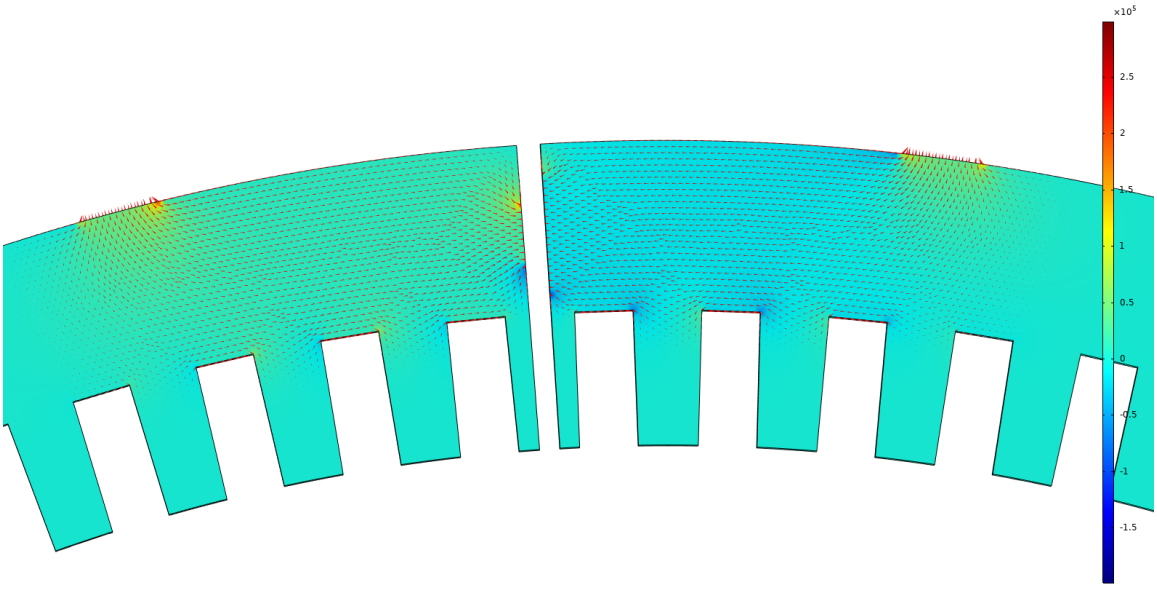

Figure C.0.3: Illustration of current densities for different sizes of fault areas. The segment to the left is the base case while the segment to the right have double the fault area. Current density is given in [A/mm^2] [3]

Results

Including the base case, simulations were performed with an increase in terminal sizes (fault areas) of 50 %, 100 % and 500 %. [3] The results from these simulations is presented in Table C.0.2.

Table C.0.2: Fault resistances for different fault areas. [3]

Fault Area	Resistance [mΩ]	Difference [%]
0.2 (Base case)	0.04826	-
0.3 (+ 50%)	0.04636	4.1
0.4 (+100%)	0.04531	6.5
1.0 (+500%)	0.04462	8.2

From these results it can be seen that the fault resistance is not heavily impacted by the size of the fault area as there was only a difference of 8.1 % for an size increase of 500 %. [3]

One Vs two ground potentials

Each stator segment are floating on the DC potential by having a connection to the DC side of the converter. One or more connections could be applied in order to manipulate the current path and thus also the fault resistance. [3]

The difference between having one or two ground connections is illustrated in Figure C.0.4. Each ground connection has a width equal to 10 % of the outer segment arc length. On the left segment, one ground potential is place in the middle of the segment, while on the segment to the right have two ground connections, 20% from the edges relative to the arc length. [3]

The red lines are streamlines, illustrating the current flow from the terminal towards the ground potentials. Although current flows through the whole segments, the current densities varies a lot. [3]

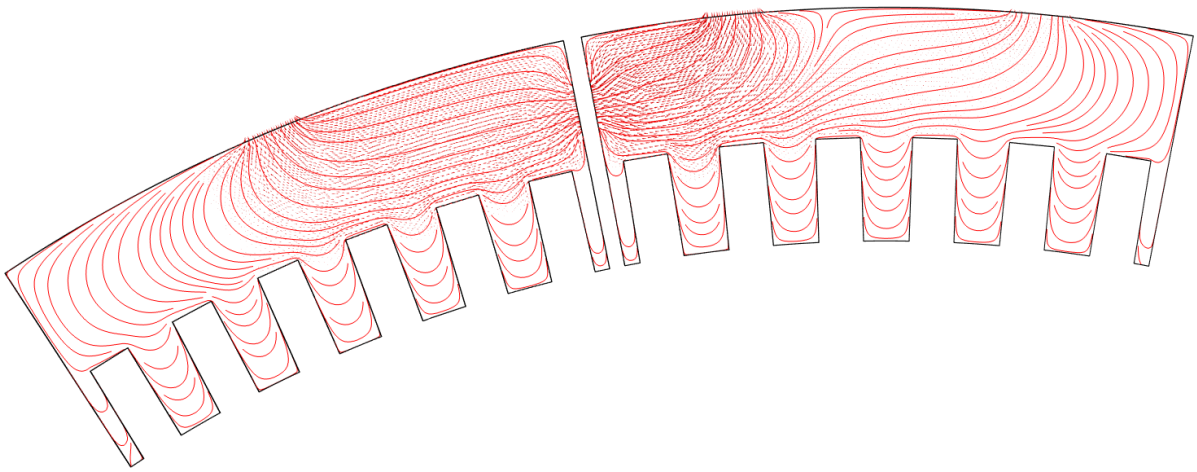

Figure C.0.4: Current path and density for segment with one or two ground potentials. [3]

Results

The results from the simulations with one and two ground connections are presented in Table C.0.3. It is shown that having two ground potentials greatly impacts the total fault resistance as two connections resulted in an decrease in resistance of 41.9 %. [3]

Table C.0.3: Comparison of fault resistance for segment with one and two ground connections. [3]

# of ground connections	Resistance [mΩ]	Difference [%]
1	0.04826	-
2	0.02802	-41.9

Fault Location

The location of the fault will have an impact on the fault resistance. In order to investigate the difference in fault resistance for different fault locations, faults occurring in the upper most part of the yoke and in the lower most part of the tooth was simulated for. This is illustrated in Figure C.0.5, where the difference in current density is visualized. [3]

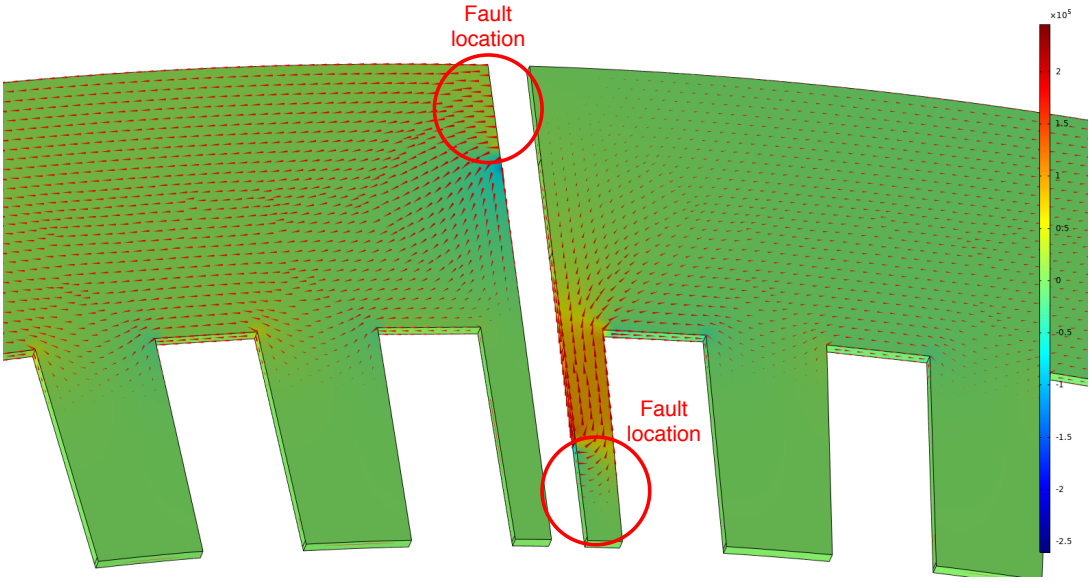

Figure C.0.5: Illustration of the difference in current density for faults occurring in the upper part of the stator yoke and in the lower part of the tooth. [3]

Results

From these simulations, it is found that for a fault occurring in the lower part of the tooth will result in a fault resistance that is 144 % higher than for a fault occurring in the upper part of the yoke. [3] The results are presented in Figure C.0.4.

Table C.0.4: Comparison of fault resistance for fault occurring in the upper yoke and lower tooth. [3]

Fault location	**Resistance** [$m\Omega$]	**Difference** [%]
Upper yoke	0.0523	-
Lower tooth	0.1275	+144.0 %

Thomas Mickelborg

Detection and Protection strategy for a modular HVDC generator

NTNU
Norwegian University of
Science and Technology