Phase-Tracking Robust-Synchronization-Loop for Grid-Connected Converters

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Abstract—This paper presents a novel phase-tracking robust-synchronization-loop (RSL) to track the phase and frequency of the grid voltage. A detailed analytical model of the proposed RSL algorithm is presented. Further, a state-space small-signal model is developed, including the dynamics of a grid-connected converter and its controller. From the small-signal analysis, it is shown that the eigenvalues associated with the states of the RSL remain in the left half-plane even for a very weak grid condition with a grid impedance of 1.0 pu, thus, it provides better stability property with the grid-connected converters. In order to show the effectiveness of the proposed RSL, simulation results are provided for different scenarios of the grid conditions such as voltage and frequency disturbance, unbalance grid condition and grid faults. Further, the performance of the RSL algorithm is tested by experiment in lab. The results show that the proposed method effectively tracks the phase and frequency of the grid voltage and maintains the good synchronism of the converters during different disturbances.

Index Terms—Robust-synchronization-loop, grid-connected converter, synchronization, converter controller, phase-tracking-loop.

I. Introduction

THE power electronics converters is increasingly used in modern power systems for integrating distributed generation (DG) based on renewable energy sources (RES) [1]–[3]. These power electronic converters are controlled using different techniques such as the standard vector control, model predictive control, [4]–[6] and more recently artificial intelligence-based control such as artificial neural network, fuzzy logic control [7]. Regardless of the control strategy employed in these DG converters, a synchronization unit is required in the controller in order to synchronize the terminal voltage of the converters to the grid before connecting them to the grid [8]–[10]. The synchronization enables the converters to connect effectively to the grid without a harmful transient overcurrent during the connection.

The synchronization of grid-connected converters is usually accomplished by detecting the phase of the grid voltage using a phase-locked-loop (PLL) [11]. The PLL is first introduced in 1930s for the synchronous reception of radio signals [12]. It is now widely used in the modern power system, to estimate the phase, frequency and amplitude of the fundamental voltage, to measure the harmonics, inter-harmonics, power quality indices, in machine drives, power electronics-based renewable energy integration, high voltage dc (HVDC) transmission

system, and flexible ac transmission system (FACTS). The PLLs present a proper performance under a balance voltage condition and a strong grid condition, however, the performance of PLLs degrades significantly under an unbalanced and distorted condition of the grid voltage, load unbalances, as well as measurement scaling error and dc offset, produces periodic disturbances. In order to improve the issues, several advanced PLLs have been proposed, for example, a moving average filter with the synchronous reference frame (SRF) PLL improves the disturbance rejection capability [13]; the dual a SRF filtering-based PLL (DSRF-PLL) improves the performance for imbalance voltage [14]; the delayed signal cancellation (DSC) improves the frequency variation performance [15]; the adaptive PLLs provides a dynamically change PLL bandwidth to achieve a fast-tracking performance for large phase jump [16]. The other advanced PLLs that exist in the literature are Type-N PLL and Quasi Type-N PLLs [17]. More details about the recent advancement on the PLL can be found in the following review paper [11]. Even though the advanced PLLs improve the performance of one targeted matrices while degrading the others, for example, the MAF improves disturbance rejection capability while degrading the dynamic performance; the DSC increases the computational effort and the implementation complexity. Moreover, PLLs are inherently non-linear, difficult and time-consuming tuning the PLLs to achieve satisfactory performance and introduce an instability problem with the grid-connected converters, especially a weak grid condition (a high impedance grid) [18], [19].

Frequency-locked-loop (FLL) is often used for the synchronization of grid-connected converters [20]. The main difference between the PLL and FLL is that PLL is implemented in SRF (dq-frame) while the FLL is in the $\alpha\beta$-frame [21]. The PLL has reached a mature stage of development in power and energy applications, contrary the FLL is not a mature technique yet, however, from the functional point of view, both FLLs and PLLs are equivalent and are nonlinear negative-feedback control systems [11], [21]. This equivalence implies that FLLs have similar issues as the PLLs. Further development of the FLLs allows the designer to mitigate the issues, for example, in order to tackle the dc offset, two additional integrator can be realized [22]; to improve performance for imbalance voltage and harmonics, a parallel configuration of two or more first-order complex band-pass filter can be used [23]. More details about the recent advancement of the FLLs can be found in the following review papers [21], [24].

The power exchange between the grid and the converters can be used to realize the synchronization mechanism of a grid-connected converter which utilizes the internal synchronization

mechanism of an ac system in a similar way as the operation of a synchronous generator (SG) [25]–[27]. This type of synchronization technique is known as power-synchronization-loop (PSL) [27]. A PLL is no longer required during the normal operation of the grid-connected converter, however, in some situations like the converter is in blocked stage, it needs a PLL to provide the initial synchronization signal to the converter controller before connection. During a severe ac-system fault, the PSL synchronization switches to the PLL synchronization mode to limit the current flowing into the converter semiconductor devices. This adds complexity to the overall control system and will impact its stability. Furthermore, control algorithms for converters have been developed where the synchronization can be performed without a dedicated synchronization unit like PLL [28], [29]. Those controllers mimic the synchronization mechanism of an SG and provide the grid voltage and frequency support. The performance of these controllers is very satisfactory during a normal operation of the grid. The main concern of these controllers is the limited capability of regulating current during faults as these controllers do not have an internal current control-loop.

This paper presents a new phase-tracking-loop, so-called Robust-Synchronization-Loop (RSL) for the grid-connected DG converters to track the phase and frequency of the grid voltage. The main difference between the PLL and proposed RSL is that in a PLL, the $q-$axis voltage is forced to be zero by a PI/PID controller to get the phase of the voltage, while in the proposed RSL, the estimated phase angle makes the $q-$axis voltage to zero without using a PI/PID controller. A detailed analytical model of the proposed RSL algorithm is presented. Further, a state-space small-signal model is developed which includes the dynamics of a grid-connected converter and its controller. The analytical small-signal model is also verified by comparing it with a simulation model. From the small-signal analysis, it is shown that the eigenvalues associated with the states of the RSL remain in the left half-plane even for a very weak grid condition with a grid impedance of 1.0 pu, thus, it provides better stability property with the grid-connected DG converters. Simulation and experimental results are provided to show the effectiveness of the proposed RSL. The results show that the proposed method effectively tracks the phase and frequency of the grid voltage and maintains the good synchronism of the DG converters.

The concept of the proposed RSL has been introduced in the author's conference version of the paper [30]. The new contribution compared to the conference paper comprises the following: (i) a detailed theoretical analysis, including the small-signal modeling and stability analysis, (ii) the performance comparison with the standard PLL, and (iii) experimental verification of the proposed RSL for a grid-connected converter. The rest of the paper is organized in the following. Section II presents the development of the proposed RSL synchronization mechanism. Section III presents the state-space model development and parameter tuning of the RSL. Section IV presents the small-signal model development for the grid-connected converter and the small-signal analysis of the system. Simulation and experimental results are presented
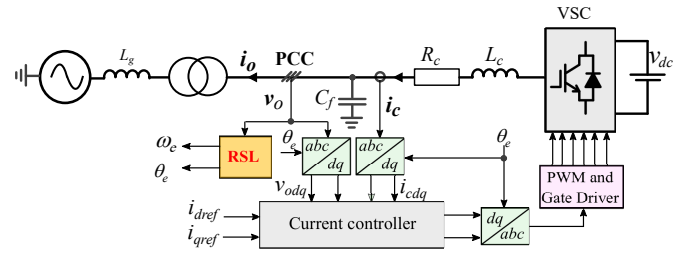

Fig. 1. A grid-connected DG converter and its controller with an RSL.

in section V. Finally, this paper is concluded in Section VI.

II. THE PROPOSED ROBUST-SYNCHRONIZATION-LOOP

Fig. 1 shows a grid-connected converter. The dc-side can be connected to a RES, such as solar PV, battery energy storage, wind power generator. In this work, a dc-voltage source has been considered here. Before enabling the pulse-width-modulation (PWM) of the converter switches, the converter voltage must be synchronized with the point of common coupling (PCC) voltage v_o in order to avoid a transient overcurrent. The synchronization unit is used to serve that purpose.

The RSL generates a voltage, e internally in the digital signal processor, which is synchronized with v_o to track the frequency and phase of the PCC voltage. Initially, it is assumed that e is not synchronized with v_o, thus, the magnitude and phase of e are not the same as v_o. As these two voltages are not synchronized, there will be a voltage error, $v_{err} = e - v_o$. The PCC voltage is available in the digital controller through voltage sensors. If a virtual impedance is introduced in between the RSL and PCC voltage, a virtual current i_v flows through this virtual impedance due to this voltage error. Thus, the virtual current can be given by

$$\mathbf{i_{vabc}} = \frac{\mathbf{e_{abc}} - \mathbf{v_{oabc}}}{sL_v + R_v} \tag{1}$$

where the bold font is used to represent the voltage in the matrix form for the three-phase system, as $\mathbf{e_{abc}} = \begin{bmatrix} e_a & e_b & e_c \end{bmatrix}^T$, $\mathbf{v_{oabc}} = \begin{bmatrix} v_{oa} & v_{ob} & v_{oc} \end{bmatrix}^T$ and $\mathbf{i_{vabc}} = \begin{bmatrix} i_{va} & i_{vb} & i_{vb} \end{bmatrix}^T$; L_v and R_v are virtual inductor and resistor. The power due to this virtual current can be given by

$$\begin{bmatrix} P_v \\ Q_v \end{bmatrix} = \begin{bmatrix} \sin\theta_v & -\cos\theta_v \\ \cos\theta_v & \sin\theta_v \end{bmatrix} \begin{bmatrix} \frac{3EV_o}{Z_v}\sin\delta \\ \frac{3E^2}{Z_v} - \frac{3EV_o}{Z_v}\cos\delta \end{bmatrix} \tag{2}$$

where E and V_o are the RMS value of e and v_o, respectively; θ_e and θ_o are their corresponding phase angle and $\delta = (\theta_e - \theta_o)$; Z_v and θ_v are the magnitude and angle of the virtual impedance.

The purpose of implementing RSL is to estimate the phase of the PCC voltage to synchronize the converter voltage to the grid. The synchronization is achieved when the estimated RSL voltage e becomes equal to the PCC voltage v_o, i.e.,

$$E = V_o \text{ and } \theta_e = \theta_o. \tag{3}$$

The active and reactive power in (2) becomes zero, regardless of the virtual impedance type when $E = V_o$ and $\theta_e = \theta_o$, i.e.

when synchronization is achieved. Contrary, synchronization can be achieved by regulating the active and reactive power to zero.

The virtual impedance is selected to be dominantly inductive which gives $\theta_v \approx \pi/2$. Thus, the active and reactive power can be rewritten by

$$\begin{bmatrix} P_v \\ Q_v \end{bmatrix} = \begin{bmatrix} \frac{3EV_o}{Z_v} \sin \delta \\ \frac{3(E - V_o \cos \delta)}{Z_v} E \end{bmatrix}. \tag{4}$$

The active and reactive power in (4) give a positive correlation between the active power with the frequency and the reactive power with the voltage which can be expressed as

$$P_v \sim \delta \text{ and } Q_v \sim E. \tag{5}$$

The frequency of the PCC voltage can be given by

$$\omega_o = \omega_s + \Delta\omega_s \tag{6}$$

where ω_s is the system fundamental frequency and $\Delta\omega_s$ is the frequency deviation from the fundamental frequency. This frequency deviation is resulting from the active power deviation which can be expressed as

$$\Delta\omega_s = -k_p \Delta P \tag{7}$$

where k_p is a droop gain or a positive gain and ΔP is the power deviation that causes fundamental frequency deviation.

As it is assumed, initially, the RSL generated voltage is not synchronized, it results in a phase difference, δ and the frequency difference, $\Delta\omega_e$. Thus, the frequency of the RSL voltage can be expressed as

$$\omega_e = \omega_o + \Delta\omega_e \tag{8}$$

and the phase difference between the PCC and the RSL voltages can be expressed by

$$\delta = \int \Delta\omega_e dt. \tag{9}$$

An integral controller is introduced to compensate this phase error of the estimated voltage by regulating active power as

$$\delta = k_p \int (P^* - P_{v2}) \, dt. \tag{10}$$

where P^* is the reference active power and P_{v2} is the virtual active power introduced by the phase difference between the PCC voltage, v_o and RSL internally generated voltage, e. Hence, the estimated frequency of the RSL can be written by

$$\omega_e = \omega_s - k_p \Delta P + k_p (P^* - P_{v2}). \tag{11}$$

When the synchronization is achieved, δ becomes zero. It can be achieved by setting the reference power, P^* to 0 in (10). Thus, the estimated frequency and phase of the RSL can be given by

$$\omega_e = \omega_s - k_p P_v \tag{12}$$

$$\theta_e = \int \omega_e dt. \tag{13}$$
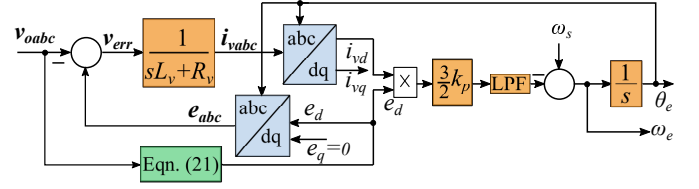
where $P_v = \Delta P + P_{v2}$.

Fig. 2. Proposed phase-tracking robust-synchronization-loop.

Another condition in (3) for achieving the synchronization is having the equal magnitude of the estimated RSL voltage and the PCC voltage. This can be achieved by setting

$$E = V_o \tag{14}$$

which is available in the digital controller through voltage transducer and after applying Clarke transformation as

$$V_o = \sqrt{v_{o\alpha}^2 + v_{o\beta}^2}/\sqrt{2}. \tag{15}$$

The RSL generates voltage e_{abc} in the stationary $abc-$frame, and produces the phase angle that keeps the $q-$axis voltage to zero. Hence, the magnitude of the $d-$ and $q-$axis voltage is given by

$$e_d = \sqrt{2}E \text{ and } e_q = 0. \tag{16}$$

Thus, the RSL voltage can be given in the $abc-$frame by

$$\mathbf{e_{abc}} = \mathbf{T_{dq}}(\theta_e) \begin{bmatrix} e_d \\ e_q \end{bmatrix} \tag{17}$$

where

$$\mathbf{T_{dq}}(\theta_e) = \begin{bmatrix} \cos\theta_e & -\sin\theta_e \\ \cos(\theta_e - \frac{2\pi}{3}) & -\sin(\theta_e - \frac{2\pi}{3}) \\ \cos(\theta_e + \frac{2\pi}{3}) & -\sin(\theta_e + \frac{2\pi}{3}) \end{bmatrix}.$$

This RSL generated voltage is used to obtain the virtual current in (1). The virtual current can be expressed in $dq-$frame as

$$\begin{bmatrix} i_{vd} \\ i_{vq} \end{bmatrix} = \mathbf{T_{dq}^{-1}}(\theta_e)\mathbf{i_{vabc}}. \tag{18}$$

Since the $q-$axis component of the estimated voltage is directly set to zero, the virtual active power can be given by

$$P_v = \frac{3}{2} e_d i_{vd}. \tag{19}$$

Hence the RSL is proposed as

$$\frac{d\theta_e}{dt} = \omega_s - k_p P_v \tag{20}$$

$$e_d = \sqrt{2}E = \sqrt{v_{o\alpha}^2 + v_{o\beta}^2} \text{ and } e_q = 0. \tag{21}$$

The proposed RSL is shown in Fig. 2, where the virtual impedance structure forms into a virtual admittance structure. The virtual admittance structure emulates the output impedance without leading to difficulties in hardware implementation. Note that a low pass filter is often necessary to remove the high-frequency component from the power.

III. Dynamic Representation and Parameter Tuning of the RSL

A. State-space modeling of the RSL

The virtual current in (1) can be presented by differential equation as

$$L_v \frac{d\boldsymbol{i_{vabc}}}{dt} = \boldsymbol{e_{abc}} - \boldsymbol{v_{oabc}} - R_v \boldsymbol{i_{vabc}}. \tag{22}$$

Since the small-signal analysis cannot be directly applied to the abc-stationary frame, the modeling and analysis of the system will be presented in a SRF. The transformation of the three-phase quantity from the stationary reference frame to the SRF is based on the amplitude-invariant Park transformation, thus, the dynamic equation of the virtual current can be given in the $dq-$frame as

$$\frac{di_{vd}}{dt} = \frac{e_d}{L_v} - \frac{v_{od}}{L_v} - \frac{R_v i_{vd}}{L_v} + \omega_e i_{vq} \tag{23}$$

$$\frac{di_{vq}}{dt} = \frac{e_q}{L_v} - \frac{v_{oq}}{L_v} - \frac{R_v i_{vq}}{L_v} - \omega_e i_{vd}. \tag{24}$$

A low pass filter (LPF) is introduced to remove the high-frequency component from the virtual active power. With the LPF, (20) can be rewritten as

$$\frac{d\theta_e}{dt} = \omega_s - k_p P_{vf} \tag{25}$$

where

$$P_{vf} = \frac{\omega_{lf}}{s + \omega_{lf}} P_v. \tag{26}$$

P_{vf} is the filtered virtual active power and ω_{lf} is the cut-off frequency of the low pass filter. The LPF can be presented in the state-space form as

$$\frac{dP_{vf}}{dt} = \omega_{lf} (P_v - P_{vf}). \tag{27}$$

The dynamic performance of the RSL can now be described by (23), (24), (25) and (27) which is presented in the state-space form through a 4th order non-linear model.

B. Parameter tuning

The phase tracking speed of the RSL depends upon the design of the parameters. As shown in Fig. 2, L_v, R_v and k_p need to be selected to achieve the desired performance for the grid-connected converter. The open-loop transfer function can be used to find the value of L_v, R_v and k_p. The RSL is a nonlinear negative feedback control system like the other synchronization units [11], [21], therefore obtaining the control-loop transfer function needs a lot of effort for the designing the parameters. The step of obtaining the transfer function has been described in the following.

In order to derive the transfer function, a relationship between the phase and dq-voltage is obtained. Applying Clarke- and Park-transformation, the dq-frame PCC voltage can be given by [11]

$$v_d = \sqrt{2} V_o \cos (\Delta \theta_o - \Delta \theta_e) \tag{28}$$

$$v_q = \sqrt{2} V_o \sin (\Delta \theta_o - \Delta \theta_e). \tag{29}$$
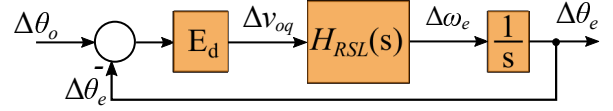

Fig. 3. Small-signal linearized model of the robust-synchronization-loop.

The RSL tracks the phase of the PCC voltage, i.e., $\Delta \theta_o = \Delta \theta_e$ which gives

$$v_d \approx E_d \tag{30}$$

$$v_q \approx E_d (\Delta \theta_o - \Delta \theta_e) \tag{31}$$

wher $E_d = \sqrt{2} V_o$.

As can be seen in (31), v_q contains the phase information which will be used to derive the open-loop and closed-loop transfer function of the RSL.

In the RSL implementation, the virtual active power given in (19) is realized to obtain the phase information. Since the phase information in (31) is obtained in terms of the q-axis voltage, it needs to find a relation between the q-axis voltage and the virtual active power. It can be started with the virtual currents. The dynamic equation of virtual current in the dq-frame has been given by (23) and (24). Applying Laplace transform, the dynamic equation of the virtual current can be rewritten in the small-signal form as

$$(sL_v + R_v) \Delta i_{vd} = \Delta e_d - \Delta v_{od} + \omega_e L_v \Delta i_{vq} \tag{32}$$

$$(sL_v + R_v) \Delta i_{vq} = -\Delta v_{oq} - \omega_e L_v \Delta i_{vd}. \tag{33}$$

Again, the voltage magnitude in (21) can also be obtained from the dq-frame voltage as

$$e_d = \sqrt{v_{od}^2 + v_{oq}^2} \tag{34}$$

which in the small-signal form gives

$$\Delta e_d = \frac{V_{od}}{\sqrt{V_{od}^2 + V_{oq}^2}} \Delta v_{od} + \frac{V_{oq}}{\sqrt{V_{od}^2 + V_{oq}^2}} \Delta v_{oq} \tag{35}$$

where capital letter is used to represent the steady-state values. At steady-state, $V_{oq} = 0$, which gives

$$\Delta e_d = \Delta v_{od}. \tag{36}$$

Inserting (36) into (32), solving for i_{vd}, the relation between the d-axis virtual current and q-axis voltage can be given by

$$\Delta i_{vd} = -\frac{\omega_e}{L_v} \frac{1}{s^2 + 2s \frac{R_v}{L_v} + \frac{R_v^2}{L_v^2} + \omega_e^2} \Delta v_{oq}. \tag{37}$$

Inserting this relation in (19) and combine with (12), it can be obtained

$$\Delta \omega_e = \frac{3 E_d k_p \omega_e}{2 L_v} \frac{1}{\left(s^2 + 2s \frac{R_v}{L_v} + \frac{R_v^2}{L_v^2} + \omega_e^2 \right)} \Delta v_{oq}.$$

The small-signal model of the RSL is depicted in Fig. 3 where $H_{RSL}(s)$ is defined

$$H_{RSL}(s) = \frac{3 E_d k_p \omega_e}{2 L_v} \frac{1}{\left(s^2 + 2s \frac{R_v}{L_v} + \frac{R_v^2}{L_v^2} + \omega_e^2 \right)}.$$
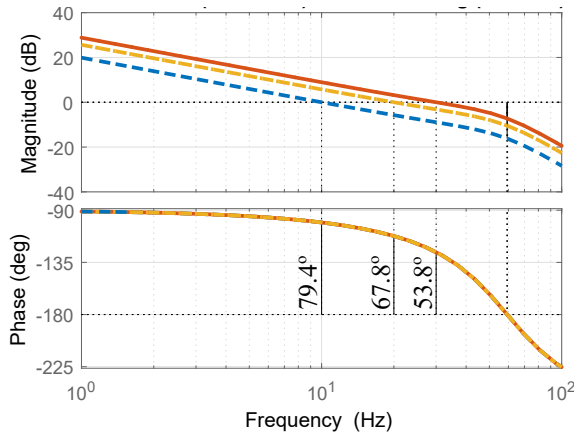
Fig. 4. Frequency response of the open-loop transfer function.

Fig. 5. Root-lucas plot of the closed-loop transfer function.

The open-loop transfer function of the RSL can now be given by

$$T_{RSL-OL}(s) = \frac{3E_d^2 k_p \omega_e}{2L_v} \frac{1}{s\left(s^2 + 2s\frac{R_v}{L_v} + \frac{R_v^2}{L_v^2} + \omega_e^2\right)}. \quad (38)$$

Eqn. (38) indicates that a higher value of k_p provides fast tracking performance while reduces the noise reduction capability as it increases the bandwidth of open-loop transfer function. A higher value of the virtual impedance ratio, $\frac{R_v}{L_v}$ provides a better stability property. Therefore, the selection of the virtual impedance and k_p is a trade-off between the response time and the stability of the synchronization loop.

The magnitude of the open-loop gain of (38) at the crossover frequency ω_c is unity. Thus, according to (38), it can be written:

$$|T_{RSL-OL}(j\omega_c)| = 1 \quad (39)$$

which gives

$$k_p = \frac{2L_v}{3E_d^2 \omega_s} \sqrt{\left(2\omega_c^2 \frac{R_v}{L_v}\right)^2 + \omega_c^2 \left(\left(\frac{R_v^2}{L_v^2} + \omega_s^2\right) - \omega_c^2\right)^2}. \quad (40)$$

It is straightforward selecting the value of the virtual inductor and resistor based on the converter parameters. The parameter of the test converter setup is given in Table I. An example of the control tuning is presented here, where $L_v = 0.25$ mH, i.e., 50% of the converter inductance and the resistance, $R_v = 0.05\,\Omega$ are used. k_p can be calculated by setting the crossover frequency ω_c. The bode plot of the open-loop transfer function is shown in Fig. 4 for ω_c of $2\pi 10$, $2\pi 20$ and $2\pi 30$ rad/s. As can be seen, the open-loop frequency responses have a phase margin of 79.4^o, 67.8^o and 53.8^o at 10, 20 and 30 Hz, respectively which ensure the stability of the synchronization-loop. In order to further investigate the performance, the location of the closed-loop poles and step responses have been studied. The closed-loop transfer function of the RSL can be given by

$$T_{RSL-CL}(s) = \frac{\frac{3E_d^2 k_p \omega_s}{2L_v}}{s^3 + 2\frac{R_v}{L_v}s^2 + \left(\frac{R_v^2}{L_v^2} + \omega_s^2\right)s + \frac{3E_d^2 k_p \omega_s}{2L_v}}. \quad (41)$$
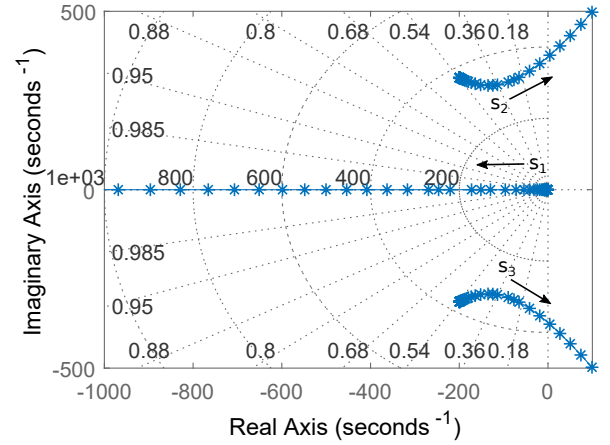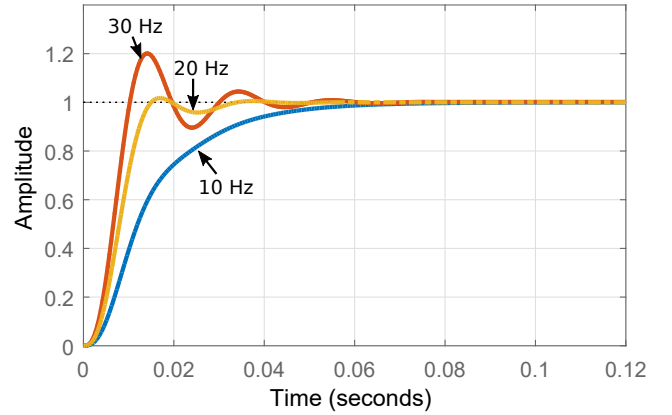

Fig. 6. Step response of the closed-loop transfer function.

The root-lucas of the closed-loop system is shown in Fig. 5. The closed-loop transfer function shows that RSL has three poles in the form of $s_1 = -\alpha_1, s_{2,3} = -\alpha_2 \pm j\omega_d$. As shown in Fig. 5, the pole s_1 always stays in the left half-plane while the left or right half-plane location of $s_{2,3}$ depends on the parameter. Moreover, the performance of the RSL depends on the location of the poles. The dominant pole determines the performance of the RSL. If s_1 is the dominant pole, then performance will be over-damped otherwise it will be under-damped response. The step response of the closed-loop system for the three crossover frequencies are shown in Fig. 6 where it is over-damped response for $f_c = 10$ Hz with $s_1 = -75.4, s_{2,3} = -162.3 \pm j296.5$ as s_1 is the dominant pole, while it is under-damped response for 20 Hz with $s_1 = -167.3, s_{2,3} = -116.4 \pm j293.6$ and 30 Hz with $s_1 = -240.1, s_{2,3} = -79.9 \pm j306.5$ as $s_{2,3}$ is the dominant pole. In order to further verify this theoretical analysis, the simulation results are presented for these three designs in Section V-A1 (see Fig. 12), which proves the accuracy of the theoretical design. The 30 Hz design has an overshoot of 20%, however, 10 Hz and 20 Hz designs ensure the robustness and stability of the closed-loop RSL, therefore, both designs can be implemented.

TABLE I
PARAMETERS OF THE CONVERTER SYSTEM.

Parameters	Values	Parameters	Values
Rated line voltage (RMS), V_o	$100\sqrt{\frac{3}{2}}$ V	C_f	$50\,\mu$F
Rated dc voltage,V_{dc}	300 V	L_c	0.5 mH
Rated frequency, f	50 Hz	L_v	0.25 mH
Converter filter inductance, L	0.2 mH	R_v	$0.05\,\Omega$

TABLE II
EIGENVALUES AND MAIN PARTICIPATING STATES.

Oscillation Mode	Eigenvalues, $\lambda = \sigma \pm j\omega$	Associated states
$\lambda_{1,2}, \lambda_{3,4}$	$-7.85 \pm j4399.1, -7.85 \pm j5027.4$	$v_{od}, v_{oq}i_{od}, i_{od}$
$\lambda_{5,6}$	$-5000.0, -5000.0$	i_{cd}, i_{cq}
$\lambda_{7,8}$	$-20, -20$	γ_{id}, γ_{iq}
$\lambda_{9,10}$	$-175.5 \pm j248.9$	i_{vd}, i_{vq}
λ_{11}	-123.1	θ_e
λ_{12}	-426.6	P_{vf}

IV. SMALL-SIGNAL MODELING AND STABILITY ANALYSIS

A. State-space modeling of the converter and its controller

The electrical circuit of a converter for analytical modeling is shown in Fig. 1 where L_c and R_c are the total series inductance and resistance between the converter and PCC, C_f is the filter capacitance connected at PCC and R_g and L_g are the grid resistance and inductance including the series resistance and inductance of the transformer. The dynamic equations of the converter current, the capacitor voltage and the grid current can be given in the $dq-$frame by

$$\frac{d\boldsymbol{i_{cdq}}}{dt} = \frac{\boldsymbol{v_{cdq}}}{L_c} - \frac{\boldsymbol{v_{odq}}}{L_c} - \left(\frac{R_c}{L_c} + j\omega_g\right)\boldsymbol{i_{cdq}} \quad (42)$$

$$\frac{d\boldsymbol{v_{odq}}}{dt} = \frac{\boldsymbol{i_{cdq}}}{C_f} - \frac{\boldsymbol{i_{odq}}}{C_f} - j\omega_g\boldsymbol{v_{odq}} \quad (43)$$

$$\frac{d\boldsymbol{i_{odq}}}{dt} = \frac{\boldsymbol{v_{odq}}}{L_g} - \frac{\boldsymbol{v_{gdq}}}{L_g} - \left(\frac{R_g}{L_g} + j\omega_g\right)\boldsymbol{i_{odq}} \quad (44)$$

where, for example, converter current $\boldsymbol{i_{cdq}} = i_{cd} + ji_{cq}$.

The current controller is assumed to be a widely used SRF-PI controller with the decoupling term and feed-forward term. If the delay introduced by the PWM switching is neglected, the output voltage reference obtained from the current controller can be given by

$$v_{cd} = k_{pc}\left(i_{d,ref} - i_{cd}\right) + k_{ic}\gamma_{id} + v_{od} - \omega_e L_c i_{cq} \quad (45)$$

$$v_{cq} = k_{pc}\left(i_{q,ref} - i_{cq}\right) + k_{ic}\gamma_{iq} + v_{oq} + \omega_e L_c i_{cd} \quad (46)$$

where $i_{d,ref}$ and $i_{q,ref}$ are the $d-$ and $q-$axis current reference; k_{pc} and k_{ic} are the proportional and integral gain of the current controller; $\gamma_{id} = \int\left(i_{d,ref} - i_{cd}\right)dt$ and $\gamma_{iq} = \int\left(i_{q,ref} - i_{cq}\right)dt$ are two auxiliary variables introduced to represent the integral part of the current controller and can be written in the state-space form as

$$\frac{d\gamma_{id}}{dt} = i_{d,ref} - i_{cd} \quad (47)$$

$$\frac{d\gamma_{iq}}{dt} = i_{q,ref} - i_{cq}. \quad (48)$$

B. Small-signal modeling of the system, including RSL

The small-signal model of the system is developed based on the state-space model developed in subsections III-A and IV-A. The system is presented in state-space form through a 12th-order nonlinear model by

$$\frac{dx(t)}{dt} = f(x(t), u(t)) \quad (49)$$

$$y(t) = g(x(t), u(t)) \quad (50)$$

where $x(t)$ and $u(t)$ are the state vector and the input vector, respectively and given by

$$x(t) = [v_{od}\ v_{oq}\ i_{cd}\ i_{cq}\ \gamma_{id}\ \gamma_{iq}\ i_{od}\ i_{oq}\ i_{vd}\ i_{vq}\ \theta_e\ P_{vf}]$$
$$u(t) = [i_{d,ref}\ i_{q,ref}\ v_{gd}\ v_{gq}\ \omega_g].$$

The non-linearity of the model prevents the direct application of classical linear analysis techniques. Therefore, a small-signal representation is derived for a steady-state operating point as given by

$$\frac{d\tilde{x}}{dt} \simeq A\tilde{x} + B\tilde{u} \quad (51)$$

$$\tilde{y} \simeq C\tilde{x} + D\tilde{u} \quad (52)$$

where, for example, $A = \Delta_x f$ and $\Delta_x f$ denotes the Jacobean matrix of f with respect to x. This small-signal model will be used for small-signal analysis and time-domain simulation verification.

C. Small-signal stability analysis

1) Eigenvalue analysis: The small-signal stability analysis is investigated for the analytical small-signal state-space (ASS) model developed in (51) and the eigenvalues are calculated analytically. The resulting eigenvalues are presented in Table II. The system has 12 eigenvalues, among which 3 pairs are complex conjugates. Further, the participation factor analysis is carried out to identify the contribution of the states and the resulting associated states with the eigenvalues are shown in Table II. The first two pairs of eigenvalues, $\lambda_{1,2} = -7.85 \pm j4399.1, \lambda_{3,4} = -7.85 \pm j5027.4$ are associated with the state of the filter capacitor voltage and grid current with an oscillation frequency of 700 Hz and 800 Hz, respectively. The eigenvalues associated with the converter inductor current and current controller are a negative real value, thus, the oscillation frequency is zero. Four eigenvalues are related to the RSL from which one pair of the complex conjugate is associated with the current of the virtual inductor. This complex eigenvalue is well damped. The other two eigenvalues associated with the RSL integrator and filter are with negative real value which indicates that the frequency tracking performance will be well damped.

2) Impact of virtual impedance on the stability of the RSL: The performance and stability of the RSL depends on the design of the virtual impedance, therefore, a discussion is presented on the design principles of L_v and R_v, by presenting a trajectory of eigenvalue for a change of the virtual inductor. Fig. 7 shows the trajectory of the eigenvalues for a change of
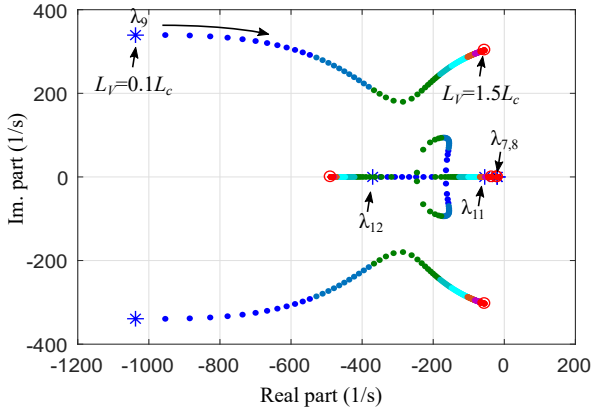
Fig. 7. Trajectory of eigenvalues for a change of grid virtual inductor, L_v from $0.10L_c$ to $1.50L_c$.

the virtual inductor, L_v. As presented in Section III.B, L_v is chosen to be 50% of the inverter series inductor L_c. Here the trajectory is presented for change L_v from 10% to 150% of L_c, while R_v is kept constant. As can be seen, the higher value of L_v, the eigenvalue, $\lambda_{9,10}$ associated with the state of virtual current, i_v is moving towards the right side of the eigenvalue plot. This means a higher value of the virtual inductor, the lower the damping part of the eigenvalue $\lambda_{9,10}$. In order to have sufficient damping of the eigenvalue $\lambda_{9,10}$, the virtual inductor should be small. λ_{11} and λ_{12} are two real-modes. It is noticed that if the virtual impedance ratio, $\frac{R_v}{2\pi 50 L_v}$ is kept larger than 1, λ_{11} and λ_{12} become oscillatory, on the other hand, the larger is the ratio, the better the damping is. In the design, the virtual impedance ratio, $\frac{R_v}{2\pi 50 L_v}$ is 0.64. It is also worth mentioning that the frequency and phase tracking speed depends on the RSL control-loop bandwidth. To have a fast-tracking speed, the crossover frequency ω_c in (40) can be selected higher depending on the inner-loop control bandwidth.

3) A comparison with standard second-order PLL: As the synchronization loop bring instability problem for a weak grid condition, the small-signal analysis is carried out for varying the grid impedance from 0.2 pu to 1.0 pu and the trajectory of the eigenvalues is shown in Fig. 8(a). As can be seen, the eigenvalues associated with the voltage of the filter capacitor, the current of the grid inductor and the current controller are moving towards the right direction, however, they are still in the left half-plane even for 1.0 pu value of the grid inductor, i.e., a very weak grid condition and stay stable. For a comparison with the PLL, a small-signal model of the system with the PLL is developed. The widely-used SRF PLL with a first-order low-pass filter as shown in Fig. 9 is used for comparison. The open-loop transfer function of the PLL can be given by [11]

$$T_{PLL-OL}(s) = \sqrt{2}V_o \left(k_p + \frac{k_i}{s} \right) \frac{1}{s} \qquad (53)$$

and, the closed-loop transfer function of the PLL can be given by

$$T_{PLL-CL}(s) = \frac{2\zeta\omega_n s + \omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2} \qquad (54)$$
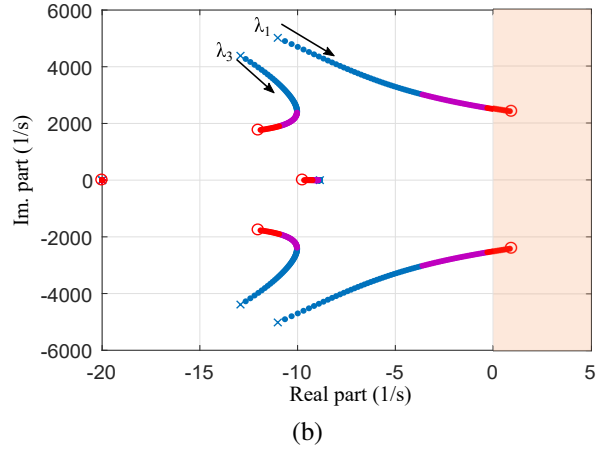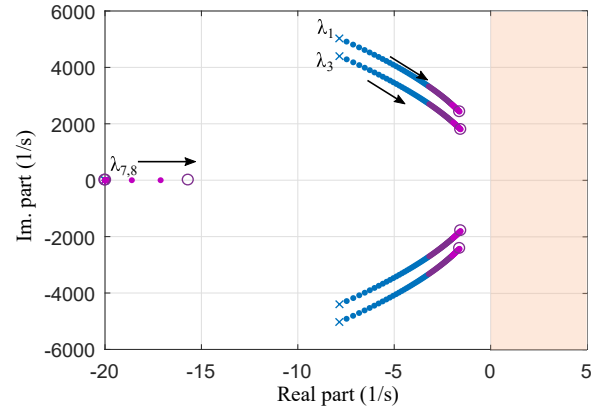

(a)

(b)

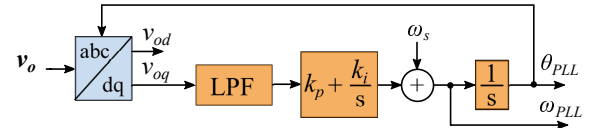Fig. 8. Trajectory of eigenvalues for a change of grid impedance from 0.2 pu to 1.0 pu: (a) RSL and (b) PLL.

Fig. 9. Standard PLL with a first-order low-pass filter.

where $\zeta = \frac{k_p}{2}\sqrt{\frac{\sqrt{2}V_o}{k_i}}$ and $\omega_n = \sqrt{\sqrt{2}V_o k_i}$.

The PLL is tuned such that the open-loop gain has a sufficient phase margin, i.e., $> 45^o$ while the bandwidth is sufficient enough to track the phase and frequency, and also rejects the high-frequency noise and operate stably in a weak grid condition. A detailed discussion on tuning the PLL can be found in [31]. The damping factor ζ is set to 0.707 to have the maximum flatness on the closed-loop frequency response and ω_n is set to achieve desired bandwidth of the PLL. Here, ω_n is set such that PLL has the same bandwidth as the RSL. $\omega_n = 2\pi 6.5$ gives $k_p = 0.5778$ and $k_i = 16.68$ for which the open-loop gain has a phase margin of 65.5^o at 10.1 Hz. Now the bandwidth of the PLL is the same as $f_c = 10$ Hz design of the RSL, which will be used for comparison. The detailed small-signal state-space modeling of the PLL has not been described due to the page limit, however, it can be found in [32]. The trajectory of the eigenvalues for the same grid
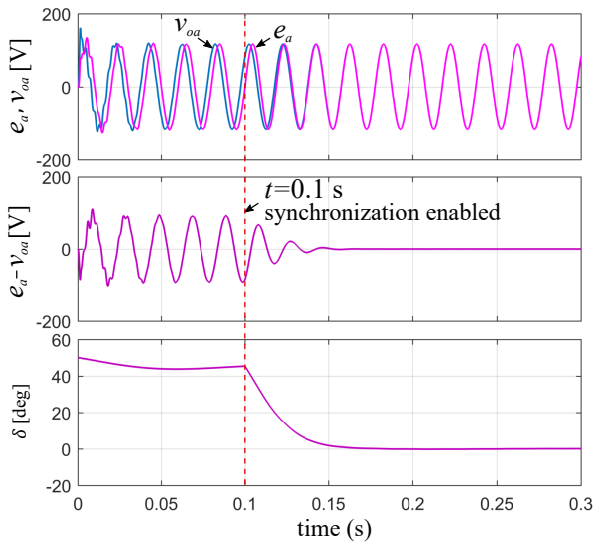
Fig. 10. Phase-A voltage of the PCC v_{oa} and RSL e_a, voltage difference, $v_{err} = e_a - v_{oa}$ and phase difference $\delta = \theta_e - \theta_o$: (i) simulation started at $t = 0\,s$, (ii) RSL is activated at $t = 0.1\,s$.

impedance variation is shown in Fig. 8(b). As can be seen, one pair of complex conjugate eigenvalues associated with the current of the grid inductor and the voltage of the filter capacitor moved to the right half-plane when the grid inductor is higher than 0.9 pu. By comparing the two trajectory plots in Fig. 8, the RSL shows a better immune from instability for a very weak grid condition.

V. VALIDATION OF THE PROPOSED RSL WITH A GRID-CONNECTED CONVERTER

In order to verify the effectiveness of the proposed RSL, simulation and experimental results are presented for a grid-connected converter. The converter is shown in Fig. 1 and the parameters of the system are given in Table I. The dc-side of the converter is connected to a dc source. The widely used standard vector control is adopted to control the converter as presented in IV-A.

A. Simulation result

The converter system has been implemented in MAT-LAB/Simulink association with the SimPower block-set with a detailed switching model of the converter and a sampling frequency of 10 kHz. Fig. 10 shows the synchronization process of the RSL with a grid-connected converter. The top plot of Fig. 10 shows the phase-A voltage of the PCC, v_{oa} and RSL, e_a; the middle plot shows the difference between these two voltages, i.e., $v_{err} = e_a - v_{oa}$ and the bottom plot shows the phase difference $\delta = \theta_e - \theta_o$ of these two voltages. As shown in Fig. 10, it has a phase difference between the RSL and PCC voltage is around 42° and a voltage difference with a peak value of around $90\,V$. The simulation is started at $t = 0$ s and the tracking-loop of the RSL is activated at $t = 0.1\,s$ to start the synchronization. Within a few cycles, the RSL voltage is synchronized with the grid. The RSL is able to track the phase of the grid voltage and the phase difference
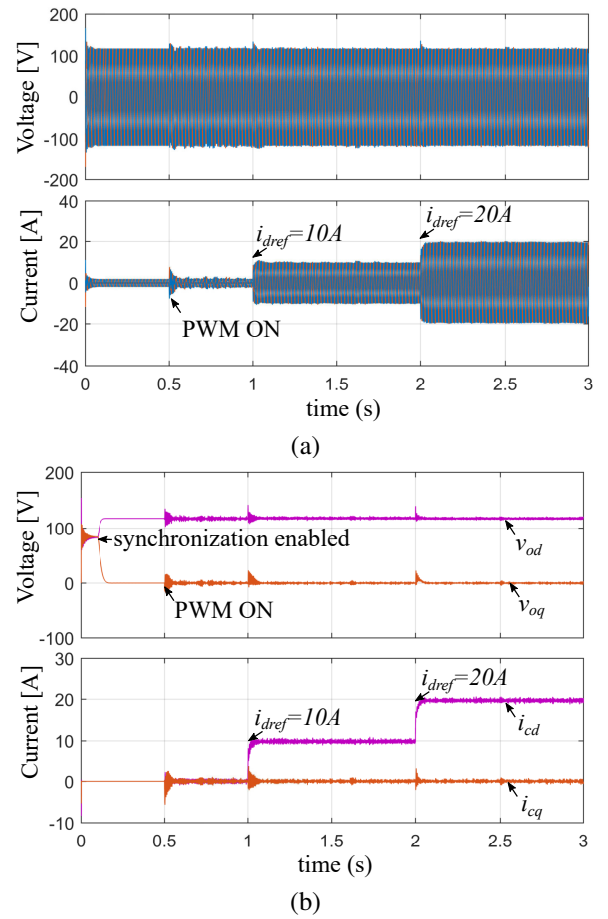

Fig. 11. Simulation result: (a) three-phase voltage, v_o and output current i_o and (b) the $d-$ and $q-$axis voltage and current of the converter.

δ becomes zero. Since the RSL tracks the phase of the grid voltage, the PWM of the converter can be enabled at any time to turn on the converter for grid connection.

Fig. 11 shows the complete simulation of the grid-connected converter. The simulation is started at $t = 0\,s$. The first 0.3 s of the simulation is presented in Fig. 10 where the tracking-loop of the RSL is activated at $t = 0.1\,s$. The PWM of the converter is enabled at $t = 0.5\,s$ after the synchronization is achieved. Since the synchronization is achieved, the grid connection is very smooth and there is no transient over-current.

Fig. 11(a) shows the three-phase instantaneous voltages and currents. Initially, the current reference is set to zero, i.e., $i_{d,ref} = i_{q,ref} = 0$ A. At $t = 1$ s, the d-axis current reference is to 10 A. The current controller follows the reference smoothly. At $t = 2$ s, another current step is applied. The controller quickly catches the reference and the system operates smoothly as expected. Fig. 11(b) shows the $d-$ and $q-$axis voltage and current of the converter. As can be seen, before enabling the RSL, the $d-$ and $q-$axis voltage are not a pure dc component, however, when the RSL is enabled to perform synchronization, the $d-$ and $q-$axis voltage becomes dc components where the $d-$axis voltage has a magnitude with a peak value of the voltage and the magnitude of the $q-$axis voltage is zero as it is set $e_q = 0$ in (21). The $d-$ and $q-$axis current components are also pure dc components as expected.
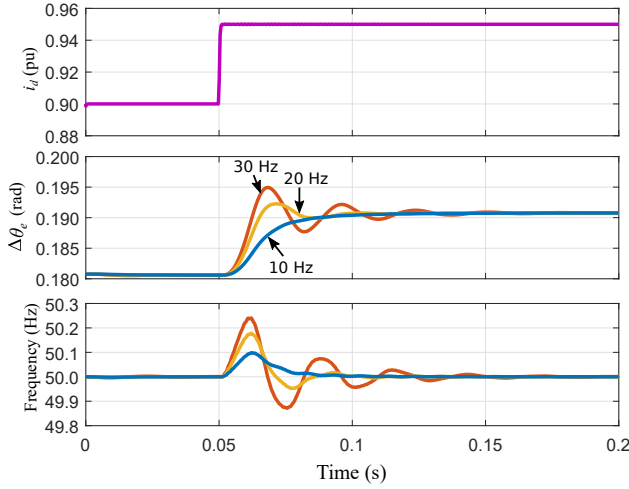
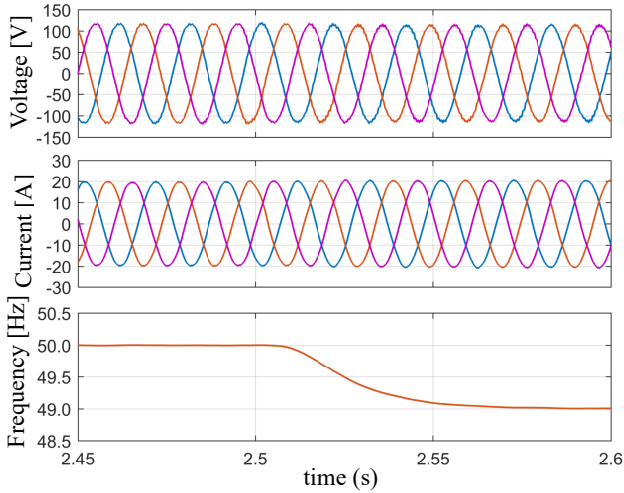Fig. 12. Performance comparison for three different crossover frequencies.

Fig. 13. Simulation result for a step change of frequency: (i) three-phase instantaneous voltage, v_o, (ii) converter current i_c and (iii) frequency of the RSL.

Fig. 14. A 20° phase jump of the grid voltage.

Fig. 15. Unbalanced and distorted grid voltage.

1) Impact of the control-loop bandwidth : As presented in section III-B, k_p in (40) is calculated for three crossover frequencies and the step responses of the closed-loop system is presented in Fig. 6 for these three designs. In order to further verify these responses, simulation results are presented in Fig. 12. As can be seen, the simulation results have the same response to the change of the d-axis current reference from 0.90 pu to 0.95 pu as the step responses shown in Fig. 6. The 30Hz and 20Hz designs have under-damped responses, and the 10Hz design gives over-damped response. Both 20Hz and 10Hz design are a good choice, however, only 10Hz design is used for the simulation and experimental results presented below.

2) Frequency and Phase Jump: The frequency tracking performance is tested by changing the frequency of the grid voltage and the simulation result is shown in Fig. 13. The bottom plot of Fig. 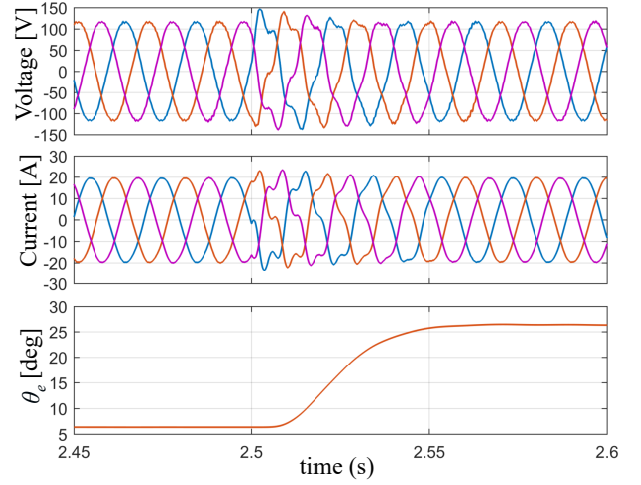1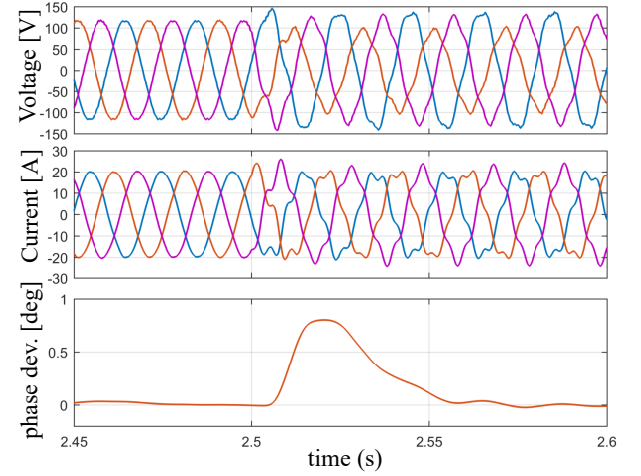3 shows the RSL frequency. The frequency of the grid voltage is reduced to 49 Hz at 2.5 s. As can be seen, the RSL follows the grid frequency. The frequency tracking performance is very fast and robust without any low/high frequency oscillation and overshoot. The instantaneous voltages and currents of the converter are also shown in Fig. 13. During the frequency change, the converter follows the reference current of the controller without any harmful transient.

The performance of the RSL has been tested for a phase jump of the grid voltage and the simulation result is shown in Fig. 14. A phase jump of 20° is applied in the grid voltage at 2.5 s. As can be seen in Fig. 14, RSL tracks the phase jump within two cycles and follow the grid voltage. Initially, the phase of the PCC voltage is 6.3^o. When the phase drift occurs, the phase becomes 26.3^o within two cycles i.e., 20° increased.

3) Unbalanced and distorted Grid Voltage: The next simulation is carried out for an unbalance and distorted grid voltage. The unbalanced and distorted grid voltage is created by injecting a 20% of negative sequence component at the fundamental frequency and a 5% 5th harmonic positive sequence
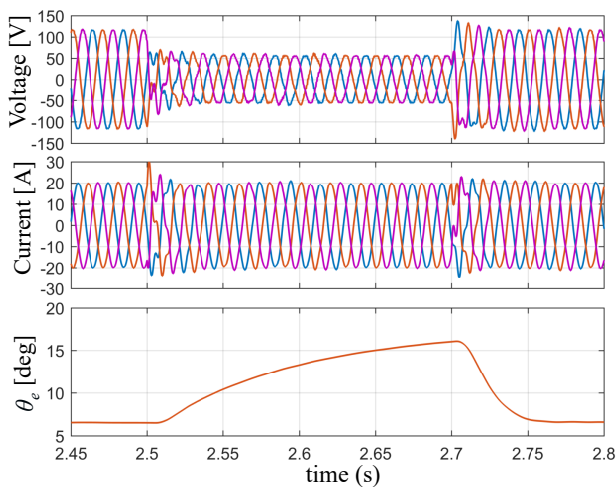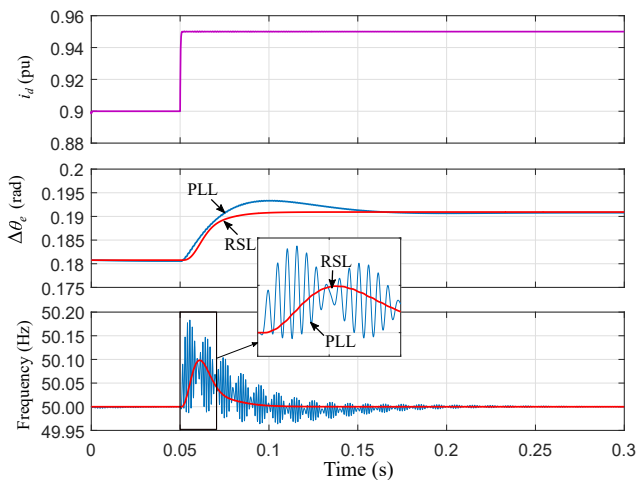
Fig. 16. 50% symmetrical voltage sag.

Fig. 17. Comparison with PLL for a step change of the converter current.

Fig. 18. Performance of the PLL under input frequency deviation from the fundamental frequency.

component. The instantaneous value of the voltages, currents and phase deviation are shown in Fig. 15. The transient phase error is around 0.8^o, which eventually becomes zero in steady-state. The phase difference is insignificant and does not have any significant impact on the steady-state operation of the converter.

4) Voltage Sag: The performance of the RSL has been tested for symmetrical voltage sag and the simulation result is shown in Fig. 16. A 50% symmetrical grid voltage sag is applied at 2.5 s. The instantaneous value of the voltages, currents and phase are shown in Fig. 16. As can be seen, the phase of the voltage is increasing during the voltage sag. When the grid fault is cleared at 2.7 s, the phase returns to it's pre-fault value within two cycles. RSL has not lost synchronization during this large disturbance.

B. Performance comparison with PLL

The performance of the RSL has been compared with a PLL as shown in Fig. 17. Here an average model of the converter is used so visualize the comparison by removing the high-
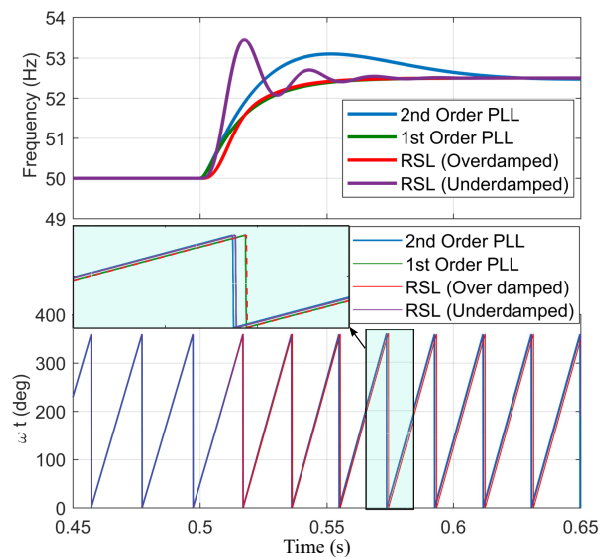
frequency oscillation caused by the PWM switching. As shown in the top plot of Fig. 17, the initial $d-$axis current is 0.90 pu. At 0.05 s, the $d-$axis current reference is set to 0.95 pu and the current of the converter immediately follows the reference. The middle plot shows the phase difference between the voltages of the grid and PCC. The initial phase difference for 0.90 pu current is 0.1808 rad, while it is 0.1909 rad for 0.95 pu of current. The phase tracking response of the RSL is well damped while it is under-damped with a small-overshoot for the PLL. If the phase margin of the loop is reduced, then it becomes under-damped with oscillatory behavior for the PLL, while it is well-damped for the RSL. The bottom plot of Fig. 17 shows the frequency obtained from the RSL and PLL. A first-order low pass filter with a cut-off frequency 500-rad/s is used with both the RSL and PLL. As can be seen, the frequency tracking performance of the RSL is smooth, while the PLL frequency has oscillation with frequency of 700 Hz (≈ 4399 rad/s) and 800 Hz (≈ 5027 rad/s). By looking at the eigenvalues in Table II, these two frequencies corresponding to the states of the grid impedance current and the filter capacitor voltages, which are reflecting on the PLL frequency while the proposed RSL effectively suppresses those oscillations.

The performance of the RSL has been investigated for the scenario when the input frequency deviated from the fundamental frequency and the results have been compared with first-order and second-order PLL as shown in Fig. 18. The results have been presented for two designs of the RSL, i.e., (i) under-damped ($f_c = 10$ Hz) and (ii) over-damped ($f_c = 30$ Hz) response of the RSL. As can be seen, phase ωt is the same as the first-order PLL when the RSL response is designed to be over-damped. However, phase ωt is the same as the second-order PLL for the under-damped response of the RSL. These phase differences do not have any significant impact on the converter operation.

As shown in Fig. 8, the PLL is more prone to instability in
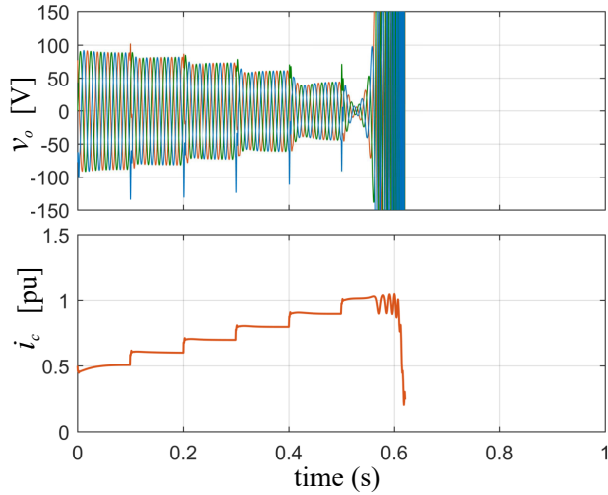
(a)
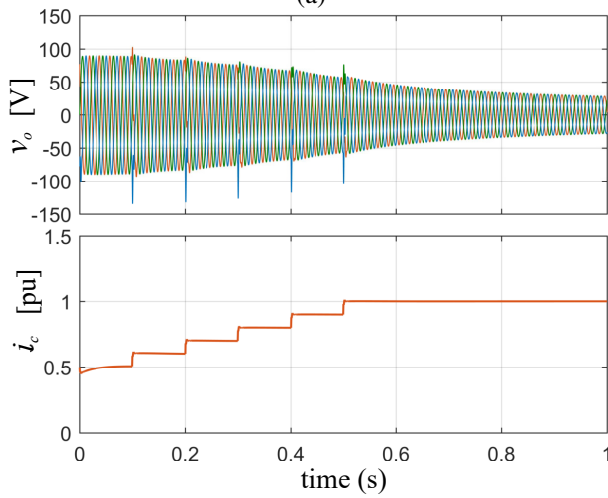
(b)

Fig. 19. Comparison with PLL in a weak grid condition: (a) PLL performance and (b) RSL performance.

weak grid condition than RSL. A simulation is carried out to see the performance as it is noticed in the eigenvalue analysis. The grid impedance is set to 1 pu. The simulation results are shown in Fig. 19. The current reference is set to 0.5 pu initially which has been increased to 1 pu with a step of 0.1 pu as shown in Fig. 19. As can be seen, the system becomes unstable with PLL synchronization, while it is stable with RSL and the voltage magnitude is reduced significantly as there is no voltage support function implemented in the control.

The voltage magnitude dependency on the control-loop frequency response is the root cause of instability for the PLL under a weak grid (high impedance) condition [33]. From the PLL transfer function in (53) and (54), it can be noted that the magnitude of input voltage has a significant influence on synchronization-loop stability. The PLL will always be stable under a strong grid as the PCC voltage is unaffected by the power injected by the converter. However, the PCC voltage will change a lot with the variation of injected power under a weak grid condition, which causes the instability with the PLL synchronized converter. The transfer functions of the
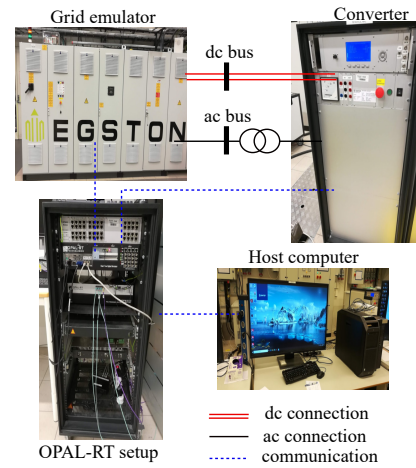

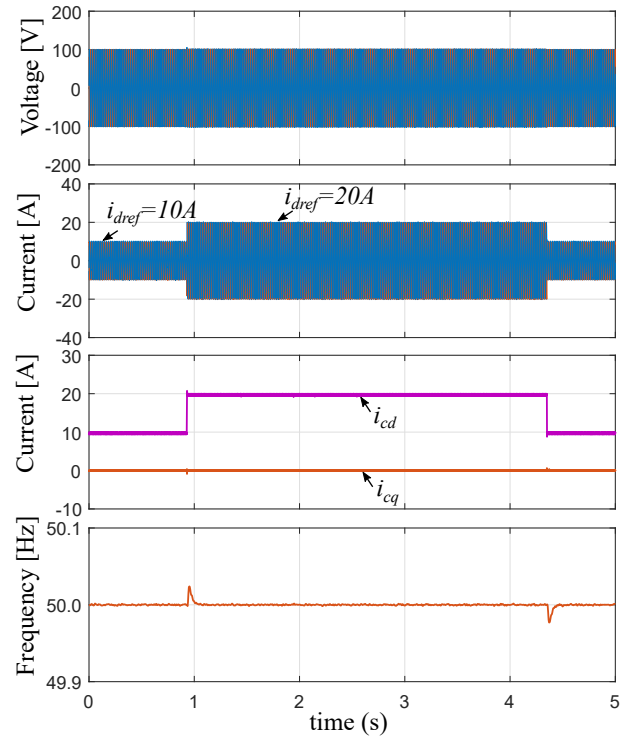Fig. 20. Experimental setup used in this work.

Fig. 21. Experimental result for a step change of current reference: (i) three-phase instantaneous voltage, v_o, (ii) converter current i_c, (iii) $d-$ and $q-$axis current of the converter and (iv) frequency of the RSL.

RSL in (38) and (41) show that the stability of the control-loop depends on the R_v and L_v rather than the PCC voltage magnitude. The PCC voltage magnitude influences the gain of the RSL transfer function. Therefore, the RSL shows a better immune from instability for a weak grid condition.

C. Experimental result

In order to further verify the effectiveness of the proposed RSL, experiments have been conducted for the system presented in the simulation. The parameters of the experiment are
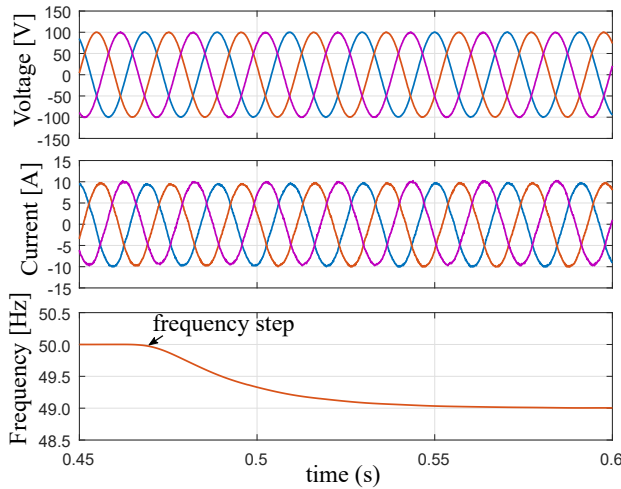
Fig. 22. Experimental result for a step change of frequency.

the same as the simulation given in Table I. Fig. 20 shows a picture of the experimental setup. A two-level converter is used in the experiment. Both the ac-side and dc-side are connected to a grid emulator. The current controller of the converter is implemented in the local FFGA-core in the converter and RSL is implemented in the OPAL-RT system. The converter and the grid emulator are controlled by OPAL-RT and they are connected by optical fiber communication. Two experimental results are presented here. Fig. 21 shows the three-phase instantaneous voltages and currents, the $d-$ and $q-$axis current and the frequency of the RSL. After the synchronization is achieved, the PWM of the converter is turned on and the $d-$axis current reference is set to 10 A. A current step is applied and the controller follows the current reference. The RSL works satisfactorily.

The frequency tracking performance is also tested in the experiment by changing the frequency of the grid voltage and the experimental result is shown in Fig. 22. The frequency of the grid voltage is reduced to 49 Hz. As can be seen, the RSL follows the grid frequency. It shows that RSL follows the frequency of the grid in 3 cycles. The frequency tracking performance is very fast and robust without any low/high frequency oscillation and overshoot.

VI. Conclusion

This paper presents a new phase-tracking robust-synchronization-loop for the grid-connected DG converters. Analytical modeling, as well as a method for tuning the parameters, is presented. A small-signal stability analysis is presented and it is shown that the eigenvalues associated with the RSL always stay in the left half-plane, which indicates that the RSL will always be stable itself. The performance of the RSL has also been compared with widely used PLL and the RSL shows a better immune than a PLL from instability for a very weak grid condition. Simulation and experimental results are provided to show the effectiveness of the proposed method in tacking the phase and frequency of the grid. The result shows that the proposed method effectively tracks the

phase and frequency of the grid voltage and maintains the synchronism of the converters during different disturbances.

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