Master's thesis

NTNU
Norwegian University of Science and Technology
Faculty of Information Technology and Electrical Engineering
Department of Electric Power Engineering

Dalina Krasniqi

Dual Active Bridge Converter

Master's thesis in Electric Power Engineering
Supervisor: Dimosthenis Peftitsis
Co-supervisor: Gard Lyng Rødal, Yoganandam Vivekanandham Pushpalatha

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Abstract

With a wide range of applications, the isolated bidirectional DC-DC (IBDC) converters have caught the attention of many researchers, among which the most prominent topology is the dual active bridge (DAB) converter. This converter topology requires a thorough study in terms of its operation to further improve the performance of the DAB converter. An estimation of the losses was conducted for the Loss DAB model where this appraisal was conducted both analytically and simulation based. The aim of this study was on observing and comparing these results to provide more data in regard to the losses. The methodology chosen for this analysis was estimating the conduction and switching losses for a varying phase shift value, for when the dead time was and was not present. The results obtained showed that there was a clear difference between the two approaches which increased for the dead time consideration and for lower phase shift values. This was ascertained to happen due to required assumptions made and the lack of consideration of the varying drain to source on state resistance for the analytical estimation of the losses. The body diode losses were observed to be very small compared to the Metal-Oxide Semiconductor Field Effect Transistor (MOSFET) losses since the body diode conduction time was far less than the aforementioned switches, and the switching losses were neglected due to the lack of data.

One important outcome of the analysis was the observation of the zero-current switching (ZCS) presence for the zero-voltage switching (ZVS) boundary of the DAB converter corresponding to a phase shift of D=0.19. This operation region of the converter resulted in Zero Switching losses during turn-on and turn-off of the power devices in the secondary H-bridge. This occurrence led to the ZVS analysis performed in the second stage of the project.

From the results obtained in the previous stage, the ZVS capability of the converter was studied to define the operating region of the DAB converter which would allow for lower switching losses. The working principle of the DAB converter for different scenarios and operating conditions, (with and without the presence of parasitic capacitors and different phase shift operating regions), were presented in this thesis. This approach provided the conditions for realizing ZVS of the switches of this converter where the conduction of the body diode was found to be necessary to allow for ZVS. The required parameters such as, inductor current and dead time, directly affected the ZVS operation of the switches. For instance, when the inductor current was lower than the calculated minimum inductor current to achieve ZVS, the parasitic capacitors would not charge and discharge completely. The shorter dead time compared to the resonance time, the charging and discharging time required for these capacitors, would result in hard switching or in partial zero voltage switching of the switches.

The ZVS boundary was set to define the ZVS operating region of the DAB converter where three phase shift values were used as references. For the boundary operation of the converter D=0.19, and for high phase shift region D=0.3, ZVS was provided for both bridges of the converter since from the relation of the phase shift and corresponding gain, the DAB converter operated within the ZVS region. The low phase shift operating region, D=0.1, for when the converter operated in Buck Mode, resulted in the secondary bridge losing its ZVS capability. When the voltage gain, G=1, the ZVS was achieved for all phase shift regions independent of the other conditions. For the DAB model used in this thesis this was only true for when D=0.5 where the input voltage was equal to the output voltage.

Sammendrag

De mange bruksområdene til den isolerte toveis DC-DC-omformeren har fanget oppmerksomheten til industrien, og den mest lovende topologien av disse er Dual Active Bridge(DAB) omformeren. Denne omformertopologien krever videre forskning på dens drift, for å kunne utvikle ytelsen på DAB-omformeren videre. I masteroppgaven har tap blitt beregnet for en Loss DAB Model, både analytisk og simuleringsbasert. Målet med denne studien er å observere og sammenligne disse resultatene, og gi mer data med hensyn til tap som denne omformeren genererer. Metodikken som var valgt for denne analysen var beregning av ledetap og svitsjetap for varierende faseforskyvningsvinkler, med og uten å ta hensyn til dødtid i svitsjingen. De oppnådde resultatene viste at forskjellen mellom de to tilnærmingene var betydelig, og den økte når dødtid ble tatt hensyn til, i tillegg økte den for avtagende faseforskyvningsvinkel. Forskjellen oppstod på grunn av neglisjering av den varierende $R_{DS(on)}$ i den analytiske beregningen av tapene. Diodetapene ble observert til å være veldig små sammenlignet med Metal-Oxide Semiconductor Field Effect Transistor (MOSFET) tapene, siden diodens ledningstid var langt mindre enn de nevnte bryterne, og svitsjetapene ble neglisjert på grunn av mangel på data.

Et viktig resultat av analysen var observasjon av nærvær av zero current switching (ZCS) for zero voltage switching (ZVS) grensedrift av DAB-omformeren, som tilsvarte når D = 0,19. Dette driftspunktet for omformeren førte til null svitsjetap under turn-on og turn-off av bryterne på sekundær H-broen. Basert på disse resultatene, ble det videreført en analyse av ZVS i den andre fasen av prosjektet.

Fra de oppnådde resultatene fra første trinn, var det nødvendig å definere ZVS-driftsområdet for DAB-omformeren basert på dens ZVS-evne, for å muliggjøre lavere koblingstap. Virkemåten til DAB-omformeren ble presentert i masteroppgaven for forskjellige driftsforhold og scenarier, altså med og uten å ta hensyn til parasittkondensatorer og ved forskjellige faseforskyvninger i driftsregionene. Basert på denne analysen, ble det lagt merke til at diodene i omformeren måtte lede når bryteren skrudde seg på, for å kunne realisere ZVS. Parametere som spolestrøm og dødtidslengde påvirket driften under ZVS. Hvis spolestrømmen var mindre enn hva som var blitt beregnet som minste spolestrøm i denne oppgaven, ville det føre til at parasittkondensatorene ikke var i stand til å lade seg opp eller tømme seg helt. Den korte dødtidslengden i forhold til resonanstiden, altså ladings- og utladingstiden som kreves for disse kondensatorene, resulterte i enten i hard svitsjing eller delvis ZVS for bryterne.

Videre ble ZVS-grensen spesifisert, for å kunne definere ZVS operasjonsområdet for DAB-omformeren, ved bruk av tre ulike faseforskyvninger som referanser. For grensedrift av omformeren ved D = 0,19, og for høye faseforskyvningsområder ved D = 0,3, ble ZVS oppnådd for begge omformerbroene. Dette ble oppnådd på bakgrunn av studien av forholdet mellom faseforskyvningen og dens tilsvarende gain, G, i DAB-omformeren. Ved å operere omformeren med lav faseforskyvning i driftsområdet D = 0,1, tilsvarte det at omformeren opererte i Buck modus, noe som resulterte i at den sekundære bruen mistet sin ZVS evne. Da G=1, ble ZVS oppnåelig for alle faseforskyvningsregioner uavhengig av andre tilstander, noe som kun var mulig å oppnå for DAB-modellen i denne masteroppgaven når D = 0,5, som tilsvarte at inngangsspenningen var lik utgangsspenningen.

Preface

This thesis concludes my studies in the International Electric Power Engineering Master Program at Norwegian University of Science and Technology in Trondheim. Through the specialization project and this thesis, I was able to specialize in Power Electronics which was truly a captivating subject.

I would like to thank Professor Dimosthenis Peftitsis for allowing me to write my thesis in such an interesting applicable topic as well as my two Co-supervisors Yoganandam Vivekanandham Pushpalatha and Gard Lyng Rødal. They both have assisted me through my Thesis and Specialization Project with patience and dedication. Their hard work and passion towards the topic provided me with the right guidance on writing this Master Thesis.

The two years of studying at NTNU were both challenging and rewarding. The assistance provided by all the Professors, PhD Candidates, Scientific Researchers and Student Assistants have paved the way for me to complete my studies successfully and therefore I want to thank them for their contribution.

A huge appreciation goes to my parents and brothers for guiding me though every step in my life and supporting me throughout my studies. Their wise counsels and supporting words have always motivated me to work hard towards reaching my goals and for that I am truly grateful.

Trondheim, June 2021

Dalina Krasniqi

Problem Description

The increasing demand of renewable energy sources has resulted in an immense increase of power electronic applications. Mainly, DC-DC Converters are required to regulate the output voltage that these renewable energy sources generate and for the storing of this energy in energy storage devices. This is necessary since the renewable energy sources are characterized by their unstable energy production due to its close dependency on nature.

The IBDC Converters allow for bidirectional power flow and among them the most well-known topology is the Dual Active Bridge converter. This converter is highly applied in automotive applications like electric, hybrid and fuel cell vehicles. Their high applicability comes along with the increasing demand of optimizing the operation of this converter. This thesis focusses on achieving this goal by studying the losses generated by this converter at different points of operation and studies the ZVS capability of the converter which directly effects the switching losses.

To obtain the losses generated by the DAB converter, an analytical and simulation-based approach should be conducted in order to provide comprehensive data for the analysis conducted. The modulation scheme that should be applied to the DAB converter is the Phase Shift Modulation Scheme due to its simple working principle which would allow to easily detect the effect of the varying phase shift on the losses generated by the converter. This insight is required to study the DAB converter for different working conditions which would allow to study the phase shift regions that provide lower losses.

The switching devices provide both conduction and switching losses which should be estimated separately where input from the datasheet of the switching devices chosen is necessary for both approaches in this task. To obtain the simulation results, the DAB model should be built in a simulation software window whereas for the analytical approach a programming language would be needed in order to provide these calculations in a more effective way.

The switching losses are closely related to the ZVS property of the DAB converter. Therefore, this property should be further analyzed in terms of the conditions of realizing the ZVS of the switches. An analytical approach should be used for this method if the time is not sufficient and if the simulation software used does not provide the required tools to study this property of the converter. This study should be conducted to define the ZVS operating region of the DAB converter which would contribute to lower losses. This analysis should result in a broader comprehension of the DAB converter operation under ZVS conditions.

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List of Abbreviations

IPCC	Intergovernmental Panel on Climate Change
CO_2	Carbon Dioxide
DC	Direct Current
IBDC	Isolated Bidirectional DC converter
DAB	Dual Active Bridge
MOSFET	Metal-Oxide Semiconductor Field Effect Transistor
Si	Silicon
SiC	Silicon Carbide
HFT	High Frequency Transformer
SPS	Single Phase Shift
ZVS	Zero Voltage Switching
ZCS	Zero Current Switching
RMS	Root Mean Square
PLECS	Piecewise Linear Electrical Circuit simulation
SPS	Single Phase Shift
EPS	Extended Phase Shift
DSP	Dual Phase Shift

1 Introduction

1.1 Problem Background

The focus on renewable energy production is increasing continuously, mainly due to the need for of substituting the emission-related energy sources such as power plants, coal fired and nuclear power-based energy production. According to IPCC (Intergovernmental Panel on Climate Change), 37% of global emission is caused by electrical energy production. This accounts for 10 gigatons of CO_2 which is expected to increase with the increase in power demand. This emission rate can be reduced by substituting the traditional energy sources with renewable energy sources [1].

Methods such as minimizing the consumption and increasing of the efficiency of the power plants have been attempted throughout the years. Yet the promising future of renewable energy has now turned the tables towards other approaches. The most prominent renewable energy sources are wind, solar and hydro power which allow for low emission energy production, and they resolve the concern of the drain of non-renewable energy sources.

These renewable energy production sources are characterized by low emission and their sustainability and are closely related to the environmental conditions. This allows for the energy production to vary throughout the day which requires a regulation to maintain a smooth and continuous power flow. In cases when it is to be connected to a grid, the voltage level should be regulated and matched to the voltage level of the bus. A sunny day could result in excessive energy production generated by the solar panels as would a high wind activity day provide high energy production by the wind farms. This excessive energy has to be stored in energy storage system which can be used when there is a drop in energy production by these sources. This process, voltage regulating and smoothing of power flow, will require bidirectional DC-DC Converters [2].

These renewable sources are not accessible everywhere or simply not efficient enough in different locations to meet the required power demand. For this reason, interconnecting grids to transfer power is important so the renewable energy can be used even in places where it is not the best option compared to power plant energy production. The interconnection, as mentioned, requires matching voltage levels which is made possible by DC-DC Converters and since the power will have to flow in two directions between the grids, bidirectional DC-DC Converters are required to satisfy this.

1.2 Bidirectional DC-DC Converters and DAB Converter Application

The storage systems for the renewable energy systems require bidirectional DC-DC converters which allow for the power to flow in two directions, and they can serve as interface between the energy storage device in these applications [3]. The interconnection of different grids is also made possible by these converters where they can boost or lower the voltage and ensure a constant output voltage. The transformer which is present in these converters, ensures galvanic insulation [4].

The bidirectional DC-DC converters are mostly used in power distribution systems and in automotive applications like electric, hybrid and fuel cell vehicles. There is a constant increase in the demand of these vehicles due to the low emission, which has caused the increase in demand on these converters as well. Other areas where these converters are broadly applied are renewable energy generators, aerospace applications and personal electronic equipment.

This broad application of these converters comes because of its noteworthy properties. Among these properties are the electric insolation provided by the transformer for IBDC Converters, the light weight and as mentioned, the bidirectional power flow [5].

These converters are available in different topologies which allows for them to provide different functions and services in accordance to their structure and components. This is one of the reasons why they are widely used where among these topologies is also the Dual Active Bridge converter. This topology of IBDC converter is mostly applied in automotive applications and is known for its high-power feasibility.

The DAB converter has the soft switching capability which allows for ZVS switching resulting in low switching losses and it operates with high switching frequency. Light weight and high efficiency are also among the merits of this topology. These properties have resulted in an increase in number of researches resulting in the improvement of the performance, broadening the application area of this converter. The future in renewable energy is promising and the DAB converter is already playing an important role in this development.

1.3 Project Description and Objectives

The most eminent merits of Dual Active Bridge converter are the low losses and Zero Voltage Switching capability. Therefore, this thesis aims at estimating the losses of a DAB converter by using an analytical and simulation-based approach and analyzing the ZVS capability of this converter. This will provide useful data regarding the DAB converter and its ZVS operating conditions.

The estimation of losses requires understanding of theoretical approach and deep perception of effects that the converter components have on these losses. Therefore, firstly the analytical calculations of the losses should be performed which can later be used as a reference to check the model build in PLECS. This approach provides good results without the need of building or using a software model. Yet, this thesis presents them in line with the simulation-based results to outline the accurate results.

Estimation of the conduction and switching losses are the focus of this thesis, where other losses are neglected, such as the transformer copper and core losses which might become dominant at higher frequencies. In the analytical approach, the switching losses are estimated by the help of the datasheet of the MOSFETs, which does not allow for accurate results due to inaccurate extraction of values. A method to overcome this obstacle is by using simulation-based approach where the data provided by the datasheet of the MOSFET can be accurately implemented for accurate results. Therefore, this thesis obtains both the conduction and switching losses by using the simulation approach. In the analytical approach, the conduction losses are calculated by considering the parameters of the converter and input values from the switching device datasheet, the drain to source on resistance which does not consider the junction temperature variation, leading to lack of precision in this approach. The switching losses are also obtained by the use of the MOSFET datasheet where by referring to the current during the turn off transition, the switching energy is found. This data allows for estimation of the switching losses during turn off transition of the switches. The turn on switching losses are considered to be zero in this thesis since ZVS is assumed during turn on of the power devices due to the DAB converter property.

Simulation based estimation of losses is also an important part of this thesis and for this approach, the PLECS software is chosen to be used since this software provides the required functions to accurately implement and build the DAB model. This will also show the promising functionality and merits of using this software which is one of the objectives of this thesis.

Comparison of the results obtained when estimating the losses from the different approaches is an important part the thesis where the comparison of the approaches provides insight on the merits and demerits of both methods and ensures the accuracy of the approaches.

This estimation of losses will allow to notice the ZVS Capability for different phase shift values and in both bridges since these losses are closely related to the switching behavior of the power devices. Therefore, this thesis presents and analyses the theory behind ZVS capability of the DAB converter and calculates the required parameters and conditions for the switches to operate at ZVS. The objective of this part of the project is to define the ZVS operation and its boundary condition and the approach chosen for the calculations of the requirements for this study is the analytical approach.

The ZVS boundary determines the ZVS operation of the DAB converter and on that account, this boundary is built. Various operating points of the converter are studied in terms of this boundary where three main phase shift values are chosen as a reference and presented in terms of this boundary.

Throughout this thesis, the phase shift modulation scheme is used, as one of the most prominent modulations schemes of the DAB converter. The phase angle is varied for all the tasks performed in this thesis to analyze the behavior of this converter operating at different phase shift values. This approach allowed for interesting review regarding the total losses of the converter and the ZVS capability where these observations are noted and highlighted throughout this thesis.

1.4 Scope and Limitations

The goal of this thesis is to define the main properties of the converter and analyze them for different operating condition in order to provide more data and point out the aspect of the DAB converter that are open for further research. The properties of interest in this thesis are the losses and ZVS capability.

The tasks are performed both by analytically and through simulations using the software PLECS. The analytical approach for estimating the losses required assumptions and did not consider variation of the parameters due to the junction temperature. This is not an issue for the simulation approach which provides the required tools for creating a control loop regarding these varying parameters allowing for more accurate results.

One of the goals of this thesis was to compare the results of these approaches with the results obtained from the experimental approach where a DAB prototype was to be used. As the laboratory setup was not ready in time, this experiment part was not conducted.

The ZVS was studied in analytical approach but with no simulation-based results since the PLECS software did not provide the required functions to give this data.

1.5 Methotology

Firstly, the parameters of the DAB converter are designed, and the switching devices are chosen according to the maximum operating condition of the converter.

Since losses are directly related to the DAB converter properties and affect the operation of the converter, they are estimated to provide more data regarding the losses generated by the DAB converter. The approaches chosen for estimating these loses are analytical and simulation based. For the analytical approach, the calculations are performed by creating a MATLAB script with input from the DAB converter parameters used in this thesis and from the chosen MOSFETs datasheet. The results obtained are presented by tables and plots.

To obtain the simulation results, the DAB converter model is built in PLECS software and used for further evaluation in this thesis. The data provided by the MOSFET datasheet is accurately implemented using the thermal library function that PLEC provides. This thermal library is responsible for providing the required data for estimating the losses generated by the power devices.

Ripples are present on the output voltage, and they cause variation on the generated losses for varying phase shift values on the Secondary Bridge. The effect of these ripples is not visible in the analytical approach. Therefore, the simulation approach, where PLECS estimates the losses in terms of the voltage current relation, is important to be conducted to observe the differences between the results in the approaches for the Secondary Bridge.

This thesis aims at comparing and differentiating the aforementioned approaches and in order to easily reach this goal, MATLAB plots were built to visualize the results obtained from both approaches. This method allowed for an easier observation of the results from where the conclusions regarding this part of the thesis took base.

Since the switching losses are closely related to the ZVS capability of the switches, there is a need to analyze this property of the converter. Therefore, an ZVS analysis was conducted where the ZVS Boundary was defined in an analytical approach. Minimum inductor current, the dead time length and the diode conduction are the parameters and conditions of interest which allow for zero voltage switching. These conditions were studied and defined in terms of different operating conditions of the converter. This allowed to better establish ZVS operating region of the DAB converter.

1.6 Background Work

The specialization project created the base of better understanding the DAB converter and its operation. The focus of that project was on conducting a literature review on the DAB converter topologies and pointing out the merits and demerits of each promising topology.

The single-phase and the three-phase topologies were found to be the topologies that were highly applicable and therefore these topologies were an important part on that project. Later through the report, the single-phase DAB converter topology was chosen to be the most promising topology in terms of the goal of specialization project. For this topology, the parameters were designed by choosing a reference application.

The working principle was presented in terms of output voltage and the inductor current for one switching period. This allowed for a better understanding of the DAB converter operation.

The goal of the Specialization Project was analyzing the transferred power in terms of the Single-Phase Shift Modulation Scheme. Two approaches were chosen for this analysis, the analytical and simulation approach where a PLECS Model was built to obtain the simulation results. The model used for this study was a lossless model where the reason behind using this model was to focus on the transferred power in terms of the modulation scheme effect rather than the effect of the losses on the power flow.

The results obtained showed that for a phase shift D=0.5, the maximum transferred power was achieved where the output voltage and input voltage were equal. No power transfer was achieved when the phase shift was D=0. From the plot build in MATLAB, Appendices , it was evident that with the increase of the phase shift angle, the transferred power would also increase.

The effect that the resistive load and the output capacitors had on the transfer power were observed in the PLECS model and presented by the generated plots by PLECS and MATLAB for different phase shift values, Appendices.

A comparison of analytical and simulation results was also conducted where the difference was noted to be very small, proving so the accuracy of both methods. The further work goal of the specialization project was on building a Loss DAB model and further analyzing its operation by estimating the losses.

The ZVS property of the converter was briefly introduced in this project where the zero-voltage switching concept was presented with aim of expanding far more on the concept in future work.

Based on the results obtained from this project and the observations made, the Master Thesis ideas and studies were developed.

1.7 Chapter Overview

This thesis is organized into 5 chapters where each chapter includes different studies and fulfills different goals of the thesis. The last sections are reserved for the references used throughout the report and appendices.

Chapter 1 presents the background of this thesis by looking at the application on the bidirectional DC-DC converter and later emphasizing the most prominent, the Dual Active Bridge converter. This converter is briefly presented alongside its merits and application area. The project description and the scope of the work are a part of this chapter which elaborate on the goals and aims of this thesis and the approaches used in order to achieve of these goals. The limitations and a summary of the background work is also introduced in this chapter.

Chapter 2 presents the DAB converter topologies and its merits over other IBDC converters. The working principle of this converter is also described which is required to understand the operation of the converter. The modulation scheme used, the single-phase shift modulation scheme, is briefly explained in this section. The design of the DAB converter parameters along with the choice of the switching device is also a part of this chapter which provides the DAB model used in the Thesis. The Sic and Si base power devices take an important part in this chapter where the merits and demerits of these materials are presented alongside with their availably.

Chapter 3 deals with the estimation of the losses. Both approaches, analytical and simulation approaches are conducted in this chapter where the process of obtaining the results is described and the results are presented. This chapter focuses on observations from the obtained results and presents the merits and demerits of each approach. An important contribution is made in this section regarding the boundary operation of the converter where low losses are obtained. The zero switching losses on secondary bridge is obtained for this boundary operation which is further discussed. The comparison of the results obtained from the two methods covers an important part of this chapter where conclusions are based on these observations.

Chapter 4 deals with the ZVS operation of the DAB converter. In this chapter the working principle of the converter in terms of ZVS capability for different operating scenarios are presented. The conditions for providing ZVS are defined and analyzed from where the ZVS boundary is obtained. The ZVS operation of the DAB converter for different phase shift values were tested in terms of this ZVS boundary and commented in this chapter.

Chapter 5 presents the outcome of this thesis by discussions and observations. Conclusions are made in terms of the observed results and suggestions for further work are presented in this chapter.

2 DAB Converter

2.1 Literature Review

The main categorization of the DC-DC converters is that of having or not a galvanic insulation. The function of the DC-DC converter is dependent on the presence of the galvanic insulation where for purposes such as interconnecting two DC systems that operate at same voltage level and same configuration, the converter without galvanic insulation is required. Whereas when the direct current paths have to be blocked, the DC-DC converter with galvanic insulation is required where this insulation is typically provided by a Transformer connected in between the two subsystems [6].

These DC-DC Converters with galvanic insulation are categorized in two main groups, single stage and two stage topologies where the difference between these two groups of DC-DC Topologies are the number and type of components where in Figure 1 there is a representation of the IBDC converter single stage components.

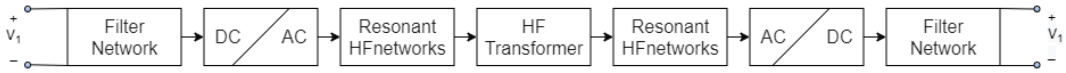

Figure 1 Single Stage IBDC Converter Components

The main topologies of this single stage DC-DC converter Topologies together with their merits and demerits are presented in the Appendices where the DAB converter catches the attention due to its visible advantages such as low switching losses which is provided by the soft switching capability that this converter has and the high switching frequency which allows for smaller and lighter weight for the transformer. The number of switches that this converter has is also a part of the merits of the DAB converter since the transmitted power of an IBDC is proportional to the number of switches which consequently allows for higher power feasibility [7]. The DAB converter itself comes with a variety of topologies where the three-phase and single-phase topology are the most prominent ones.

The three-phase topologies come with its advantages and disadvantages where the large number of switches and the difficulty in designing a symmetrical three-phase transformer are among the disadvantages of this topology. But the low device stress and reduced current ripple are among the merits of this topology that make it applicable in many applications [8].

The single-phase topology is mainly known for its merits such as the low number of passive components, evenly shared current between the switches, soft switching properties and high-power density. These and the fact that the three-phase topologies allow for high switching and conduction losses are the reason why in this thesis, the Single-Phase DAB converter Topology is used. Other topologies other than the traditional DAB converter topology are available but the traditional Topology is to be used in this Thesis due to its simple strudture.

2.2 Working Principle and Modulation Scheme

The purpose of the DAB converter is to transfer power and it is important to select the right modulation scheme which is easy to control to obtain the desired output.

The fact that this converter is composed by two full bridges can make the control a little complicated, but it also allows for different types of modulation schemes where the most prominent ones are Single Phase Shift (SPS), Extended Phase Shift (ESP) and Dual Phase Shift (DSP) modulation. In SPS modulation, power flow control is done by the phase shift angle which is represented by the following equation:

$$P = \frac{nU_1U_2}{2f_{sw}L}D(1-D) \qquad \textbf{2-1}$$

where D=0 corresponds to the phase shift angle zero and D=0.5 to phase shift angle $\frac{\pi}{2}$.

In this modulation scheme, and in other modulations as well, the duty ratio is kept constant d=0.5 and the power transfer is controlled by changing the phase shift ratio. The advantages of this control strategies are small inertia, high dynamic and soft switching control, though the losses are high. The other strategies such as ESP, is an improved SPS control that in addition to the outer phase shift has an inner phase shift which results in an enhancement to the regulating flexibility. ESP is further discussed in [9] where this control strategy is proposed for power distribution in micro grid. A theoretical and experimental analysis was performed and some of the features found were that it had expanded regulation range and improved system efficiency. DSP is also a control strategy widely used and is known for its ability to decrease current stress and improve efficiency. Two control degrees are required of EPS and DPS ,whereas for SPS only one control degree is required [10].

This thesis does not focus on a certain application of the DAB converter, instead it focuses on a general application. This allows for the attention to be on the DAB converter operation rather than on its application. For this reason, the simplest modulation scheme is used which is also highly applied due to its simple principle of operation, the Single-Phase Shift Modulation Scheme. This modulation scheme is the simplest to be implemented in a digital processor and the one that enables the easiest controllability of the converter. This is due to the fact that it only requires to adjust only one parameter, compared to the other modulation schemes that require more than one controllable parameter, which makes it easier to develop the analytical expressions.

The DAB converter is composed of two full bridge converters which are connected through a High Frequency Transformer and coupling inductor where H-bridge 1 acts as an inverter and H-bridge 2 as a rectifier when looked from the primary side of the DAB converter.

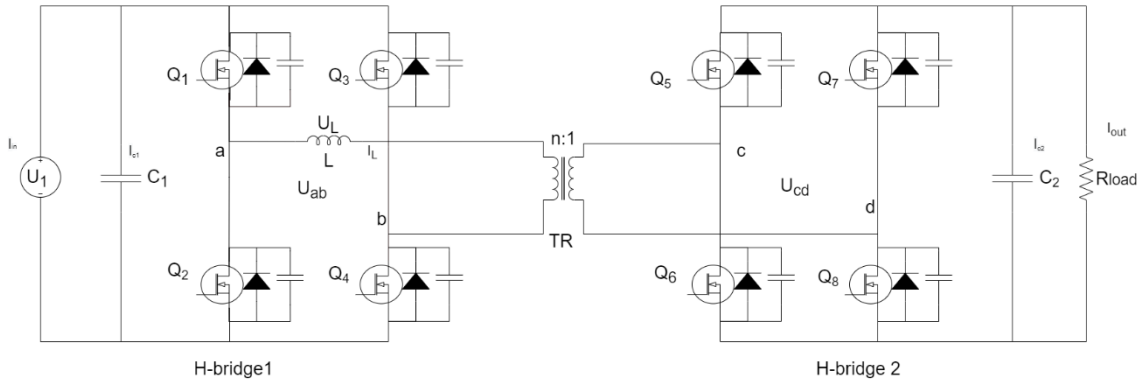

Figure 2 DAB Converter Circuit

Each bridge is composed by two legs, each consisting of two MOSFETS. The Q_1 and Q_4 switches receive the same gate signal, and Q_2 and Q_3 will receive complementary gate signal. This applies for the Secondary Bridge as well, but these switches will receive a phase shifted gate signal due to the Phase Shift Modulation Scheme applied in this converter. This phase shift will allow for the power transfer. This transfer of power is made possible due to the phase shift between U_{ab} and U_{cd} which generates a voltage over the leakage inductance of the HF Transformer where this leakage inductor of the transformer acts as an energy storage element[8]. The phase shift between these voltages will be equal to the phase shift injected to the switching signal of the secondary bridge switches.

Figure 3 presents the gate signal and the generated voltages on the terminals together with the varying inductor current. This plot depicts also the working principle of the SPS modulation scheme where the phase shift between the switching signals results in the output voltage not being zero. Form this plot it can be predicted that for a higher phase shift angle, higher output voltage would be generated resulting in higher transferred power. This relation is studied in [8], where for D=0.5 the maximum transferred power is obtained and for D=0 no power transfer is obtained.

The operation of the DAB converter is closely dependent on its parameters therefore, the DAB converter parameters are to be designed. The selection of the switching devices is also required for this thesis since a loss DAB model is to be used.

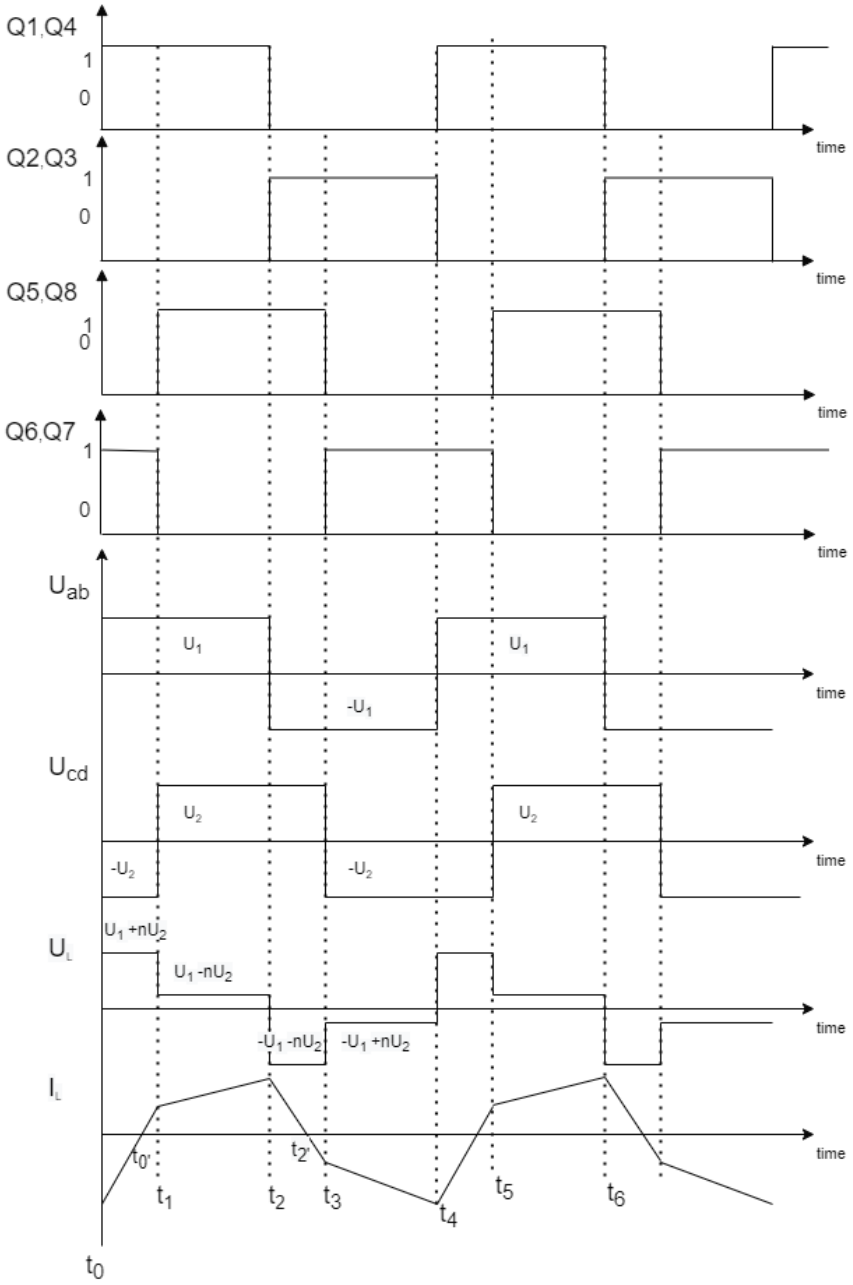

Figure 3 Single Phase Shift Modulation Scheme

2.3 Design of DAB Parameters

The parameters of a DAB converter have to be designed according to the operation of the converter for a maximum transferred power. This will allow for the performance that is expected from this converter.

The transformer turn ratio is considered 1 and all the switches operate at a fixed Duty Cycle 0.5 with a constant switching frequency.

Considering that the maximum transferred power for this converter in this thesis is 25kW, the parameters of the DAB Converters are designed accordingly. By assuming a passive load and for the given rated power of 25kW and output voltage of 700V, the load resistance is obtained:

$$R_l = \frac{U_2^2}{P_l} = \frac{700^2 V}{25kW} = 19.6\Omega \qquad \textbf{2-2}$$

Since Single-Phase Shift Modulation Scheme is applied to the DAB converter, accordingly the transferred power equation is obtained from the following equation:

$$P = \frac{nU_1U_2}{2\pi f_{sw}L_l}\varphi\left(1-\frac{\varphi}{\pi}\right) = \frac{nU_1U_2}{2f_{sw}L_l}D(1-D) \qquad \textbf{2-3}$$

where for different values of phase shift angle and output voltage, corresponding transferred power value can be obtained. From the same equation the leakage inductance value can be obtained:

$$L_l = \frac{n*U_1U_2}{8f_{sw}P_l} = 24.5\mu H \qquad \textbf{2-4}$$

for a switching frequency of 100kHz and a constant input voltage and an output voltage of 700V which corresponds to maximum power transfer. These values are considered for calculating the value of the leakage inductance because the converter has to be designed for the maximum operating conditions which corresponds to the DAB converter operating at D=0.5.

In the further analysis that will be conducted on this converter it should be noted that the output voltage will vary with the change of the phase shift value where other parameters will be kept constant. The output voltage is obtained using:

$$U_2 = \sqrt{PR_l} \qquad \textbf{2-5}$$

These steps provide the required data for the DAB converter design which are presented in the table below where the capacitor value is chosen to obtain small ripples on the output voltage.

DAB Specification							
P(kW)	**U_1(V)**	**U_2(V)**	**n**	**L_l(µH)**	**C_{out}(µF)**	**R_{load}(Ω)**	**f_s(kHz)**
25	700	700	1	24.5	100	19.6	100

Table 1 DAB Parameters

2.4 Selection of the Switching Devices

The DAB converter is composed of 8 switching devices which can be IGBTs, MOSFETs or other controllable power devices. These devices are usually Silicon (S) or Silicon Carbide (SiC) material based where throughout the years, both these two material technologies have developed.

SiC power devices were mostly known for their material properties that make it possible to design the junction with higher breakdown voltage and moreover they offer better conductivity and higher maximum temperature which also allows design of high temperature electronic devices [11].

These material properties have always pushed the research towards the application of these power devices, but its counterpart, Silicon was well established and did not have the complicated manufacturing process of substrates as in the case of SiC. It also had its own issues such as the defect of micropipes which were overcome by the limiting the micropipes and increasing of the diameter [11].

Many SiC material-based switches were introduced throughout the years but in 2010 CREE introduced the first commercially available SiC MOSFETs. Yet the SiC based transistors were firstly built back in 1980 [11]. This switch had its disadvantages such as the stability of oxide layer, but the fast improvement in performance and increased number of manufacturers are among the merits. The difference in driver supply voltage and the threshold voltage separated the SiC MOSFETs from Si transistors.

Silicon has limitations such as low bandgap energy and thermal conductivity but most importantly, limitation in switching frequency. The SiC material allows for high switching frequency which is also the main advantage of this material property. For reasons such as reducing the size of the DC-DC converter, the increase of the switching frequency is required which would also result in a short switching time. This led to SiC based power device being the most preferred type for the DAB converter application used in this project [11].

There are different kinds of power devices based on SiC material where the most prominent one is the SiC MOSFET. This due to its advantages such as small area and capacitance due to high doping and current densities[11].

These SiC MOSFETs allow for improvement in efficiency of fast switching power converters. A lower on state resistance is also among the requirements for the power converters design which this SiC based switches does provide.

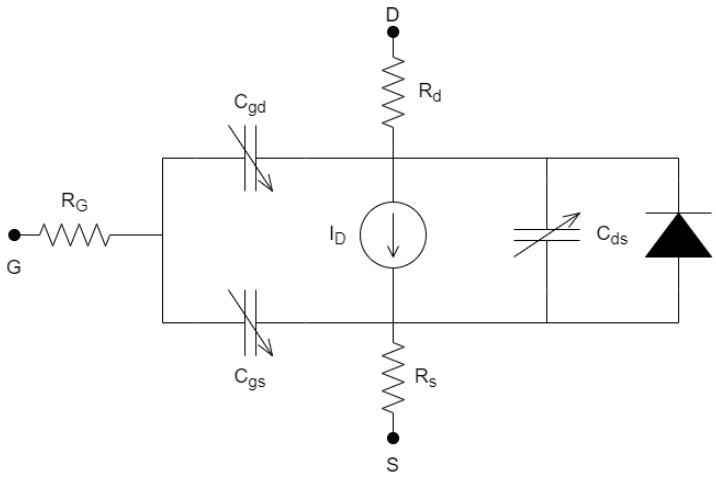

Figure 4 MOSFET Circuit [11]**.**

The 1.2kV SiC MOSFET is the most prominent and available type of power device since 6.5,10 and 15 kV MOSFETs are not available yet. The 1.7kV MOSFETs are commercially available but still need some improvement on their commutation characteristic and their 3.3kV counterparts still suffers from some issues [12].

The choice of the MOSFET to be used in the DAB Model of this thesis is done considering the current rating. Since the current will vary with a varying phase shift, the RMS current flowing through the switches for maximum power transfer, D=0.5, is considered. This value is obtained as followed:

$$\boldsymbol{i_{Lrms} = \frac{nU_2T_s\sqrt{-3(8D^3k-12D^2k-k^2+2k-1)}}{12L} = 58.3\ A} \qquad \textbf{2-6}$$

$$\boldsymbol{i_{Q1rms} = \frac{i_{Lrms}}{\sqrt{2}} = \frac{58.3}{\sqrt{2}} = 41.2\ A} \qquad \textbf{2-7}$$

This current value is considered for choosing the MOSFET since the switch can be destroyed for a high junction temperature which is contributed by this RMS current. The peak current should also be calculated in order to assure that the switch is going to be able to withstand this high current.

$$\boldsymbol{i_{peak} = \frac{nU_2}{4Lf_s}(2D + k - 1) = \frac{700}{4x24.5x10^{-5}100000} = 71.4\ A} \qquad \textbf{2-8}$$

The MOSFET chosen in accordance to the current and voltage rating is the C3M0016120K Silicon Carbide Power MOSFET [13]. The current rating of this MOSFET is chosen higher than the peak value of the current calculated due to the safety margin. The data provided from the datasheet of this switching device will be used throughout this thesis where the required plots provided by the datasheet are presented in Appendices.

3 Estimation of Losses

3.1 Introduction

An important aspect of the DAB converter are the losses. The low losses that this converter provides is one of the main attractions for this converter and therefore, an estimation of the losses is performed.

The estimation will be conducted both analytically and software based where the purpose of this is to compare the results of both these methods as well as to observe occurrences which are not evident in one of the methods. With the results obtained from this analysis, a better understanding of the operation of this converter will be obtained allowing for further analysis. The estimation of losses data allows for better selection of the switching frequency as well as the cooling module design.

In order to obtain the simulation results a DAB model has to be built in the simulation software and the designed parameters should be implemented together with the data of the switching device chosen in the previous chapter. The analytical approach will require to build a MATLAB script in order to perform the required calculations in an effective way.

A comparison of the two approaches chosen for estimating the losses will be conducted, where MATLAB plots will be built in order to visualize the differences between these methods.

One of the main advantages of this converter, as previously mentioned, is the ZVS which results in low total switching losses. The estimation of losses will identify the phase shift regions where this property is evident.

3.2 Theory on the Losses

In the power flow analysis conducted in [8] , a Lossless Model was considered where the transferred power results from the simulation would match with the analytical results. This allowed for a better understanding of the phase shift modulation scheme where a maximum power flow was obtained for D=0.5. The DAB model used in this part of the study is a Loss DAB model where the inductor and transformer losses are ignored for simplicity and with the aim on focusing only on the losses generated from the power devices.

The losses across a power device are composed of two loss mechanisms, static and dynamic losses where the static losses are the conduction and cut off losses where since the leakage current of the SiC power device in the blocking state is negligible, only the conduction losses, are considered. Whereas the dynamic losses are composed of the turn on and off losses known as the switching losses [7].

The losses that occur during the on state of the power device are known as the conduction losses whereas the losses which occur during and due to the transitioning process of the

power devices state from on-off and vice-versa during which the device is exposed to high voltage and high current, are known as the switching losses.

Two different scenarios are considered for this thesis, one is by considering the dead time to be zero, when only the MOSFETs will conduct, and one where the dead time is considered where the body diodes will conduct during this dead time. For the analytical calculation, the diode conduction losses are considered without effecting the conduction losses of the MOSFET. This will not be true for the simulation-based calculations where the conduction of the diode will have an effect on the MOSFET conduction time.

For this type of approach, input from the datasheet is used for a higher accuracy of the methodology.

3.3 Analytical Approach

3.3.1 Conduction Losses

For calculating the conduction losses, the on state losses, both the losses caused by Drain-Source On State Resistance $R_{DS(on)}$,and the losses that occur across the body diode are to be considered. The conduction losses across the MOSFET are calculated by multiplying the square of the RMS current across this switch with $R_{DS(on)}$ obtained from the datasheet. The value of this resistance varies with the change of the junction temperature of the MOSFET and for accuracy purposes, the junction temperature for the MOSFET is assumed to be higher than the ambient temperature. Thereafter from the following plot, the corresponding $R_{DS(on)}$ is found.

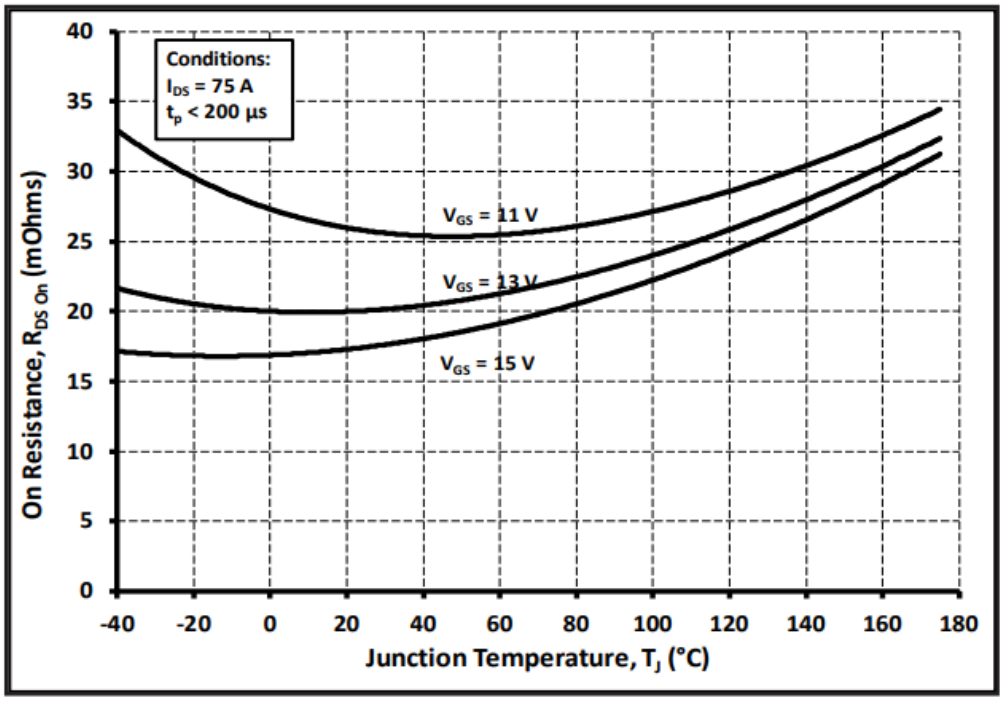

Figure 5 Drain-Source On Resistance Value for Varying Junction Temperature

Other parameters required to define the conduction losses are the current that flows through the switches. In order to define the RMS value of the current across the power device, the rms and peak value of the inductor current should be calculated where the RMS inductor current is obtained from the following relation:

$$i_{Lrms} = \sqrt{\frac{1}{T_s}\int_{t_0}^{t_0+T_s} i_L^2(t)dt} = \sqrt{\frac{2}{T_s}\int_{t_0}^{t_0+\frac{T_s}{2}} i_L^2(t)dt} = \frac{nU_2T_s\sqrt{-3(8D^3k - 12D^2k - k^2 + 2k - 1)}}{12L} \quad \textbf{3-1}$$

By obtaining the RMS inductor current, the RMS of the current that flows through the switches, the MOSFETs, can easily be obtained. This current is defined by:

$$i_{Q1rms} = \sqrt{\frac{1}{T_s}\int_{t_0}^{t_0+T_s} i_{Q1}^2(t)dt} = \sqrt{\frac{1}{T_s}\int_{t_0}^{t_0+\frac{T_s}{2}} i_{Q1}^2(t)dt} \quad \textbf{3-2}$$

where since $i_{Q1} = i_L$ during $0 \le t \le \frac{T_S}{2}$, the final equation for the RMS value of the current that flows through one switch on the primary H-bridge is:

$$i_{Q1rms} = \frac{i_{Lrms}}{\sqrt{2}} \quad \textbf{3-3}$$

All other switches in the primary side will share the same RMS current whereas for the secondary side switches, the RMS current will be dependent on the transformer turn ratio:

$$i_{Q5rms} = \frac{ni_{Lrms}}{\sqrt{2}} \quad \textbf{3-4}$$

since, as previously mentioned, the transformer winding ratio of this DAB converter is considered n=1, then all the switches, in primary and secondary side of the converter will share the same RMS current.

The SiC MOSFETs enables reverse current flow through the MOSFETs and not through the body diode. This minimizes the conduction power losses. The body diode only conducts the reverse current during the dead times and then, since the channel of the MOSFET is open, the current flows through the MOSFET, which also exhibits lower on-state voltage drop compared to the diodes, and thus lower conduction losses.

The diodes do not share the same RMS current as the MOSFETs, but this current that flows through them should be defined as well in order to find the losses across the diode, when the diodes conduct. This value corresponds to the inductor current during t_2 time value, for the primary H-bridge, which is also the peak inductor current:

$$i_L(t_2) = \frac{nU_1}{4Lf_s}(2D + k - 1) = i_{Lpeak} \quad \textbf{3-5}$$

The conduction losses over a switching period of the switching device are calculated by the following equation [14]:

$$P_{Q,cond} = \frac{1}{T_{sw}}\int_0^{T_{sw}} U_Q(t)I_Q(t)dt = U_{Q0}I_{Q,avg} + R_{Q1}I_{Q,rms}^2 \quad \textbf{3-6}$$

Where significant contribution to the conduction losses is provided from $R_{Q1}I_{Q,rms}^2$ and therefore, $U_{Q0}I_{Q,avg}$ is neglected in further calculations.

3.3.1.1 Results

MOSFET Losses

By using the generated equations, the calculations of the currents across the MOSFETs and body diodes are presented for a phase shift D=0.5.

$$i_{Lrms} = \frac{nU_2T_s\sqrt{-3(8D^3k - 12D^2k - k^2 + 2k - 1)}}{12L} = 58.3\ A \quad \textbf{3-7}$$

$$i_{Q1rms} = \frac{i_{Lrms}}{\sqrt{2}} = 41.2\ A \quad \textbf{3-8}$$

$$i_L(t_2) = \frac{nU_2}{4Lf_s}(2D + k - 1) = 71.4\ A \quad \textbf{3-9}$$

where the voltage convention ratio k, is obtained from the following relation:

$$k = \frac{U_1}{nU_2} = 1 \quad \textbf{3-10}$$

As previously mention, $R_{DS(on)}$ is found with the help of the datasheet where for the corresponding junction temperature of 45°, $R_{DSon} = 18.5m\Omega$. This junction temperature is chosen by assuming that the junction temperature will be higher than the reference ambient temperature. The reasoning behind this choice is further explained in 3.3.3. All the parameters required to calculate the conduction losses across the MOSFETs are found and the losses can be obtained as followed:

$$R_{Q1} = R_{DSon} = 18.5m\Omega \quad \textbf{3-11}$$

$$P_{cond,prim} = 4R_{Q1}I_{Q1rms}^2 = 125.85W \quad \textbf{3-12}$$

$$P_{cond,second} = 4R_{Q1}I_{Q1rms}^2 = 125.85W \quad \textbf{3-13}$$

In this approach the primary and secondary conduction losses are equal since all the switches share the same current and the junction temperature of the switches is also assumed to be constant for all the switches, therefore all the switches have the same R_{DSon} value.

The losses for phase shift values $0 \leq D \leq 0.5$ values are presented in Table 2 with corresponding voltages and current values. From this table, the increase of the losses in terms of the RMS current and phase shift value is noted. The results obtained from this approach will be further discussed in 3.3.4**.**

Phase Shift D	$P_{cond,prim\ MOSFET}$ **(W)**	$P_{cond,second\ MOSFET}$ **(W)**	$P_{cond,\ Diode}$ **(W)**	$i_L(t_1)$ **(A)**	i_{Lpeak} **(A)**	i_{Lrms} **(A)**	i_{Q1rms} **(A)**	$U_{F,prim}$ **(V)**	$U_{F,second}$ **(V)**
0.1	28.3	28.3	16.7	-31.4	50.9	27.7	19.6	3.75	3.2
0.2	24.9	24.9	8.6	2.8	44	25.9	18.3	3.4	1.1
0.3	47.8	47.3	15.8	31.4	47.4	35.7	25.3	3.7	3.2
0.4	85.2	85.2	24.9	54	57.7	47.9	33.9	3.9	3.8
0.5	125.8	125.8	34.08	71.4	71.4	58.3	41.2	4	4

Table 2 Conduction Losses of the DAB Converter, Analytical Results

Diode Losses

The conduction losses across the diode correspond to the losses during the dead time. Before the switching on of the MOSFET, a deadtime is present. This dead time happens due to the device properties. To avoid conduction of both the switches in a leg simultaneously to prevent short circuit of the input supply, and during this time the diode will conduct for a short period of the total dead time.

The diode conduction time during dead time, for the primary H-bridge, can be calculated by firstly calculating the capacitor charging time t_A which is obtained by [12]:

$$t_A = 2\frac{U_1 C_2}{I_{L(t_1)}} = 2\frac{700x230x10^{-12}}{71.4286} = 4.5x10^{-9}s \quad \textbf{3-14}$$

where C_2 is the parasitic capacitor of the MOSFET whose value is obtained by the datasheet and $I_{L(t_1)}$ is the inductor current at t_1 time instance.

The dead time value is obtained from the datasheet of the switching device. From:

$$t_{d(off)} + t_{fall} = 78ns \quad \textbf{3-15}$$

the dead time is obtained which due to safety margin, the total dead time will be considered $150ns$. Finally, the diode conduction time is:

$$t_B = dead\ time - t_A = 150 - 4.5 = 145.49\ ns \quad \textbf{3-16}$$

It is evident that the time which the diode conducts for during the dead time is around 98% of the total dead time which shows that the conduction losses across the diode have to be considered. Comparing this dead time with the resonance time it is noted that the diode conduction time is way longer but since the focus of this thesis is not on the length of this dead time rather on its effect, the aforementioned value will be considered throughout this project ignoring the difference it has with the resonance time due to the assumptions made regarding the safety margin.

The 8 diodes will conduct once for one switching period and to calculate the losses caused by this conduction, the following equation is used where $U_{F,prim}$is the diode forward voltage at the I_{Lpeak} which is obtained from the datasheet for $U_{GS} = 0$ for primary switches. For the secondary switches $I_L(t_1)$ is used to obtain $U_{F,second}$ for $U_{GS} = 0$. The junction temperature is considered $T_J = 25°C$ since the datasheet provides a $-40°C$ and $175°C$ junction temperature body diode characteristic where in an analytical approach, without actually designing the heat sink, obtaining an accurate junction temperature value is not possible. So $T_J = 25°C$ is used since it is closer to the desired case and the data for this junction temperature is provided by the MOSFETs datasheet..

For $I_{L\,peak} = 71.4\,A$ which corresponds to peak reverse recovery current and $I_L(t_1) = 71.4\,A$ at $T_J = 25°C$.

$$U_{F,prim} = 4\,V \quad \textbf{3-17}$$

$$P_{cond,deadtime} = 8U_{F,prim}I_{p,lk}\frac{t(B)}{T_{sw}} = 34.08\ \mathrm{W} \quad \textbf{3-18}$$

This concludes the analytical approach of conduction losses calculation for a phase shift equal to D=0.5. The same approach will be performed for other phase shift values as well where these results are presented in Table 2.

3.3.2 Switching Losses

3.3.2.1 Results

Calculating the switches losses in an analytical approach is more complicated than the conduction losses since there is no direct accurate method to calculate these losses without any input from simulation results. Though, different methods have been presented in different papers on how to calculate these losses without using only simulation-based results such as in [6], [7].

An easier approach to the switching losses calculation would be by using the datasheet of the MOSFETs where from the plots provided by it, an approximate switching losses calculation can be performed. In Appendices , two voltage levels and their switching losses for varying drain to source current are presented, 600V and 800V. Since the DAB converter in this thesis has a 700V voltage input, an approximation of the two plots provided from the datasheet will be made. Figure 6 depicts the method used to extract the switching energy from the datasheet plots.

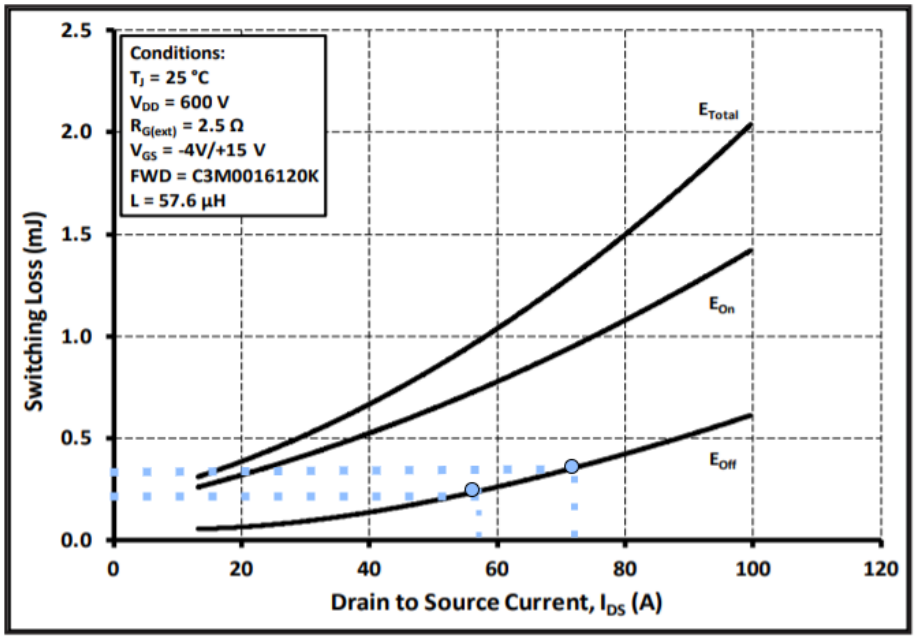

Figure 6 Switching Losses vs Drain to Source Current Plot

The turn off losses are the only one to be considered in the analytical approach of estimating the losses since ZVS is assumed to be provided for turn on of the switches in the current operating conditions of the DAB converter. ZVS property will be discussed further in Chapter 4 of this thesis.

One important note is that the data provided from the datasheet are not accurate since the data of the device is measured under ideal conditions which is not the same as the ones measured in practical conditions. This affects the accuracy of this approach.

From:

$$P_{sw} = E_{off} f_{sw} \quad \textbf{3-19}$$

where the switching frequency is 100kH, the switching losses are obtained, and these results are presented in Table 3 per switch.

Phase shift D	i_{Lpeak}**(A)**	$i_L(t_1)$ **(A)**	$E_{off,prim}(mJ)$	$E_{off,second}(mJ)$	$P_{sw,prim}(W)$	$P_{sw,second}(W)$
0.1	50.9	31.4	0.25	0.15	25	15
0.2	44	2.8	0.2	0.03	20	3
0.3	47.4	31.4	0.23	0.15	23	15
0.4	57.7	54	0.33	0.3	33	30
0.5	71.4	71.4	0.45	0.45	45	45

Table 3 Switching Losses, Analytical Results

3.3.3 Thermal Circuit

The junction temperature of the switching device should be kept within some limits, otherwise it will cause the device to smelt and so destroy the power device. The heat sink has the role of maintaining this junction temperature within the limits which is a part of the thermal circuit presented in Figure 7. The junction to case thermal resistance is obtained from the datasheet of the MOSFET whereas P_{tot} from the analytical calculation of the losses. The thermal resistance R_{thc-w} is chosen in an arbitrary way which is not an reasonable value since it is very low. But the focus of this study is not on the heat sink design, so it is assumed that the heat sink is an ideal heat sink with liquid cooling system, water cooling, and a very low thermal resistance. An important note is that the water temperature corresponds to the ambient temperature.

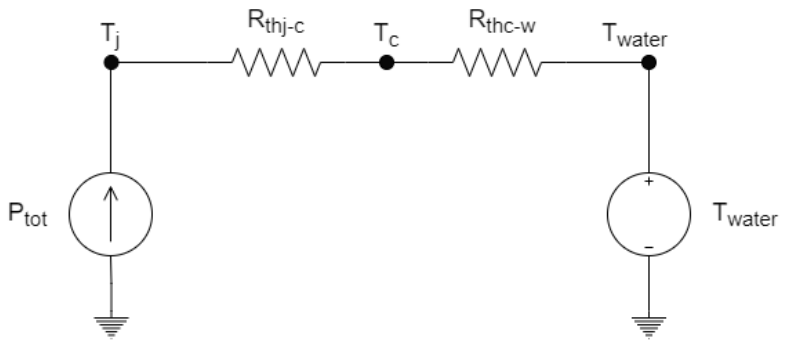

Figure 7 Thermal Circuit

By using the following equation:

$$T_j = T_{water} + P_{tot}R_{thc-w} + P_{tot}R_{thj-c} = 25.27°C \quad \textbf{3-20}$$

the junction temperature is obtained. This result is not realistically achievable since the thermal resistance cannot be so low as in this study but due to the focus being on the losses and not the heat sink for this thesis, these results are accepted.

3.3.4 Results and Discussions

Figure 8 presents the total losses, diode and MOSFET Losses for a varying phase shift angle. The losses increase with the increase of the transferred power. This happens since the current though the switches will increase for the increased phase shift angle and from the conduction losses equation it is evident that the losses are directly related to this current. From [8], the transferred power was noticed to be increasing for an increase in the phase shift angle, whereas the losses seem to follow this logic except for when D=0.2. The losses for this phase shift value are lower than for D=0.1. This happens due to the lower current flowing though the switches, because of lower power reflow for this region of phase shift values, resulting in lower losses, both conduction and switching losses. This phase shift value is therefore to be observed further in the simulation-based approach which provides more data regarding the operation of the converter at this particular phase shift angle.

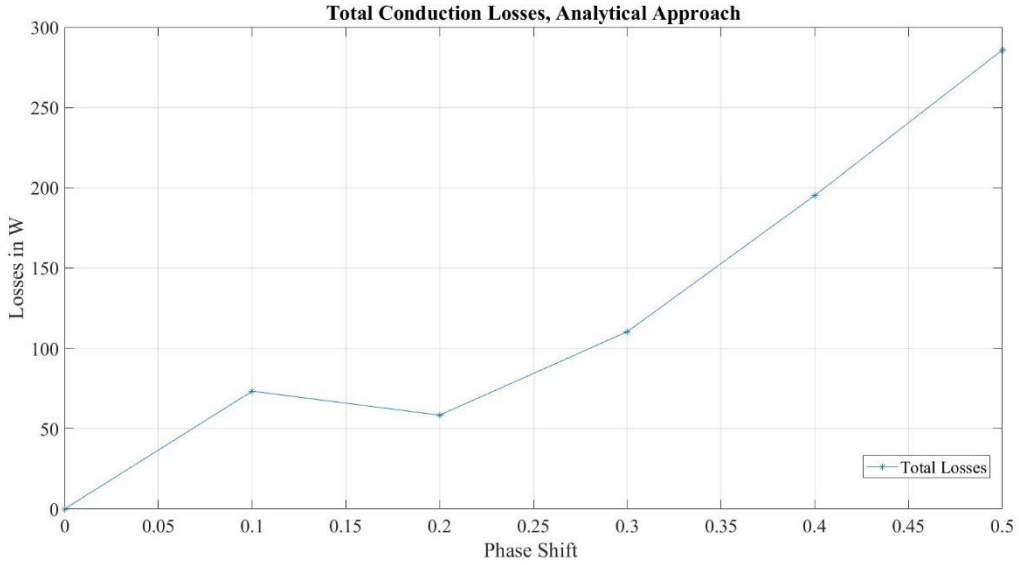

Figure 8 DAB Converter Total Conduction Losses, Analytical Approach

Compared to the total transferred power for each operating point, the total conduction losses are noted to be low, for a maximum power transfer D=0.5:

$$P_{totcond} = \underset{MOSFET}{P_{cond,prim}} + \underset{MOSFET}{P_{cond,second}} + \underset{Diode}{P_{cond}}$$
$$= 125.8 + 125.8 + 34.08 = 285.68W \quad \textbf{3-21}$$

which shows that the DAB converter is characterized by low conduction losses. Assumptions regarding the junction temperature were made in this approach which automatically points out that these results are not accurate in terms of real-life application. Though, these results are still acceptable since the R_{DSon}value does not vary significantly with the junction temperature. The total losses generated by this converter, conduction and switching losses are presented in the Table 4 where it can be seen that the total losses are also low compared to the total transferred power. The low switching losses for D=0.2 and the low RMS current flowing through the secondary H-bridge switches, contributes to low total losses for the converter operating at this phase shift range. The total losses are obtained by the following equation:

$$\boldsymbol{P_{totc} = P_{tot,cond} + P_{tot,sw}} \qquad \textbf{3-22}$$

Phase shift D	$P_{tot,cond}$(W)	P_{tot}(W)
0.1	81	232.8
0.2	70.4	150.4
0.3	120.6	262.4
0.4	203.7	479.3
0.5	296.6	645.7

Table 4 Total Losses, Analytical Approach

3.4 Simulation Approach

Using a simulation software would provide more accurate results since components and parameters that might be neglected in the analytical calculations, are considered which allows for closer results to the real practical results. This approach would allow for other useful observations which were not possible in the analytical approach.

Therefore, the previous task of calculating the losses, is conducted also by using a simulation software in order to achieve closer results to the practical one, which as a result would allow for a better study of this converter.

The simulation tool used for this thesis is PLECS and the reason why this simulation software is chosen is because it provides electrical thermal and mechanical aspects by its library. Scopes that visualize the data, simulation scrips which allow for change of the parameters and the built-in analysis tools which allows for steady state operation, are among the tools which assist in the design and analysis of power electronic systems provided by PLECS software.

All of these tools and other, will provide results which will later be compared with the analytical results. In order to conduct this study, the first step is setting up the system on PLECS window.

3.4.1 PLECS Model Setup

The procedure of setting up the systems starts by building the DAB converter model on the PLECS window where from the PLECS library, electrical components such as MOSFETs, capacitors, transformer inductor and voltage source are extracted. The setup of these components is made according to the DAB circuit, composed by two full bridges, and these components are connected by wires which PLECS will considered lossless, and their length has no effect on the results. Ammeters and Voltmeters are also setup on different points of the model at which the voltage and current are desired to be measured.

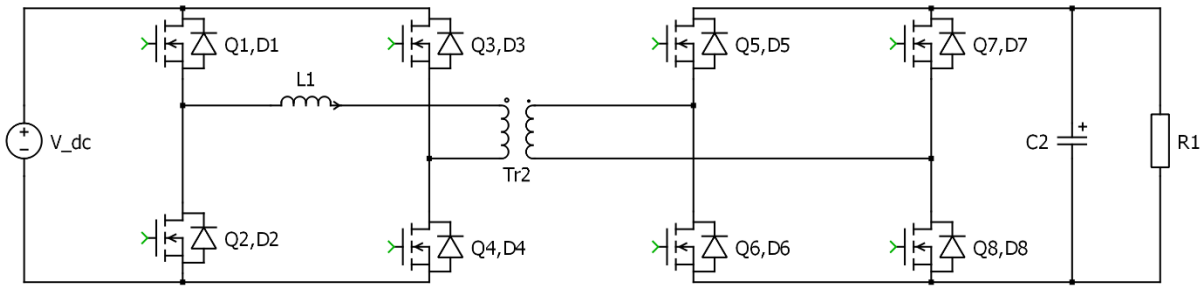

Figure 9 DAB Circuit PLECS Setup Model

By using the simulation script, the parameter values of each component are assigned to the according component where the values used are attained from Table 1. The initialization script is presented in Appendices .

The data for the switching components cannot be implemented using the simulation scrip and therefore, the datasheet of the MOSFET chosen previously has to be implemented in the simulation model. There are two methods to achieve this, either by implementing the data manually or by incorporating the datasheet of the MOSFET as a file in the Thermal Library. Both methods are acceptable but in order to achieve more accurate losses, which is what this thesis aims at, the second method is used. The same approach will be used for the body diodes data implementation.

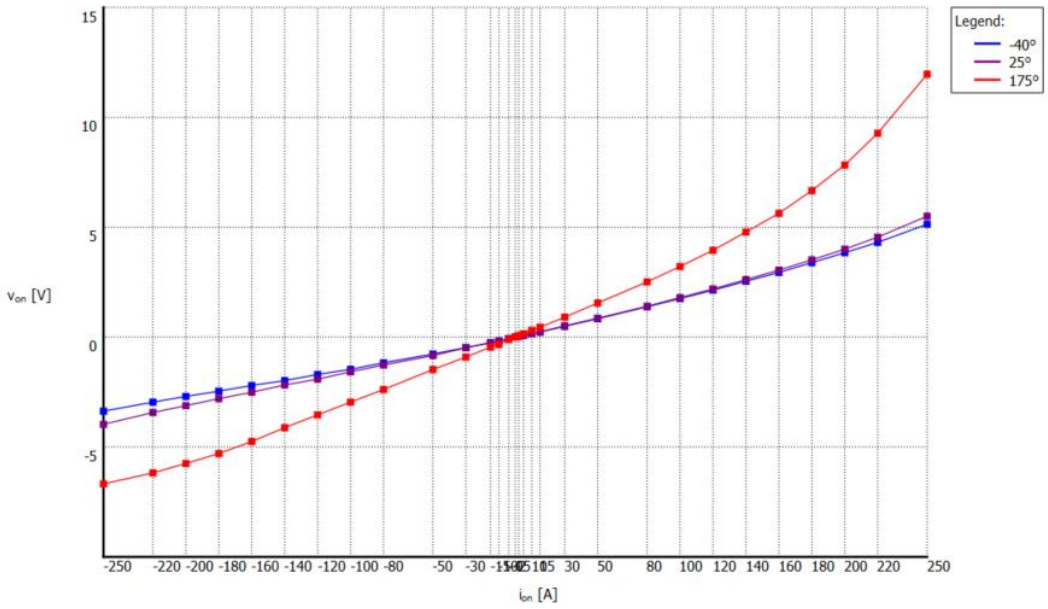

Figure 10 Conduction Losses Data, MOSFET

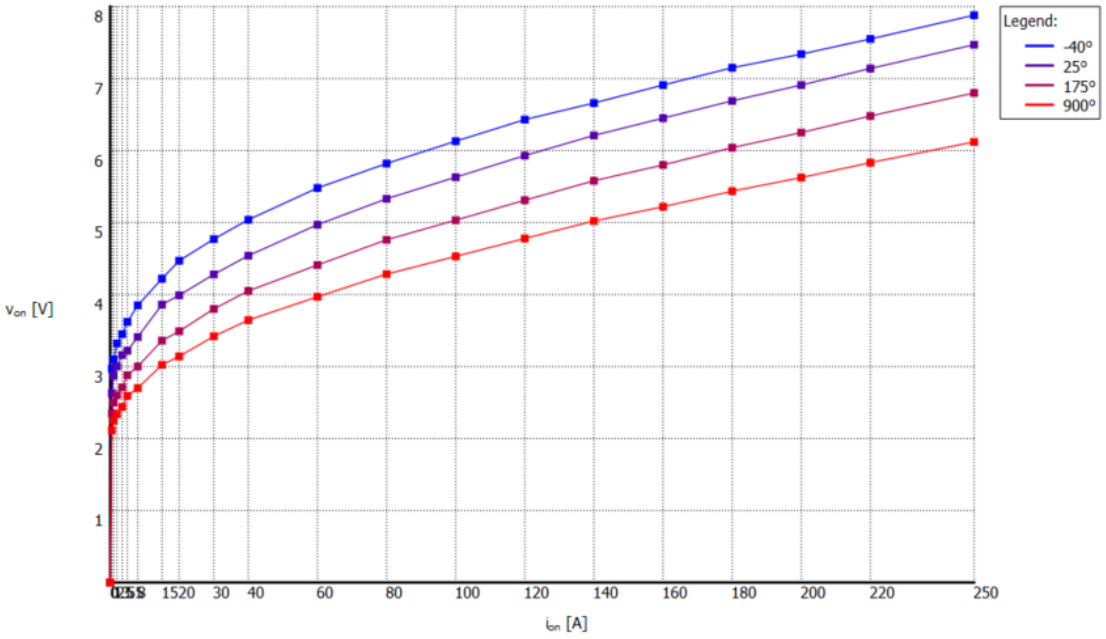

Figure 11 Conduction Losses Data, Body Diode

The Figure 10, Figure 12 and Figure 13 present the implemented data for estimating the conduction losses and turn-on and turn-off losses for the MOSFETs and Figure 11, the data for estimating the conduction losses for the body diode.

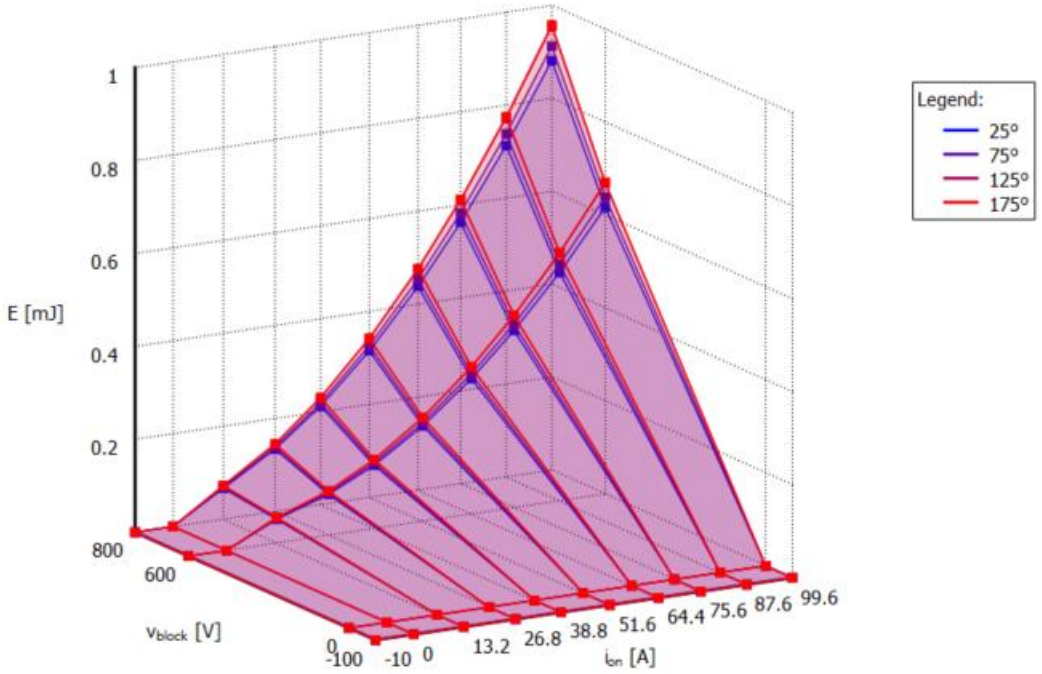

Figure 12 Turn-Off Losses.

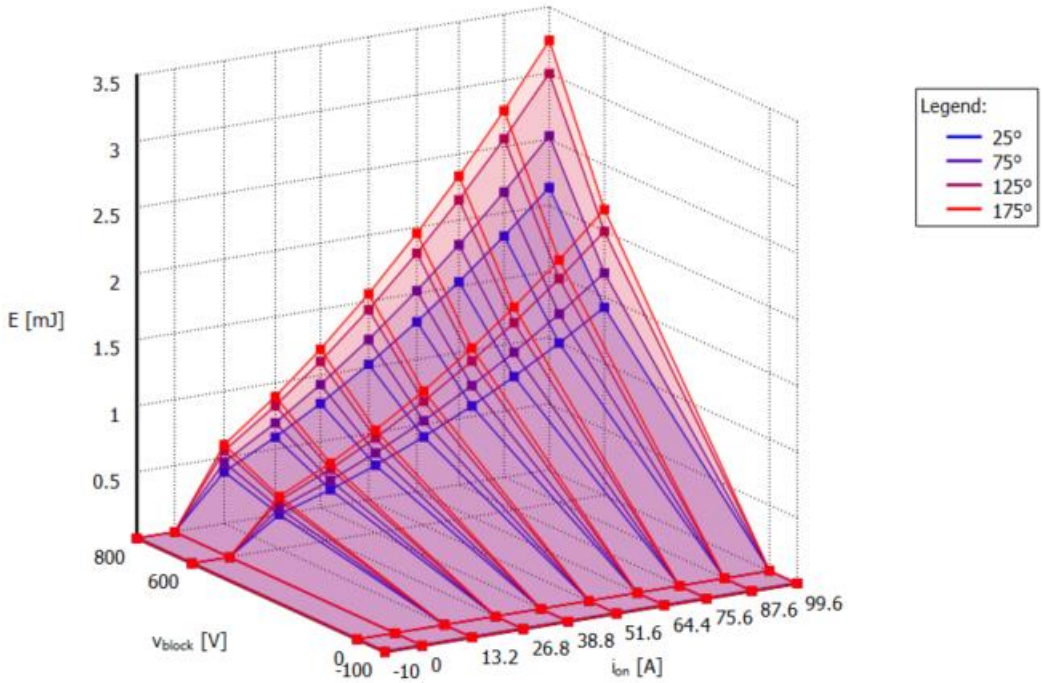

Figure 13 Turn-On Losses.

After assigning the MOSFET and the body diode with the corresponding Thermal Library, the conduction and switching losses can be estimated with the help of probes where the parameters selected are the conduction losses, switching losses and temperature. The losses of the MOSFET and body diode are estimated separately and therefore presented separately which are visualized by scopes. The results obtained from the scopes are difficult to read in this condition and therefor the Periodic Average Block is used in order to obtain the conduction losses and Periodic Impulse Average Block are used to obtain the switching losses which are later to be compared with the analytical results.

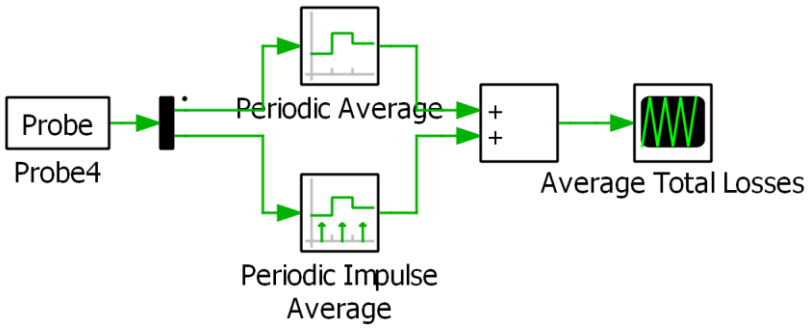

Figure 14 Averaging Blocks.

3.4.1.1 High Accuarcy Setup Approach

In order to obtain more accurate results, the effect of more components have to be considered. The way the system is setup at this point does not consider the heating of the switching device, which in practice would be a real issue. The MOSFET junction temperature would continuously rise causing the power device to melt and reach saturation. The temperature of the power devices has to be kept within the manufacturing limits and for that, different mechanisms are available.

The role of the heat sink is that of absorbing the thermal losses dissipated by the components covered by it. Therefore, a heat sink that will absorb this heat is required [15]. The heat conduction between the heat sink and ambient temperature, is modelled by thermal resistance and capacitors connected to the heat sink which needs to be designed for the worst case scenario [16]. The thermal circuit build Figure 15, consists of a thermal resistance $R_{th} = 0.001\frac{K}{W}$ where the capacitor is neglected for this approach, and an ambient temperature of $25°C$ which chosen as a reference.

For the heat sink design, the thermal capacitance is choses $0.01\frac{J}{K}$ and the initial temperature $25°C$. The thermal impedance, junction to case impedance, of the switches are provided by the datasheet of the MOSFET and are implemented automatically when the data of the switches were assigned to the switches, Appendices . The heat sinks chosen to be used for this DAB model will cover all 4 switches in the corresponding bridge. As it can be seen from Figure 17 two heat sinks are used for this study.

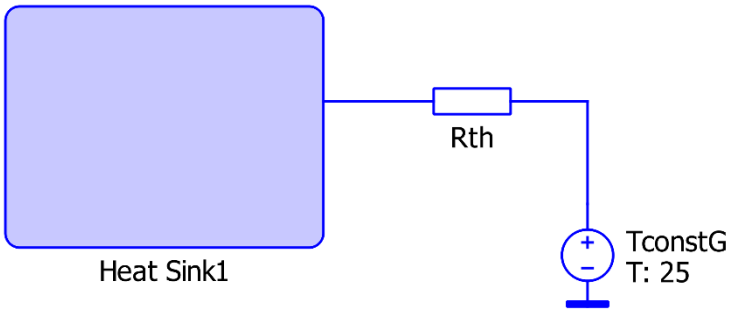

Figure 15 Thermal Circuit

Throughout the analysis a reference temperature, ambient temperature, has to be chosen where for this project a temperature of $T = 25°C$ is chosen in order to avoid two effects, the electric losses and additional influence on the total losses due to components with different temperatures [17]. The running time of the converter has to be considered as well in order to assure no heating of the converter, but PLECS will not consider this effect.

For more accurate results, series variable resistor components are connected to the MOSFETs which represents the Drain-Source On resistance R_{DSon}. The reasoning behind this is that the R_{DSon} varies with the junction temperature, therefore a temperature dependent R_{DSon} is connected in series with the MOSFET. This would allow for more accurate results. This is presented in Figure 16.

In order to test the system and check if the obtained results are accurate, throughout the whole study, the current and voltage of the inductor and the input and output voltages are observed. This concludes the setup of the DAB Model system setup where the working space together with the model used in this thesis is presented in Figure 17.

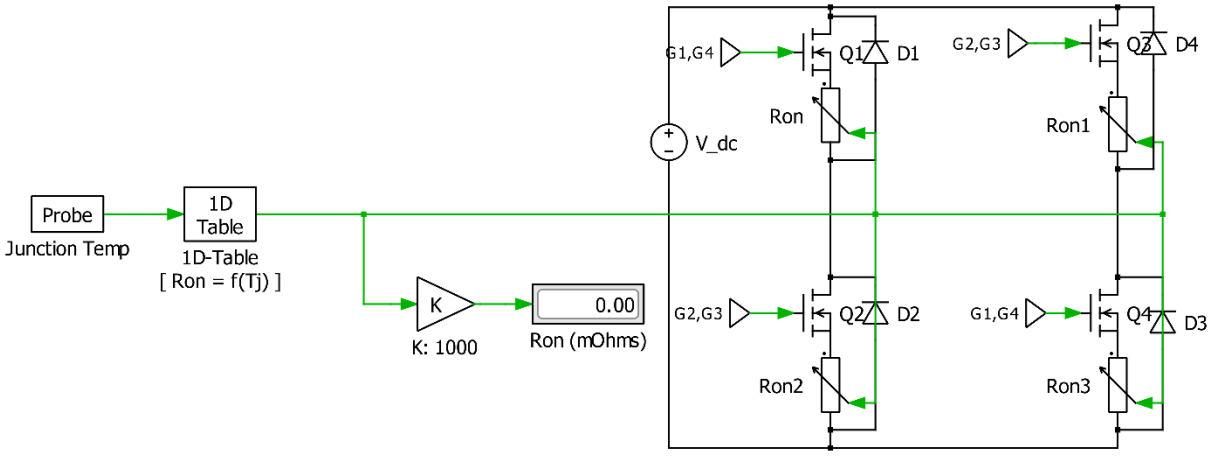

Figure 16 R_{DSon} Control Unit

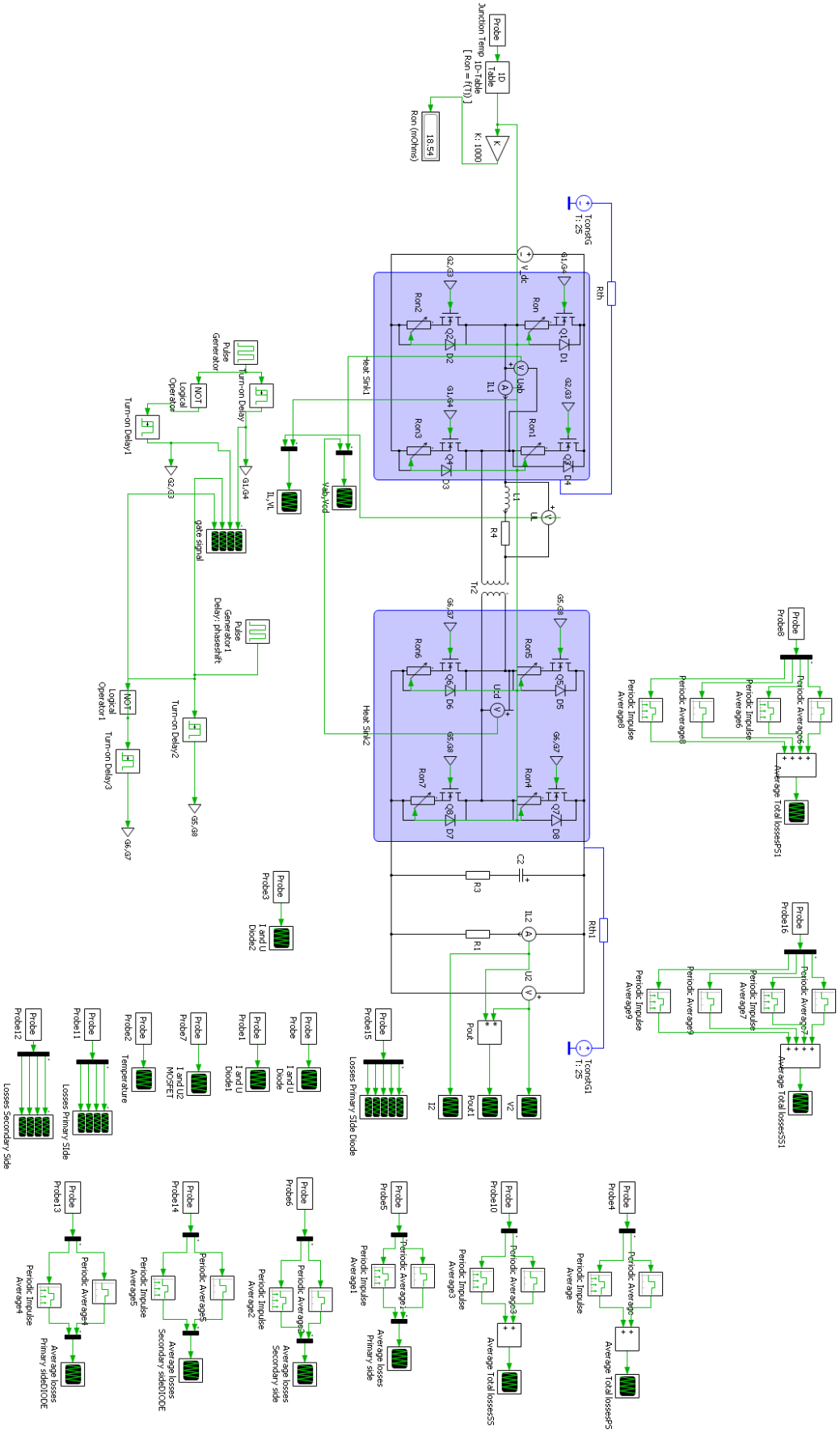

Figure 17 PLECS Setup

3.4.2 Simualtion Results and Discusssions

By running the simulation for a period of time, the plots in the corresponding scopes will provide the required data, during the steady state operation. With the help of the RMS, Max data command in these scopes, the values which are required are obtained.

The losses presented on the scopes are only the losses for one switch in the primary H-ridge and one for the secondary H-bridge, so in order to obtain the total losses of primary and secondary bidges, these losses have to be multiplied with 4, the number of switches in the corresponding bridge since all the switches of the corresponding bridge will share the same current and same varying R_{DSon}.

Two simulations are conducted, one considering the dead time and one not considering the dead time. These two simulations will provide slightly different result. For when the dead time is not considered, there are no diode losses and the conduction losses of the MOSFET are expected to be a bit higher compared to when the diode conducts. This is expected to happen since the MOSFET will conduct for a slightly longer time when the dead time is not present which results in higher conduction losses.

3.4.2.1 When the Dead Time is not Considered

In the tables below, Table 5 and Table 6, the results obtained from PLECS are presented for when the dead time is not considered together with the measured currents that flow though the switches and inductor currents are presented.

PLECS plots are also presented which are used as the primary source of observing the losses and their variation for different conditions. In Appendices plots that present the conduction and switching losses for a varying phase shift are available, and Figure 18 and Figure 19 show the total losses for a varying phase shift. These plots are generated by the scopes where the averaging blocks are used.

Phase shift D	$P_{cond,prim\ MOSFET}$ **(W)**	$P_{sw,prim}$ **(W)**	$P_{cond,second\ MOSFET}$ **(W)**	$P_{sw,second}$ **(W)**	$P_{tot,prim}$ **(W)**	$P_{tot,second}$ **(W)**
0.1	26.9	102.33	26.2	74.9	129.1	101.2
0.2	23.7	83.7	22.5	3.6	107.4	26.1
0.3	45.8	93.2	43.8	42.1	138.9	85.9
0.4	85	124.8	81.3	106.8	209.9	188.2
0.5	130.2	174.6	122.7	173.8	304.8	296.4

Table 5 DAB Losses when No Dead Time, Simulation Approach

i_{Lpeak} **(A)**	i_{Lrms} **(A)**	i_{Q1rms} **(A)**
50.6	27.5	20.6
43.8	25.9	18.3
47.3	35.7	28.4
57.5	47.9	33.9
71.3	58.2	41.1

Table 6 Corresponding Current Values

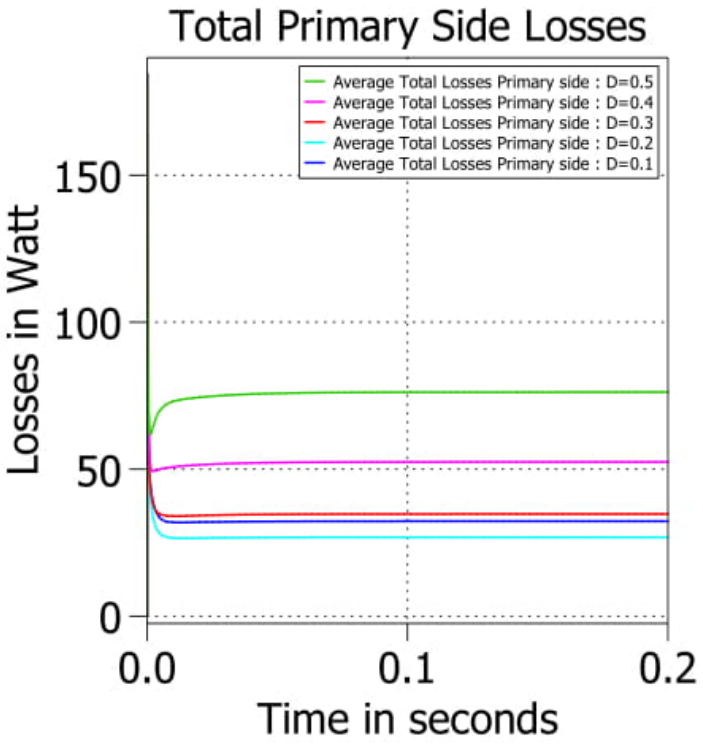

Figure 18 Total Losses Primary Bridge for Varying Phase Shift Value

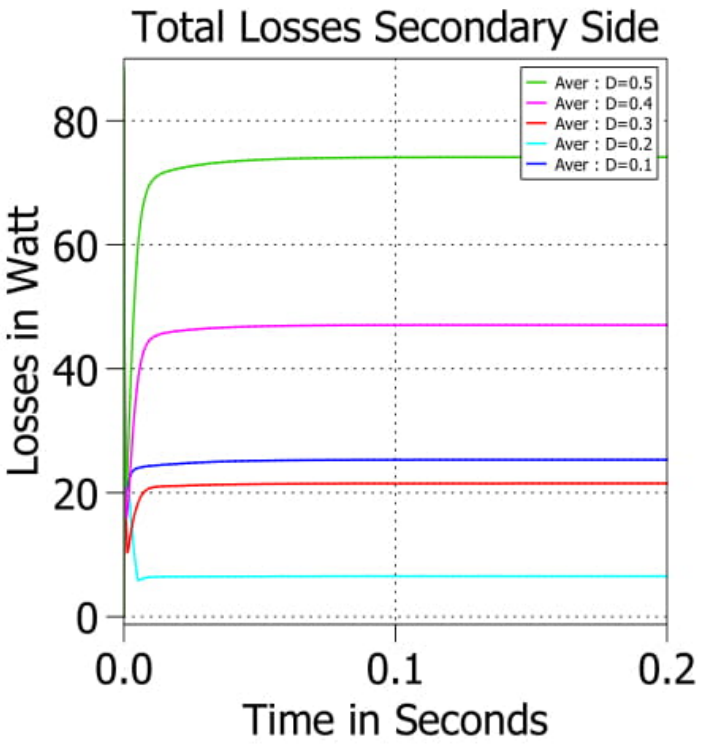

Figure 19 Total Losses Primary Bridge for Varying Phase Shift Value

In the analytical approach, the primary and secondary side conduction losses were equal since the current that flows though the switches on both sides were considered equal when the transformer winding ratio is 1. But in the simulation-based approach, as it can be seen from the results presented in the above table, Table 5, and the Figure 21, the primary and secondary losses are slightly different for D=0.5 and with lowering the phase shift value the bigger the difference between the losses from primary and secondary side are noted. This happens due to the fact that the voltage in the secondary is characterized by ripples whereas in the primary bridge, the input voltage is constant. The method PLECS uses to estimate the conduction losses is different from the analytical approach. When in the analytical approach the reference on obtaining the conduction losses was on the current flowing though the switches, in the simulation based it is on the voltage current relation presented in Figure 10 .This dependency allows for the simulation based approach to consider the effect that the output voltage has on the losses, and this output voltage directly affect the estimation of the secondary H-bridge losses. For this reason, a difference between the conduction losses in the secondary H-bridge compared to the primary bridge is noted. With the phase shift value decreasing, the lower the secondary side voltage will be compared to the primary side. Therefore, it is always expected that the losses are higher on the primary side of the converter for a positive unidirectional power flow where the input voltage is at its maximum.

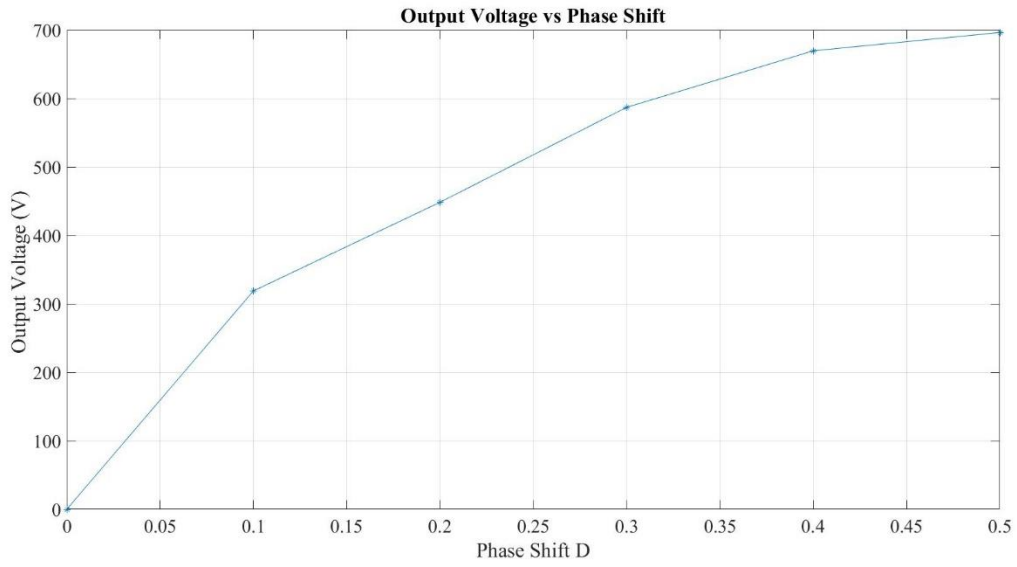

Figure 20 Output Voltage for Varying Phase Shift

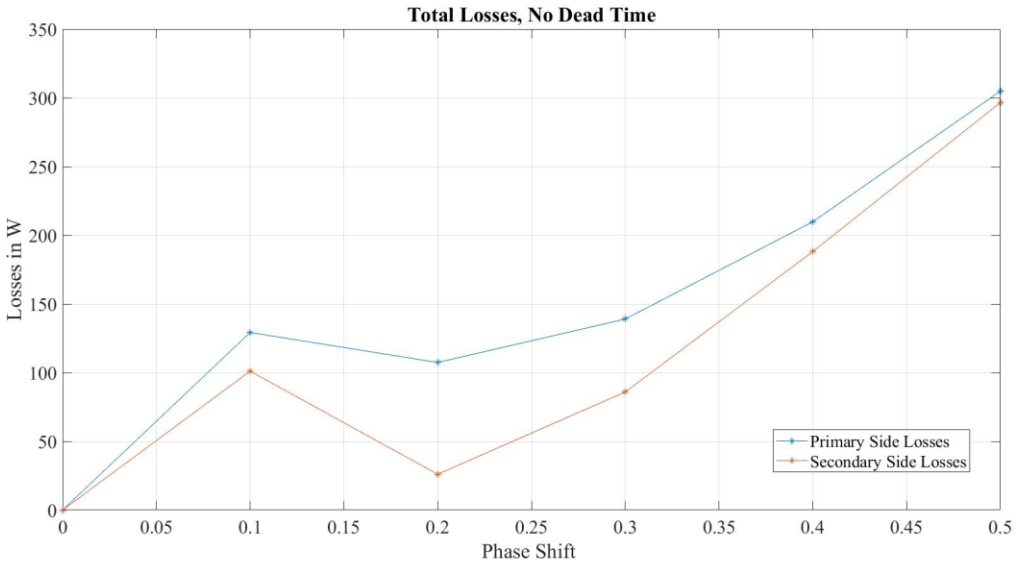

Figure 21 Total Losses for Varying Phase Shift, No Dead Time

The average total losses are highest for a maximum phase shift since the transferred power is higher and the output voltage is at its maximum. Therefore, it is expected that for lower phase shift values, lower losses to be obtained. This applies for all phase shift values except for a certain phase shift range where the inductor current value is lower than when the phase shift is smaller. A part of this range is the phase shift D=0.2 where clearly from the obtained results, the total average losses, conduction and switching losses, are the lowest among all the phase shift values presented in this study. The conduction losses are closely related to the RMS current that flows though the switches so just by observing the relation of the phase shift with this RMS current value it can be predicted that higher RMS current will lead to higher losses and that for the phase shift D=0.2, since the RMS current is the lowest, than lower losses will be obtained. This will occur both for when the dead time is considered and not. The relation between the phase shift and the RMS current flowing thought he switches is also presented in Figure 22 where the cases when the dead time is and is not present are depicted.

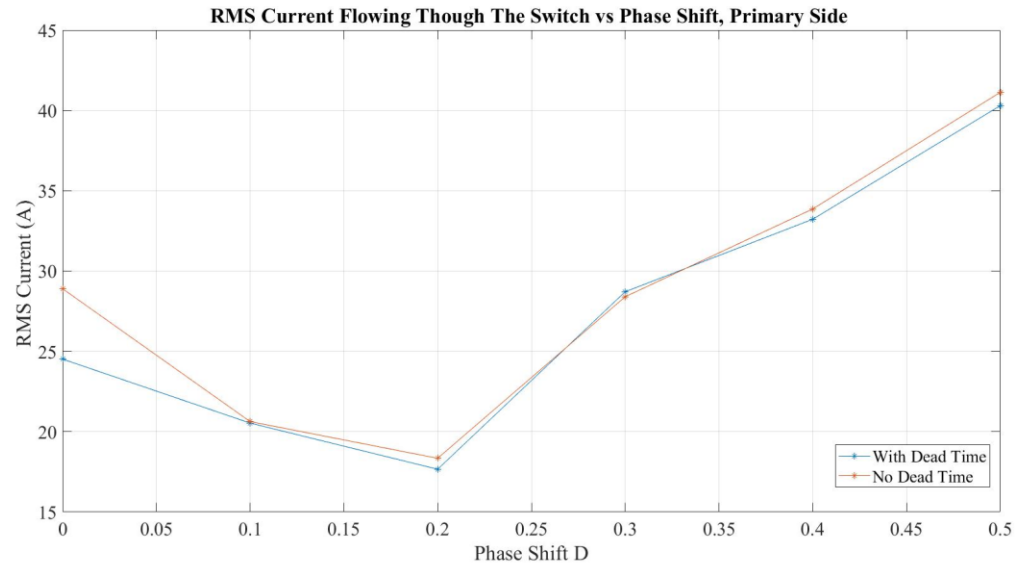

Figure 22 RMS Current Flowing Though the Switches for Varying Phase Shift

Previously, the difference between the losses in the primary and secondary bridges was noted where the reasoning behind this difference was the method PLECS uses to estimate the losses which refers on the output voltage. The difference between the results seems to be consistent except for the phase shift D=0.2. Drastic low switching losses in the secondary side are spotted for this phase shift angle which contribute to the low total losses for this phase shift value. These switching losses are extremely low due to the low switching current during the turn-off of the secondary H-bridge switches for this particular phase shift value. From Figure 23,Figure 22 lower currents flowing though the secondary bridge are evident for all the phase shift values presented but is particularly lower for D=0.2. This is also presented with the plots generated from PLECS, Figure 24, where it is evident that during turn-off of Q5, the current flowing through that switch is 3.12 A, a value which is very close to allowing the switch to realize ZCS. This triggered the idea of further researching this phenomenon in 3.4.3 where the boundary operation of the converter is observed in terms of realizing ZCS. The current flowing through the primary and secondary bridges for D=0.1 is also presented in Figure 25 which shows that the turn-off current is significant for both bridges which led to the switching losses during turn on of the switches. From these plots, the turn-on currents are noted to be zero which show the ZVS capability of the converter during turn-on of the switches, providing so zero turn on switching losses. More on this phenomenon will be explained in Chapter 4.

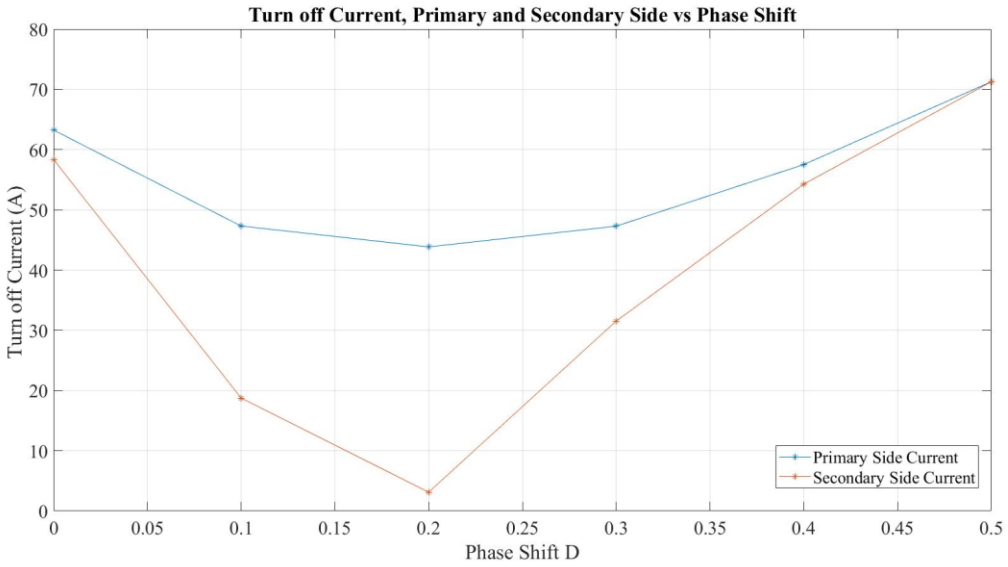

Figure 23 Turn off Current Primary and Secondary Side for a Varying Phase Shift

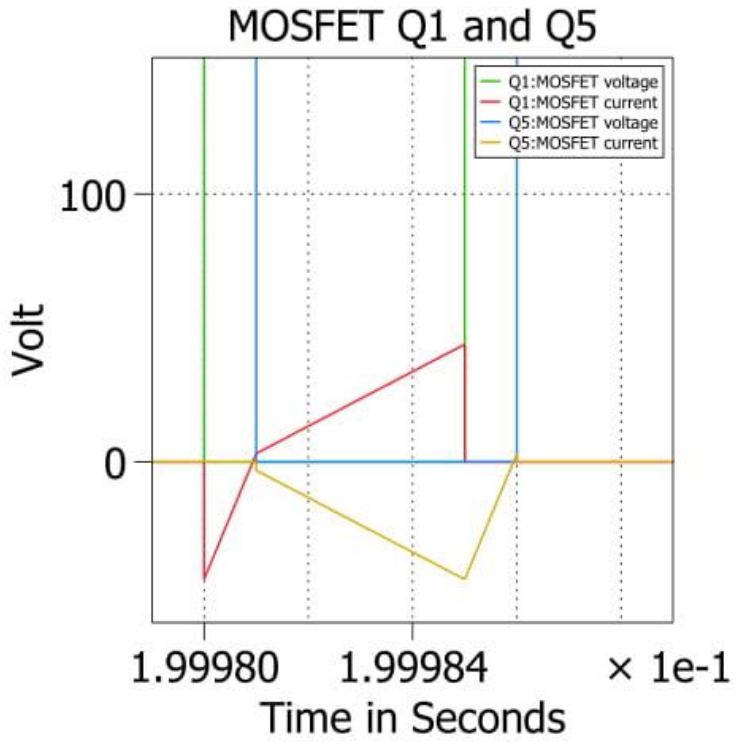

Figure 24 Currents Flowing Though Q1 and Q5 Switches for D=0.2

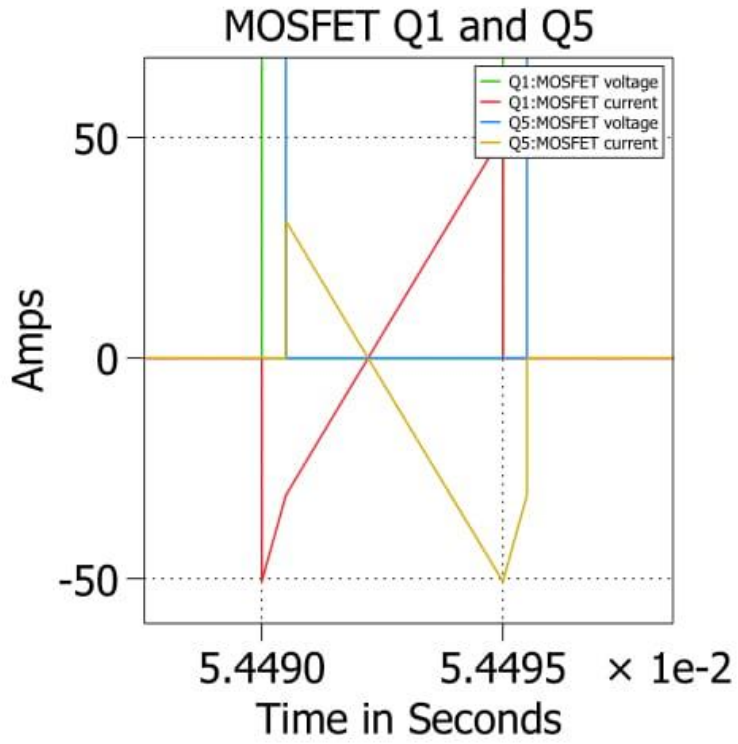

Figure 25 Currents Flowing Though Q1 and Q5 Switches for D=0.1

3.4.2.2 When the Dead Time is Considered

The losses results for when the dead time is considered, by injecting a delay time to the switching signal, are presented in Table 7, Table 8 and Table 9 alongside the measured currents that flow though the switch and inductor current.

The results obtained for different phase shift values are also presented by PLECS scopes Figure 26, Figure 27, where the difference between the losses for different phase shift values is evident.

For when the dead time is present, the body diode will conduct, thus generating losses, and therefore, results regarding the operation of this diode are depicted in this section.

Phase shift D	$P_{cond,prim\ MOSFET}$ **(W)**	$P_{sw,prim\ MOSFET}$ **(W)**	$P_{cond,second\ MOSFET}$ **(W)**	$P_{sw,second\ MOSFET}$ **(W)**	$P_{tot,prim}$ **(W)**	$P_{tot,second}$ **(W)**
0.1	20.8	93.6	21.7	71.2	114.4	92.9
0.2	21.9	84.2	22.5	3.6	106.1	26.2
0.3	43.8	93.6	42.8	42.3	137.4	85
0.4	81.9	125.3	78.1	107.3	207.2	185.4
0.5	125.1	175.1	116.9	174.2	300.3	291.2

Table 7 DAB Losses when the Dead Time is Present, Simulation Approach, MOSFET

i_{Lpeak} **(A)**	i_{Lrms} **(A)**	i_{Q1rms} **(A)**
47.3	25.5	20.5
43. 9	25.9	17.7
47.3	35.7	28.7
57.5	47.8	33.2
71.3	58.2	40.3

Table 8 Corresponding Current Values

Phase shift D	$P_{cond,diode,prim}$ **(W)**	$P_{cond,diode,second}$ **(W)**	$P_{sw,diode}$ **(W)**	$P_{tot,prim}$ **(W)**	$P_{tot,second}$ **(W)**
0.1	12.3	5.7	0	126.7	98.6
0.2	10.9	0.7	0	117.1	26.9
0.3	11.9	8.3	0	149.3	93.3
0.4	15.4	15.8	0	222.6	201.2
0.5	20.4	22.1	0	320.7	313.3

Table 9 DAB Losses when the Dead Time is Present, Simulation Approach, Diode.

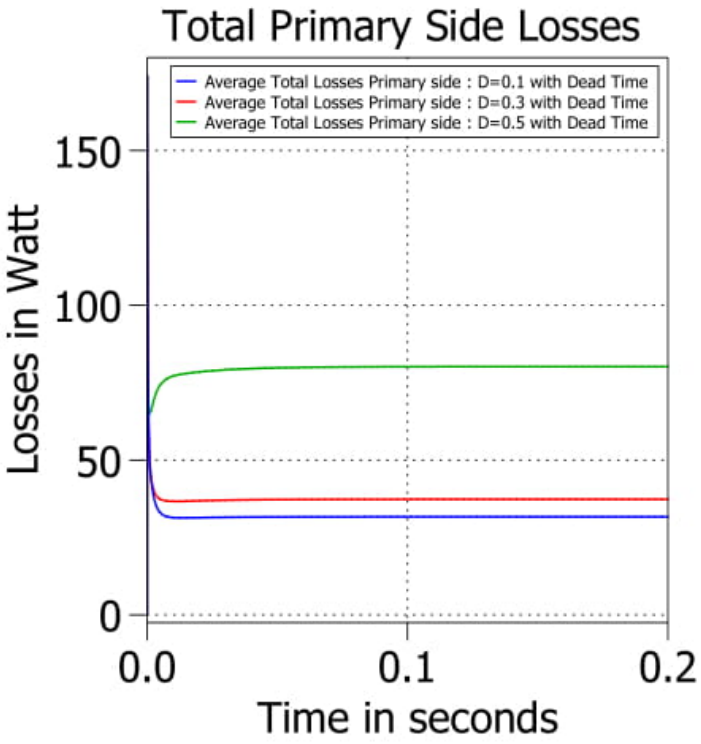

Figure 26 Total Losses for Varying Phase Shift, Primary Bridge

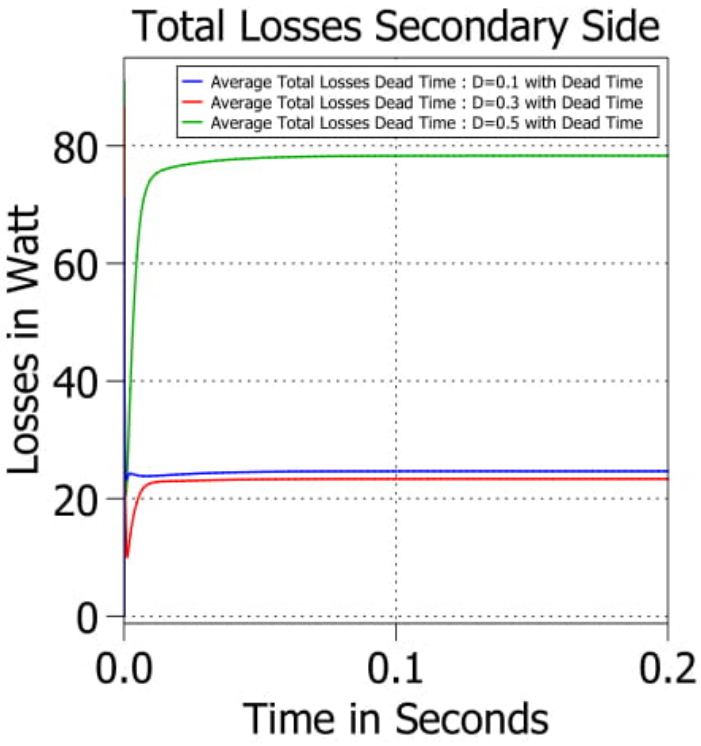

Figure 27 Total Losses for Varying Phase Shift, Secondary Bridge.

For this part of the study of the estimation of the losses, a dead time of 150 ns, which is a value found in section 3.3.1, is applied to all switches. This dead time will allow for the diode to conduct for a short period of time which will as a result cause diode losses. The losses considered as caused by the diode are only conduction losses since there is no data

for the switching losses provided by the body diode datasheet, leading to them being zero. Considering that the conduction losses are dependent on the peak value of the inductor current, then the current that flows though the diode, where its peak value corresponds to the peak value of the inductor current, is important to estimate these losses. This current is therefore is presented by the PLECS plot in Figure 28.

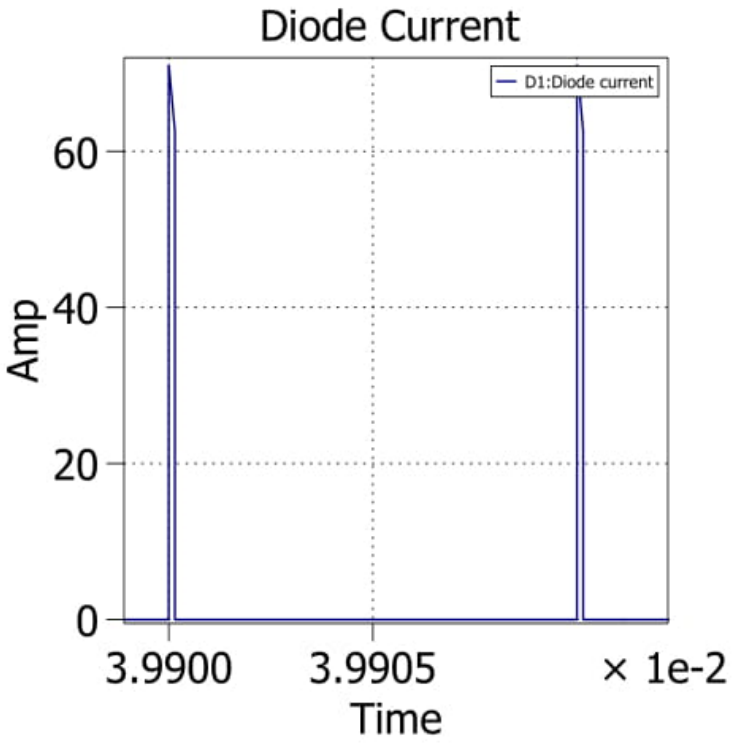

Figure 28 Diode Current for D=0.5.

In the Figure 29 , which depict the current that flows though Q1 and Q5 switches and the voltages across these switches, a voltage overshoot and dip is evident which is not present for when there is no dead time.

When the dead time is present, then the diode will conduct, and the diode voltage will cause this voltage overshoot and dip. From the results obtained, the diode losses have a difference between primary H-bridge and secondary H-bridge. This was also noted in the case for the MOSFET losses due to the approach PLECS uses to estimate these losses by using the voltage current plots presented in Figure 10. The same approach is used for estimating the diode losses Figure 11, thus resulting in the difference between the losses generated in the two bridges.

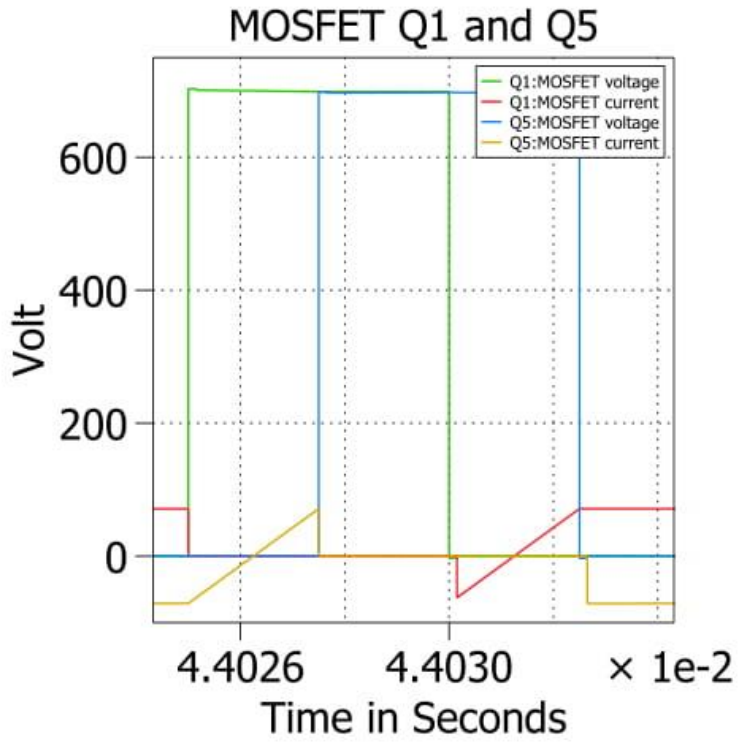

Figure 29 Currents Flowing Though Q1 and Q5 Switches for D=0.5

The diode conduction time will cause the MOSFETs to conduct for less. This will result in lower conduction losses for the MOSFETs which can also be seen from the results obtained presented in Figure 30 . The difference between the MOSFET losses for both the cases is not big but still worth mentioning is that in average, they are less for when the dead time is present.

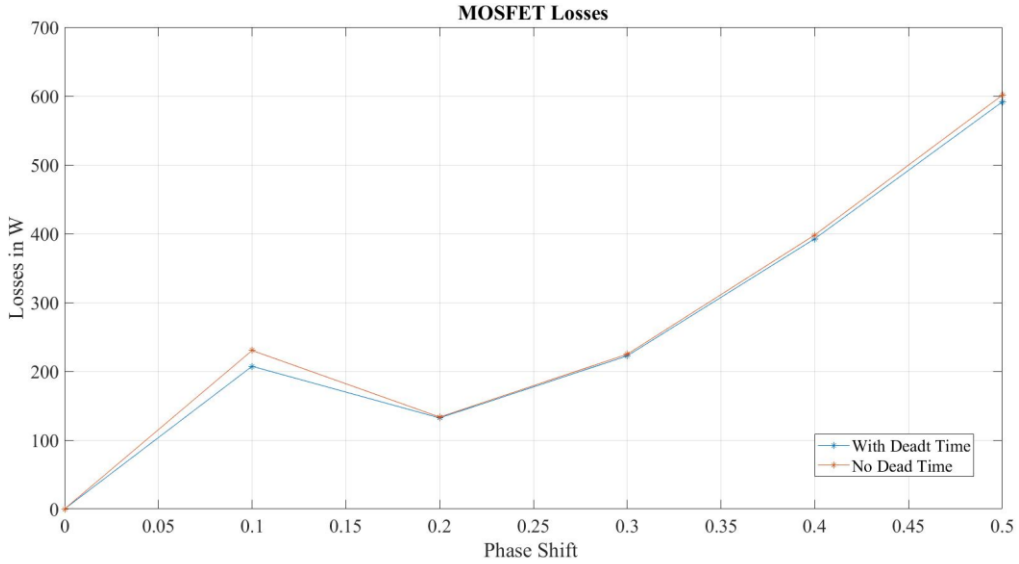

Figure 30 MOSFET Losses for when the Dead Time is Present and Not

This though does not prove that lower losses are generated for when the dead time is present since now the diode losses also have to be considered. The diode losses will cause the total losses to be higher than when the dead time was not present. This can be seen also in the Figure 31 where the total losses are higher compared with when the dead time was not considered. Though, this seems to be true for all phase shift values except for D=0.1 where the total losses are less, and this happens due to the lower inductor current that this phase shift provides when the dead time is considered.

A method to mitigate these losses for when the dead time is considered is by connecting antiparallel diodes to the switches. This approach is tested in [12] where it was proven that the efficiency of the converter was higher by 0.3% for when an SiC antiparallel diode was considered compared to when only the body diode was present. Therefore, it was suggested to connect these antiparallel diodes in the DAB converter. Though, there are more discussions regarding this matter but since the focus of this thesis is only on studying the operation of the DAB model built, this case will not be further discussed.

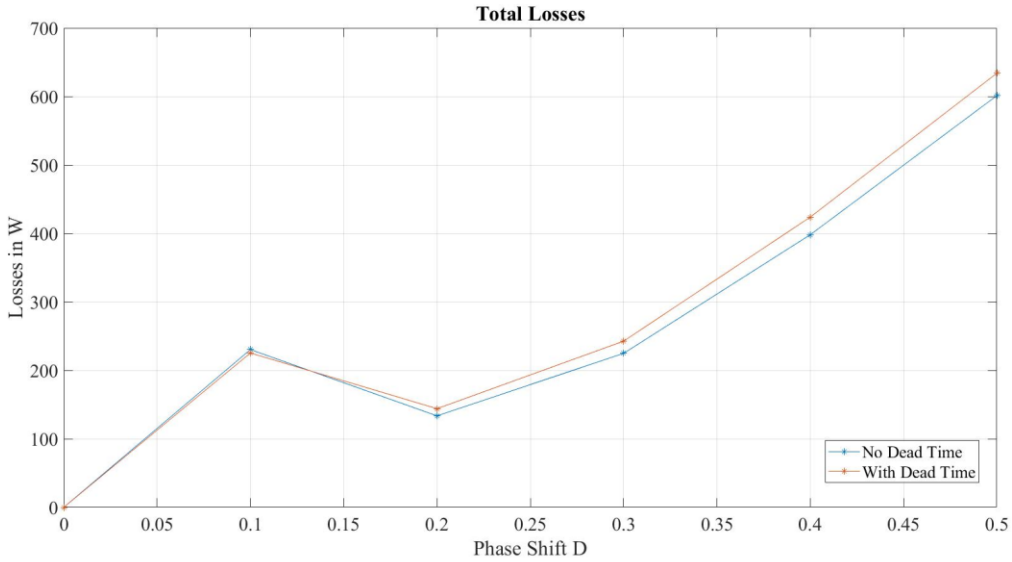

Figure 31 Total Losses Comparison for when the Dead Time is Present and Not.

The phenomena that occurred for when the dead time was not considered in terms of losses and low turn off current for D=0.2 are observed in this part of the study as well but will not be further commented since the same logic applies and the reason for this occurrence is further explained in the upcoming section.

3.4.3 Losses for D=0.19 Operation of the DAB Converter

For when the phase shift was D=0.2, it was noticed that the current was very small during the turn-off transition of the secondary swithces. This triggered the idea of studying the operation of the DAB converter around this region.

As it will be explained later in this thesis, the DAB converter is characterized by the ZVS capability and its boundary. For a certain phase shift values, the DAB Model used in this thesis will operate at the ZVS boundary. This phase shift value is obtained from:

$$D = \frac{Rn^2 + 4Lf_s - \sqrt{R^2n^2 + 16L^2f_s^2}}{2Rn^2} = 0.19 \qquad \textbf{3-23}$$

The PLECS model was run for these conditions and the switching losses and the currents flowing through the switches in the secondary H-bridge were observed.

The current at the turn-off time instance of the secondary H-bridge switches was found to be zero. This is evident from the generated plots from PLECS presented in Figure 32. This zero current value allows the switches to operate at zero current switching, ZCS, conditions, leading to zero switching losses during the turn-off of the switches.

The DAB converter is characterized by the zero voltage switching, ZVS, capability during turn-on of the switches whereas during turn-off, it generates switching losses. This led to the important finding in this thesis regarding the DAB converter operation. For when the converter operates at boundary, ZVS during turn-on and ZCS during turn-off is provided for the switches. This occurs only on the secondary H-bridge for the DAB model used in this thesis. For the primary H- bridge, the current value during the turn off transition, is considerable which as a result, generates switching losses.

The boundary phase shift value affects only the secondary H-bridge of the converter for when the DAB converter operates in Buck Mode. The operating modes of the converter and the ZVS and ZCS concepts will be further discussed in Chapter 4.

This analysis provided insight on the effect that the phase shift modulation scheme has on the DAB converter operation. This also shows the close relation between the phase shift value with the generated losses. This operating region of the DAB converter can be further developed with the aim of extending its operation.

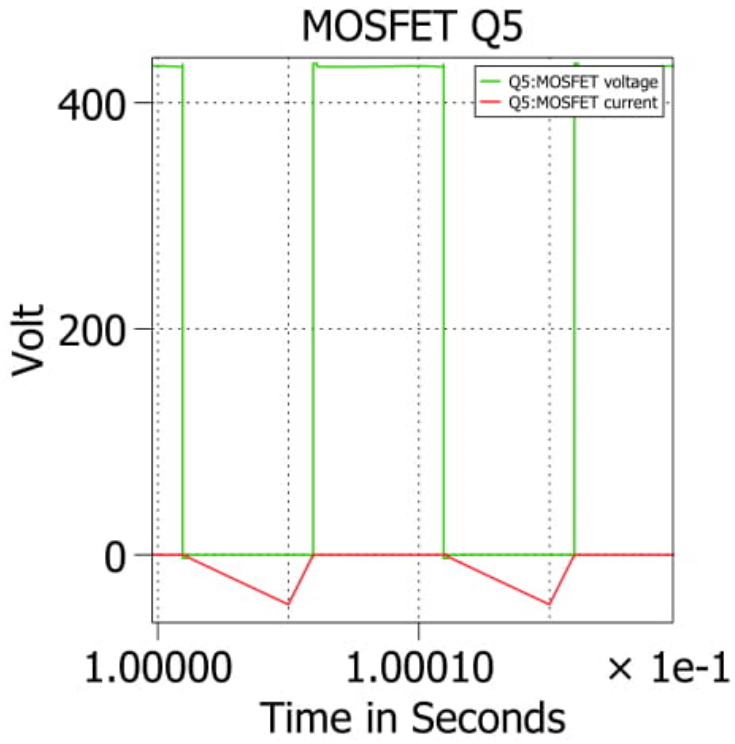

Figure 32 Voltage and Current Across Q5 Switch

3.4.4 Junction Temperature Relation with Phase Shift Value

An important observation that is made possible from the simulation based approach is that of the junction temperature for different operating conditions of the DAB converter. For this reason, the junction temperature of the MOSFET Q1 is noted for different phase shift values and the results are presented in Table 10 and visually presented by PLECS plots.

Phase shift D	**Heat Sink Temperature** $(°C)$	**Junction Temperature** $(°C)$
0.1	25.14	33
0.2	25.13	32.35
0.3	25.2	34.5
0.4	25.3	39.4
0.5	25.4	45.8

Table 10 Junction and Heat Sink Temperature for a Varying Phase Shift Value

From these results is can be seen that for lower phase shift values, lower junction temperature values are generated. This shows the relation of the junction temperature with the losses, for lower junction temperature, lower losses are obtained. The lowest junction temperature values correspond to D=0.2 which corresponds to the operating condition for when the lowest losses were obtained. For maximum power flow the highest junction temperature is generated, and highest losses are obtained according to the

previous analysis which shows the contribution that the junction temperature has on these losses.

For the heat sink temperature, it is noted that the temperature is almost constant for a varying phase shift vale, due to the very low thermal resistance chosen. As mentioned in the analytical approach, this low value is chosen by assuming an ideal heat sink. In a real application the heat sink temperature would be higher and varying.

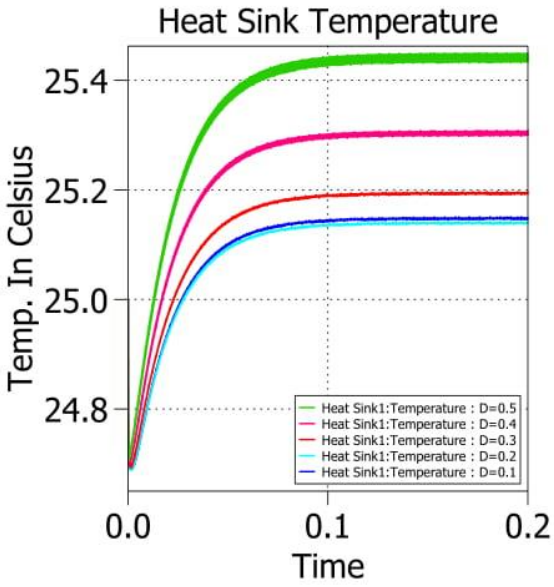

Figure 34 Heat Sink Temperature

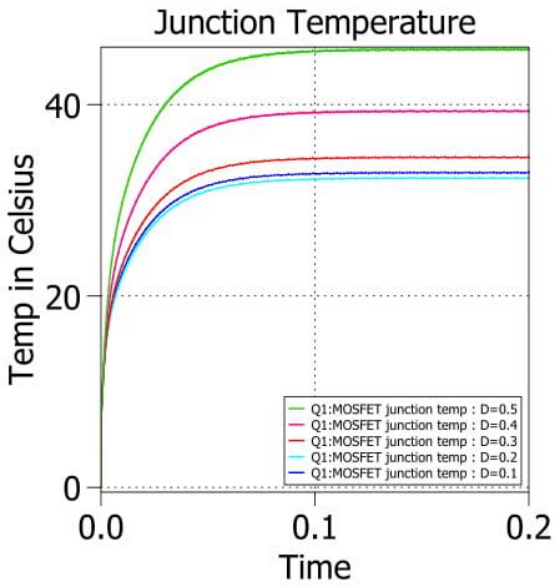

Figure 33 MOSFET Junction Temperature

3.5 Comparison Between Analytican and Simualtion Based Results

Two methods were used for estimating the losses and the reason behind this was comparing the results of these two approaches as well as ensuring that the results obtained from these two methods are trustable.

By looking at Figure 35 , which is a representation of the results in a visual way, it can be noted that the simulation-based losses are slightly lower compared to the results obtained from the analytical approach. Though, both the approaches are shown to be quite accurate and the difference between the results obtained is small.

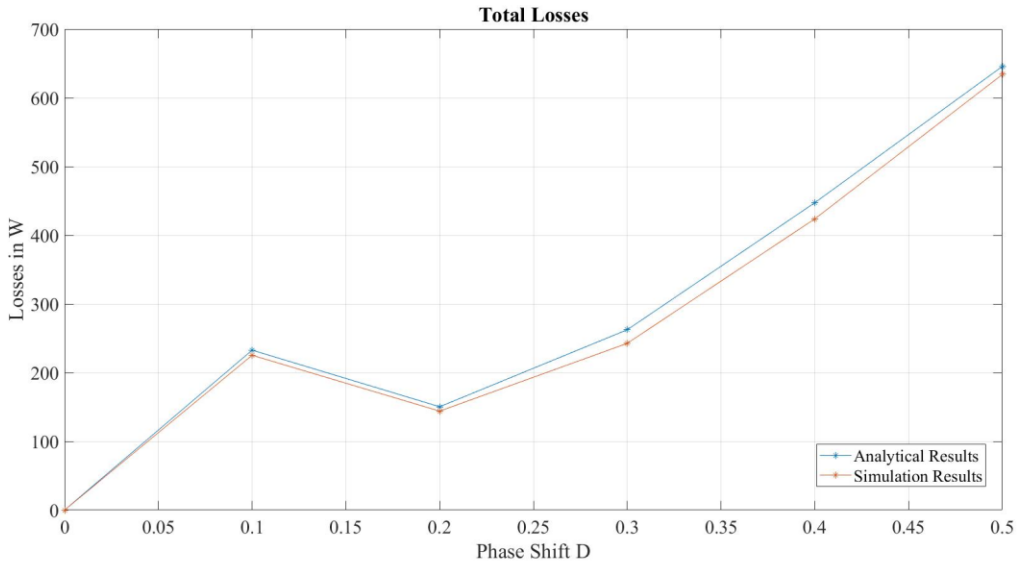

Figure 35 Total Losses Analytical Results Vs Simulation Results

The analytical approach aims at exact results through mathematical formulation, but it requires some assumptions due to the lack of needed input which when using a simulation software, these assumptions can be avoided. This is one of the reasons behind the difference in losses between the two methods.

In this study, for the analytical solutions, the plots from the datasheet were used where corresponding values were found but due to the lack of accurate approximation of the extracted values, less accurate results were obtained. The lack in input of the junction temperature in steady state and not considering it through the analytical approach did also contribute to this difference between results since in the PLECS Model, a varying R_{DSon} according to the junction temperature was implemented as well as the plots for turn on, off and conduction losses where accurately implemented in the model allowing for better and more precise results.

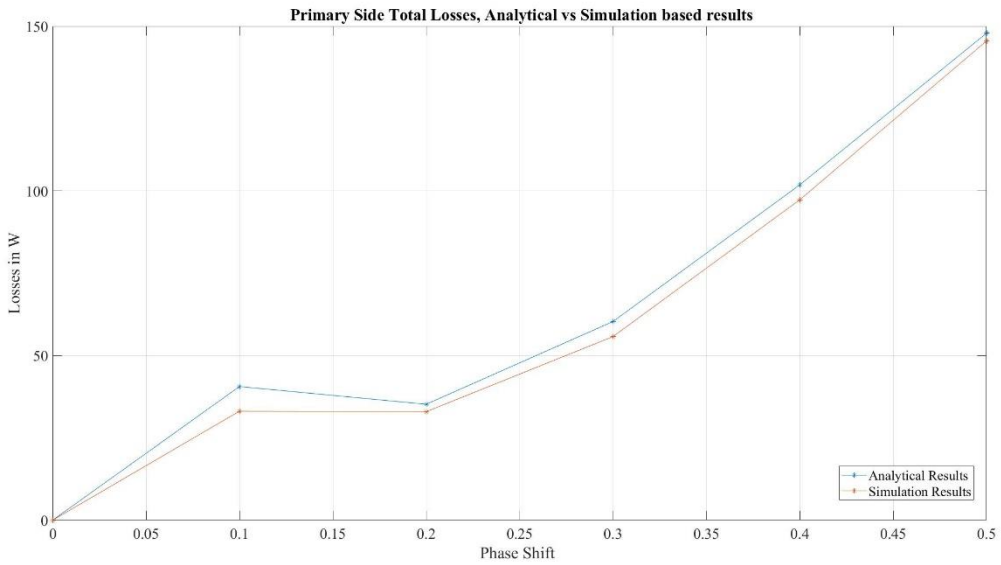

Figure 36 Primary Side Total Losses, Analytical vs Simulation Based Results

The analytical approach did not consider the voltage ripples in the output side and the calculation was based on the current flowing though the switches on both bridges, which was equal, and therefore the primary side losses and secondary side losses were equal which also resulted in higher total losses. The losses on the secondary H-bridge of the converter, from the simulation-based approach, are less compared to the primary H-bridge for all phase shift values and this causes less total losses compared to the aforementioned method for all phase shift values.

The plots below represent the difference from the two approaches for the conduction losses where it is visible that this difference is higher for the secondary H-bridge. The difference between the primary and secondary side conduction losses is evident for the simulation approach whereas the for the analytical approach it is not. As previously mentioned, PLECS follows a different method for calculation the conduction losses. It considers the voltage current plot provided from the datasheet and from previous analysis in [8] it is observed that the output voltage is characterized by ripples which are not considered in the analytical approach. The simulation approach takes these ripples into account and based on the UI plot in Figure 10 it estimates the conduction losses in secondary H-bridge. This method applies for both MOSFET and body diode losses which contribute to the total losses. The difference in conduction losses for primary and secondary bridge are visually presented in Figure 37 and Figure 38.

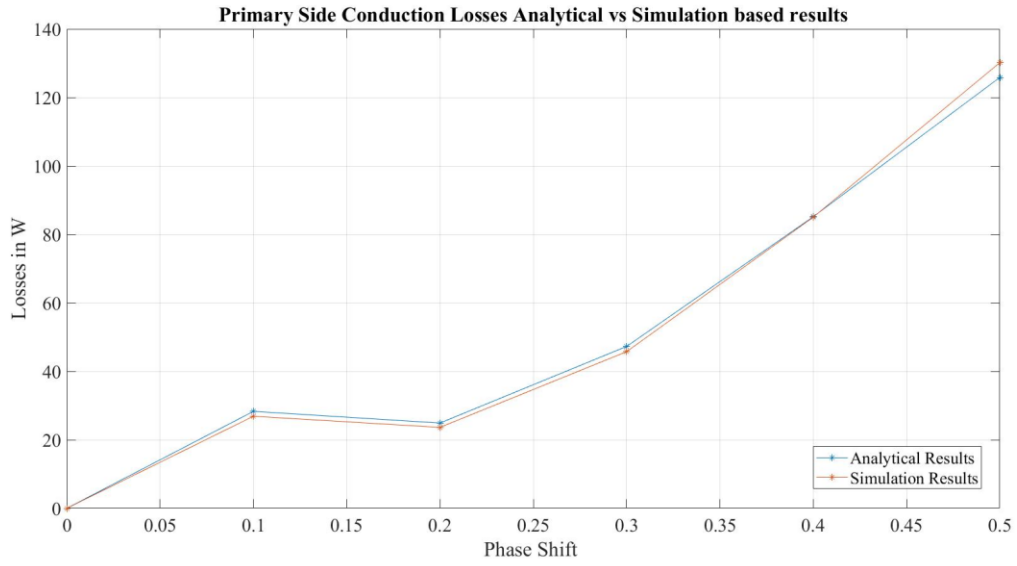

Figure 37 Primary Side Conduction Losses, Analytical vs Simulation Based Results

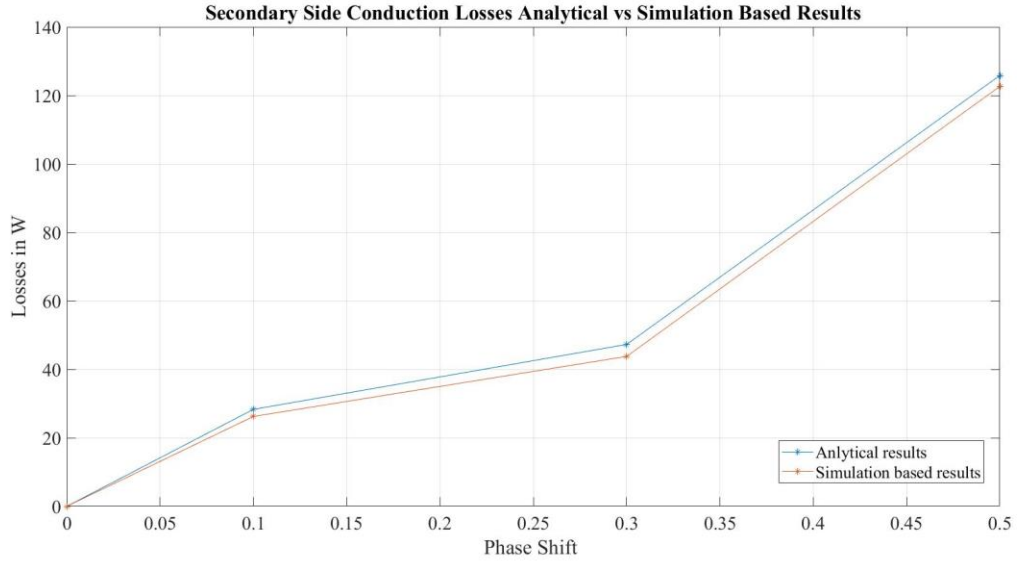

Figure 38 Secondary Side Conduction Losses, Analytical vs Simulation Based Results

The slight change in values for the current that flows through the switches and inductor current can also be noted and this is something that is observed even in [8] where the results obtained from simulation and from the analytical solution would be slightly different. This is also a factor that affects the difference in results.

The diode losses have a difference in obtained results from the approaches due to U_F values obtained from datasheet being used and these values extracted from the plot not being as accurate as when the PLECS extracts them from the implemented library Figure 39. This contributes to the total losses difference as well.

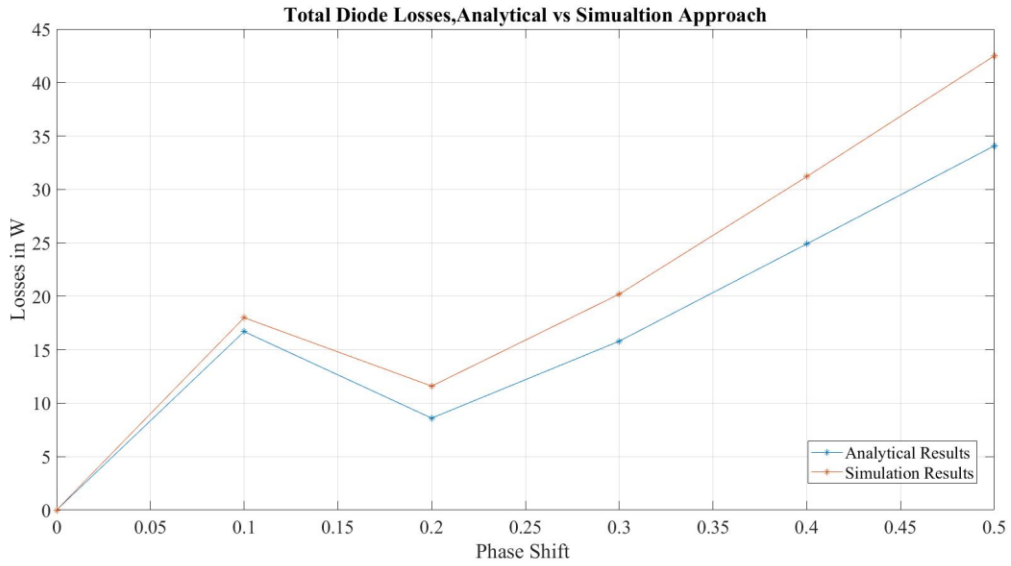

Figure 39 Total Diode Losses, Analytical vs Simulation Based Results

The conduction losses comparison is more direct than for the switching losses, since there is no accurate method to estimate the switching losses in an analytical method. The approach of calculating the switching losses is presented in section 3.3.2 where a comparison between these results with the simulation results are presented in the MATLAB plot below Figure 40.

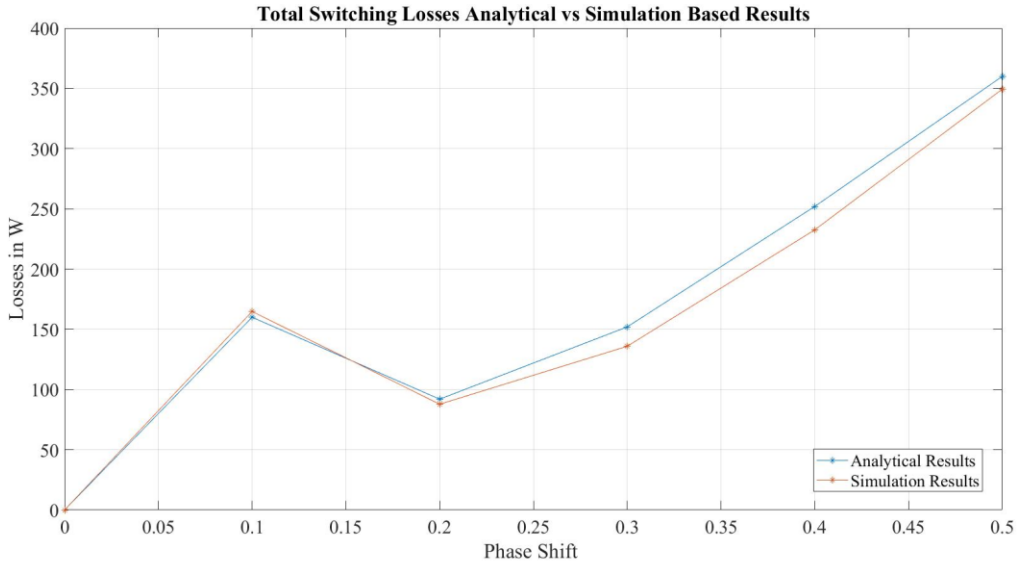

Figure 40 Total Switching Losses, Analytical vs Simulation Based Results

The analytical approach considers only the turn-off losses since the DAB converter is characterized by ZVS during turn on and assumes no ZVS for turn off of the switches. Though this is theoretically true, it was previously noted that on the secondary side for a phase shift D=0.19, ZCS was provided during turn off of the MOSFETs. These occurrences are not predicted by the analytical approach which also results in difference between the obtained results. The fact that the method used to calculate the losses in the analytical part is not direct and extracts the values in an inaccurate way, where an approximation of

two plots is conducted, leads to errors in results which contributes to the difference between the two curves presented in the aforementioned figure.

These two methods, analytical estimation of the losses and simulation-based estimation of the losses, have slightly different results due to the mentioned reasons. These results are considered accurate enough and are expected to be close to in practice estimation of losses. There is space for improvement of both methods such as designing the heat sink in order to properly implement the varying R_{DSon} and to consider the varying output voltage for the analytical approach. Though the simulation approach is expected to be closer to practical results, it has space to include more varying factors and parameters that affect the losses in practical applications as well as implement more data regarding the diode losses and the diode conduction time. These improvements would allow for better and more trustable results.

3.6 Reasoning Behind Low Losses

The total losses are considerable low compared to the total transferred power and the main reasons for this are the soft switching capability that the DAB converter has which results in low total switching losses and due to the SiC power device property which allows for low conduction losses. An important factor is also the fast switching in SiC power devices which allows for low switching losses.

These low losses that characterize the DAB converter due to its properties, are one of the of many attractions that this converter provides where throughout the years, the losses have been mitigated.

Though these losses are considered acceptable, there are many studies in trying to lower these losses where they mostly focus on switching losses. Expanding the ZVS operation is the main approaches for mitigating these losses thus, increasing the efficiency of the converter. For this reason, this thesis looks closer into the ZVS property of the DAB converter and its ZVS capability as well as the conditions that will allows for ZVS operation.

3.7 Discussions

It was observed from both approaches that the losses increase for an increase in the phase shift value due to the increase of the RMS current flowing through the switches which results in more losses. This logic was noted not to be true for D=0.2 where the losses obtained were lower compared to D=0.1, even though the power transfer was higher. At this phase shift the RMS current is smaller compared to the mentioned phase shift value and since the losses are directly related to this current, lower losses are obtained. For this reason, this phase shift was observed further in the simulation approach since the analytical approach lacks space for further study regarding the matter.

The conduction losses obtained from the approaches were low compared to the total transferred power, proving so the low losses property of the DAB converter. Due to assumptions made, the analytical results were expected to not be equal to the simulation

results. The junction temperature was assumed constant at a certain arbitrary value which was used to obtain R_{DSon} and the secondary H-bridge losses calculation did not consider the output voltage ripples.

The simulation approach did surpass these obstacles where a control loop was built in order to obtain the varying R_{DSon} and the output voltage ripples were automatically considered by the software when estimating the losses.

The analytical estimation of the switching losses was not accurate since an approximation of the plots provided by the datasheet of the MOSFETs was made in order to obtain these losses. The DAB Model was built in the PLECS widow which allowed to implement all the required data provided by the datasheet of the MOSFET in an accurate manner which provides accurate estimation of the switching and conduction losses.

In the simulation approach many other properties of the DAB converter were observed, such as the ZVS and ZCS capability of the converter at D=0. 19 which resulted in zero switching losses. At this point the switches would realize soft switching both during turn-on and turn-off transition on the secondary H-bridge. This raises more attention on the DAB converter operating at the ZVS boundary, D=0.19, which is to be studied further in the upcoming chapter.

The junction temperature and heat sink temperature were only able to be accurately observed in the simulation-based approach from where it was noted that an increase in junction temperature resulted in an increase of the total losses. The heat sink, which allow for the switches not to overheat, temperature was observed to be constant through the study. This occurred due to the low thermal resistance chosen for this model.

The effect of the dead time was only able to be noted in the simulation approach where for when the dead time was present, higher total losses were obtained due to the body diode conduction. Lower MOSFET losses were obtained since these switches would conduct for less time in this case.

Differences in the primary and secondary bridge losses were noticed throughout the whole study in the simulation-based approach due to the output voltage dependency method PLECS uses. This difference in losses were presented by MATLAB plots. This difference was evident in both cases for when the dead time was considered and not which results in the dead time not having an effect on this occurrence. Since the losses are lower on the secondary side, the focus would be on how to minimize the losses of the primary side, such as by expanding the ZVS operating range or by considering the ZVS boundary operation of the converter.

For when the dead time was present, diode conduction losses were obtained and as well as voltage dips were observed. Even though this diode conduction contributed to the total losses, it provides the ZVS operation during turn-on of the MOSFETs resulting in lower switching losses. Therefore, the ZVS property of the converter is analyzed in the upcoming chapter.

From comparing the approaches, it was noticed that the difference was not very big for the primary H-bridge total losses whereas the difference was bigger for the secondary H-bridge total losses due to the aforementioned reasons. The biggest difference was noticed to be on the switching losses since the analytical approach was known not to be accurate whereas the simulation based was known for its favorable ability of implementing the required data for estimating the switching losses. For the boundary

operation of the DAB converter ZCS was provided during turn-off of the secondary switches, which was not taken into account in the analytical approach, contributing so to the difference between the approaches.

A difference in the diode conduction losses results obtained from the two approaches was also evident due to the analytical approach not accurately extracting the forward voltage value from the datasheet plot.

From the analysis performed it is concluded that the analytical approach needs to be further developed or combined with software reading of the datasheet data. This would allow for better trustable results. Whereas the simulation based approach provides satisfying values but the amount of time in estimating these losses using this approach is much longer since it requires more work on building the converter in order to obtain the required results. The simulation running time can be longer depending on the implemented data on the converter which also needs to be improved in order to use the time efficiently in real life tasks.

From the observations made the focus comes on the ZVS operation of the converter since it directly contributes to the switching losses and therefore it takes an important part in this thesis.

4 Zero Voltage Switching

4.1 Introduction

Among the most prominent advantages of a DAB converter is the Soft Switching capability, ZVS (Zero Voltage Switching). In estimating the losses, this concept was briefly introduced where this property of the converter would lead to lower switching losses. In order to better understand this merit of this converter, the theory behind the concept of ZVS, different operating conditions backed by the working principle of the converter will be discussed. The DAB converter's operating Modes will be used as a base and analyzed in terms of ZVS operation during turn on of the switches for two different scenarios. For when no additional components are considered and for when parasitic capacitors are connected in parallel with the switching devices. The working principle of these two scenarios will be introduced with the aim of analyzing the operation of the DAB converter under ZVS Conditions.

To realize ZVS in the DAB converter, certain conditions have to be satisfied. Therefore, this thesis presents these conditions and conducts calculations in order to define them and check the operation of the DAB converter under these conditions. Dead time length and inductor current value are among the most important parameters which affect the ZVS operation of the switches and therefore, this thesis analyzes these parameters in terms of the DAB converter ZVS operation.

The ZVS Boundary will be built based on the analysis conducted which will allow for an easier perception of the ZVS operation of the converter. In terms of the phase shift value, this plot will provide the insight on the switching behavior of the converter.

4.2 Introduction to ZVS and ZCS Concepts

After performing the estimation of losses, where the conduction and switching losses were presented, naturally the focus is set on the switching losses and the reasoning behind such low switching losses in certain phase shift values. These losses are closely related to the switching behavior of the power devices where in power electronic circuits, the topologies can be soft switched or hard switched [10].

The DAB converter has the merit of realizing soft switching which means that the voltage across the switch is zero in the switching moment which results in low switching losses. For a better understanding of the soft switching capability concept, the theory behind Zero Voltage Switching and Zero Current Switching is provided.

The basic concept behind ZVS and ZCS is the capability of the switching device to turn-on or turn-off at zero voltage or current. ZVS and ZCS are closely related to the resonant technologies where these resonance techniques force the voltage or current in the semiconductor to be zero. As a result, this would provide soft switching capability and thus

reduction or elimination of the switching losses, regardless of the operating frequency and the input voltage [18].

The ZVS, ZCS technique is applicable in all switching topologies such as buck, boost converter and half and full bridge converters. Since the DAB converter is composed of two full bridges than this technology can be applied easily.

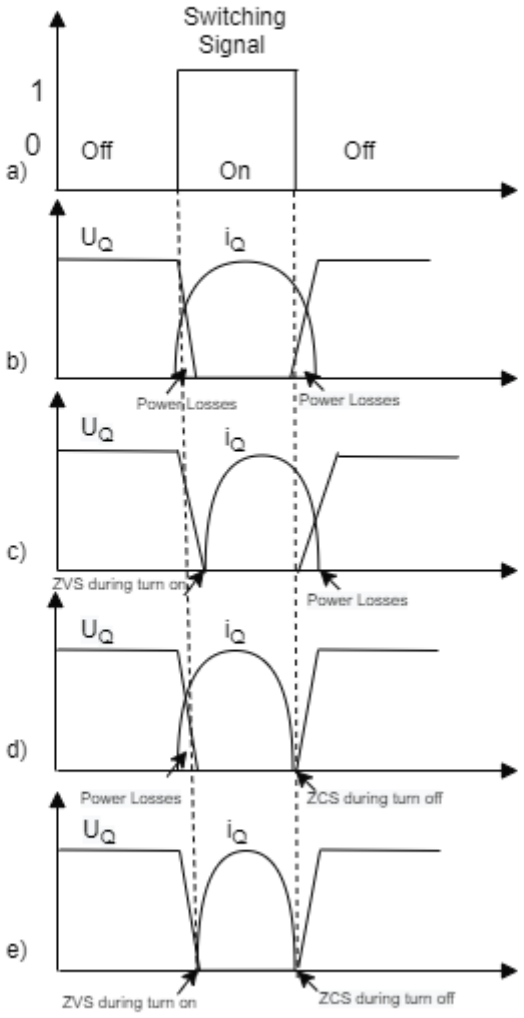

Figure 41 Current and Voltage Waveforms for Different Switching Conditions a) Switching Signal, b) Hard Switching During Turn-on and Turn-off of the Switch, c) ZVS During Turn-on of the Switch, d) ZCS During Turn-off of the Switch, e) ZVS During Turn-on and ZCS During Turn-off of the Switch.

One important note to make is that ZVS is preferred over ZCS for converters that employ MOSFETs [4]. ZCS is known for zero switching losses during turn off while minimizing the turn-on losses whereas ZVS is known for elimination the turn-on losses. Since the DAB converter operates at a high switching frequency, the turn-on losses are low or absent due to the ZVS capability of the converter[19].

High efficiency and operation at high frequency are among the main aims of the optimization for the converter where the losses play a major role. Therefore, these losses have to be minimized as much as possible, hence ZVS capability has a major focus on this thesis and is further analyzed. Among the merits that the soft switching capability, ZVS, will bring for the DAB converter are:

- No power loss during turn-on transition of the switches.
- High efficiency with high input voltage at any frequency.
- Reduced electromagnetic interference during transition.
- Short circuit tolerance [18].

4.3 ZVS Theory and Working Principle

The DAB converter is widely known for its ZVS capability, which means that the power device will turn-on at a zero-voltage across the switch. In the DAB converter this is made possible by the conduction of the body diodes before the MOSFETs are turned on. During this time instance, the current will flow though these diodes right before the MOSFETs receive their gate signal which would allow for the MOSFETs to turn on at Zero Voltage without the need of any additional components, such as parallel capacitors connected though the switch, to provide this voltage level across the switches. Later in the thesis the effect of adding parasitic capacitors across these switches will be presented together with its effect on ZVS Capability. Different operating instances are to be studied and analyzed in this part of the thesis with focus on the ZVS during turn-on of the switches by observing the diode conduction conditions and the current flowing though the switches.

Firstly, the ZVS concept for one switch is presented. The theory behind the conduction of the MOSFET is that it requires a gate signal and regardless of the voltage V_{DS} sign across this MOSFET, the conduction of the MOSFET is assured as long as it receives a gate signal. Whereas for the body diode, the current has to flow from source to drain in order for it to conduct, since it is an uncontrollable switch, meaning the voltage across the diode has to be $-V_{DS}$, for the diode to conduct. Even though, the MOSFET is independent on the voltage sign or the current direction in normal operation for it to conduct, in order to provide ZVS the current that flows through the switch has to be negative for the diode to conduct firstly and the MOSFET to turn on at ZVS. One important remark is that even when the current flowing through the switches is negative, it will flow on the switch that has the least resistance which the MOSEFTs are characterized by.

For the DAB converter used in this thesis, both the cases when the MOSFETs turn on at ZVS and no ZVS will be presented and explained further where these operations are closely related to the phase shift value. The inductor current also plays an important role in the ZVS operation of the switches since the direction that this current flows defines the sign of the current flowing though the switches.

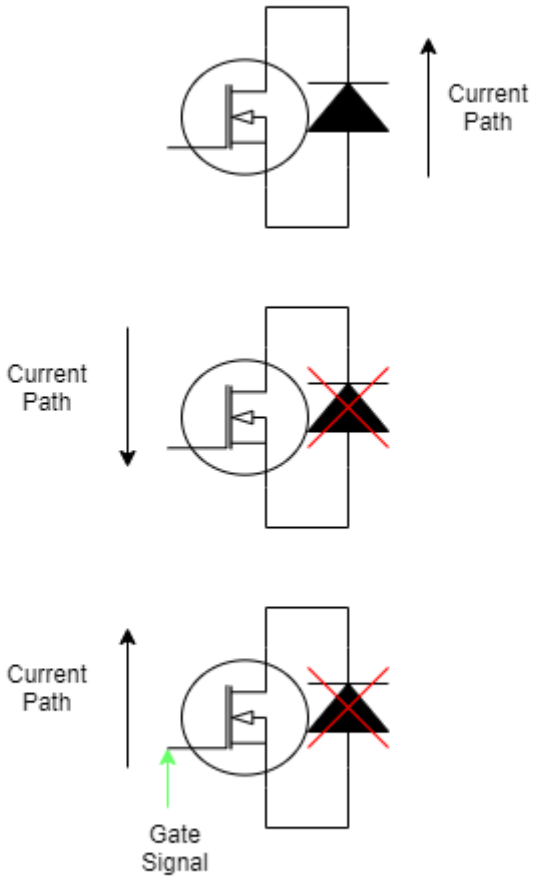

Figure 42 Current Path in the DAB Power Device

To elaborate more on the diode and MOSFET conduction and the ZVS concept on the DAB converter, different modes are presented where according to the inductor current sign and gate signals, the conduction scenario of the switches is defined. The modes presented in this thesis are based on the analysis performed in [8].

The first operating model used to study the ZVS capability of the DAB converter is for when $\frac{k-1}{2k} \leq D$ for which, as it can be seen in Figure 47, the zero crossing happens before t_1.

In Mode 1, which corresponds to t_0 time instance, the inductor current is negative. The MOSFET Q_1 and Q_4 should conduct regardless of the inductor current direction as long as they receive a gate signal which does not happen at t_0 time instance due to a delay time of the gate signal. This delay time is also known as the dead time during which the diode will conduct. For the diode to conduct the condition of the current flowing from source to drain has to be fulfilled. As it can be seen from the arrows depicted in the plot below, the current flowing through the switches Q_1 and Q_4 is negative in this Mode, allowing so for the diodes D_1 and D_4 to conduct which provides ZVS during turn on of these MOSFETs.

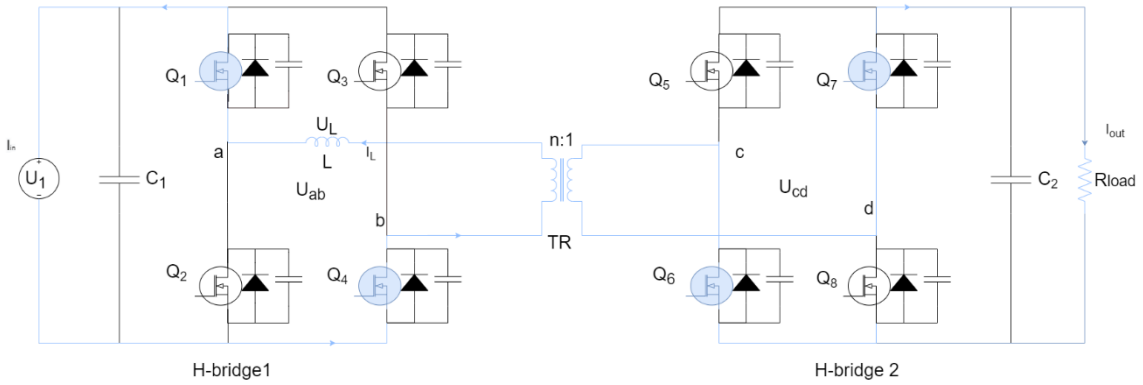

Figure 43 DAB Converter, Mode 1.

In Mode 3, t_1 time instance, switches Q_5 and Q_8 will turn on after the dead time. By observing the inductor current direction, it is noted that for a positive inductor current the current flowing through the switches Q_5 and Q_8 is negative, allowing so for the diodes D_5 and D_8 to conduct. Hence, ZVS is provided for Q_5 and Q_8 due to this diode conduction.

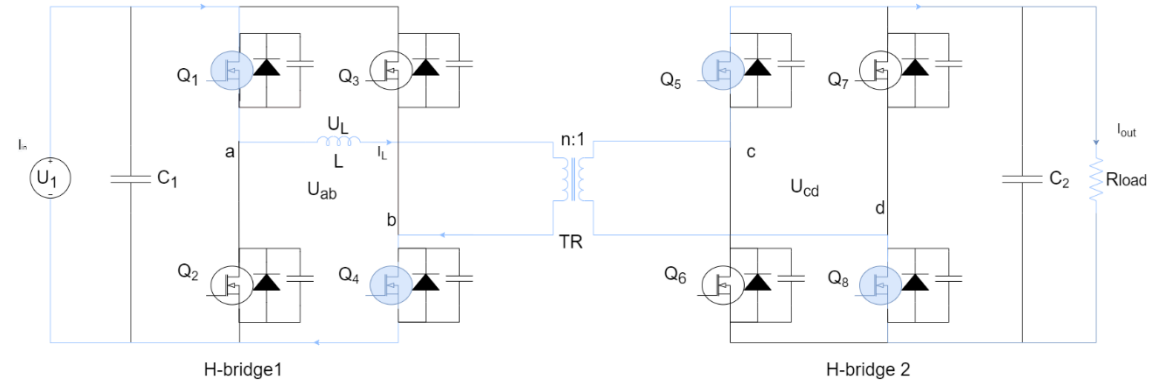

Figure 44 DAB Converter, Mode 3.

Mode 4 accounts for t_2 time instant when the inductor current is positive and the switches Q_2 and Q_3 will turn on. The current flowing though Q_2 and Q_3 switches during this mode is negative, allowing so for the diode to conduct and so providing ZVS during turn-on of Q_2 and Q_3.

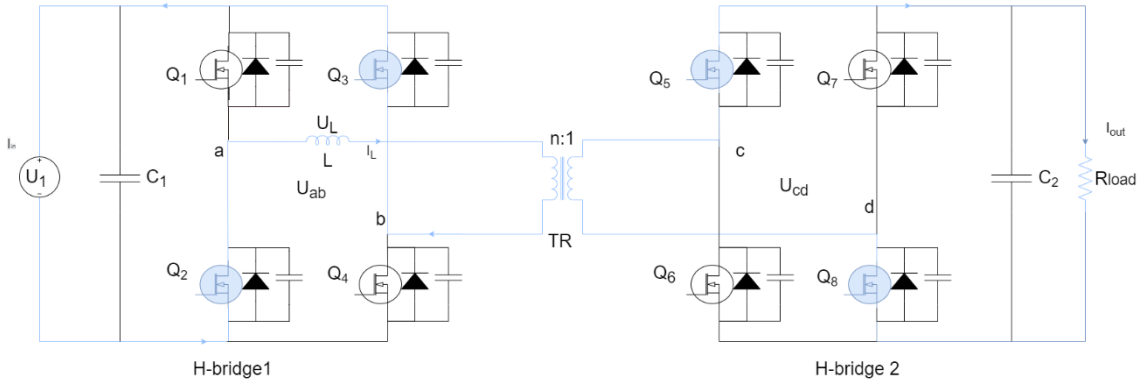

Figure 45 DAB Converter, Mode 4.

For Mode 6, t_3 time instance, secondary switches Q_6 and Q_7 will turn on which, same as in the other modes, requires a negative current in order for the diodes to conduct. This is provided by a negative inductor current where according to the direction of the current flowing though the switches depicted in the plot below, the diodes D_6 and D_7 will conduct during the dead time and so the Q_6 and Q_7 switches will turn on at ZVS.

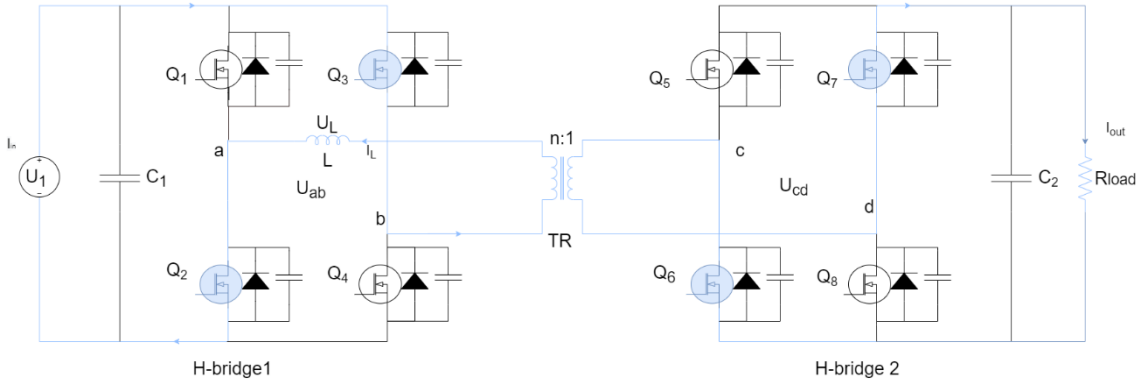

Figure 46 DAB Converter, Mode 6.

Notice that Mode 2 and Mode 5 are skipped since for these Modes the operation of the switches is not changed, meaning no switches are turned on or off. Regardless of the inductor current changing its sign, which was also previously explained, the MOSFETs still conducts. This happens because the MOSFETs at this point are only dependent on the gate signals. As long as they receive a gate signal, despite the current flowing through these switches change direction, they will conduct, which is seen to happens during the aforementioned Modes.

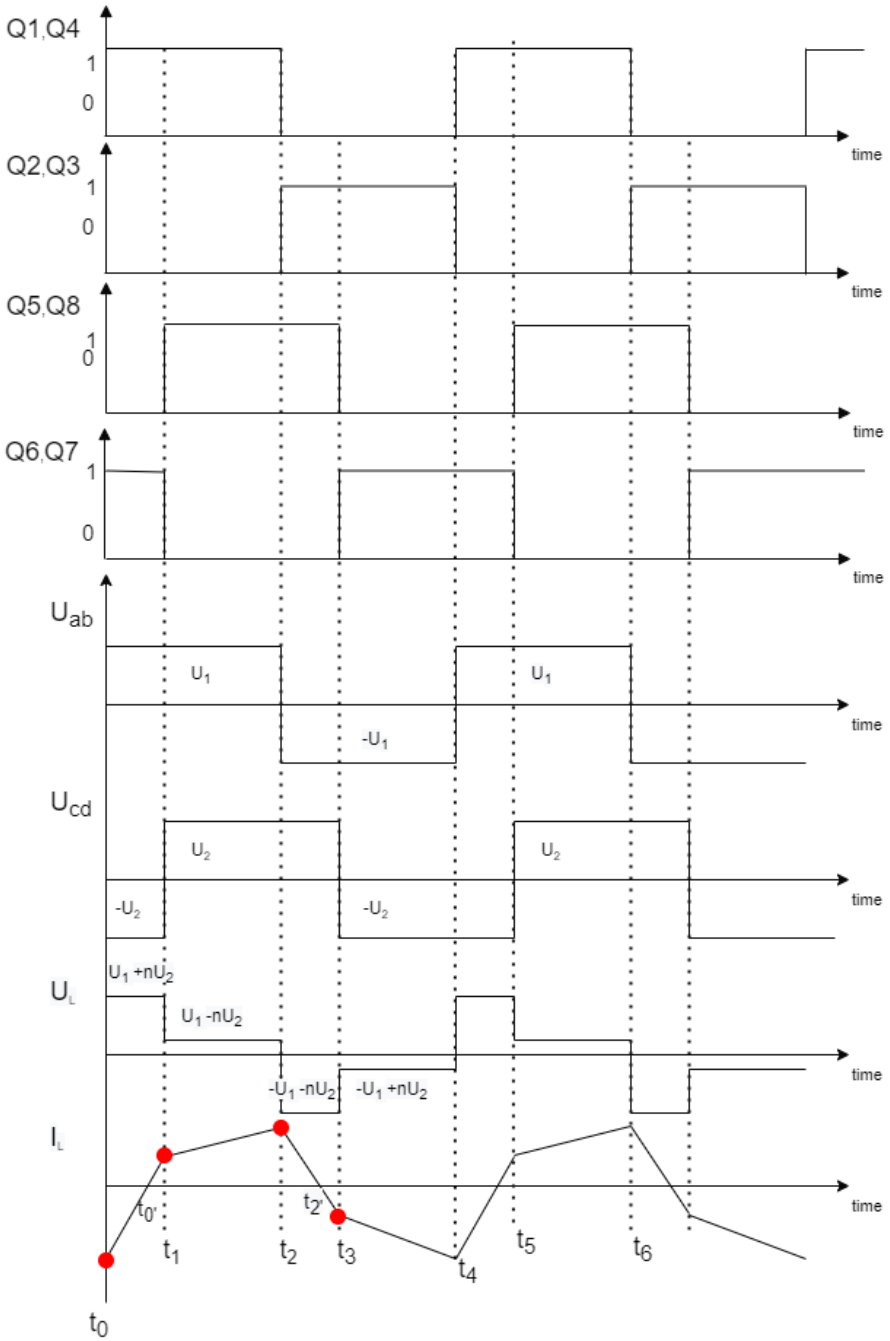

Figure 47 Single Phase Shift Modulation Scheme Waveform for $D \geq \frac{k-1}{2k}$ and $k \geq 1$.

From the above observation it is noted that the operation of the diode and the current sign flowing though the switches is closely related to the inductor current sign. Therefore, by closely analyzing the above Modes, the following equations are generated which depict the requirements for the inductor current sign which would allow for ZVS of the switches at the certain time instances.

$$\boldsymbol{I_{Lt_0} < 0 \ (for \ Q1, Q4)} \qquad \textbf{4-1}$$

$$\boldsymbol{I_{Lt_1} > 0 \ (for \ Q5, Q8)} \qquad \textbf{4-2}$$

$$\boldsymbol{I_{Lt_2} > 0 \ (for \ Q2, Q3)} \qquad \textbf{4-3}$$

$$\boldsymbol{I_{Lt_3} < 0 \ (for \ Q6, Q7)} \qquad \textbf{4-4}$$

By the above investigation of different modes for when $\frac{k-1}{2k} \leq D$ is true, ZVS was provied for both switches in the primary and secondary side. In this part of the thesis, the case when the above condition is not satisfied, meaning $\frac{k-1}{2k} > D$ operation of the converter, is to be studied in order to see what occurs in such conditions. The plot below depicts the operation of the DAB converter for when $\frac{k-1}{2k} > D$, which corresponds to low phase shift operation region. The same logic is followed for this part of the study as well by observing the current flowing though the switches and defining the conduction of the diodes.

The first time instance t_0 depicted in Figure 48 corresponds to Mode 1 presented in the previous study, where the current flowing during the dead time is negative allowing for D_1 and D_4 to conduct and so providing ZVS for switches Q_1 and Q_4.

At t_1 time instance, the inductor current is negative when Q_5 and Q_8 are about to conduct. This differs from the previous case where the inductor current was positive which allowed for the current flowing though the switches to be negative. In this case Q_5 and Q_8 won't be able to turn on at ZVS since the diodes D_5 and D_8 will not conduct due to the positive current flowing though the switches.

The third time instance t_2 where Q_2 and Q_3 switches will start to conduct, the current flowing though the switches in negative which allows for D_2 and D_3 to conduct during the dead time. The switches Q_2 and Q_3 receive their gate signal after this dead time, and they turn on at ZVS due to the conduction of the diodes prior to them turning on.

The inductor current at t_3 is again positive where the switches Q_6 and Q_7 are to be turned on. Prior to this, the diodes have to conduct to allow for ZVS of these switches but by observing the circuit it is noted that the current does not flow from source to drain resulting in D_6 and D_7 not being able to conduct. This results in hard switching of the Q_6 and Q_7 MOSFETs.

The conditions specified in 4-1, 4-2, 4-3 and 4-4 are not all satisfied for this operation of the DAB converter. It is observed that the secondary H-bridge loses its ZVS capability for when $\frac{k-1}{2k} > D$, whereas the primary H-bridge does not. The DAB converter will lose the ZVS capability in the secondary side when it operates in Buck Mode. This is an important note for the DAB converter where even though the converter is not operating in the most favorable conditions, at low phase shift D values, the primary side of the converter does not lose its ZVS capability, which is one of the most prominent characteristics of this converter.

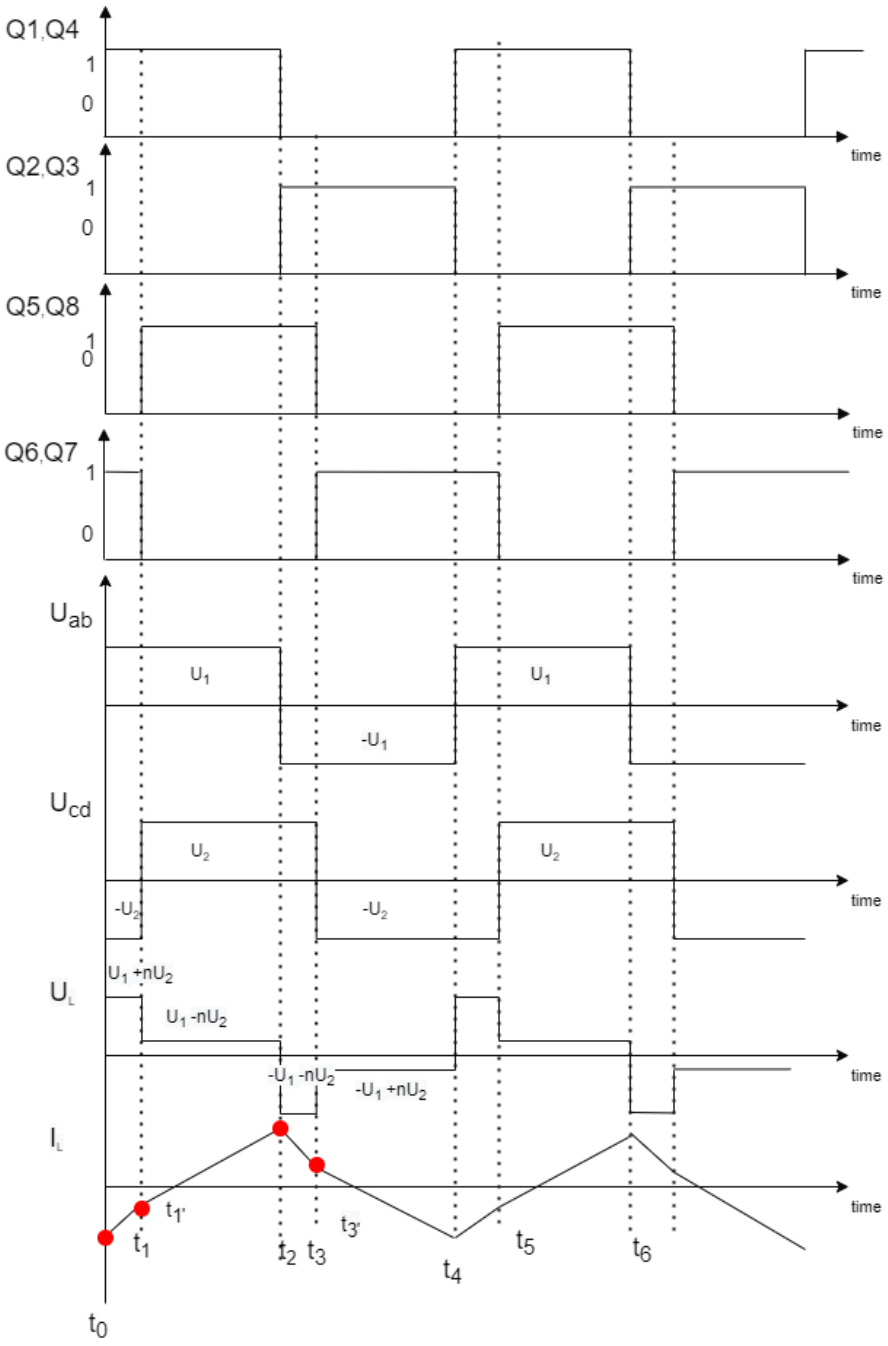

Figure 48 Single Phase Shift Modulation Scheme Waveform for $D < \frac{k-1}{2k}$ **and** $k \geq 1$.

4.4 Conditions for Realizing ZVS During Turn-on of the Power Devices

4.4.1 Condition Without Additional Components

In the previous section, the operation of the DAB converter was presented in terms of ZVS capability of the switches. The conditions which would ensure ZVS during turn on of the switches were mentioned but without further studies. In this section the focus will be on these conditions and in defining them. The phase shift effect on ZVS operation takes an important part in this part of the thesis as well.

For when the voltage convention ratio is equal to one, ZVS is ensured despite the conditions that are required for ZVS operation. This is true for when the output voltage is equal to the input voltage providing so $k = 1$. This property will be observed later when the ZVS boundary will be built.

For a 50% duty cycle and a phase shift $0 \leq D \leq 0.5$, the primary voltage U_1 is higher or equal to the secondary side voltage U_2, resulting in $k \geq 1$ being true. For this operating region, $\frac{k-1}{2k} \leq D$ should be met in order to provide ZVS during turn on in both bridges, according also to the analysis conducted in the previous section. If this is not assured than no ZVS is ensured in the secondary H-bridge. This is true when $\frac{k-1}{2k} > D$ which corresponds to the low phase region as shown in Figure 48 it can be seen that the zero crossing happens before t_1.

For ZVS to be provided for the switches during turn on, the zero crossing has to happen before or during $\frac{DT_S}{2}$ time instance, which can be presented by the following relation:

$$\boldsymbol{t_0' \leq \frac{DT_s}{2}} \qquad \textbf{4-5}$$

where t_0 is expressed by [20]:

$$\boldsymbol{t_0' = \frac{T_s[nU_1+U_2(2D-1)]}{4(nU_1+U_2)}} \qquad \textbf{4-6}$$

For when this relation is not satisfied than ZVS is not provided for the secondary bridge during turn-on of the secondary switches.

For the DAB Model used in this thesis, the aforementioned conditions are evaluated for different phase shift values where these values presented are according to the ZVS boundary. The phase shift value corresponding to the converter operating on the ZVS boundary is defined by:

$$\boldsymbol{D = \frac{Rn^2 + 4Lf_s - \sqrt{R^2n^2 + 16L^2f_s^2}}{2Rn^2} = 0.19} \qquad \textbf{4-7}$$

and this value is used as a reference for the other phase shift values that are expected to either be in the ZVS boundary or out.

For the phase shift value that corresponds to the ZVS Boundary D=0.19, the previous relations are checked as well as two other phase shift values that are expected to be within and out of the ZVS Boundary where this boundary will be built at a later stage of this thesis.

For when the converter operates at ZVS boundary, D=0.19, the following results are obtained. The voltage convention ratio for this phase shift value is:

$$\boldsymbol{k = \frac{U_1}{nU_2} = \frac{700V}{430.9V} = 1.6244} \qquad \textbf{4-8}$$

from where the first condition is clearly satisfied since the converter operates at ZVS boundary, $\frac{k-1}{2k}$ is expected to be equal to D :

$$\boldsymbol{\frac{k-1}{2k} \leq D} \qquad \textbf{4-9}$$

$$\boldsymbol{\frac{1.1905-1}{2x1.1905} \leq 0.19} \qquad \textbf{4-10}$$

$$\boldsymbol{0.19 = 0.19} \qquad \textbf{4-11}$$

The other condition was that of the zero crossing where from the following calculations, this condition is also assured:

$$\boldsymbol{t_0' = \frac{T_s[nU_1 + U_2(2D-1)]}{4(nU_1 + U_2)} = 9.5)x10^{-7}} \qquad \textbf{4-12}$$

$$\boldsymbol{t_0' \leq \frac{DT_s}{2}} \qquad \textbf{4-13}$$

$$\boldsymbol{9.5x10^{-7} = 9.5x10^{-7}} \qquad \textbf{4-14}$$

In the table below the result for other phase shift values are presented where it is noted that for a phase shift out of the ZVS boundary the conditions are not satisfied, D=0.1, whereas for a phase shift greater than the ZVS boundary phase shift value, the conditions are satisfied allowing for ZVS during turn on of the power devices. The reason why these conditions define ZVS is since they assure the current direction through the switches allowing the diodes to conduct and so providing ZVS.

D	**k**	**t_0**	$\boldsymbol{\frac{k-1}{2k}}$	$\boldsymbol{\frac{DT_s}{2}}$	**Conditions**
0.1	2.77	$1.3088x10^{-6}$	0.31	$5x10^{-7}$	Not Satisfied
0.19	1.6244	$9.5x10^{-7}$	0.19	$9.5x10^{-7}$	Satisfied
0.3	1.1905	$9.0217x10^{-7}$	0.08	$1.5x10^{-6}$	Satisfied

Table 11 ZVS Conditions

For when the phase shift is D=0.1 the conditions are not satisfied resulting in no ZVS on the secondary bridge since the primary bridge, from the previous observation, did not lose its ZVS capability in Buck operation of the DAB converter. For when D=0.3, ZVS is assured in both bridges according to the satisfaction of the condition.

These conditions make an exemption for when D=0.5 which corresponds to k=1 where the DAB converter switches will turn on at ZVS independent of other factors.

For this study the dead time effect was ignored, and the parasitic capacitor was not considered. This resulted in an easier approach of the working principle of ZVS for the DAB

converter but in the original model used for the estimation of the losses in this thesis, the dead time is defined, and parasitic capacitors are present in the MOSFETs which are connected in parallel with all switches. Therefore, in the following section, this case will be studied.

4.4.2 Conditions for Realizing ZVS for when Parasitic Capacitors are Present

The DAB converter realizes soft switching during turn on of the devices by allowing for the body diodes to conduct whereas hard switching is provided for turn off of the devices resulting in switching losses. Therefore, parasitic capacitances are added in order to minimize these turn off losses.

The turn-off of the switching device is a more complex state in terms of ZVS capability. Many studies have been conducted and many suggestions have been made. The most known method is that of realizing ZVS by connecting a parasitic capacitor across the transistor.

In lack of a parasitic capacitance connected through the transistors, resonance occurs between the coupling inductance and the output capacitance of the device. A high initial current fall and rapid voltage rise across the device during turn-off due to the low output capacitance value will occur which will provide switching losses during turn-off of the device [21].

Adding a parasitic capacitance to all 8 switches would surpass this phenomenon but it also has its own requirements and boundaries of realizing ZVS which will be further analyzed in the upcoming sections. This parasitic capacitor connected in parallel with the MOSFET will ease both turn-on and turn-off transition where the working methodology of this concept will be explained in the following section.

4.4.3 Working Principle of DAB converter with Parasitic Capacitors

During the transition of the switches from one state to another, there is a certain delay time which is also known as the dead time where the phenomena that provide ZVS occur. During this time the parallel capacitors connected to the switches get charged and discharged respectively by the leakage inductor current which allows for the voltage across the switches to be zero before them turning on. In this paper the switches are SiC MOSFETs which have a body diode and parasitic capacitors connected in parallel to them. In terms of the capacitor value, it will be assumed that the value chosen fulfils the requirements for allowing ZVS for this part of the study.

When the switches are transitioning, which is also when the resonant transition happens, the inductor current will have the role of charging and discharging all the parallel capacitors connected to the switches which ideally is a lossless process[21].

An illustration of the Modes of the DAB converter which were analyzed in [8] paper will be presented, where for this approach, the dead time will be considered and the events that happens during this time will be presented accordingly.

Considering that the transformer turn ratio is 1, it will make this study easier to interpret since the primary and secondary side will share the same inductor current.

For the transition from (t_0-t_1) to (t_1-t_2) time interval the inductor current is positive and Q_1 and Q_4 still conduct and the voltage across these switches is zero, whereas Q_5 and Q_8 will start conducting while Q_6 and Q_7 will turn off. But right before Q_5 and Q_8 start conducting, during the dead time, none of the MOSFETs conduct on the secondary side and the inductor stored energy will circulate a current which is responsible for charging and discharging the parasitic capacitors. The capacitors connected to Q_6 and Q_7 are going to be charged during this period whereas Q_5 and Q_8 capacitors will be discharged in order for the switches to turn on at zero voltage. The charging and discharging process will bring the voltage across the MOSFETs to zero. This process allows for Zero Voltage Switching which allows for zero losses. The charging and discharging period will be shorter than the dead time and therefore after this process is finished the inductor current will have to flow through the diodes D_5 and D_8, considering that a diode can only conduct when the current flows from source to drain. After the dead time the gate signal is applied to Q_5 and Q_8, where the current is transferred from D_5 and D_8 to Q_5 and Q_8 which allowing for ZVS [21], [22].

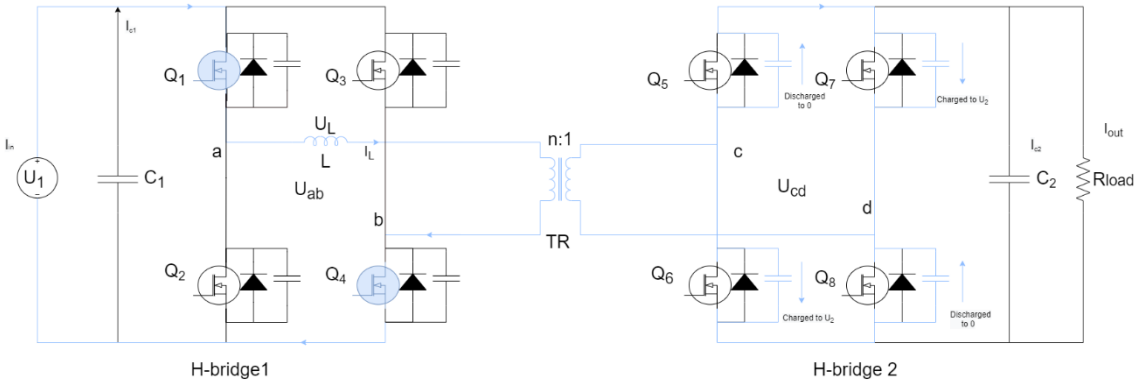

Figure 49 Charging and Discharging of the Parallel Capacitors

The same logic is followed for all the other time intervals transition when for example the transition to interval t_2-t_3 where the transition of the switches happens in the primary side. Q_1 and Q_4 are to be turned off and Q_2 and Q_3 to be turned on, whereas Q_5 and Q_8 still conduct. The voltage across Q_1, Q_4 is zero before switching off while Q_2 and Q_3 block the entire primary voltage. Right before Q_2 and Q_3 start conducting there is a dead time when all the switches in the primary side don't conduct and during this time the charging and discharging of the capacitors happens the same way as previously described. Right after the charging and discharging process is finished the diode D_2 and D_3 will conduct, still during this dead time, until the MOSFETS start conducting, until the dead time is finished. This process will once again provide zero voltage switching for Q_2 and Q_3 which lead to no switching losses.

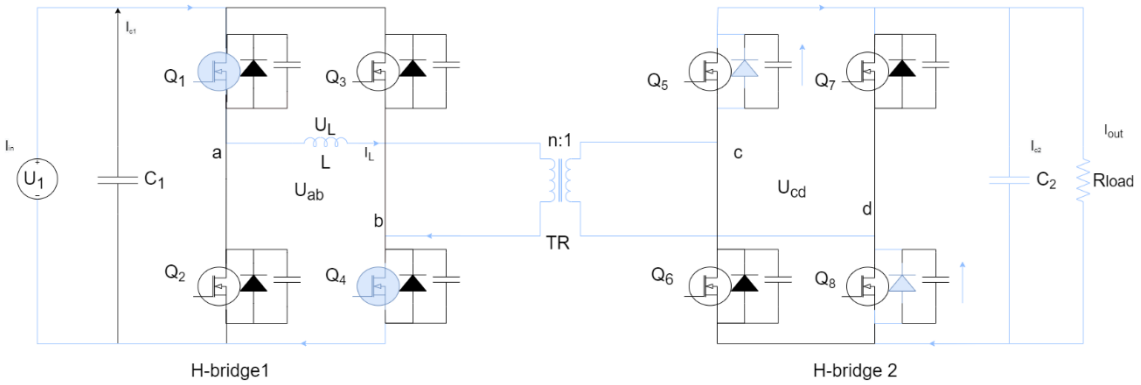

Figure 50 Diode Conduction Instance

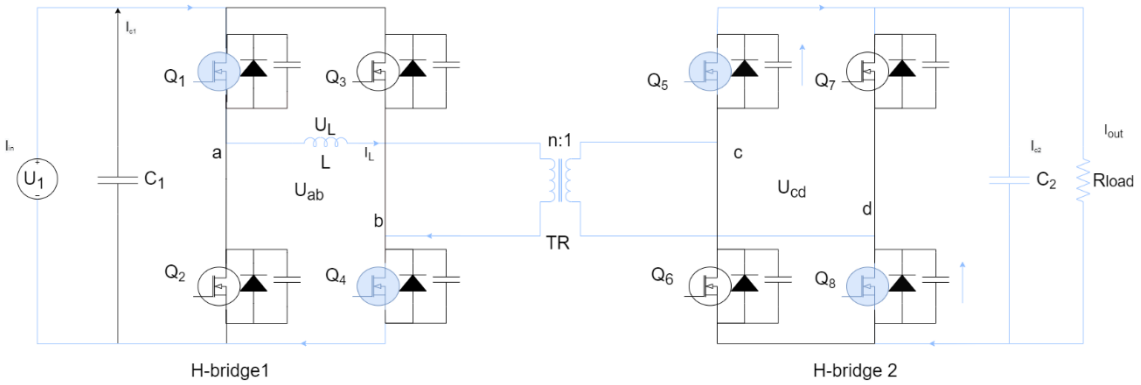

Figure 51 Turn on of Q_5 and Q_8

Since the operation of the DAB converter when the parasitic capacitors are present results in lower losses during turn-on and turn-off of the switches, they are highly applied. Yet, this model requires some conditions to be satisfied to ensure low switching losses. These conditions are closely related to the inductor current value and the dead time length, which in the previous analysis were assumed to be at the required values.

One of the conditions that have to be met in order to obtain ZVS in the DAB converter is that the inductor current has to be large enough to provide the charging and discharging of the parasitic capacitors when these parasitic capacitors are present. In this thesis the MOSFETs used for the DAB converter were chosen according to the current ratings where the body diode and a parasitic capacitance data is provided by the datasheet of this MOSFET. Therefore, the parasitic capacitance value will be constant and according to the data provided from the datasheet.

The other condition that should be met for the DAB converter to operate efficiently with ZVS is that of the dead time length. Previously this dead time was assumed to be long enough to charge and discharge the capacitors and to allow for the conduction of the diode. Hence, this dead time will be defined by referring to the data provided by the datasheet of the MOSFETs.

4.5 Inductor Current Requirements to Provide ZVS

To achieve ZVS, the frequency of resonance should be higher than the operating frequency. Therefore, the angular frequency for the parasitic capacitance and the inductor should be:

$$\omega = \frac{1}{\sqrt{L' C_S}} \qquad \textbf{4-15}$$

For the capacitors to be charged and discharged, the inductor current should be sufficient to provide this. The approach of finding this minimum inductor current value is presented in [21], from where the influence of the parasitic capacitance connected through the switching devices on this current is evident. This approach is presented in this thesis as well considering the primary H-bridge as reference. A representation of this bridge during the charging and the discharging time instant is presented in the Figure 52 below.

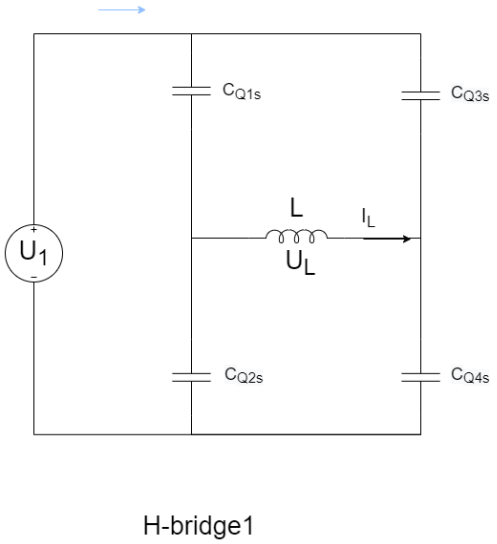

Figure 52 DAB Converter Circuit During Resonance, Primary H-Bridge.

By neglecting the losses and considering all the parallel capacitors to be equal, the inductor current will be divided in two parts to charge and discharge these components. This is presented by the following relation:

$$I_L = 2I_C \qquad \textbf{4-16}$$

where I_C is the current that flows though the capacitors:

$$I_C = I_{Q_n C_s} \qquad \textbf{4-17}$$

The inductor current is closely related to the energy stored in the inductor that has to be equal or larger to the energy delivered to charge and discharge the parasitic capacitors and the device output capacitances [21]. For this reason, a relation between the stated condition is expressed by:

$$\frac{1}{2} L I_{sw}^2 \geq E C_s \qquad \textbf{4-18}$$

$$\frac{1}{2}LI_{sw}^2 \geq K\frac{1}{2}C_sU_{dc}^2 \qquad \textbf{4-19}$$

Where K is the number of switches, I_{sw} is the inductor current peak value during switching and C_s is the parasitic capacitor.

It was mentioned before that the sign of the current is important in different time instances to allow for the body diode to conduct but even if this requirement is met, ZVS during turn on is not secured when the third step, diode conduction, is skipped resulting in switching losses.

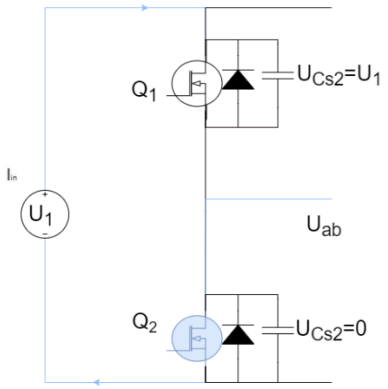

Figure 53 Primary Bridge Leg Circuit Representation, Before the Dead Time

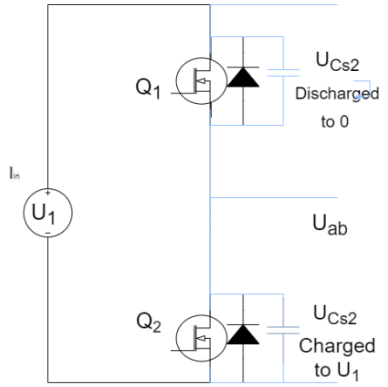

Figure 54 Primary Bridge Leg Circuit Representation, Just when the Dead Time Starts

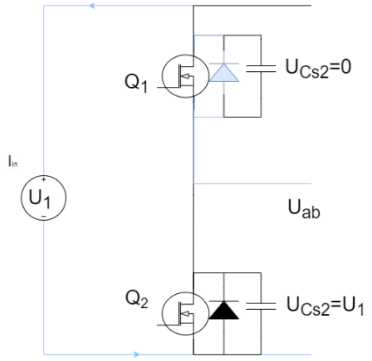

Figure 55 Primary Bridge Leg Circuit Representation, Diode Conduction Time

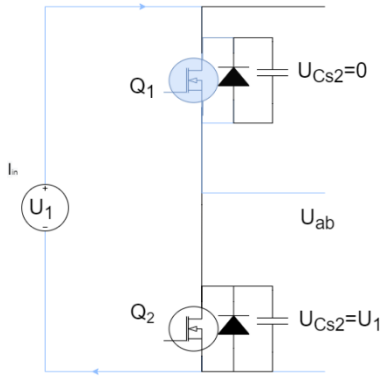

Figure 56 Primary Bridge Leg Circuit Representation, After the Dead Time

Therefore, other requirements have to be fulfilled such as the minimum inductor current. The parallel capacitors are not discharged to zero and charged up to input voltage if the magnitude of the inductor current is smaller than the minimum inductor current [3]. This minimum current will restrict the output current and voltage region which allows for soft switching operation[23]. From the above relation between energies, the minimum current required to charge and discharge the capacitors is derived[23]:

$$I_L = 2\sqrt{\frac{V_0 V_{in}}{\frac{L'}{C_S}}} \qquad \textbf{4-20}$$

If the inductor current is bigger or equal to this value during transition to turn on, ZVS is obtained. This though will restrict the output current and voltage region for soft switching operation due to the minimum current required during transition of the switches. This is also where the concept of boundary of ZVS or ZVS operating region comes[23].

The angular frequency of resonance is calculated and compared with the operating frequency where the resonance frequency results to be higher than the operating frequency which meets the requirement:

$$\omega = \frac{1}{\sqrt{L'C_S}} = \frac{1}{\sqrt{24.5x10^{-6}x230x10^{-12}}} = 13321497.26(\frac{rad}{s}) \quad \textbf{4-21}$$

$$f_r = 2120182\ (Hz) \quad \textbf{4-22}$$

$$f_r > f \quad \textbf{4-23}$$

where L' is obtained from the DAB Model parameters and C_S from the MOSFET datasheet.

The minimum inductor current will be calculated for different phase shift values where the same approach as in section 4.4 is chosen where the phase shift values used for this study are regarding the ZVS Boundary. Worth mentioning is that for D=0.5, k=1 so the I_L minimum value is not required to be specified since the DAB converter will operate in ZVS region as long as k=1 regardless of other parameters.

The minimum inductor current value for a phase shift D=0.19 is estimated as followed:

$$I_L = 2\sqrt{\frac{V_0 V_{in}}{\frac{L'}{C_S}}} = 2\sqrt{\frac{700x430.92}{\frac{24.5x10^{-6}}{230x10^{-12}}}} = 3.3655\ (A) \quad \textbf{4-24}$$

Other phase shift values and the corresponding minimum inductor are presented in the table below. For a phase shift value of D=0.1, the minimum inductor current is defined but due to the previous condition mentioned in section 4.4, ZVS will not be provided in the Secondary Bridge for this operating region.

Phase shift	I_{Lmin}(A)
D=0.1	2.5737
D=0.19	3.3655
D=0.3	3.9314

Table 12 Minimum Inductor Current Value

These inductor values are very low compared to the calculated inductor values for different phase shift values presented in in the tables of the estimated losses. This results in the inductor current being sufficient to charge and discharge the parasitic capacitors for the varying phase shift value of the DAB converter used in this thesis. The reason why the inductor current minimum value is so small is because of the capacitors value provided from the datasheet.

In Figure 57, the varying phase shift and its relation with the minimum inductor value is presented form where, an increase in inductor minimum current is noted for the increase in phase shift value. Still this increase is not drastic emphasizing so that the DAB converter used in this thesis, fulfills the minimum inductor current requirement for all phase shift vales in accordance to the chosen switching device.

The same figure also depicts the relation of the inductor current with the parasitic capacitor value from where, in general application, it is evident that for a higher C_s value, a higher inductor minimum current value is required for a varying phase shift value and logically, for a lower C_s a lower minimum current value is required.

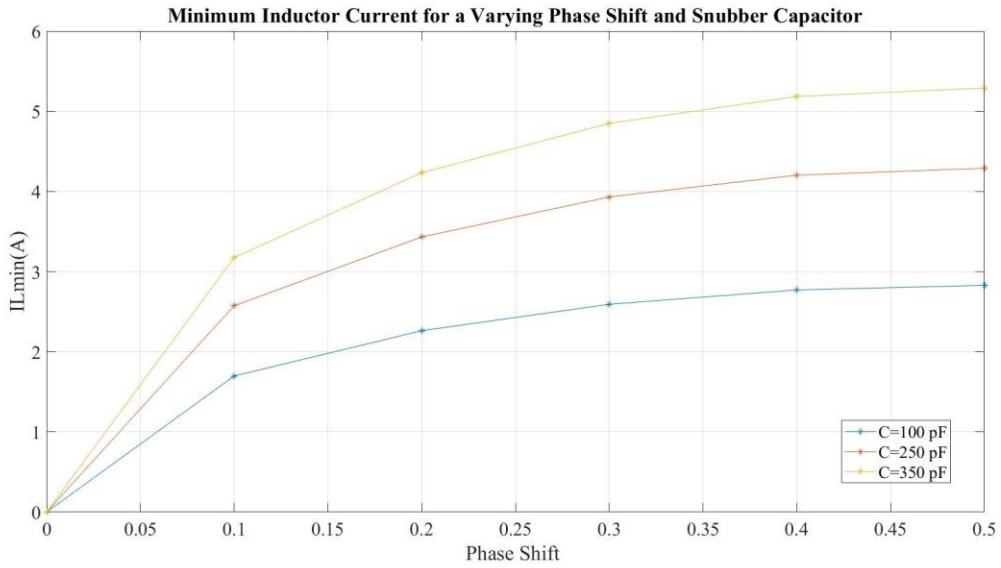

Figure 57 Minimum Inductor Current for a Varying Phase Shift and Parasitic Capacitor

4.6 Dead Time Effect on ZVS Operation

The dead time length plays a major role in ZVS operation where in section 4.4.2 the dead time was assumed to be longer than the resonance time, charging and discharging of the capacitors. In this section the effect of the dead time on ZVS will be further discussed.

The ZVS boundary when having a parasitic capacitor will be narrower since these capacitances require a minimum charge provided by I_L. The dead time has to be long enough for the process of charging and discharging to happen. If this dead time is too short compared to resonance end time, the resonance will be uncompleted which will result in large currents during turn on of the switch, then a partial ZVS or hard switching will happen. Therefore, the minimum charging-discharging time has to be set by assuming that I_{sw} and V_{dc} are constant during the switching transition. So the minimum resonance time is[4]:

$$t_{A\,min} = \frac{Q}{I_{sw}} = \frac{2V_{dc}C_S}{I_{sw}} \qquad \textbf{4-25}$$

$$t_{dead\ time} \geq t_{A\,min} \qquad \textbf{4-26}$$

The capacitor charging time is calculated in the estimation of losses where t_A is presented as the charging and discharging time and t_B as the body diode conduction time. This is one condition for the dead time length to achieve ZVS which is presented by the relation in 4-26. If the length is not met than it can cause hard switching or partial ZVS [4][12].

If the dead time is longer than the resonance time, the leakage current crosses the zero before the switches are turned on and the voltage changes its polarity, resulting in reverse charge and discharge. This will also result in partial ZVS or hard switching. Therefore, the following condition should also be met:

$$t_{dead\ time} < t_1 \qquad \textbf{4-27}$$

The conditions for the dead time length and the resonance length are to be defined. Results from previous sections are used in these calculations as well as data from the datasheet of the switching devices. The minimum charging and discharging time is estimated by using equation 4-25 and data provided from the datasheet:

$$\boldsymbol{t_{A\,min} = \frac{Q}{I_{sw}} = \frac{2V_{dc}C_S}{I_{sw}} = 2\frac{700x230x10^{-12}}{71.4286} = 4.5x10^{-9}(s)} \qquad \textbf{4-28}$$

The dead time is found in section 3.3.1.1 from $t_{d(off)} + t_{fall} = 78\,(ns)$,where $t_{d(off)}$is the turn off delay time and t_{fall} is the fall time, but due to safety margin, this dead time is considered 150ns. From the results obtained, the mentioned condition is satisfied where the total dead time is longer than the charging and discharging of the capacitors time.

$$\boldsymbol{75x10^{-9}(s) > 4.5x10^{-9}(s)} \qquad \textbf{4-29}$$

From 4-26 the dead time has to be smaller than t_1 which corresponds to:

$$\boldsymbol{t_1 = \frac{DT_s}{2} = 9.5x10^{-7}(s)} \qquad \textbf{4-30}$$

$$\boldsymbol{15x10^{-8}(s) < 9.5x10^{-7}(s)} \qquad \textbf{4-31}$$

Satisfying so this condition as well for ZVS operation of the DAB converter for when parasitic capacitors are present.

4.7 ZVS Boundary

Previously the ZVS boundary was mentioned where it was defined in correspondence with the phase shift value. In this section this ZVS Boundary is to be built and analyzed with respect to the ZVS operation of the primary and secondary H-bridge of the DAB converter.

For this study, the effect of the parasitic capacitors on the ZVS boundary will be neglected for simplicity.

The ZVS boundary is presented in terms of a varying phase shift value and gain $G = \frac{U_2}{U_1}$. The plot that depicts this boundary is built by using MATLAB where the written script is presented in Appendices and the generated plot is presented in Figure 58. By interpreting the plot, it is evident that for a gain equal to 1, G=1, which also corresponds to voltage convention ratio k=1, ZVS is provided for all phase shift values since the converter will operate within the ZVS region. However, unity is only achieved for when D=0.5 for the DAB converter model used in this thesis.

The ZVS operation area is also noted to widen with the increase in the phase shift value and to be quite narrow for lower phase shift values. In the low phase shift region, it is observed that ZVS is most likely not achieved for the DAB converter since the ZVS operating region is very small.

The ZVS boundary of the DAB converter is presented by the primary and secondary ZVS boundary where the primary H-bridge boundary is defined by G>1 and secondary H-bridge boundary by G<1. In section 4.3 it was observed that the primary side in a DAB converter did not loses its ZVS capability in Buck mode operation whereas the secondary side did.

This can also be noted from the plot below where the Primary Side will lose its ZVS capability for the Boost mode operation and the secondary side for its Buck mode.

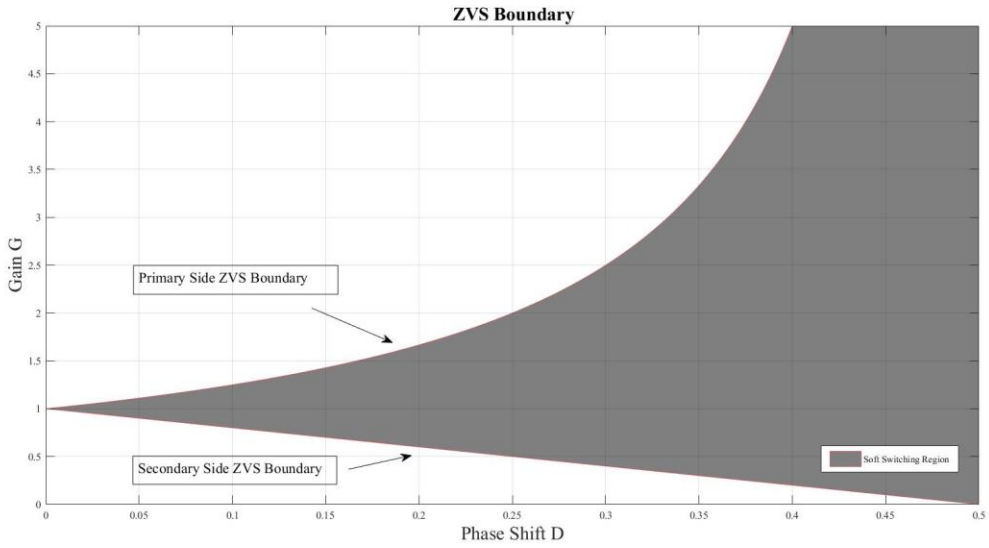

Figure 58 ZVS Boundary

In the analytical approach of testing the ZVS operation of the DAB converter, different phase shift values were chosen in correspondence to the ZVS boundary where D=0.19 phase shift value was found to be operating at ZVS boundary, D=0.3 to be operating in ZVS region and D=0.1 to be operating out of the ZVS region. These values and their ZVS operation are to be observed by the plots below.

A phase shift D=0.19 corresponds to a gain G=0.62, which observed from the plot corresponds to the DAB converter operating at the ZVS boundary Figure 59, proving so that the secondary side of the converter will operate at ZVS since the primary side does not lose its ZVS capability.

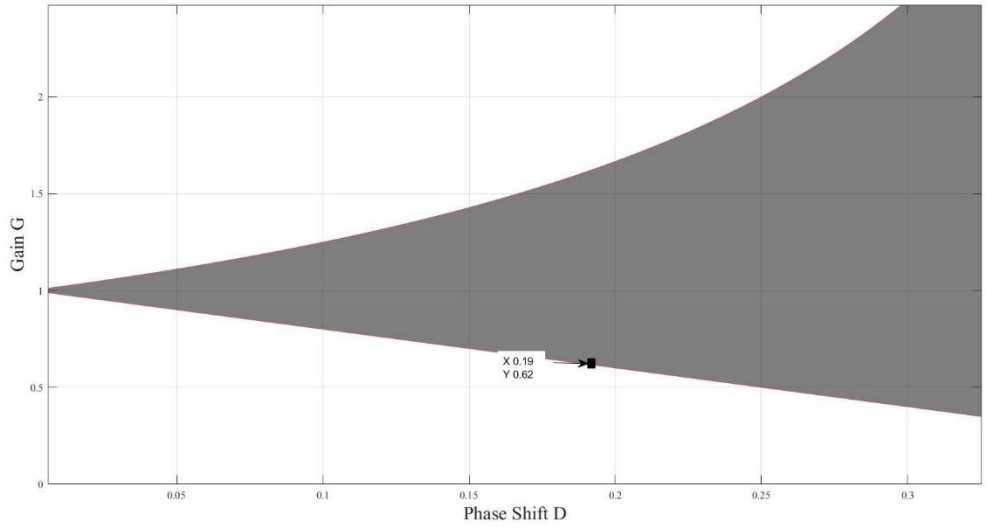

Figure 59 DAB Converter ZVS Boundary, D=0.19.

For the second phase shift value D=0.3 Figure 60, the DAB converter should operate in the ZVS region both for primary H-bridge and secondary H-bridge. This phase shift value has a gain of G=0.84 and from the plot below it can be seen that the DAB converter will operate in the ZVS region allowing for ZVS switching on both bridges.

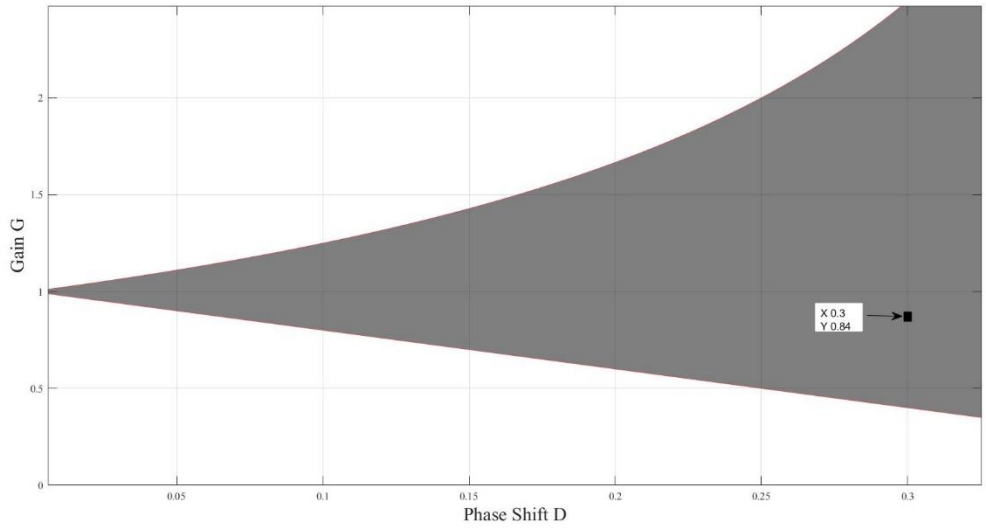

Figure 60 DAB Converter ZVS Boundary, D=0.3.

The last case that is considered when defining the ZVS operation of the converter is that for when the phase shift D=0.1 which corresponds to a gain G=0.36 Figure 61. According to the analytical approach, the converter loses its ZVS capability on the secondary H-bridge in this region. From the plot below it is also noticed that the converter operates out of the ZVS boundary on the secondary side resulting so in no ZVS operation of the DAB converter for this phase shift value. Worth mentioning is that this is the case when the DAB converter operates in Buck Mode.

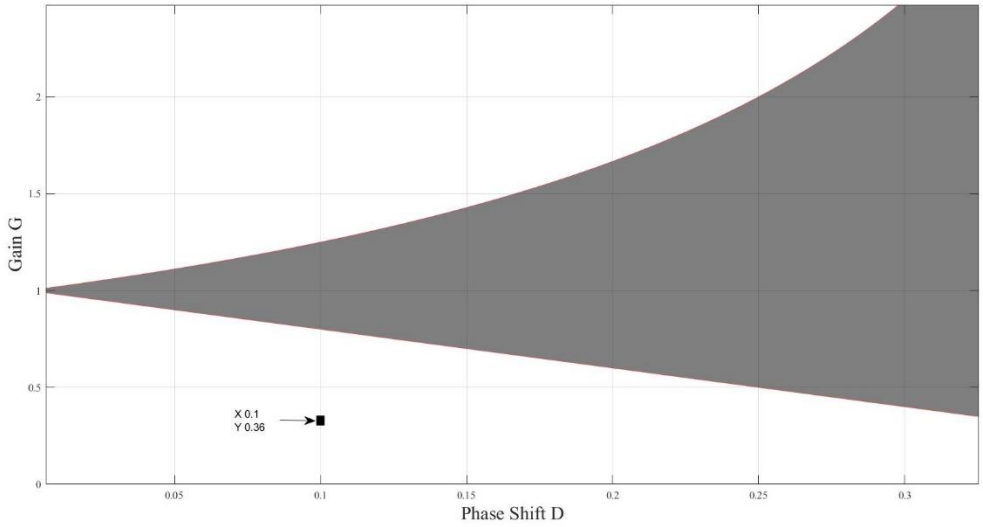

Figure 61 DAB Converter ZVS Boundary, D=0.1.

From the above observation it is noted that the ZVS operating region expands for an increase in phase shift value, both for Buck and Boost operation of the DAB converter. This brings interest on the high phase shift region of the converter but, as observed previously, the high phase shift region provided more losses in spite of its ZVS capability.

This concludes the basis of ZVS operation of the DAB converter where there are studies and research in expanding the ZVS boundary by adding new components or simply by modifying the modulation scheme.

4.8 Discussions

This chapter studied the ZVS operation of the DAB converter and defined the condition for the ZVS operation of the converter. It was noticed that the ZVS operation was closely related to the phase shift value and other parameters such as dead time and inductor current value.

For the switches to turn on at zero voltage, the body diodes had to conduct which required for the current to flow from source to drain. This condition was defined and checked for two operating scenarios of the DAB converter by presenting the working principle of the converter for these two cases. From these cases it was noticed that for when $\frac{k-1}{2k} > D$, the diode did not conduct on the secondary bridge resulting in hard switching of the secondary side switches whereas for when the relation was not true, all the switches in both bridges would turn on at zero voltage. This created the relation of the diode conduction with the zero-crossing time instant and the relation between the phase shift and the voltage convention ration which were defined as the main conditions that would allow for ZVS of both bridges of the converter. The mentioned conditions were tested for three different phase shift values where the ZVS operation was identified for a phase shift D=0.19 up to D=0.5 since this thesis only considered the phase shift range $0 \leq D \leq 0.5$.

The conduction of the diode itself was not enough for the converter to operate at ZVS. Therefore, other conditions for ZVS operation were defined. The scenario for when parasitic capacitors were added in parallel to the MOSFETs was also considered which would allow for lower switching losses due to their property of easing turn off and turn on losses. This approach resulted in additional requirements for the DAB converter to operate at ZVS region. The dead time had to be sufficient to allow for the conduction of the diode and for when the parasitic capacitor was added, it had to be long enough to allow for charging and discharging of these capacitors provided by the inductor current.

The dead time was defined by using data provided by the datasheet of the MOSFETs and was proven to be long enough for the DAB converter model used in this thesis to allow for ZVS. The inductor current value also had a major focus in this chapter where the minimum inductor current value required for the charging and discharging of the capacitors was calculated for different phase shift values which were noted to be very low compared to the actual inductor values that this DAB model provided. This allowed for a complete charge and discharge of the parasitic capacitors. The effect that the parasitic capacitors value had on this minimum inductor current was also observed where an increase of the capacitor value resulted in higher minimum inductor values.

For when the converter was operating at a low phase shift region it was noticed that the secondary bridge lost its ZVS capability whereas the primary bridge was still able to operate at ZVS when in Buck mode, highlighting so the merit of the DAB converter and its ZVS property. This low phase shift operating region was later identified by ZVS boundary.

The boundary phase shift value calculated was D=0.19 where for the DAB converter operating at this value, the primary and secondary bridges operated at ZVS and for phase shift values bigger than this, the converter would still operate in ZVS region. Whereas for a phase shift smaller than the aforementioned value, the secondary H-bridge would lose its ZVS capability resulting in hard switching of the switches. Cases when D=0.1 and D=0.3 were considered and presented in the plot generated for the ZVS boundary which corresponded to the described occasions.

An important outcome of this study was also for when G=1, where from the generated ZVS boundary it is evident that for when the input and output voltage are equal, ZVS is achieved independent on the varying phase shift. This though is not achieved practically since for the DAB converter used in this thesis to operate at unity using the phase shift modulation scheme, the phase shift should be D=0.5.

This study presented ZVS operation of the DAB converter for different scenarios and conditions which allowed to back the low switching losses attained in Chapter 3. The conditions specified helped to identify the ZVS operation region of the DAB converter also to address the operating regions when the ZVS is not obtained. By defining these areas and the parameters that affect it, this chapter created a base for further research on expanding ZVS operating region.

5 Conclusion and Future Work

5.1 Conclusion

Throughout this thesis, important studies were conducted where discussions based on the observations were presented in each of the corresponding chapters. This will cover the most important observations and findings of the thesis.

In Chapter 3, two approaches for calculating the losses were presented. Both approaches were found to be close to each other where the difference was mainly due to the assumptions made in either of the approaches.

For the analytical approach it was observed that the conduction losses were directly related to the RMS current and the drain to source on resistance 3-12, 3-13. Higher RMS current would result in higher conduction losses. An important observation was for the ZVS boundary operation of the converter, for phase shift D=0.19 region, where the lowest RMS current was achieved and as a result, the lowest conduction losses which contributed to lower total losses.

The switching losses were calculated using the datasheet where the obtained results were expected not to be accurate due to the approximations made when extracting the required data from the two plots of the MOSFET datasheet. The secondary H-bridge switching losses for D=0.2 was noticed to be very low and this sparked the further investigation of this operating region of the converter in the simulation approach. Overall, it was is concluded that this approach is accurate and an efficient way of estimating the losses without the help of any software-based results. This method allowed for important observation which were later observed and discussed in the simulation approach.

The simulation results were more accurate since the varying R_{DSon} and output voltage ripple were considered. The data from the MOSFET chosen were accurately implemented into the DAB model which allowed for accurate results. This methodology provided scope for important observation which were mentioned in the discussions in the related chapter. The difference in losses in primary and secondary bridge were spotted. This difference was not present in the analytical approach since the conduction losses, were dependent on the RMS current flowing though the switches. These currents in the analytical approach were equal and so resulting in equal conduction losses for both bridges. For the simulation approach, the method PLECS uses is by considering the voltage current characteristic. As a result, it considered the ripples on the output voltage which led had an effect on the losses results. This was the reason why the difference between conduction losses in both bridges was only evident in the simulation approach.

The ZCS capability during turn off of the switches of the DAB converter on the secondary bridge for the ZVS boundary operation D=0. 19 was observed. This resulted in zero switching losses of the secondary H-bridge switches contributing to the low total losses of the DAB converter operating at phase shift D=0.19. The junction temperature effect on the losses was also observed in the simulation approach where higher junction

temperatures were present for high phase shift values which contributed to higher losses since it affects the R_{DSon}resiatnce value. By the assumption in the analytical approach of the junction temperature to be $45℃$, R_{DSon} value was obtained. The junction temperature was later calculated and found to be different from the assumed value which contributes to the difference between the results obtained from the simulation and analytical approach losses.

From the studies conducted in Chapter 3, the difference in results was spotted where the analytical results were slightly higher than the simulation results. The reasoning behind this difference was mainly also due to the inaccurate method of extracting data from the datasheet in the analytical approach. The aforementioned method of estimating the conduction losses in the two approaches also effected the difference between the results. From the simulation approach it was concluded that it allowed for a broader observation of the DAB converter operation but at the same time required more time since the DAB model had to be built in a simulation software window together with its corresponding parameters. The broad tools provided from the PLECS software were used for this study which concludes that the PELCS software does provide the necessary tools for estimating the losses in an accurate way.

The ZVS operation of the converter dealt with the conditions for realizing ZVS of the switches in the DAB converter. The conduction of the diode, the dead time length and the minimum inductor current value were among the most important conditions for realizing ZVS. The minimum inductor current was found to be very small for the DAB model used in this thesis and as a result, was able to charge and discharge the parasitic capacitors. The dead time used for this model was also found to be long enough to allow for this charging and discharging of the parasitic capacitors and to allow for diode conduction.

The ZVS boundary was set and the operation of the DAB converter in, at and out of this operating region were analytically tested. From this study it was concluded that the DAB model used in this thesis, when operating in Buck mode, does not lose its ZVS capability on the primary side, when operating in Buck mode, independent on the phase shift vale. Whereas the secondary bridge is dependent on the varying phase shift value where for the low phase shift operating region it loses its ZVS capability. Another important note in this chapter was that DAB converter did not lose its ZVS capability for when k=1 or G=1 which corresponds to the input voltage equal to the input voltage. From this approach in this part of the thesis it was concluded that the ZVS operation of the DAB converter directly affected the switching losses and therefore, expanding this ZVS operating range would allow for lower switching losses which contributes to lower total losses that the DAB converter generates.

All the aforementioned studies highlight the prominent properties of the DAB converter, low losses and ZVS capability. The DAB model used in this thesis with its' parameters allowed for a good study of the DAB converter operation and provided important observations which can be used as a starting point for other DAB models.

5.2 Future Work

This thesis considered a Loss DAB model where the switching devices contributed to the losses. For future work, the losses caused by the transformer and other components should be considered. For this the design of the transformer and its material properties and dimension, copper and coil losses, will have to be considered in order to estimate its' losses. By considering the losses provided by all the components in the DAB converter, an analysis of the impact that the losses have on the performance of the converter can be performed.

The estimation of the losses considering the aforementioned components can be conducted both analytically as well as through simulations. This would allow to further explore the tools that the PLECS software provides as well as its limitations. This estimation of the losses should also be conducted experimentally as well which would provide more data on testing the accuracy of the results obtained from the mentioned approaches.

The DAB model used in this thesis studied only the Buck operation of the converter and therefore, the Boost operation of the converter should also be studied in terms of the analysis conducted in this thesis. The antiparallel diode presence was briefly mentioned together with its positive effect on the total efficiency of the DAB converter but was not studied. In future work this antiparallel diode should be considered and its effect on the total losses should be observed.

Ways on optimizing the analytical approach of calculating the losses can be the next step in future work with focus on the switching losses. Since the method used in this thesis showed that the obtained results have a difference with the simulation results due to the approximations made when extracting the values, optimizing this approach is of big interest.

The DAB converter topology used in this thesis was a traditional topology. Using the same approach as in this thesis on other prominent and highly applied topologies of the DAB is also an aim for future work. This will provide data for comparing the topologies and differentiating their use in different applications.

The ZVS Capability of the converter was studied in an analytical approach since the PLECS software did not provide the required tools to observe this operation in further details. In future work, LTspice software should be used for further study of the operation of the DAB converter under ZVS conditions. The parameters of the converter should be varied and the effect that they have on the ZVS operation of the DAB converter can be an important aspect of future work. This can provide more data in regards to expanding the ZVS operating region. Many papers present methods and approaches on expanding the ZVS operating region by additional components. These methods can be further studied and applied to the DAB converter model used in this thesis.

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Appendices

Appendix 1: PLECS Plots

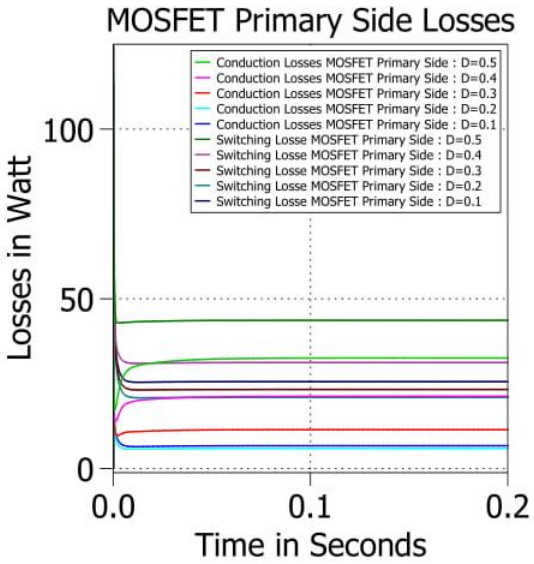
Appendix 2: MATLAB Plots

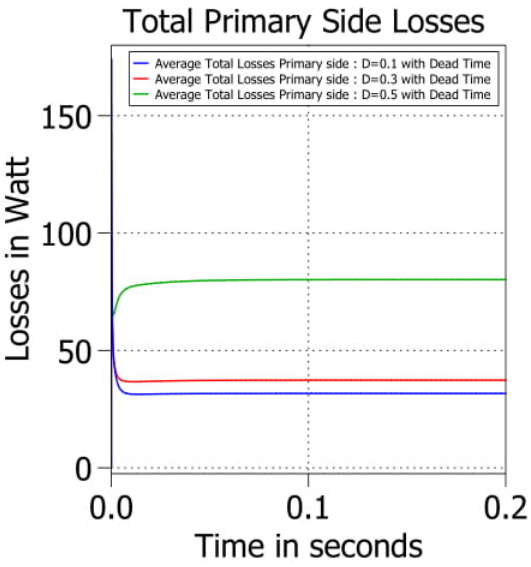
Appendix 3: MOSFET Datasheet Plots

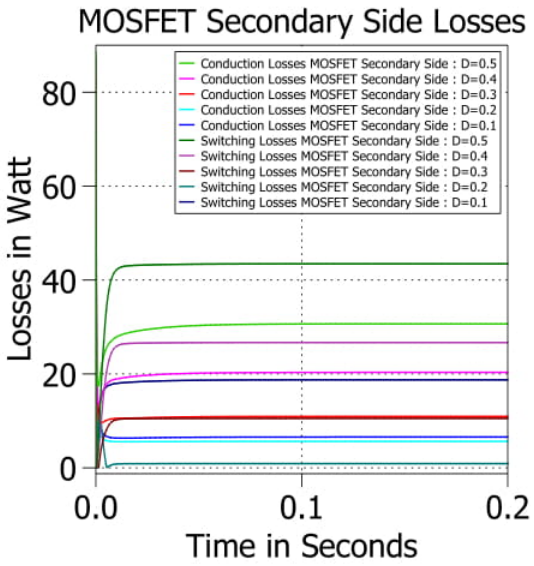
Appendix 4: Scripts

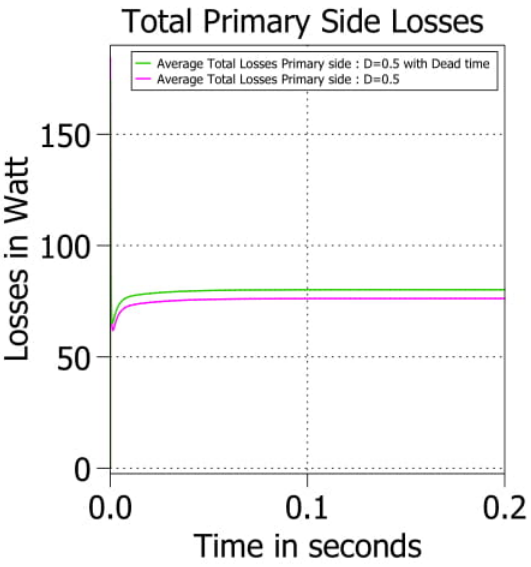
Appendix 5: Tables

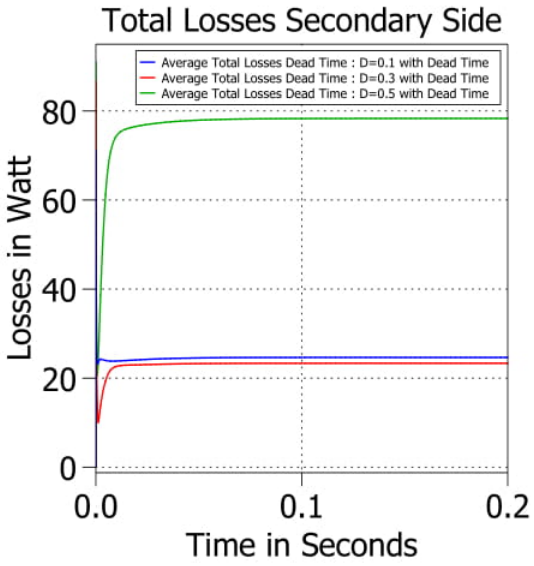
Appendix 1: PLECS Plots

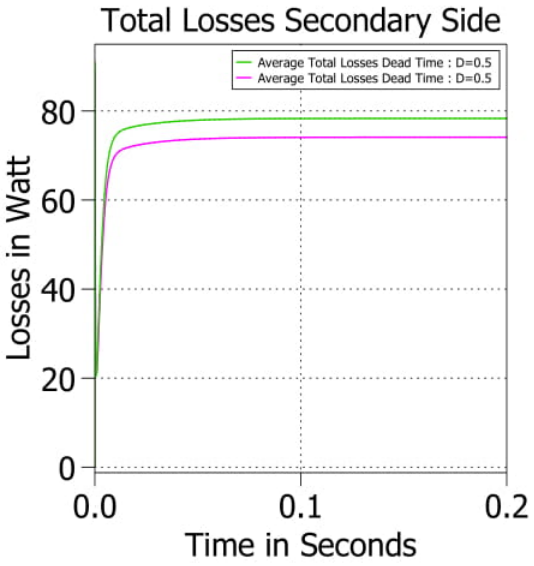


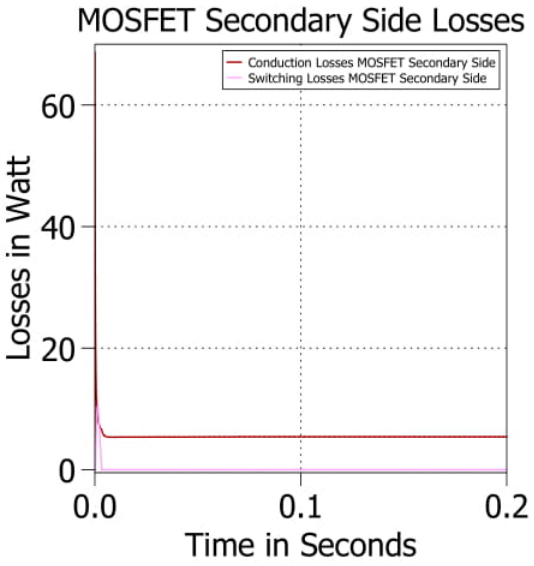


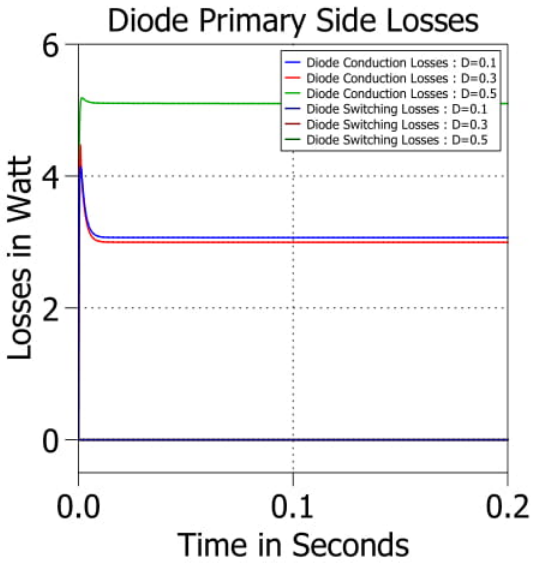


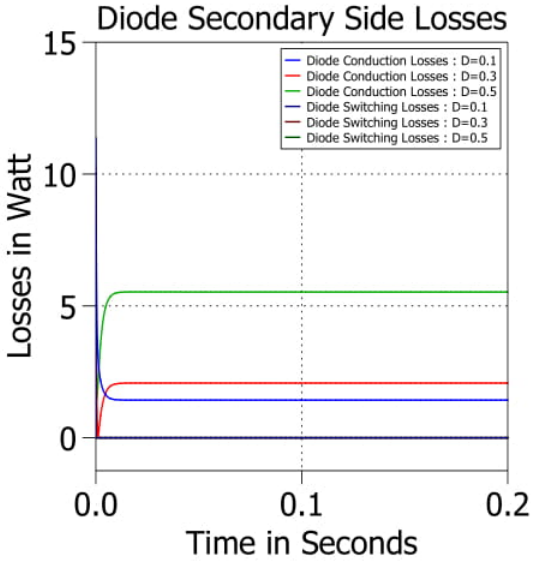



Total Losses Secondary Side
Average Total Losses Dead Time : D=0.1 with Dead Time
Average Total Losses Dead Time : D=0.3 with Dead Time
Average Total Losses Dead Time : D=0.5 with Dead Time
Losses in Watt
0
20
40
60
80
0.0
0.1
0.2
Time in Seconds

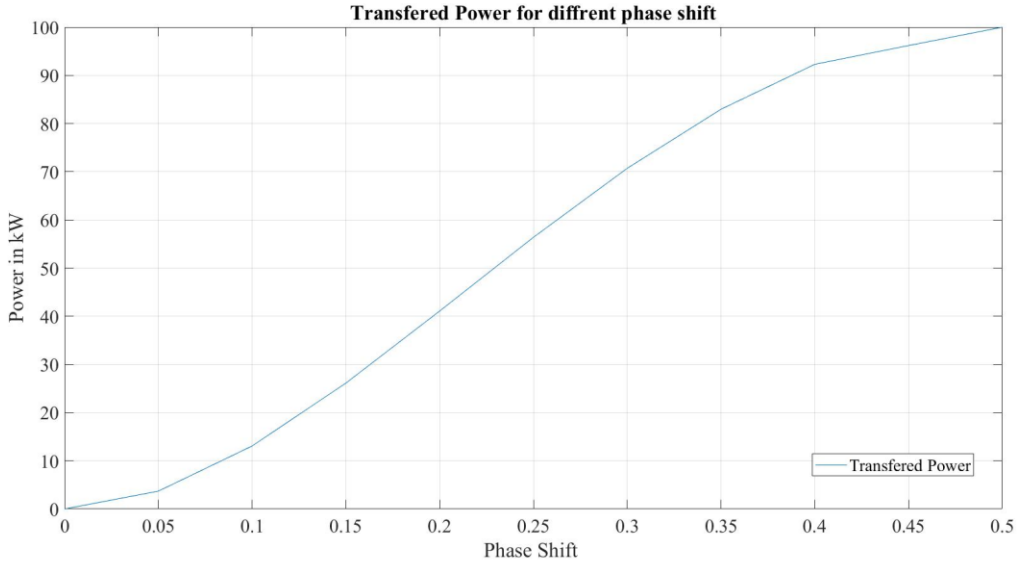

Total Losses Secondary Side
Average Total Losses Dead Time : D=0.5
Average Total Losses Dead Time : D=0.5
Losses in Watt
0
20
40
60
80
0.0
0.1
0.2
Time in Seconds

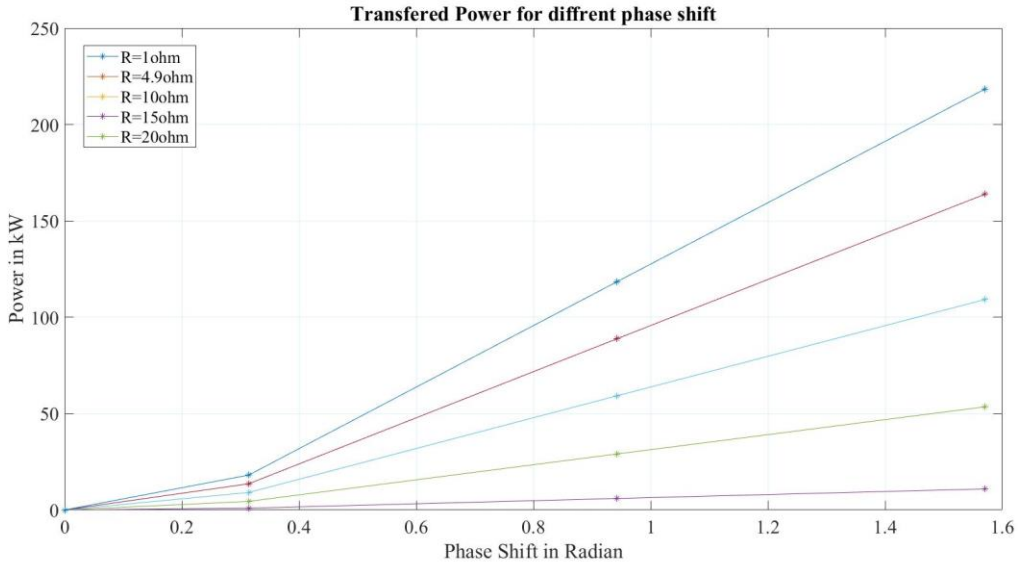

MOSFET Secondary Side Losses
Conduction Losses MOSFET Secondary Side
Switching Losses MOSFET Secondary Side
Losses in Watt
0
20
40
60
0.0
0.1
0.2
Time in Seconds


Diode Primary Side Losses
Diode Conduction Losses : D=0.1
Diode Conduction Losses : D=0.3
Diode Conduction Losses : D=0.5
Diode Switching Losses : D=0.1
Diode Switching Losses : D=0.3
Diode Switching Losses : D=0.5
Losses in Watt
0
2
4
6
0.0
0.1
0.2
Time in Seconds

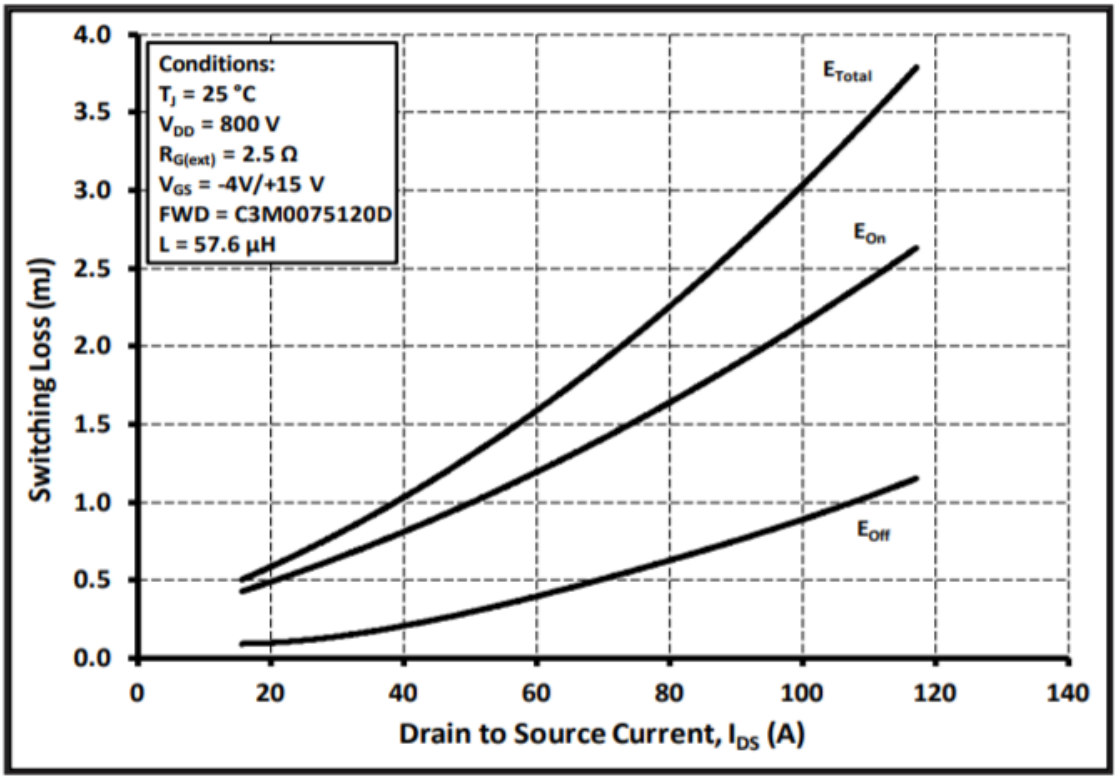

Diode Secondary Side Losses
Diode Conduction Losses : D=0.1
Diode Conduction Losses : D=0.3
Diode Conduction Losses : D=0.5
Diode Switching Losses : D=0.1
Diode Switching Losses : D=0.3
Diode Switching Losses : D=0.5
Losses in Watt
0
5
10
15
0.0
0.1
0.2
Time in Seconds

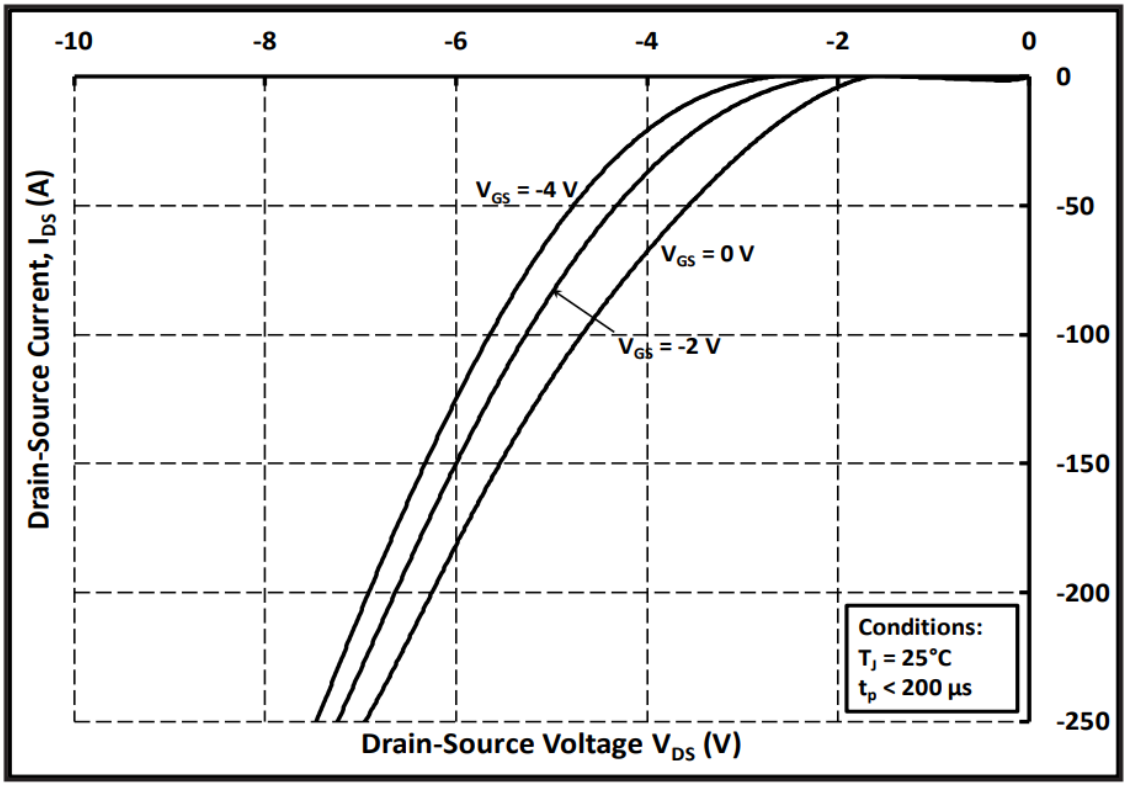
Appendix 2: MATLAB Plots

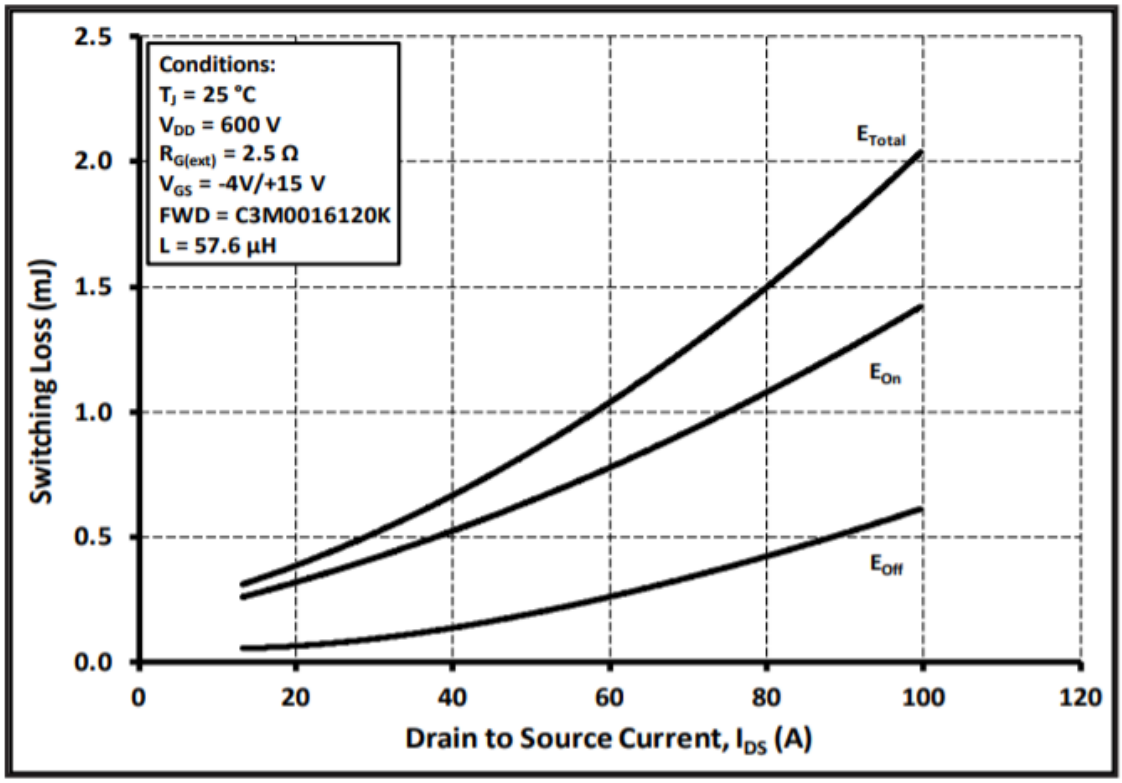


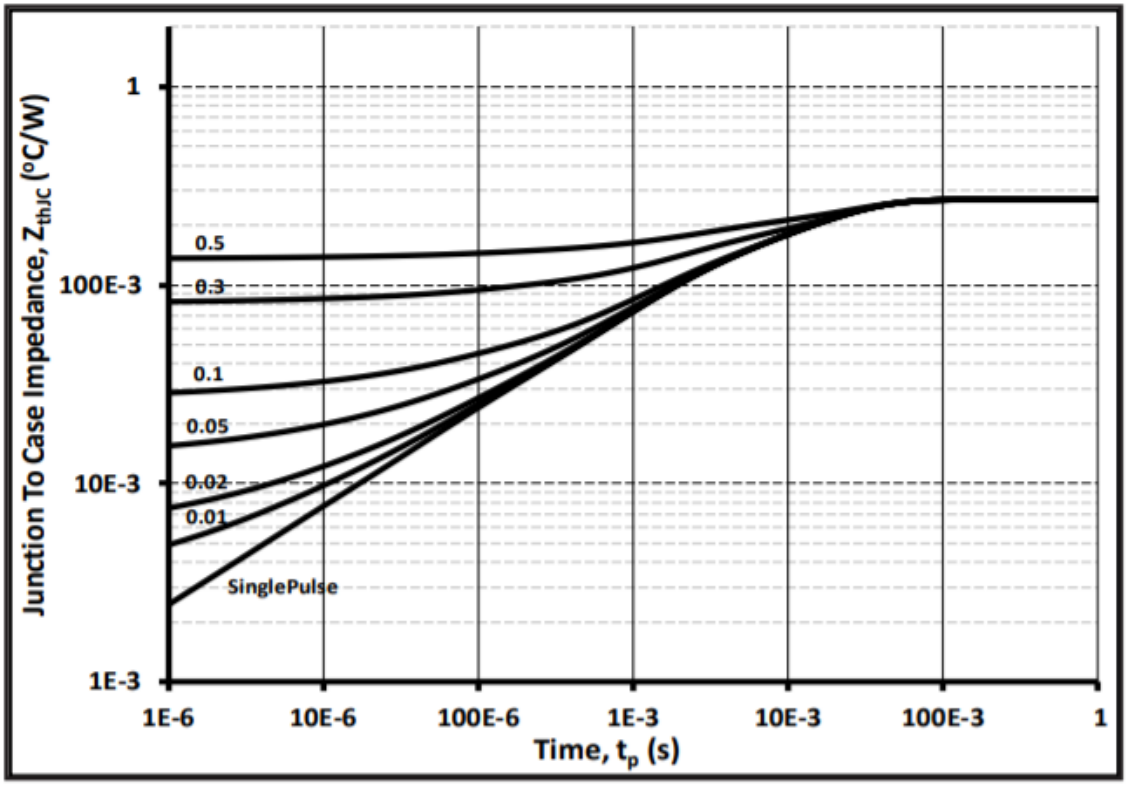


Appendix 3: MOSFET Datasheet Plots






Conditions:
T_J = 25 °C
V_{DD} = 600 V
$R_{G(ext)}$ = 2.5 Ω
V_{GS} = -4V/+15 V
FWD = C3M0016120K
L = 57.6 µH
E_{Total}
E_{On}
E_{Off}
Switching Loss (mJ)
Drain to Source Current, I_{DS} (A)
2.5
2.0
1.5
1.0
0.5
0.0
0
20
40
60
80
100
120


Junction To Case Impedance, Z_{thJC} (°C/W)
Time, t_p (s)
1
100E-3
10E-3
1E-3
0.5
0.3
0.1
0.05
0.02
0.01
SinglePulse
1E-6
10E-6
100E-6
1E-3
10E-3
100E-3
1

Appendix 4: Scripts

- **PLECS Initialization Script**

```
V_dc=700;
R1= 19.6;
L1=24.5e-6;
C2=100e-6;
phaseshift=(1/100e3)*0.5*0.5;
Turn_on_delay=1.5e-7;
Rth=0.001;
Averaging_time=1e-5;
```

- **Conduction Losses Script**

```
u1=700;
Rl=19.6;
fs=100000;
T=1/fs;
L=24.5e-6
D=0.5;
P=(u1^2*Rl)/(2*fs*L)^2*((D*(1-D))^2)
u2=(P*Rl)^(1/2)
k=u1/u2
Rq=18.5e-3;
uF=4.1;
ILrms= ((u2*T)*(-3*(8*(D^3)*k-12*(D^2)*k-k^2+2*k-
1))^(1/2))/(12*L)
IQrms=ILrms/2^(1/2)
ILpeak= (u2/(4*L*fs))*(2*D+k-1)
tA=2*((u1*230e-12)/ILpeak)
tB=(1.5*(10^-7)-tA)
Pcond_prim=4*Rq*IQrms^2
Pcond_sec=4*Rq*IQrms^2
Pcond_deadtime=8*uF*ILpeak*(tB/T)
Total_Losses=Pcond_prim+Pcond_sec+Pcond_deadtime
```

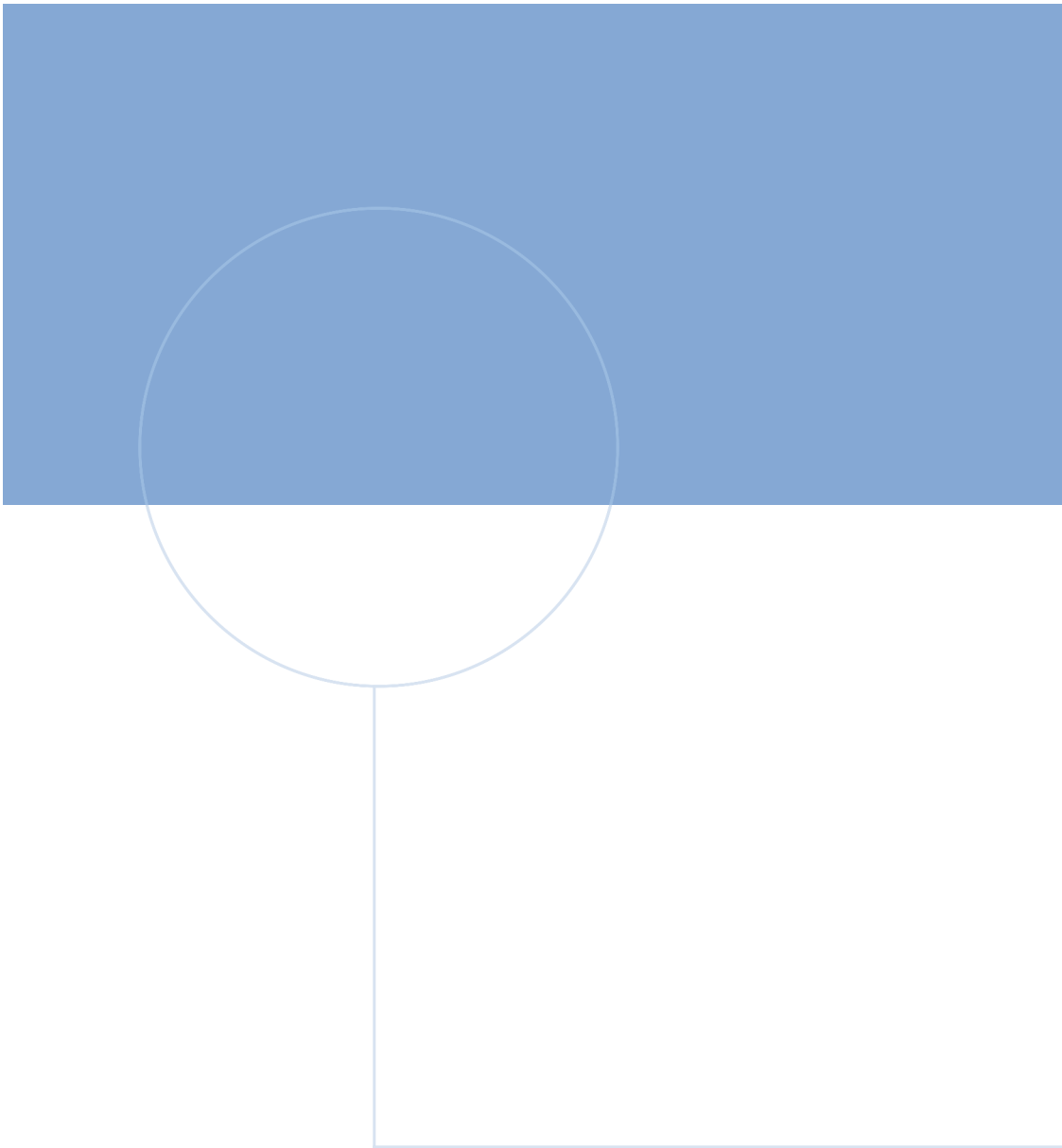
- **ZVS Boundary Script**

```
t=0.0001;
D=0:t:(0.5-t)
G1=1-2*D
G2=1./(1-2*D)
[ph,msg]=jbfill(D,G2,G1,[0 0 0],[1 0 0],0,0.5)
    grid on
    ylim([0,5])
```

Appendix 5: Tables

<table>
<tr><th colspan="5">SINGLE STAGE TOPOLOGIES</th></tr>
<tr><td>Converters with low number of switches</td><td colspan="2">Dual bridge converters without Resonant Network</td><td colspan="2">Resonant Dual Bridge Converters</td></tr>
<tr><td>Flyback, Forward, Forward-Flyback Cuk converter topologies.</td><td>Two Voltage sourced ports</td><td>Voltage and Current sourced ports</td><td>Two Voltage sourced ports</td><td>Voltage and Current sourced ports</td></tr>
<tr><td>(+) Simple circuit structure</td><td colspan="2">(+) More effective converter utilization</td><td colspan="2">(+) Increased capabilities regarding the utilization of the semiconducting switches</td></tr>
<tr><td>(+) Low number of switches</td><td colspan="2">(+) Low switching losses for the semiconducting switches</td><td colspan="2">(+) Low switching losses</td></tr>
<tr><td>(-) Ineffective transformer and switch utilization</td><td colspan="2">(+) High power is feasible</td><td colspan="2">(-) Higher converter complexity</td></tr>
<tr><td></td><td colspan="2"></td><td colspan="2">(-) Additional required power components</td></tr>
</table>

DAB TOPOLOGIES	
Three-Phase	**Single-Phase**
(+) Low device stress	(+) The low number of passive components
(+) Reduced capacitor ripple current	(+) Evenly shared current between the switches
(-) High number of active components	(+) Soft switching properties
(-) High conduction and switching losses	(+) High power density
(-)Design of 3-phase Transformer complexity	(+) Low grade of difficulty for Transformer design



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Norwegian University of
Science and Technology