Masteroppgave

NTNU
Norges teknisk-naturvitenskapelige universitet
Fakultet for informasjonsteknologi og elektroteknikk
Institutt for elektroniske systemer

Benjamin D. Askelund

28nm On-Chip Ultra Low Power Switched Capacitor Buck Voltage Regulator for use in Wireless Sensor Nodes and IoT Applications

Masteroppgave i Electronics Systems Design and Innovation
Veileder: Trond Ytterdal
Medveileder: Pål Øyvind Reichelt

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PREFACE

The presented work is the result of the final project of the TFE4940 Master of Science at Electronics Systems Design and Innovation (ELSYS), as part of the Norwegian University of Science and Technology (NTNU). The project was carried out at the Department of Electronic Systems between January and June of 2021, and has been supervised by Trond Ytterdal (NTNU) and co-supervised by Pål Øyvind Reichelt (Disruptive Technologies AS). The initial idea of this Master's thesis was suggested by Disruptive Technologies AS Oslo.

The authors background and experience

During my time at ELSYS, I specialized in design of digital systems. Therefore, my knowledge and experience with analog circuit design is limited. This will probably be reflected in the conducted work and results of this thesis. However, I chose this project because of my interests in power-saving techniques and the future potential of this technology. This thesis may presents a simplified version of a very complex topic. However, I hope that this thesis will contribute with a better understanding of the applicable theory for those who follow. Despite the fact that it felt like an enormous amount of work for someone with limited experience, I have learned a great deal. All figures presented is made by the author.

Keywords

IoT, Integrated step-down converter, charge pump, switched capacitor arcitecture. $1MHz$ Clock frequency, 3.3 to 1.8V converter, $47\mu F$ capacitive load, low-power low-current $1nA$ to $10\mu A$ output. $28nm$ technology.

Abstract

This thesis presents the fundamental aspect of a Switched Capacitor Power Converter (SCPC) and how to achieve multiple voltage conversion ratios for a practical application. This thesis builds on existing theoretical concepts, but also contributes by investigating new aspects within the field of research. The end-product is intended to serve as a proof-of-concept. Due to the increased circuit complexity, this thesis focuses on the analysis and design of the power stage of DC-DC converter mainly.

In this thesis, an on-chip switched capacitor step-down voltage regulator (OCVR) utilising three different topologies is designed and simulated with 28nm technology. The converter's load requires only 10 μA, and any losses above 10 μA is considered critical for the design. The main purpose is therefore to have the most effective power transfer with minimal losses when stepping down a varying input voltage source ranging from 3.3 V to 2.4 V to a stable 1.8V on the output terminal.

It was discovered during testing of the triple-topology module that both capacitors and MOS-switches had to be multiplied with a factor of 3 to meet the specified operation parameters. The final triple-topology design, excluding the control circuits, achieved an efficiency ranging from 71.2% to 95.7%, peaking at 2.4 V, however, area demanding. The proposed converter provides an output voltage of 1.8V well within the requirement as the voltage at the output varied by a maximum of $\pm$ 25 mV in both ripple and DC offset. The final design has also taken into account a 200 mV voltage-drop over the output load. A 47 μF load capacitor outside the integrated circuit is used for handling current-spikes when in active mode, as the load may require more power for a short period of time. The device will have a 1MHz clock available when in active mode, which is utilized by the Switch-Capacitor module.

Sammendrag

Denne oppgaven tar for seg grunnleggende aspekter i Switched-Capacitor Effekt Omformere (SCPC), og hvordan man kan realisere de nødvendige spenningsomregningsforholdene for et bestemt bruksområde. Denne masteren bygger på eksisterende teoretiske grunnlag, men bidrar også ved å undersøke nye muligheter innen forskningsfeltet. Sluttproduktet er ment som å tjene som et proof-of-concept. På grunn av kretskompleksiteten i dette feltet, fokuserer denne oppgaven hovedsakelig på analyse og utforming av effekt-trinnet til DC-DC-omformeren.

Denne oppgaven presenterer en on-chip switched capacitor step-down voltage regulator (OCVR) som bruker tre forskjellige topologier, og denne er designet og simulert i 28 nm teknologi. Omformerens last krever bare 10 mu A, og eventuelle tap over 10 mu A anses å være kritiske for designet. Hovedformålet er derfor å ha den mest effektive effektoverføringen med minst mulig tap når man trapper ned en varierende inngangsspenning som spenner fra 3,3 V til 2,4 V, til en stabil 1,8 V på utgangsterminalen.

Det ble oppdaget under testing av trippel-topologimodulen, at både kondensatorer og MOS-brytere måtte multipliseres med en faktor på 3 for å oppfylle de spesifiserte driftsparametrene. Det endelige trippel-topologidesignet, unntatt kontrollkretsene, oppnådde en effektivitet fra $71,2\%$ til $95,7\%$, og nådde maks på 2,4 V, men som betyr at den ble arealkrevende. Den foreslåtte omformeren skal gi en utgangsspenning på 1,8 V, men hvor spenningen ved utgangen kan maksimalt variere med $\pm$ 25 mV i både støy og DC offset. Den endelige utformingen har også tatt hensyn til et 200 mV spenningsfall over utgangslasten. En 47 mu F lastkondensator utenfor den integrerte kretsen brukes til å håndtere strømtopper når den er i aktiv modus, da belastningen kan kreve mer kraft i en kort periode. Enheten vil ha en 1MHz klokke tilgjengelig i aktiv modus, som brukes av Switch-Capacitor-modulen.

ACKNOWLEDGEMENTS

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Pål Øyvind Reichelt, Senior Analog Architect, Disruptive Technologie AS: Co-supervisor

Pål Gunnar Hogganvik, PhD Student, Nanoelectronicsystems at UiO: General know how in analog circuit design

It would be a understatement to say that I would not have been able to hand in this thesis without some help along the way. First and foremost, I would like to thank Prof. Trond Ytterdal for his support and professional approach while supervising me during my project and master's thesis. His years of experience within the field of nanoscale electronics, and his know how from hundreds of publications have greatly inspired me to improve my work on this thesis. Both Ytterdal and co-supervisor Pål Øyvind Reichelt never failed to encourage me, even when struggling with the task at hand, asking all kinds of questions. They have been both helpful and supporting, which have helped me to improve the way I handle challenging tasks.

I can also not ignore Pål Gunnar Hogganvik's help, which was been crucial for setting up and navigating the complexity of the Cadence software, at the same time explaining to me some fundamental theory within the field of nanoscale CMOS electronics, giving me a good start to it all.

I would also recommend the reader to check out the references provided in this work as there are many great minds working every day to improve this technology.

Lastly I would like to thank my friends and family for all support during this project, and as well throughout my studies. I love you you all!

PROBLEM DESCRIPTION

The goal of this thesis is to design a proof-of-concept DC-DC voltage regulator aiming to reach the absolute minimum power-loss possible, hence maximising efficiency. This task is one of the highest priorities set by Disruptive Technologies in order to reach the ambitious goal of maximising the lifespan of a 3.3V battery-cell, giving their Wireless Sensor Network technology an astonishing 15 year life expectancy without the possibility of recharging. The most complicated aspect, is the area requirements, which restrict the use of bulky and passive components leaving the only option to implement the voltage regulator as an on-chip integrated circuit using 28nm technology. The required specifications are:

- Input voltage range: 3.3V to 2.4V
- Output voltage: 1.8V
- Output accuracy: $\pm 25mV$
- Maximum load current: $10\mu A$
- Load capacitor: $47\mu F$
- Maximum clock frequency: 1MHz

This master's thesis is a continuation of the project thesis written by the author in autumn 2020 [5]. The project acted as a feasibility study for this thesis and some parts presented here are directly related to the project thesis. In that project, a circuit design of a multi switched-capacitor circuit was presented situated on Charge Balance Analysis in combination with a Verilog-A-based regulation system. In that project, it was not taken into account any voltage-drop across the load, and non of the topologies used charged in both phases. This approach came close to satisfy the given parameters at some intervals, confirming some of the theory, but fell short when implemented/simulated over a wide input range. This thesis builds upon the work carried out in the specialization project and is a continuation that is intending to improve upon this work by using a Charge Flow Analysis approach. This work will also emphasise on the Charge Balance Analysis versus Charge Flow Analysis and how the two can give different result and performance.

Abbreviations and Notations

ARCT CTRL	Architecture Control
COMP	Comperator
CLK	Clock
CMOS	Complementary Metal Oxide Semiconductor
DC/dc	Direct current
FPGA	Field-Programmable Gate Array
IC	Integrated Circuits
ICT	Information and communication technology
IoT	Internet of Things
KCL	Kirchoffs Current Law
KVL	Kirchoffs Voltage Law
LED	Light-emitting diode
MIM	Metal-Insulator-Metal
MOM	Metal-Oxiede-Metal
MOSFET	Metal-Oxide-Semiconductor-Field-Effect-Transistor
MCU	Microcontroller Unit
NMOS	Negative-Channel Metal Oxide Semiconductor
ULP	Ultra-Low-Power
OCVR	On-chip voltage regulator
PMOS	Positive-Channel Metal Oxide Semiconductor
PMIC	Power Management Integrated Circuit
PMU	Power Management Unit
PFM	Pulse-Frequency Modulation
PWM	Pulse-Width-Modulation
SC	Switch-Capacitor
SCPC	Switch-Capacitor Power Circuit
SoC	System on Chip
SOI	Silicon on Isolation
SW	Switch
TG	Transmission Gate
VAMS	Verilog Analog and Mixed-Signal
VRM	voltage regulator module
WSN	wireless sensor node

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CHAPTER

ONE

INTRODUCTION

Over the past decades, information and communication technology's (ICT) role in society has grown exponentially in conjunction with Moore's [45] and Bell's law [6], leading to an increased demand for computational power. There were about 500-million devices connected to the internet in 2003 [48]. Today, we have reached 35.82-billion devices [49]. With the growing opportunities in "Internet-of-Things" (IoT), an estimation indicates that there will be tens of billions more devices connected by the year 2030 [20]. This development has facilitated an enormous economic potential, and companies are now competing in order to have the best products on the marked. However, a forecast predicts as much as 6000 TWh annual electricity consumption related to ICT by the year 2035 [41]. This places additional demands on the power comsumption of devices connected to the grid and portable battery-driven devices. In terms of competitiveness, it is in every company's interest to optimize power consumption to meet costumers demand of smaller products with longer life expectancy, as well as becoming more sustainable [37].

Parallel to this development during the last four decades, complex electronic systems went from being entirely built from multiple discrete components mounted on a Printed-Circuit Board (PCB) to circuits in a microscopic scale, also known as system on chip (SoC). SoC is the integration of necessary functional elements in order to implement an electronic system onto a single chip or chipset [10]. This physical reduction in size is illustrated in Figure 1.1, where a modern smart phone is compared to a coin-sized battery driven wireless sensor node (WSN).

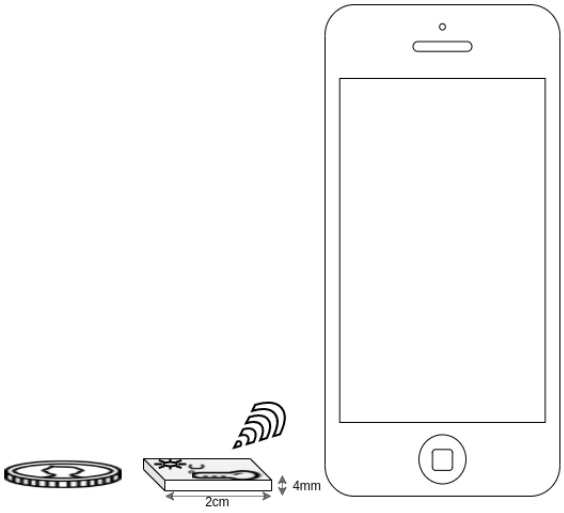


Figure 1.1: Technology size comparison between a coin, wireless sensor node and a smartphone

The main benefit of integration is the ultra-low-power (ULP) consumption. Therefore, any power-loss is regarded as critical when designing ULP circuits. The reduction in size also leads to some complications such as limited space for passive components or battery cells, which in turn limits the available supply voltages. Additionally, smaller WSNs and SoC means narrower wires handling less current and smaller transistors, which lead to shorter gaps between conductors that can add up to a greater current leakage. Because transistor operation is based on its physical properties, small variations in the manufacturing process can lead to large deviations, which in turn can degrade the performance of an integrated circuit. Another consequence is that the threshold voltage does not scale proportional to supply voltage, and the difference between the supply voltage and transistor threshold voltage is reduced, limiting the switching capabilities of a transistor and at the same time increases parasitic capacitance losses [21]. Additionally, the voltage-source of WSNs are varying as the output voltage of batteries changes over time. A Li-ion battery outputs typically between 2.2V-4.2V [53]. This is also problematic as transistors operating in SoC are sensitive to voltage variations. It is therefore critical to achieve a stable load voltage by conversion in one or more stages. Manipulation of the supply voltage is achieved by inserting a Voltage Regulator Module (VRM) between the regular supply and the loading circuit. Actually, this VRM is nothing more but a well-controlled DC-DC converter.

Digital electronics have come a long way in optimisation and power consumption and contributes to lower power consumption in electronic devices. Analog circuits on the other hand can not compete, becoming a bottleneck in this field [51]. A good deal of energy consumption in electronic devices come from inefficient use of power within the electronic devices via thermal power generation. From a power conversion perspective, one of the main contributors to these power-losses are the voltage regulator modules [8], which are performing the DC-DC conversions in a circuit. These VRMs are however crucial as a stable supply voltage is critical for any microcontroller system. In order to increase the battery efficiency of a WSN, and therefore provide longer operating time, power management units (PMU) such as power management integrated circuits (PMIC) are used to control the power consumption. PMIC are one out of many modules in a microchip system and consists of integrated VRMs, or on-chip voltage regulators (OCVRs). This thesis will investigate how to design an efficient OCVR module for an ultra-low-power WSN which is powered by a battery, or in collaboration with an energy harvester, as this is becoming more common with the advent for IoT technology in recent years.

1.1 State-of-the-Art - Year 2021 Landscape

The three main State-of-the-Art OCVR topologies suited for on-chip integration is the linear regulator [27], the traditional Buck converter (inductor-based) [17] and the switched capacitor converter (e.g. [30, 29]). The key differences between these three topologies are the trade-off between the size and performance parameters also known as the figure of merit (FoM). Sometimes a combination of the three can be beneficial. Depending on the application that DC-DC converters is build for, the advantages and disadvantages have to be considered. A more detail explanation of the Line regulator and the Buck converter is given in the appendix E.0.1 and E.0.2 respectively, whereas the switch capacitor power converter will be further investigated in this thesis. A summary of the three alternatives is here given:

Linear Regulators: A linear regulator consists of an analog switch that is controlled by an operational amplifier (Opamp) in order to step down an input voltage to the desired output voltage. The Opamp compares the output voltage to a ratio of the input voltage. This small circuit is easy to build and cost-effective. Linear Regulators are efficient when the dropout voltage is small $<$ 100mV. These circuits also have less noise on the output terminal than compared to switching converters. The main disadvantage for the linear regulator is the challenge of designing the operational amplifier circuit so that it is stable at high switching frequencies.

Buck Converter: A Buck converter consists of a transistor and diode, which applies an input voltage to an inductor-capacitor (LC) circuit. The output voltage is then the voltage across the capacitor. The output voltage of the Buck converter is a function of the well-known expression $V_{out} = DV_{in}$ [19], hence regulation of the output voltage can be done by changing the duty cycle (D). The ideal efficiency of the Buck converter is $\approx 97 - 99\%$ [12], or approximately 100% when using ideal components. However, the accuracy of the inductor is heavily dependent on the core material as well as the frequency with which the current flows through the coil. This physical limitation is the reason why few Buck converters are implemented in nano-scale microprocessor technology. Traditional Buck converters are preferred in situation where area is not an issue such as on a PCB level where coils can be added outside the PMU.

Switch Capacitor Converters: Alternatively there are the switch capacitor converters (SCC)[1] which have high efficiency per area at the cost of circuit complexity. Effectively, SCCs can reach an efficiency >80% [12], which is less than the traditional Buck converter, however similar to the linear regulator while allowing a higher dropout voltage. The efficiency drop is due to the parasitic losses related to the transistor-switching when charging the capacitors that is performing the voltage conversions. Because of these parasitic losses, inductive converters have traditionally been preferred, but it has been shown to be hard to integrate because of the size and accuracy of the inductors. The main advantages of the SC converter is that no inductors are required. The ongoing development of CMOS technology providing high-quality capacitors, and smaller and faster MOSFET transistors for switching, making the SCC more popular among developers. SCCs can also achieve both up- and down-converting topologies. One major drawback of traditional SC DC-DC converters is their ability to provide only a single topology at the time. To overcome this, the state-of-the-art switched capacitor power converters (SCPC) involve the use of recon-

[1] First ever published Switched capacitor DC-DC converter was in 1932 [13]

figurable multi-topology stages to supply variable input or output voltages. The main disadvantage is the sheer complexity of the circuit. Higher accuracy demands multiple topologies meaning more switches. Each switch adds another parasitic loss to the system, thus becoming less efficient.

1.1.1 Figure of Merit

The principal figure of merit (FoM) of published OCVR is the efficiency (%) and their power density(W/mm^2). This characterizes the integration capability relative to its alternatives. A handful of publications are compared and displayed in figure 1.2 based on their maximum efficiency versus output power.

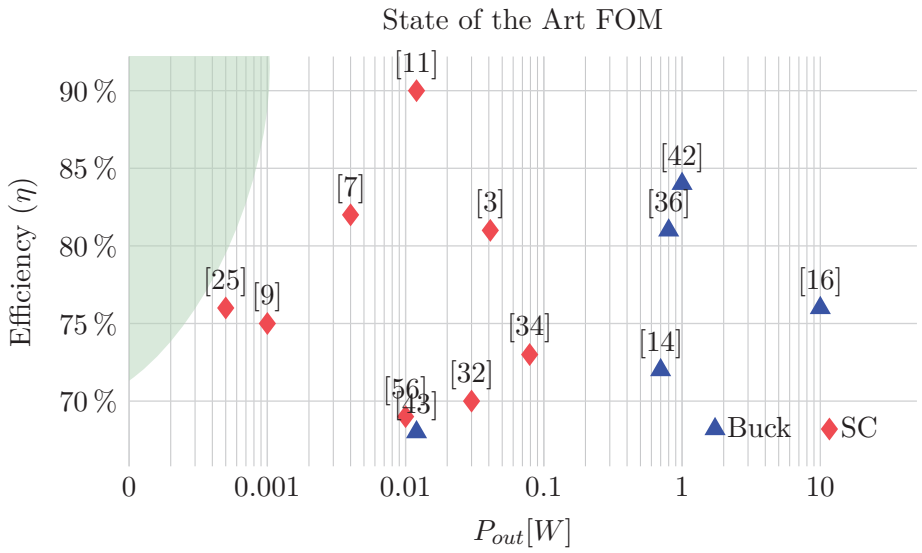


Figure 1.2: Quoted efficiency versus power outputted. This thesis's target zone is indicated in green

As publications often focus on performance comparison (e.g. power density and efficiency), it is easy to understand their focus in the literature. Therefore, the efficiency of this thesis circuit remains a key parameter. However, the reader has to be aware that the efficiency and power density given in some published works are often achieved in the best topology case [21]. Often people only report the power consumption in their conversion topology, and not together with the control logic[2], which also goes for this thesis.

Be that as it may, the overview of the main OCVR converters presented in figure 1.2 indicates that the SC circuits are in the lower power ranges. For this reason, the most suitable approach when designing a VRM for a ULP-WSN would be to use a SC circuit. In figure 1.2 the SC can be seen ranging from $68\% - 90\%$, which should be a good indication for the expected maximum efficiency given in this work. Due to the low output power of $18\mu W$ the estimated target zone is indicated as a green region of the figure.

[2]In [21] they conclude FoM gives a partial view and that this is more often used for convincing reviewers than making a fair comparison.

1.2 Goal of Thesis

This thesis deals with the importance and the technological requirements imposed on the design of DC-DC converters. Moreover, this thesis will investigate how to design an efficient OCVR module for an ultra-low-power WSN which is powered by a battery, or in collaboration with an energy harvester, as this is becoming more common with the advent for IoT technology in recent years. The aim of this work is to present a complete analysis and design methodology for a SC converter which is being used for specific practical application.

1.3 Contributions

This thesis presents an simplified version of what is a very complex topic. One of the main contributions is that this thesis will help to an better understanding of the applicable theory for those who follow, as there are few who have published how the actual circuits have come about. The author has further contributed by:

- deriving a mathematical term for the $\frac{3}{4}$ topology when utilizing three charge transfer capacitors using Charge Balance Analysis
- expending the $\frac{3}{4}$ topology from single to double charge input when utilizing three charge transfer capacitors by applying Charge Flow Analysis, which has never been done before
- introducing the first ever Low-Power High-Speed Charge-Steering Based StrongARM Comparator [1] in an SC circuits.
- designing a triple combination topology[3] using the $\frac{2}{3}$, $\frac{3}{4}$ and $\frac{4}{5}$ fractions which all utilizes three charge transfer capacitors
- implementing a set of optimised custom logic gates for used in the low-power control circuit
- applying the entire concept in 28nm technology

1.4 Thesis outline

Instead of directly presenting the final design and layout in this thesis, the key learnings of each design step are presented. It is therefore the hope that the reader can follow the logic of the design decisions being made along the way, ultimately leading to the finale result. Covering all the relevant background material would also not be feasible in this thesis, so the emphasis has been put on theory that is more or less directly used in the subsequent chapters. Explicit citations are given through the chapters when necessary. The outline of the thesis is as follows:

Chapter 2 - Background theory; provides the background theory that is necessary in order to understand the work done in this thesis. Mathematical foundations of the switched capacitive conversion theory as well as an introduction to basic CMOS implementation and capacitor properties is given her.

[3]topology: "the way in which constituent parts are interrelated or arranged."

Chapter 3 - Conversion Block; will look into the method and implementation of the chosen SC topologies regarded to limitations of the given parameters. The given topologies will be explained using matrices based on Charge Flow Analysis in contrast to the Charge Transfer Analysis in order to account for the choices made.

Chapter 4 - Control Block; will look into the method and implementation of the chosen control circuity. These extra circuits are implemented in order to minimise the overall power consumption.

Chapter 5 - Results; presents simulation data of the finished model

Chapter 6 - Discussion; elaborates on the findings in order to confirm or disclaim the choices made in Chapter 3 and 4. Performance of various state-of-the-art publications is compared to the final result of this thesis in Section 6.3.

Chapter 7 - Conclusion; Finally, conclusions are drawn in chapter 7. Lastly, future work and possible modification will be discussed in section 7.1.

CHAPTER

TWO

THEORETICAL BACKGROUND

The content of this chapter aims to address the necessary background theory of which the main design for this master thesis is based upon. This chapter may resemble some of the work done in this thesis' pre-project [5] written in the previous year. This is necessary in order to build a complete theoretical foundation for this thesis. Fundamental equation within capacitor and transistor theorem will be provided as it is the foundation in SC mechanics. On the other hand, it is not feasible to cover all areas of the SC subject. Therefore, some subject such as energy storage, device cost, optimized capacitor values, optimized switch conductance, etc. is not addressed in this thesis. If necessary, more of the classical switched capacitor theory found in textbooks, such as the half-converter[1], is presented in this thesis pre-project. Other important theoretical remarks are further given where it is considered necessary throughout this thesis.

[1]Multistage converters are a rarity, hence the series-parallel half-converter are used in most of the publications. Common voltages such as 48V, 24V, 12V can be achieved using half-converters.

2.1 Capacitive DC-DC Converter Structure

Capacitive DC-DC converters consists of two main structures: A Conversion Block and a Control Block. The Conversion Bock is responsible for preforming the voltage conversion between the DC input voltage and the DC output voltage. The Control Block manipulates the behavior of the Conversion Block and can preform tasks such as manipulating duty cycle, turning on or off switching-networks, or just shutting of the Conversion Bock entirely in order to save energy. A simplified converter structure is illustrated in figure 2.1 as a point of reference.

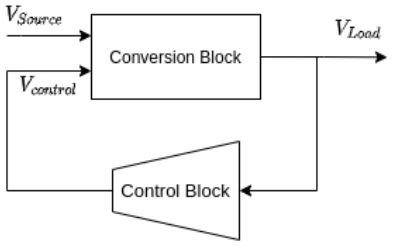


Figure 2.1: Graphical representation of a simplified OCVR system

2.2 Converter Characteristics and Fundamentals

To give a solid understanding of the switched capacitive conversion theory used in the Conversion Blocks, this section introduces the fundamental converter characteristics of DC-DC converters in general. The following sub-chapters introduces equations provided from textbooks such as [4, 8], which will give the reader some relevant background in the fundamental theorems and building blocks which the DC-DC conversion principles is build up on, thus laying the mathematical foundations for the chosen SC circuit presented later on in Chapter 3.

2.2.1 Voltage Conversion

The main goal of the OCVR conversion block is to transform the output voltage to a desired ratio of the input voltage. This characteristic is often represented in textbooks as the Voltage-Conversion-Ratio (VCR):

$$VCR = \frac{V_{out}}{V_{in}} \tag{2.1}$$

The VCR equals a ratio between an output voltage (load) in relation to a input voltage (source) and is often refereed to as the voltage gain of a VRM. In addition to being featured in VRM, this term is often used in other parts of electronics such as in amplifiers. When the VCR is considered a constant value and not varying it's called an ideal voltage conversion ratio ($iVCR$). For simplicity this report will from here on represent the $iVCR$ as a fraction named M. This simplification is done in order to ease the readability of further equation given in this thesis[2]. Based on this, the output voltage can be represented as:

[2]The representation M (Mode) is not uncommon in publications related to SCC.

$$V_{out} = MV_{in} \tag{2.2}$$

As M is constant the output voltage will change linearly with the input voltage. If M is smaller than one, it is known as a down- or Buck converter, when larger then it is called a up-, or Boost converter. Equation 2.2 represents the DC value of the output voltage which does not take into account any noise factor, meaning that any noise from the input will also be amplified with a factor M. If a varying current flows through a series and parallel-connected RLC-ladder (Resitor, Inductor and Capacitor), the DC voltage of the source is turned into a voltage that exists of a large DC component and an AC signal. This AC signal is called the input noise. A more accurate representation of the output voltage is to say it is an constant DC voltage as an average between upper and a lower limit of the output voltage, also refereed to as the DC offset.

$$V_{out} = |V_{DC} \pm V_{AC}| \tag{2.3}$$

2.2.2 Noise Factor

In the case of a switching capacitor circuit the most prominent noise factor would typical be ripple. Ripple is a byproduct and will appear on the output terminal due to the nature of switching while performing the charge transfer between the capacitors [31]:

$$V_{ripple} = \pm V_{AC} = \frac{I_{out}}{C_{load}} \cdot \frac{T}{2} = \frac{I_{out}}{2f_{sw}C_{load}} \tag{2.4}$$

where T is the switching period, and C_{load} is the SCC buffer capacitor. In a situation where the output load is a digital circuit and its main function is to manipulate multiple transistor, such as in a MCU or a FPGA, then the noise outputted by the DC-DC converter can unintentionally influence the threshold voltage by introducing errors in data converters.

2.2.3 Voltage Gap

Voltage gap, or drop out voltage, points out the mismatch between the input voltage and the maximum supply voltages in electronic circuits:

$$\Delta V = V_{in} - V_{out} \tag{2.5}$$
$$= V_{in} - MV_{in} \tag{2.6}$$

In fact, equation 2.6 gives rise to the sizing of the SC charge transfer capacitor. ΔV is also associated with the capacitors charge-sharing losses [21]. If the output voltage deviates from this desired level, the efficiency of the SC converter drops. Also, if the variation is large, the power loss becomes unacceptably high due to charge redistribution [54].

2.2.4 Efficiency

The converter's efficiency is calculated through the output power and its losses during operation. Efficiency η is given as the ratio of the converter's output power in relation to the converter's input power, as shown in equation 2.7. The converter's efficiency is one of the most important characteristics of a DC-DC converter. Because P_{out} is so small when working with ULP converters, η is very dependent on the size of P_{loss}. This means that there is little margin before P_{loss} will dominate. In an ideal case there are no power losses, however there are many sources to losses witch will be addressed in the forthcoming chapters.

$$\eta = \frac{P_{out}}{P_{in}} = \frac{P_{out}}{P_{loss} + P_{out}} \tag{2.7}$$

2.2.5 Power Density

Power Density ρ indicates how much power the converter can preform/deliver to the output with respect to its occupied area:

$$\rho = \frac{P_{out}}{A} \tag{2.8}$$

Since the system must be implementable, the overall area is also important. Therefore, the best trade-off between size and performance should be found. This is why Power Density is known as one of the key performance metrics.

2.3 Introduction to Switched Capacitor Power DC-DC Converters

The essence of the switched-capacitor in ICs is to mimic the function of a resistor by using capacitors and analog switches. In conventional analog circuits, a ratio of resistances is used to set the transfer functions of amplifiers. The frequency responses of active filters and signal generators are determined using the values of the RC product [50].

The intention of SCPCs, however, is not to control amplifiers, but rather to affect the output voltage across a load by acting as an adjustable resistance in accordance with the input voltage. The voltage conversion ratios in SCPC can be generated according to the configuration of its switches and capacitors. By turning switches on and off consecutively, a configuration of the charge transfer capacitors changes. A consequence of this is that the output voltage can be equal, higher, lower or opposite in polarity compared to the input voltage. Figure 2.2 illustrates how three different topologies with three different conversion ratios can be implemented when using a single fly-capacitor in combination with two sets of switches to control the output voltage.

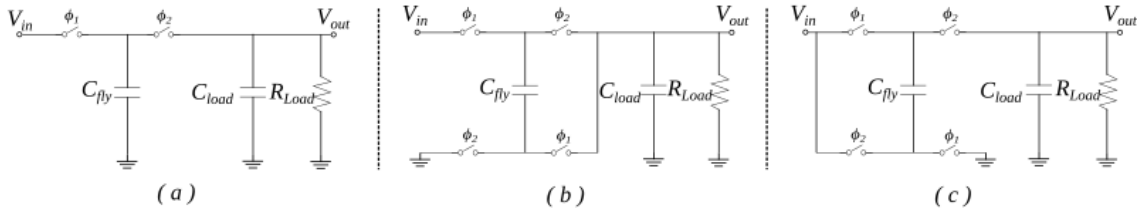


Figure 2.2: Three examples of Switched Capacitor Converters: (a) 1-to-1 Topology (b) 2-to-1 Topology (known as the half converter) (c) 1-to-2 Topology

SCPC circuits consist of two types of capacitors, one preforms the charge transfer (C_{fly}), while the other influences the startup behavior of the load (C_{load}). The ideal conversion ratio M is determined by the numbers of fly capacitors used in the circuit as well as the frequency governing the parasitic on-state resistance of the switches. The ideal efficiency of an SCC is, at it's maximum, when ratio between the output voltage and the input voltage get close to the ideal conversion ratio:

$$\eta_{ideal.SC} = \frac{V_{out}}{MV_{in}} \tag{2.9}$$

2.3.1 Basic operation of Switched Capacitor Converters

Figure 2.2 illustrates a system in two stages of operation for a 1-to-1 SCC. Here, the two switches are operated by the non-overlapping clock signals, ϕ_1 and ϕ_2.

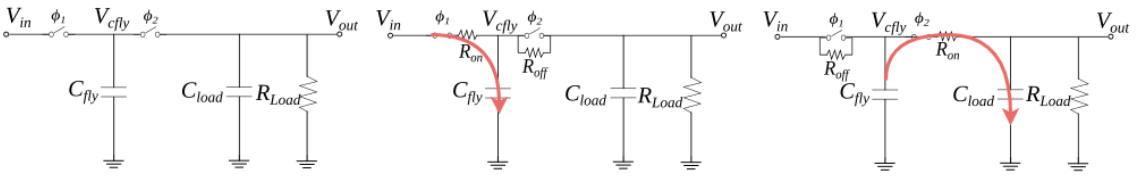


Figure 2.3: Switched Capacitor converter 1-to-1 Topology

When each set of switches are moving charge from one capacitor to another at typically 50% duty cycle[3], then the system can be seen as two circuits, a charging and discharge circuit. When charge propagates through the circuit, the voltages across each capacitor is affected. The voltage across C_{fly} is given in equation 2.10:

$$V_{C_{fly}} = V_{out} + (V_{in} - V_{out})e^{-t/\sum(R_{out}C_{fly})} \tag{2.10}$$

Where the initial voltage is V_{in} at time zero, and the voltage the capacitor is charging towards is V_{out}. R_{out} represents the total amount of resistance across both the flying capacitors and the switches that is utilized by the converter, which will be derived later in equation 2.20. This resistor is the fundamental foundation in switched-capacitor circuits.

[3]SCC operating at duty cycles below 50% is possible, effecting the R_{out} resistance, which is similar to using PWM [30]

This means that this system is effectively working as a controllable voltage divider circuit. In the case of the 1-to-1 SCC, the output would propagate towards the input value as shown:

$$V_{out_T} = \sum_{t=0}^{T} \frac{C_{fly} V_{C_{fly|_t}} + C_{load} V_{out|_t}}{C_{fly} + C_{load}} \tag{2.11}$$

When in steady state, the load capacitor C_{load} is fully charged working as a voltage source. In practise, the load capacitor have to be greater than the sum of flying capacitors, however it should be much larger, hence eliminating the ripple at the output terminal[3].

2.3.2 Switched Capacitor Topologies

A math-based theory of possible conversion ratio M ranging from $i = 1$ to $i = 4$ flying-capacitors when using two clock phases [4] is developed and proposed in literature such as [39, 38, 22][5], and are here summed up and presented in Table 2.1. According to [22], this table shows which values of M that can be realized (independent on the nm-technology used), but points out that the systematic synthesis of each of these values had so far (2017) not been addressed. One simple reason for this could be that the inductor based technology have been superior, and that there have not yet been a good enough reason to to apply anything else. As we now know, this might change if to adapt to the new demands of low-power miniature electronics. There are however some drawbacks when considering the available conversion ratios, mainly the fact that they can only approach the true ratio when no load i present, e.g. [21, 22, 46, 55]

Table 2.1: Available conversion ratios

Numbers of Cfly (i)	Available conversion ratios (M_i)
1	$\frac{1}{2}$, 1, 2
2	$\frac{1}{3}$, $\frac{1}{2}$, $\frac{2}{3}$, 1,$\frac{3}{2}$, 2, 3
3	$\frac{1}{5}$, $\frac{1}{4}$, $\frac{1}{3}$, $\frac{2}{5}$, $\frac{1}{2}$, $\frac{3}{5}$, $\frac{2}{3}$, $\frac{3}{4}$, $\frac{4}{5}$, 1, $\frac{5}{4}$, $\frac{4}{3}$, $\frac{3}{2}$, $\frac{5}{3}$, 2, $\frac{5}{2}$, 3, 4, 5
4	$\frac{1}{8}$, $\frac{1}{7}$, $\frac{1}{6}$, $\frac{1}{5}$, , $\frac{1}{4}$, $\frac{2}{7}$, $\frac{1}{3}$, $\frac{3}{8}$, $\frac{2}{5}$, $\frac{3}{7}$, $\frac{1}{2}$, $\frac{4}{7}$, $\frac{3}{5}$, $\frac{5}{8}$, $\frac{2}{3}$, $\frac{5}{7}$, $\frac{3}{4}$, $\frac{4}{5}$, $\frac{5}{6}$, $\frac{6}{7}$, $\frac{7}{8}$, 1, $\frac{8}{7}$, $\frac{7}{6}$, $\frac{6}{5}$, $\frac{5}{4}$, $\frac{7}{5}$, $\frac{3}{2}$, $\frac{8}{5}$, $\frac{5}{3}$, $\frac{7}{4}$, 2, $\frac{7}{3}$, $\frac{5}{2}$, $\frac{8}{3}$, 3, $\frac{7}{2}$, 4, 5, 6, 7, 8

From Table 2.1 we can see that for each extra fly capacitor added, the complexity (multiple switches) and output accuracy (ratios) increases. A single fly capacitor system will have the fewest switches, hence be more power efficient on it's own. However, increasing fly capacitors and combining multiple topologies will increases the average overall efficiency as pointed out in [22]. It is possible to achieve these ratios by adding them, for example adding a half-converter (2-to-1) to another half-converter to get a quarter-converter (4-to-1). There are also many different design techniques in order to achieve these conversion ratios, such as the Ladder, Dickson, Fibonacci, Series-Parallel and Doubler architecture, which is addressed in sources such as [47]. There will always be a trade-of when choosing

[4] An expansion of Table 2.1 is possible if to use multi-clock-phase topologies as shown in [22]

[5] In 2015 a published paper [29] criticise two of the mentioned articles saying the approach in these works was mathematical and not circuit-design oriented, quote; "The proof provided in [39] and [38] was non-constructive, i.e., it was not possible to directly synthesize the SCPC topologies based on this proof"

these ratios, as higher complexity will take more time to design and test, and also increase the consumed area on the chip. However, it will increase the accuracy and thus becoming more power efficient. Moreover, increasing i capacitors indicates a higher amount of switches in the circuit, effecting the ripple as well as add to the power leakage, thereby becoming less efficient. Even though fractional converters exist for a whole range of conversion ratios, in practice the number of capacitors is kept below four since the output impedance increases fast in function of the number of capacitors and switches used [8]. Capacitors is also the dominant area consumer in CMOS technology, which makes it even more reasonable to minimise the use. How to determine the different topologies will be explained in section 2.4 analysis of SCC.

2.4 Analysis Techniques

Analysis techniques are used to determine the ideal convection ratios M for more advanced SCPCs. Because SCPCs are complex time-varying circuits, as pointed out in section 2.3.1, they have to be simplified using a set of static analysing techniques. This is useful as differential equations in power electronic circuits are very time consuming to solve [3]. There are multiple[6] analyses techniques developed within the field of SCPC. Analysis techniques such as Charge Balance Analysis, Charge Flow Analysis or Branch Analysis are the most commonly used methods, leading to different performance tradeoffs. In this thesis, we will only look at two of the most common ones, Charge Balance and Charge Flow techniques.

A steady state behavior of a switched capacitor power converter can be represented as an ideal transformer with a series output impedance meaning one can ignoring frequency dependent parasitic losses [46]. Based on Kirchhoff's laws of conservation, KVL and KCL, it is possible to simplify these circuits as a modeled Thevenin equivalent circuit, as seen in figure 2.4.

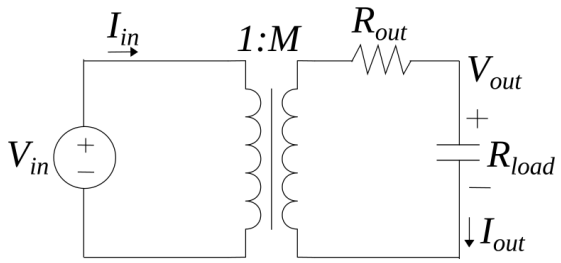


Figure 2.4: Thevenin equivalent SC circuit model for all possible topologies M_i including an circuit output-resistor combined with load decoupling component

The SCC is at its simplest form when in steady state, meaning the load current equals zero. When no load current is applied, $I_{out} = 0$, then the voltage drop across R_{out} is zero, meaning the total voltage drop across the transformer model must equal $C_{load}R_{load} \cdot V_{in}$.

[6]Even by 2021 there are not one **exact method** or theory on how to approach SCC synthesize, making some analysis challenging to apply for SC converters with conversion ratios other then $M_{i=1}$ [3]

2.4.1 Charge Balance Analysis

The charge balance analysis [55] is a model based on energy conservation when in steady state, and applies KVL and KCL in each connected node between the input terminal and the output terminal in both the charging and discharging circuits. When performing charge balance analysis, [55] states in his work that the capacitor and switch system should be treated as an energy transfer device. Charge balance analysis assumes an absolute amount of charge (Q) in the circuit at a set time. This results in the following charge conservation equation, assuming that energy is conserved with 100% power efficiency; input power equals output power:

$$V_{in}Q_{in} = V_{out}Q_{out} \tag{2.12}$$

rearranging equation 3.1 yields to:

$$\frac{V_{out}}{V_{in}} = \frac{Q_{in}}{Q_{out}} \tag{2.13}$$

Where Q_{in} refers to the total amount of charge in the charging circuit, and Q_{out} to the total charge in the discharging circuits. When charge balance analysis is applied to circuits where the number of capacitor i in the circuit is > 1, then the sum of the charge in the capacitors (C_{eq}) in parallel can simply be added. However, as pointed out in [55] the capacitors in series when fully charged will not equal $\frac{C_1C_2}{C_1+C_2}$ but $\frac{2C_1C_2}{C_1+C_2}$. The next step is then to simplify equation 2.13 in terms of V_{in} and V_{out} by applying KCL (equation 2.30) to solve for any unknown $V_{C_{fly}}$ in the system.

2.4.2 Charge Flow Analysis

Charge flow analysis [46, 39], which treats the capacitor and switch system as a resistor, demonstrates an intuitive method to determine the VCR ratio of any chosen topology of the capacitive converters mentioned in Table 2.1, assuming steady state conditions. It differs from charge balance analysis as it concerns the change in charge (q) of the components. In this method the VCR M_i can be derived using KVL and KCL assuming all charge into a node equals to zero:

$$M_i = iVCR = \frac{q_{in}}{q_{out}} = \frac{q_{in}^{(1)} + ... + q_{in}^{(n)}}{q_{out}^{(1)} + ... + q_{out}^{(n)}} \tag{2.14}$$

This approach plays an important role in the modeling and design choices presented in this work. The Charge Flow mathematical framework was first introduced in [39] denoting the charge multiplier vector a^n as a mean of exploring performance limits of switched-capacitor converters. The charge vector a^n can be split into two types of vectors, the charge capacitor element a_c^n and the charge resistance element a_r^n. These vectors play an important role when determining the systems power loss, hence effecting the efficiency η. The general notation of the capacitor element a_c^n is given in equation 2.15 and can be applied for any n number of phases:

$$a_c^n = \left[\frac{q_{out}^n}{q_{out}}, \frac{q_{c,1}^n}{q_{out}}, ..., \frac{q_{c,i}^n}{q_{out}}, \frac{q_{in}^n}{q_{out}}\right] = \left[a_{out}^n, a_{c,1}^n, a_{c,i}^n, a_{in}^n\right] \tag{2.15}$$

The charge resistance element a_r^n can only be deduced by analyzing the circuit, which will be demonstrated later.

Equation 2.15 can be used to determine the topology. Equation 2.15 is valid when:

$$\sum_{n=1}^{N} a_{out}^n = a_{out}^{(1)} + ... + a_{out}^{(n)} = 1 \tag{2.16}$$

2.5 Output Load Requirements

A realistic output voltage must take into account the losses related to the non-ideal impedance component R_{out}[7] when charging and discharging a circuit capacitor. The actual output voltage differs from the unloaded ideal output voltage given in equation 2.2 by adding an equivalent non-zero output impedance γ in the equation [8]. The actual output voltage can then be represented as:

$$V_{out|real} = \gamma M V_{in} \tag{2.17}$$

where the equivalent non-zero output impedance γ corresponds to the resistive division between the load resistance and the output impedance, which is depicted in figure 2.4, and quantified as:

$$\gamma = \frac{R_{load}}{R_{load} + R_{out}} \tag{2.18}$$

R_{load} in equation 2.18 is the real component (however frequency dependent) of the C_{load} impedance, while R_{out} is the real component of the SC circuit impedance of both switches and flying capacitors. From equation 2.18 we can see that the smaller R_{load} gets, the more R_{out} dominates. Meaning that the impedance γ shrinks, where according to equation 2.17 the true output voltage falls. Thus, a voltage drop will occur at the output node as the output impedance R_{out} increases:

$$V_{loss|real} = MV_{in} - \gamma MV_{in} \tag{2.19}$$

A consequence of this is that some level of margin has to be considered regarding the input voltage range. For example, operating with an input voltage of 3V with a VCR of 3/5 to ensure an output voltage of 1.8V is not realistic since this will require a 0V voltage drop over the output impedance R_{out}. In this particular example, the approach will not be ideal, and the system will struggled to output the minimum required voltage. It is

[7]For the sake of simplicity it is chosen to call the output impedance R_{out} and not Z_{out} as the following content only focus on the real component $\mathbb{R}$ and not the complex $\mathbb{C}$ of the capacitors impedance (the same goes for γ).

therefore good practice to implement VCRs which accounts for a minimum margin, such as in this example, where a 200 mV voltage drop over the output impedance γ is sufficient.

The output impedance can been derived from Tellegen's Theorem [18] as a sum of two impedance components, The Slow Switching Limit (SSL) and the Fast Switching Limit (FSL) :

$$R_{out} = \sqrt{R_{SSL}^2 + R_{FSL}^2} \tag{2.20}$$

which should be approximately equal the conventional method:

$$R_{out} = \frac{MV_{in} - \gamma MV_{in}}{I_{out}} \tag{2.21}$$

2.5.1 The Slow Switching Approximation

The SSL as seen from a charge flow analysis perspective when applying two-clock phases, assuming 50% duty cycle when operating with ideal switches, allows currents in the circuit to be modeled as a charge transfer. SSL is therefore expressed as:

$$R_{SSL} = \sum_{i=1}^{j} \frac{(a_{c,i})^2}{C_i f_{sw}} = \frac{1}{C_{tot} f_{sw}} \sum_{i=1}^{j} |a_{c,i}|^2 \tag{2.22}$$

where j equals the total number of flying capacitors that is preforming the charge transfer at a fixed frequency f_{sw}. The sum of the capacitors multiplying vectors a_c squared is known to be the dominating factor when analysing the SSL. The SSL related losses can be reduced by either increasing the frequency or the flying capacitors.

2.5.2 The Fast Switching Approximation

When assuming the same conditions mentioned for the SSL, the FSL can be derived as:

$$R_{FSL} = 2 \sum_{k=1}^{K} R_{on,k} (a_{r,k})^2 \tag{2.23}$$

where k equals the total number of switches utilized by the system, and R_{on} is the transistors impedance. In the case of FSL, the conduction losses related to the switching multiplier-vectors a_r dominate. The choice of topology-type such as Ladder, Dubler, Series-Parallel matter, as the number of switches sums up to a total output resistance, this is clearly pointed out in research such as [46] where they compare the same VCR topology M = 1/4 applying the named approaches. Losses related to FSL can be reduced by increasing the transistor widths. This implies that output impedances is related to the area of the chip. The most notable difference when comparing capacitor to inductive DC-DC converters is that lossless conversion can only be achieved with infinitely high switching frequencies or by using an infinitely large amount of capacitance [4]. This is obviously not possible, but a well design capacitive DC-DC converter will however theoretically only face a relatively small efficiency penalty for violating these requirements.

2.6 MOSFET Transistors as Switches in IC Circuits

Switches in electronic integrated circuit can be designed using a doped Metal-Oxide-Semiconductor-Field-Effect-Transistor (MOSFET). MOSFETs can be positively (PMOS) or negatively (NMOS) doped giving them slightly different properties such as on-resistance under the same operating conditions [28]. A switch comprising of both NMOS and PMOS is often used and are called a transmission gate (TG)[35]. A known challenge in SCC is when the gate-source voltage gets low, as switches can be turned of before they should. With TG, this problem can be ignored, as either PMOS or NMOS will be open at any time. It is a cost in area and efficiency, but an investment in time when designing circuits with continually changing voltages. Switch configurations are convenient for sensor module design in chip design, however, the cost, size, complexity and power-loss of the chip increases with each transistor added.

2.6.1 Switching Properties

When regulated in the linear region (strong inversion) of a MOSFET, the transistor can be seen as an on/off switch. However, both layout and doping method can lead to some inaccuracy in CMOS (complementary metal-oxide-semiconductor) technology. Therefore, the following equations are near approximations of the true behavior. The following two conditions have to be satisfied for linear behavior:

$$V_{GS} - V_t \geq V_{DS} \tag{2.24}$$

$$V_{GS} > V_t \tag{2.25}$$

The gate-to-source voltage minus the threshold voltage have to be equal or greater than the drain-to-source voltage for a current I_D to flow from the drain to source terminal of the transistor. I_D is given as:

$$I_D = \mu C_{ox} \frac{W}{L} \left((V_{GS} - V_t) V_{DS} - \frac{V_{DS}^2}{2} \right) \tag{2.26}$$

where C_{ox} is the gate-oxide capacitor per unit width, μ the carrier mobility, W is the transistor width, and L the transistor length. A MOS-switch can be operated by applying a voltage to the gate node. When equation 2.25 is satisfied, the transistor will let the current I_D pass through (closed switch), and $R_{sw} = R_{on}$:

$$R_{on} = \frac{V_{DS}}{I_D} = \frac{1}{\mu C_{ox} \frac{W}{L} ((V_{GS} - V_t) - \frac{V_{DS}}{2})} \tag{2.27}$$

When the gate-voltage is so low that equation 2.24 no longer apply then the PMOS transistor can be viewed as a very large resistance $R_{sw} = R_{off}$ (open switch). This is important as power consumption is related to the parasitic losses in the circuit, which should be minimized, therefore the width W is desirable to be as small as possible. Another observation is that the on-state resistance is dependent on the drain-to-source voltage $V_{DS} = V_D - V_S$, where the drain-voltage V_D increase proportionally with the battery-source voltage. Therefore, ULP circuits are usually designed with a low supply voltage.

In circuit design the gate-, drain- and source-terminals of a CMOS transistor are regarded to as the most interesting ones, although manipulating the bulk terminal has significant influence on the transistors performance. The bulk voltage with respect to the source voltage influences the threshold voltage V_{th} of the transistor that is in turn one of the critical parameters for both analog and digital circuit design. In ultra-low voltage designs, when equation 2.24 is satisfied but not 2.25, this is especially problematic. Actually, in the cut-off region, when both equation 2.24 and 2.25 is not satisfied, there is a significant current-leakage in MOSFET transistors. This so-called sub-threshold leakage [4] is a static power loss that can not be neglected as it unintentionally effects the power-consumption. Sub-threshold leakage can be seen in a off-state resistance when given as:

$$R_{off} = \frac{V_{DS}}{I_{subTh}} = \frac{1}{\frac{W}{L} I_D e^{[\frac{1}{\eta V_{th}}(V_{gs} - V_{th} - V_{sb} + \beta V_{ds})]}(1 - e^{\frac{V_{ds}}{V_{th}}})} \tag{2.28}$$

Both the gate-, drain- and bulk- in relation to the source-terminal affects the sub-threshold leakages as well as many other factors. When MOS-switches are connected in series or parallel, the nodes on each of the terminals changes with time, making it near impossible to calculate an expected power-loss value without simulation.

2.7 Capacitors in Capacitive Converters

A capacitor is an component with many useful properties. One of which is to store potential energy within an electric field. This occurs when charge is being compressed between two conductive surfaces, building up energy which can later be released when needed [5]. The amount of charge Q stored in a capacitor depends on the potential differences ΔV over a distance d between the surface area A and the permittivity ϵ of the insulator between them. In the case of two parallel surfaces an ideal capacitance can be derived as:

$$C = \frac{\epsilon A}{d} = \frac{Q_{ab}}{\Delta V} \tag{2.29}$$

When charge is realised, a current flows from the capacitor and a change in voltage across the capacitor is observed:

$$i_c = C\frac{d}{dt}(V) = \frac{d}{dt}(q) \tag{2.30}$$

However, as demonstrated in figure 2.5, real capacitors have equivalent series resistance (ESR) and inductance (ESL). These parasitics have no effect on the capacitor's ability to store charge. They can, however, have a significant impact on the switched capacitor output voltage and its overall efficiency [23, 52].

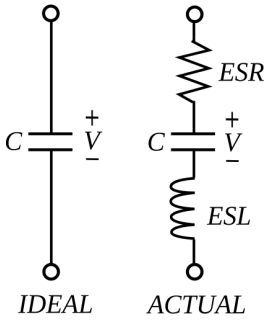


Figure 2.5: Theoretical capacitor and its real-world counterpart

Although the equivalent RLC circuit of the capacitor can be underdamped or overdamped, the relatively large switch resistance generally makes the final output voltage response overdamped. An example using two equally sized capacitors ($C_1 = C_2$) can be used to fully understand the capacitors properties in switched-capacitor circuits. Figure 2.6 shows two capacitors in parallel where the first capacitor is used to transfer charge to the second capacitor. If the capacitor C_1 is charged to a voltage V_1, then the total charge stored in the capacitor, q, is given by $q_1 = C_1V_1$. If this charge flows between the two equally sized capacitors at a set frequency f_{sw}, then the charge transferred in each cycle is $\Delta q = C_1(V_1 - V_2)$.

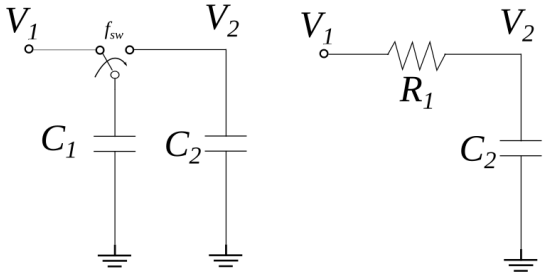


Figure 2.6: Charge transfer in Switched-capacitor circuits

This corresponds to an average current (current = charge transferred per unit time) of:

$$I = C_1(V_1 - V_2)f_{sw} = \frac{V_1 - V_2}{\frac{1}{C_1 f_{sw}}} = \frac{V_1 - V_2}{R_1} \tag{2.31}$$

Notice that the quantity, $\frac{1}{C_1 F_{sw}}$, can be considered as the equivalent resistance, R_1, connected between the source and the load [50]. The power dissipation associated with this resistance is essentially forced to be dissipated in the switch on-resistance and the capacitor ESR, regardless of how low those values are. (It should be noted that capacitors ESR and the switch on-resistance cause additional power losses as will be discussed shortly.) Not shown in figure 2.6 is a capacitor on the input terminal which is generally required to ensure low source impedance as the frequencies contained in the switching propagates [52].

2.8 Loss analysis of Switched-Capacitor converters

Loss analysis is important as maximizing the efficiency corresponds to minimizing the losses, according to equation 2.7. The following equation is based on litterateur [4, 5], where the losses are summed up as:

$$P_{loss} = P_{R_{on}} + P_{R_{out}} + P_{f_{sw}} + P_{cfly} + P_{bp} \tag{2.32}$$

Losses can be categorised into two distinct losses: intrinsic and extrinsic losses. Intrinsic losses occurs due to the laws of conservation of energy, while extrinsic losses relate to implementation of the circuit. There are four main types of losses associated with the SC converter: conduction losses, switching losses, flying capacitor losses and bottom plate parasitic capacitance losses. Conduction losses are inherited to the load current and is duty-cycle dependent. Conduction losses are proportional to the drainsource resistance R_{on} of the MOSFET switch and is given as:

$$P_{R_{on}} = I_D^2 R_{on} = (CV)^2 R_{on} \tag{2.33}$$

In equation 2.33, the conduction loss is dominant at high load current since it is proportional to the quadratic current value. Conduction losses also gives rise to power losses $P_{R_{out}}$ due to the finite output resistance:

$$P_{R_{out}} = \frac{(MV_{in} - \gamma MV_{in})^2}{R_{out}} \tag{2.34}$$

Beside conduction losses there are switching losses which is associated with the Pulse-Frequency Modulation (PFM) switching activity of the SC converter. The switching losses are:

$$P_{f_{sw}} = C_{ox} V_{in}^2 W f_{sw} \tag{2.35}$$

Where W is the transistor width. The third loss mechanism is the flying capacitor loss P_{fly} that is defined as charge loss caused by C_{fly} during the charge transfer throughout the charging and discharging phases. The flying capacitor losses are given as:

$$P_{cfly} = \frac{I_{out}^2}{C_{fly} f_{sw}} \tag{2.36}$$

Note that P_{fly} is inversely proportional to the C_{fly} and f_{sw}, and proportional to quadratic I_{out} . This means that P_{fly} is a load-current-dependent loss. The fourth loss mechanism P_{bp} is caused by the bottom plate capacitor[8] $C_{bp} = \alpha C$ where α represents a particular percentage of the total capacitance based on the CMOS technology. C_{bp} is formed due to the PN junction between the N well and the P substrate and is highly dependent on the technology. Power losses related the bottom plate capacitor is:

[8]The term flying capacitor comes from the fact that these capacitors are not always attached to the bottom plate, hence flying

$$P_{bp} = C_{bp} V_{in}^2 f_{sw} \tag{2.37}$$

The bottom plate capacitance can be as high as 5-20% of the total charge-transfer capacitance, and can have a major impact on SC circuits transfer functions[4].

2.8.1 Minimize leakage in CMOS technology

Leakage power dissipation is one of the dominant contributor to power dissipation in nanoscale electronics. There are many ways to archive a MOS-layout, some of which is more suited for minimizing leakage than others, such as MOM (Metal-Oxide-Metal) or MIM (Metal-Insulator-Metal) [44]. The three primary concepts for reducing leakages at gate level designs is body-biasing, multi-threshold techniques and transistor stacking. Mainly, it all comes down to cost. Leakages can be minimized by separating metallic layers with nonconducting material, also called Silicon on Isolation (SOI). This application can also reduce ripple via the ground plane, which is good, as noise can migrate to other parts of the SoC through parasitic connections, and influence conversion in other parts of the SoC.

2.9 Converter Control Techniques

The following sections intend to explain the control block structure featured in figure 2.1. In order to increase efficiency and extend operating time it is common to combine multiple converter topologies, which means that multiple switching-operations have to be implemented. Control circuits are used to manage these switching operations, e.g. operating the switches in opposite phases at different duty cycles or intervals. A control block is therefore divided into multiple modules as visualised in figure 2.7.

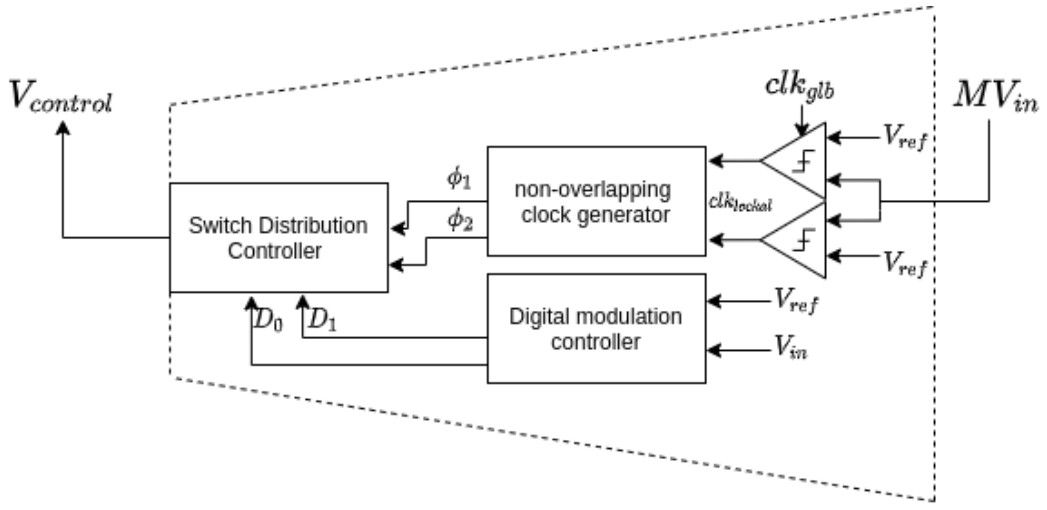


Figure 2.7: Visualisation of a multi module control block

Each module in a control block executes a specific task. A digital modulation controller is used when transiting between multiple topologies. Each transition is executed when the input voltage is smaller (negative) or larger (positive) than a point of reference. A

switch distribution controller distributes the correct non-overlapping clock signals for each of the operating MOS-switches utilized by the converter block. Non-overlapping clocks-generators [15, 40] are well know circuits and have been used in SCC to turn on/off switches independently in opposite phase without short-circuiting the circuit. Because PMOS and NMOS switches is a mirror image of another, they need inverted clock-signals. This function can easily be solved by adding a latency to one of the two phases. A set of one or two comparitor circuits provide switching control signals to the converter in phase with the input clock, using pulse-width modulation (PWM) or pulse-frequency modulation (PFM), thus regulating the output impedance. Both PWM and PFM uses reference voltage(s) to correct the output. This is show by an example in figure 2.8. Because control circuits are mainly design using logic gates, then it is possible to save a large amount of energy and space by simplifying their Boolian functions. One way could be to use inversions, which is derived by De Morgan's law[26], for example:

$$\overline{\overline{D_0} + \overline{D_1}} = D_0 D_1 \tag{2.38}$$

Equation 2.38 shows that an AND gate can be implemented using an NOR gate and two inverters. If $\overline{D_0}$ and $\overline{D_1}$ is available, then this equations saves two transistors because AND gates is implemented with a total of six transistors, and the NOR only needs 4. By applying the rules of absorption, involution, De Morgans or the associative function, then most Boolean expressions can be simplified, thus reducing numbers of transistors needed.

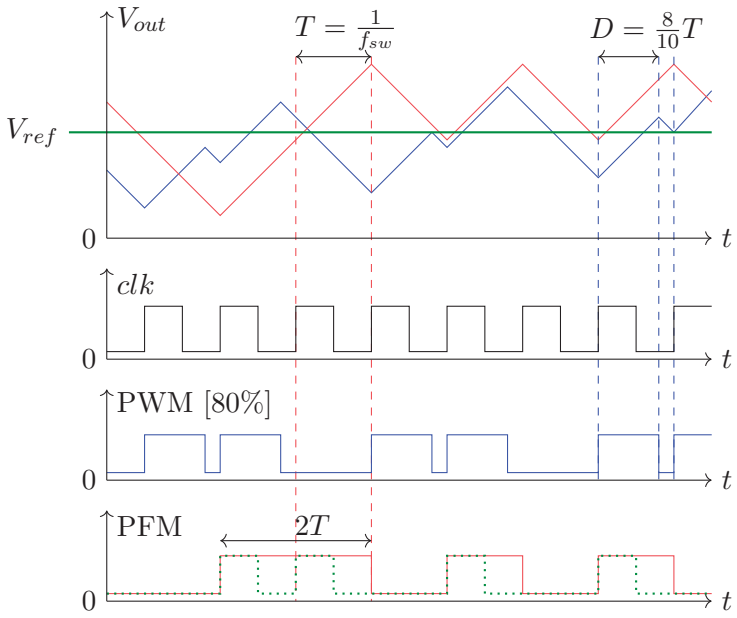


Figure 2.8: PWN applying 80% Duty Cycle, versus PFM. Both signals control the output voltage on rising clock

An observation from figure 2.8 is that PFM, which changes its period over time, can also be achieved when switching off the clock over time. In fact, the most straightforward technique to reduce power consumption in a digital system is by shutting down the clock, also referred to as clock gating. Clock gating can be achieved by implementing a single-

or double-bond hysteric feedback controller. Clock gating can also be applied to control the entire WSN device. One of the most common system level algorithms for power management is dynamic power management (DPM) [4]. DPM is a design methodology that achieves energy-efficient operation by selectively turning off system components when they are idle, by laying dormant (sleep mode), and by operating them at peak performances when activated (active mode). During sleep mode, the switch-capacitor system can re-charge the load capacitor, then turn it self off entirely until the output voltage reaches the minimum regiments and re-waken.

CHAPTER

THREE

CONVERSION BLOCK

This chapter describes how the final switched-capacitor circuits are built by using two of the most known analyzing techniques, before the actual circuit implementation is finalized in section 3.3. Due to the specific application, only relevant topology are demonstrated for a selection of capacitive DC-DC converter as the lithium battery gradually decay from $3.3V$ and eventually dies at $2.4V$. Because the theory on SSC is a work in progress, the aim of this chapter is to further explore the possibility of designing a circuit that can chare the flying capacitors in both phases. This should minimize power losses as well maintaining a positive trend of output voltage in both stages. In section 3.2 the analyse techniques are demonstrated in order to differentiate and conclude the choices made using examples that are limited by the given parameters in this thesis. This will contribute to bridge the gap between the specialization project [5] and this thesis, and also make it easier to describe the actual implementation of the circuitry layout afterwards in section 3.4.

3.1 Topology Selection

A wide range of input voltage requirements poses a design challenge due to linear efficiency loss, given by equation 2.7. Different SC topologies need to be switched in the converter circuit to preserve efficiency. To satisfy the given requirements, three SC topologies, namely 4/5, 3/4, and 2/3, were chosen for the varying input voltage, assuming ∼200mV voltage drop over the the output impedance. This means the SCC is aiming for an approximately output voltage around 2V and not 1.8V, this is possible as the control block will ensure 1.8V over the load with clock manipulation.

First Input Voltage Range: 3.3 - 3V
SC topology chosen: 2/3 Expected efficiency (η_{exp})

$$V_{out|max} = 3.3 \cdot \frac{2}{3} = 2.2V \qquad \eta_{exp} = (1 - (2.2V - 1.8V)/2.2) = 81.81\%$$
$$V_{out|min} = 3.0 \cdot \frac{2}{3} = 2.0V \qquad \eta_{exp} = (1 - (2V - 1.8V)/2) = 90.0\%$$

Second Input Voltage Range: 3.0 - 2.7V
SC topology chosen: 3/4

$$V_{out|max} = 3 \cdot \frac{3}{4} = 2.25V \qquad \eta_{exp} = (1 - (2.25V - 1.8V)/2.25) = 80.0\%$$
$$V_{out|min} = 2.7 \cdot \frac{2}{3} = 2.025V \qquad \eta_{exp} = (1 - (2.025V - 1.8V)/2.025) = 88.9\%$$

Third Input Voltage Range: 2.7 - 2.4V
SC topology chosen: 4/5

$$V_{out|max} = 2.7 \cdot \frac{4}{5} = 2.16V \qquad \eta_{exp} = (1 - (2.16V - 1.8V)/2.16) = 83.3\%$$
$$V_{out|min} = 2.4 \cdot \frac{4}{5} = 1.92V \qquad \eta_{exp} = (1 - (1.92V - 1.8V)/1.92) = 93.75\%$$

Figure 3.1 illustrates the expected efficiency of the three topologies combines compared to using one topology.

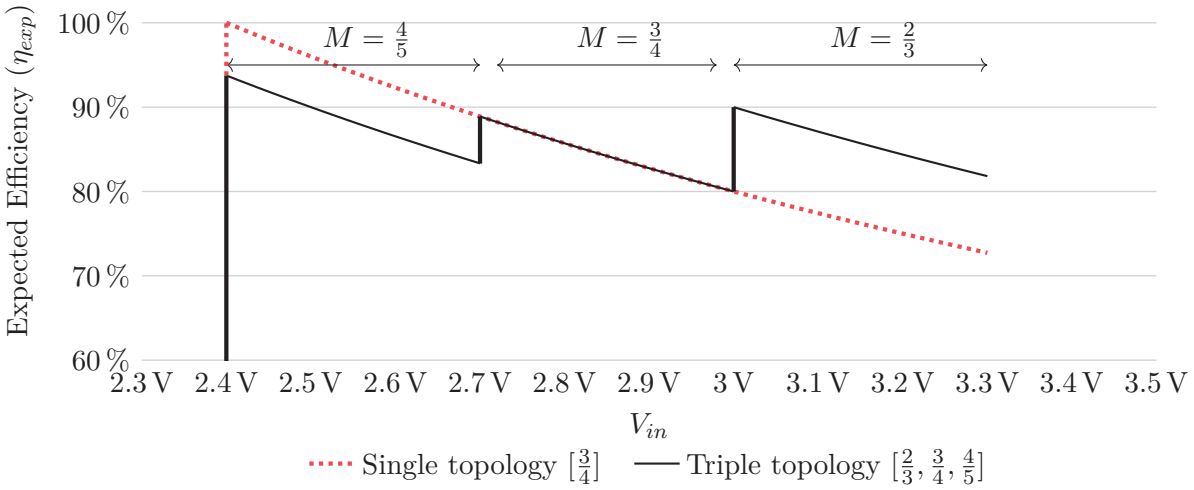


Figure 3.1: Expected efficiency; One topology versus triple topology

3.2 Topology Synthesis

In order to minimize complexity, area-consumption and switches used, while at the same time not risking ending up with too high output impedance, a total of $i = 3$ fly capacitors were chosen. According to Table 2.1, the only suitable conversion ratios that will satisfy the given parameters are then $M_{i=3} = \frac{2}{3}, \frac{3}{4}, \frac{4}{5}$. The simplest form of circuit approach would be to use a series-parallel system. The parasitic bottom plate capacitors are not considered in this chapter, as existing model framework does not support this, even though it plays an essential role in on-chip SC converters, affecting both the operation and the converter's efficiency. For that reason, the anticipate efficiency would be lower that what is illustrated in figure 3.1.

3.2.1 Charge Balance Analysis of the Series-Parallel 3/4 Converter

A circuit approach of any desired topology can be obtained by applying the mentioned principle from section 2.4.1. As charge is stored in a capacitor, the voltage-capacitance relationship changes, enabling the ideal conversion ratio M of any SC converter topology to be calculated. By means of example using a triple-capacitor system which equals to a converter that divides the input voltage by a factor of three quarters can be seen as:

$$\frac{V_{out}}{V_{in}} = \frac{3q}{4q} = \frac{3}{4} \tag{3.1}$$

With an series-parallel approach both structure's phases must contain an equal amount of energy, therefore:

$$\begin{aligned} 3q &= 4q \\ 3V_{in}C_{fly} &= (1+3)V_{out}C_{fly} \\ 3V_{in}C_{fly} &= V_{out}C_{fly} + 3V_{out}C_{fly} \\ 3C_{fly}(V_{in} - V_{out}) &= V_{out}C_{fly} \end{aligned} \tag{3.2}$$

In the first state, the energy is stored on a parallel connection of $3 \cdot C_{fly} \rightarrow [C_1||C_2||C_3]$ capacitors with $V_{C_{fly}} = V_{in} - V_{out}$, and in the second state the energy is stored in a series structure $3 \cdot C_{fly} \rightarrow [C_1 \oplus C_2 \oplus C_3]$, with $V_{C_{fly}} = V_{out}$:

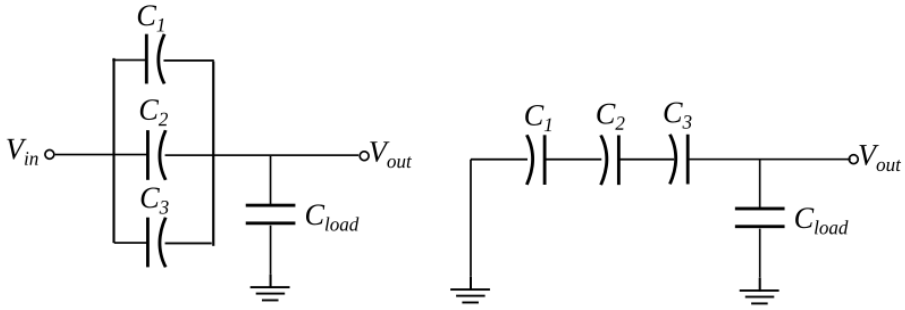


Figure 3.2: Two phased single charge input 4-to-3 converter

$$\phi_1 : Q_{in} = (C_1||C_2||C_3)V_{C_{fly}} = 3C_{fly1-3}(V_{in} - V_{out}) \tag{3.3}$$

$$\phi_2 : Q_{out} = (C_1 \oplus C_2 \oplus C_3)V_{C_{fly}} = C_{fly1-3}V_{out} \tag{3.4}$$

In steady-state, the load decoupling component C_{load} can be taken out of the equation. This shows that a structure of capacitors can achieve a voltage conversion $M = \frac{3}{4}$. However, despite the conservation of energy, a change in voltage across the structure is observed. This approach is only practical if the voltage-capacitance relationship can handle the load decoupling capacitor when applied to the output, as pointed out in [2]. If we assume that C_1, C_2 and C_3 from figure 3.2 is equally sized, then according to KVL the voltage across the capacitors in the parallel connection equals:

$$V_{C1}^{(1)} = V_{C2}^{(1)} = V_{C3}^{(1)} = V_{in} - V_{out} \tag{3.5}$$

and in the series connection, the output voltage is equally shared across each capacitor:

$$V_{C1}^{(2)} + V_{C2}^{(2)} + V_{C3}^{(2)} = V_{out} \tag{3.6}$$

The charge stored in both stages can be written as:

$$Q_{\phi_1} = C_1V_{C1}^{(1)} + C_2V_{C2}^{(1)} + C_3V_{C3}^{(1)} + C_LV_{out} \tag{3.7}$$

$$\begin{aligned} Q_{\phi_2} &= C_1(V_{C1}^{(2)} - 0) + C_2(V_{out} - (V_{C3}^{(2)} + V_{C1}^{(2)}) + C_3(V_{C3}^{(2)}) + C_L V_{out} \\ &= (C_1 - C_2)V_{C1}^{(2)} + C_2 V_{out}^{(2)} + (C_3 - C_2)V_{C3}^{(2)} + C_L V_{out} \end{aligned} \tag{3.8}$$

Substituting equation 3.5 into equation 3.7, this yields 3.9:

$$Q_{\phi_1} = V_{in}(C_1 + C_2 + C_3) + V_{out}(C_1 + C_2 + C_3) + C_L V_{out} \tag{3.9}$$

However, the node voltages in equation 3.6 are unknown and can not be substituted into equation 3.8. Hence, equation 3.6 have to be calculated using KCL when in series connection:

$$i_{c_1} = C_1\frac{dv_{c1}}{dt} = i_{c_2} = C_2\frac{dv_{c2}}{dt} = i_{c_3} = C_3\frac{dv_{c3}}{dt} \tag{3.10}$$

Since each of the capacitors have the same value, it can be stated that:

$$\frac{dv_{c1}}{dt} = \frac{dv_{c2}}{dt} = \frac{dv_{c3}}{dt} \tag{3.11}$$

The rate of change in C_1, C_2 and C_3 is simply the voltage across each capacitor in phase one, subtracted by the voltages across the capacitors in phase two, which yields:

$$\frac{dv_{c1}}{dt} = V_{C1}^{(1)} - V_{C1}^{(2)} \iff (V_{in} - V_{out}) - V_{C1}^{(2)} \tag{3.12}$$

$$\frac{dv_{c2}}{dt} = V_{C2}^{(1)} - V_{C2}^{(2)} \iff (V_{in} - V_{out}) - V_{C2}^{(2)} \tag{3.13}$$

$$\frac{dv_{c3}}{dt} = V_{C3}^{(1)} - V_{C3}^{(2)} \iff (V_{in} - V_{out}) - V_{C3}^{(2)} \tag{3.14}$$

From 3.11 we can see that the relationship between equation 3.12, 3.13 and 3.14 is:

$$V_{C1}^{(2)} = V_{C2}^{(2)} = V_{C3}^{(2)} \tag{3.15}$$

When inserting 3.15 into 3.6, we get that:

$$V_{out} = 3V_{C1}^{(2)} = 3V_{C2}^{(2)} = 3V_{C3}^{(2)} \tag{3.16}$$

Rearranging equation 3.16 and substituting it into 3.8, we see that:

$$Q_{\phi_2} = (C_1 - C_2)\frac{V_{out}}{3} + (C_3 - C_2)\frac{V_{out}}{3} + C_2 V_{out}^{(2)} + C_L V_{out} \tag{3.17}$$

Then, by setting equation 3.17 equal 3.9 according to the laws of charge conservation $Q_{\phi_1} = Q_{\phi_2}$ while simplifying the equation, we get that:

$$V_{in}(C_1 + C_2 + C_3) + C_L V_{out} = \frac{4}{3} V_{out}(C_1 + C_2 + C_3) + C_L V_{out} \iff \frac{V_{out}}{V_{in}} = \frac{3}{4} \quad (3.18)$$

It can be concluded from equation 3.18 that there is a voltage gain of $\frac{3}{4}$ when applying the load decoupling component, assuming lossless components. This technique can however not defend the choice of topology at this stage, as a voltage across a capacitor is accurately given by equation 2.10 adding complexity to the mathematical statement.

3.2.2 Charge Flow Analysis of the Series-Parallel 3/4 Converter

To simplify the process, a circuit approach can also be archived by analysing charge when flowing between capacitors. Applying the technique mentioned in section 2.4.2 allows for more complex circuits without to many differential equations. This will be demonstrated for the following two cases, introducing a new addition never explored as far as the author knows.

Case one: The $M_{i=3} = 3/4$ topology when applied using charge input in a single phase. According to equation 2.15, the charge flow vectors of this scenario are:

$$a_c^{(1)} = \left[\frac{3}{4}, \frac{1}{4}, \frac{1}{4}, \frac{1}{4}, \frac{3}{4}\right] \quad (3.19)$$

$$a_c^{(2)} = \left[\frac{1}{4}, -\frac{1}{4}, -\frac{1}{4}, -\frac{1}{4}, \frac{0}{4}\right] \quad (3.20)$$

The reason for this is based on equation 2.14, which says that $M = \frac{3}{4} + \frac{0}{3} = \frac{3}{4}$ as long as equation 2.16 is satisfied: $\frac{3}{4} + \frac{1}{4} = 1$. Furthermore, $+ = charge$, $- = discharge$ and $0 = off$. Due to KVL, the sum of $a_{c,i}^n$ have to equal zero. A circuit representation for this scenario would look like:

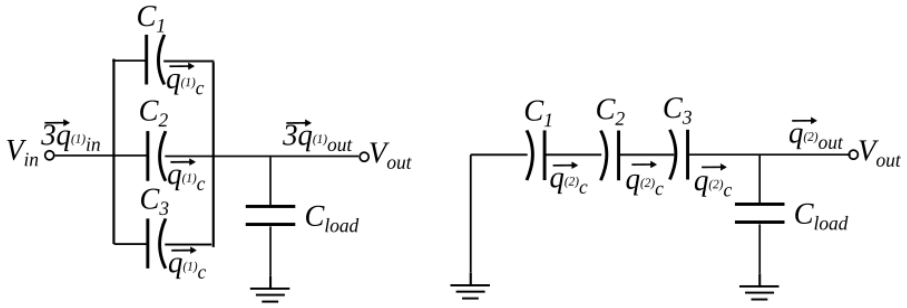


Figure 3.3: Circuit representation showcasing the charge capacitor element $a_c^{(1)}$ to the left when in the charging phase, and $a_c^{(2)}$ to the right in the discharge phase

Figure 3.3 demonstrates how charge from the input node equally spreads out between each capacitor in the charging phase, then cascading to the output node. While in the discharge phase, this charge is transferred to the output node. Note that this result is the same as

for the example given in section 3.2.1. When applied in a switching scheme similar to the one seen in figure 3.7, the resulting resistance element a_r^n would look different than the one which will be shown in case two.

Case two: The $M_{i=3} = 3/4$ topology applying charge input in both phases. The charge flow vectors of this scenario are:

$$a_c^{(1)} = \left[\frac{3}{4}, -\frac{1}{4}, -\frac{1}{4}, -\frac{1}{4}, \frac{2}{4}\right] \tag{3.21}$$

$$a_c^{(2)} = \left[\frac{1}{4}, \frac{1}{4}, \frac{1}{4}, \frac{1}{4}, \frac{1}{4}\right] \tag{3.22}$$

$$a_r^{(1)} = \left[\frac{2}{4}, 0, \frac{1}{4}, 0, \frac{1}{4}, 0, 0, \frac{2}{4}, 0, \frac{1}{4}, 0, 0, 0, \frac{2}{4}\right] \tag{3.23}$$

$$a_r^{(2)} = \left[0, \frac{1}{4}, 0, 0, 0, 0, \frac{1}{4}, 0, \frac{1}{4}, 0, \frac{1}{4}, 0, 0, 0, 0\right] \tag{3.24}$$

The resistance element given in equation 3.23 and 3.24 are determined based on figure 3.7 which has implemented a switching-network based on figure 3.4. In this case, M equals $= \frac{2}{4} + \frac{1}{4} = \frac{3}{4}$ witch is satisfied as $\frac{3}{4} + \frac{1}{4} = 1$.

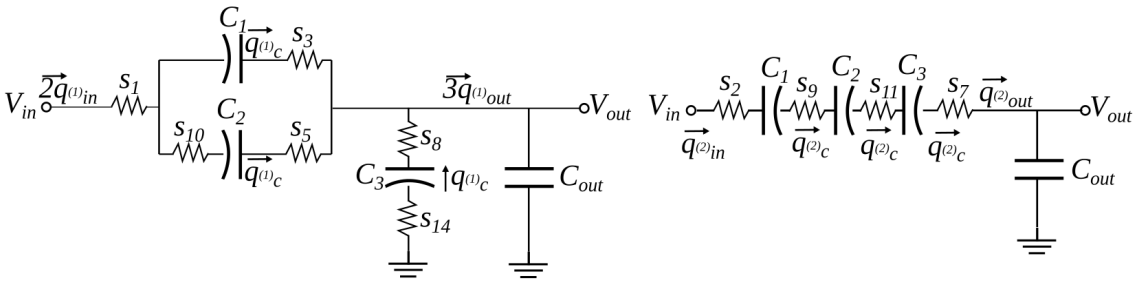


Figure 3.4: $M_3 = 3/4$ topology utilizing charge input in both phases ϕ_1 (left) and ϕ_2 (right). The switch charge vector $a_r^{(1)}$ and $a_r^{(2)}$ both originates from figure 3.7

However strange, according to theory both parallel and series capacitors will transfer the same amount of charge as long as $C_1 = C_2 = C_3$. When comparing case one given in figure 3.3 to case two in figure 3.4, one can observe that V_{in} is applied in both phases. This effectively means that less flying capacitance is needed, thus area on the chip can be saved thereby increasing the power density of the circuit. The switching limits when analysing figure 3.4 are:

$$R_{SSL} = \frac{3}{8}\frac{1}{(C_1 + C_2 + C_3)f_{sw}}$$

$$R_{FSL} = \frac{19}{8}\sum_{k=1}^{10} R_{on,k}$$

3.2.3 Charge Flow Analysis of the Series-Parallel 2/3 Converter

The $M_{i=3} = 2/3$ topology when applying charge input in both phases was first published in [4] (without presenting its charge flow vectors). Note that the fly capacitors polarity should not matter in theory as long as KVL is satisfied. On the other hand, according to [33], this might affect the performance. An analysis of the charge vector yields:

$$a_c^{(1)} = \left[\frac{2}{6}, \frac{1}{6}, \frac{1}{6}, -\frac{2}{6}, \frac{2}{6}\right] \tag{3.25}$$

$$a_c^{(2)} = \left[\frac{4}{6}, -\frac{1}{6}, -\frac{1}{6}, \frac{2}{6}, \frac{2}{6}\right] \tag{3.26}$$

$$a_r^{(1)} = \left[0, \frac{1}{6}, 0, \frac{1}{6}, 0, 0, \frac{2}{6}, 0, 0, \frac{1}{6}, \frac{2}{6}, 0, 0, 0\right] \tag{3.27}$$

$$a_r^{(2)} = \left[0, 0, \frac{1}{6}, 0, \frac{1}{6}, \frac{2}{6}, 0, \frac{2}{6}, 0, 0, 0, \frac{1}{6}, \frac{1}{6}, 0\right] \tag{3.28}$$

Resulting to the circuit shown in figure 3.5.

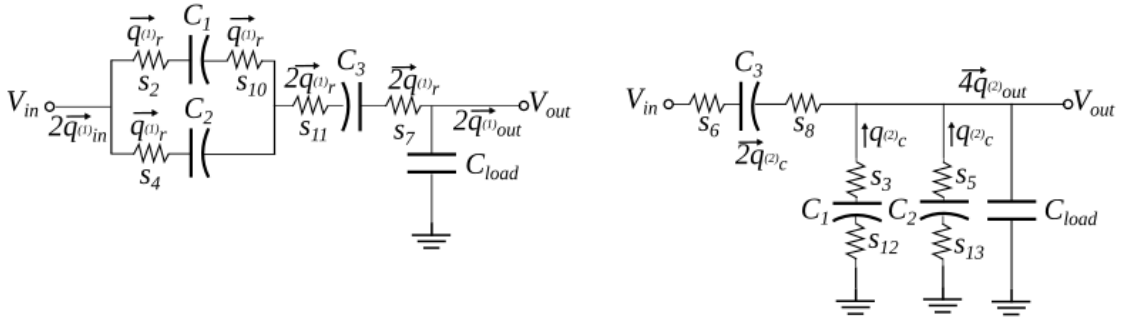


Figure 3.5: $M_3 = 2/3 = 4/6$ topology utilizing charge input in both phases ϕ_1 (left) and ϕ_2 (right). The switch charge vector $a_r^{(1)}$ and $a_r^{(2)}$ both originates from figure 3.7

Which corresponds to:

$$R_{SSL} = \frac{1}{3}\frac{1}{(C_1 + C_2 + C_3)f_{sw}}$$

$$R_{FSL} = \frac{23}{18}\sum_{k=1}^{11} R_{on,k}$$

Approaching the mention circuit using charge balance analysis would yield multiple equations with unspeakably many unknown factors to be solved.

3.2.4 Charge Flow Analysis of the Series-Parallel 4/5 Converter

The $M_{i=3} = 4/5$ topology when applying charge input in both phases originates from [4]. This textbook had a confusing misprint in the charge flow vectors, however, this is corrected in the following equations:

$$a_c^{(1)} = \left[\frac{2}{5}, \frac{1}{5}, \frac{1}{5}, -\frac{2}{5}, \frac{2}{5},\right] \tag{3.29}$$

$$a_c^{(2)} = \left[\frac{3}{5}, -\frac{1}{5}, -\frac{1}{5}, \frac{2}{5}, \frac{2}{5},\right] \tag{3.30}$$

$$a_r^{(1)} = \left[0, \frac{1}{5}, 0, 0, 0, \frac{2}{5}, 0, 0, \frac{2}{5}, \frac{2}{5}, 0, 0, 0\right] \tag{3.31}$$

$$a_r^{(2)} = \left[0, 0, \frac{1}{5}, 0, 0, \frac{2}{5}, 0, \frac{2}{5}, \frac{1}{5}, 0, 0, 0, \frac{1}{5}, 0\right] \tag{3.32}$$

Resulting to the circuit shown in figure 3.6:

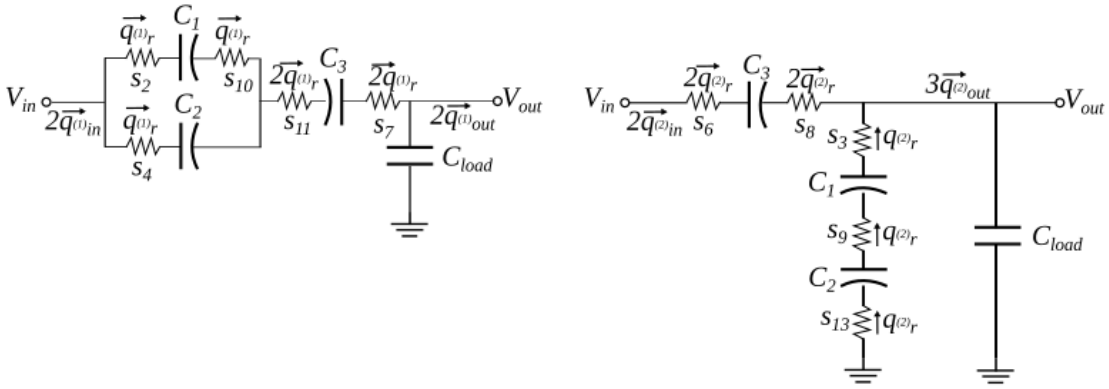


Figure 3.6: $M_3 = 4/5$ topology utilizing charge input in both phases ϕ_1 (left) and ϕ_2 (right). The switch charge vector $a_r^{(1)}$ and $a_r^{(2)}$ both originates from figure 3.7

Which corresponds to:

$$R_{SSL} = \frac{12}{25}\frac{1}{(C_1 + C_2 + C_3)f_{sw}}$$

$$R_{FSL} = \frac{48}{25}\sum_{k=1}^{9} R_{on,k}$$

3.3 Multi-Topology Converter

It is entirely possible to operate each individual circuit in parallel and one must not merge them, but that also means poor utilization of space. Half of the circuit will then not be in use most of the time. Both energy and area can be saved by combining multiple conversion ratios in one and the same circuit. In this thesis the three independent switched-capacitor topologies from the previous sections is selected in order to perform the power conversion between the battery and the load. This combination is visualised in figure 3.7. The 3/4 topology is based on figure 3.4 as to utilise charge input in both phases. The ideal topology are governed by the switching algorithm featured in Table 3.1.

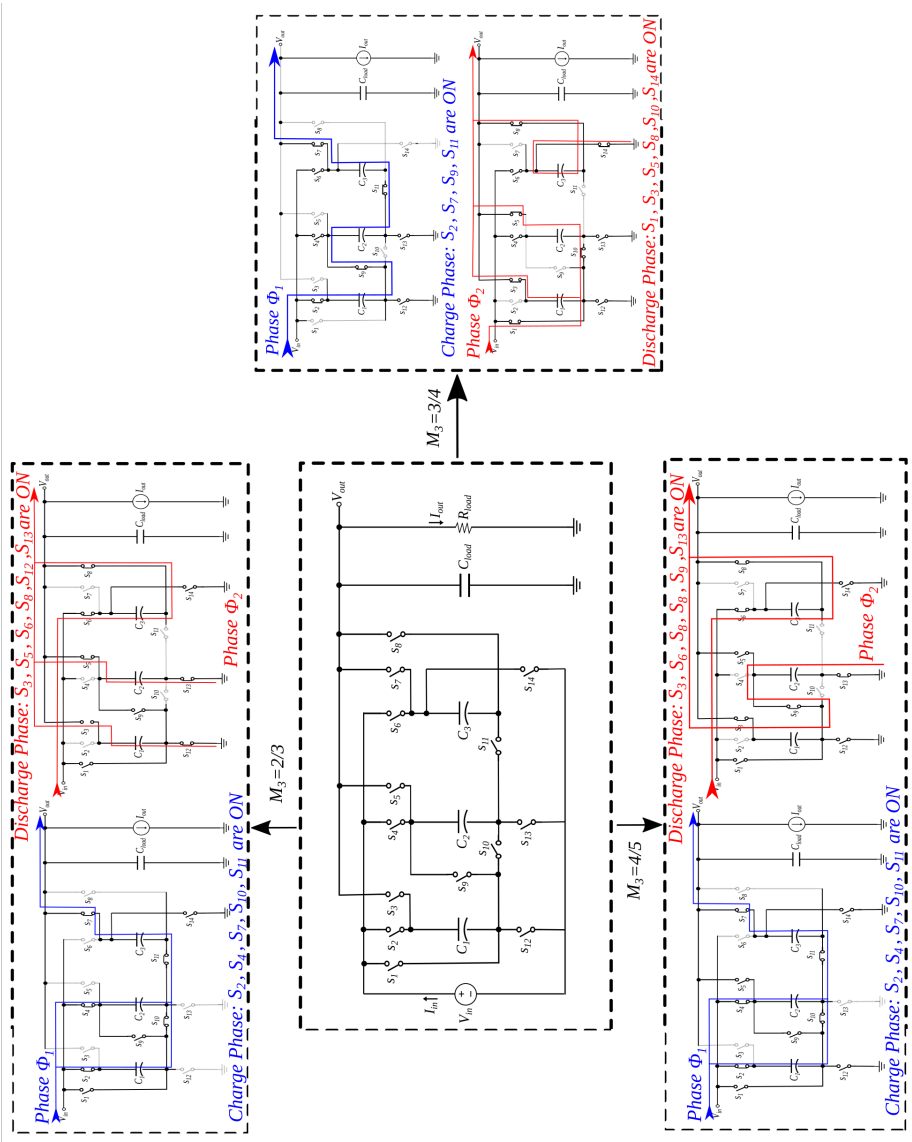


Figure 3.7: Proposed Multi-Topology Converter combining the $\frac{3}{4}$, $\frac{2}{3}$, $\frac{4}{5}$ topologies

Mode	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	S_9	S_{10}	S_{11}	S_{12}	S_{13}	S_{14}
2/3	-	ϕ_1	ϕ_2	ϕ_1	ϕ_2	ϕ_2	ϕ_1	ϕ_2	-	ϕ_1	ϕ_1	ϕ_2	ϕ_2	-
3/4	ϕ_2	ϕ_1	ϕ_2	-	ϕ_2	-	ϕ_1	ϕ_2	ϕ_1	ϕ_2	ϕ_1	-	-	ϕ_2
4/5	-	ϕ_1	ϕ_2	ϕ_1	-	ϕ_2	ϕ_1	ϕ_2	ϕ_2	ϕ_1	ϕ_1	-	ϕ_2	-

Table 3.1: The ideal 3-stages switching algorithm

3.3.1 Flying Capacitors and Transistor Sizing

Switches: Thick-oxide transistors (NMOS and PMOS) is chosen to overcome any breakdown at 3.3V. So, a 5V 28nm technology MOSFET with minimum gate length of 280nm is chosen. This increases the short channel effect and to maximize the source-drain voltage, thus minimize the on-state resistor.

Capacitors: In practice, the output capacitor is often in the same order of magnitude as the flying capacitors [4], but this is not not a limitation. However, the load capacitor have to be greater then the sum of flying capacitors [3], actually it should be much larger, hence eliminating the ripple at the output node. İn this particular case there is a 47 μF load capacitor outside the SC circuit, and in normal operation the load only pulls about 10 μA. This means that only a small amount of charge has to pass through the SC circuit. It should be noted that the floating capacitors should have identical charge coefficients as recommended in [46], thus gaining the same SSL and FSL impedances. An estimated value of the flying capacitor can be derived from equation 2.31. The worst case scenario for each topology will decide the minimum value as the same flying capacitors are shared among the three SC topologies:

$$C_{3.0V} = \frac{10\mu A}{(3.0V - \frac{2}{3} \cdot 3.0V) \cdot 1MHz} = 10.0pF \tag{3.33}$$

$$C_{2.7V} = \frac{10\mu A}{(2.7V - \frac{3}{4} \cdot 2.7V) \cdot 1MHz} = 14.8pF \tag{3.34}$$

$$C_{2.4V} = \frac{10\mu A}{(2.4V - \frac{4}{5} \cdot 2.4V) \cdot 1MHz} = 20.8pF \tag{3.35}$$

Equation 3.35 shows that the smallest value for the charge transfer capacitor is 20.8 pF in order to deliver a minimum 10 μA to the load capacitor, assuming no losses. Only three MOM capacitors are available in the technology, and no MIM. The most suitable capacitor is a hexa-layered MOM, with a maximum value of 10.867 pF when occupying $60\mu m \cdot 60\mu m = 3600\mu m^2$.

3.3.2 Area Estimation

To estimate area consumption, some initial calculation is done. Equation 3.35 requires a minimum of two MOM capacitors, and there is three flying caps in total. In addition, 14 dummy capacitors are used to surround the circuit to optimize matching. This means a total of 72000 μm^2 is required by the capacitors. As a rough starting point, 85% of the area is estimated to be contributed to the capacitors. This increases the total area to

approximately 82800 μm^2. Equation 2.8 makes it possible to estimate the power density for a given area:

$$\rho_{exp} = \frac{18\mu W}{82800\mu m^2} = 217.4\mu W/mm^2 \tag{3.36}$$

3.3.3 Circuit Diagram

The ideal switching network given in figure 3.7 is implemented according to figure 3.8. There are 11 PMOS an 3 NMOS switches and 3 MOM capacitors in the network. All PMOSs bulk connections are connected to V_{in}, and GND for the NMOSs.

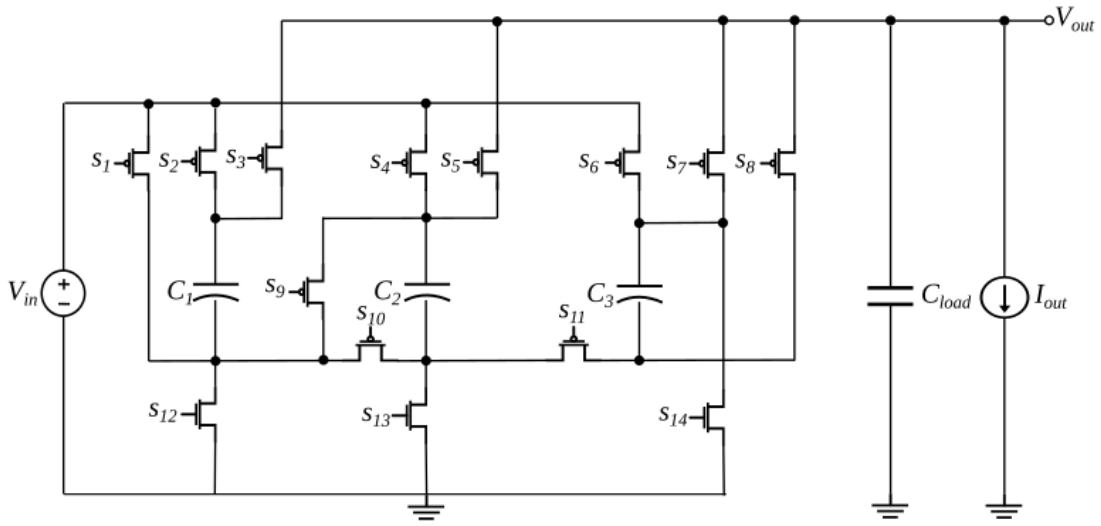


Figure 3.8: Multi-Topology scheme

A trial and error method have led to implementation of the MOS-switches. However, NMOS are generally used for switches connected to ground, hence switch 12, 13 and 14. And PMOS generally connected to the highest voltage source, hence switch 1, 2, 4 and 6. Switches 3, 5, 7, 8, 10 and 11 where implemented with transmission gates, and gradually replaced with PMOS switches. The switch state algorithm given in Table 3.1 has to be converted into a table suitable for MOSFET implementation. All implemented PMOS switches have inverted signals as the polarity of the gate voltage is opposite of that of an NMOS. The clock signals driving each switch is listed in Table 3.2.

Mode	P_1	P_2	P_3	P_4	P_5	P_6	P_7	P_8	P_9	P_{10}	P_{11}	N_{12}	N_{13}	N_{14}
2/3	Vin	$\phi_{1_{inv}}$	$\phi_{2_{inv}}$	$\phi_{1_{inv}}$	$\phi_{2_{inv}}$	$\phi_{2_{inv}}$	$\phi_{1_{inv}}$	$\phi_{2_{inv}}$	Vin	$\phi_{1_{inv}}$	$\phi_{1_{inv}}$	ϕ_2	ϕ_2	GND
3/4	$\phi_{2_{inv}}$	$\phi_{1_{inv}}$	$\phi_{2_{inv}}$	Vin	$\phi_{2_{inv}}$	Vin	$\phi_{1_{inv}}$	$\phi_{2_{inv}}$	$\phi_{1_{inv}}$	$\phi_{2_{inv}}$	$\phi_{1_{inv}}$	GND	GND	ϕ_2
4/5	Vin	$\phi_{1_{inv}}$	$\phi_{2_{inv}}$	$\phi_{1_{inv}}$	Vin	$\phi_{2_{inv}}$	$\phi_{1_{inv}}$	$\phi_{2_{inv}}$	$\phi_{2_{inv}}$	$\phi_{1_{inv}}$	$\phi_{1_{inv}}$	GND	ϕ_2	GND

Table 3.2: Multistage implemented switch logic algorithm

3.4 Layout

A layout synthesis of the multi-topology scheme using a common centroid layout method [24] is shown in figure 3.10. The 2 x MOM x $3C_{fly}$ prototype is symmetrically centered around a common geometric point to minimize area consumption as shown in figure 3.9. Additional 14 dummy capacitors encapsulate the flying capacitors to improve matching. Each flying capacitor lies from layer 1 to 6 to achieve the required charge capacity, while each dummy capacitor is designed from layer 2 to 6 for accessibility. It is not routed on a ground plane in order to avoid further parasitic losses. Every MOS-switch is doubled since it is good practice to operate with even numbers when designing a layout. The total occupied area is here 247 μm x 380 μm = 93860 μm^2.

D	D	D	D	D
D	C_2	C_1	C_3	D
D	C_3	C_1	C_2	D
D	D	D	D	D

Figure 3.9: Common Centroid Layout

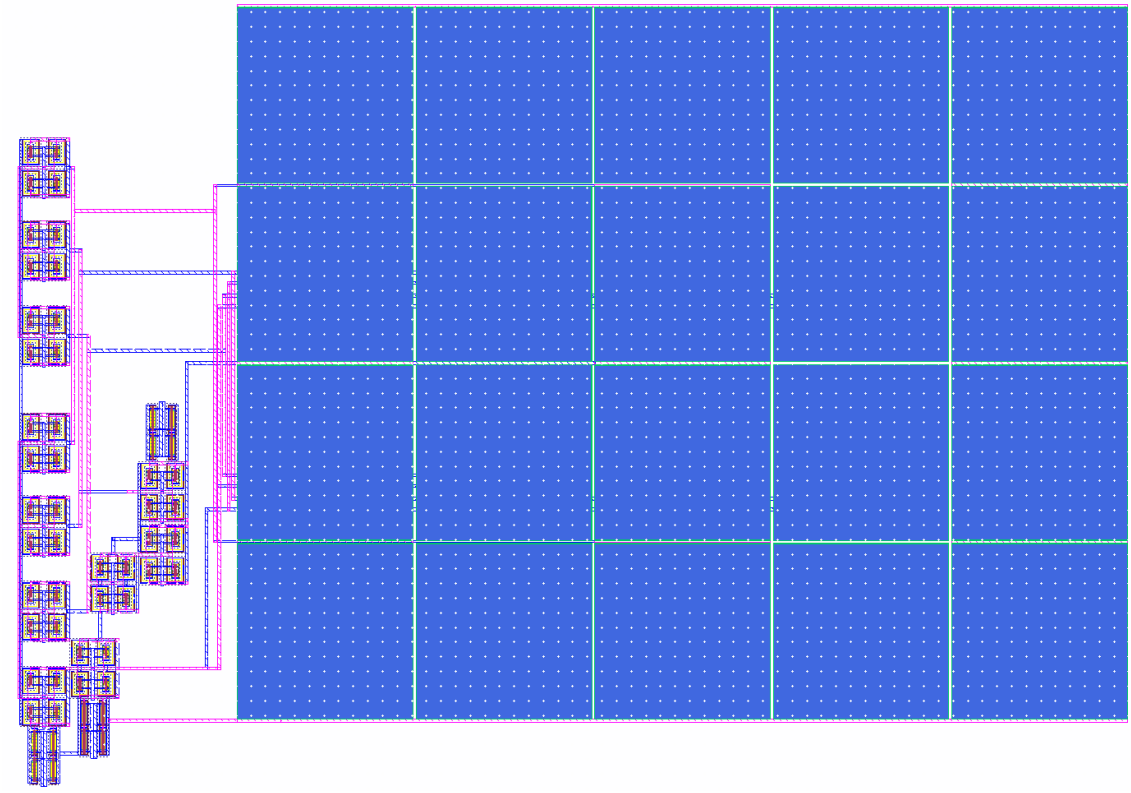


Figure 3.10: Converter Block Layout

CHAPTER

FOUR

CONTROL BLOCK

Implementation of the control block structure is introduces in this chapter. Due to limited time, the layout of the control block was not prioritized. The final design is featured in figure 4.1. This control block contains of a modulation controller as a topology selector with a PFM function using clock gating. The purpose of this chapter is to give a detailed description of the converter's control techniques and how to implement this as an integrated power management system. Each of the modules will be explained one-by-one based on their related functions and priority. This expansion is intended to give the reader an understanding of why each module is important and what role each module plays in order to fulfill the goal of of minimising the system's power consumption.

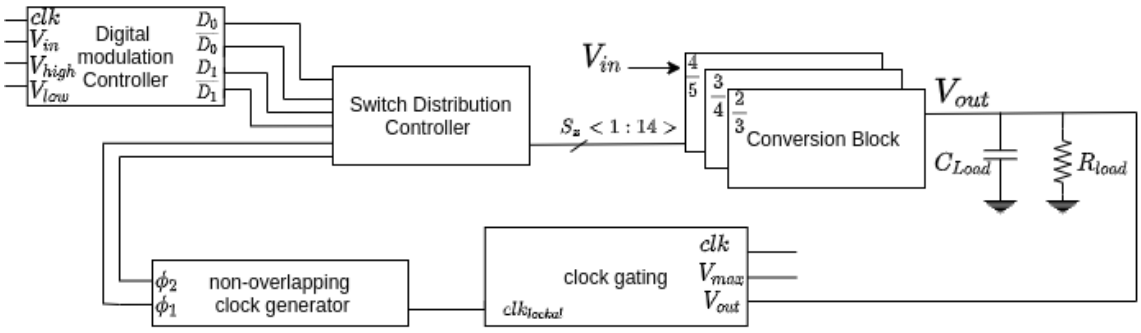


Figure 4.1: Block visualisation of the control block as a cascaded connection

4.1 Control Method

An overview of the control functions is presented in figure 4.2 using a flow diagram. Each set of functions are implemented in order to control the conversion block efficiently. The function can be described as follows: A digital modulation controller is implemented as the lithium battery gradually decays from 3.3 V and eventually dies at 2.4 V. The digital modulation module compares the input voltage of the battery to two reference voltages at 3.0 V and 2.7 V. Then, based on the comparison, outputs two digital bits D_0 and D_1. These two digital signals are sent to a switch distribution controller which in turn outputs the corresponding non-inverting clock signals ϕ_1 and ϕ_2 to each of the MOS-switches. If the output voltage of the converter block goes above the maximum allowed output of 1.8 V+25 mV, then the clock gating modules will engage turning off the global clock until the output voltage falls below the minimum allowed output of 1.8 V−25 mV, thereon repeating the sequence.

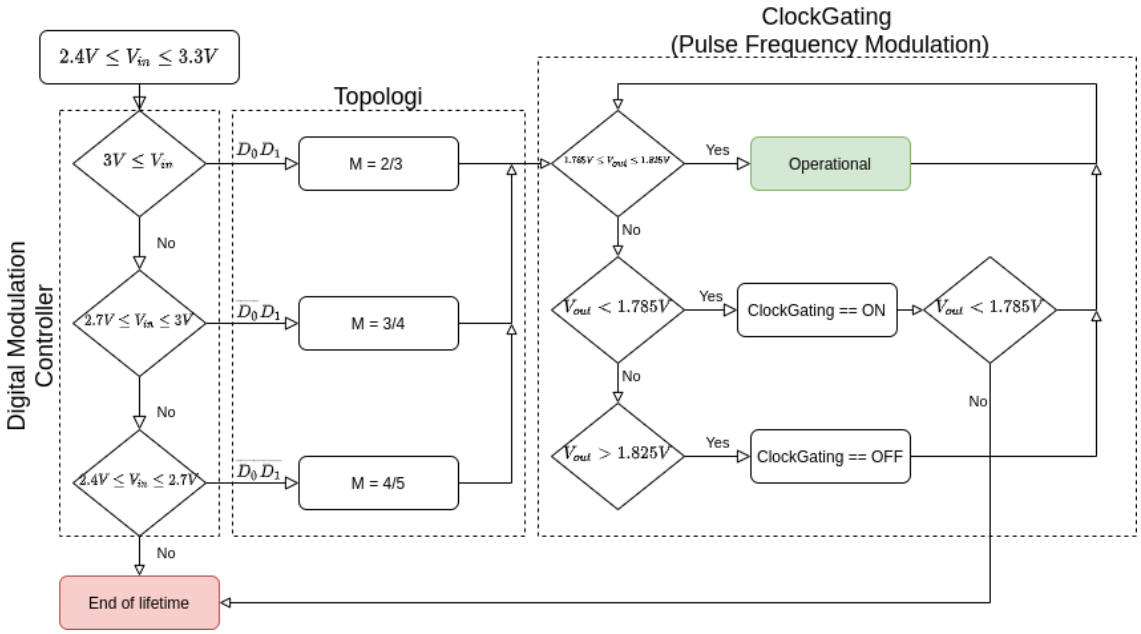


Figure 4.2: Flow Diagram of the systems control functions

4.2 Clock Gating

The clock gating module shown in figure **??** is achieved by implementing a single bond hysteretic feedback controller. The one-boundary hysteretic configuration employs only one comparator for the feedback controller to compare the output voltage with the reference voltage V_{max}. The controller provides switching control signals to the converter in phase with the input clock by outputting a local clock-signal clk_{local}. This module is based on a circuit mentioned in [3], but improved for this specific thesis in order to save energy by implementing a Low-Power High-Speed Charge-Steering based StrongARM Comperator. The Low-Power High-Speed Charge-Steering based StrongARM Comperator was first proposed in [1] as a power saving implementation of a conventional based strongArm comparator clock comparator. In this circuit, a capacitor C_T is added to avoid that energy

is not leaking to ground in each clock cycle.

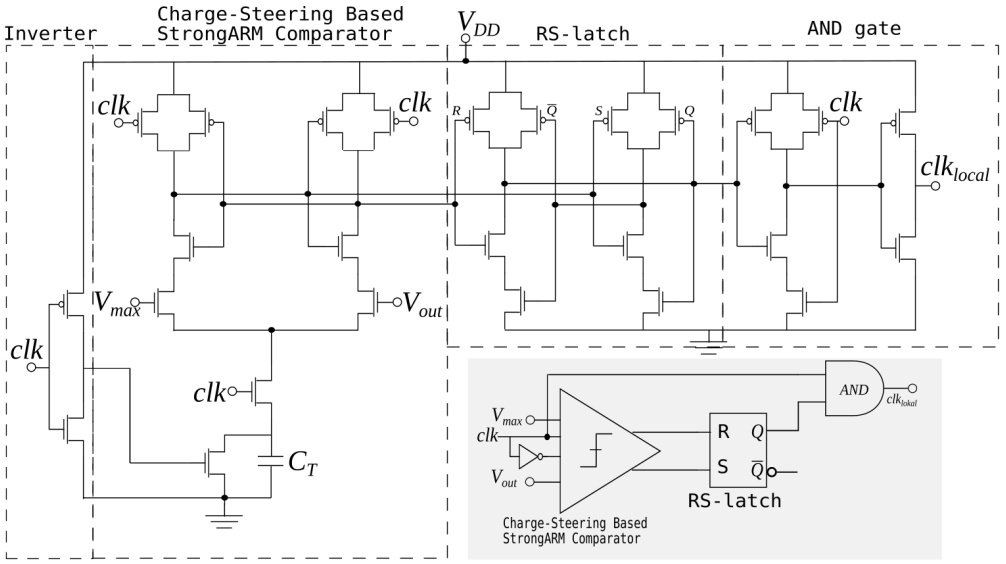


Figure 4.3: Transistor level Pulse Frequency Modulation circuit implemented using a single hysteretic feedback controller circuit. This is the first ever adapted Charge-Steering based strongARM cooperator used in PFM circuit

4.2.1 Non-overlapping clock

Both clock phases, as well as their inverted part, is archived by designing a ring-oscillation non-overlapping circuit. This action is implemented in this thesis as shown in figure 4.4. Each NAND gate adds a latency to the phase. Without enough delay, some switches may turn on simultaneously. If both phases, ϕ_1 and ϕ_2, turns on simultaneously, then either the charge will flow from the input terminal to ground via the transistor-switches, trying to equalize the source, or the charge will flow to the output terminal, thus uncontrollably short circuiting the load. The outcome would be a power-loss as heat builds up in the transistors due to the small resistance in it. The clock's phase-shift given in Table 3.2 is illustrated in figure 4.8.

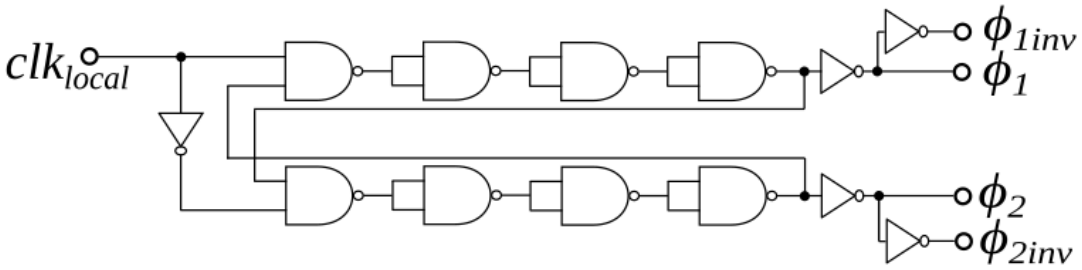


Figure 4.4: Non-overlapping clock, implemented with 2x4 logic NAND gates and 2x2 Inverters

4.3 Digital modulation controller

A feed-forward controller can be implemented in order to transit between multiple topologies. The feedforward controller module consist of one clocked strongArm comparator, combined with an RS-latch for each 2^n digital output bit. Because there are three topologies, a minimum of two digital outputs have to be implemented. In this case, D_0 is set to V_{in}, representing a digital '1' when the input voltage is larger than $V_{low} = 2.7V$, else it is equal to ground as a digital zero '0'. For the second digital output D_1, this function is opposite at $V_{high} = 3.0V$. Combination of the two stages represents a double output with three different outcomes. The implemented RS-latch does not allow a case where $D_x = \overline{D_x}$. A circuit implementation of the modulation controller combined with an equivalent circuit is displayed in figure 4.5.

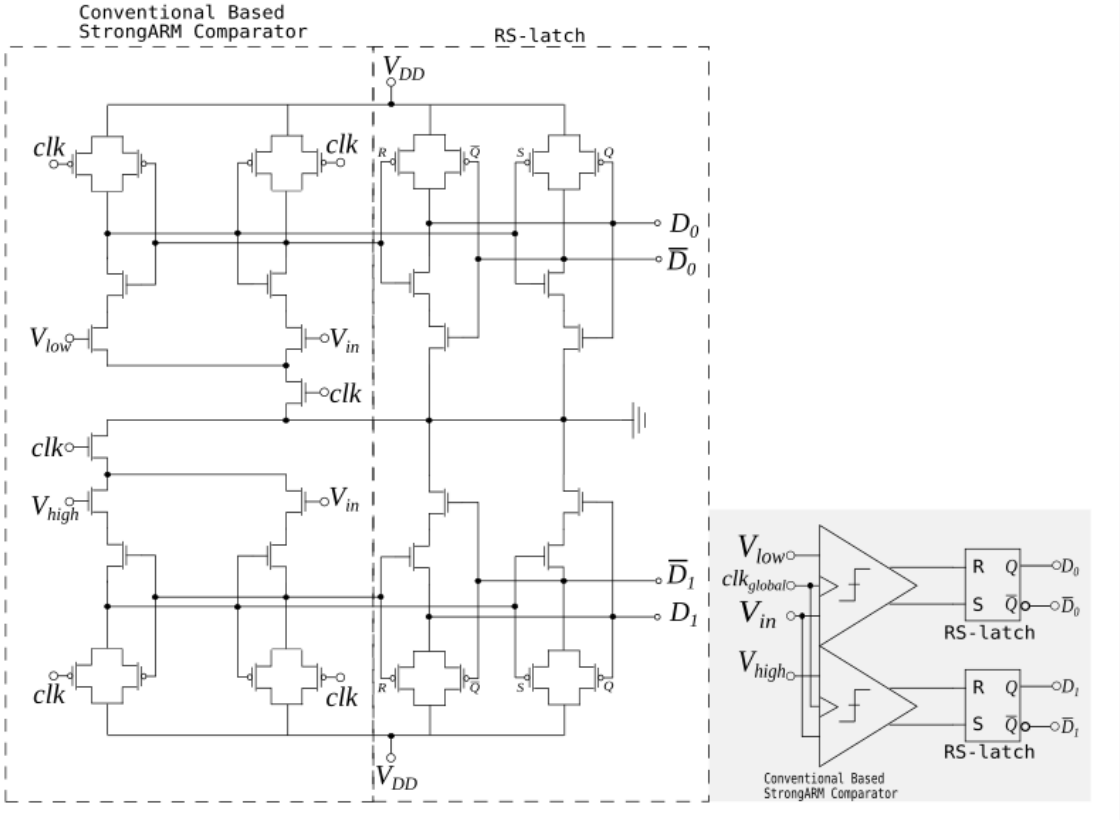


Figure 4.5: Digital modulation using a double feedforward controller.

A list of modes and digital outputs compared to the input domain is given in Table 4.1.

Mode	D_0D_1	V_{in}
2/3	11	3.0 - 3.3
3/4	01	2.7 - 3.0
4/5	00	2.4 - 2.7

Table 4.1: Topologies and inputs

4.4 Switch Distribution Controller

The Switch Distribution Controller's function is to make sure that the correct control signal reaches the switches that will perform the voltage regulation in all stages of it's operation. In the conversion block, 14 MOS-switches is utilizes in order to achieve both states for each of the three topologies. These topologies are governed by the digital input D_0D_1 as shown in Table 4.1. By using Table 3.2 as a truth-table, then each switch can be controlled by implementing logic gates. Unfortunately, the 28nm technology did not contain any digital library, so all digital logic gates such as AND, NAND, OR, NOR, XOR, XNOR, INV, SR-Latch as well as the Strongarm-Latch had to be implemented by the author as shown in appendix D.1. One operation will be shown as an example using switch S_{13}, where the following Boolean expression will satisfy the needs:

$$\begin{aligned} N_{13} &= \overline{((D_0\overline{D_1}) + (\overline{D_0}D_1)}\phi_2 \\ &= ((D_0 \text{ AND } \overline{D_1}) \text{ NOR } (\overline{D_0} \text{ AND } D_1)) \text{ AND } \phi_2 \end{aligned} \tag{4.1}$$

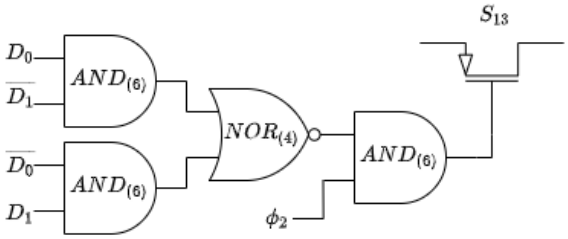


Figure 4.6: Logic gate diagram for switch S_{13} based on equation 4.1

It is possible to look at ways of simplifying equation 4.1 using equation 2.38 since the inverted signals is readily available in order to minimise the use of transistors needed in the control circuit. As the inverted signals already are available, two inverters are not required, and we save four transistors, thus some power. In the case of switch 13, a simplification can be written as:

$$\begin{aligned} N_{13} &= \overline{\overline{D_0}D_1 + \phi_{2_{inv}}} \\ &= (\overline{D_0} \text{ NAND } D_1) \text{ NOR } \phi_{2_{inv}} \end{aligned} \tag{4.2}$$

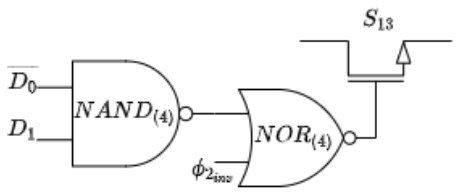


Figure 4.7: Logic gate diagram for switch S_{13} based on equation 4.2

The logic gates featured in figure 4.6 equals a total of 24 transistors, while the logic in figure 4.7 counts to only 8 transistors, which is a reduction of 67%. Table 4.2 list all the implemented logic gates for the nine different cases mentioned in Table 3.2. The timing diagram in figure 4.8 illustrates how the switching sequence is preserved in the logic gates through its life cycle. It is important to notice that $\phi_{1_{inv}} = \overline{\phi_1} \neq \phi_2$ due to the small delay which is visualized in the timing diagram in figure 4.8.

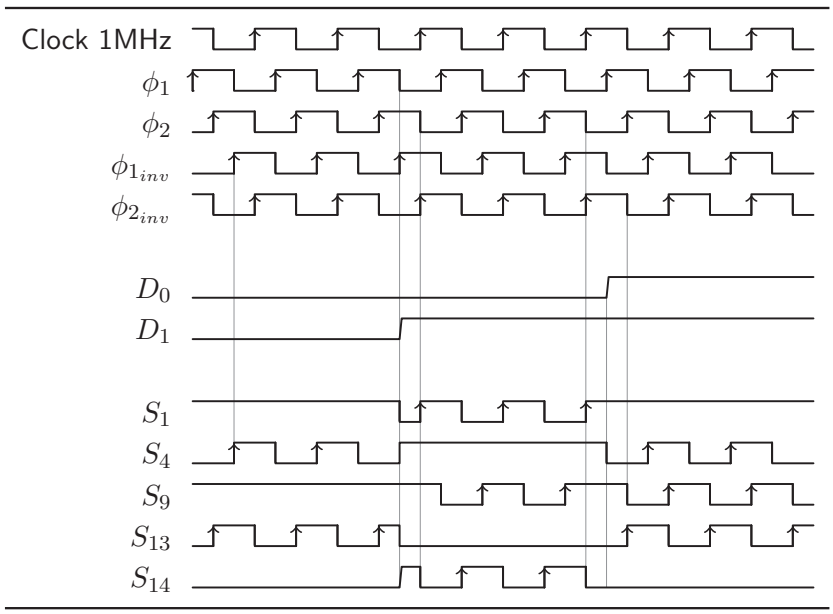


Figure 4.8: Timing diagram showcasing a selected five out of fourteen switches. This timing diagram illustrates the delay and inversion of both phases ϕ_1 and ϕ_2. *Figure is not to scale.

By applying the rules of absorption, involution, the associative function and De Morgans law, all of the Boolean expressions given in Table 4.2 can be simplified. Hence, the overall use of transistors is minimized thus saving both power and area.

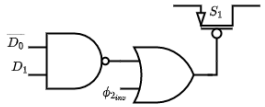
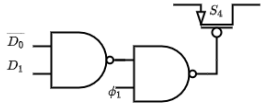
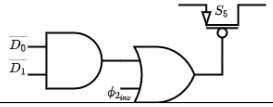
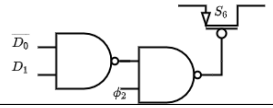
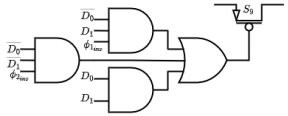
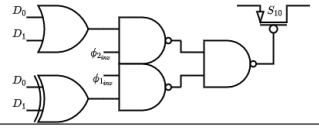
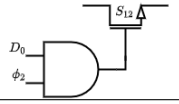
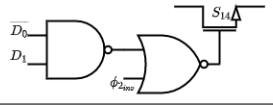
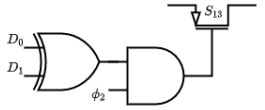
Switch nr	Function	Boolean Algebra	Critical Path
S_1	$= \phi_{2_{inv}} + \overline{D_1 \overline{D_0}}$	$= \phi_{2_{inv}} + (D_1 \uparrow \overline{D_0})$	
S_4	$= \overline{\phi_1 \overline{D_1 \overline{D_0}}}$	$= \phi_1 \uparrow (D_1 \uparrow \overline{D_0})$	
S_5	$= \phi_{2_{inv}} + \overline{D_1 D_0}$	$= \phi_{2_{inv}} + (D_1 \cdot D_0)$	
S_6	$= \phi_{2_{inv}} + D_1 \overline{D_0}$	$= \phi_2 \uparrow (D_1 \uparrow \overline{D_0})$	
S_9	$= \phi_{1_{inv}}(D_1 \overline{D_0}) + \phi_{2_{inv}}(\overline{D_1 D_0}) + (D_1 D_0)$	$= (\phi_{1_{inv}} \cdot D_1 \cdot \overline{D_0}) + (\phi_{2_{inv}} \cdot \overline{D_1} \cdot \overline{D_0}) + (\overline{D_1} \uparrow \overline{D_0})$	
S_{10}	$= \phi_{2_{inv}}((D_1 \overline{D_0}) + (\overline{D_1} D_0)) + \phi_{1_{inv}} \overline{((D_1 \overline{D_0}) + (\overline{D_1} D_0))}$	$= (\phi_{2_{inv}} \uparrow (D_1 \oplus D_0)) \uparrow (\phi_{1_{inv}} \uparrow (D_1 \overline{\oplus} D_0))$	
S_{12}	$= D_0 \phi_2$	$= D_0 \cdot \phi_2$	
S_{13}	$= \overline{((D_0 \overline{D_1}) + (\overline{D_0} D_1))} \phi_2$	$= (D_1 \uparrow \overline{D_0}) \downarrow \phi_{2_{inv}}$	
S_{14}	$= ((D_0 \overline{D_1}) + (\overline{D_0} D_1)) \phi_2$	$= (D_1 \overline{\oplus} D_0) \cdot \phi_2$	

Table 4.2: $\cdot$ = AND, $+$ = OR, $\oplus$ = XOR, $\overline{\oplus}$ = XNOR, $\uparrow$ = NAND, $\downarrow$ = NOR

CHAPTER

FIVE

RESULT

This chapter presents the pre-layout simulation of the entire on-chip voltage regulator scheme featured in figure 4.1. No post-layout results will be presented due to time spent on troubleshooting and multiple iterations until the project deadline, which is also reflected in the results. When the results are presented, some directly considerations will be commented. More general and elaborate discussions of the work carried out in this thesis are presented in chapter 6. The aim of this chapter is to verify the decisions made, and not to search for optimal component values.

5.1 Testing methodology

In this thesis every single module for the proposed design was implemented at transistor level with transistor-models using the university's available 28nm CMOS technology library. An overview of the transistors sizes and other parameters used in the proposed design are listed in Table A.1 for the static design variables, and Table A.2 for the varying design variables. Data presented in this chapter originates from transient simulations preformed using the Cadence Virtuoso software when swiping different input variables. Choices of all the selected variables mentioned in Table A.2 will be explained according to the section's experiment. The converter block is implemented as shown in figure 3.8 unless specified otherwise.

Moreover, only the length for the thick-oxide transistor is considered since the width of the transistor is fixed in this technology. The gate lengths of the switches will be set to the shortest possible value in order to reduce gate capacitance and thereby gate-drive losses. Both the transistor on-state resistance and the performance of the charge transfer capacitor depends on several parameters and are nonlinear with voltage and temperature. Although the nonlinear temperature factor plays a role, it is disregarded in this thesis. Simulations are only based on a room-temperature of 27 degrees Celsius in order to simplify the process. The source voltage V_{DD} will be considered equal to V_{in} as there are no other available sources than the onboard WSN battery.

The design target is to archive an output voltage between 1.785V and 1.825V by regulating an expected output voltage varying from $3.3V \cdot \frac{2}{3} = 2.2V$ to $2.4 \cdot \frac{4}{5} = 1.92V$, while aiming for minimal losses.

5.1.1 Steady-state

The first and most important criterion is to verify the three conversion ratios of the conversion-block. If this condition is not met then there is no need for further testing. Verification can be done by performing an steady-state simulation on the conversion block. That is, to achieve saturation of the load capacitor. When no load-current is applied, the output voltage should stabilize at a constant output value when the load capacitor is fully charged, as according to equation 2.2. In steady-state, there are no impedance checks, and therefore no need to simulate with a large load capacitor. In order to save hours of simulation time, the load capacitor is lowered to 47pF and the initial output voltage is set to start at 1.8V. The transfer capacitor value for $C_{fly} = C_1 = C_2 = C_3$ is based on calculation given in section 3.3.1. This test was performed for all three VCRs, $M = \frac{4}{5}|^{Vin=2.6V}_{Vin=2.4V}$, $= \frac{3}{4}|^{Vin=2.9V}_{Vin=2.7V}$, $= \frac{2}{3}|^{Vin=3.3V}_{Vin=3.0V}$, and the result are displayed in figure 5.1.

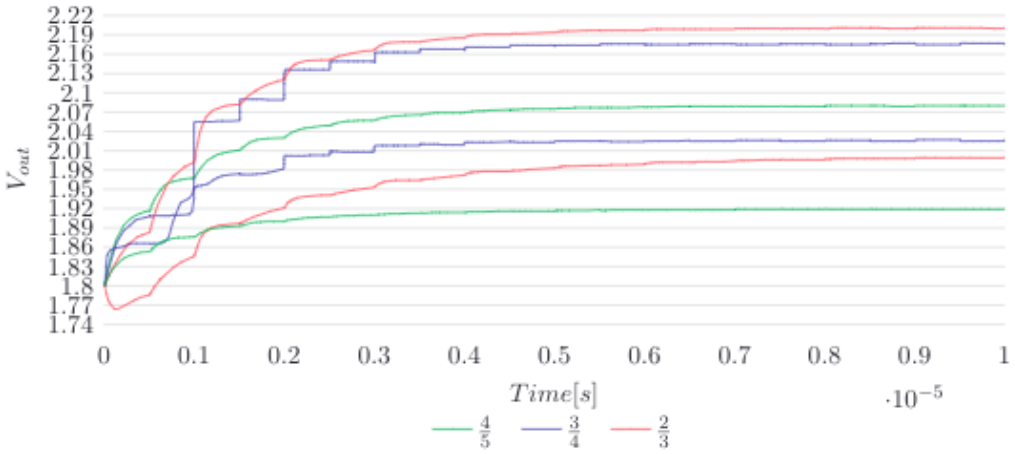


Figure 5.1: Maximum and minimum V_{out} values for each topology during steady-state

Simulation results from figure 5.1 is summarised and displayed in Table 5.1.

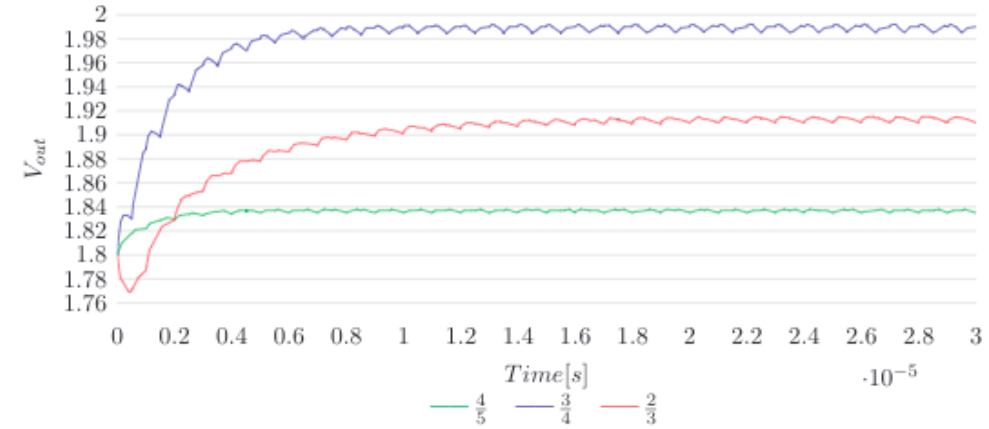
Table 5.1: Recapitulation of figure 5.1

V_{in}	Mode	MV_{in}	γMV_{in}	Deviation
2.4V	4/5	1.920V	1.919V	0.5%
2.6V	4/5	2.080V	2.080V	0%
2.7V	3/4	2.025V	2.026V	0.5%
2.9V	3/4	2.175V	2.175V	0%
3.0V	2/3	2.000V	1.998V	1%
3.3V	2/3	2.200V	2.200V	0%

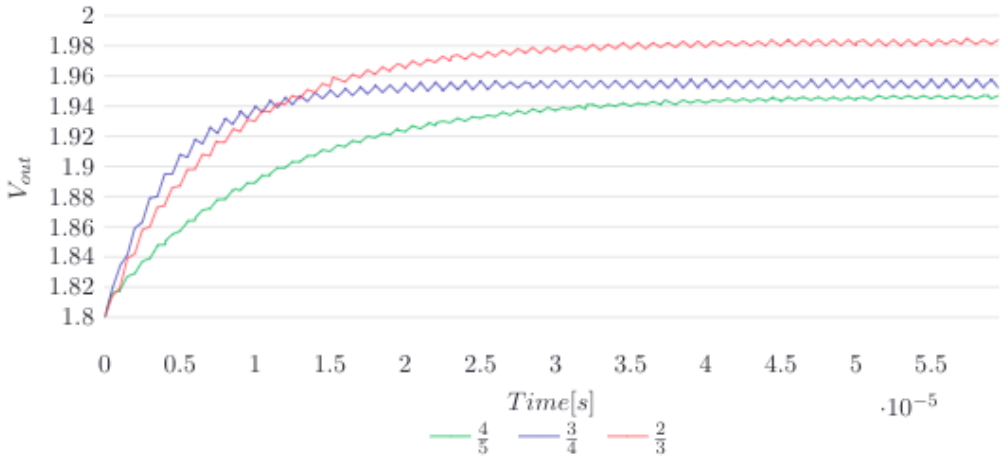
The results displayed in Table 5.1 clearly indicates that the VCRs are achieved with 100% accuracy for all the high input voltages, and 99 - 99.5% accuracy for the low input voltages. The small voltage-drop at low inputs indicates that this is the worst case scenario, and therefore this will be the starting point for further testing.

5.1.2 Load requirements

Introducing a load to the system should reveal any weaknesses in the converter. Further testing was therefore carried out as indicated in Table A.2, and plotted in figure 5.2. This test was performed for each of the topologies when exposed to the maximum load current of 10 μA, with the same input variables as in figure 5.1. The load capacitor was set to 470 pF as a compromise of minimising ripple and charging time, as 47 μF would stabilise at the same output value with less ripple at some point. Simulation of the worst case scenario at low inputs is presented in figure 5.2a, while high inputs is presented in figure 5.2b. This simulation reveals the true voltage drop $V_{loss|real}$ mentioned in equation 2.19, meaning a quantity of R_{out} can be calculated using equation 2.21.



(a) Voltage droop for lowest input scenario applying $I_{out} = 10\mu A$ in each topology.



(b) Voltage droop for highest input scenario applying $I_{out} = 10\mu A$ in each topology.

Figure 5.2: Output Voltage Requirements

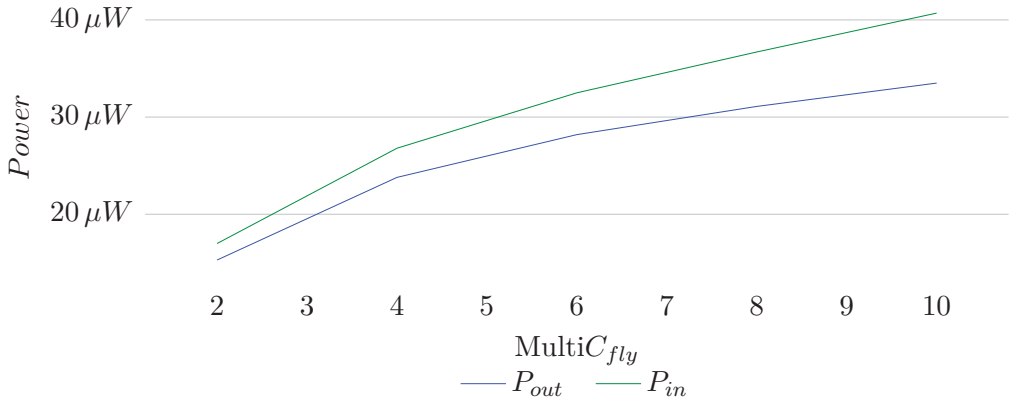
A magnified perspective of figure 5.2a is displayed in figure B.1, showing that charging in both phases is achieved when applying a 2.4 V input. More data based on figure 5.2 is presented in Table 5.2. This data will be discussed in chapter 6.

Table 5.2: Recapitulation of figure 5.2

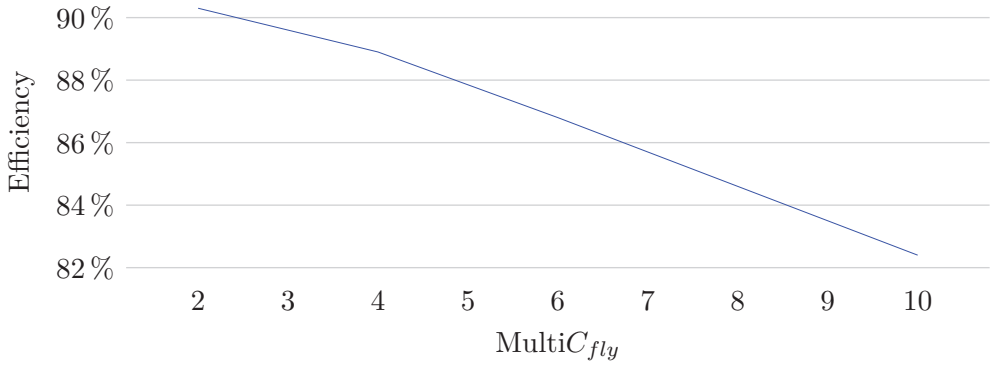
V_{in}	Mode	MV_{in}	γMV_{in}	Deviation	$V_{loss\|real}$	$R_{out\|real}$	V_{ripple}
2.4V	4/5	1.92V	1.837V	4.32%	83mV	$8.2K\Omega$	2mV
2.7V	4/5	2.16V	1.944V	10.0%	214mV	$21.4K\Omega$	3mV
2.7V	3/4	2.025V	1.985V	1.97%	40mV	$4.0K\Omega$	14mV
3.0V	3/4	2.25V	1.957V	16.4%	293mV	$29.3K\Omega$	5mV
3.0V	2/3	2.0V	1.914V	4.30%	86mV	$8.6K\Omega$	5mV
3.3V	2/3	2.2V	1.982V	9.91%	220mV	$22.0K\Omega$	3mV

5.1.3 Capacitor Scaling

It can be seen in Table A.2 that most of the simulations have an increased multiplier of both capacitors and the MOS-switches with a factor of 3, this was done in order to stabilise the output voltage so to stay within the given parameters. This will affect the overall performance of the DC-DC converter and contribute to an increased area occupation. In figure 5.3, the multiplier of the capacitor is swiped from 2 to 10 at 2.4V. This shows how the efficiency decreases, as the gap between the input power deviates from the output power. Implications of this scaling will be elaborated in the next chapter.



(a) Exponential power consumption of increasing flying capacitors



(b) Decreasing efficiency relationship

Figure 5.3: Side effects of scaling flying capacitors

5.1.4 Switching Resistance

The efficiency-resistance relationship is heavily based on the CMOS technology. It is therefore important to investigate the changes in resistance as a function of applied voltages. A test bench for a transmission-gate was used to collect the most approximate data as NMOS and PMOS behaves differently. The same width and length were applied to both of the MOSFETs. The result is plotted in figure 5.4 with two different multipliers.

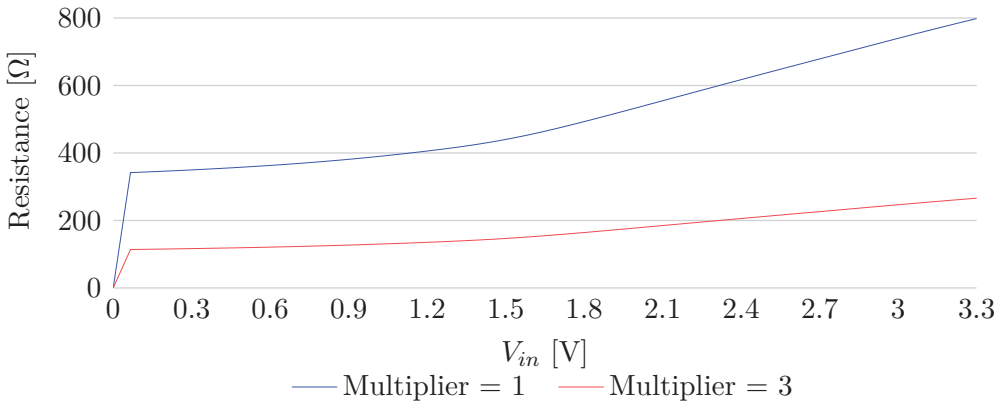


Figure 5.4: On-resistance relationship as a function of input voltage

The resistance in a transistor is non-linear with change in gate-voltages and temperature, it can therefore be expected a non-linear efficiency.

5.2 Pulse Frequency Modulation

The absolute minimum amount for $V_{out|real}$ is still above the allowed maximum of $1.825V$ according to Table 5.2. In order to overcome this problem, a regulation scheme was proposed in section 4.2, which intended to shut off the system clock when the output voltage increases above a reference voltage $V_{max} = 1.81V$. This function is simulated and shown in figure 5.5.

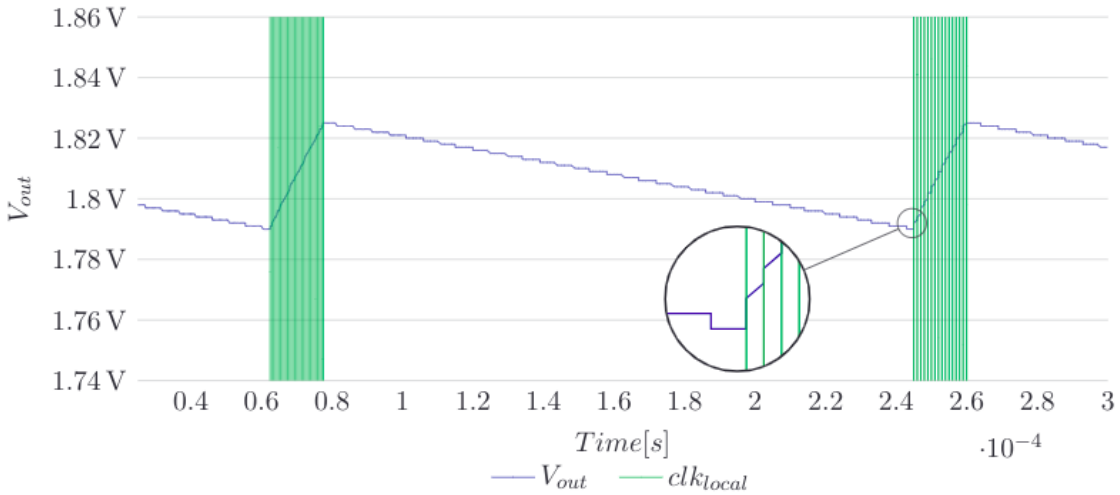


Figure 5.5: Clock Gating simulation preforming the PFM sequence

This simulation was only partially successfully. Ideally the local clock should shut down exactly at 1.81V and recharge at the first rising clock below 1.8V. From a Monte Carlo simulation of the clock gating circuit, it was discovered that this circuit had an accuracy span of 30mV. This was exploited to the fullest, meaning a range from $1.81 \pm 15mV$ could

be archived. In this case, the maximum point was measured to be at 1.824V ($t = 260\mu s$) and minimum at 1.792V ($t = 60\mu s$). This discrepancy seems to relate to the Charge-Steering based strongARM. Implementation of the Charge-Steering strongARM was also attempted in the digital modulation controller, but proved to be unstable and not reliable. The energy saved was marginal, but the outcome was proven to be useful.

5.3 Multi-Topology Efficiency

Figure 5.6 presents the achieved efficiency of the entire lifespan for both the triple topology featured in figure 3.7 and a double topology attached in appendix figure C.1. The efficiency of the triple topology is achieved by tripling the amount of capacitors and switches, while the double topology is applied with a single multiplier.

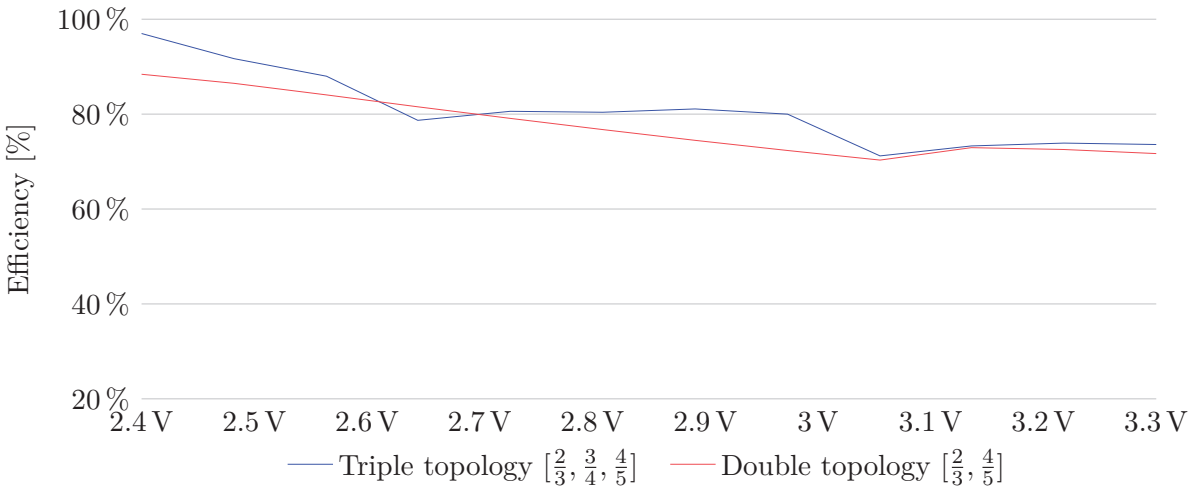


Figure 5.6: Efficiency versus topology

This result clearly shows an improvement in comparison, especially when in the region where the 3/4 topology is used. We can see compared to figure 5.3b, that the efficiency is higher than the expected 86.7% at 2.4V because the output tries to charge above 1.8V. However, because the clock switches off the system for a period, the difference between P_{out} and P_{in} will go down and the efficiency goes up. Since the transistor's on-state resistance is nonlinear with voltage, the general nonlinearity of the topology in the figure is as expected. The maximum efficiency of the triple topology is found to be 95.7% at 2.4V, and the minimum efficiency is found to be 71.2% at 3.06V.

CHAPTER

SIX

DISCUSSION

The aim of this chapter is to take one step back and discuss the work conducted in this thesis more in general, and to point out things that can be improved. The simulation data presented in the previous chapter will be discussed. Additionally, comparison between the implemented design and other published work will be discussed in section 6.3. The discussion may be limited by the author's knowledge within this field, as he specialises in digital electronics.

6.1 Evaluation and Analysis of Simulated Data

A steady-state simulation was carried out, which proved that the intended conversion ratios were archived with a minimum of 99.5% accuracy. This suggests that the schematic implementation of the proposed topology design works as intended. The reason for the 0.5% margin of error most likely relates to the charge redistribution as the sum of the three fly capacitors do not match the load capacitor. Overall, the result confirms the design implementation made in chapter 3.

The simulations presented indicated a major problem. It turned out that there was an output voltage drop when the maximum load was applied for all input voltages between 2.4-2.5V and 2.7 to 2.9V. There is two possible reason for this voltage drop:

1. There is a current-leak due to either switching mismatch or parasitic shortcuts.
2. The circuit impedance R_{out} dominates equation 2.18 and according to equation 2.17, the output voltage drops.

Statement 1. was tested and verified as not true by using DC-analysis. It turned out that the only parasitic losses found were in the order of *pico* and *femto* amps for the MOS-switches. A closer inspection of the switching sequence as well as possible leakage to ground did not point at any significant failures. This problem seems to not be linked to technology as a test was carried out on ideal components.
Statement 2. is therefore the most likely cause of the problem. This can be explained by

Ohm's law: When R_{out} increases and the current remains constant, the output voltage decreases linearly with the resistance.

A sweep test of the transfer capacitors indicated a solution as seen in figure 5.3. Only by tripling the transfer capacitors and MOS-switches were all the output voltages trending positive below inputs of 2.9V. Doubling was not satisfactory enough for the 3/4 converter, because the topology experienced a marginally higher loss than gain in its second phase ϕ_2 between 2.7 and 2.81V. It is speculated that this might have to do with the fly capacitors polarity, which according to [33] matters. As the 3/4 topology is struggling to charge up in phase ϕ_2, it means this topology is not as compatible with the other two. This can be confirmed as R_{out} for both 2/3 and 4/5 is ideally matched as shown in table 5.2. The double topology can accrual be seen to work with maximum load at a one-to-one scale as pointed out in figure 5.6.

One interesting observation is in fact that $V_{loss|real} < 200mV$, which means that there is more wiggle room when it comes to choice of topology. It can also be see that γMV_{in} is approaching the target value of 1.8V, meaning less work has to be done by the clock gating module, thus saving some energy. However, it must be pointed out that by increasing the load capacitor, it may take multiple seconds to recharge C_{load} when empty, hence burning more energy.

6.1.1 Consequence of modification

When increasing the capacitors multiplier from 2 to 6, the efficiency at 2.4V drops from 90.3% to 86.7% as shown in figure 5.3b. This also implies that power consumption increases by a factor of 2, which is twice compared to the load's power consumption as pointed out in figure 5.3a. This is even worse as this is not a linear behavior, meaning that at 3.3V the converter's power consumption is actually 17 times bigger than of the load, at approximately 306 μW. Although the by-product of upscaling is an increase in both area consumption and power loss, one has managed to get a positive trend on the output terminal in all stages.

Moreover, an increase in flying capacitors with a factor of 3 would indicate a further implementation of 22 dummy-transistors to improve matching, which will not justify the decision. This action will decrees the power-density with an massive amount. Increasing the capacitors could have been avoided if one could increase the frequency. This would save area, but would still affect consumption as various functions have a direct connection with increased frequency such as equation 2.22, 2.35 and 2.36.

6.1.2 Noise analysis

It can be observed from Table 5.2 that the ripple noise is well within the required limits of ±25 mV with a C_{load} a million times smaller than the final load. According to equation 2.4, increasing the load capacitor will only dampen the noise further.

6.1.3 Resistance analysis

The plot in figure 5.2b is based on a single multiplier simulation. This means that the listed output resistance in Table 5.2 can be compared to a calculation based on each of the

topologies R_{SSL} and R_{FSL} when considering the on-state resistance simulated in figure 5.4. This yields to:

$$
\begin{aligned}
R_{out|\frac{2}{3}} &= \sqrt{\left(\frac{1}{3}\cdot\frac{1}{60\cdot 10^{-6}}\right)^2+\left(\frac{23}{18}\cdot 11\cdot 800\Omega\right)^2} = 12.5K\Omega \\
R_{out|\frac{3}{4}} &= \sqrt{\left(\frac{3}{8}\cdot\frac{1}{60\cdot 10^{-6}}\right)^2+\left(\frac{19}{8}\cdot 10\cdot 747\Omega\right)^2} = 18.8K\Omega \\
R_{out|\frac{4}{5}} &= \sqrt{\left(\frac{12}{25}\cdot\frac{1}{60\cdot 10^{-6}}\right)^2+\left(\frac{48}{25}\cdot 9\cdot 679\Omega\right)^2} = 17.7K\Omega
\end{aligned}
$$

In Table 5.2, these values are found to be about 10 $K\Omega$ more for all three topologies, meaning there must be losses from other sources. This could be related to sub-threshold leakage given in equation 2.28.

6.2 General discussion of the results

One important observation is that there is a greater mismatch when evaluating the 3/4 topology, compared to the two other topologies. The cause of some of the problems found when simulating, can be that the input from the battery is not constant, leading to that the voltage across the SCPC changes between 3.3V and 1.8V. The 3/4 topology may be unpredictable because some switches may turn off prematurely due to problems related to equation 2.24. This would most likely be switch 10 or 11. It can also be caused by the polarization of the capacitors in the circuit, or the fact that only C_3 is connected to ground between phases, unlike C_1 and C_2. Another possibility is that it could be due to switching errors if the clock signals are mismatched. Thus, opening switch 14 at the same time as on of the other switches, leading to a small loss occurring multiple times per second. Due the time constraint and sheer complexity associated with this project, it is necessary to further see what problems may arise with a physical implementation of the design.

6.3 Comparison to the current state-of-the-art

Table 6.1 lists published works with similar characteristics as mentioned in this thesis. The results from this thesis will be compared to the existing state-of-the-art.

Table 6.1: Performance summary and comparison

Characteristics	This Work	[34]	[56]	[32]	[3]	[4]
Technology(nm)	28	130	45	130	32	180
Input voltage (V)	3.3-2.3	3.3	1.8	1.8	1.8	5.5-3
Output voltage (V)	1.8	1.5-1.2	1-0.8	0.3-0.55	1.1-0.85	2
Maximum load current (A)	10u	53m	10m	55m	37m	2m
Topologies	$\frac{2}{3}, \frac{3}{4}, \frac{4}{5}$	$\frac{1}{2}$	-	$\frac{1}{2}, \frac{1}{3}$	$\frac{1}{2}, \frac{2}{3}$	$\frac{1}{2}, \frac{2}{3}, \frac{4}{5}$
Number of C_{fly}	3	1	2	2	2	2-3
Flying capacitance (F)	65p	2.176n	534p	-	-	288p
Load capacitance (F)	47u	1n	700p	5n	-	7n
Switching frequency (MHz)	1	40	30	100	100	20
Peak efficiency η (%)	95.7	73	69	70	90	82
Power density $\rho(mW/mm^2)$	0.217	31.2	50	24.5	370	39.1

Not found (-)

It is somewhat difficult to make one-to-one comparison with the recently published SC converters as many of them are fabricated in different CMOS technologies with different input voltages. On the other hand, comparison is still helpful to evaluate circuit performance, in relation with recent designs, specifically in certain domains.

First of all, the most noticeable result when comparing is the peak efficiency, which in this thesis is based on the conversion block only. Suppose one takes into account that the ideal peak efficiency at 2.4V was designed to be 93.75% as pointed out in figure 3.1, then the final result at 95.5% as well as the median efficiency at about 80% throughout the entire lifespan, and a minimum efficiency of only 71.2% can be considered a success. It is however important to criticize the result. It can be said that an artificial result has been achieved, since it is not realistic to implement something that is 3 times as large as what it is budgeted for. Because the final design is 3 times larger, the power consumption at 3.3V would extend beyond $300\mu W$, which is 17 times more when compared to the power consumption of the load at about $18\mu W$. Another interesting observation is that the efficiency seems to increases in the case of $\Delta C = C_{load} - C_{fly}$, except in the case of [34]. Power density is not realistic to compare as there are two different power scales.

CHAPTER

SEVEN

CONCLUSION

In this thesis, an on-chip switched capacitor step-down voltage regulator (OCVR) utilising three different topologies has been designed and simulated with 28nm technology. It was discovered during testing of the triple-topology module that both capacitors and MOS-switches had to be multiplied with a factor of 3 to meet the specified operation parameters. The final triple-topology design, excluding the control circuits, then achieved an efficiency ranging from 71.2% to 95.7%, peaking at 2.4 V. Both the $\frac{2}{3}$ and $\frac{4}{5}$ topologies were inspired by the work presented in [4], while the $\frac{3}{4}$ topology with double charge input has been carried out in this thesis. It is also implemented a set of optimized custom logic gates for use in the low power control circuit. Furthermore, implementation of the Charge-Steering strongARM comperator was proven to be useful as it was possible to use one feedback controller to archive efficient clock gating instead of two. Finally, a layout of the converter block has been attempted. However, due to time constraints, this was not completed in its entirety.

This work has therefore proven both fundamental analysis and practical design methods for switched-capacitor power DC-DC converters. For this thesis' input and output conditions the chosen SC topologies are one of the most suitable candidates to achieve the goals as far as theory goes. It can be concluded from steady-state simulation that all three topologies have achieved the intended voltage conversion ratios. It can therefore be concluded that the mention theory is sufficient to explain the complicated aspect of this thesis' topic. It is however interesting how some of the references cited in this thesis seams to not be in total agreement with another when it comes to synthesis of SCPCs.

However, irregularities have been discovered during testing of the tipple topology module. This is problematic from a practical point of view. When the maximum load-current was applied on a one-to-one scale of the triple topology, the output voltage dropped below the minimum target value of 1.785V. Troubleshooting and multiple iterations have not directly given any answers to the specific cause of this issue. With that being said, one has managed to get a positive trend on the output terminal for the triple topology. Thus, satisfying all the specified operation parameters. Although this can be used as a proof-of-concept, this modification would however not be sufficient if to achieve a 15 year life

expectancy from the battery.

Ultimately, simulation indicates that the main problem lies in the $\frac{3}{4}$ architecture. As shown in figure 5.6, the double topology circuit that does not include the $\frac{3}{4}$ topology would most likely work without problem in an one-to-one scale. That means that several more iterations are required to achieve the absolute best result for the triple topology, as it is not prudent to implement the circuit at this current stage. However, the SC converter should not be ruled out based solely on electrical specifications. One must assess other parameters such as semiconductor technology, integration level, complexity etc.. It would most likely costs less to continue on the same path to achieve a better result than accepting the current design.

To quote Thomas Edison when discovering the electric DC-DC light bulb: "*I have not failed. I've just found 10,000 ways that won't work.*" .

7.1 Recommendation for further work

Based on the concepts and results presented in this thesis, recommendations for further research and investigation are as follows:

- Try 10,000 more times..
- More research is needed to asses the problem revolving the $\frac{3}{4}$ topology.
- Optimise for area and power density.
- When assessing a layout, one should merge the different switches into one to save space. Additionally, one should also dimension the guides based on the amount of current, which in turn should be part of the planning before routing. A good practise is to also make layout with several metals (routing), and not only layers 1 and 2 as it has been done in this case.
- This circuit should be build to support DPM in order to charge the load capacitor while the WSN is in idle mode.
- It is possible to upgrade to a 4-topology with n = 4 fly capacitors adding more switches at the same time increase area consumption. However, this will also open the opportunity for more conversion ratios, which can be exploited in order to lower the average power-consumption and become more efficient.
- Other models such as Ladder, Dickson, Fibonacci or Doubler may be more power-efficient compared to the Series-Parallel model and should therefore be explored. It might be more energy-efficient to use a 1.65V instead of a 3.3V battery with a Boost converter outputting 1.8V. This would lower V_{GS} which lowers I_D, at the same time lowering V_{DS} reducing R_{on} . One problem would then be that there is a need for a larger C_{fly}, however, it might not need to be that large.
- Due to the time constraint and share complexity associated with this project it is necessary to further see what problems may arise with a physical implementation of the converter.

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APPENDIX

A

INPUT DESIGN VARABLES

Table A.1: Fixed Design Variables

Input parameters	Value
Gate length-N	280nm
Gate length-P	280nm
C_{fly}	10.876pF
$V_{out_{inic}}$	1.8V
f_{sw}	1MHz
V_{DD}	V_{in}

Table A.2: Changing Design Variables

Input parameters	Figure 5.1	Figure 5.2	Figure **??**	Figure 5.6	Figure 5.5	Figure B.1
C_{load}	47pF	470pF	47uF	47uF	47nF	47uF
I_{out}	0	10uF	10uF	10uF	10uF	10uA
V_{in}	2.4:3.3V	2.4;2.7;3.0V	2.4V	2.4:3.3V	3.3V	2.4V
V_{max}	3.5V	3.5V	1.8V	1.81V	1.81V	3.5V
V_{high}	3.0V	2.95V	3.0V	3.0, 2.9V	3.0V	3.0V
V_{low}	2.7V	2.65V	2.7V	2.7, 2.9V	2.7V	2.7V
MultiC_{fly}	2	6	1:10	6	6	6
Multi-NMOS	1	3	3*	3	3	3
Multi-PMOS	1	3	3*	3	3	3
Total steps	6	3	5	24	1	1

APPENDIX

B

TWO PHASES CHARGING

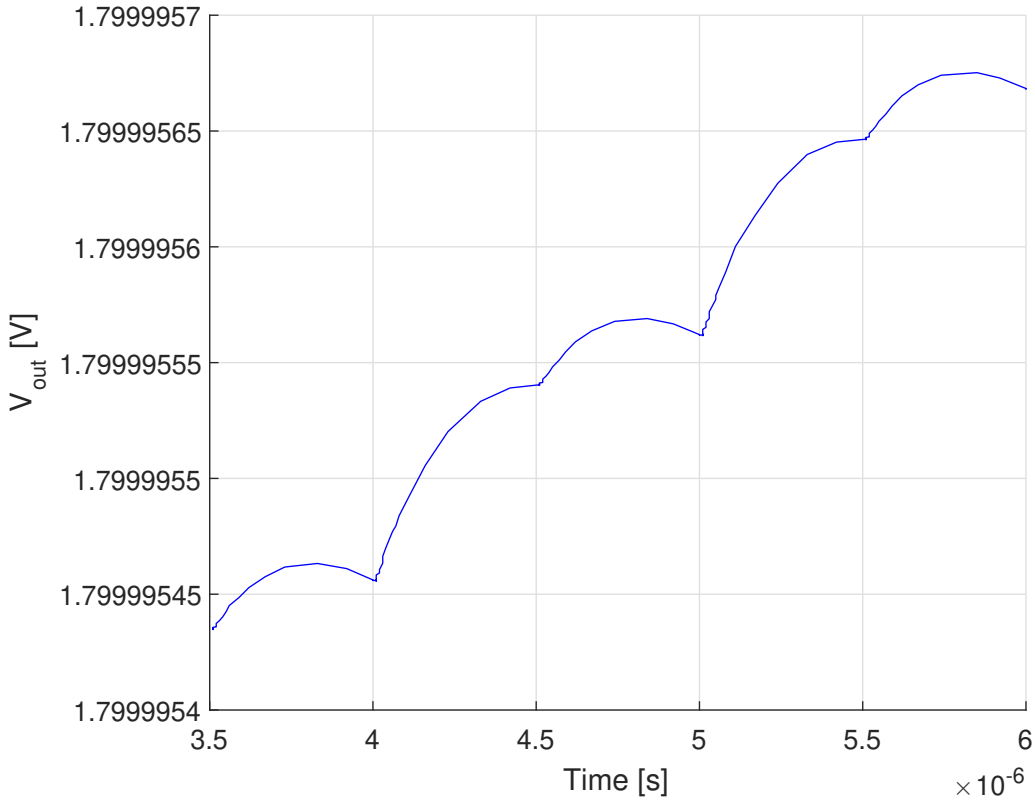

Figure B.1: $V_{in} = 2.4V$: Charging in both phases. $T_{sw} = \frac{1}{1MHz} = 1\mu s$

APPENDIX

C

DOUBLE MULTI-STAGE CONVERTER

Mode	D_0D_1	V_{in}
2/3	11	3.0 - 3.4
4/5	00	2.4 - 3.0

Table C.1: The Double-Topology Inputs

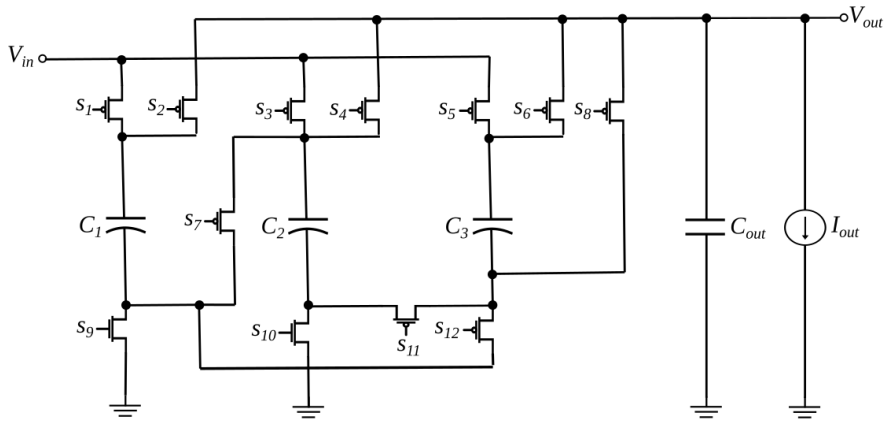

Figure C.1: Double-Topology Converter

mode	D_0D_1	P_1	P_2	P_3	P_4	P_5	P_6	P_7	P_8	N_9	N_{10}	P_{11}	P_{12}
2/3	11	$\phi_{1_{inv}}$	$\phi_{2_{inv}}$	$\phi_{1_{inv}}$	$\phi_{2_{inv}}$	$\phi_{2_{inv}}$	$\phi_{1_{inv}}$	Vin	$\phi_{2_{inv}}$	ϕ_2	ϕ_2	$\phi_{1_{inv}}$	$\phi_{1_{inv}}$
4/5	00	$\phi_{1_{inv}}$	$\phi_{2_{inv}}$	$\phi_{1_{inv}}$	Vin	$\phi_{2_{inv}}$	$\phi_{1_{inv}}$	$\phi_{2_{inv}}$	$\phi_{2_{inv}}$	GND	ϕ_2	$\phi_{1_{inv}}$	$\phi_{1_{inv}}$

Table C.2: Pmos and NMOS switch algorithm

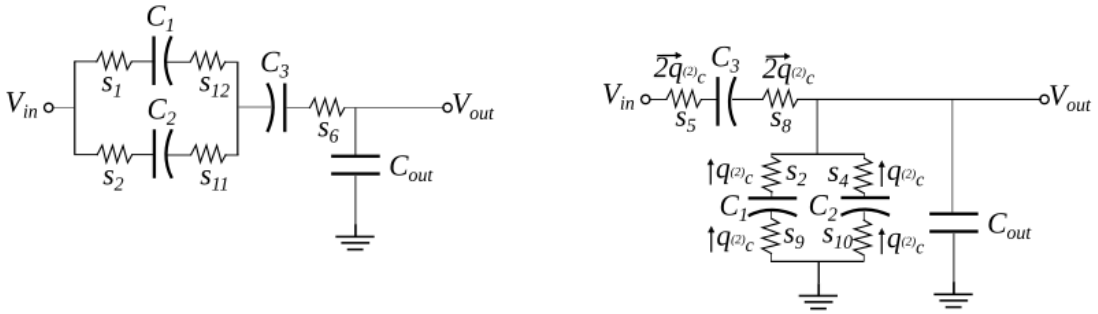

Figure C.2: 2/3: Left = charge phase, Right = discharge phase

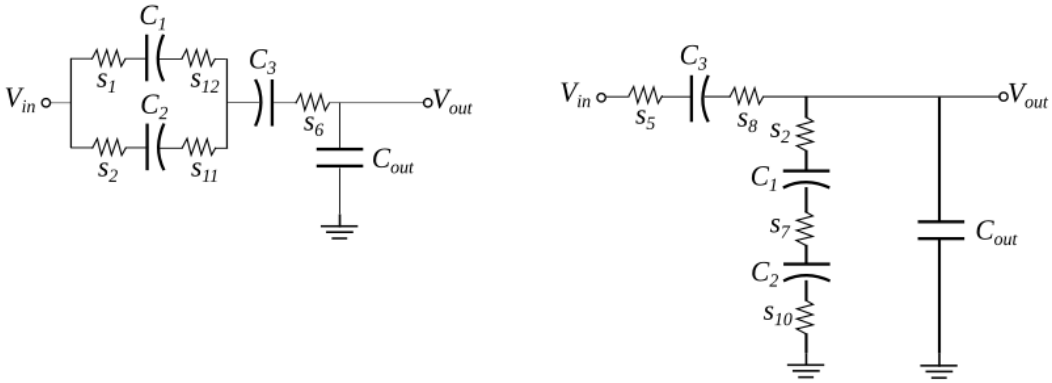

Figure C.3: 4/5: Left = charge phase, Right = discharge phase

$$P_4 = \overline{D_0} + \phi_{2,inv} = \overline{D_0 \cdot \phi_2}$$
$$P_7 = D_0 + \phi_{2,inv} = \overline{\overline{D_0} \cdot \phi_2}$$
$$N_9 = D_0 \cdot \phi_2 = \overline{\overline{D_0} + \phi_{2,inv}}$$

APPENDIX

D

LOGIC GATES

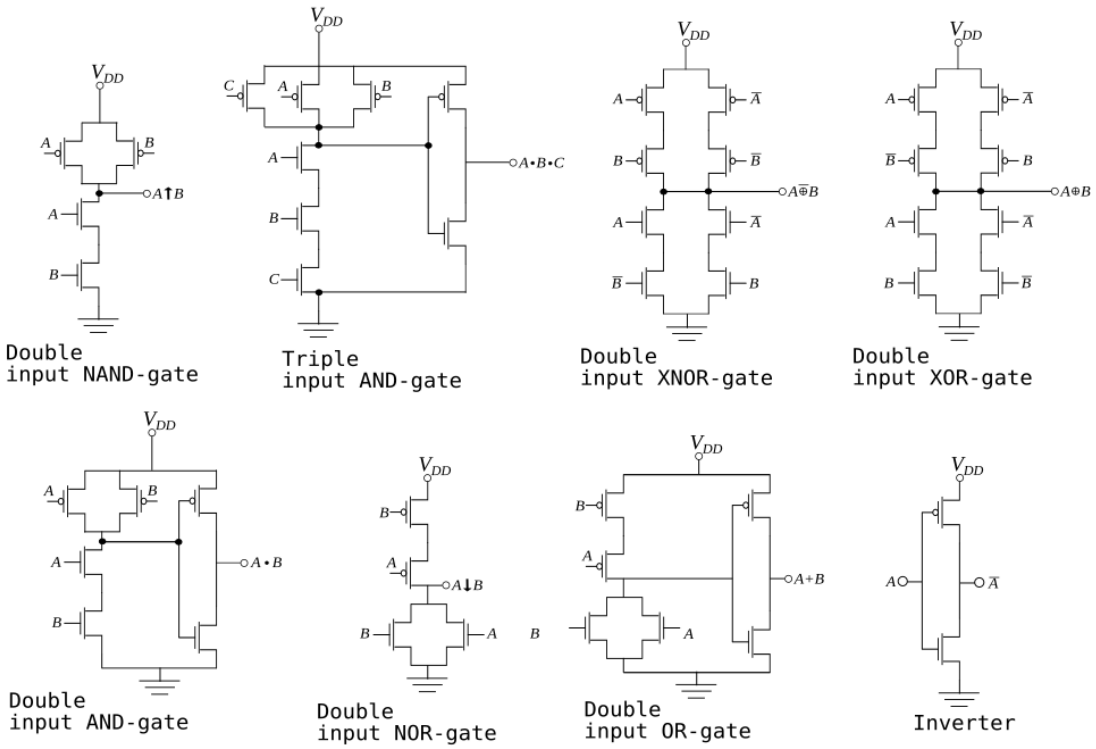

Figure D.1: Logic gates

APPENDIX

E

CLASSIFICATION OF DC-DC CONVERTERS

The three main converter topologies suited for on-chip integration is the linear regulator, the traditional Buck converter (inductor-based) and the switched capacitor converter. The key differences between these three topologies are the trade-off between the size and performance parameters. Some times a combination of the three can be beneficial. Depending on the application that DC-DC converters is build for, the pro and cons have to be considered.

E.0.1 Linear Regulators

The linear regulator consists of a source voltage in series with a PMOS transistor, where the PMOS is controlled by an operational amplifier sensing the output voltage in conjunction with a reference voltage. This action allows an voltage drop over the transistor controlling the voltage on the output node that is connected to a load resistance, therefor effectively working as an voltage divider between the two. The ideal efficiency of an linear regulator is therefor given as:

$$\eta_{ideal.lin} = \frac{P_{out}}{P_{in}} \tag{E.1}$$

Where the linear regulator source-voltage V_{in} is considered constant meaning that the efficiency will drop linearly with the output voltage that is only dependent on the load resistance. Linear regulators are efficient when the dropout voltage is small < 100mV. The dropout voltage is the difference between the output voltage and the input voltage at which the circuit quits regulation with further reductions in input voltage. The advantages of linear regulators is that it uses neither inductors or capacitors meaning area of the chip can be minimized thus gaining an higher power density compared to other converters. The main disadvantage for the linear regulator is the challenge of designing the operational amplifier circuit so that it is stable at high switching frequencies, at the same time handling the variation of the change in the threshold voltage applied to the PMOS transistor.

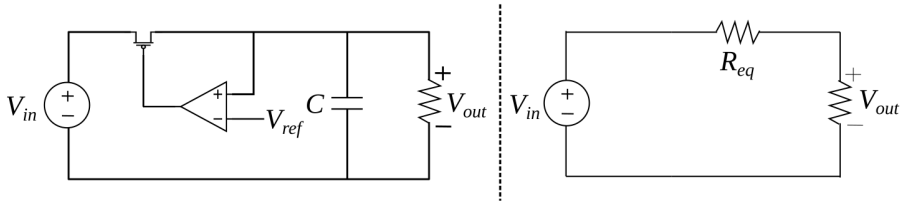

Figure E.1: DC-DC comparison LR Circuit, illustration obtained from source TokeMyer

E.0.2 Traditional Buck Converters

The traditional Buck converter utilizes the electromagnetic properties of both a inductor and capacitors by storing energy in an electromagnetic field releasing it in pulses a set frequency. This converter can generate different levels of DC voltages. Two transistor-operated switches in opposite phases is controlled by the duty cycle D of the frequency. An illustration of the Buck converter can be seen on the left hand side in figure E.2. The output voltage of the Buck converter is a function of the well-known expression $V_{out} = DV_{in}$ [19], hence regulation of the output voltage can be done by changing the duty cycle. The ideal efficiency of the Buck converter is $\approx 97 - 99\%$ [12], or approximately 100%, as most of the energy is stored in the coil of the inductor between transition:

$$\eta_{ideal.Buck} \simeq 1 \tag{E.2}$$

However, the accuracy of the inductor is heavily dependent on the core material as well as the frequency which the current flows through the coil. This physical limitation is the reason why few Buck converters are implemented in nano-scale microprocessor technology. Traditional Buck converters are however preferred in situation where area is not a issue such as on a PCB level where coils can be added outside the PMU due to the incredible high efficiency rate. One low-power application where this function is useful are for example when dimming LED lights where the load current is so small the most accurate way of dimming is by turning on and off the LED multiple times per second. This control technique is also known as pulse-width-modulation (PWM). One illustrative example of this would be if D is 2/5, meaning the duty cycle would be 40% ON and 60% OFF. For a system using a 50Hz frequency, or in other words is OFF and ON 50 times per second, the human eye will only perceive this as if the light is 60% less bright.

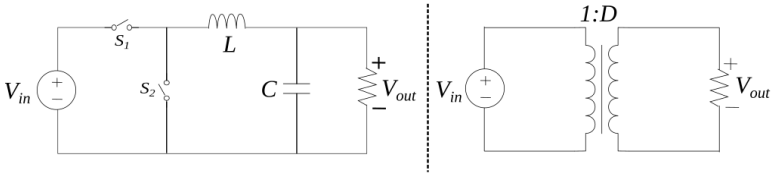

Figure E.2: Traditional Buck converter Circuit

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