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Process optimization for the fabrication of an Atomic Layer Deposition reactor for in situ Transmission Electron Microscopy

Masteroppgave

NTNU
Norges teknisk-naturvitenskapelige universitet
Fakultet for ingeniørvitenskap
Institutt for maskinteknikk og produksjon

Masteroppgave i Mechanical Engineering
Veileder: Jan Torgersen
Medveileder: Stephanie Burgman
Juni 2021

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Kunnskap for en bedre verden

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Acronym

a-si Amorphous Silicon.

ALD Atomic Layer Deposition.

CMP Chemical Mechanical Polishing.

CVD Chemical Vapor Deposition.

DI De-ionized water.

EBPVD Electron Beam Physical Vapor Deposition.

IC Integrated Circuits.

ICP RIE Inductively coupled plasma Reactive-ion etching.

IPA Isopropyl alcohol.

KOH Potassium hydroxide.

MLA Maskless aligner.

MMR Material removal rate.

PDSM Polydimethylsiloxane.

PECVD Plasma Enhanced Chemical Vapor Deposition.

SEM Scanning Electron Microscope.

TEM Transmission Electron Microscope.

TFEL Thin Film Electroluminescent.

TMA Trimethylaluminium.

TMAH Tetramethylammonium hydroxide.

Glossary

Atomic Layer Deposition Type of sequential gas to solid material deposition process, used for both process and machines.

Chemical Mechanical Polishing A polishing process combining mechanical abrasion and chemical etching to remove material, and get a plane surface.

Chemical Vapor deposition A continuous gas to solid deposition technique that uses gasses to make high quality thin films at elevated temperatures .

Electron Beam Physical Vapor Deposition vacuum deposition process that uses a electron beam to melt and evaporate a target material, and the evaporated material deposits as a solid onto the sample .

Inductively coupled plasma Reactive-ion etching A plasma etcher that removes material anisotropic by using ionized gas.

Maskless aligner A photo lithography machines that performs the exposure step in lithography without using a physical mask. Often used for small batches and making photo masks.

Photo Lithography A commonly used process to have a temporary polymer pattern on a sample so permanent post processing such as etching, doping or material deposition can be done in the desired pattern.

Plasma Enhanced Chemical Vapor deposition Same as CVD, but also uses plasma to improve deposition chemistry and lower reaction temperatures .

Scanning Electron Microscope Electron Microscope that hits the sample with an electron beam and measures the reflected electrons to form an image. Gives lower resolution than a TEM, but much higher resolution than a optical microscope can.

Transmission Electron Microscope A electron microscope that produces images by transmitting electrons through a ultra thin sample..

1 Preface

This master thesis is written during spring 2021 at the Department of Mechanical and Industrial Engineering (MTP) at the Norwegian University of Science and Technology (NTNU). I want to thank my supervisor, associate professor Jan Torgersen for guidance and help throughout the year and co-supervisor Stephanie Burgmann for the guidance and help in the lab and making the photo-mask and reactor design. I would also like to thank Markus Joakim Lid and Abdullah Bin Afif for their help with some of the machines and expertise in the NanoLab. I would also thank everyone at NTNU NanoLab, especially Jens Høvik, Mark Chiappa, Mathilde Isabelle Barriet and Martijn de Roosz. I would also like to thank my parents, brother, and sister for supporting me during my master.

2 Abstract

ALD is a thin-film deposition technique allowing to challenge the limits of manufacturing with sub nanometer precision. By using gas to produce high-quality pinhole-free thin films for integrated circuits, solar cells, and many more. Understanding of the nucleation regime, i.e. the first 10nm is indispensable for approaching the limits of thin film devices. The limited possibilities for characterization and observation of growth mechanism in the first 10 nm of deposition makes it necessary to open up new characterization possibilities such as in situ study in Transmission Electron Microscope. Where TEM produces images with high enough resolution to distinguish between individual atoms. Understanding the growth regime is crucial for improving the ALD process.

Microrector size is crucial so electrons pass through the sample, and still fit a TEM sample holder, length and width can not exceed more than a few millimeters and the thickness must be 100 nm or lower. Each chip needs a compartment for the chemical reaction to occur, and this is achieved by making tunnel-like structures. The structures are made in a sequential fabrication process with thin film deposition, photolithography to make temporary patterns, and etching to permanently remove the material in the lithography pattern. The thin films are multipurpose, serving as etch stop layers, membranes, sacrificial layer, stabilization layers, and is the structural element of the microstructure itself

In this thesis, process optimization for the fabrication of a novel microreactor for thin-film characterization in a Transmission Electron Microscope(TEM) were conducted, and is part of a larger project involving a PhD student. Development and process optimization for manufacturing a disposable micro reactor involves exploring possible fabrication steps, characterizing each process step in regards to process parameters, process time, and limiting the failure rate in each process step to a minimum. Processes used in manufacturing and each fabrication step in depth. Seven reactors in 3 batches with different design and fabrication sequences were made. The individual fabrication steps for the reactor were tested and shown to work, except for filling the holes after xenon difluoride etching. During the fabrication, the etch rates, the deposition rates, and manufacturing times for individual processes have been found, and working fabrication processes to make the final product. Changes to the original design during the project increase chip output and reduce damage to chips. Important process data such as process time and cost, etch rates, and deposition rates were collected. The microreactor is disposable with limited volume for film deposition, a cost-effective manufacturing with low cycle time, and this can help to finalize a working ALD-TEM microreactor and increase process speed.

2.1 Sammendrag

Denne master går gjennom produksjonsprosessen for ein liten ALD reaktor for "in situ" studie i eit TEM mikroskop. Innfallsvinkel er prosessopptamilersing og fabrikkering blir evaluert etter repeterbarhet, kostnad, tid, og kvalitet. Hensikten med det overordnede prosjektet er å bedre forstå hvordan ALD prosessen fungerer og at denne nye informasjonen skal kunne brukes til forbedre ALD maskiner. ALD er en mye brukt teknikk innenfor produksjon av integrerte kretser, solceller, og mer. ALD brukes til å lage tynn filmer med materialer fra rundt 1 nm opptil rundt 50nm. Prosessen er brukt når kravene til kvaliteten er høye og det er nødvendig å ha nøyaktig tykkelse. Denne master går ut på å lage reaktoren og er ein del av et større PhD prosjekt. Teksten går først gjennom relevant teori om de prosessene som er brukt for å lage rektoren og deretter gå gjennom fabrikerinsk prosessen. For at reaktor brikken skal fungere i TEM er små dimensjoner en nødvendighet og dimensjonene på strukturene ligger i nanometer til noen få mikrometer. Det derfor både tidkrevende og mange ulike prosesser som må brukes. I prosjektet er det laget 7 prøver, fordelt på tre batcher, med flere reaktorer per prøve, og dei ulike stega som er nødvendig for en mikro rektor er blitt utviklet og testet. Det originale designet og forandringer på designet blir beskrevet. Alle prosess stega har blitt testet og vist seg å fungere med unntak av tetting av tunnel hull etter xenon difluoride etsing. Reaktoren har frittstående tunneler som er hullet ut med xenon difluoride, og åpninger inn til tunnelen for å la elektroner i TEM lett gå igjennom prøven. Hver individuelle reaktor er også laget slik at den passer inn i en TEM holder. Strukturene er laget ved flere steg med tynn film deponering, fotolitografi, etsing, CMP, og karakterisering for å verifisere resultatet.

3 Introduction

This report describes process optimization of the fabrication of micro Atomic Layering Deposition (ALD) reactors for in situ study of the atomic layer deposition process in a Transmission Electron Microscope (TEM).

Atomic layer deposition is essential for producing integrated circuits and other devices, where high-quality thin films are needed. The initial growth regime of ALD deposited layers is still not fully understood, and more knowledge about the process will improve the uniformity and quality of ultra-thin films in many applications [16]. Understanding the growth mechanism and implementing the gained knowledge is a cornerstone in achieving films with angstrom resolution. Implications can be huge for applications where only a few atoms thick layer is enough and the materials used are expensive and difficult to acquire, such as materials for catalyst. Also, in the manufacturing of IC circuits, where transistor sizes are still reducing. Pinhole free ALD deposited layers with excellent quality of just a few nanometers will be essential for reaching higher resolution and pursuing Moore's law [17]

The reactor's requirement is being usable in a TEM microscope adds several constraints and requirements to reactor design. The length and width need to be small enough to fit into a TEM holder, and the thickness needs to be small enough to allow for electrons to pass through the sample. Constraints in size and especially in thickness make nanofabrication tools such ALD, CVD, ICP RIE, and lithography the best suited manufacturing tools for this Micro Electrical and Mechanical (MEMS) device. Each chip needs a compartment for the chemical reaction to occur, and this is achieved by making far-reaching free-standing tunnel-like structures. The structures are made in a sequential 2D fabrication process with thin film deposition, photolithography to make temporary patterns, and etching to permanently remove the material in the lithography pattern. The thin films are multipurpose, serving as etch stop layers, membranes, sacrificial layer, stabilization layers, and is the structural element of the microstructure itself. High-quality thin film is needed and deposited by PECVD and electron beam evaporator so that thin-film thickness is made within nanometer accuracy. Several etching processes are used employing both liquid chemicals and plasma etchants. Corresponding etch rates are highly dependent on etching chemicals and material. Structure construction uses sacrificial layers removed in a pattern corresponding to the lithography mask, with integrated etch stop layers to ensure the complete removal of a sacrificial layer without damaging structures underneath. Etch stop means a layer of material that a specific etching process does not etch or with negligible etch rate, while the process easily etches the sacrificial layer. Some layers serve several purposes during the various process steps. One are aluminum oxide layers, serving both as etch stop layers, tunnel walls, and ultra-thin membranes for inducing little absorption and scattering for the electrons traveling through them during characterization. The final chemical reactor chip design has far-reaching, free-standing tunnel structures hollowed out by vapor etching, with a stabilization layer over the tunnels to protect the structures from mechanical stresses and physical damage. The stabilization layer is made with small windows etched in, so a small part of the tunnel is exposed to reduce electron absorption

and scattering in TEM. The hollowing out of the tunnel is done by xenon difluoride vapor etching.

"Some parts of the master thesis are gotten from the project thesis and previous work during fall 2020 at NTNU."

4 Theory

4.1 Nanofabrication

A common definition of nanotechnology is devices with at least one dimension in the 1-100 nm, and nanofabrication is the fabrication process of these devices [18]. There are many different techniques and machines that are used for nanofabrication. Because devices are often too small to be inspected with an optical microscope, specialized characterization tools are needed to characterize the results. This chapter reviews the main process steps, instruments, tools, and characterization methods used in this project.

4.2 Plasma cleaning

Clean surfaces are needed for many processes in nanofabrication to improve surface adhesion between the film layer and get defect-free films and high-quality interfaces. Chemicals such as but not limited to acetone, isopropanol, and ethanol are used, but these chemicals can remain in small amounts on the surface as contaminants. One approach to obtain clean surfaces is plasma cleaners which can be used instead of or after chemical cleaning. The plasma, which consists of ions, electrons, radicals, and neutral chemical species, tends to be created by either an RF or DC source ionizing a gas that flows through the plasma source. Plasma parameters such as density of ions, electrons, electron/ion energy are affected by the gas pressure, flow rate, and type of gas/gasses used. At NTNU, oxygen, nitrogen, or argon are used either in combination or separately. The plasma cleaner at NTNU NanoLab is a Diener Electronics Model:Femto with maximum generator frequency at 40kHz, maximum flow rate at 200 sccm. [19]. The plasma cleaning itself entails several reactions such as ion bombardment, UV radiation, radical forming on the surface if using oxygen. For inductively coupled plasma, the substrates are negatively charged in relation to the plasma, and ions will be attracted and accelerate ions towards the surface. This ion bombardment helps break chemical bonds, which in turn increases the adsorption of chemical species, chemical reactions, and desorption of chemical species [20]. In addition, UV radiation helps break bonds in organic materials. The breaking of the bonds creates smaller hydrocarbons that are more easily removed in the low-pressure atmosphere or by the plasma's chemical reaction, which is then removed with the exhaust gas flow.

4.3 Thin film deposition

Nanofabrication uses a 2D approach where each layer is structured independently. Each layer is manufactured as thin-film ranging from a few nanometers to several μm on a substrate. Among known manufacturing techniques are deposition methods such as dip coating, ALD, CVD, evaporation, spin coating, sputtering. Essential measures in all of them are deposition speed, film quality, thickness control, cost, time, and what materials

can be deposited.

4.3.1 Atomic layer deposition (ALD)

ALD is a highly conformal, self-limiting deposition technique that can be controlled with one atom layer precision giving high aspect ratio results [21]. The drawback is that it is slower than other deposition techniques. ALD was discovered independently in the soviet union by Stanislav Koltsov and in Finland by Tuomo Suntola. By mid-1980, the only industrial use of ALD was for Thin Film Electroluminescent(TEFL) display and remained the only industrial use of ALD until the 1990s. As the demand for smaller transistors continued to rise in the 1990s, IC manufacturing started to use ALD in IC production. Increased research was conducted, and the technique was more and more implemented in industrial applications. The unique qualities in terms of thickness control and uniformity and the ever-increasing library of available materials place great expectations on the technology.

4.3.2 ALD process

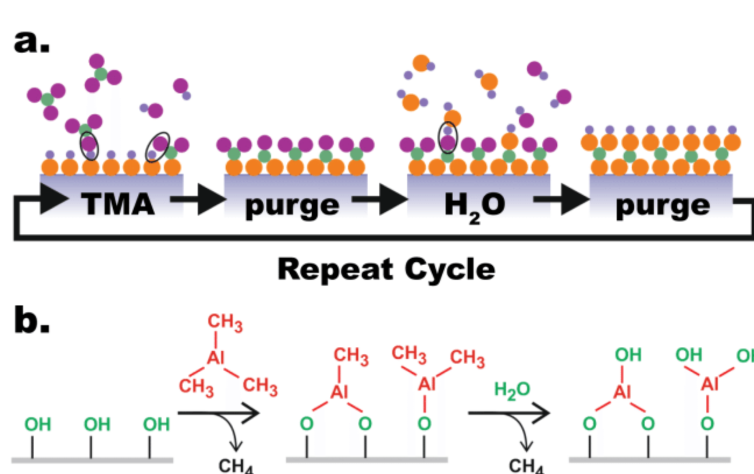


Figure 1: Atomic Layer Deposition Aluminum oxide process [1]

ALD is a four-step sequential process repeated until the desired thickness is achieved [22]. Prior to the deposition, the initial cleaning procedure removes organic and metallic contaminants and the native oxide layer of an oxidizing species(e.g., Si, Ti, Al). The substrate is then placed into the reactor that is then evacuated. After achieving desired vacuum and temperature, the first half cycle is started by introducing a precursor gas into the reaction chamber and is left there until the precursor has reacted with all available surface sites [22]. Then, the first purging step removes any remaining precursor gas and waste gases. The second precursor gas is then introduced into the chamber and reacts with the substrate. The reaction products and the remainder of the reactants are purged after a certain residence time. After pumping and purging the chamber, the cycles repeat

until reaching desired thickness [22]. Each cycle is in the range of 1 angstrom depending on the atom size and bond distance. For example, for the aluminum oxide deposition at NTNU NanoLab, the thickness found per cycle is 0.114nm/cycle when 500 cycles are deposited and measured with an ellipsometer.

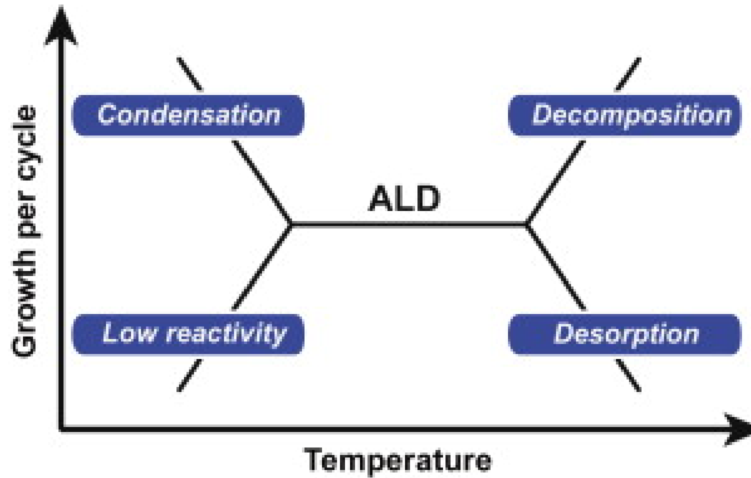


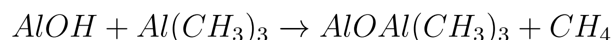
Figure 2: Schematic of ALD window [2]

Thermal activated ALD, which is the most common type, the temperature is paramount. Depending on the material and precursor, the temperature window or ALD window where deposition is achieved can be very narrow. So temperature control is vital for the quality of the thin film. The temperature range for the ALD window varies depending on the material and precursors. If the temperature gets outside of the window, there are four possible competing processes. As we can see from the figure 2 if the process is outside of the temperature range, condensation or low reactivity happens at low temperature, and decomposition or desorption at higher temperatures [2]. At lower temperatures, low reactivity can occur where there is not enough thermal energy for the surface reaction to occur, or the precursor can condense on the surface and remain on the sample as a liquid. If the temperature goes over, the ALD window precursors decompose on the surface or desorption where molecules are released from the sample [23].

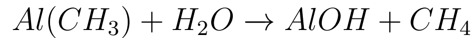
4.3.3 Atomic layer deposition of Al_2O_3

Aluminum oxide deposition from TMA and H_2O has extensive research available, and the process is commonly used as it renders a high-quality thin film, self-terminating reactions, and methane as an inert waste product. The Al_3O_2 layer is a dielectric with a bandgap of 9 eV, making Al_3O_2 useful in a wide range of application.

The two following chemical reactions are the two half reaction that occur with a purging step before and after each cycle [2].



$$AlOH + Al(CH_3)_3 \rightarrow AlOAl(CH_3)_3 + CH_4$$



$$Al(CH_3) + H_2O \rightarrow AlOH + CH_4$$

The CH_4 is the waste in both reactions and is removed by the purging. A single AlOH layer remains after one cycle, which consists of both half-reactions and purging. The aluminum oxide deposition has a relatively large ALD window where temperature ranging from 200°C to 400°C in some hot-wall reactors [24], Deposition in this projects were done at 160°C to give an example over the ALD window for Aluminum Oxide [2].

4.4 Chemical vapor deposition (CVD)

CVD is a thin film deposition technique producing high-quality films by having volatile precursor compounds react with the substrate's surface. ALD is a special case of CVD, where most CVD processes have continuous gas flow; ALD is a sequential gas deposition technique. While ALD is a type of CVD, we will treat it as a separate process in this text. There are many variants of CVD as shown in table 13, where we mention some

Name	Abbreviation
Atmospheric pressure CVD	APCVD
low pressure CVD	LPCVD
ultra high vacuum CVD	UHVCVD
sub atmospheric CVD	SACVD
Hot wall CVD	
Cold wall CVD	
Microwave plasma assisted CVD	MPACVD
Plasma enhanced CVD	PECVD
Remote plasma enhacned CVD	RPECVD
Low energy plasma enhanced CVD	LEPECVD
Atomic layer CVD	ALD
Hybrid physical CVD	HPCVD
Laser CVD	LPCVD

Table 1: List of variants of CVD

In this text, we will focus on PECVD as a variant of the CVD process. CVD processes, in general, can achieve functional films with a quality that can not be obtained using other manufacturing techniques.

What makes a good precursor is a combination of several factors volatility, thermal stability, decompose cleanly and controllable, stable byproducts, cost, non-prophetic, and non-toxic, still it is not possible to get all these qualities in a precursor.

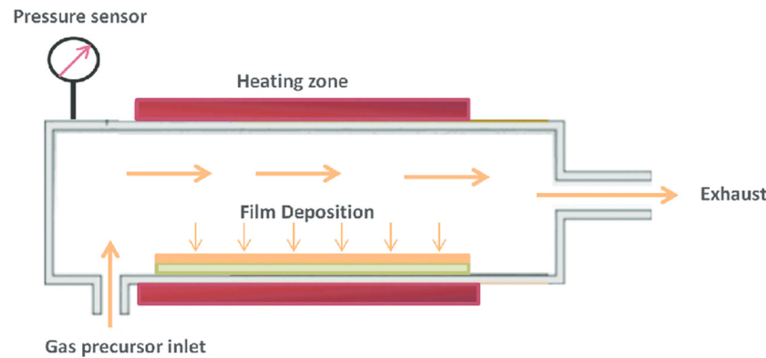


Figure 3: Schematic of chemical vapor deposition process [3]

4.4.1 The CVD process

The precursor gas/gases, along with carrier gas, are transported to the heated reaction zone in the chamber[25]. In the reaction zone, deposition happens through diffusion, a chemical reaction on the surface. The chemical reaction creates a thin film on the surface and waste, which are removed from the chamber[25]. The reaction chamber is at low pressure and is heated [25]. During the silicon dioxide deposition, the pressure and temperature is set at 1000mTorr and at 300°C

4.4.2 Plasma enhanced chemical vapor deposition (PECVD)

PECVD is commonly used in nanofabrication for its ability to make high-quality films at a lower temperature than thermal CVD with high deposition rates[26]. In PECVD, the energy needed comes from part plasma and part heat energy. Since some of the energy comes from the plasma, the PECVD is able to operate in a lower temperature range than thermal CVD[26]. A broader range of materials can therefore be manufactured, such as polymers.

The plasma is created and sustained by applying a high voltage to gases in a vacuum. The plasma consists of electrons, ions, free radicals, and neutral molecules. Employing a magnetic field to ionize the precursors creates reactive species that can react to the substrate at substantially lower temperatures than thermal CVD. The lower deposition temperature can be 300 or below [27].

4.4.3 Electron beam physical vapor deposition

Also called e-beam evaporator is a thin film deposition technique, where an electron beam melts and evaporates the target material so the evaporated material will spread in the vacuum chamber and deposited on all surfaces in the line of sight. Since the process works by melting, there can be high temperatures in the chamber that can lead to impurities

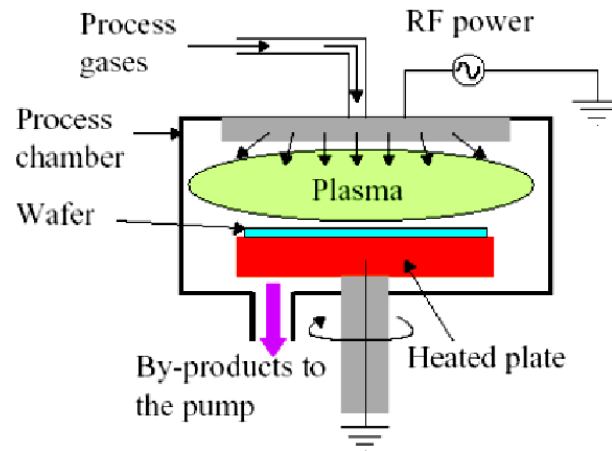


Figure 4: Schematic of Plasma Enhanced CVD [4]

in the film. The process typically have deposition rate, ranging from 0.1 µm/min to 100 µm/min [28]

E-beam evaporators produce thin film at a high rate.

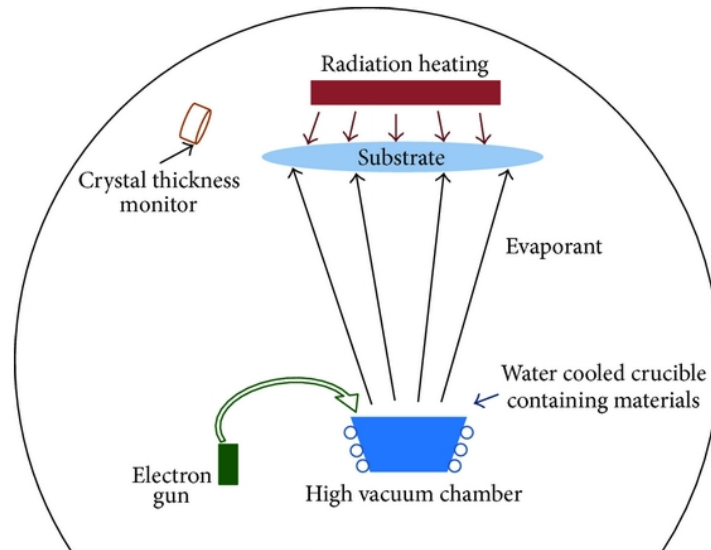


Figure 5: Schematic of E-beam evaporator [5]

4.5 Lithography

Photolithography has been integral in nanofabrication for years with its ability to transfer patterns to a substrate for post-processes such as doping, etching, and film deposition [29]. Since its importance for IC production and being a bottleneck for IC fabrication,

considerable research and development have been done to develop lithography over the years[29].

From the research and development, several variants of lithography exist, such as contactless or contact physical mask, and maskless with many different exposing wavelengths [30]. The pre-processing is the same, starting with cleaning, dehydration bake with temperature over 100°remove water and coating. The dominant way of coating is spin coating. Where photoresist is dropped onto the wafer, which is fastened to the spinner by a vacuum chuck. Then the spinner is run at specified acceleration and speed for the desired time. Acceleration, speed, spin time, and resist type affect resist thickness. After spin coating, some resists require a pre-exposure bake after spin coating, where temperature and time vary depending on resist type. Afterward, the sample is exposed during the lithography step. Exposure can consist of a light source or electrons. Various wavelengths can be used depending on resist type, but 405nm is used in this project. After exposure, a post-exposure bake on a hotplate is sometimes done. Then development, consisting of submerging the sample into a mix of chemicals specifically made only to etch either exposed or unexposed areas, depending on whether the resist is positive or negative. A temporary polymer pattern is then on the surface. Post-processing such as etching, deposition, or doping can then be done selectively. Afterward, resist is removed with either chemical such as acetone or plasma. [31]

The theory that completely describes lithography is extensive, but a short conceptual theory is sufficient and helpful when working with lithography.

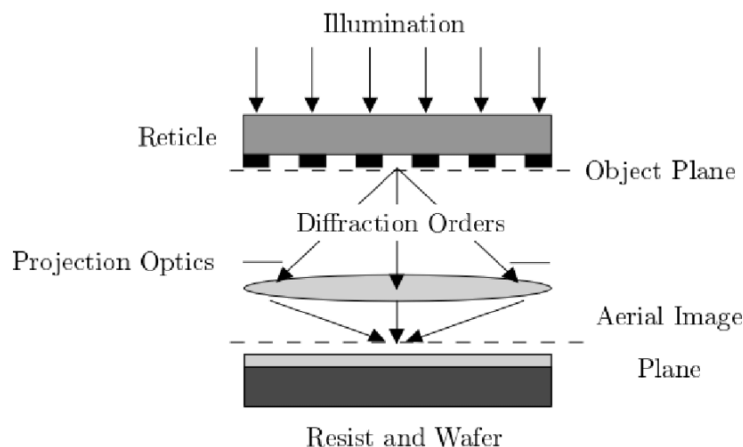


Figure 6: Diagram of masked lithography [6]

The lithography process can be divided into four modules Those are the illumination system, comprising a light source and the condenser optics, the photomask, the projection optics, and the resist-coated wafer. Physical masks are an opaque plate with transparent patterning that allows light through if the mask and resist is in contact pattern transfer is 1:1, but in contactless the projected pattern can be in the range 5:1 to 10:1. These transparent patterns can be modeled as small slits, and the angle of diffraction is given by

$$Sin(\phi) = m\frac{\lambda}{a}, m = 1, 2, 3, ...[31]dr$$

Where λ is the light wavelength, and ϕ is the diffraction angle of the light, and a is the width of the slit. The scattered light will then focused by a lens system which can be described by the formula

$$NA = nSin(\theta)[31]$$

Here NA is the numerical aperture, θ is the illumination length. This can be rewritten to get the systems critical resolution limit R, where for brevity some calculations steps have been skipped.

$$R = k_1\frac{\lambda}{NA}[31]$$

Where R is the critical dimensions, k_1 is a factor depending on the imaging process (k_1 < 1)

4.5.1 Maskless lithography aligner (MLA)

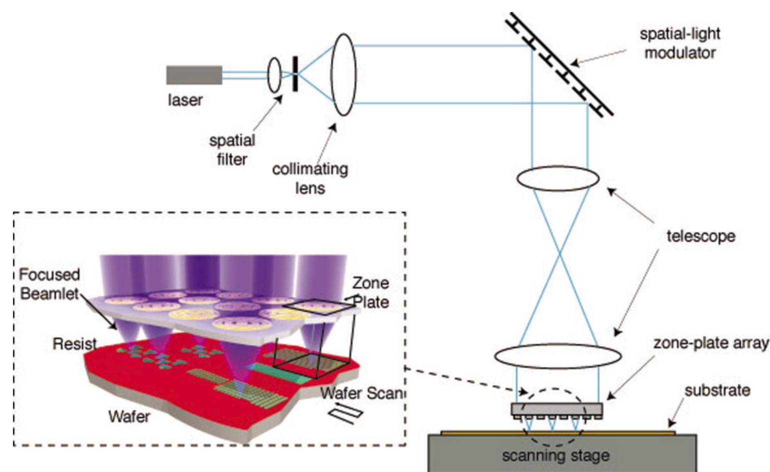


Figure 7: Maskless lithography system [7]

The industry standard for high bulk production is to use mask litho, but for prototyping and mask making MLA is the standard. MLA is already the standard for smaller batch sizes both for research and industry. As we can see from 7 MLA, consists of a laser/electron source, several lenses, and a spatial light modulator (SLM). SLM is maneuvered, so the desired pattern is exposed. The telescope will focus individual beams onto a zone plate. While a Fourier telescope within the telescope ensures enough contrast between on and

off states. [7]

4.5.2 The photoresist and exposing source

A photoresist is a polymer-based light-sensitive material that can be coated with spray or spin coating. There many types of resist commercially available with different chemical compositions and uses. One of the most important ways to categorize resist is positive or negative resist. As seen in Figure12 after developing exposed areas remains when positive is used, and for negative resists, the opposite is true. In general, there are also differences in critical feature size, cost, etch resistance, surface adhesive properties, and lift-off between positive and negative resist that will affect resist selection. In this project, SPR700 is used, which is a positive resist, and developed with mf-26a developer.

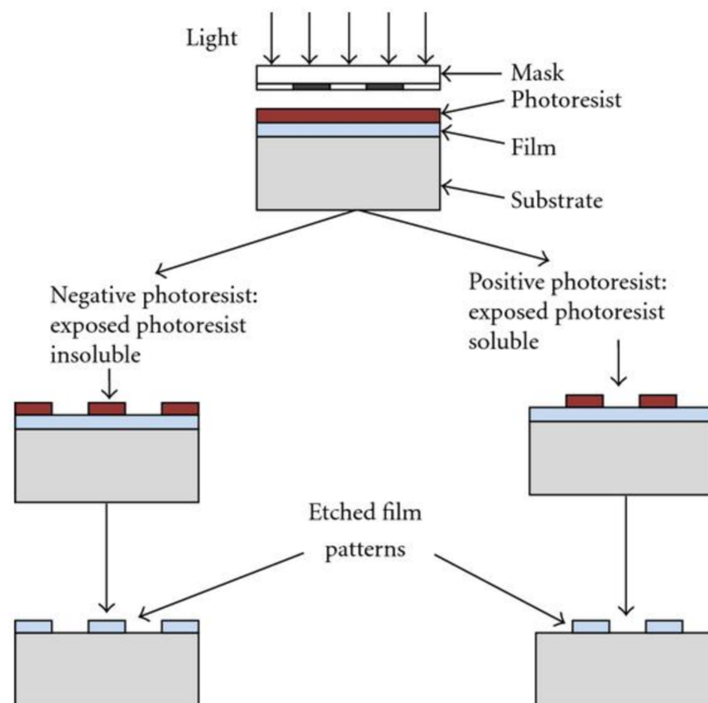


Figure 8: Difference between positive and negative resist [8]

4.6 Etching

Etching is a micro-fabrication process used to remove layers of material by either liquid chemicals (wet etching) or plasma (dry etching). The etching can be done on the whole substrate surface but is often done after lithography to etch and create permanent structures on the substrate selectively. Wet etching is a simple way of etching but requires the handling of chemicals and the etching is isotropic. Dry etching uses plasma, and etching is highly an-isotropic

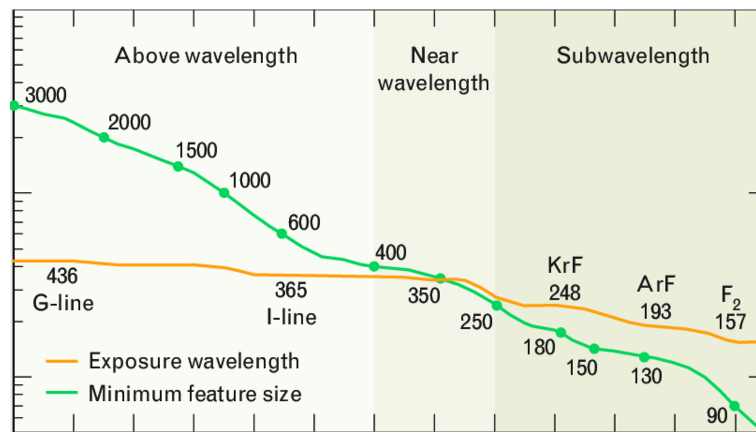


Figure 9: Common wavelengths and their minimum feature size [9]

Etching is the process of removing material either selectively by doing lithography before etching or whole surfaces. The two significant categories of etching are wet etching and dry etching. Wet etching is when liquid chemicals are used to etch. The thin film is exposed for a specific time to the etching liquid depending on the etching rate and desired etching depth. The etch liquid varies depending on what material is being etched but tends to be a solution of several chemicals. Wet etching is stopped by removing the etchant by using DI water or other suitable chemicals. This etching method is simple and does not require expensive equipment but requires handling and disposing potentially dangerous chemicals. The etching is also isotropic compared to the highly anisotropic dry etching. The dry etching uses plasma to etch and requires a specialized machine to etch. Dry etching removes material by utilizing one or a combination of several processes. They can be divided into chemical or physical material removal. A gas flowing over and reacting with the substrate surface is an example of chemical dry etching.

4.6.1 Inductively Coupled Plasma - reactive ion etching (ICP RIE)

Combining the chemical and plasma etching ICP-RIE etcher are highly efficient at removing material anisotropically and can give high aspect ratio results[31]. The ICP-RIE differs from regular RIE by having an inductively coupled plasma source that works by having an RF-powered magnetic field ionizing the gasses[31]. This means that there is a higher density of plasma in the chamber. The plasma presence increases the etching done by ion sputtering, reactive etching, radical formation, and radical etching. [31] ICP is partially ionized gas with an equal amount of negative and positive charged particles. Material removal by having reactive ions chemically react with the surface RIE[31].

4.6.2 KOH etch

Potassium hydroxide etching will be used for an-isotropic etch of the Silicon nitride layer. KOH etching is done at a angle of 54.74°between the <1 0 0> and <1 1 1> plane. the etch

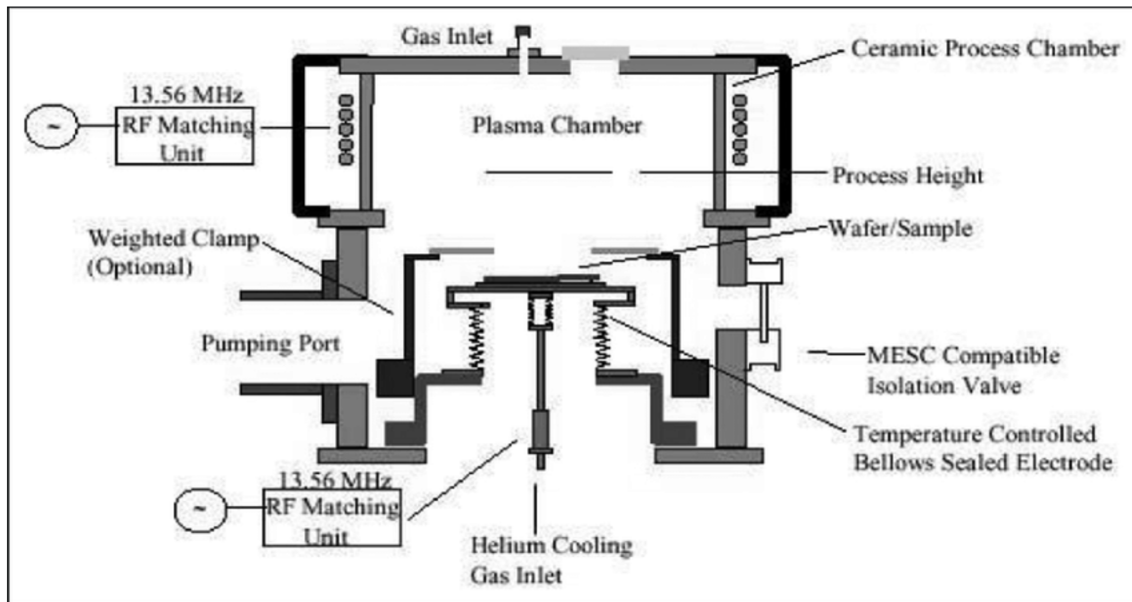


Figure 10: Schematic of ICP RIE setup [10]

rates depend on temperature, and the concentration of KOH [11]. Since the etching is a highly selective process, care needs to is taken to ensure that mask design and lithography alignment is correct [11]. Tetra-methyl-ammonium-hydroxide (TMAH) is an alternative to KOH etch, but it is more expensive and requires a more complex setup, but since KOH often will give good enough results, it is preferable to use. [32]. In this project 30% KOH solution is used.

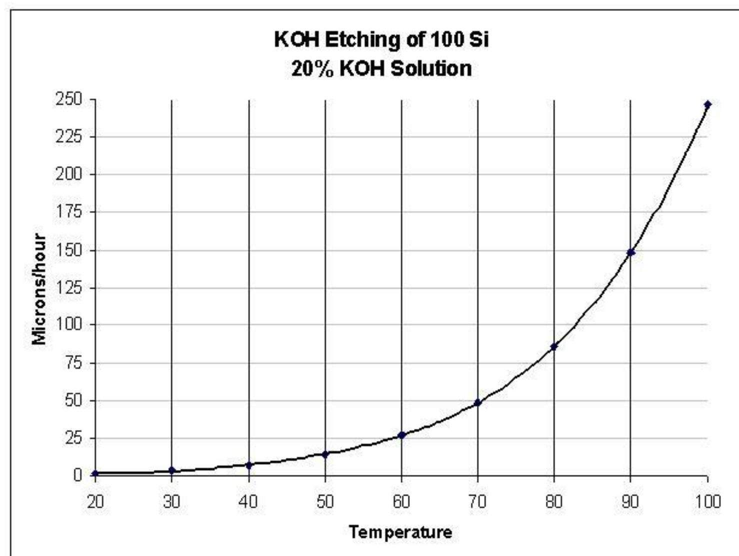


Figure 11: Etch rates of KOH etching Si [11]

4.6.3 Buffered Hydrofluoric Acid (BHF)

Hydrofluoric Acid (HF) and buffered HF are used for etching material such as silicon dioxide and silicon nitride. At ambient temperature 49% HF etch rate can be up to 1µm, and for 1:6 BHF typical etch rate is 0.1 µm [33]. So for some types of etching, the HF can give to high etch rates, and for a more controlled process, the BHF is preferred.

4.7 Chemical mechanical polishing (CMP)

CMP is a polarization technique combining chemical etching and mechanical abrasion to create a highly plane surface [34]. The colloid used for the chemical etching is called slurry. Mechanical abrasion is done by having the wafer grind towards a spinning surface while the wafer chuck rotates. The combined effect is that all the mechanisms give a highly plane surface, but with several variables connected with the mechanism, it can be hard to predict the optimal settings. So the actual use of CMP often requires trial and error to find the optimal working pressure, slurry mixture, and speed to avoid delimitation and polarization within tolerances.

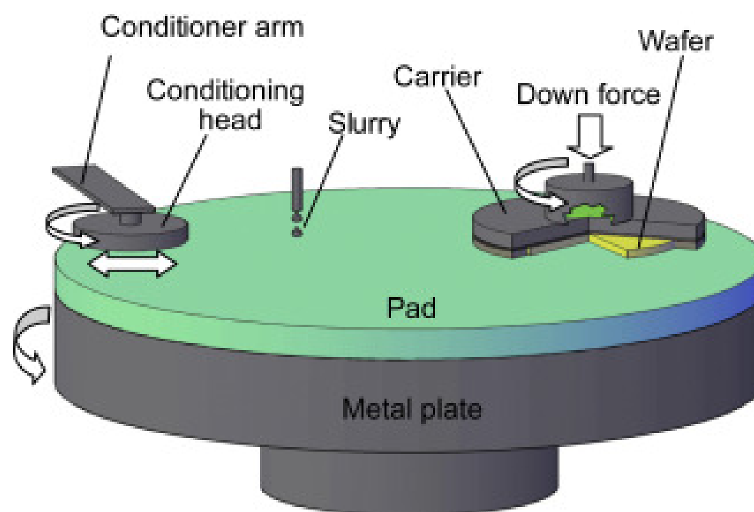


Figure 12: Schematic of CMP setup[12]

4.8 Characterisation and elipsometer

Characterization of layer thickness, geometry, and surface quality after fabrication requires, in many cases, specialized tools for characterization. Electron microscopes come in two variants SEM and TEM. To check the results of the fabrication SEM is used, so an overview of SEM is given[35]. SEM requires less sample preparation, and samples can be larger in all dimensions compared to TEM. TEM, however, gives higher resolution images, but samples need to be thin. SEM is an essential tool when dimensions are in the lower

micrometer or nanometer range and optical microscopes have too low resolution. This chapter will also look into ellipsometer for measuring film thickness since some deposition rates, etch rates, and thickness is determined by the ellipsometer, [35]

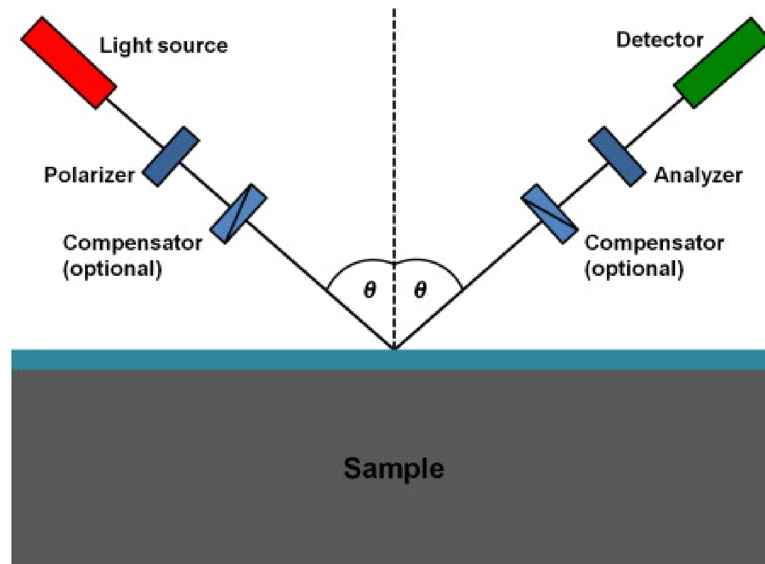


Figure 13: schematic of elliomstry setup[13]

Ellipsometer is an optical device used to investigate surface properties. The machines are fast, nondestructive, accurate, easy to use, and operate in ambient air. The technique is base on the changes in light polarization after being reflected off the surface. The reflected light will give two parameters: the amplitude component Ψ and phase difference Δ[35]. Using these variables, we can find thickness, doping density, electrical conductivity, and surface roughness [35]

4.9 Scanning Electron Microscope

Scanning Electron Microscopy (SEM) focuses an electron beam on one part of the sample and produces an image based on the electron reflected from the sample and then hits the detectors [14]. The two common types of electron detectors in an SEM, which detect either Back-scattered electrons (BSE) or secondary electrons (SE) depending on the mechanism of their origin [14]. The BSE is caused by elastically scattered electrons, while SE is caused by inelastically scatter. Electron scattering angles are different for SE and BSE. Detectors is be set up to detect either BSE or SE and then create an image from BSE or SE. SE gives a clearer image and information about the surface since the electrons are reflected from about 100 nm depth. For BSE, the electrons originate from about 1µm and can give more data about conditions slightly deeper into the sample. x-ray and auger electrons are also scattered but will not elaborate on them here. [36]

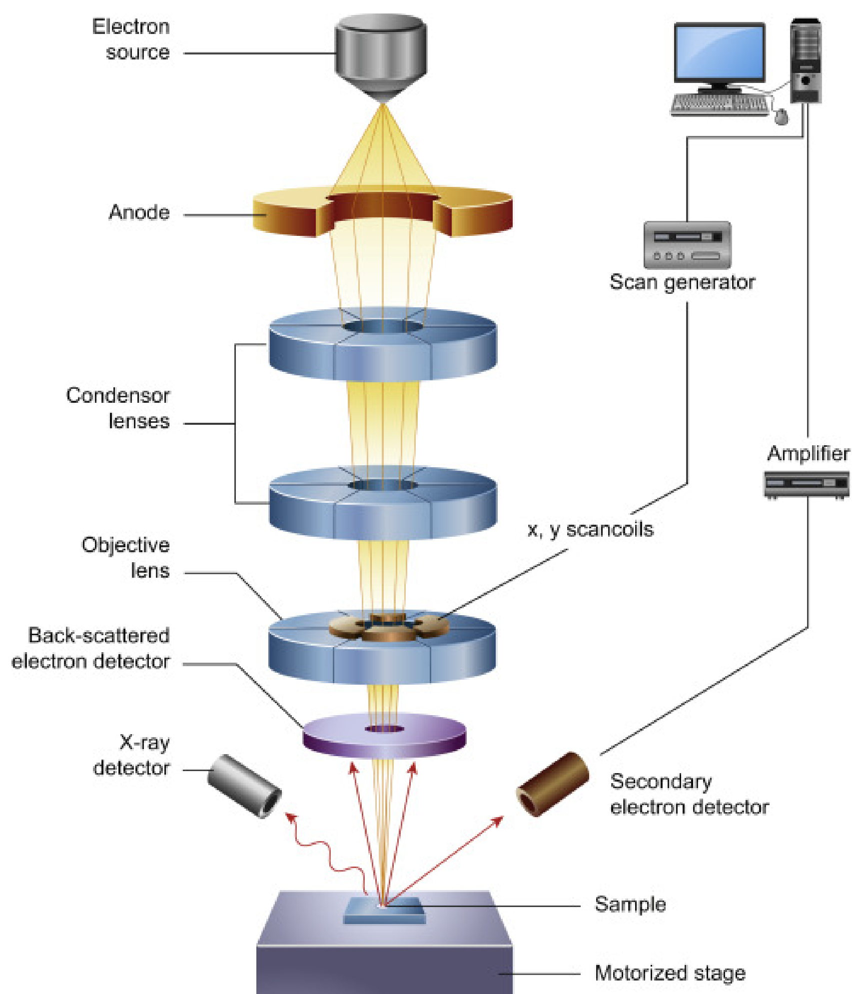


Figure 14: schematic of Scanning Electron Microscope [14]

4.10 Transmission Electron Microscope

A transmission electron microscope is not used in this project, but the microreactor is made to be operational in a TEM. It is therefore useful to have a short description of how a TEM works. The focus in this subsection is to give a background for how the TEM affects the requirements for reactor dimensions and design.

Transmission Electron Microscope is an electron microscope that works by having electrons pass through a sample and project an image on a fluorescent screen, with a resolution high enough to study features in the atomic range [37]. For electron transmission, typical sample thicknesses range from 100nm to 200nm, and thick samples do not allow the electrons to go through a sample [38]. In recent decades, the TEM characterization has moved from static to allow in situ characterization while applying external gas/liquid flow, heat, stresses, and electrical bias [39]

The sample is placed in a TEM holder, and there are several different variations in sample holders to accommodate different sample geometries, sizes. Also, TEM holders can be

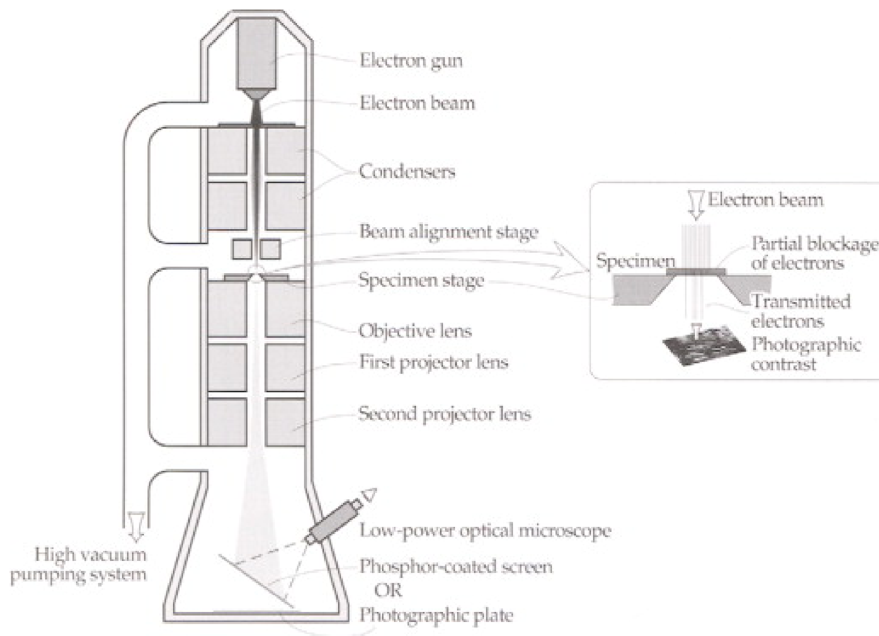


Figure 15: schematic of Transmission Electron Microscope [15]

made to apply gas/liquid flows, heating, or mechanical stresses if needed during the TEM characterization. [40][41][42]. While sample dimensions vary depending on the manufacturer, samples need to be small and typically range in a few millimeters in x and y dimensions.

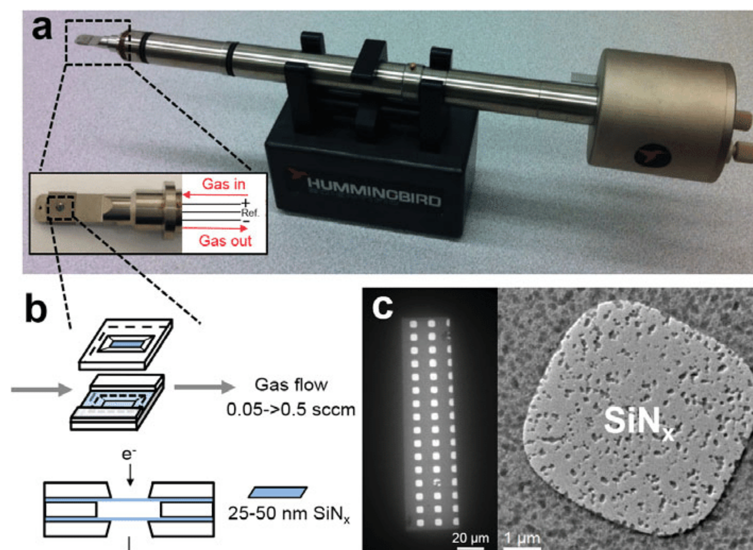


Figure 16: Picture of TEM holder
[43]

5 Method

5.1 The ALD reactor

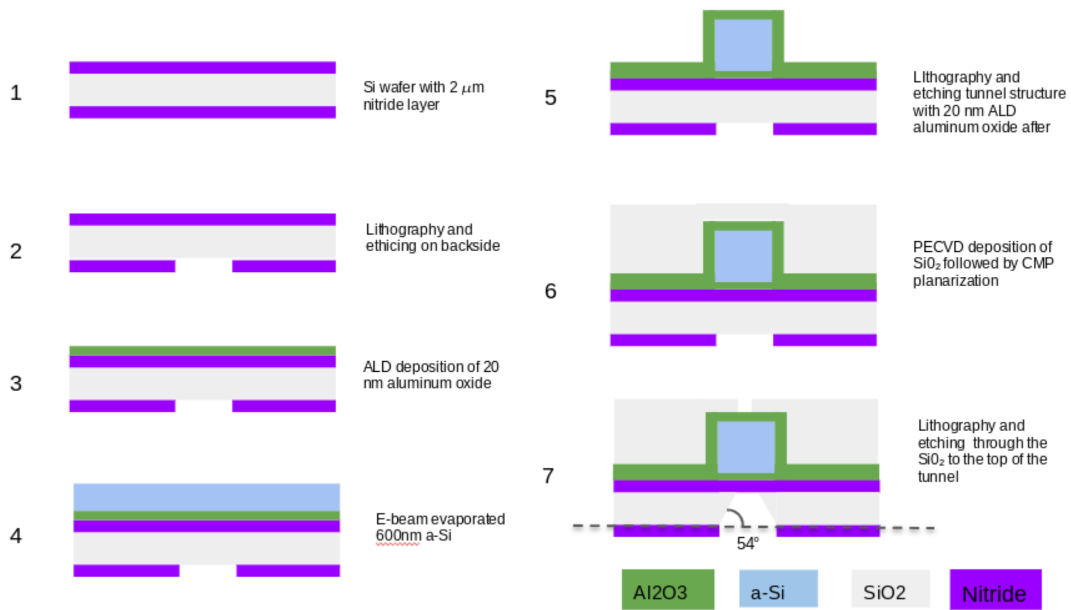


Figure 17: Main process steps for Batch 1

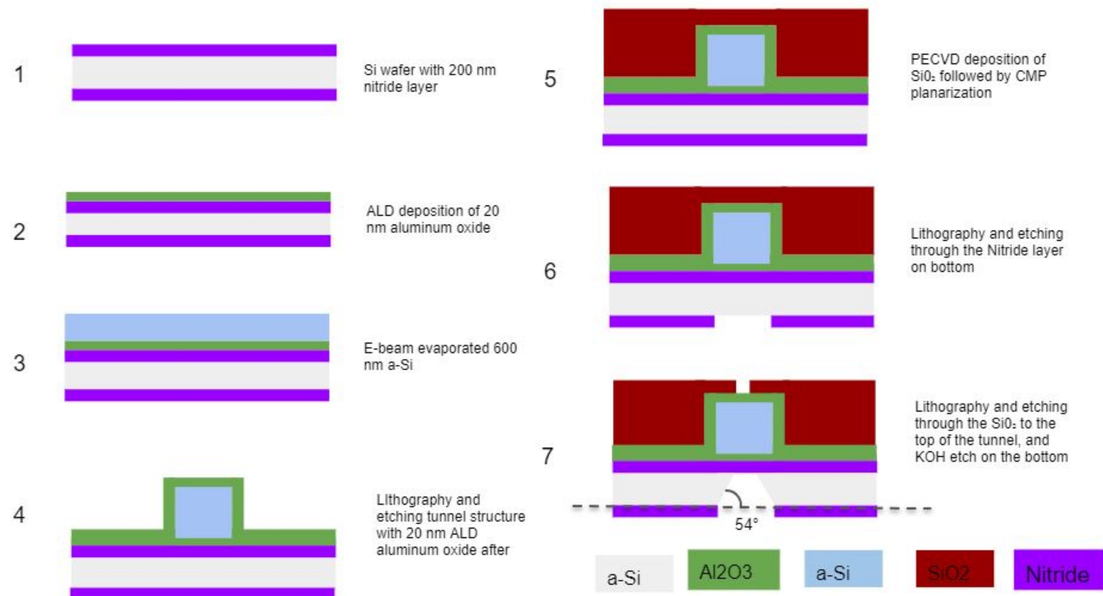


Figure 18: Main process steps for Batch 2

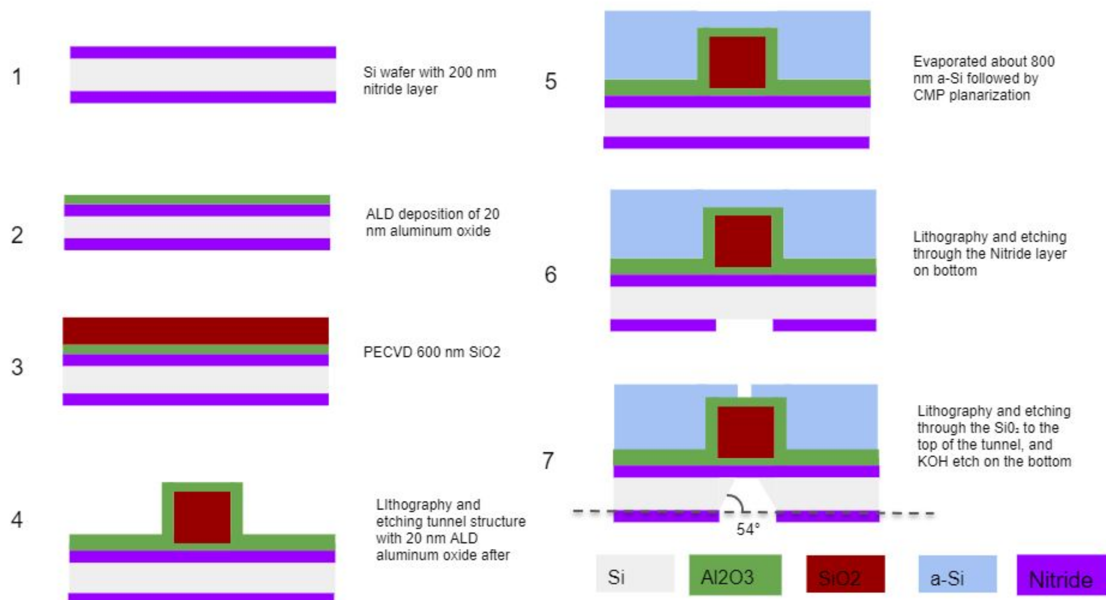


Figure 19: Main process steps for Batch 3

The final product is a small ALD reactor that fits into a TEM holder so the ALD process can be studied in situ in a TEM. The chemical reactor chamber is a series of tunnels where the material deposition will occur, and in order for this reaction to occur while inside a TEM, the structures must be in the micrometer range, and some dimensions are only a few nanometer thick to ensure a good TEM result. Fabrication of the reactor chip includes several intermediate steps such as deposition of etch stop layers and sacrificial layers and etching the structure to the desired shape. The walls of the tunnels are made of aluminum oxide, and there are layers of material over and under that function at stabilization layer. The tunnel walls and layer over and under also need to be thin enough to allow electrons to go through to achieve adequate TEM results, and therefore openings in the stabilization layer to the tunnel wall are made so electron absorption and scattering are reduced. The tunnel walls are freestanding ultra thin membrane made from aluminum oxide with a thickness of 23nm. The tunnel dimensions are approximately 600nm in height and varies width with sizes 5 µm, 7.5 µm, and 10µm.

Fabrication of the reactor chip includes several intermediate steps such as deposition of etch stop layers and sacrificial layers as well as etching to make structures with the desired shape. Several etching, deposition, lithography, and characterization steps are needed and will be explained in the following chapter. There are three different batches made in this project with slightly varying designs. The reactors are made on 4-inch wafers and is later made into several individual reactor chips. 4-inch wafers are a requirement since the available CMP sample holder only takes 4-inch wafers. Several reactors are made on each wafer since it is likely that some reactors get damaged, making several reactors per wafer not increase cost or fabrication time by much.

5.2 Sample preparation and lithography

The starting wafers is Si wafers with a polished Si_3N_4 200nm layers on both sides. The Silicon nitride serves as a etch stop layer in later KOH etching. In the first batch that consist of 3 samples, backside patterns for the KOH windows are put on first. The backside of the sample is plasma cleaned for 3 min with O_2 at full power(40kHz) and flow rate (200sccm) removing contaminants before backside lithography. The sample is then put on a hotplate for 5 min dehydration bake for at 115°. With as little delay as possible, the sample is spin coated with approximately 800 nm SPR700 photoresist, and a pre exposure baked at 95°for 1 min. The sample exposed in a Heidelberg MLA 150 for exposure at a dose of 100 mj/cm^2. Post exposure bake is then done at 115°C for 1 min. After the pattern is developed by immersing it into mf-26a developer for 50 seconds after it is put in DI water and dried with N_2 gas. Backside pattern and etching were done were the first fabrication steps for batch 1, but for batch 2 and 3 have been moved until after front-side pattern were completed

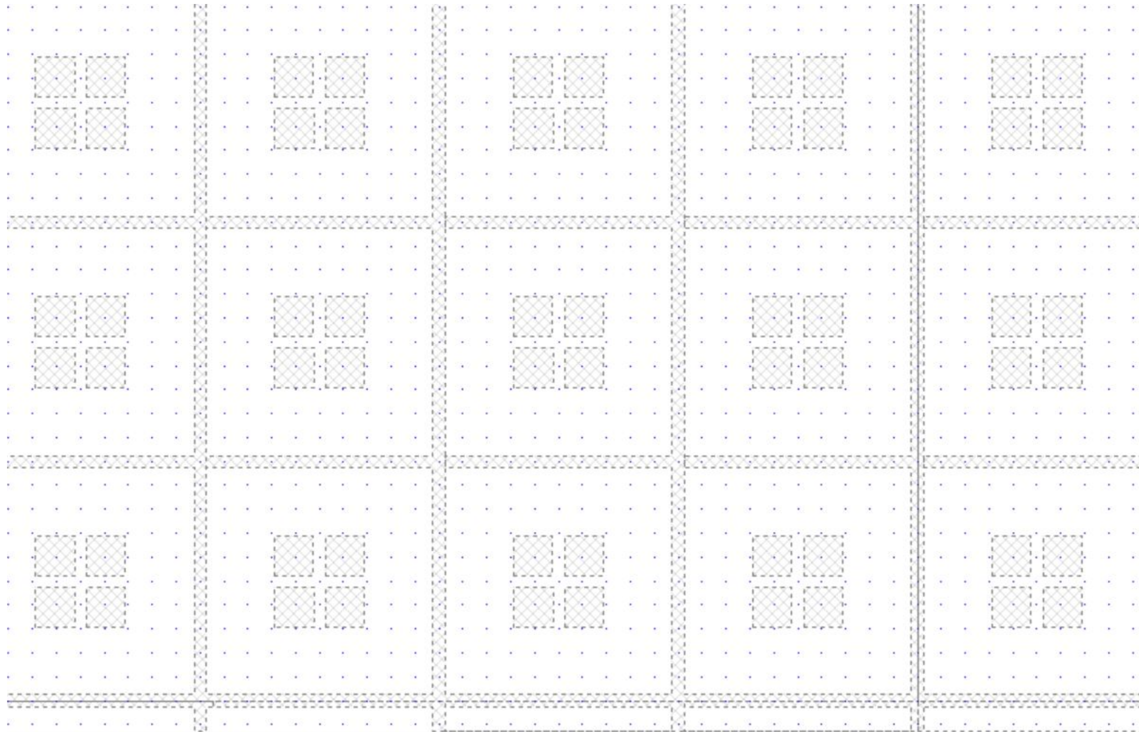


Figure 20: KOH window mask. One square with four windows inside is corresponds to one chip.

The lithography is done with SPR700 photoresist, the steps are done as in table 2. The photo-mask put on, is the mask for the KOH etch on the backside. The pattern after etching can also be seen in figure 38

Process step	Process description
Dehydration bake	Hotplate for 5 min at 115°
Spin coating	SPR700 resist spinned at 4000 for 31 sec
Soft bake	Hotplate 95°for 1 min
Exposure	Exposed with dose 100 mj/cm^2
Post exposure bake	Hotplate at 115°for 1 min
Developing	Developed mf-26a for 50sec and put in DI water

Table 2: Steps for for lithography with SPR700 resist. Dyhadration bake can be changed for Plasma Asher in batch 2 and 3

5.2.1 Nitride etch

The sample is loaded into the ICP RIE and etched for 4min 10 sec with a fluorine based nitrite etch recipe from Table 3. The etching is sufficient to etch through the 200nm silicon nitrite layer and is then over etch a few nanometers into the silicon dioxide underneath. After the ICP is finished, the sample is soaked in acetone in an ultrasonic bath, rinsed with IPA and dried with nitrogen gas. The reason for the ultrasonic bath is that acetone and plasma cleaning did not remove all the resist. The sample is also cleaned in the plasma cleaner to prepare it for ALD deposition

Name	Jens si Nitride etch
Gas	SCCM
O_2	7
CF_4	10
CHF_3	50
Pressure	22 mTorr

RF Generator	
Forward power	175W

ICP Generator	
Forward power	0W

Table Temprature	20°C

Table 3: Process settings for Silicon Nitride etch

5.2.2 Aluminum oxide deposition front side

The aluminum oxide layer is deposited with ALD using TMA and water vapor for 200 cycles producing a layer of 22.8nm. The temperature of the chamber is 160°Celsius and

it takes 1 hour 15 min for the whole process. The machine can be loaded and started and left for the duration of the ALD process produces consistently the same results for specific numbers of cycles. The ALD can take two 4inch samples at the time, but will however deposit some Al_2O_3 on the backside. The backside deposition is not uniform and decreases the closer to the center. To rectify this problem, a clamping system in figure 21 was devised so only deposition on one side occurs. The clamping works by having a steel plate with several threaded holes so clamps can be placed and tightened. So no gas is deposited on the backside a dummy wafer is placed between the steel plate and the backside of the sample. Reflectometer measurement on the backside after deposition with clamps, no deposition on the backside occur. Although the error margin of the measurement indicate that it is possible that some aluminum oxide is deposited, it is not enough to be measurable.

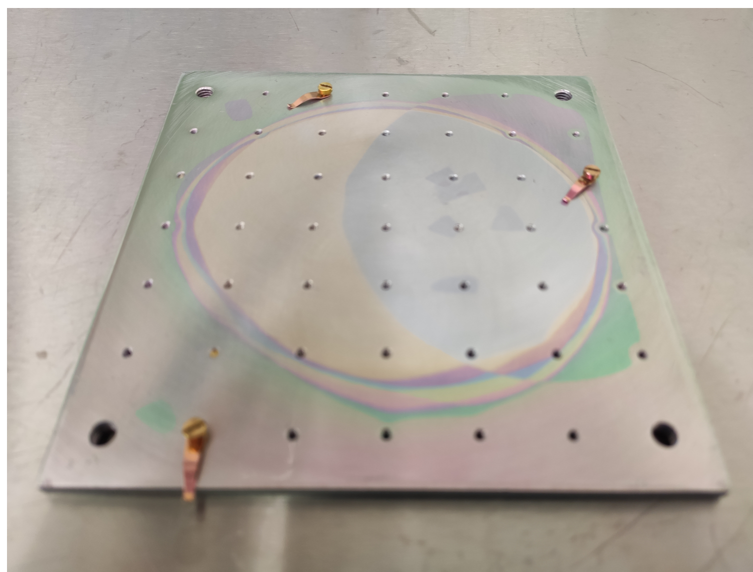


Figure 21: Clamping plate. One dummy wafer is placed under, and sample is placed on top with desired deposition side facing up

5.3 Amorphous silicon deposition on front side

There are several machines at NTNU that should be able to produce a-Si thin films, and PECVD, and E-beam evaporator was both tested to to find what was the optimal process to run. Both came with benefits and drawbacks. The evaporator give consistent results, and shorter process time, there are a few imperfection in the film. The PECVD require longer time for the same thickness compered to evaporation. it takes slightly more than 3 hours to get 600nm thickness with PECVD compared to 1 hour with evaporation. The biggest issue with a-Si deposition with the PECVD is the inconsistency of the final results. PECVD on two inch wafer gives the highest quality film, but on four inch wafers produce low surface adhesion where it de-laminate from being handled with tweezers. Test were run on a 2inch Si wafers placed on a 4 inch carrier wafer and this had high quality surface used to for finding deposition time and etch rate for a-si. Because the CMP

sample holder available only hold 4 inch wafers, a way to make a-si on 4 inch wafers were needed. Three 4 inch samples with deposition thickness corresponding to 200,400,600 nm all had poor surface adhesion and would delaminate. Efforts were made to find the cause for the insufficient results, and try to get consistently good results with the PECVD. Initially the 4 inch wafer look good at visual inspection, but would degrade over a several hours until the surface looks like figure 30. four 4 inch samples were tested, all having the same result. However, no changes to the process yielded consistently good results with the PECVD. Therefore the evaporator was chosen to be the best machine for a-Si deposition. A important requirement for the a-Si layer no or little delamination in the CMP step, and the evaporated a-Si have very little delamination, but PECVD a-si showed delamination from being handled with tweezers. Solution to PECVD a-si, that were tried include changing temperature, and 180 and 300 °C, and changing gas composition

The electron beam evaporator is used to deposit a 600nm a-Si. This takes 1 hour including the handling time and waiting time. The e-beam evaporator can be used in both manual and automatic mode. Manual deposition require a operator to be present during the whole process, but in automatic mode the machine can be left unattended when running already tested recipes. The e-beam requires several operator inputs during the process. After shutting down the vacuum pump, the waiting time is 8 min before opening a valve, so the process chamber door can be opened. Loading is then done, an additional waiting time of 8 min is needed before the processes can be started. For 600nm, the deposition takes 30 min. After deposition, the time is another 8 min for the the pressure to reach atmospheric, before unloading can be done. deposition rate for the recipe was set to 5 Å/s in automatic mode, but when doing it in manual mode a around 10 Å/s was used. So it is faster to use the machine in manual mode, and although it could be run at higher deposition rate during automatic mode it was not tried because of limited samples. The deposition rate did not affect the quality of the a-si film in a way that was noticeable. The automatic mode is preferred because the machine can be left unattended while deposition occur, so parallel work can be done.

5.3.1 ALD to make hydroxide layer

The SPR700 when directly put on a-si were would slide off during development with mf-26a. To fix this problem a addional ALD step to running 1 cycle aluminum oxide were added. The ALD recipe run 10 cycles of only water vapor at 160°C which adds a hydoxide layer on top of a-si layer. This layer were sufficient to stop problems with the resist in the next lithography step.

5.3.2 Photo Lithography front side

The lithography step is the same as the previous one and won't be repeated for brevity. The only difference is the mask design. The mask design is the tunnel design seen in figure 24. The pattern used lines of with width 5,7.5 and 10 µm . The lines are aligned

with the backside with the help of alignment markers on the backside of the sample in batch 1. In batch 2 and 3 this photo mask require no alignment since it is the first mask for batch 2 and 3.

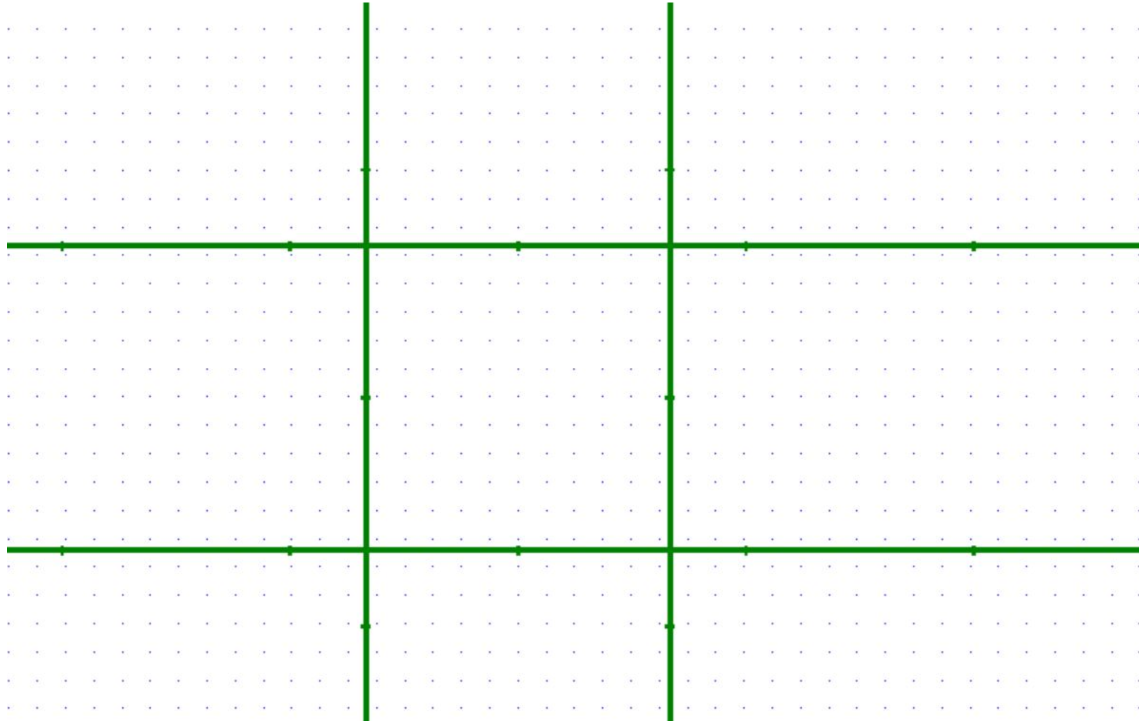


Figure 22: Tunnel mask for one chip. Note the Cross-junctions that are for the vapor etch holes. The whole mask is repeating units of this design, but with varying tunnel width

5.3.3 Etching and PECVD

The wafer is loaded into the ICP RIE etcher for etching and the recipe used is SF_6 and CHF_3 at flow rates 7.5 and 50 SCCM.The etching time is 3min, which is a slight over etch but the aluminum oxide layer acts as a etch stop layer. Were over etching meaning etching is done for a longer time than is necessary for a given etch depth to ensure all material is removed. The etch rates are found by measuring before and after etching with a reflectometer.

Name	Jens Si etch SF6 + CHF3
Gas	SCCM
SF_6 CHF_3	7.5 50
Pressure	15 mTorr

RF Generator	
Forward Reflected Power	40 1
DC bias	200v

ICP Generator	
Forward	600W
Reflected Power	1W
Table Temperature	20°C

Table 4: Process settings for Silicon etch

After the etching the photoresist is removed with acetone and IPA before being dried with $N2$gas.

Next the PECVD is used to deposit 930 nm SO_2 layer. A slightly thicker layer than needed is deposited, because in subsequent CMPing step it is faster to remove excess thickness, then to add additional thickness

Name	OPT SiO2
Gas	SCCM
SiH_4 N_2 N_2	8.5 710 161.5
Pressure	1000 mTorr

RF Generator	
Forward power	20W

LF Generator	
Forward power	0W

Table Temprature	300°C

Table 5: Process settings for Silicon dioxide Depostion

5.3.4 Elipsometer measuring and CMP

The Sample is transported out of the NanoLab to Trånslate lab for thickness measurements, performed at several location on the wafer to account for thickness differences. Then, the wafer is CMPed for 50 seconds and cleaned before it is measured again to check thickness, and this step is repeated on the sample until the desired thickness is achieved. The cleaning of the the sample is done immediately after CMPing. First, the sample backside and frontside is rinsed with DI water before being dried with N_2 gas. Then IPA is applied on top and the wafer is wiped with cleanroom wipes. The sample is then put in IPA and cleaned in ultrasonic bath and dried again with N_2gas. The cleaning is done to improve the results obtained by the ellipsometer, but it does not clean the sample sufficiently for subsequent Al_2O_3 deposition and a HF clean is necessary after the final CMP step is done. This cleaning step were needed for all 7 samples in all the batches.

Based on the measurements, the material removal rate can be estimated. Since the samples have hills and valleys before CMPing, the initial removal rate is slightly higher before planarization is performed.

5.3.5 HF clean

After CMPing the wafer needs to be to be cleaned. Attempts to remove contaminates with plasma, acetone, IPA, and sonic baths was insufficient, and HF was used to remove contaminants. The front side needs to be protected from HF etching since HF will remove the front side structures. Buffered HF was used and samples was submerged for approximately 30 seconds in the solution until clean.

5.3.6 Al_2O_3 ALD deposition on both sides

The ALD deposition 20 aluminum oxide is done on both sides of the sample and at this time a slight modification to the ALD process was introduced to stop deposition on the backside a clamping system was used so a uniform layer is deposited. This clamping system is a steel plate with screw holes for clamp fastening. A dummy wafer is put on the steel plate and the actual sample is placed on top of the dummy wafer and clamps are fasted so no or little deposition occur on the backside. This modification produces the same quality film on the front side without any deposition on the backside, but does increase fabrication time since only one sample can be processed at the time. However without the clamping system the backside deposition is unevenly deposited on the backside and with thicker layer on the circumference and thickness decreasing further in to the center, producing a uneven layer. The uneven backside deposition can cause some problems with uneven etching later on because of difference in thickness. Also in some ALD steps we only want aluminum oxide on one side. The aluminum layer on both sides acts a protective layer in the xenon difluoride etch, and in the forKOH etching on the backside it could increase the etch resistance.

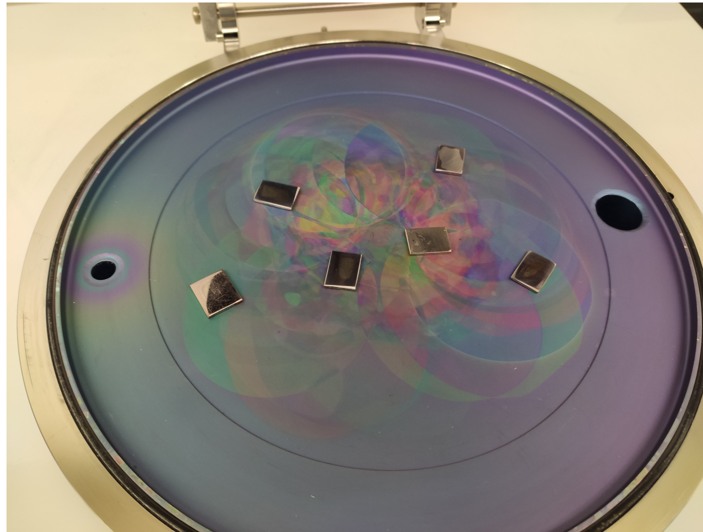


Figure 23: Sample is placed on the steel pieces to have uniform deposition on both sides at the same time

5.3.7 Lithography and etching to open the holes for Xenon difluoride etch

To allow XeF_2 etch to remove the α silicon inside the tunnels, holes need to be etched into the tunnels. The lithography steps was done as described earlier, but the exposure was done with the holes mask in figure 24 as photomask. After the holes need to be etch and the underneath layers are 23nm Al_2O_3, 200 nm SiO_2, $and 23 nm Al_2O_3$. To get trough all the layers the 3 etch steps are needed. These 3 layer are the top aluminum oxide layer and the silicon dioxide layer underneath, and last the tunnel walls. A fourth etching step is also done to etch into the sacrificial a-Si layer, so the Xenon difluoride vapor etch time is reduced.

Name	OPT SiO2 etch
Gas	SCCM
Ar	25
CHF3	25
Pressure	30 mTorr

RF Generator	
Forward power	1000W

ICP Generator	
Forward	200W

Table 6: Process settings for Silicon dioxide etch

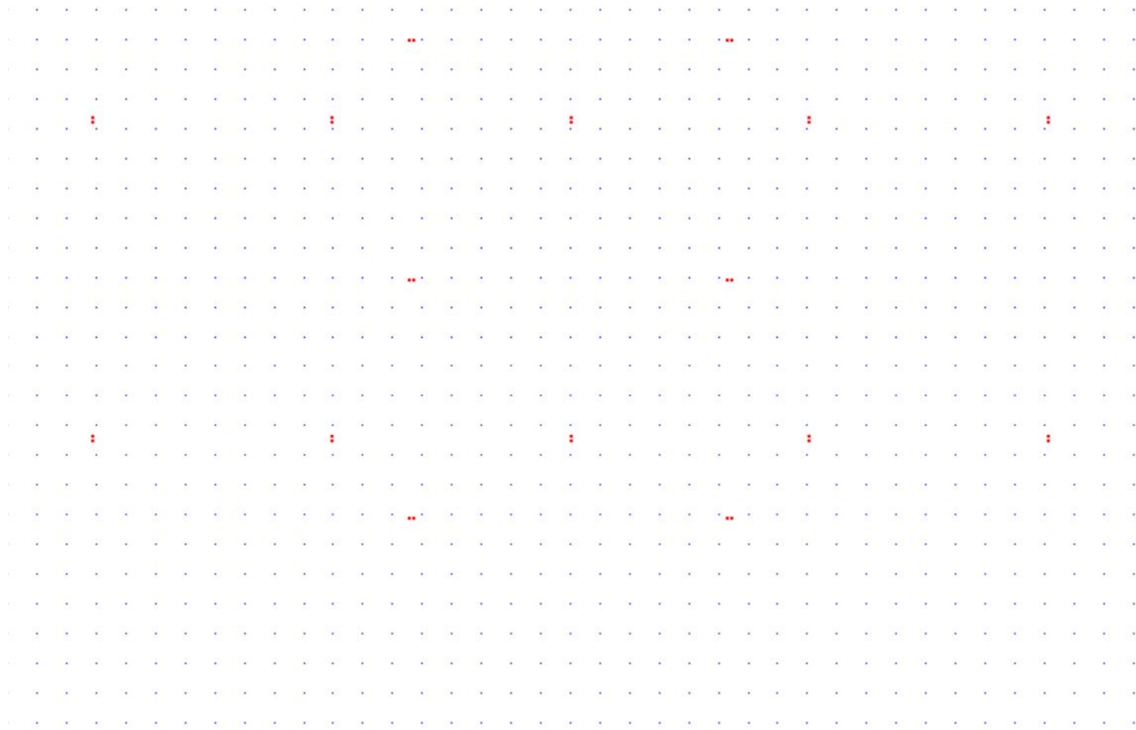


Figure 24: Hole mask were the placement of holes corresponds to the cross junctions in the tunnel mask.

Name	NL Al2O3 etch si carrier
Gas	SCCM
BCl_3	10
Cl_2	10
Pressure	10 mTorr

RF Generator	
Forward power	40W

ICP Generator	
Forward	700W

Table 7: Process settings for Aluminum Oxide etch

5.3.8 Xenon diflouride etch

With the holes open the the samples are ready for XeF_2 etching, and since Al_2O_3 is not available at NTNU nanolab, some samples are sent to Bergen university, and some are sent to Stanford university. The test run show done at Stanford show the etch on the hole test sample work, In order to check the vapor etch rate several etch rate test chips

was made and sent together with the reactor wafers. The etch rate test wafers is chips with a-Si layers with aluminum oxide on top. The mask in figure 25 was put on and holes were etched through the aluminum oxide layer.

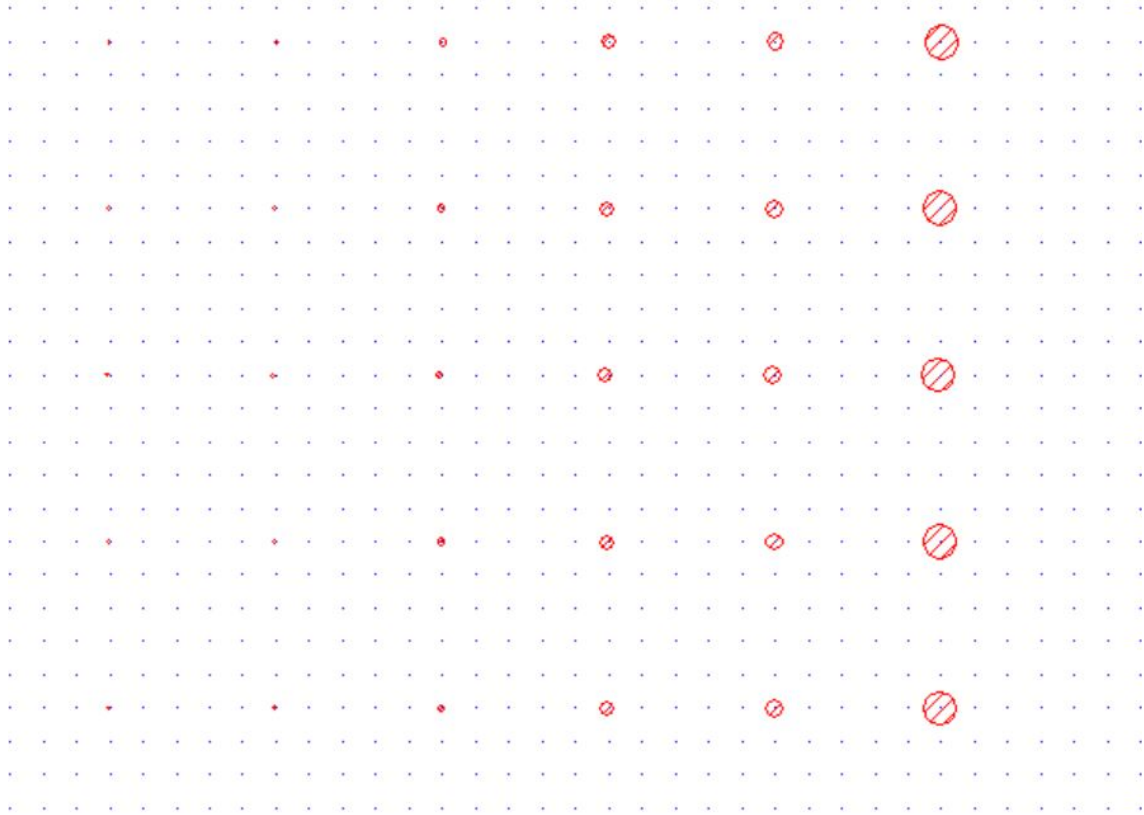


Figure 25: Holes mask for vapor etch rate test wafer.

5.3.9 Filling the holes

The holes need to be filled after XeF_2 etching, but this is the only step not tried, since samples did not return in time to try this step.

5.3.10 Front side windows

The front side windows are the openings that expose the tunnels from the top side of the wafer. These windows are made by doing a lithography step as described earlier with SPR700 resist at 100 mJ/cm^2 exposure dose. Then the aluminum oxide layer is etched in the ICP RIE cryo with the aluminium oxide etch. The etch is 10 SCCM of both BCl_3 and Cl_2 for 60sec. The top layered of Al_3O_2 is then slightly over etched into the SiO_2, and the SiO_2 etch is done in the ICP RIE chiller. The thickness varies slightly for each sample since the SiO_2 layer after CMP is slightly different on each sample, but a 5 min

etch is sufficient for all of them, and the Al_2O_3 works as an etch stop layer. The Al_2O_3 etch rate was tested, but the etch rate was too low to be measured accurately, and it is certain that the over etch does not remove more than 1-2 nm.

5.3.11 Potassium hydroxide etch

The KOH etch is done to etch the backside windows to open up the surface of the tunnels. The sample is spin coated on the front with a protective layer to protect the sample from unwanted etching on the front. The protective layer is first ProTEK B3 Primer product and then ProTEK B3 product series. The sample is the submerged in a 20% KOH bath at 80 °C and etched for 8 hours with a physical clamping protecting the front side if the wafers are 4 inch if individual chips are etched a protective layer is spin coated instead. The physical clamping only fits 4 inch wafers, and has the benefit of being faster.

6 Results

6.1 Process times and cost

Fabrication Step	Fabrication step note	Total fabrication time
ALD alumimin oxide depostion	23 nm thickness	1 hour 15 min
Evaported a-Si	600 nm thickness	1 hour
Put on Hydroxide layer in ALD		15 min
Lithography with tunnel mask		30 min
a-Si etch	Etch down to aluminum oxide layer	40 min
PECVD SiO2	930 nm thickness	60min
Ellipsometry		10min
CMP	450 second total	10 min
Ellipsometry		10 min
ALD alumimin oxide depostion both side	23 nm thickness	1 hour 15 min
Lithography with holes mask		30 min
Aluminum oxide etch	Etch down to SiO2 layer	30min
SiO2 etch	Etch down to tunnel wall	40min
Aluminum oxide etch	Etch through tunnel wall	30min
a-Si etch	Etch into tunnel	30min
Backside lithography with KOH window mask		30min
Aluminum oxide etch	Etch down to Silicon nitride	30min
Silicon nitride etch	Etch down to Silicon layer	40min
KOH etch	Etch along 100 plane to tunnel wall	8 hours
Xenon difluoride vapor etch	Remove all a-Si from tunnels	Not done at NTNU
Refill holes		
Scribe sample into reactors chips		

Figure 26: Fabrication time for each process. Rounded up to nearest 5min. Cleaning and characterization is not included

Taking times for the process and knowing which processes can be left unattended is useful for planning the labwork and for doing different wafers on different machines in parallel. It saves time in the long run by having data for better structuring of the work. The times can also be used to estimate the total cost for a prototype beforehand, since NTNU nanolab charges money for the time spent on each machine for certain users.

The following tables here give the times for each process step for the various machines

used. The constant/variable is for indicating if the process step is constant for all samples run or can be changed by, for example, (but not limited to) deposit a different material or etch for longer/shorter time. Some of the handling time can differ depending on the operator or have small variations by the same operator, but tend to be approximately the same for experienced operators and is therefore left as a constant.

Process Step	Time (min)	Require operator to be present	Constant/variable
Loading and setup	2	Yes	Constant
Cleaning step	3-5	No	Variable
Unloading and shutdown	2	Yes	Constant

Table 8: Plasma Cleaner

Process Step	Time(min)	Require operator to be present	Constant/variable
Spin coat 31 sec SPR 700	5	Yes	Variable
Pre exposure bake	1	Yes	Variable
Loading into MLA and starting	5	Yes	Constant
Exposure	15-30	No	Variable
Unloading from MLA	3	Yes	Constant
Post bake 105°C for 1min	1	Yes	Variable
Developing (MF-26a)	5	Yes	Variable

Table 9: Lithography

Process Step	Time (min)	Require operator to be present	Constant/variable
Venting and loading	4	No	Constant
Etching	1-15	No	Variable
Pumping/Purging	20	No	Constant
Venting Unloading	5	Yes	Constant

Table 10: ICP RIE

Process Step	Time (min)	Require operator to be present	Constant/variable
Venting and loading	4	No	Constant
Deposition	10-30	No	Variable
Pumping/Purging	20	No	Constant
Venting Unloading	5	Yes	Constant

Table 11: PECVD

Process Step	Time (min)	Require operator to be present	Constant/variable
Venting	10	No	Constant
Loading and pumping down	10	Yes	Constant
Deposition	20	Yes	Variable
Venting	10	No	Constant
Unloading and pumping down	10	Yes	Constant

Table 12: E-beam evaporator

Process Step	Time (min)	Require operator to be present	Constant/variable
Venting and loading, evacuate	5	yes	constant
Running pre dep. steps	15	no	constant
Depostion 200cycles Al_2O_3	50	No	Variable
Venting unloading	5	Yes	Constant

Table 13: ALD reactor

In Table 14, the cost for NTNU academic users are given. For the master students users it is possible to pay a flat rate for of 200 000 kr/year for access to the machines, but the Table 14 is for the other options, which is hourly paying for the use. There are higher pay rates for industrial users, but the same tables would apply for them only with different rates. NTNU NanoLab only booking 30 min blocks are possible so time is different from earlier tables since it is rounded up to nearest 30 min. The cost of using things such as resist is include in the cost of using lithography, and for some machines like plasma cleaners are free to use, and CMP is not included since it is located in a different lab.

Process	NOK/hour)	Required booking	Total cost
Lithography	600	1.5	900
ALD	300	3.5	750
Evaporator	600	1.5	900
ICP RIE	600	5	3000
PECVD	600	1	600
Totalt		12.5	6150

Table 14: Price list for academic users NTNU nanolab, and the cost of batch size of 1

6.2 Etch rates

The aluminum oxide etch rates were also tested with an ellipsometer, but the profilometer gave consistent results and therefore later etch rates are only found with reflectometer. The Si_3N_4 thickness was measured with a profilometer. To get the most accurate etch rate, it is preferable to use long etch times with sufficiently thick layer to ensure not all the material is removed by the etching. When etch rates were calculated in the lab, there

were instances of unmeasurable material removal when the etching time was only a few seconds indicating that the plasma needs a few second to stabilize before etching to start. For this reason, high etch rates and short etching time can be considered undesirable since it can be hard to stop at the correct etch depth.

Finding the etch times varies depending on the material, but for example the aluminum oxide needed 2 hours and 15 seconds to deposit 57nm, and an additional 40 min in the ICP RIE to etch for 30 seconds. Similar results as seen for batch 2 sample 1 is found for other samples as well, but the higher MSE in batch 1 gives slightly more unaccurate data, but show the same effect. For sample 2 in batch two no good messurment could be achived with ellipsometer, but the sample was CMPed for 450s in one cycle, and is hopefully at the same thickness as sample 1. No other characterization technique were used to verify the results, but processing on sample 1 continued. Sample 1 can still be verified in SEM after individual reactors have been scribed and crossection can be checked.

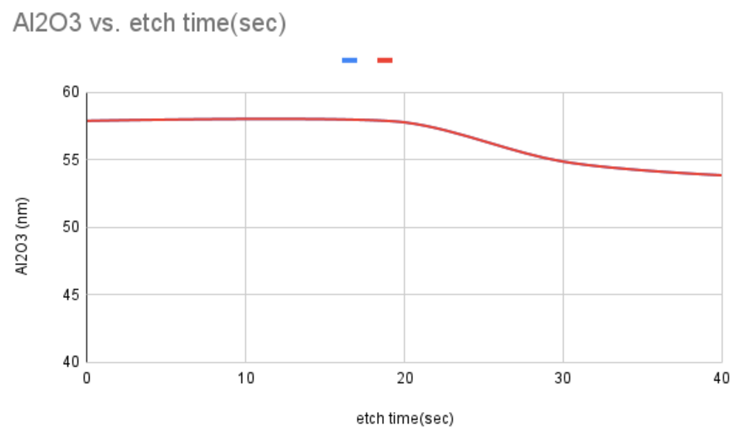


Figure 27: Etching vs time for aluminum oxide etch

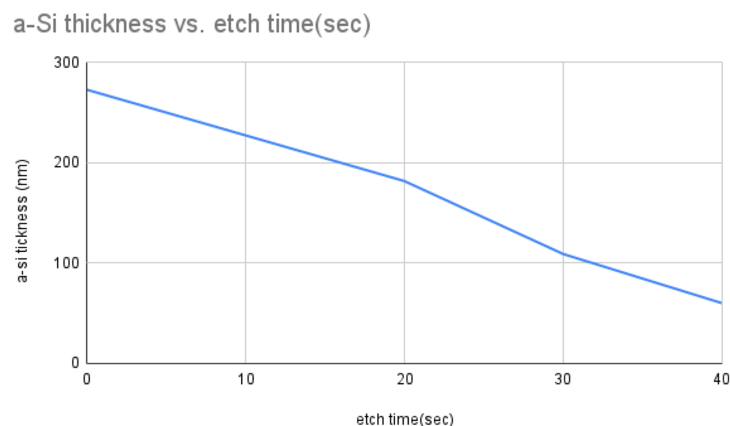


Figure 28: Etching vs time for the amorphous silicon etch

Material etched	Etch rate
αSilicon	5.357 nm/s
SiO_2	0.675 nm/s
Al_2O_3	0.4 nm/s
Silicon nitride	0.769 nm/s

Table 15: ICP RIE etch rates for etched materials

The etch rate for the the 200nm thick silicon nitrite layer was found by etching and measuring with the profilometer. The etch rate found for silicon nitrite was 0.769 nm/s and therefore it takes about 4 min 30 sec to etch through the layer. Since under etching will cause problems since KOH etching later on will not be able to etch through the Silicon nitride, and over etching is preferable to ensure the silicon nitride layer is removed. Over etching does not affect later KOH etching. The total etch time were 4 min and 40 seconds.

6.3 Deposition rates

The aluminum oxide deposition rates found with the ALD was 28.9 nm/hour . In addition a 15 min pre and post deposition step are required when running the machine.

The deposition rate for the evaporator is 5 Å/sec. For the evaporator the deposition rate can be changed directly in the machine and can be for the machine at NanoLab up to 5 Å/sec. The quality of the film is fairly good, but does have a few imperfection so on each sample there are some reactors that cannot be used. This is however not a big problem since most of the structures are fine, and several reactors are made on a single wafer.

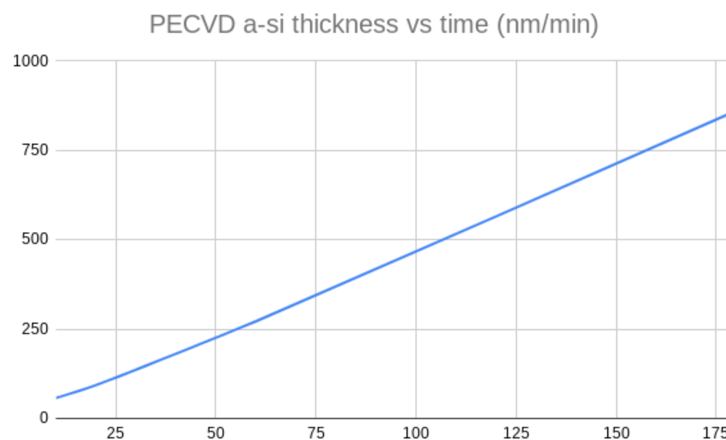


Figure 29: PECVD amorphous silicon depostion rate

The deposition rate for SiO_2 was 77.5 nm per min, and on all samples the deposition rate were constant for all thicknesses tried.

6.4 Lithography

The pre- and post lithography steps are very hands on. The spin coating, baking, and the developing are processes that are more efficient by doing the whole batch at once. Especially the developing that require hazardous chemicals is improved by doing the whole batch at once, since the time spent taking on and off protective gear is reduced. Also the handling of dangerous chemicals are reduced, which increases the safety and saves money since developers tend to be expensive.

6.5 Amorphous silicon on PECVD vs Evaporator

The amorphous silicon could be deposited by both PECVD and Evaporator. The highest quality results was achieved with PECVD, but there was a high chance of problems with the surface as seen in figure 30. A considerable amount of time was spent on trying to get consistent good results with the PECVD. Since the high film quality of the PECVD would have been beneficial for the CMP step later on, but the randomness of quality made the evaporator the main choice. It would have also reduced overall batch fabrication time to have two processes for a-Si deposition in parallel.

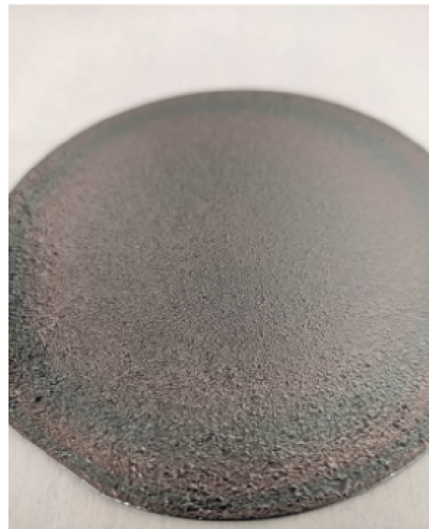


Figure 30: PECVD amorphous silicon surface adhesion failure

6.6 Adhesion problems for SPR700 resist

The initial lithography and use of SPR700 was successful without any problems, but when applying SPR700 photoresist on amorphous silicon, the developing with mf-26a developer caused the resist pattern to deform and slide across the sample. The reason for this could be caused by Tetramethylammonium hydroxide (TMAH) in the developer

etching the the amorphous silicon. The developer data sheet claims Tetramethylammonium hydroxide (TMAH) should be around 2.3 % and TMAH etches silicon even at low concentrations,however when used for etching the temperature tends to be higher since increasing temperature increase the etch rate [44]. A experimental number for the etch rates for TMAH for 20 °C was not found, but it is likely to be low since temperature at lab is 20 °C, but still a likely cause for the adhesion problems. The problem was solved by making a hydroxide layer on top of sample before applying the photoresist. No adhesion problems occurred after this was done. The hydroxide layer was made by putting the samples into the ALD and running 10 H_2O cycles at 160°C with 1 cycle of Al_2O_3. There are other options to make the hydroxide layer but the ALD was used since it was available at the time. The one cycle of 1 aluminum oxide is so thin that it is likely not to effect the later fabrication steps, and were only put on since no recipe changes were needed when one cycle were applied. If more samples were needed to be fabricated this one aluminum oxide layer could be removed, and only have put on hydroxide layer.

6.7 Cleaning the sample

The sample needs to be cleaned sufficiently at several stages during the processing. On initial steps with batch 1 acetone, IPA, and/or plasma cleaner with O2 was used. For batch 2 and 3 Plasma cleaning was used to both clean and remove the resist. Using the plasma cleaner for resist removal and cleaning did not give a noticeable cleaner surface, but did save around 5-10 min per cleaning step required.

6.8 Buffered Hydrogen Fluoride etch after CMP

Batch 1 after CMPing was initially cleaned in a ultrasonic bath with acetone and then IPA before being cleaned with oxygen plasma. This was shown to not be as effective as expected and ALD deposition of Al_2O_3 only partially stuck as can be seen in 31 and 32. Therefore, a buffered HF solution was used to clean the sample remove contaminants and improve adhesion of Al_2O_3. As we can see from the 33 and 34 the HF removed contaminates. After adding the HF clean Al_2O_3 deposition had no adhesion problems to the a-silicon in batch 1 and 2, or SiO_2 in batch 3.

6.9 Design changes and changes to the process in batch 2 and 3

The first batch of reactor fabrication started with making the backside pattern first, but later fabrication steps on the front side caused the backside pattern to deteriorate. This is caused by the silicon nitride layer being sensitive, and can be damaged even by careful handling .This did not cause the whole sample to be unusable, but we did lose some chips because of damage to the backside pattern. In batch 2 and 3, the backside fabrication steps will be made at a later stages of the process after xenon difluoride etch.

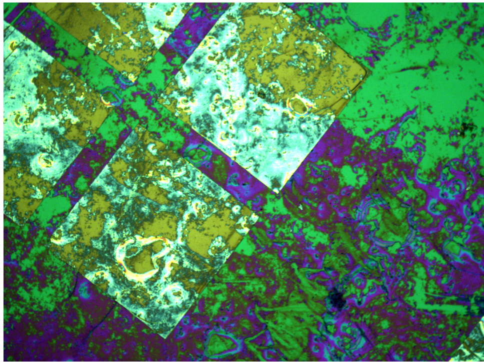


Figure 31: Backside of sample after CMP and ALD

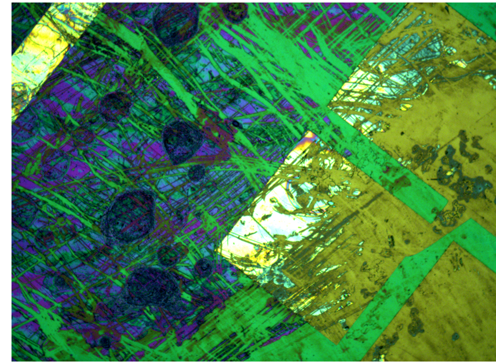


Figure 32: Backside of sample after CMP and ALD

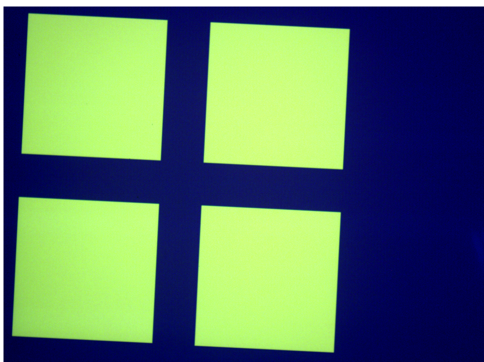


Figure 33: Backside after HF

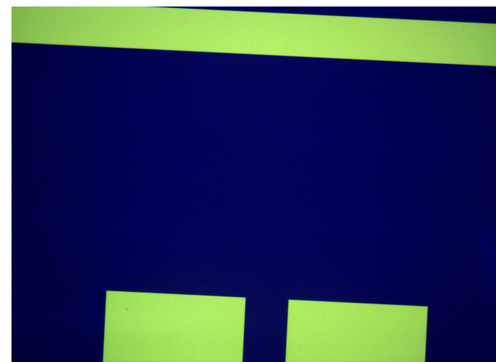


Figure 34: Backside after HF

The front-side pattern on batch 1 was harder to measure with the ellipsometer and the measurement had high mean square error. Increasing the uncertainty of the results, also the pattern had both SiO_2 and α-silicon in the top layer and this caused an uneven polishing in the CMP as a result of different material removal rates. The CMPing was tried with different concentration 1/3 and 1/5 for the slurry mix, and this reduced the difference in the material removal rate. This can be taken as evidence for the slurry being the the biggest factor in the difference in material removal rate. This is expected as depending on type of material some are more sensitive to chemical vs physical removal and vice versa. Finding a combination of slurry mixture and setting for the mechanical abrasion so both material are removed at the same rate can be difficult to calculate, and must be found experimentally.

6.10 Chemical mechanical polishing

CMP is the process step that has the most varying result and is the cause for some design changes. Since the CMP sample holder only holds 4 inch wafers it is the cause for 4 inch wafers being the sample size the reactors are made on. Also because of the forces that the sample is under during the polishing it is also a critical process step in regards to film delimitation. The CMPing is done at Trånslate lab at NTNU, which is a non

cleanroom lab, and combined with CMPing this step introduces a contaminates to the sample surface. Despite cleaning both sides of the sample after CMPing slurry is left on the sample. Sample contaminates and the change in surface topography combined with several relative thick layers, with pattering makes ellipsometry more inaccurate. Especially batch 1 had higher mean square error(MSE) in measurements with varying MSE, but typically around 130. In batch 2 and 3 MSE was reduced to around 60-73. Design change is the likely cause for MSE reduction in batch 2 and 3.

The CMP for some wafers the material removal is done step by step so more data can be gathered about the process, after each CMP step the sample is cleaned and measured. For sample 1 in batch 2 with 1/5 slurry mixture the data shows initial Material Removal Rate(MRR) is higher initially, and reduces until MR stabilizes around 0.21 nm/s, from a initial value of 0.588 nm/s. This change were expected and thought to be caused by the hills over the tunnel structures being removed at a higher rate. When the hills are reduced and the sample becomes more plane the contact area for sample and polishing pad increase, as a consequence MRR reduces. The same MRR is seen in batch 1 on the Silicon dioxide layer when 1/5 slurry mixture is used. When a 1/5 slurry to DI-water were used higher material removal rate was seen, and the MRR were 1.13 nm/s with no clear reduction in MRR with time. For batch 1 the top layer consist of both silicon dioxide and a-silicon, were difference in MR is observed for, were silicon dioxide have a higher MRR. Two samples in batch 1 were CMPed using 1/3 slurry and two samples with 1/5 slurry. The 1/3 slurry had less difference in MRR and were easier to stop at a time when the a-Si and silicon dioxide were at the same level.

Total Time CMP	Sample Point	SiO2 layer thickness [nm]	MSE		
0 second	center	930	64		
	top	926.73	67		
	bottom	934.3	59		
	left	931.6	59		
	right	930.85	64		
	avg	930.696	63		
50 sec	center	906.41	73		
	top	896.81	70		
	bottom	903.3	61		
	left	899.92	62		
	right	899.91	68		
	avg	901.27		MR [nm]	29.426
				MRR [nm/s]	0.58852
100s	center	876.39	67.8		
	top	887.84	79		
	bottom	879.96	60		
	left	876.18	66		
	right	878.76	70		
	avg	879.826		MR	21.444
				MRR	0.42888
150s	center	867.67	68		
	top	864.96	74		
	bottom	868.91	60		
	left	865.93	63		
	right	868.4	69.75		
	avg	867.174		MR	12.652
				MRR	0.25304
200s	center	852.08	70		
	top	860.05	76		
	bottom	858.62	57		
	left	855.28	66		
	right	856.76	70		
	avg	856.558		MR	10.616
				MRR	0.21232

Figure 35: Ellipsometer measurements before, during and after CMPing on batch 2 sample 1

250s	center	847.12	70		
	top	851.16	75		
	bottom	850.68	59		
	left	850.27	66		
	right	851.01	72		
		850.048		MR	6.51
				MRR	0.1302
300s	center	839.8	72		
	top	839.27	76		
	bottom	845.9	57		
	left	843.29	63		
	right	842.28	70		
	avg	842.108		MR	7.94
				MRR	0.1588
350s	center	829.89	71		
	top	832.41	73		
	bottom	833.84	57		
	left	842.01	69		
	right	834.35	70.8		
	avg	834.5		MR	10.936
				MRR	0.2187 2
400s	center	820.11	70		
	top	827.71	73		
	bottom	820.59	57		
	left	823.8	61		
	right	825.61	69		
	avg	823.564			
				MR	10.936
				MRR	0.2187 2
450s	center	809.99	67		
	top	811.91	72		
	bottom	813.96	56		
	left	815.24	60.3 4		
	right	815.45	68		
	avg	813.31		MR	10.254
				MRR	0.2050 8

Figure 36: Ellipsometer measurements before, during and after CMPing on batch 2 sample 1 continued

6.11 Photos of backside and front side

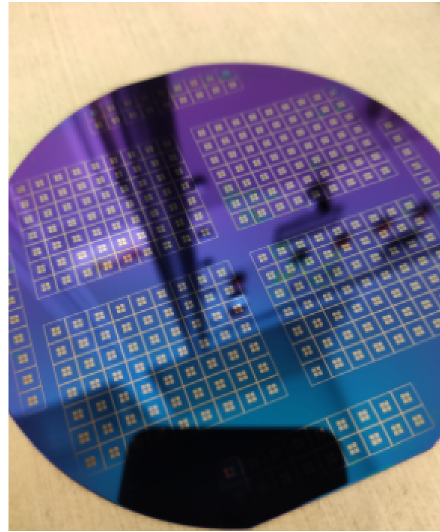


Figure 37: Picture of sample backside before first aluminum deposition

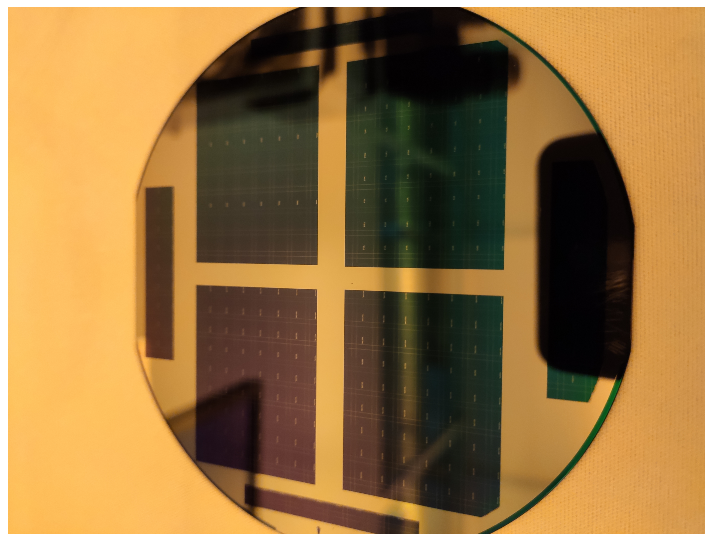


Figure 38: Picture of the front side of sample batch 1

6.12 Profilometer data

Messuruments before and after CMP with profilomter were conducted. The image profilometer in Figure 39, 44 and 41 are all from the samples with a-si tunnels in batch 2, but similar results are seen in batch 1 and 3. Figure 39 confirm that tunnel structure were made and in approximately correct dimensions. The profilometer is slightly inaccurate when going over structures, so actual value can vary slightly for profilometer data, and corssection photos in SEM the high is 570nm . In batch 2 silicon dioxide is put on as a

stabilization layer on top of a-si tunnels, and it is after the silicon dioxide depostion figure 39 is done.

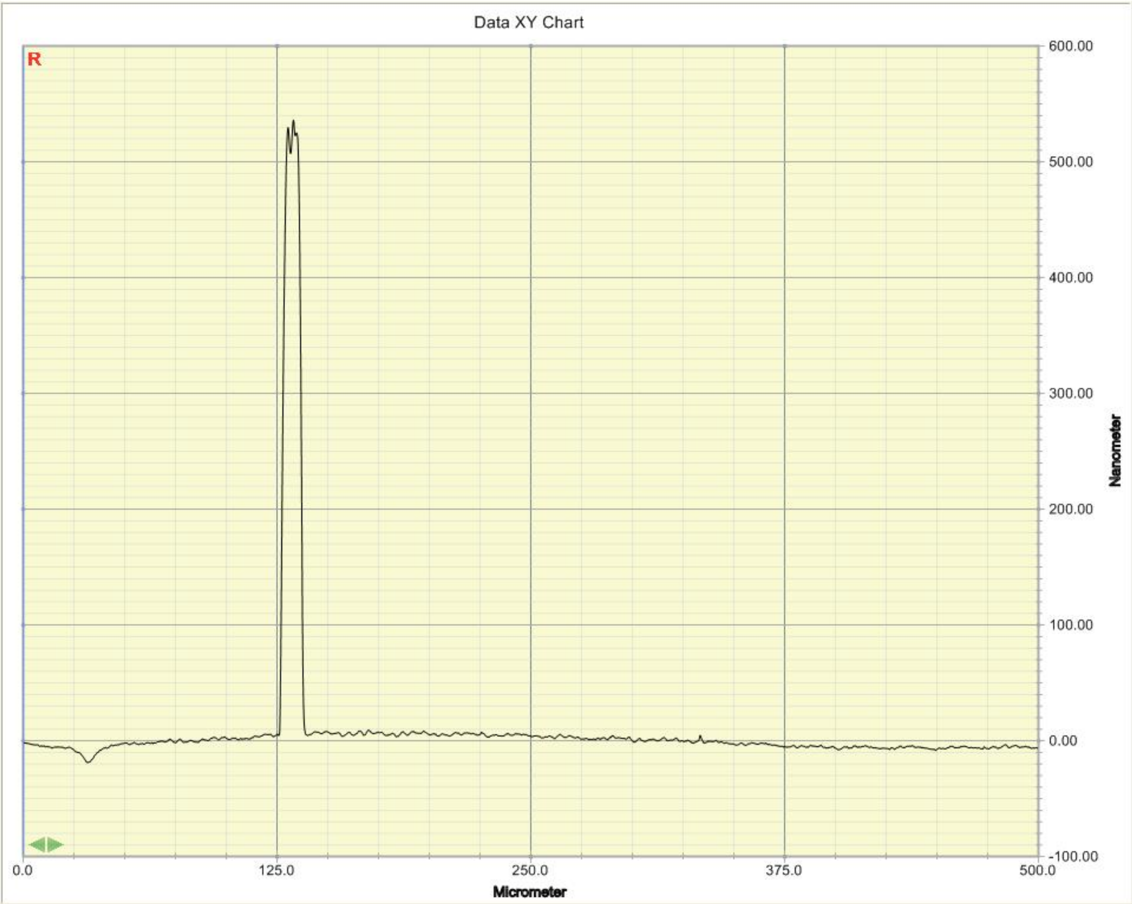


Figure 39: Profilomter before CMP over the tunnels structure. Batch 2

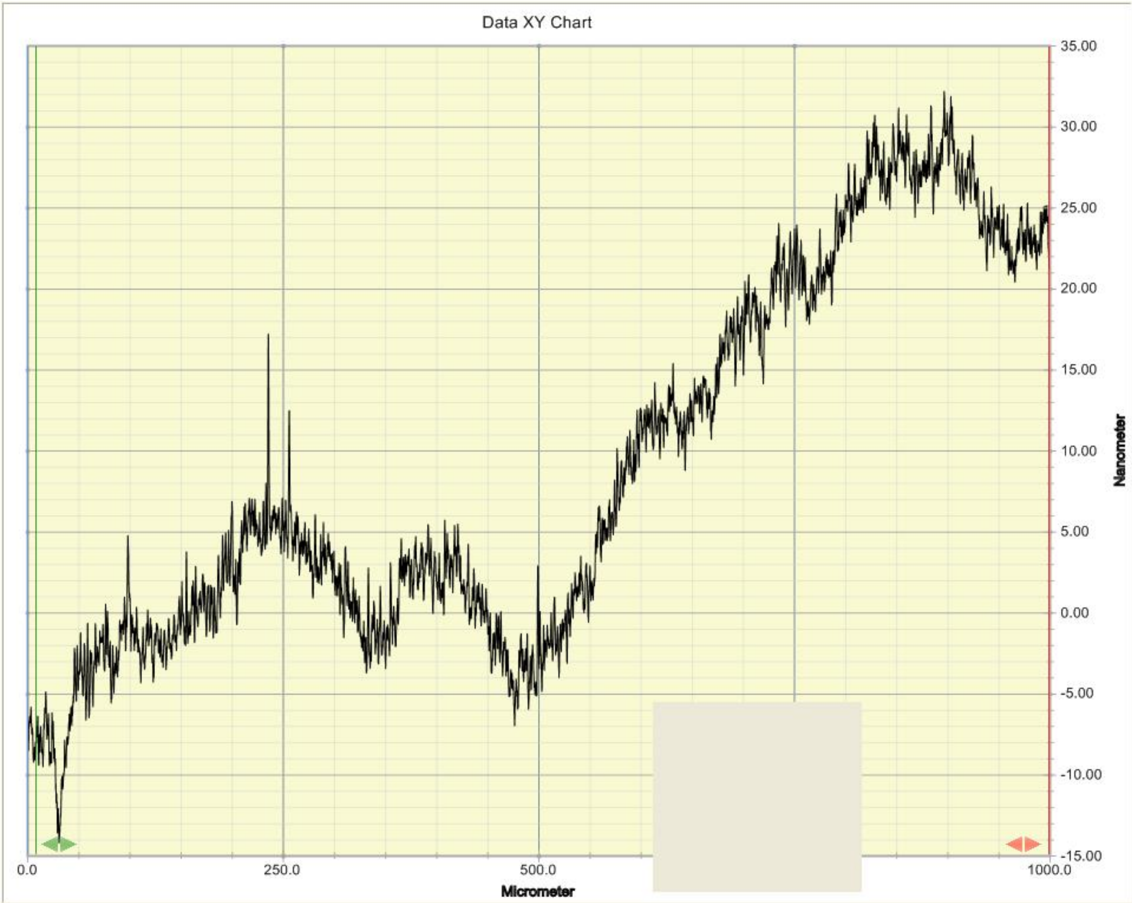


Figure 40: Profilometer after CMP over the tunnel structure. Batch 2

From figure 44 we can see that CMPing have reduced the hills over tunnel structures, but have also increased the roughness. Before CMPing the roughness were R_a is 1.12nm, but after R_a is 13.32nm.

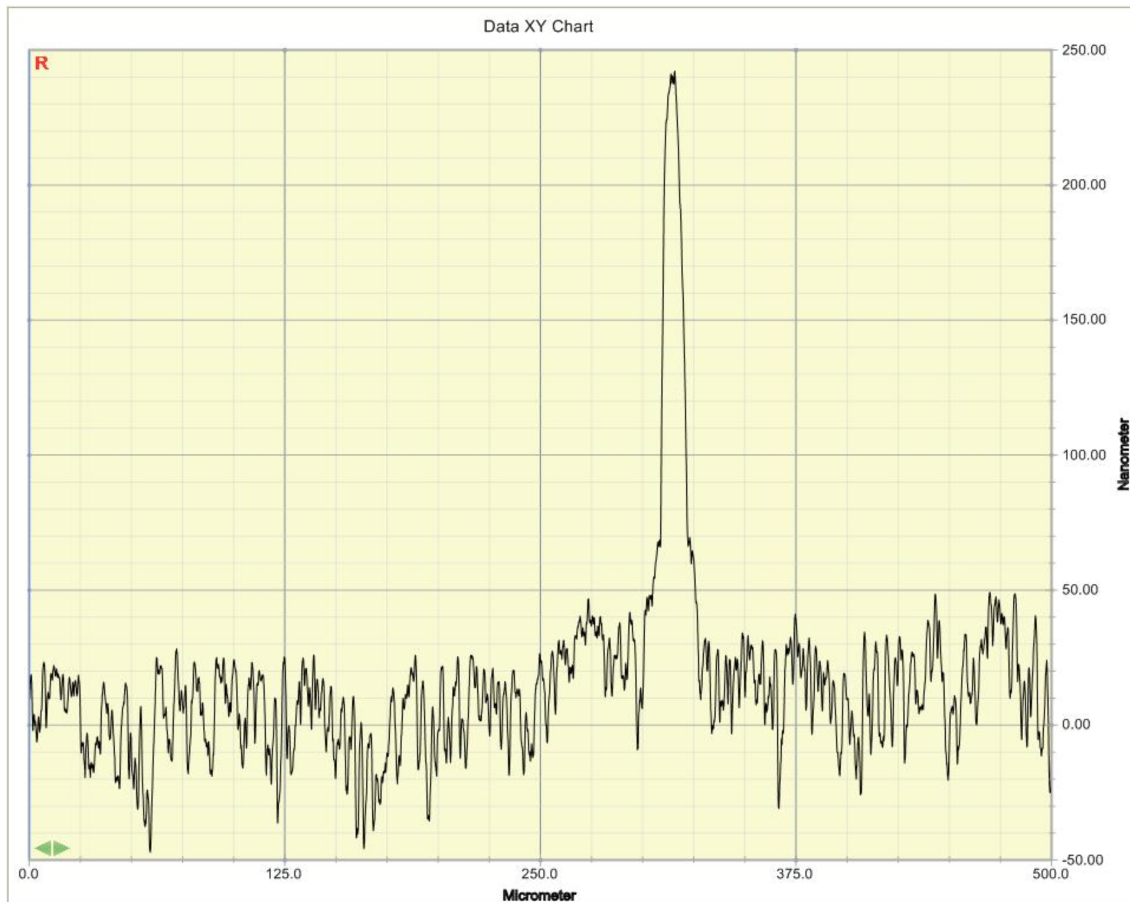


Figure 41: Profilometer over tunnels after CMP. Batch 1, with 1/5 slurry mixture

Comparing profilometer data from batch 1 and 2 we can see that design changes have reduced the hills over the tunnels.

6.13 Scanning Electron Microscope of cross section

One of the samples in batch 1 has been cut to check the cross section of the sample in a SEM. As can be seen in the 42 the amorphous filled tunnel pattern have been made according to specs. There are unwanted voids on both side of the tunnels. The voids do not likely to affect the quality of the reactor, and the deviation from expected pattern is adaptable. From 43, we can see the dimensions of the geometry of the tunnels. The height of the tunnels is 570nm and deviates from the 600nm height of the target. This deviations is caused by the accuracy of the reflectometer and the elliposmeter as thickness and number of layers increase. This deviation is totally acceptable within specified requirements of the reactor, which are sustaining ALD reaction and working in a TEM.

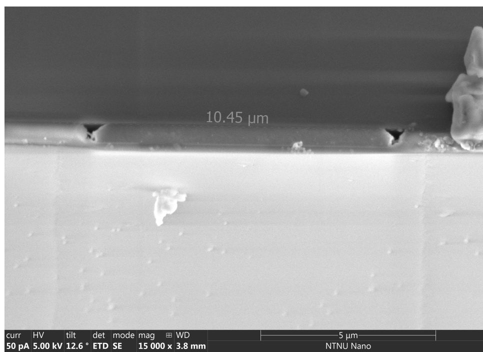


Figure 42: Cross section of the tunnels

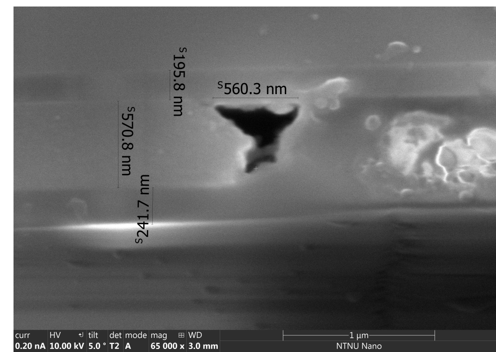


Figure 43: Cross section of the tunnels

6.14 3D Optical Profiler

Figure 44: 3D Optical Profiler photso of Si tunnels in batch 1. charactrization is done by Stephanie Burgman

The 3D optical profile have been used to confirm the etched holes goes all the way into the tunnel structure, and subsequent xenon difluoride etching can be done.

7 Discussion

The fabrication steps of a microreactor for in situ thin film characterization in a transmission electron microscope were developed and studied in detail. The production steps were conducted and studied in regards to (1) repeatability, (2) cost, (3) time (4) quality.

Several challenges during manufacturing made modifications of the process sequence or changing the chip design necessary. The first challenge was getting a functioning a-Si layer. α-Silicon deposition were attempted first with PECVD. Since PECVD produced poor results on the 4-inch wafers but had no noticeable surface defects when deposited on 2-inch wafers, modifications that would give consistently good results on 4-inch wafers were explored. Trying various recipes at different temperatures and different gas composition were tried, it did not produce the desired results. The electron beam evaporator (evap) did give consistent results, but there were some imperfections on the sample after deposition, so some chips on each wafer could be defective because of this. Overall the evap worked, and most chips on the sample were without any noticeable defects, but each sample had around 2-4 chips damaged. There were also some initial problems with using the evap in automatic mode, where the silicon target would heat too rapidly, and silicon spread around the evap chamber as a liquid. Some of the samples in batch 1 were made using evaps manual mode, but after lab staff changed the automatic modes silicon recipe, the automatic mode was used for the rest. There has not been any difference in the a-silicon layer from using automatic or manual mode after modification to the automatic mode recipe. The changes to automatic mode were increasing the pre-deposition soaking time and lowering the power for soaking.

After the second ALD layer on the a-Si layer, there were some challenges with applying the mask on the aluminum oxide and finding the cause. Since the resist had good adhesion during the spin coating, it was unlikely that the problems were caused by adhesion problems or improper cleaning. The likely cause was etching from the MF-26a developer that contains Tetramethylammonium hydroxide (TMAH) that etches amorphous silicon. The developer datasheet claims Tetramethylammonium hydroxide (TMAH) should be around 2.3 % and TMAH etches silicon even at low concentrations, however when used for etching, the temperature tends to be higher since increasing temperature increases the etch rate [44]. A number for the etch rates for TMAH for 20 °C was not found, but it is likely to be low since the temperature at the lab is 20 °C, but still a likely cause for the adhesion problems. The problem was solved by making a hydroxide layer on top of the sample before applying the photoresist. No adhesion problems occurred after this was done. The hydroxide layer was made by putting the samples into the ALD and run 10 H_2O cycles at 160°C with 1 cycle of Al_2O_3. There are other options to make the hydroxide layer, but the ALD was used since it was available at the time, but other options would likely have given the same results. The reason for running 1 cycle with TMA and H_20 to save time, since otherwise, a new recipe would need to be made. 1 ALD cycle is small and has not had any noticeable negative effect on any batches. Although unnecessary to run one ALD cycle, it was used to save time and should remove this cycle step if a higher volume is produced.

Aluminum oxide deposited in the ALD will deposit material on both sides, which for some fabrication steps is unwanted. In addition, backside deposition occurs unevenly with the least thickness in the center and increasing further away from the center, where on the edge deposition where it is equal on frontside and backside. Uneven backside can cause problems in later etching processes where the extra aluminum layer can act as a protective layer, and the wanted etch-depth is not achieved. In addition, the difference in thickness will cause etching to go through first close to the center compared to the outer perimeter, which could cause an increase in defective reactor. Since the sample backside resting on the ALD reactor hotplate allows for gas flow, but the gas flow is reduced the closer it gets to the center because of limited space that reduces flow. A solution consists of stopping gas flow in areas we do not want deposition by using a clamping system with a steel plate with screw threads that clamp a dummy wafer and the sample together when the screws are fastened. This has been shown to stop backside deposition, but because of the clamping system size, only one sample can be processed at a time. An improvement could be to make a smaller clamping system so two samples can be processed in parallel. During one stage in the fabrication process, the sample needs aluminum oxide on both sides to act as a protective layer. In this step, to ensure even deposition, small steel pieces can be used to elevate the sample. This makes it possible to deposit an even layer on both sides on two samples at the time.

The backside pattern for KOH etch is the first pattern made in batch 1, and while initially, the results were good, there was damage on the backside that appeared when working on the front side. Therefore, putting the KOH windows on later in the process reduces the number of damaged reactor chips.

The CMPing used for making the surface plane was the primary source for damaging chips. There was some delimitation on the samples, especially in batch 3 that had -silicon as a top layer. However, several chips per sample were damaged, but most were usable. The initial problem with batch 1 was that the design had two types of materials exposed to the polishing pad, -silicon and SiO_2 and that the -silicon etched faster than SiO_2. The slurry concentration was reduced from 1/3 to 1/5, and this produces more desirable results. There remained a difference between the material removal rates (MRR) at both concentrations, but an additional lowering of the slurry was not tried since the difference in MRR was low enough to stop when the layers were about the same thickness easily. Also, the CMP did not produce a plane surface as expected, and hills over the tunnels were still present after finishing CMP. There was not enough material left on top of the sample to continue CMPing without risking damaging the tunnels. These two problems were the reason for the design changes of the tunnel design in batch 2 and batch 3. Changes to top design also gave better results for ellipsometry, reducing the mean square error in the measurement from 120 to about 70. So design changes also gave a more plane surface than what we saw in batch 1 by removing hills over tunnels, but it increased the surface roughness.

CMPing introduced a considerable amount of contaminants on the wafers. Even after cleaning with acetone and plasma, the sample was not clean enough for ALD deposition. Therefore an added HF cleaning step was needed to clean the wafers to ensure high-quality

results.

Etching the holes and into the sacrificial a-si layer can be etched in the same chlorine-based ICP-RIE, and it would be faster to do it that way if the batch size is one sample. However, when more samples are processed simultaneously, it saves time to use fluoride and chlorine ICP-RIE for parallel processing. The time saved on each sample is about 5 min but varies a little because handling time varies. There is also an added time saving from not needing to find one new etch rates that can take around several hours with deposition, etching, and two measuring steps.

Future work would be to fill the holes after xenon difluoride vapor etch and scribe the samples into individual ALD microreactors

8 Conclusion and future work

The fabrication steps of a microreactor for in situ thin film characterization in a transmission electron microscope were developed and studied in detail. The production steps were conducted and studied in regards to (1) repeatability, (2) cost, (3) time (4) quality.

Improvements have been made to ALD Aluminum oxide deposition by using a clamping system to ensure deposition one side occurs at the time. When deposition on both sides is needed, a uniform deposition is achieved by elevating the sample using small steel pieces, and uniform deposition is achieved on both sides.

Design changes to the reactor have increased the number of reactors produced per sample, reduced costs, and made the sample more plane in the CMP step, improving later fabrication steps. An added HF cleaning step after CMP were added to the original manufacturing sequence to improve subsequent aluminum oxide deposition in the ALD. Also, an added fabrication step includes adding a hydroxide layer to prevent SPR700 on a-si from sliding off during development. The backside pattern has also been moved to a later part of the manufacturing to reduce damage to the backside pattern and increase the number of working reactors produced on each sample.

A total of 7 samples over three batches have been worked on to test the various fabrication steps, and all of these are near completion. If future batches are needed, the cycle time can easily be calculated. Future work would be to fill the holes after xenon difluoride vapor etch and scribe the samples into individual ALD microreactors, and the fabrication steps have been tested for repeatability.

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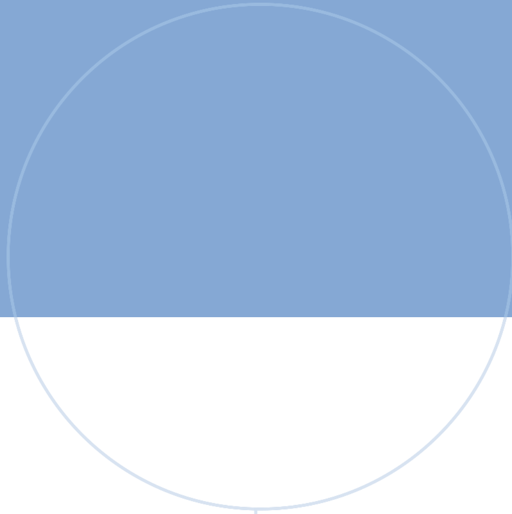
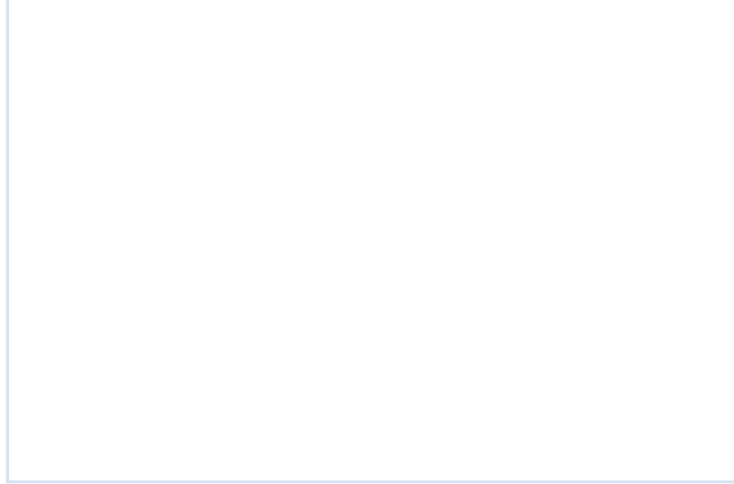

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