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Energy Harvesting for Ambient Backscatter Communications

Master's thesis in Electronic Systems Design Supervisor: Egil Eide Co-supervisor: Lloyd Clark June 2021

Master's thesis

NTNU Norwegian University of Science and Technology Faculty of Information Technology and Electrical Engineering Department of Electronic Systems



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Abstract

In this thesis the design of a 50 Ω patch antenna and radio frequency energy harvesting system usable for a plausible ambient backscatter communications device is detailed. The system is assembled on a FR-4 substrate and built using only off-the-shelf components, and harvests power by converting 1800 MHz electromagnetic radiation to DC through the use of a 1-stage Villard voltage doubler circuit, which acts as a rectifier.

The rectifier uses Skyworks SMS7630, zero-bias Schottky diodes to rectify any incoming low power AC signals into electrical charge which can then be used to power a low-power microcontroller like Microchip's ATMega4809. In theory each stage should double the input voltage. By cancelling the capacitance of the rectifier diodes through the use of inductors the voltage multiplier is further increased without the need for more stages.

Through spectrum measurements at a fixed location it was found that the antenna could at best provide an output AC power of -13 dBm (50 μ W) for a band ranging from 1790- to 1910 MHz. Supplying a 1850 MHz sine wave with the same power on the input of our energy harvester gave us a measured DC output voltage of 107 mV, which is not enough to power the ATMega4809. The minimum amount of input power required for the system to provide 2 V is 6 dBm (4 mW).

It was concluded that developing a feasible radio frequency energy harvesting system with off-the-shelf components was a difficult process due to the need for accurate simulation models and post-manufacture tuning, and lack of control over parasitics and component tolerances. As a final verdict, it was reasoned that a lowpower charge pump would have been a useful addition for the system so as to provide 2 V with less input power.

Abstrakt

I denne avhandlingen blir designet av en 50 Ω patch antenne og et radiofrekvens energihøstings system egnet for en sannsynelig ambient backscatter kommunikasjons enhet forklart. Systemet er montert på et FR-4 substrat og består av butikk-kjøpte komponenter, og høster energi ved å konvertere 1800 MHz elektromagnetisk stråling til DC ved bruk av en 1-trinns Villard spennings dobler krets, hvilket handler som en likeretter.

Likeretteren bruker Skyworks SMS7630, null-bias Schottky dioder til å likerette innkommende lav effekt AC signaler til elektrisk ladning som kan brukes til å drive en lav-effekt mikrokontroller slik som Microchip's ATMega4809. I teorien skal hvert trinn doble inngangs spenningen. Ved å kansellere kapasitansen til likeretter diodene ved bruk av spoler kan spennings multiplikatoren økes videre uten behov for flere trinn.

Gjennom spektrummålinger ved et fast sted ble det funnet at antenna klarte på sitt beste å gi en utgangs AC effekt på -13 dBm (50 μ W) for ett bånd som spenner fra 1790- til 1910 MHz. Levering av en 1850 MHz sinus bølge med samme effekt på inngangen av energi høsteren gav oss en målt DC utgangsspenning på 107 mV, hvilket ikke er nok til å drive ATMega4809. Den minste mengden effekt som kreves for at systemet skal kunne gi 2 V er 6 dBm (4 mW).

Det ble konkludert med at å utvikle av et fungerende radiofrekvens energihøstings system med butikk-kjøpte komponenter var en vanskelig prosess på grunn av behovet for nøyaktige simulerings modeller og etter produksjons tuning, samt mangel på kontroll over parasitter og komponent toleranser. Som avsluttende dom ble det resonnert til at en lav-effekt ladepumpe ville vært ett nyttig tillegg til systemet for å gi 2 V med mindre inngangs effekt.

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List of Abbreviations

ABCS	Ambient Backscatter Communication System
AC	Alternating Current
ADS	Advanced Design System
ASIC	Application-Specific Integrated Circuit
BW	B andwidth
CCL	Copper Clad Laminate
CMOS	Complementary Metal-Oxide-Semiconductor
DC	Direct Current
EDA	Electronic Design Automation
EM	ElectroMagnetic
EMR	ElectroMagnetic Radiation
ESL	Equivalent Series Inductance (L)
ESR	Equivalent Series Resistance
HSLS	High-Side Load Switch
IC	Integrated Circuit
IMN	Input Matching Network
ΙοΤ	Internet of Things
LSSP	Large Signal S-Parameter
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
MPT	Maximum Power Transfer
MPTT	Maximum Power Transfer Theorem
NKOM	Norwegian Communications Authority (KOM)
NMOS	N-channel Metal-Oxide-Semiconductor
PCE	Power Conversion Efficiency
PMOS	P-channel Metal-Oxide-Semiconductor
RF-EH	Radio Frequency Energy Harvester
RMS	Root Mean Square
SMD	Surface-Mount Device
VCVS	Voltage Controlled Voltage Source
VNA	Vector Network Analyzer
WPT	Wireless Power Transfer

Physical Constants

Speed of Light	$c = 2.99792458 \times 10^8\mathrm{ms^{-1}}$ (exa
	$k = 1.38 \times 10^{-23} \mathrm{J}\mathrm{K}^{-1}$
Elementary Charge	$q = 1.60 \times 10^{-19} \mathrm{C}$

List of Symbols

ϵ_{a}	Antenna Efficiency	%
ϵ_r	Dielectric Constant	%
ϵ_{reff}	Effective Dielectric Constant	%
η	Power Conversion Efficiency	%
θ	Zenith Angle	0
λ	Wavelength	m
Т	Period	S
ϕ	Phase	0
ϕ_a	Azimuth Angle	0
Ω	Ohm	Ω
Α	Ampere	А
D	Directive Gain	
D_a	Antenna Directivity	
D_{dim}	•	m
f	Frequency	$Hz (s^{-1})$
f_{Δ}	Bandwidth	Hz
f_r	Resonant Frequency	Hz
G_a	Antenna Gain	
G_{max}	Maximum Antenna Gain	
G_{min}	Minimum Antenna Gain	
G_R	Receiver Gain	
G_T	Transmitter Gain	
h	Substrate Thickness	m
i	Current	А
I_{Di}	Diffusion Current	А
I_{Dr}	Drift Current	А
I_S	Saturation Current	А
K	Kelvin	Κ
L_p	Patch Length	m
L_{pf}	Patch Feed Length	m
L_{pi}	Patch Inset Feed Length	m
m	Meter	m
0	Origin	
Р	Power	W
P_{in}	Input Power	W
P_L	Load Power	W
Pout	Output Power	W
P_R	Received Power	W
P_T	Transmitted Power	W
Q	Q-Factor	
R	Resistance	Ω
R_a	Transmitter-Receiver Distance	m

R_{ff}	Far-Field Distance	m
R_{in}	Input Resistance	Ω
R_L	Load Resistance	Ω
R_o	Output Resistance	Ω
R_{nf}	Near-Field Distance	m
R_S	Source Resistance	Ω
s	Second	S
t	Time	s
Г Т	Temperature	K
U U	Radiant Intensity	$W sr^{-1}$
v	Voltage	V
V	Volt	V
V_{in}	Input Voltage	V
V_L	Load Voltage	V
V_0	Barrier Voltage	V
Vout	Output Voltage	V
V_D	Diode Threshold Voltage	V
V_p^-	Peak Voltage	V
V_{pp}	Peak-to-Peak Voltage	V
V_T	Thermal Voltage	V
V_{ZK}	Breakdown Voltage	V
W	Watt	W
W_p	Patch Width	m
W_{pf}	Patch Feed Width	m
W_{pi}	Patch Inset Feed Width	m
X	Reactance	Ω
X_L	Load Reactance	Ω
X_S	Source Reactance	Ω
Ζ	Impedance	Ω
Z_{in}	Input Impedance	Ω
Z_L	Load Impedance	Ω
Zo	Output Impedance	Ω
Z_S	Source Impedance	Ω

Chapter 1

Introduction

1.1 Background

Ever since the introduction and widespread adoption of electrical power grids during the second industrial revolution back in the 19th century, scientists and inventors have pondered and experimented with the idea of transmitting power wirelessly, often referred to as wireless power transfer (WPT), thus circumventing the physical constraints introduced by electrical wires. Heinrich Hertz demonstrated back in the 1880s that one could transmit and receive electromagnetic radiation (EMR) through the use of a specialized construction called an antenna, thus proving Maxwell's theory of electromagnetics (EM) in the process [1]. The inventor Nikola Tesla did extensive experimentation to both demonstrate and improve on wireless power transfer methods. One particular circuit he would use was a tuned LC circuit, which let him implement high frequency resonances, and this circuit is today commonly found in modern short-range wireless power systems [2].

1.2 Motivation

In more recent times there has been a great surge of interest in expanding the capabilities of wireless power systems, in part due to the widespread use of smartphones and other smart devices. Such smart devices are often considered to be part of a cluster commonly referred to as an Internet of Things (IoT), which is a term used for a network of devices that can communicate with each other or some server [3]. One important property of a well-functioning IoT is that its performance stays constant when the total amount of devices increases, a property referred to as scalability. A scalable IoT is desirable as it gives the users or maintainers the ability to introduce new devices to their network without worrying about the whole system underperforming or become unreliable. This is particularly true if the network consists of hundreds, if not thousands of devices that collects, calculates and communicates data with one another or some receiver. Due to the desire for scalability, it is also beneficial that the devices are physically small in size and allow for mobility.

Scalability in IoT is difficult to accomplish however, as each device is usually required to communicate wirelessly in some form, which requires significant amounts of power when using conventional wireless transmission methods, e.g transmitting with an antenna. Having to electrically wire and setup an IoT with a few smart devices in some building might not be too much work at first, but when you later down the road want to add a few more smart devices to the network, one quickly runs into the problem of physical constraints provoked by the already wired environment. There is also the consequence how having the network itself be lacking in mobile capabilities, thus discouraging changes to the network layout in the future, which in turn can reduce potential for improving the IoT's performance. The next logical step to these problems is to use batteries instead, which allows for a mobile network of communicating devices. The issue then is that the batteries must eventually be switched out or be recharged in a somewhat periodic manner, which requires a great deal of surveillance and manual labour when working with a large-scale network.

Renewable energy harvesting technologies are enticing when considering power sources for IoT devices, as the devices can be self-sufficient and operate without human interference, thus reducing the need for maintainability. Technologies like piezoelectric (kinetic), thermoelectric (heat), and photovoltaic (solar) energy harvesting have become quite common in low-power devices, and are capable of operating autonomously [4]. These energy harvesting technologies do however need to adhere to certain restrictive conditions to work, e.g piezoelectric energy harvesters need to be acted upon by a kinetic force, thermoelectric harvesters needs a source of heat, and the photovoltaic ones have to be exposed to photons. Due to these limitations, long-range WPT have become more popular in the field of energy harvesting topics, as EMR has some useful properties like being able to penetrate materials like water and plastic [5]. WPT is also becoming particularly relevant today as man-made EMR is becoming more and more prominent due to rapid globalization of the world, primarily lead by the use and development of smartphones and telecommunications.

As with most technologies, WPT comes with its own share of difficulties. EMR is quite complex to predict as it is scattered and absorbed by objects and electromagnetic fields. When EMR is scattered by an object like an antenna or an object, it will spread out, meaning the distance travelled by the EMR will have a significant impact on the energy it will carry. These realities shapes EMR to act as a sporadic energy source, as the environment decides where the EMR energy will reside or go. Harvesting enough energy from EMR to power a battery-less IoT device that can transmit wirelessly is therefore no easy feat, which has been the motivation for the development of a technique called ambient backscatter.

1.3 Ambient Backscatter

Ambient backscatter is a special variant of the backscatter communication technique, and grants a battery-less device the ability to transmit data by scattering ambient RF sources off of an antenna. An ambient RF source is considered to be an already deployed RF source, like a TV tower, a cellular base station, or a wireless access point.

A device utilizing the ambient backscatter technique, can be referred to as a ambient backscatter communication system (ABCS). A bare-bones ABCS, such as the one seen in Figure 1.1, is generally made up of an antenna, a RF-DC converter, a transmitter or a receiver (or both), and a microcontroller. The RF-DC converter acts as a RF energy harvester when connected to the antenna. The antenna is also connected to the transmitter or the receiver. The transmitter is not actually transmitting anything, but modulating the antenna through a switch that connects the antenna to ground. By turning the switch on or off with the microcontroller, the antenna load impedance can be modulated, thus changing the scattering electric field of the antenna. This can be used to communicate data wirelessly without the need of much power. Nearby ABCS devices will then be able detect dips in the average EMR through the use of a specialized receiver, which then converts the detected dips into digital signals for the microcontroller to process.

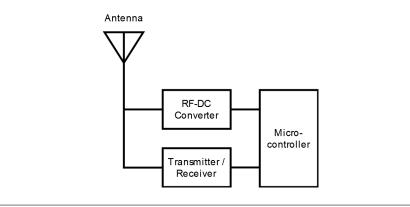


FIGURE 1.1: A bare-bones ambient backscatter communication system that is assembled as either a transmitting or a receiving device.

Ambient backscatter has advantages that other backscatter techniques do not have, the most apparent one being that it does not need deployment of dedicated RF sources, thus reducing the overall cost [6]. Additionally, a lot of energy that goes into the transmission of radio waves are wasted as most it is not picked up by antennas, but instead simply reflected off into space or absorbed into random materials. Ambient backscatter makes use of this 'free' energy to not only harvest, but also transmit and receive data.

The biggest drawback of ambient backscatter is the unpredictable nature of ambient RF sources due to changes in the environment, thus challenging the sustainability of any device making use of it. It is therefore crucial that the RF energy harvesting circuitry is highly efficient and can reliably work with wide ranges of input power.

1.4 **RF Energy Harvester**

A device that converts EMR to electrical power is called a RF energy harvester (RF-EH). The simplest form of RF-EH is made out of a rectenna. A rectenna converts EMR to direct current (DC), and is made out of two components, an antenna and a rectifier. The antenna is constructed so that it resonates at one or more frequencies, and will convert nearby EMR at these frequencies into alternating current (AC). The rectifier is a circuit that converts the AC to DC. The DC can be used to charge a energy storage, usually a capacitor, which can then act as a power source for some load.

The rectifier is usually made up of some component that can block the negative or positive polarity of an AC signal, e.g a diode. Regular diodes such as silicone diodes require a forward bias of around 0.7 V to allow for current to pass, and for battery-less RF-EH that is often a difficult ask as the AC tends to be below that threshold. Schottky diodes are therefore more commonly used, as their forward biases are much lower. Rectifier topologies called voltage doublers are popular choices in RF-EH, as they can be cascaded to allow for higher output voltages, at the cost of loss in efficiency and an increase in parasitics.

A general system block diagram of a RF-EH is shown in Figure 1.2. Here an impedance matching network (IMN) is connected between the antenna and the rectifier so as to maximize the power going into the rectifier. The power management block is responsible for providing power to some load with the DC given by the rectifier. In context of an ABCS, the load would be the microcontroller, and possibly

sensors or some other additional circuitry that requires power. In this thesis we are referring to the RF-DC converter when talking about the RF-EH.

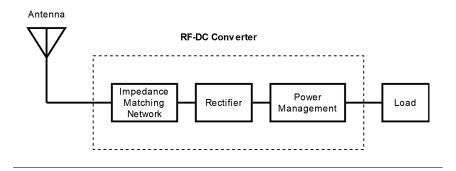


FIGURE 1.2: A general RF-EH system, consisting of an antenna, an impedance matching network, a rectifier, and a power management circuit.

1.5 Thesis Contribution

This thesis is an attempt at taking the reader step by step through the process of developing a RF-DC converter using off-the-shelf integrated circuits (IC) and discrete components, with the goal of it being compatible with a battery-less device that can make use of ambient backscatter to communicate wirelessly.

Our proposed RF-DC converter operates on input AC of 1850 MHz, and is designed for a device that utilizes the ATMega4809 by Microchip as the brain, which is an 8-bit microcontroller that is capable of running on a low power supply with a voltage of at least 1.8 V.

1.6 Thesis Outline

Chapter 1 is the introduction of the thesis and presents historical background and motivation behind the development of RF energy harvesting. In addition, the more recent backscatter technique called ambient backscatter is described in light of RF energy harvesting. An overview of a general RF energy harvesting device is also given.

Chapter 2 is a review on literature pertaining to RF energy harvesting systems, especially battery-less systems, so as to establish an overview over major trends, challenges, and state-of-the-art. In particular, this thesis presents a performance comparison between papers where the authors have designed RF energy harvesting systems and attained voltage levels high enough to power low-power microcontrollers, given input RF signals of ultra-low power.

Chapter 3 is a collection of theoretical knowledge, mathematics, and concepts highly relevant to RF energy harvesting, with its purpose being to aid the reader in getting the most out of this thesis. The chapter covers topics of EMR, semiconductors, transmission lines, and the RF-DC converter.

Chapter 4 details the entire design process that was followed from start to finish. The chapter begins by elaborating on the simulation aspect of the design, e.g microstrip, substrate and components. Further, it moves on to establish and justify the requirements and design for both the antenna and the RF-EH. **Chapter 5** sheds light on matters relating to how the results were measured and interpreted, including the equipment usage.

Chapter 6 shares measurements so as to gauge the performance of our design, which is then discussed in contrast to simulations and requirements.

Chapter 7 wraps up the thesis with conclusions and some pointers on future work that can be done to improve upon the design.

Chapter 2

Literature Review

2.1 Major Trends and Challenges

In most of the recent literature, RF energy harvesting designs have primarily focused on outputting usable voltages while maintaining a consistently high power conversion efficiency (PCE) across a wide range of ultra-low to low input powers for certain radio waves, the most commonly examined being ultra high frequencies (UHF). Frequencies ranging from 300 MHz to 3 GHz are defined as UHF [7]. UHF is a popular choice due to it being used as a medium for an extensive list of applications worldwide, such as Wi-Fi, cell phones (e.g GSM, LTE), TV broadcasting, Bluetooth, GPS, and more [5]. The most attractive frequencies have been 900 MHz (GSM900), 1800 MHz (DCS-1800), and 2.4 GHz (Wi-Fi, Bluetooth), as they are most common place. Since the aforementioned technologies are used almost everywhere in modern society at all times, it can therefore be expected that they are present in all urban and most rural areas in developed countries, and therefore be considered a constant source of ambient RF energy.

Although RF can be transmitted at substantial power levels legally in most nations, the power density of waves reduce considerably with distance due to Friis equation (Section 3.1.2). This coupled with the fact that waves interfere with each other, often leads to meager amounts of RF power being harvestable. For that reason, a high PCE is desirable so as to get the most out of what little power can be harvested, meaning both the antenna and RF-DC converter must have high PCE. For the antenna to efficiently convert EMR to AC, it must be matched to particular frequencies of interest. A chunk of research has gone into developing broadband RF energy harvesters with high efficiencies, as it can increase the total amount of power that can be extracted from nearby EMR [8][9]. Since most of the literature is concerned with battery-less restrictions, the matching is most commonly accomplished through the use of network topologies consisting of passive components like capacitors, inductors, and microstrip lines.

The inherent non-linearity of semiconductor components used to achieve RF-DC conversion (e.g diodes, CMOS) makes it difficult to efficiently handle wide ranges of input powers, which is particularly troublesome as ambient RF is inherently spurious. A built-in limitation of these components is the minimum threshold voltage required for the semiconductors to operate. This restraint can be lessened by having high Q resonators right before the rectifier, thus increasing the peak-to-peak voltage of the incoming AC signal [10]. Achieving high Q resonance is a difficult process however, as the antenna, IMN and rectifier have to be co-designed to operate optimally due to low-input power and parasitics [11].

There have also been done studies demonstrating that wide ranges of input powers can be handled more efficiently by negating the reactance of rectifier semiconductors through the use of passive components [12][13]. While efficiency is quite important in a RF-EH due to the low power levels, it is for some applications more important to reach and maintain a certain voltage output. Prioritizing the output voltage is relevant if the RF-EH is to power a micro-controller, sensor, LED, or some other device requiring a minimum DC voltage to operate. One way to increase the output voltage is to have the output of the rectifier be high in impedance, but that can lead to loss in total PCE. It is not uncommon to utilize some form of DC-DC boosting after the rectifier to reach higher output voltages [14][15]. The authors of [16] have demonstrated that a low-voltage charge-pump can efficiently boost a rectifier output voltage of around 0.3V to a level that is high enough to operate low-power microcontrollers, where their rectifier was made with off-the-shelf Schottky diodes.

Combining RF-EH with solar, thermal and kinetic energy in the form of hybrid energy harvesting has become a staple both commercially and in research, with the added benefit of being highly adaptable in various environments [17].

2.2 State of the Art

Most state of the art RF-EH research uses some form of custom-made, applicationspecific integrated circuits (ASIC) made with complementary metal-oxide-semiconductor (CMOS) technology (see Section 3.2.3 for theory on CMOS). There are two primary reasons for using CMOS over Schottky diodes. Firstly, it provides the designer with more freedom and flexibility, as there are more parameters to work with, and secondly, CMOS is more sensitive to low operational voltages [18]. More parameters will lead to a more complex design process however, which is more avoidable when using off-the-shelf Schottky diodes.

ASIC allows for the development of complex techniques to improve capabilities of a RF-EH. One such technique is to have the RF-DC converter reconfigure itself based on the input power, categorized as low-power mode and high-power mode [15]. The motivation behind the technique is the non-linearity of rectifiers, whose performance vary considerably based on the input power. By switching between these modes, one can extend the input power range and maintain a high efficiency. This is demonstrated by the authors of [19], where for a PCE above 20 % they extended the total input power range from 10- to 13 dB. Their design requires a external battery however, so as to provide a stable reference voltage for a comparator that determines whether the RF-EH should be in low- or high-power mode.

Lately, more researchers have tried to lower the threshold voltage of rectifiers by making use of adaptive threshold-compensation techniques [20][21]. A lower threshold voltage will give a better input power sensitivity and thus a wider input power range, while also allowing for more rectifier stages if needed. For CMOS, such techniques are accomplished in passively or actively. Active solutions tend to require external power, such as for biasing gate voltages, whereas passive ones require more complicated circuitry, e.g a secondary rectifier providing gate bias.

A performance summary encompassing a wide range of different RF-EH designs in literature can be seen in Table 2.1, sorted by minimum input power required to output a DC of 2 V.

Ref. (year)	Design	Technology	Frequency (MHz)	P _{in} for 2V (dBm)	Efficiency @ P _{in} (%)	Load (Ω)
[8] (2018)	Single-diode	HSMS-2860	700	12	72	0.3k
[12] (2020)	Shunted single-diode	Avago HSMS-286	2100	11	72	1.7k
[22] (2015)	Single-diode	HSMS-2862 (SOT-23)	2450	9	60	0.9k
[23] (2020)	Voltage doubler	HSMS-2850 (SOT-323)	900	8	40	2k
[<mark>9</mark>] (2020)	Voltage doubler	Skyworks SMS7630	1500, 1800, 2100	7	53-57	1.6k
[13] (2020)	Voltage doubler	Skyworks SMS7630	800	6	72	1.4k
[15] (2017)	ASIC	65 nm CMOS	900	-9.5	32.5	147k
[24] (2015)	ASIC	180 nm CMOS	900	-12	44.1	144k
[16] (2011)	Single-diode or voltage doubler, ultra-low- voltage charge-pump IC	Agilent HSMS-2850, Skyworks SMS-7630	2450	-15.2, -15.6	2.71	20k
[20] (2020)	ASIC	130 nm CMOS	915	-17	22	1M
[19] (2020)	ASIC	180 nm CMOS	902	-18	23.5	1M
[21] (2019)	ASIC	130 nm CMOS	896	-18.5	30	1M

TABLE 2.1: Comparisons between measured performance of RF-DC conversion systems assembled using either discrete or ASIC, sorted by minimum input power needed for 2 V.

Chapter 3

Theory

3.1 Electromagnetic Radiation

The theory of electromagnetics is covered by Maxwell's equations, and explains how electromagnetic waves function. Since the theory behind the equations is quite extensive mathematically [25], this section will prioritize on giving a more easy to digest and broad coverage of the most important concepts concerning electromagnetic radiation in terms of **radio waves**, so as to help orientate the reader.

Like all waves in physics, radio waves have a wavelength λ given by Equation 3.1, where *f* is the frequency of the wave and *c* is the speed of light, a constant.

$$\lambda = \frac{c}{f} \qquad [m] \quad (3.1)$$

In a two-dimensional space a wave can at its simplest be expressed by Equation 3.2, which is the expression for a sine wave, where *A* is the amplitude, *t* is time, ϕ is the phase, and T is the period of the wave. The sine wave and its relationship with the named variables is illustrated in Figure 3.1. Sine waves are used to represent AC as well.

The period *T* is inversely proportional to the frequency *f* of the wave, and thus proportional to the wavelength λ . Therefore, if the period *T* is lowered, the frequency *f* will increase, and thus a shorter wavelength λ is achieved. This property is important as it has a big impact on antenna and RF circuitry design. For instance, higher frequency RF waves can be converted by smaller antennas, whereas lower frequencies require bigger ones. Additionally, higher frequencies have higher data rates capabilities than low frequencies. On the flip-side, high frequency RF waves have a shorter range due to being more prone to interference from being more easily absorbed or scattered by the environment. For circuitry, higher frequency AC is usually more difficult to work with than low frequency AC, as it is more vulnerable to noise sources such as EMR, thermal noise or parasitics.

$$y(t) = A\sin(\frac{2\pi}{T}t + \phi)$$

= $A\sin(2\pi ft + \phi)$ (3.2)

For a propagating EM wave there are two main components, the **electric field** E and the **magnetic field** B. Both fields can be expressed as a sine wave in a three dimensional space, with them being perpendicular to each other as shown in Figure 3.2. The time t will move the waves across the axis they are propagating (x-axis in illustration). The propagation direction will be perpendicular to both fields. If E is vertically aligned, then B is horizontally aligned, and vice versa. The alignment of

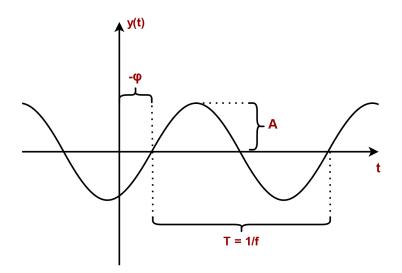


FIGURE 3.1: Illustration of a sine wave. Note that in this case the phase is negative since the wave is delayed.

the electric field and the phase difference between it and the magnetic field determines the **polarity** of the wave, which refers to the orientation of the electric field. If there is no phase difference and *E* is vertically aligned, the polarity will be considered vertical (like in the illustration). Otherwise, if *E* is horizontally aligned, the polarity is horizontal. Should there be a phase difference between *E* and *B*, then the wave has a **elliptical polarity**, meaning it has a combination of vertical and horizontal polarity. A **circular polarity** is a special case of elliptical polarity where the phase difference between the electric- and magnetic field is 90°.

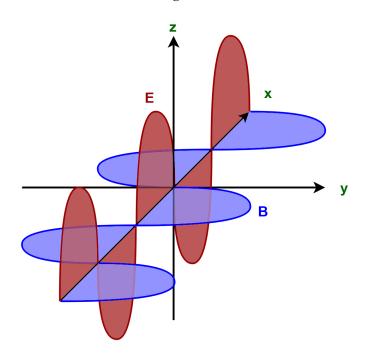
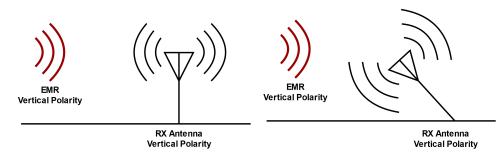


FIGURE 3.2: Illustration of a propagating EM wave in a three dimensional space, made up of a electric field E (red) and a magnetic field B (blue).

The polarity and orientation of a propagating EM wave affects how much power an antenna can extract from it. Each antenna has its own electric- and magnetic field across all frequencies, and thus also has a polarity and orientation property to it. If the polarity and orientation does not perfectly match between EM wave and antenna, called a **polarity mismatch**, then there will be a loss in power conversion from EMR to AC. As an example, if an EM wave with vertical polarity propagates directly towards a receiving antenna with vertical polarity that is oriented correctly as shown in Figure 3.3a, then there will be no polarity mismatch. Should however the antenna be rotated such that its orientation is not matched as in Figure 3.3b, there will be a loss. If the orientation is completely wrong, or the orientation is correct but polarity is the opposite, the antenna will not pick up the EM wave in question at all. This is a consequence of the inherent relationship happening between the polarity of the antenna, which is defined by its form, shape, or geometry, and the rotational degrees of freedom for the antenna, meaning its pitch, yaw and roll parameters. Depending on the antenna design, certain rotational parameters have negligible effect on power losses due to symmetrical properties in its power conversion behavior (more on this later).



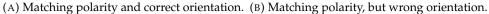


FIGURE 3.3: Illustrations demonstrating how polarity and orientation can lead to power conversion losses.

When a EM wave is scattered by something, like a building or some surface, its polarization will flip. This is troublesome as EMR is in practice constantly scattered by the environment, meaning a lot of realizable power is not converted. This is where circular polarity shines, as it is both vertically- and horizontally polarized at the same time, so when it flips, its essentially the same except that the electric- and magnetic field switched places. The phase difference will remain the same however, and thus it will stay circular in polarity. Circularly polarized EMR can also be converted by both vertically- and horizontally antennas no matter the orientation. Since a circularly polarized EMR has its power split between both vertical- and horizontal polarity however, only half the power can be converted at most by a vertically- or horizontally polarized antenna, which is equivalent to a loss of -3 dB.

3.1.1 Antenna

An antenna is a component usually made out of a metal, and can convert AC to radio waves (**transmitter**), or radio waves to AC (**receiver**). The transmitting and receiving properties of an antenna are identical due to the Reciprocity theorem [26], meaning it can do both if it is part of a system that can switch between a transmitting and receiving state.

The geometry and form of an antenna can vary considerably, some ranging from massive towers, to tiny microstrip antennas small enough to easily fit inside smartphones or some other small devices. An antenna's material and structure determines its properties, most notably what is referred to as its **radiation pattern**.

Radiation Pattern

In [27], a radiation pattern is defined as "a mathematical function or a graphical representation of the radiation properties of the antenna as a function of space coordinates. In most cases, the radiation pattern is determined in the far-field region and is represented as a function for directional coordinates. Radiation properties include power flux density, radiation intensity, field strength, directivity, phase, or polarization".

The radiation patterns vary considerably depending the antenna construction, which is why it is common to make use of heavily simplified models of antennas, primarily to help convey the behavior of and to act as a theoretical foundation for antennas in general.

Theoretically, the simplest antenna is a **isotropic antenna**, or **isotropic radiator**, which is defined as a point that is radiating equally in all directions without any loss of power. The isotropic radiator's radiation pattern is therefore visualized in 3D as a perfectly round sphere, otherwise known as a **unit sphere**, with its point *O*, called the **origin**, being in the center of the sphere.

If we were to supply some AC to a isotropic radiator, it would radiate EM waves in all directions equally, which would then spread outwards in a spherical fashion. Imagine drawing a small rectangle (area) on a balloon (radiation pattern), which signifies some amount of energy. Next draw a small point inside the area, which indicates some EM wave and its direction in relation to the origin. If we were then to expand this imaginary balloon, the area would expand accordingly as well, but the point would remain the same essentially. If we continued to do this, the point would eventually become infinitely smaller than the rectangle, e.g the energy that previously covered a small area is now covering a much larger space. EMR can be considered to act in a similar manner, where eventually all energy is spread out so much that there is barely any left at every particular point.

Directivity

The **directive gain** is a characteristic used to quantify the concentration of emitted radiation at a certain point *P* on an antenna's radiation pattern. In antenna theory it is common to make use of the spherical coordinate system as a representation of three-dimensional space. One can then define the directional angle from the origin *O* to the point *P* through the use of two parameters; the zenith angle θ , and the azimuth angle ϕ_a . The directive gain $D(\theta, \phi_a)$ is then given by the formula shown in Equation 3.3, where $U(\theta, \phi_a)$ is the radiant intensity, and P_t is the total radiated power of the antenna.

$$D(\theta, \phi_a) = \frac{4\pi \cdot U(\theta, \phi_a)}{P_t}$$
(3.3)

A isotropic radiator has a directive gain of 0 dBi for all directions, as its radiation pattern is a unit sphere, where dBi is a unit used to define the directive gain relative to the directivity of a lossless isotropic antenna. The **directivity** D_a is defined to simply be the maximum directive gain of an antenna.

Gain

Every antenna has a ratio called **gain** G_a , which is used to signify how well a antenna converts AC signals into or from radio waves. It is defined by the directive gain and the electrical efficiency ϵ_a of the antenna as shown in Equation 3.4. In short, a perfectly efficient antenna has a gain equal to its directive gain, which makes it lossless in theory.

$$G_a(\theta, \phi_a) = \epsilon_a \cdot D(\theta, \phi_a) \tag{3.4}$$

The plot of the gain is commonly used to refer to the radiation pattern of an antenna, but directive gain can be used as well. When talking about gain one is usually referring to the maximum gain, which is found by swapping the directive gain $D(\theta, \phi)$ with the directivity D_a .

Far-field Region

Continuing with the previous balloon analogy, imagine drawing in a grid-like fashion, tiny areas for the entire balloon. After expanding the balloon considerably, divide each area into even smaller areas. With the balloon having been expanded a certain amount, at some point each area will essentially be flat and not curved.

The aforementioned behavior is applicable to EMR in that a wave approximates to a **plane wave**, whose direction is constant and energy dependent on the distance only. The area in which this applies is called the **far-field region**, and is at a distance greater than $R_{ff} = D_{dim}^2/\lambda$ from the origin *O*, where D_{dim} is the maximum overall dimension of the antenna and $D_{dim} > \lambda$ [28]. The flattening is further demonstrated two-dimensionally in Figure 3.4, where it can be seen that the stippled lines (representing a tiny area) get flatter the larger the circle expands.

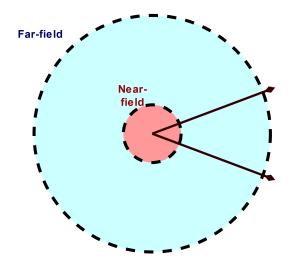


FIGURE 3.4: A simple demonstration showing how expanding a circle flattens the marked areas (stippled lines).

For a distance less than $R_{nf} = 0.62 \times \sqrt{D_{dim}^3}/\lambda$, we are in the **reactive near-field region**. The area inbetween the far-field- and reactive near-field region is **radiating near-field region**. In most cases, one will be dealing with the far-field region, as near-field usually covers at most a few metres for a regular UHF antenna.

3.1.2 Available energy

Friis equation

The **Friis transmission formula** is useful for getting an estimate on how much power one might expect to receive. One begins by assuming there is only coming transmission from one transmitter towards our receiver in a free space. The resulting power at the receiver P_R can then be calculated with Equation 3.5. Here P_T is the total power delivered to the transmitting antenna, G_T and G_R is the gain of the transmitting- and receiving antennas respectively, and R_a is the distance between the two antennas. It is very apparent that the distance R_a and frequency f has a significant impact on how much power will be available on the receiver antenna, and so in deciding which frequency to choose in terms of maximum P_R , they should ideally stay as small as possible.

$$P_R = \frac{P_T G_T G_R c^2}{(4\pi R_a f)^2}$$
 [W] (3.5)

Maximum transmittable power

With every nation having different laws on regulating man-made EMR, it is necessary to be aware of the maximum amount of power that can be transmitted by energy sources of interest. For our RF-EH designed around 1850 MHz, such sources would be telecommunication stations for mobile consumers, as they are abundant. According to [29] by the European Telecommunications Standards Institute (ETSI), the maximum output power that a modern GSM base station system is allowed to transmit for DCS-1800 (1850 MHz) is (>27)-32 dBm, which is equivalent to about (>0.5 W)-1.5 W.

To get some worst-case estimations, we can make use of Friis equation and a few assumptions. Firstly, we assume that our antenna is a isotropic radiator, meaning it has a gain $G_R = 1 = 0$ dB. Then we define a distance R_a , for which we pick 25 m. With us not being aware of the base station antenna gain, we assume it is a isotropic radiator as well, so $G_T = 1$. With these values, we end up with a P_R of -27.8 dBm (min) to -23.0 dBm (max). In reality an antenna is unlikely to be a isotropic radiator due to most of the energy being directed towards space, so this number would likely be greater, but it works well as a starting point for a estimate.

3.2 Semiconductors

In this section a crash course on how semiconductors work on the top level is presented, which will serve as a helpful foundation for later when elaborating on diodes, CMOS, and rectifiers.

A semiconductor is a general term for a component that is made out of materials that can act as both electrical conductors and insulators [30], e.g germanium and silicon, with the latter being the most common in modern electronics. At very low temperatures a silicon material acts as a insulator, whereas for higher temperatures it will conduct. A untreated silicon material is referred to as being **intrinsic**, meaning it has impurities.

A process called doping can be used on intrinsic silicon to purify it into what is called **extrinsic** silicon. There are two types of doped silicon: **n-type** and **p-type**. The n-type is negatively charged as it has an increased concentration of free electrons, whereas p-type is positively charged as it has an increased concentration of holes. A **hole** here is a term for a positively charged carrier, and is attracted to free electrons. Free electrons behave in a similar manner but inverted, being attracted to holes, while at the same time resisting other free electrons.

By combining a p-type and a n-type semiconductor, a **pn junction** is created. The physical connection between the two will influence the free electrons in the n-type to move and fill in the holes near the junction in the p-type semiconductor. The p-side of the junction will then build-up a negative charge, whereas the n-side junction will build-up a positive charge. These opposing charges create a electrical field *E* which acts as a barrier between the p- and n-type semiconductor called the **depletion region**, and will resist the flow of electrons across the junction.

There are two currents present in a pn junction: **diffusion current** and **drift current**. The diffusion current I_{Di} is an amalgamation of the movement of holes from p-side to n-side and electrons from n-side to p-side, and will flow from p-side to n-side. This current is strongly dependent on the **barrier voltage** V_0 of the pn junction, which is determined by the voltage drop caused by the electric field in the junction. The drift current I_{Dr} arises from some thermally generated electrons and holes moving back and forth between the junction, adding together to a current that goes from n-side to p-side. In a open-circuit with no external current being applied, the pn junction will enter a state referred to as **equilibrium** as shown in Figure 3.5, where $I_{Di} = I_{Dr}$. Should one of the currents change, then the contrasting current will change accordingly to maintain this equilibrium.

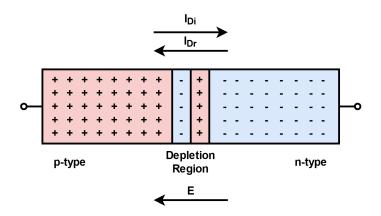


FIGURE 3.5: Illustration of a pn junction in a state of equilibrium.

3.2.1 Diode

A pn junction is essentially a diode in principle, with the p-side being defined as the **anode**, and n-side as the **cathode** [31]. This is illustrated in Figure 3.6. If a positive voltage v is applied on the anode of the diode such that it is more positive than the cathode, then the diode will start conducting current i from the anode and through the cathode. This is referred to as **forward biasing** the diode, and that the diode is in the forward-bias region.

If a positive voltage v be applied on the cathode instead such that it is more positive than the anode, then current i will flow from cathode and through the anode, which means the diode is being **reverse biased** and in the reverse-bias region. The amount of current being conducted when reverse-biasing is quite low compared to a forward-biased diode, and approximately equal to I_S . I_S is the **saturation current** of a diode and is directly proportional to the cross-sectional area of the diode. When reverse biasing, should v become greater than the **breakdown voltage** V_{ZK} , then the diode will enter the **breakdown region** and rapidly increase the current. This breakdown voltage varies based on how the diode is constructed and is usually found in a diode's data sheet.

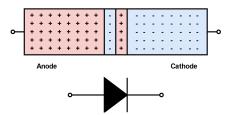


FIGURE 3.6: A illustration showing the equivalence of a pn junction and a diode.

The current *i* flowing through an ideal diode when forward-biased can approximately be expressed by Equation 3.6, where V_T is the **thermal voltage**.

$$i(v) = I_S(e^{\frac{v}{V_T}} - 1)$$
 [A] (3.6)

The thermal voltage V_T is proportional to the absolute temperature T, and is expressed by Equation 3.7, where k is the Boltzmann's constant and q is the electrical charge, both being constants. In room temperature V_T is roughly 25 mV.

$$V_T = \frac{kT}{q}$$
 [V] (3.7)

The amount of voltage needed to forward bias a diode and achieve good conductance is determined by the **diode threshold voltage** V_D , and changes based on the temperature *T*. Generally it is in the range of 0.6 V to 0.9 V for regular silicon diodes in room temperature.

A diode can therefore be considered to act as a one-way street for current to flow, ideally acting as a short-circuit looking into the anode side, but in reality there will be some resistance due to e.g parasitics caused by wires and packaging. For a higher voltage applied on the cathode, the cathode side will be perceived as open-circuited, and thus no current will flow across the diode ideally. The breakdown region is usually not a worry for RF-EH, as the voltages being dealt with are all far below what is considered to be low breakdown voltages for most diodes.

3.2.2 Schottky Diode

A **Schottky diode** is a specialized diode that is made out of some metal (anode) and a moderately doped n-type semiconductor material (cathode) [32]. It has two advantages over a pn junction diode. Firstly, it can switch on and off much faster than a regular diode, and secondly it can have a voltage threshold of just 0.3 to 0.5 V when forward-biasing, half of what regular silicon diodes requires. The latter property makes it well suited for ultra low power applications such as RF-EH.

3.2.3 CMOS

Before touching on how a CMOS is implemented, one needs to elaborate on the metal-oxide-semiconductor field-effect transistor (**MOSFET**), whom CMOS is a derivative of. A MOSFET is a three terminal device [33], made out of both n- and p-type silicon. There are N-channel (n-type) MOSFETs (**NMOS**) and P-channel (p-type) MOSFETs (**PMOS**), which refers to the type of the silicon connected to two of the terminals; the **source** *S* and the **drain** *D*. The third terminal is in the middle between the other terminals, and is called the **gate** *G*. We will be covering the general NMOS structure.

A side-view of a general NMOS structure is shown in Figure 3.7. The NMOS allows for variable voltage output based on a voltage input across the gate G, also known as a **voltage controlled voltage source** (VCVS). By varying the voltage going across gate G and source S, a channel will connect S and D, in which current can flow from D to S. Current will flow from G to S as well, but in a lot smaller quantities due to high impedance created by the gate oxide. The higher the voltage across G and S, the bigger the channel gets. If the voltage is too small, then the channel will big enough to connect S and D, thus no current will flow. The body B is the substrate and can sometimes have a terminal, which will create a pn junction between S and B, and will cause the body-effect. The PMOS is similar in its structure, but will have n-type flipped, and will have D and G pull current from S.

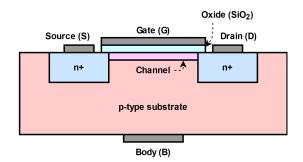


FIGURE 3.7: A side-view illustration of a general NMOS structure.

Then we can move on to the CMOS, which has a significantly more complex structure than a regular MOSFET. The CMOS combines NMOS and PMOS to end up with a semiconductor that has a low static power consumption and waste heat, which is realized by separating the NMOS and PMOS by a **n-well** that allows for less current to pass through the device when it is on.

3.3 **RF-DC Converter**

3.3.1 Impedance Matching Network

The input matching of the RF-DC converter is necessary for primarily two reasons.

Firstly, the impedance of the antenna for frequencies of interest needs to be matched so that the antenna load impedance is perceived to be equal by the antenna, this way the maximum amount of power can be transferred to the antenna load. This is applicable to any system dealing with electrical power in general, and is referred to as the **maximum power transfer theorem** (MPTT). The theorem states that **maximum power transfer** (MPT) across a load P_L is realized when the **load impedance** Z_L is the complex conjugate of the **source impedance** Z_S (antenna in our example). The complex conjugate property causes the reactance of both source X_S and load X_L to cancel each other out, leaving only the real parts R_S and R_L left, as illustrated in Figure 3.8. This gives us a purely resistive voltage divider where $R_S = R_L$, meaning half the total voltage will be applied across the load (V_L). Therefore only half of the total power in the system will go to the load at most, as the other half will rather go to the antenna itself. In most RF systems the antenna will have an impedance of $Z_S = 50 \Omega$ for some band of frequencies, and therefore MPT requires that the load is $Z_L = 50 \Omega$.

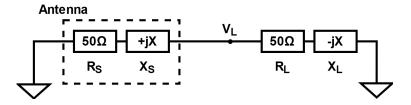


FIGURE 3.8: Illustration demonstrating how to MPT is achieved by having the load be the complex conjugate of the antenna.

Secondly, the **peak-to-peak voltage** V_{pp} of the input AC will increase with an increase in IMN resonance. Having a high enough V_{pp} is needed for diodes in the rectifier to operate in the forward-bias region. The resonance of a circuit is defined by the **Q-factor** or Q, and also defines the resonant **bandwidth** f_{Δ} of a circuit around some resonant frequency f_r , as shown in Equation 3.8. From this one can determine the maximum realizable Q for a given bandwidth at a certain resonant frequency.

$$f_{\Delta} = \frac{f_r}{Q}$$
 [Hz] (3.8)

The Q of an individual reactive component can be calculated by Equation 3.9. Here X is the inductive- or capacitive reactance, and R is the resistance.

$$Q = \frac{|X|}{R} \tag{3.9}$$

It can be seen that the Q-factor and MPT is related, as a Q > 0 leads to lower MPT due to a introduction of reactance. There is a balance that must be struck between these two, since neglecting one or the other leads to subpar performance, or none at all. If sufficient amounts of power is not being supplied to the rectifier semiconductors, then they will not operate reliable due semiconductor sensitivity limitations. If the Q is too low, then the V_{pp} will not be large enough to forward-bias the semiconductors, and therefore also not operate.

3.3.2 Rectifier

One can categorize the rectifier circuitry used in RF-EH into two types; **single-diode** and **voltage doublers**. A single-diode rectifier consists of one diode and a capacitor, with the diode being configured so as to block either the positive- or the negative cycle of the input AC. This type is also sometimes referred to as a **half-wave rectifier**. A positive half-wave rectifier is shown in Figure 3.9a, where the diode *D* rectifies the input voltage V_{in} , which then charges the capacitor *C* to some voltage V_{out} . Since half the wave does not get rectified however, half the power P_{in} is lost and thus $V_{out} = \sqrt{1/2} \times \sqrt{P_{in} \times R_L}$ at best, where R_L is the load resistance.

The Villard voltage doubler is more commonly used in RF-EH due to being a full-wave rectifier and supporting cascading. Cascading a voltage doubler is useful for achieving higher voltage multiplication, where each stage doubles the theoretical output voltage, as defined by Equation 3.10, where N is the total number of stages and V_p is the peak voltage of the input AC V_{in} .

$$V_{out} = 2N \times V_p \qquad [V] \quad (3.10)$$

The general topology for a cascaded Villard voltage doubler can be seen in Figure **3.9b**. The dark red stippled rectangle indicates components that make up one stage. There are two cases to consider; positive- and negative cycle of input AC.

During the positive cycle the capacitor C_1 blocks any DC, and diode D_1 acts as an open circuit. We are then left with a regular single-diode rectifier made out of D_2 and C_2 . For each additional stage the input AC splits and gets rectified as well, which adds another doubled DC voltage on top of the previous stage's output voltage.

In the negative cycle the current will be pulled from ground through D_1 , on the assumption that the input voltage supply (antenna) is connected to ground, and charge C_1 . Here D_2 will block AC pulled up through C_2 , and pull this current up to the next stage (if there are any) for additional rectification.

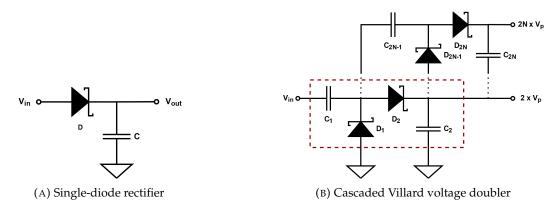


FIGURE 3.9: General rectifier topologies used in RF-EH.

Conversion efficiency

The PCE of the rectifier is calculated by comparing how much power goes into the rectifier P_{in} and across the rectifier load P_L as shown in Equation 3.11.

$$\eta = \frac{P_L}{P_{in}} \tag{W} (3.11)$$

The villard doubler as a system can be better characterized with the schematic shown in Figure 3.10, where Z_{in} is the impedance seen by the source Z_S (antenna) looking into the rectifier. We assume the source provides a single sine input AC voltage $V_A = V_{A,p} \times sin(2\pi ft + \phi)$, where $V_{A,p}$ is the peak voltage. The voltage across Z_{in} is $V_{in} = V_p \times sin(2\pi ft + \phi)$, where $V_p = V_{A,p} \times \frac{Z_{in}}{Z_{in}+Z_S}$.

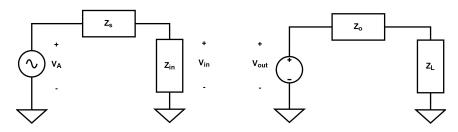


FIGURE 3.10: Schematic of a villard doubler circuit connected to a AC source.

To calculate the input power P_{in} the root mean square (RMS) of the AC voltage must be found, which for a sine wave is $V_{in,RMS} = V_p / \sqrt{2}$. Assuming the input matching is purely resistive ($Z_{in} = R_{in}$) and that we have MPT on the input, then P_{in} is given by Equation 3.12.

$$P_{in} = \frac{\left(\frac{V_p}{\sqrt{2}}\right)^2}{R_{in}} = \frac{V_p^2}{2R_{in}}$$
[W] (3.12)

For the output of the rectifier we have a DC voltage source V_{out} and some output impedance Z_o . If we assume the load and output impedance is purely resistive $(Z_o = R_o, Z_L = R_L)$, the voltage across the load V_L will be $V_L = V_{out} \times \frac{R_L}{R_L + R_o}$. Then the load power P_L is given by Equation 3.13.

$$P_L = \frac{(V_L)^2}{R_L} = 4R_L \times (\frac{N}{R_L + R_o} \times V_p)^2$$
 [W] (3.13)

The maximum attainable PCE for the rectifier is then found with Equation 3.14.

$$\eta = \frac{4R_L \times (\frac{N}{R_L + R_o} \times V_p)^2}{V_p^2 / 2R_{in}} = 8(N \frac{\sqrt{R_{in}R_L}}{(R_L + R_o)})^2$$
(3.14)

3.3.3 Power Management

The power management circuit is needed to make sure that the output voltage is large enough to be usable for the load, e.g a microcontroller. This can be accomplished by making use of a comparator circuitry that starts conducting the charged DC current to the load when a voltage threshold is crossed.

Chapter 4

System Design

4.1 Simulation

4.1.1 Advanced Design System

For all simulations we will be using Advanced Design System (ADS) by Keysight Technologies, which is an Electronic Design Automation (EDA) software bundled with useful design tools. It can be used to design electronic schematics, layouts, and do different kinds of time- and frequency-domain simulations e.g transient- and S-parameter simulations. It also supports EM simulation, which is needed for antenna simulations. ADS also comes with optimization tools, and is used to search for design parameters that gives the best results based on predefined goals. In our design process we will be using 50 Ω for all our input and output terminals when doing S-parameter simulations.

4.1.2 Microstrip & Substrate

When designing regular PCBs, the substrate and the microstrip is often not that crucial to the performance. In RF designs this rule is turned on its head, as the higher you go in terms of frequency, the more likely you are to stumble into parasitics and oddities. Accurately simulating these parasitics can be complicated, but ADS provides tools and components that aid in taking such parasitics in consideration. Microstrip substrates in ADS schematics are defined with *MSUB* components, and our values can be seen in Figure 4.1.

As we wanted to create a board that had a low threshold in terms of manufacturing and cost, we decided on FR-4 for our substrate, the most commonly used for manufactured PCBs. The dielectric constant *Er* can vary considerably with FR-4, with higher values increasing the capacitance between the top- and bottom layer, but in our schematics we chose 4.5, which is around average. Further we had to decide on a substrate thickness H, for which we chose 1.6 mm, which is also a standard for PCBs. The conductor material was chosen as copper. Finally we have the thickness of the microstrip conductor T, for which we use 35 µm. For the other values we have the conductor conductivity Cond in Sm^{-1} , the cover height Hu (for which infinite simulates an open space), and the dielectric loss tangent TanD, which varies considerably for FR-4.

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	MSub			
		L .		
	MSUB			
	100 C 10 C 10 C 10 C			
	MSub1			1
	H=1.6 mm		1	1
			1	1
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	Cond=587	òò	ó	ò
	Cond=587	00	υι	JU
	Hu=1e+33	m	m	1
• •				1
• •	T=35 um	• •		1
• •	TanD=0.02	, .		•
	ianD-0.02	•		1

FIGURE 4.1: Component used to define substrates in ADS, including the values used for our design.

4.1.3 Component modelling

All components have some form of parasitics, be it resistive, capacitive, or inductive, and can lead to significant losses e.g due to impedance mismatching. For this reason it is necessary to create sufficient models for components so that any circuit simulations are close to their real counterparts. A good balance between simple models and accuracy is desired, as increasing the complexity of models increases the time needed to do simulations.

Diode model

We will be modelling our diode based on the SMS7630 by Skyworks¹, which is a zero-bias diode that comes packaged in a Surface-Mount Device (SMD) casing. Skyworks has provided a diode model in their datasheet that includes parameters such as series resistance, non-linearities and junction capacitance. In ADS a custom diode model can be defined with a *Diode_Model* component as can be seen in Figure 4.2. Here all values are taken from the aforementioned datasheet. The two inductor components *Ls1* and *Ls2* are modelled after the total series inductance *Ls* of the diode, which is a inductive parasitic arising from the input and output pins used in the SMD IC. This inductance is split between the two inductor components, and can the value is given by the datasheet as 0.7 nH.

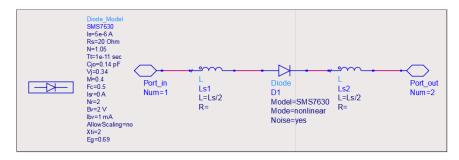


FIGURE 4.2: Skyworks SMS7630 diode model in ADS.

There are additional parts needed for the model to be more accurate however, as there are additional parasitics that arises due to the SMD packaging. This is shown in Figure 4.3 by comparing SMS7630 S-parameter measurements (red) provided by Skyworks on their website² against S-parameter simulations of our current model (blue). Plots for output reflection (S22) are not included here as they were equal to the input reflection (S11) readings, same goes for inverse gain (S12) and gain (S21). It can be observed that S11 is accurate enough at around 1850 MHz, our frequency area of operation, but for S21 we can see it is quite off across the entire spectrum by several decibels.

In the same graphs the S-parameter simulation of our expanded model is shown in magenta. In this expanded model the other parasitics introduced by the packaging is approximated by adding two additional components, as can be seen in the schematic in Figure 4.4. Both the inductor Lf and capacitor Cpp are caused by the packaging [34]. In some cases a parasitic capacitance Cp in parallel with the diode can be utilized, but in our case it did not make the approximation any better, so

¹https://www.skyworksinc.com/en/Products/Diodes/SMS7630-Series (Accessed 2021/06/11)

²https://www.skyworksinc.com/-/media/SkyWorks/Documents/Products/1701-1800/ SMS7630_079_S2P_Pin_0dBm.zip (Accessed 2021/06/11)

it was left out to reduce the model complexity. The values for these two components were found by using ADS optimization tools until the simulated S-parameter approximated the measured S-parameters. The expanded model is overall more accurate than our first model. Notice how S21 is now a lot closer to the measured performance, at the cost of a slightly less accurate S11 of around 0.2 dB for 1850 MHz.

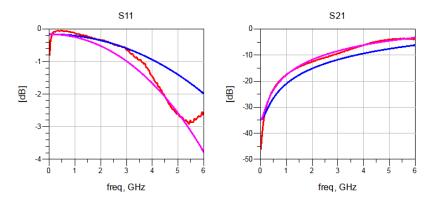


FIGURE 4.3: S-parameter comparison between Skyworks measured S-parameter data (red), our first SMS7630 diode model (blue), and our expanded model (magenta).

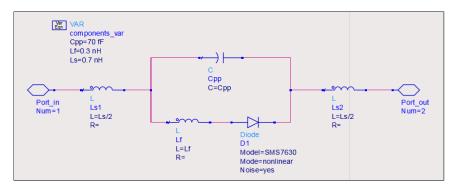


FIGURE 4.4: Expanded SMS7630 diode model that includes parasitics caused by the packaging.

We could continue to expand the model further to account for the S11 mismatch, but the S-parameter measurements only cover a input power of 0 dBm, and so the model will be less accurate for different input powers due to the non-linearity of the diode. In other words, even if our model was perfectly accurate to the S11 and S21 measurements provided, it would lose that accuracy if different input powers were used in the simulation. As Skyworks has not provided any measurements for other input powers at the time of this writing, this is the best middle-ground for accuracy and model simplicity as of now.

Passives

All RF-DC converters need at least one capacitor to not only charge, but to store DC from AC that is rectified as well, for it later to act as a power source. Additionally, there are motivations for using lumped capacitors e.g to create resonance tanks on

the input for better matching or a higher Q-factor. In our design we have decided to use the R14S capacitors by Johanson Technology³, which are SMD packaged at a size of 0603 (1608 metric). These capacitors are well-suited for RF circuitry such as mobile and WiFi, and have low equivalent series resonance (ESR) so that power dissipation is kept low. As with the SMS7630 diode, the R14S capacitors can be modelled through the use of S-parameter measurements provided by the company⁴. It is possible to make use of the measurements directly in the design, but these measurements can not be optimized without having to manually switch out the component values, which is why we are making use of a model instead.

The model we are using is an approximation of these measurements, and is intended for values ranging from 1- to 82 pF. Its ADS schematic can be seen in Figure 4.5, and consists of a series inductor *L1* (which includes series resistance) and capacitor *C1*, and two shunt capacitors *C2* and *C3* going to ground. The variable *C* in the component equations is the user-defined capacitance for the component.

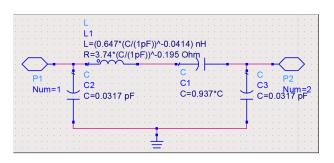


FIGURE 4.5: Capacitor model of R14S series by Johanson Technology, intended for values ranging from 1- to 82 pF. Original author: Morten Olavsbråten

The series resistance and inductance approximates the ESR and equivalent series inductance (ESL) of the capacitor, where the latter is a parasitic arising from the packaging leads. The shunt capacitors are estimates on the capacitance that is derived from the capacitor (assuming its on the top layer) and bottom layer (assuming ground) of the PCB acting as a capacitor, where the substrate of the PCB is the insulator. This capacitance can vary depending on the substrate and bottom layer material, where more insulated substrates usually cost more.

A comparison between the measured S-parameter (red) and the model (blue) is depicted in Figure 4.6, where the dotted lines are for a 1 pF capacitor, and solid lines are for 82 pF. As with the diode comparison, S11 is equal to S22, and S21 is equal to S12. The gain S21 is quite good for both cases, whereas the input reflection S11 is only accurate for up to 3 GHz with 1 pF. For 82 pF the matching is not that good, and is a consequence of the model being an approximation of all S-parameter measurements ranging from 1- to 82 pF. On one hand, a greater accuracy could be found by expanding the model with additional components or by focusing on a smaller range of capacitances. On the other hand, for our use case it should be usable, as we will be using small capacitances with our converter and work with frequencies lower than 3 GHz. The higher capacitances should therefore in our design be reserved for DC applications.

In our design we will also make use of inductors for matching, resonance and capacitance cancelling purposes. The inductors used are also made by Johanson Technology, and are part of the L14S series⁵. As with the capacitors, they are also intended for RF applications such as mobile and are of sizes 0603 (1608 metric), covering an inductance range of 1.0- to 220 nH. The method used in creating the model

⁴https://www.johansontechnology.com/s-parameter (Accessed 2021/06/11)

³https://www.johansontechnology.com/R14S (Accessed 2021/06/11)

⁵https://www.johansontechnology.com/ceramic-inductors (Accessed 2021/06/11)

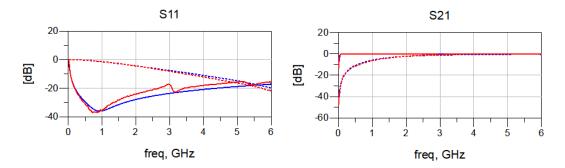


FIGURE 4.6: S-parameter comparison between R14S S-parameter data (red) and our capacitor model (blue).

is the same as with the R14S capacitors, the S-parameter measurements provided by the same company.

There are two models made to improve accuracy, one ranging from 1- to 8.2 nH shown in Figure 4.7 (low-inductance model), and 10- to 220 nH shown in Figure 4.8 (high-inductance model). Here L is the user-defined inductor value. Shunt-components C2 and C3 functions the same as the capacitor model. There are more advanced parasitics found in the inductor due to its physical design being a lot more complex than the capacitor, so there is more to consider. We do not have insight into the design itself, but such small inductors are commonly designed in the form of a swirl- or a wave-like structure, where inductance is being generated by the sharp corners. Therefore due to the tiny distance between the adjacent lines, there will be capacitive parasitics arising. There are also resistive parasitics existing due to the component lines being quite limited in size, so current has less space to conduct through.

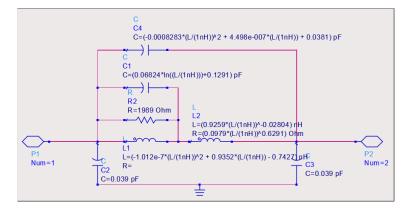


FIGURE 4.7: Inductor model of L14S series by Johanson Technology, intended for values ranging from 1- to 8.2 nH. Original author: Morten Olavsbråten

Comparisons between S-parameter measurements and low- and high-inductance models are shown in Figure 4.9 and Figure 4.10, respectively. The graphs follow the same plotting rule-set as capacitor, red being measurements, blue being the model. For the low-inductance model, the dotted line is for 1.0 nH and solid is 8.2 nH. For high-inductance model its 10 nH dotted, and 82 nH solid. Besides a few dips here and there, the models are quite on point overall, especially around 1850 MHz.

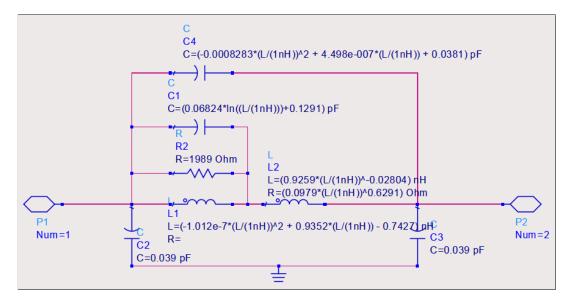


FIGURE 4.8: Inductor model of L14S series by Johanson Technology, intended for values ranging from 10- to 220 nH. Original author: Morten Olavsbråten

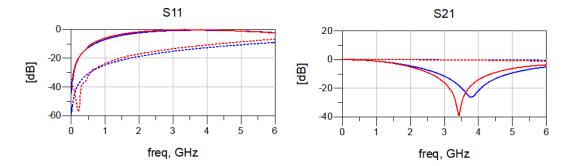


FIGURE 4.9: S-parameter comparison between L14C S-parameter data (red) and our low-inductance model (blue).

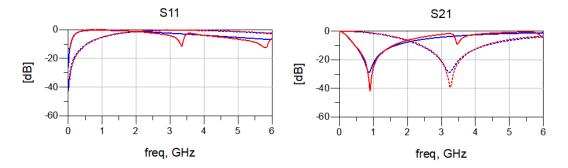


FIGURE 4.10: S-parameter comparison between L14C S-parameter data (red) and our high-inductance model (blue).

4.2 Antenna

The design of the R-FEH is highly dependent on what type of antenna will be used. This is a consequence of the MPTT, which tells us that both the antenna and rectifier must be matched accordingly for us to attain MPT. This is an essential requirement for all RF systems in general, but even more so for our case as we want to make sure we waste as little power provided by the antenna as possible.

In the same vein, we want to have the antenna to convert all potential EMR to AC power. The antenna will however need to be matched to a certain bandwidth for it to efficiently absorb EMR of particular frequencies, and therefore we must first decide on what those frequencies will be. This step is important to get right the first time, as all later design work will depend on it. Since we are only concerned about EMR with the most energy that also resides in the UHF band, a preliminary estimate on expected energy can be found by doing spectrum measurements at the location we are working with.

4.2.1 Preliminary Spectrum Measurements

The EMR at a particular location varies depending on a lot of factors like the environment (both static and dynamic objects) and EMR interference (e.g from industrial equipment). It is therefore practical to decide on where the RF-EH will be used so that such variables can be accounted for. Having the location be fixed is also advantageous as that means we can worry less about ambient RF sources being present or not, particularly when it comes to radio masts and towers. We therefore settled for a fixed location at NTNU Gløshaugen.

With the help of antenna information provided by the Norwegian Communications Authority (NKOM)⁶ we got an overview of three nearby commercial antennas, as demonstrated in Figure 4.11. Each red line in the figure roughly indicates the distance between each antenna and our location. These distances were found by using the distance measuring tool in Google Maps⁷, but it is worth mentioning that this tool does not take height coordinates into the equation. These investigations were done back in 2019 and would be the basis for the requirements that we made for our RF-EH design. One of the challenges that comes with relying on static ambient RF sources, is that they will inevitably change someday or be removed entirely e.g due to technological innovation (such as the recent introduction of 5G). The figure's defined antenna frequencies were given based on standard frequency bands used in telecommunications and the proximity, so for example here it shows the closest 1800 MHz antenna being 25 m, whereas the closest antenna transmitting at 800 MHz was 200 m. Such antennas actually operate in multiple different frequencies bands, and the antenna 200 m from our location was also working with 1800 MHz, but it was not included in the figure as the nearest 1800 MHz antenna EMR would greatly exceed that of the one 200 m as implied by Friis equation.

Before doing any spectrum measurements we needed an antenna to pick up signals, which would then act as a reference antenna later when comparing it to the antenna we would design for our RF-EH. The antenna we used was a custom-made, 50Ω folded dipole antenna resonating at around 900MHz and can be seen in Figure 4.12. Ideally the reference antenna's resonance would be tunable to the frequency bands being investigated and calibrated such that the input reflection coefficients

⁶https://finnsenderen.no (Accessed 2021/06/11)

⁷https://www.google.com/maps (Accessed 2021/06/11)

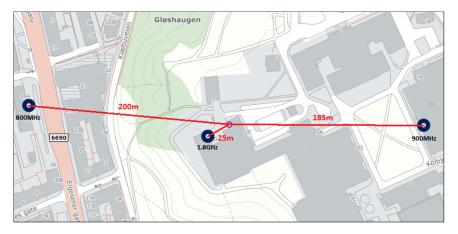


FIGURE 4.11: Map showing the location of the three closest commercial antennas relative to our location (NTNU Gløshaugen).

were equal for the bands in question. Since we had no such equipment at our disposal in this project, we had to keep in mind that any EMR measured outside of 900 MHz would actually be more than what spectrum measurements told us. Another problem was the radiation pattern of the antenna, which in our case was such that its main lobe was coming out on the front of the loop (the long side), and therefore had to be pointed towards incoming EMR for the best results. In our approach we pointed it in the general direction of the aforementioned three antennas. The spectrum analyzer used when doing these and any future measurements was the portable Anritsu MS2721A.

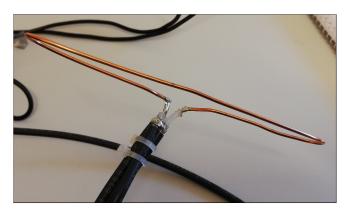


FIGURE 4.12: The custom-made, 50 Ω folded dipole antenna used as a reference antenna for our spectrum measurements.

At our location we looked at the three frequency bands 800, 900- and 1800 MHz, and measured their minimum (worst-case), average (10 samples) and maximum (best-case) power, as shown in Table 4.1. A few observations can be made given what we know about our reference antenna. Firstly, it can be seen that 800 MHz had approximately five times more power to offer than 900 MHz on average, despite our antenna's resonance. Secondly, 1800 MHz showed a significant improvement for all cases, and had on average around 26 times more power than both 800- and 900 MHz combined. Undoubtedly, the major proponent behind this huge difference in available EMR was the distance to the already identified RF sources. The 1800 MHz total bandwidth was 120 MHz, but most of its power actually resided from 1830- to

1870 MHz, which was a good sign as a designing an antenna with a wider bandwidth leads to a smaller realizable Q-factor and thus loss in realizable power. With these observations in mind, we concluded that 1850 MHz would be a good resonant frequency to base our antenna design on, as not only did it greatly outperform the other bands, but we were also aware that there was considerably more power to be picked up with better frequency matching. Working with higher frequencies also means that the physical antenna can be smaller for it pick up the EMR, due to the wavelengths being smaller.

	Center Frequency [MHz]	Total Bandwidth [MHz]	Minimum [dBm]	Average [dBm]	Maximum [dBm]
П	806	60	-49.1	-46.5	-42.7
	942.5	31	-53.2	-53.9	-49.1
	1850	120	-32.4	-31.6	-25.6

TABLE 4.1: Power measurements of noticeable EMR peaks using our reference antenna and a spectrum analyzer.

4.2.2 Requirements and Goals

The antenna to be designed has be built such that its resonant frequency f_r is at 1850 MHz, with its bandwidth f_{Δ} being 40 MHz, which tells us the best possible Q-factor will be approximately 46. This extends to the design of the rectifier's input matching as well. For the impedance we will be using the same impedance as our reference antenna, not only for performance comparisons but also because 50 Ω is the standard for antennas and RF in general.

Designing an antenna that provides the most power is not a straightforward problem, as one has to consider the usage. Due to how the gain and radiation pattern of an antenna is related, a trade-off between a high amount of gain and radiation pattern shape needs to be found for us to overall get a lot of power. Realizing a high gain means the antenna will have a narrow bandwidth, and since we have already defined this bandwidth to be 40 MHz, the Q-factor tells us the maximum gain for the antenna main lobe will be $G_{max} = 33$ dBi. This is quite high and not something easily attained using a passive antenna and off-the-shelf components, so we will have to settle for a lot less. On the flip side, this will be more appropriate as the intended use case for our RF-EH is to get power from ambient RF sources, which in practice will be spread around the surroundings of the RF-EH. In most use cases, these sources will not be too high above or below our device, so something like a toroid radiation pattern shape would be the absolute minimum requirement. This is also coincidentally the radiation pattern for a regular dipole antenna.

As the design of the antenna and RF-EH is a co-dependent process, we found through preliminary rectifier simulations that we would need atleast -13 dBm to get a DC output voltage of 2 V. We can therefore assume, given a maximum power measurement of $P_i = -25.6$ dBm for 1850 MHz, that the minimum antenna gain requirement will be the difference, that is $G_{min} = -13dBm - P_i = 12.6$ dBi.

4.2.3 Design and Layout

For a passive antenna, the radiation pattern is determined by its size and form. We want to have the antenna be easy to manufacture on the assumption that it will be mass-produced with the RF-EH for uses such as IoT, and one common way to achieve this is with microstrip antennas.

Microstrip Antenna

Microstrip antennas are convenient as they can be fabricated directly on PCBs and tend to not need as much space as other forms of antennas like dipole- and horn antennas. This is due to the microstrip itself mostly scaling in width and length, but not height, and so they are commonly found in thin devices like smartphones. These antennas are also straightforward to design and simulate in software such as ADS, as one can either generate it from a schematic or manually draw the layout, and then do EM simulation.

The scaling is often dependent on two things; the resonant frequency and number of elements. Since size is proportional to the resonant frequency, microstrip is commonly used in high frequency RF design. The number of elements specifies how many duplicates of a single microstrip antenna design is connected together to form a bigger antenna, referred to as an antenna array. This is usually done to increase the gain, as the elements radiation patterns will accumulate to form a more prominent main lobe, provided the array is symmetrical and elements are matched properly.

A microstrip antenna works somewhat like dipole antennas, but instead of having two conducting rods acting as two poles with the same orientation, separated by some distance, we have two conducting layers in parallel separated by a substrate as demonstrated in Figure 4.13. The two conducting layers are often referred to as the top- and bottom layer, with the bottom layer commonly being ground. Whereas the dipole expels its electric field in its main and and back lobe to create a toroid 3D radiation pattern, the microstrip antenna has most of its electric field reaching far out through its main lobe in the form of a bubble-like shape, the ground acting as a shield to shrink the back lobe. The radiation pattern itself can be changed based on the layer layout. More freedom and flexibility with the shape can also be attained at cost of increased complexity by creating a sandwich of added layers and substrates. The solid substrate holds the antenna in place but comes with the price of being lossy, allowing more of the EMR to seep into the ground plane instead of outwards. The material's lossiness is based on its dielectric constant ϵ_r , for which vacuum has $\epsilon_r = 1$, and as such the solid substrates with lower ϵ_r (e.g Teflon) are more expensive.

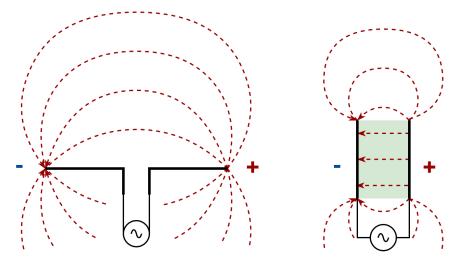


FIGURE 4.13: Illustration demonstrating the difference in topology and electric field between both ideal dipole- (left) and microstrip antenna (right), with red lines representing the electric field lines.

Patch Antenna

The type of microstrip antennas are categorized based on their layout, as the inherent capacitive and inductive parasitics found in microstrip can be exploited through careful design to attain one or more desired resonances. A common microstrip antenna that is relatively simple to manufacture is the patch antenna, where the top layer is shaped as a patch in the form of a rectangle or circle, with bottom of the substrate covered in its entirety by the ground layer. For our antenna we will be creating a rectangle patch antenna array, as it is easier to design in software and tune after manufacturing than circular.

Instead of designing the entire layout of the array from the start, we begin with the design of a single patch, which will be identical for all the elements in the array. Our single rectangular patch antenna layout is shown in Figure 4.14, and includes a inset feed, which can be identified by the short input line of length L_{vi} . The inset feed is a common matching technique used in tandem with patch antennas and helps in getting a more desirable resonant input resistance, at the cost of introducing a junction capacitance.

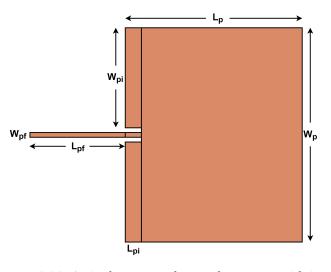


FIGURE 4.14: A single rectangular patch antenna with inset feed of length L_{pi} .

The preliminary design approach in finding the antenna parameters is done through the use of equations from [35]. The width W_p of the patch determines the resonant frequency f_r , and is calculated with Eq. 4.1. Given that we want a resonant frequency of $f_r = 1850$ MHz and have a dielectric constant of $\epsilon_r = 4.5$ from using a FR-4 substrate, we get an estimated width of $W_p = 48.9$ mm.

$$W_p = \frac{c}{2f_r} \sqrt{\frac{2}{\epsilon_r + 1}} \tag{4.1}$$

Before we move on to estimating the length L_p , we first calculate the effective dielectric constant ϵ_{reff} with Eq. 4.2. This is done to account for fringing effect and electric field line wave propagation, which is the case when $W_p/h \gg 1$ and $\epsilon_r \gg 1$. Given the substrate thickness h = 1.6 mm, we get an effective dielectric constant of $\epsilon_{reff} = 4.23$.

$$\epsilon_{reff} = \frac{\epsilon_r + 1}{2} + \frac{\epsilon_r - 1}{2} [1 + 12\frac{h}{W_p}]^{-1/2}$$
 (4.2)

The fringing effect will change the apparent length L_p of the patch by ΔL_p , and is approximately calculated with Eq. 4.3, which gives us $\Delta L_p = 0.74$ mm.

$$\Delta L_p = 0.412h \frac{(\epsilon_{reff} + 0.3)(\frac{W_p}{h} + 0.264)}{(\epsilon_{reff} - 0.258)(\frac{W_p}{h} + 0.8)}$$
(4.3)

The actual length L_p can now be estimated with Eq. 4.4, and so we end up with $L_p = 37.9$ mm.

$$L_p = \frac{c}{2f_r \sqrt{\epsilon_{reff}}} - 2\Delta L_p \tag{4.4}$$

For the other parameters there are also equations that can be used to find estimates, but we are choosing to find them through the use of ADS optimization tools instead, out of convenience. This approach has some problems however, as the optimization space is large due to the many parameters being worked with, so the time needed for the optimization algorithm to stumble upon the global maximum could vary considerably, assuming a random search is used. Since we are going for an array of patches, we do the optimization of the array microstrip lines together with the single patch feed parameters. These lines connect the patch elements together, with the goal of the array being perceived as having a certain impedance at f_r , which in our case is 50 Ω . For a rectangular patch antenna, it is desirable for us that the array is as symmetrical as it can be, which means we should have $M \times M$ elements. This allows for each element's main lobe to accumulate into one big main lobe at the center of the elements.

One might think that the gain of the array will be the gain of a single patch times the number of elements, but due to the spacing needed between the elements, which is dependent on the resonant frequency f_r wavelength, the array main lobe will eventually stop getting much narrower as more elements are introduced. A trade-off between size and gain must therefore be made, for which we choose M = 2. This keeps the antenna at a moderate size while also allowing for an increased potential gain. The potential gain of the 2x2 array would ideally be four times the gain of a single patch, but element spacing will lower this multiplier.

Our array layout can be seen in Figure 4.15. The array lines (light brown color) are vertically symmetrical, with each single patch (element) colored in grey. The parameters for the patches and the array lines can be found in Table 4.2. The previously estimated width W_p and length L_p were changed slightly through optimization for better performance.

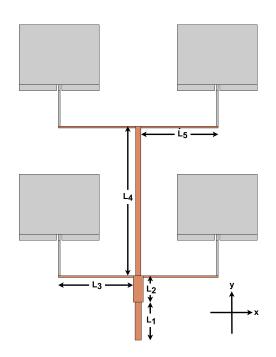


FIGURE 4.15: The final layout of our 2x2 array that is symmetrical along the y-axis. Width parameters are not shown, but for all array

lines n = 1, 2, 3, 4, 5 we have $L_n > W_n$.

Patch Parameter	Value [mm]	Array Parameter	Value [mm]
W _p	46.7	W_1	3.0
L_p	38.7	L_1	22.2
W _{pi}	1.2	W2	5.2
L'_{pi}	3.5	L_2	15.6
W_{pf}	0.6	W_3	0.6
L_{pf}	20.6	L_3	44.6
		W_4	2.4
		L_4	88.6
		W_5	0.6
		L_5	46.0

 TABLE 4.2: Design parameters used for the single patch antenna and antenna array.

The simulated radiation pattern of our antenna can be seen in Figure 4.16, where the main lobe can be seen in the center, with small side lobes protruding from the sides. The input line of the antenna is coming in at -y (0°). The lack of symmetry around the x-axis is demonstrated by looking at the x-axis side lobes, which are angled forward.

The simulated gain of the main lobe is about G = 6.76 dBi, with a radiation efficiency of 27.3%, as the maximum directivity is $D_a = 12.4$ dBi. For the remaining 5.84 dBi gain that is required we assume that our antenna has a considerably better matching for 1850 MHz compared to our reference antenna, such that the minimum required gain G_{min} is sufficiently lowered for us to get a input power $P_i = -13$ dBm.

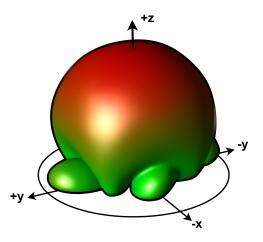
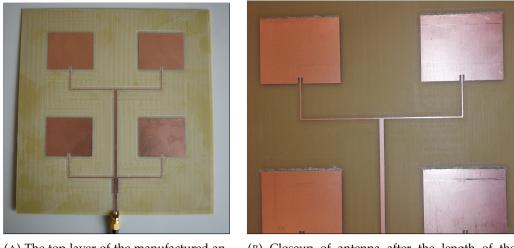


FIGURE 4.16: Simulated radiation pattern of our antenna, where zaxis illustrates the magnitude in dBi.

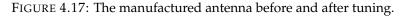
4.2.4 Manufacturing and Tuning

The antenna seen in Figure 4.17a was manufactured in FR-4 Copper Clad Laminate (CCL) with copper thickness $35\mu m$ through a milling process. The substrate thickness ended up being 1.5 mm as 1.6 mm was not available for the PCB area of $200mm \times 210mm$ that we required. The matching was a little off and resonated at 1810 MHz, the likely cause being physical inaccuracies from the milling process, the variability of dielectric constant in FR-4 substrates, and the slightly thinner substrate thickness. By chipping off the elements length by about 0.7 mm as seen in Figure 4.17b, the matching was adjusted to 1845 MHz.



(A) The top layer of the manufactured antenna.

(B) Closeup of antenna after the length of the patches have been chipped equally.



4.2.5 Performance Comparison

Input Reflection

A S11 comparison plot for the antenna is presented in Figure 4.18, and some values of interest taken from the plot is included in Table 4.3. The most noticeable difference between simulation and our tuned antenna is that the simulation goes a lot deeper, where approximately nothing is reflected. For our tuned antenna around 7.2% of the incoming EMR at $f_r = 1850$ MHz is reflected, and the antenna covers a bandwidth (BW) of 40 MHz, which is quite close to the simulation.

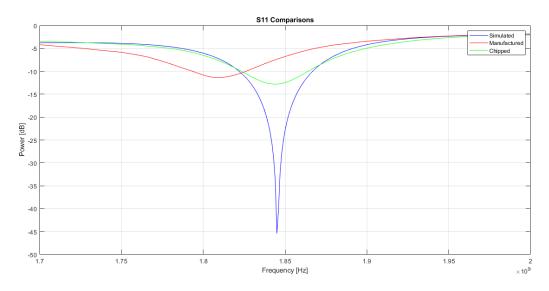


FIGURE 4.18: Diagram of S11 for simulated, manufactured and chipped (tuned) antenna.

	Frequency [MHz]			Matching [dB]			[%]		
Antenna	-10 dB	f_r	-10 dB	BW	1.8 GHz	1.85 GHz	1.9 GHz	fr	BW of f_r
Simulated	1823	1845	1867	44	-6.04	-22.90	-4.20	-45.42	2.38
Manufac.	1793	1810	1826	33	-10.69	-6.77	-3.48	-11.37	1.78
Tuned	1824	1845	1864	40	-6.52	-12.48	-4.96	-12.81	2.16

TABLE 4.3: Resonant frequency f_r , -10 dB matching frequencies around f_r , bandwidth coverage for -10 dB around f_r , and input matching (S11) for frequencies of interest.

Radiation Pattern

Diagrams comparing co- and cross-polar radiation patterns between simulated and manufactured antenna can be seen in Figure 4.19 and Figure 4.20, respectively. The antenna has a vertical polarity. We can see that our manufactured antenna (red plot) has a significant back lobe compared to simulated (blue plot), which means more power will be expanded in the back and thus lower the maximum antenna gain. The most probable cause for this back lobe is the lossiness of FR-4 and the EM simulation not taking it into consideration.

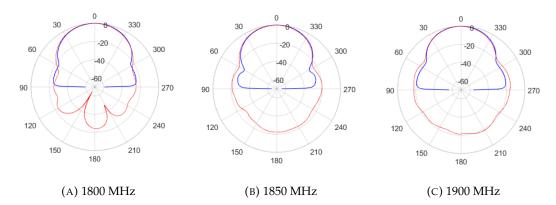


FIGURE 4.19: Co-polar radiation pattern comparison between simulated (blue) and manufactured (red) antenna.

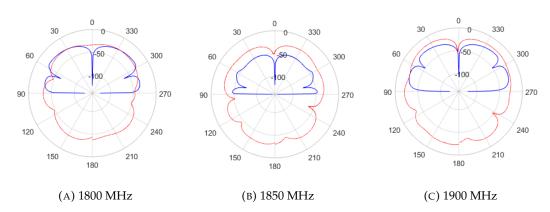


FIGURE 4.20: Cross-polar radiation pattern comparison between simulated (blue) and manufactured (red) antenna.

Spectrum Measurements

Another round of spectrum measurements were done at the same location so that our antenna (patch) and reference antenna (dipole) could be compared. The measurements are shown in Table 4.4, including the difference in dBm. The EMR present overall around 1850 MHz was a lot less this time compared to our preliminary measurements, the most likely reason being that the transmitting antenna nearby was transmitting less.

From the measurements we can see a noticeable difference between the two, where our best case (max) demonstrated that our antenna can provide 12.4 dBm more. Assuming the gain of our manufactured antenna is a bit below our simulated gain due to losses from back lobe and lower radiation efficiency, say G = 6 dBi, then roughly 6.4 dBm would be gained from the matching alone. As we need a power increase of atleast 12.6 dBm, the antenna is performing slightly below the minimum requirement.

Туре	Min.	Avg.	Max.
Patch	-29.0	-26.9	-19.4
Dipole	-39.6	-37.2	-31.8
Difference	+10.6	+10.3	+12.4

 TABLE 4.4: Power spectrum measurements of our manufactured, chipped antenna and reference antenna.

4.3 **RF-EH**

4.3.1 Requirements and Goals

For our RF-EH design we want it to be able to produce a DC output voltage of at least $V_{out} = 2$ V, given a sine wave of input power $P_{in} \ge -13$ dBm with a frequency of $f_r = 1850$ MHz. On the assumption that the antenna impedance is $Z_s = 50 \Omega$ and we have MPT due to $R_{in} = 50 \Omega$, theoretical calculations tells us that the input peak voltage will equal $V_p = \sqrt{2P_{in}R_{in}} = 70.7$ mV. The number of stages *N* will then have to be $N = \frac{V_{out}}{2V_n} \ge 15$.

4.3.2 Topology and Techniques

Having fifteen stages is not that much of an issue in small-scale IC's, but on a PCB it will end up taking a lot of space. Furthermore, it is not even the biggest issue that comes with having more stages on a PCB. Research into cascaded villard doubler's [16] has found that as more stages are added, less is gained in terms of increased output voltage. This is due to the increase in non-linear parasitics partly due to the diodes, which makes matching even more difficult as energy is being lost in both substrate and diodes.

Consequentially, the energy losses will decrease the overall efficiency of the RF-EH. It is therefore better to make use of techniques such as the ones discussed in Section 2.1 to achieve high enough output voltage while keeping the number of stages at a minimum, a common choice being to make use of a ultra-low power, DC-to-DC converters. We will not be using such a device in our design as it is outside the scope of this thesis.

Diode Capacitance Cancellation with Inductors

In [13] the authors make use of inductors in series with their diodes to cancel out the diode capacitances and increase the output voltage. This technique only requires one inductor for each diode, but getting the matching right is not easy as we are working with discrete components, and thus have few parameters to work with and optimize. It is therefore crucial that the simulated models are accurate, as elaborated on in Section 4.1.3.

The inductor will allow for even higher output voltages due to its self-resonance, and therefore less stages can be used to satisfy requirements related to the output voltage V_{out} . The inductor will spike the peak voltage coming in, and thus the voltage going out will be higher. Placing the inductor before the diode is recommended to further lower the minimum input power required to operate the diodes. A good inductor choice would therefore have a high self-resonant Q close to f_r . In our design we use an inductor value of 12 nH, which has a calculated Q-factor of 2.93 at f_r according to our model. This resonance almost triples the incoming AC peak voltage before it is being fed into the diode and rectified.

In Figure 4.21a, Figure 4.21b and Figure 4.22 the S11, impedance, and resistance & reactance of our diode model with and without capacitance cancellation is compared, respectively. These simulations are done using a large signal S-parameter (LSSP) simulation, where the input is a sine wave with input power -13 dBm. Notice how the impedance drops from around 500 Ω to 106.5 Ω at f_r , which in turn greatly lowers the input reflection (S11) from around -1 dB to -8.2 dB, and thus less power is being reflected from and wasted in the diode.

Due to the complexity of our inductor model, an easy approach in finding a good inductor value is through optimization. As microstrip lines introduce parasitics, these should be included in the optimization as well to achieve more accurate cancellation. The process of determining the layout should be done with this in mind.

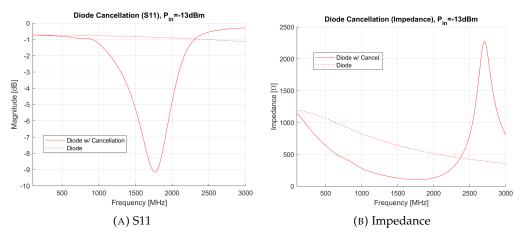


FIGURE 4.21: Simulations demonstrating the effect capacitance cancellation has on input reflection and impedance.

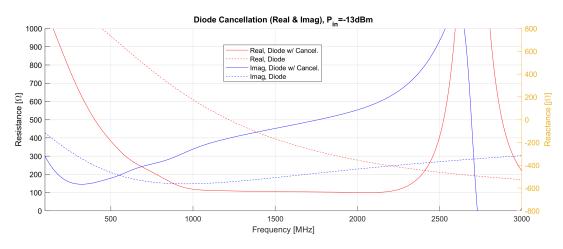


FIGURE 4.22: Simulations demonstrating the effect capacitance cancellation has on resistance and reactance.

High-side Load Switch

The most straightforward way to get more voltage on the output is to increase the load impedance, at the cost of a lower efficiency. The microcontroller we are designing the RF-EH for, the ATMega4809, has a voltage supply impedance of 333 $k\Omega$. We can get a greater load impedance by having a High-Side Load Switch (HSLS) between the rectifier output and the microcontroller. It acts as a high impedance load up until a certain voltage threshold is crossed on the rectifier output DC voltage V_{out} , then it switches so the load becomes the microcontroller, which then gets powered by the energy stored across the capacitor on the output of the rectifier.

The MIC94090⁸ by Microchip lets us do this. It has an enable pin that determines if the HSLS can conduct to the connected load. This enable pin has an internal impedance of 2 $M\Omega$, so if we place a 4 $M\Omega$ external resistor in series with the pin such that we have a voltage division of the output DC voltage V_{out} , we create a voltage threshold that is surpassed when $V_{out} \approx 2$ V. In total this gives us a load impedance of 6 $M\Omega$ when charging up the capacitor, which then more easily charges up to 2 V than if the impedance was 333 $k\Omega$.

With our design being a prototype, we choose to use a regular resistor with a load impedance close to the HSLS when the RF-EH is charging, as we are most interested in how high we can get the charging voltage with the least amount of input power.

4.3.3 Input Matching & Q-Factor

The topology chosen for the IMN comes down to experience and experimentation. On one hand we want it to be matched to 50 Ω for $f_r = 1850$ MHz, but on another hand we want a somewhat high Q-factor so that the peak voltage V_p is increased. If the Q-factor or less than 1, then the peak voltage coming into the input of the diode will be less. This is most troublesome should it happen when working with quite low input powers e.g -10 dBm as then the diodes are already struggling to conduct, although the diode capacitance cancellation inductor can mitigate this.

In our IMN design we have a series resonator made out of a capacitor and an inductor in series such that it resonates at around f_r . Before this resonator we have a microstrip line used for further matching while also acting as the input line for AC coming from the antenna.

4.3.4 Diagram

A diagram of our RF-EH design without any microstrip lines is shown in Figure 4.23, and the components we are using is listed in Table 4.5. The series resonator is formed by L_1 and C_1 , whereas L_2 and L_3 are the diode inductors. Lastly there are the capacitors C_2 and C_3 used to charge and store the DC energy.

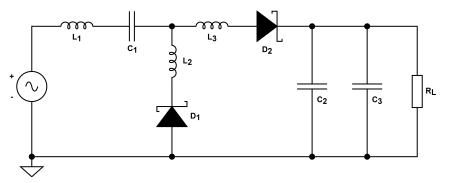


FIGURE 4.23: Diagram of RF-EH design without microstrip lines.

Component Tolerance

A simulated sensitivity analysis taking the tolerances into account found that the components with the most detrimental effect on the output voltage were the inductors L_2 and L_3 . Their independent influence on V_{out} can be seen in Figure 4.24a and Figure 4.24b.

⁸https://www.microchip.com/wwwproducts/en/MIC94090 (Accessed 2021/06/11)

ID	Manufacturer	Part Number	Comment
$D_1 \& D_2$	Skyworks Solutions	SMS7630-079LF	RF Schottky Diode
L_1	Johanson Technology	L-14C1N0SV4T	SMD, 1.0 nH \pm 0.3 nH
<i>L</i> ₂ & <i>L</i> ₃	Johanson Technology	L-14C12NJV4T	SMD, 12 nH \pm 5%
C_1	Johanson Technology	251R14S3R9CV4T	SMD, 3.9 pF± 0.25 pF
<i>C</i> ₂	Johanson Technology	251R14S2R7BV4T	SMD, 2.7 pF± 0.1 pF
<i>C</i> ₃	Johanson Technology	251R14S820JV4T	SMD, 82 pF± 5%
R_L	N/A	N/A	General Through Hole Resistor, 500 mW, 6.8 M $\Omega \pm$ 5%

TABLE 4.5: Components used in the design.

For L_2 we calculate a linearly proportional change in voltage of $\pm 15 \text{ mv/nH}$, which tells us we would ideally have more inductance for L_2 . With L_3 we have -21.5 mV/nH for a lower inductance and -28.5 mV/nH for a higher inductance. The series inductor has a bigger impact on V_{out} as the negative half-wave of the input AC will be rectified by the shunt diode D_2 and charge up C_1 with a DC voltage, which is then biases D_2 during the positive half-wave. The analysis demonstrates the importance of making use of high-quality inductors with low tolerances for the diode capacitance cancellation.

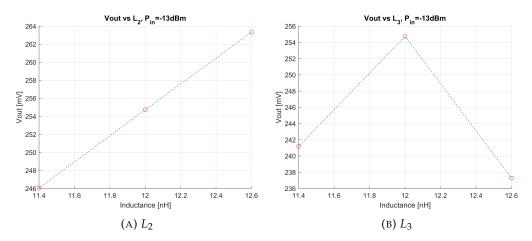


FIGURE 4.24: Plot illustrating how change in inductance due to tolerance for L_2 and L_3 can affect the output voltage.

4.3.5 Layout

The PCB layout for the top layer of the RF-EH design can be seen in Figure 4.25. The entire bottom layer is covered in copper. The entire PCB has an area of $80mm \times 54mm$. There are essentially three parts to the top layer.

Firstly, we have the IMN with its input microstrip line and then series resonator. The small pads are placed there so that the matching can be tuned post-manufacture. These pads act like open stubs when they are connected to the input line and add tiny amounts of capacitance to the matching. These allow us nullify inductances arising from inductor tolerances.

Secondly, we come to a crossroad, where we have the shunt-inductor L_2 and diode D_1 downwards, the series-inductor L_3 and -diode D_2 to the right, and an open stub going upwards. The stub is used to add more capacitance to help with the matching, and comes with some tuning pads as well. The long thin line in the shunt is a shorted stub that adds appropriate amounts of inductance where the shunt-inductor could not.

Thirdly, we have the capacitor C_2 that shunts high frequencies while quickly charging up DC, and then a output matching line which tapers to a configuration for the HSLS IC. At the end we also have some space next to the leftmost square pad for the slightly more capacitive, shunted capacitor C_3 that can store more energy. It is kept close to the IC to minimize noise. The thin trace going underneath the configuration connects to the external resistor used to set the threshold voltage.

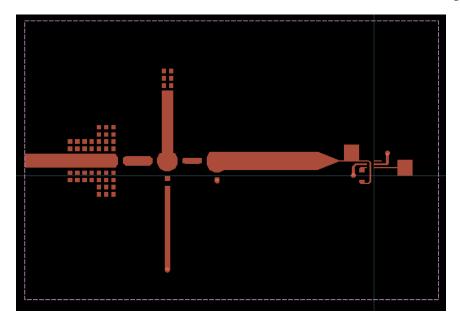
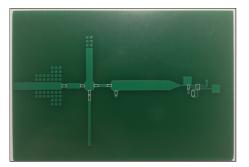


FIGURE 4.25: Final layout of our RF-EH top layer.

Resulting PCB

The manufactured PCB without and with soldered components is shown in Figure 4.26a and Figure 4.26b, respectively. Due to human error in the ordering process of the PCB it ended up being completely covered in thin, protective resin. This was not too much of an issue as it could simply be scraped away to get to the traces for soldering. On the right on the soldered PCB one can see the general resistor used to represent the HSLS during the charging phase of the RF-EH.



(A) Freshly manufactured



(B) With soldered components

FIGURE 4.26: The manufactured FR-4 PCB.

4.3.6 Post-manufacture Tuning

The input reflection for the manufactured RF-EH was shifted slightly down in frequency as can be seen in Figure 4.27. For 1850MHz it changed from -17.5 dB to -1.1 dB.

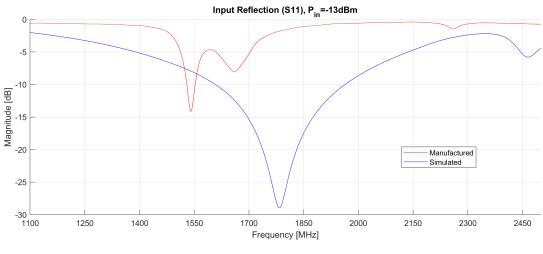


FIGURE 4.27: S11 comparison between simulated- and manufactured RF-EH.

Through further inspection we found that the input impedance for 1850 MHz was $Z_{in} = (13.96 + j122)\Omega$, suggesting that the matching was quite inductive. It was discovered that the tuning pads were too small for them to have a noticeable improvement on the matching. At the same time we needed more resistance on the input, meaning the input microstrip line had to become thinner and longer. The input tuning pads and input line were therefore scraped away to better allow for experimental tuning with conductive tape, but due to the limited area there was not enough space for a proper input matching line.

For the final tuning solution we ended up adding a 2.7 pF capacitor in series at the input and then a patch resonator, as can be seen in Figure 4.28. The capacitor lowers the inductance considerably, and the patch shifts the resonance to a higher frequency.

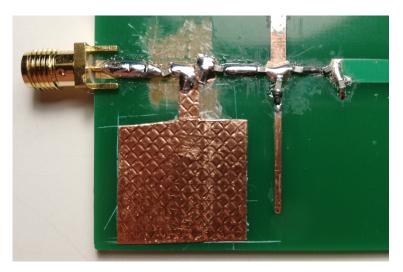


FIGURE 4.28: The manufactured RF-EH modified so that the matching is better for 1850 MHz.

The input reflection for the tuned RF-EH is shown in Figure 4.29, and resonates deeply at 1765 MHz. Compared to the simulation the BW is much narrower how-ever, and so for 1850 MHz we have -7.94 dB.

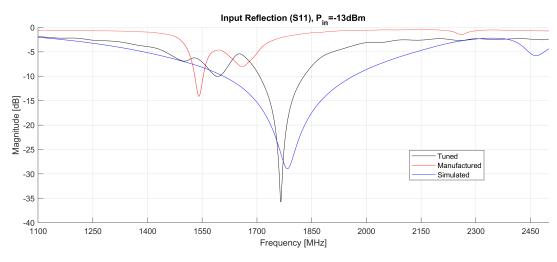


FIGURE 4.29: S11 comparison between simulated-, manufactured-, and tuned RF-EH.

Chapter 5

Methodology

5.1 Equipment and Input Power

S-parameter measurements were done using a Rohde & Schwarz ZVA 50 Vector Network Analyzer (VNA), and input AC signals were supplied by the APSIN20G signal generator. Voltages were measured with a Fluke multimeter.

An input power of 0 dBm and -13 dBm will be investigated, the latter having been arrived to as a important value in our requirements, and the former acting as a comparison value for us to observe how the input power affects the RF-EH performance.

5.2 Measuring Output Voltage

It must be clarified that 1 $M\Omega$ multimeter probes were used to measure the output DC voltage, meaning the load would appear to be approximately $R_1 = 872 \ k\Omega$ due to the probes being in parallel with the load resistor. Our method in finding the voltage for 6.8 $M\Omega$ was through calculation, which can be done if the output voltage has been measured for two different load values. For the second load value we simply switched out the 6.8 $M\Omega$ resistor with a 470 $k\Omega$ resistor, which approximates to $R_2 = 320 \ k\Omega$ with probes in parallel.

The calculation method works as follows. The output resistance R_o will together with the output voltage V_{out} determine the voltage across the load V_L . As we do not know R_o or V_o , we can solve one by eliminating the other. For the first load R_1 we have some voltage V_1 going across it, which can be found through voltage division given in Eq. 5.1. We get a similar equation for our second load, where we have R_2 and V_2 instead.

$$V_1 = V_{out} \times \frac{R_1}{(R_1 + R_o)}$$
 [V] (5.1)

If we then solve for V_{out} then put them together, we end up with Eq. 5.2, which lets us calculate R_o . Note that in this equation it is required that $V_2 > V_1$, as the output resistance can not be negative or exactly zero. With R_o calculated we can calculate V_{out} with Eq. 5.1.

$$R_o = R_1 R_2 \times \frac{(V_2 - V_1)}{(R_2 V_1 - R_1 V_2)}$$
 [Ω] (5.2)

And finally, if we imagine the load to be R_3 , we can estimate its voltage V_3 with Eq. 5.3 and the calculated values for R_o and V_{out} .

$$V_3 = V_{out} \times \frac{R_3}{(R_3 + R_o)}$$
 [V] (5.3)

Chapter 6

Results & Discussion

6.1 Input Reflection

In Figure 6.1a and Figure 6.1b is a S11 comparison between the simulated- and tuned RF-EH with both $R_L = 6.8 \ M\Omega$ and 470 $k\Omega$ for $P_{in} = 0$ dBm and $P_{in} = -13$ dBm, respectively.

The simulated input reflection is not affected by the output load resistance, whereas in reality the load has a significant influence on the matching. A lower load resistance indicates a upwards shift in the matched frequency, and for the jump down to 470 $k\Omega$ the matching for $f_r = 1850$ MHz is improved on average by around 4 dB, from -8.8 dB to -12.8 dB.

The input power P_{in} acts upon the real RF-EH in the opposite manner that the simulation does. The simulation matching is a lot more sensitive to P_{in} , rapidly shifting upwards in frequency as input power is lowered. For the tuned RF-EH we see a slight shift, but not in such a dramatic fashion as the simulation. One likely cause for this discrepancy between simulation and reality is the diode model used, as it was based on 0 dBm S-parameter measurements only. This combined with the fact that the diodes are non-linear and that ambient RF is unpredictable, authenticates any previous notions about the importance of accurate modelling when designing a stable and reliable harvester.

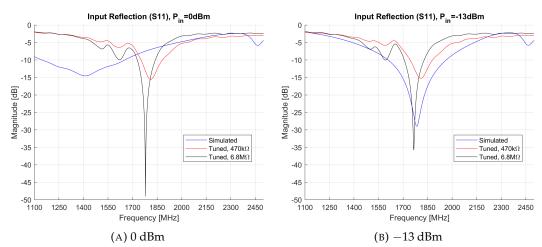


FIGURE 6.1: S11 comparison between simulated- and tuned RF-EH for $R_L = 6.8 M\Omega$ and 470 $k\Omega$

6.2 Impedance and Q-Factor

Figure 6.2a and Figure 6.2b demonstrates the difference in the impedance of the simulated- and tuned RF-EH. As a complement to the discussion, the Q-factor calculated from resistance and reactance is shown in Figure 6.3a and Figure 6.3b.

The peaks are resonant harmonics caused by parasitics in the circuitry, and alternates between very small to large impedance due to the reactance varying between a capacitive and inductive state. Looking at the Q-factor plots, the resonances are spaced by around 55 ± 5 MHz, and the spacing does not change particularly based on the input power. An increase in input power slightly shifts the resonances up in frequency by a few MHz, seemingly proportional to how the input reflection is shifted with power.

On the assumption that the diodes are influenced the most by the input power due to their non-linearity, and hence their parasitics change with input power, it seems reasonable that their parasitics are not the main culprit behind the resonances, and rather determined by the microstrip or the other lumped components.

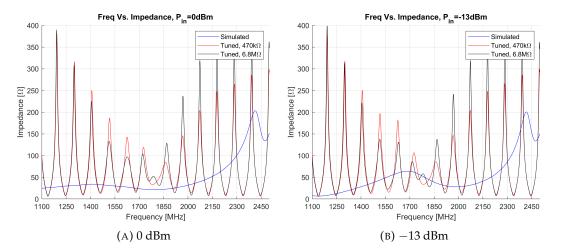


FIGURE 6.2: A comparison between the impedance of simulated- and tuned RF-EH for $R_L = 6.8 M\Omega$ and 470 $k\Omega$

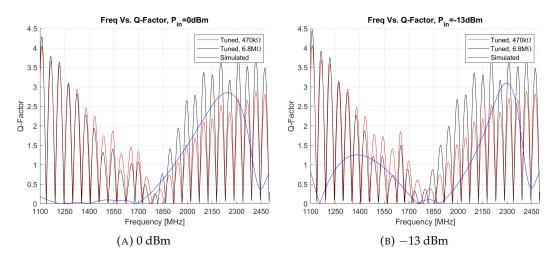


FIGURE 6.3: Graphs of Q-factor with simulated- and tuned RF-EH for $R_L = 6.8 M\Omega$ and $470 k\Omega$

6.3 DC Voltage

6.3.1 Frequency

The measured output voltages V_1 and V_2 for $R_1 = 872 \ k\Omega$ and $R_2 = 320 \ k\Omega$ are on display in Figure 6.4. Although a higher load gives a noticeable increase in voltage for 0 dBm, the same can not be said for -13 dBm. Comparing the graph against the input reflections from previously proves that a good match is not all that matters in terms of voltage output, as in that case we should have gotten the peak at around 1770 MHz. For high voltages the resonance is equally important.

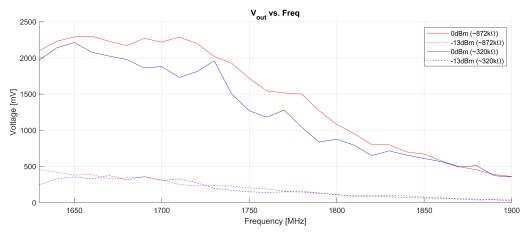


FIGURE 6.4: Raw voltage measurements based on frequency and input power.

6.3.2 Calculated Output Resistance

By incorporating the methodology elaborated on in Section 5.2, we end up with the calculated output resistance R_o shown in Figure 6.5. Any negative data points are ignored. Through the use of a 6th polynomial fitting curve of the points, we end up with two smooth curves that better shows the trends. Based on these curves at 1850 MHz, the average R_o resides from around 125- to 175 $k\Omega$, and would have been a good pick if efficiency was a greater concern.

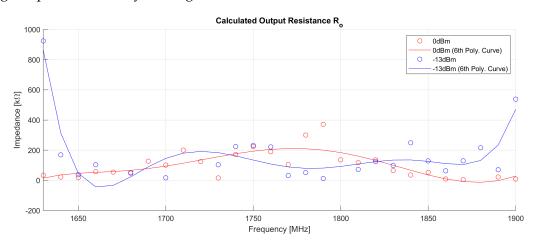


FIGURE 6.5: The calculated output resistance based on voltage measurements for two different loads.

6.3.3 Calculated Output Voltage

With the output resistance we calculate the output voltage for a 6.8 $M\Omega$ load, we end up with the data points in Figure 6.6, which are then smoothed with a 6th polynomial fitting curve as with the output resistance. The trend tells us that more can be gained with frequencies that have better matching and resonances. Clearly a high impedance load has a greater impact on the output voltage when the input power is not that small e.g 0 dBm. Considering most of the literature is concerned about maximizing the efficiency, it might be more worthwhile to use smaller loads when one expects to be dealing with low input powers like -13 dBm. In addition, a higher efficiency will more quickly charge up the power storage.

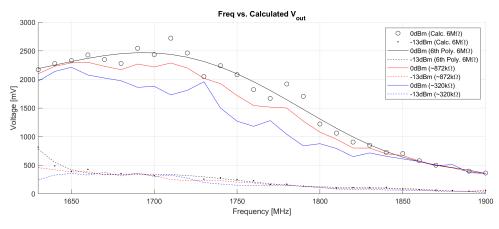


FIGURE 6.6: Calculated voltage for a 6.8 $M\Omega$ load based on frequency and input power.

6.3.4 Input Power and Efficiency

The effect input power has on the output voltage and efficiency for 1850 MHz can be seen in Figure 6.7. Included is also voltages from the simulation, which is clamped at 1.85 V. This is a fault of the simulation, and would in reality continue rising exponentially, as can be seen happening with our measurements. According to the measurements, we need roughly an input power of 6 dBm for our prototype to produce 2 V, meaning we are 19 dBm short from our requirement of -13 dBm, for which we get 107 mV. Comparatively, -13 dBm gave us 254 mV in simulations.

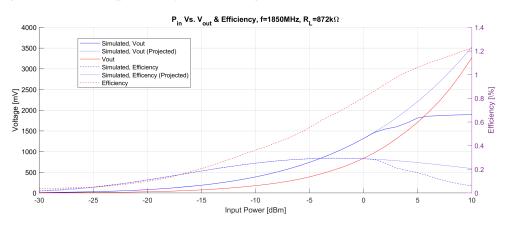


FIGURE 6.7: Input power and efficiency for 872 $k\Omega$.

6.3.5 Comparison with literature

In Table 6.1 our result is compared against the literature researched in Chapter 2. Our prototype provides as much voltage as [13], but due to their design using a smaller load, their efficiency is significantly better. Looking back at the best design that is not ASIC, the authors of [16] managed to get good voltage with quite low power. They do however mention the difficulty in getting the matching right due to mismatch between model and circuit, and therefore they did several iterations to get it right.

The key take-away here is that the combination of no power supply, low input power, lumped components and high frequency signals is a difficult mix to get right, as all the negatives that they bring accumulates and degrades performance considerably. By not having a power supply we are quite limited in what type of ICs we can use, and the low input power is prone to noise and difficult to efficiently rectify. The lumped components combined with high frequency signals leads to and increasing complexity in both simulations and reality due to parasitics.

All things considered it is challenging to get the design to perform as desired without doing multiple prototype iterations, and even then it will be affected by randomness like components tolerances and the substrate dielectric. Due to these variables, it is likely required to manually tune a reliable design in post for most cases, and for that reason the better route in the long run is to develop the design in the form of a custom IC.

Ref. (year)	Design	Technology	Frequency (MHz)	P _{in} for 2V (dBm)	Efficiency @ P _{in} (%)	Load (Ω)
[8] (2018)	Single-diode	HSMS-2860	700	12	72	0.3k
[12] (2020)	Shunted single-diode	Avago HSMS-286	2100	11	72	1.7k
[22] (2015)	Single-diode	HSMS-2862 (SOT-23)	2450	9	60	0.9k
[23] (2020)	Voltage doubler	HSMS-2850 (SOT-323)	900	8	40	2k
[9] (2020)	Voltage doubler	Skyworks SMS7630	1500, 1800, 2100	7	53-57	1.6k
This work	Voltage doubler	Skyworks SMS7630	1850	6	0.8	872k
[13] (2020)	Voltage doubler	Skyworks SMS7630	800	6	72	1.4k
[15] (2017)	ASIC	65 nm CMOS	900	-9.5	32.5	147k
[24] (2015)	ASIC	180 nm CMOS	900	-12	44.1	144k
[<mark>16</mark>] (2011)	Single-diode or voltage doubler, ultra-low- voltage charge-pump IC	Agilent HSMS-2850, Skyworks SMS-7630	2450	-15.2, -15.6	2.71	20k
[20] (2020)	ASIC	130 nm CMOS	915	-17	22	1M
[19] (2020)	ASIC	180 nm CMOS	902	-18	23.5	1M
[21] (2019)	ASIC	130 nm CMOS	896	-18.5	30	1M

TABLE 6.1: Comparison between our prototype and literature designs, sorted by minimum input power for 2 V.

6.4 Antenna and RF-EH Test

As a final test we wanted to see how the RF-EH would perform at our location using the patch antenna. Before doing this, spectrum measurements had to be made so that we roughly knew the amount of power we were dealing with. Compared to previous spectrum measurements, the amount of power at 1850 MHz was so low this time that there was no point in testing it. This can be seen in Figure 6.8, where we see how the power measurements have changed over time from best case -13 to -52 dBm. Since these measurements were not done across many days however, it might just have been quite bad on the measurement days in particular. The data for the patch antenna in the Fall of 2019 is an estimation made by taking the difference for Fall of 2020 and adding it to the dipole measurement of 2019.

This highlights the problem that comes with relying on an unreliable source of power that can change over time. For telecommunication antennas in particular the changes can be drastic due to the rapid innovation of mobile consumer devices in modern society. In contrast, countries like USA have large, static TV towers that broadcast all the time, and are therefore much more reliable as a power source. Whether these towers can be considered ambient or not could be argued against, but in most cases one would not have the ability to control its transmitting capabilities.

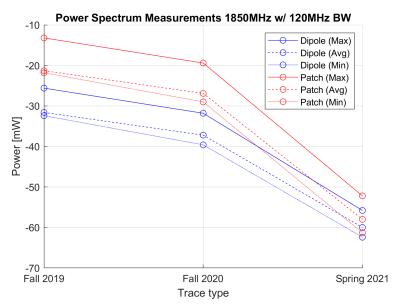


FIGURE 6.8: Graph demonstrating how the amount of power picked up by our antenna for 1850 MHz has changed considerably over time.

Chapter 7

Conclusion

In this thesis we have elaborated on the process of designing an antenna and a villard voltage doubler RF-EH that together form a energy harvester that can be used to power a ambient backscatter system that utilizes a low-power microcontroller. The requirement for the RF-EH was that it could provide 2 V when given a 1850 MHz input AC signal of -13 dBm, an input power requirement which we arrived to based on spectrum measurements performed at a fixed location.

Voltage measurements of the RF-EH design exposed that at most 107 mV could be provided with an input power of -13 dBm, and that the signal would need to be atleast 6 dBm for the RF-EH to provide a DC voltage of 2 V. It was simulated that -13 dBm would give us 254 mV, and so it was concluded that the primary cause for the significant drop in voltage were inaccurate component models, which lead to faulty matching and thus loss of power due to a increase in input reflection.

Further, there is the question whether a PCB design is even feasible or not. As lumped components are more prone to parasitics and tolerances, the final verdict is that it can be, as literature shows its possible, but it requires multiple iterations and careful tuning, and therefore custom IC design is likely a better choice.

Over the span of two years, executed spectrum measurements have demonstrated the chosen RF band source to be unreliable, as it ranged between -13 dBm and -52 dBm for the best case. More regular measurements should have been done to better investigate this, but it showcased the biggest drawback that comes from relying on ambient RF as a power source; that it can rapidly change over time.

7.1 Future Work

The voltage provided by the RF-EH can be pushed further through the use of a ultralow voltage charge pump and is more suited for increasing voltage than a rectifier, the latter whose primary purpose is to convert AC to DC. Research indicates that a few hundred millivolts are required to power such charge pumps available as IC, and so it is important to make sure that the rectifier in the RF-EH can provide enough on its own.

The components to be used in the design should be investigated and measured beforehand independently. The data can then be used to develop more accurate models so that minimal amounts of design iterations and tuning are required for the harvester to perform as expected.

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Appendix A

Schematics

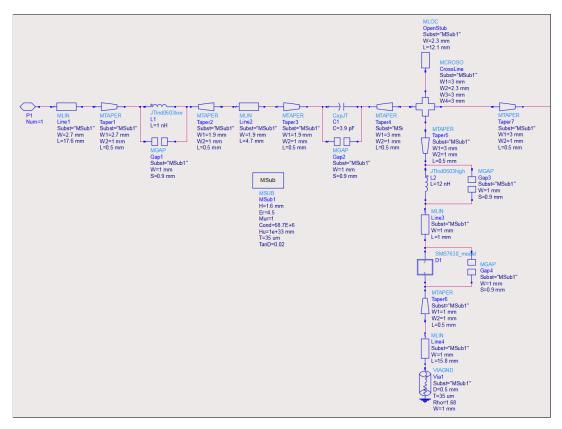


FIGURE A.1: Final design schematic, pt. 1 of 2.

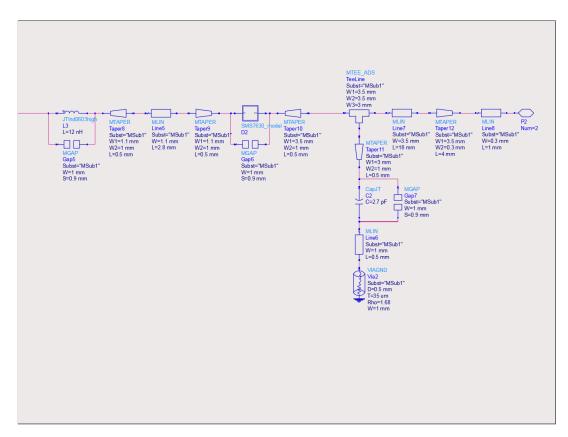


FIGURE A.2: Final design schematic, pt. 2 of 2.



