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A universal automatic and self-powered gate driver power supply for normally-ON SiC JFETs

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Abstract

Normally-ON silicon carbide junction-field-effect transistors have a simple design and exhibit advantageous performance in terms of losses, elevated junction temperatures and high switching frequencies. However, under a loss of power to their gate, normally-ON junction-field-effect transistors are subject to a shoot-through situation, which might be severe for their survivability. This paper presents a universal concept for an automatic and self-powered gate driver power supply circuit for normally-ON silicon carbide junction-field-effect transistors employed in high input-impedance circuits. The power to the gate is supplied during start-up and steady-state operations through a mutually coupled inductor with the high input impedance inductor and by employing a typical low-voltage, power supply circuit. The performance of the proposed automatic and self-powered gate driver was evaluated on a DC/DC boost converter rated at 6 kW, as well as in a low-voltage solid-state DC circuit breaker. From experiments it is shown that using the proposed circuit, the start-up process requires approximately 350 μs, while the steady-state switching process of the junction-field-effect transistor during steady-state is also shown. Using the proposed circuit in a low-voltage solid-state DC breaker, a fault current of 68 A is cleared within 155 μs.

1 | INTRODUCTION

Silicon Carbide SiC power switching devices exhibit lower power losses, enable utilisation of high switching frequencies and can operate at higher temperatures (> 200°C) compared to state-of-the-art silicon (Si) counterparts [1–13]. Today, SiC power metal-oxide-semiconductor field-effect transistors (MOSFETs) [14–16] and the SiC junction-field-effect transistors (JFETs) [17–21] are available with voltage ratings in the range of 650–1700 V. SiC JFETs can be designed as either normally-OFF or normally-ON switches. From a converter performance point-of-view, the normally-ON SiC JFET exhibits a lower specific on-state resistance that results in lower conduction losses and a significantly higher saturation current [10, 22]. Moreover, normally-ON JFETs have a lower temperature coefficient compared to normally-OFF counterparts. From the driving perspective, normally-OFF SiC JFETs require a significant gate current for if on-state losses need to be optimised. On the other hand, normally-ON JFET has a voltage-controlled gate. Applications such as current-source and impedance-source inverters [23–25], high-power modular multilevel converters [26] and DC circuit breakers can benefit from using normally-ON SiC JFETs [27]. However, the normally-ON characteristics of SiC JFETs impose severe driving challenges when employed in power converters. In particular, the greatest challenge of driving normally-ON SiC JFETs is associated with ensuring a safe turn-OFF of the device not only during switching at steady-state operation, but also at the start-up process [28]. Thus, a sufficiently negative voltage (more negative than the pinch-off voltage, V_{pi}) must always be present and supplied to the gate driver.

Various circuit concepts to deal with the "Normally-ON problem" have been developed and applied either at gate-driver [29–31] or converter level [32–34]. However, these concepts require an external power supply for energising the various circuit components. The need for external power supplies has been eliminated in the self-powered gate driver for normally-ON SiC JFETs shown in [28]. This circuit concept is able to energise the gate-drive circuit without the need of an external

power supply, both at start-up phase of the converter and at steady-state operation. Nevertheless, this concept can only be activated in low-input impedance circuits. This is due to the fact that the self-powered gate driver utilises the energy from the shoot-through current during the start-up phase. If the input impedance is high, the anticipated energy of the shoot-through current might not be sufficient to properly activate the circuit. For steady-state operation, the required power to the gate driver is supplied by the blocking voltage of the JFET via a low-power DC/DC forward converter. A similar circuit concept for normally-ON SiC JFETs has been proposed in [35], but it also needs an external power supply for steady-state operation.

Normally-ON SiC JFET can also be perfect device candidates for solid-state DC breakers compared to other SiC active devices. One main reason for this is their lower expected temperature rise compared to SiC MOSFETs under a short-circuit condition [36]. In addition to this, the normally-ON nature of JFETs eliminates the need for continuously supplying a positive gate voltage (i.e. as in MOSFETs) or a substantially high base current (i.e. as in SiC bipolar junction transistors (BJTs)) during current conduction [13]. In particular, normally-ON SiC JFETs can conduct the load current without biasing the gate-source junction, unless further reduction of conduction losses is targeted by applying a low positive voltage. The absence of gate-oxide layer in normally-ON SiC JFET also induces advantages compared to SiC MOSFETs under repetitive short-circuits when operating in solid-state DC breakers [37].

Under a fault condition, the voltage drop across the normally-ON SiC JFET can be utilised and converted to a sufficiently negative gate voltage in order to turn-OFF the device [27]. However, this type of self-triggered JFET-based solid-state DC breaker requires a complicated circuitry and a sufficiently high voltage drop for proper activation, which might cause excessive heat dissipation in the JFET die. Similar circuit concepts have also been presented for bipolar-injection field effect-transistors (BIFETs) [38], which also exhibit similar disadvantages.

This paper presents a generic circuit concept of a universal automatic and self-powered (UASP) gate driver supply for normally-ON SiC JFETs employed in high-input-impedance circuits. The proposed circuit concept utilises the voltage drop across the high input-impedance and supply a sufficiently negative voltage to control the gate. By using the proposed solution, the need for connecting additional circuit components across the SiC JFET is eliminated. The performance and applicability of the proposed automatic supply concept is demonstrated in a switch-mode power converter during start-up and steady-state operations, as well as in a low-voltage solid-state DC breaker employing normally-ON SiC JFETs.

The paper is organised as follows. Section 2 shows the operating principle of the proposed circuit, while the design process and dimensioning of the circuit is presented in Section 3. The experimental investigation of the UASP circuit operated in a DC/DC boost converter is found in Section 4. Section 5 presents both simulations and experimental results of the UASP circuit employed in a low-voltage solid-state DC breaker. Last but not least, conclusions are given in Section 6.

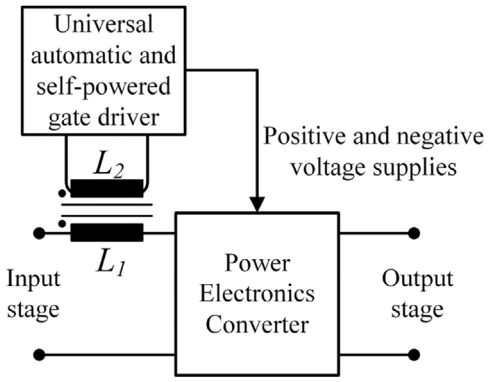

FIGURE 1 Block diagram of the operating principle of the proposed UASP gate driver in a switch-mode power converter

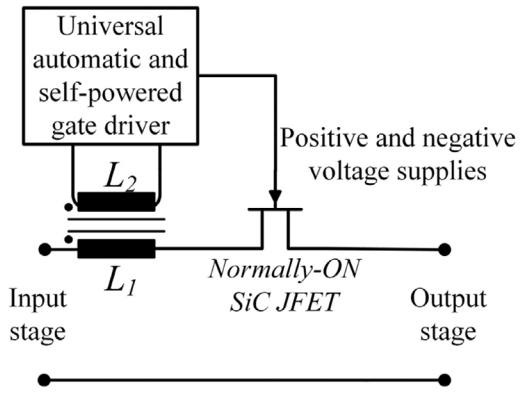

FIGURE 2 Block diagram of the operating principle of the proposed UASP gate driver in a solid-state DC breaker

2 | OPERATING PRINCIPLE

The operating principle of the proposed circuit is based on utilising the voltage drop across the high input-impedance and convert it to a sufficiently negative voltage suitable to control the gate. Figure 1 shows a block diagram of the proposed UASP circuit concept operating in a switch-mode converter, where the high input-impedance, L_1 is also depicted. In addition to this, the proposed circuit can also be employed to control the gate voltage in solid-state DC breakers utilising normally-ON SiC JFETs, as shown in Figure 2. For the latter case, the high impedance is basically the current-limiting inductor that is needed to limit the rate of rise of fault current, as well as the peak value of the fault current. In both applications, a second inductor, L_2, is magnetically coupled with L_1 using a magnetic core and by employing a proper circuitry in the UASP circuit (e.g. a positive and a negative voltage regulators) the desired floated voltages can be generated and supplied to the gate.

2.1 | UASP in switch-mode converters

In order to present the operating principle of the proposed UASP gate driver in a switch-mode converter, a non-isolated DC/DC boost converter is considered (Figure 3). L_1 operates

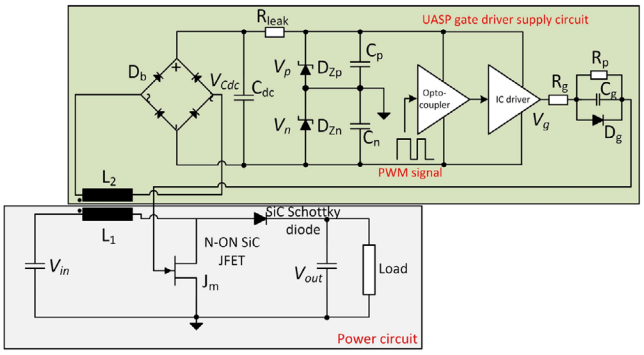

FIGURE 3 Circuit diagram of the DC/DC boost converter with the UASP gate driver

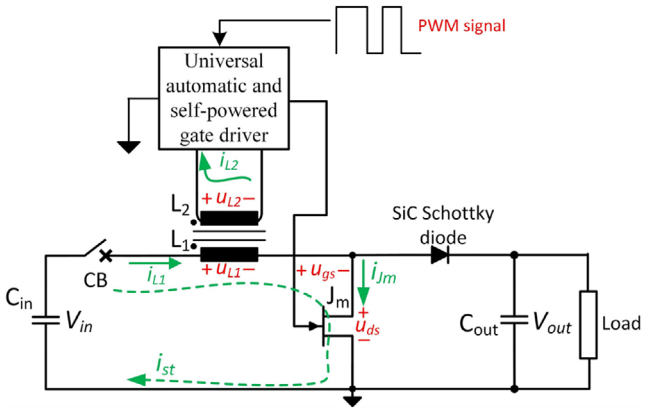

FIGURE 4 Path of the shoot-through current during the start-up process of the DC/DC boost converter

as the main inductor of the DC/DC converter and L_2 is the auxiliary inductor, which is directly connected with a low-voltage diode rectifier, D_b. The direct output voltage of D_b, $u_{C_{DC}}$, is fed to a pair of Zener diodes, D_{Z_p} and D_{Z_n} that supply the positive and negative voltage to the gate. Any potential high current through the Zener diodes is limited by a series-connected resistor, R_{leak}. This is basically one possible way to realise a power supply for the gate driver. A plethora of various low-voltage source concepts might also be employed in order to convert the voltage across L_2 to suitable voltage levels for the gate driver. To complete the gate driver design, an optocoupler for signal isolation and a totem-pole integrated-circuit driver (IC-driver) are also employed. Last but not least, for controlling the switching speed of the JFET and preventing breakdown of the gate, a series-connected gate resistor R_g and a diode-resistor-capacitor ($D_gR_pC_g$) parallel network are connected on the output of the IC-driver [39].

A favourable characteristic of the proposed UASP circuit is the fact that the shoot-through current is only limited by means of L_1, and thus, the need for a start-up resistor to limit the shoot-through current is eliminated. However, the inductance of L_1 must be properly chosen in order to set the peak value of the shoot-through current in such a way that it will not stress thermally the SiC JFET and that will not saturate the channel of the JFET either. Along with this, the range of the input voltages of the DC/DC boost converter must also be carefully set for ensuring a successful start-up procedure. Additionally, in steady-state operation of the converter, the design of the inductance L_1 must take into account the switching frequency of the SiC-JFET, as well as the input voltage and the load current. Then, the inductance L_2 will be defined accordingly, as mentioned above. It should be noted that a high switching frequency is anticipated due to the utilisation of SiC power semiconductor device and thus, L_1 and L_2 can be low resulting in a high power density DC/DC converter design. However, at elevated frequencies, the power losses associated with the mutually coupled inductors and more importantly the core losses, will also increase. In addition to this, operation at elevated switching frequencies imposes the need for more powerful gate drivers that will be able to supply sufficient gate current peaks for fast switching and to also ensure a stable gate voltage supply.

During the start-up process of the converter and under the assumption that there is no power supplied to the gate of the normally-ON SiC JFET, J_m, the JFET is kept in the ON-state. This means, that a shoot-through current, i_{st}, is flowing through L_1 and J_m as shown with the dashed line in Figure 4, while Figure 5 illustrates the theoretical performance during the start-up process. When the start-up process is initiated, it is assumed that the input capacitor C_{in} is fully charged at the input voltage V_{in}. Moreover, it must be noted that the DC/DC converter is energised when the circuit breaker, CB, shown in Figure 4 closes, and thus, C_{in} feeds the circuit.

As soon as the CB is closed and since there is no power to the gate, J_m is subjected to a short-circuit condition and the input voltage, V_{in} appears across L_1 and J_m. The derivative of the shoot-through current is determined by the values of L_1 and V_{in}. A graphical representation of the current, i_{J_m} flowing through J_m and current i_{L_1} through L_1 are shown in the first and second waveforms in Figure 5. From this figure, it is clear that two current peaks are observed on both of i_{J_m} and i_{L_1} waveforms. The different time intervals which can be observed in Figure 5 are analySed as follows.

- t_0–t_1: The first current peak in the interval t_0–t_1 is due to the charging current of the DC-link capacitor of the auxiliary circuit, C_{DC} (Figure 3). During this time interval, the voltage across L_1, u_{L_1}, is rising and has a maximum value of approximately V_{in}. In particular, the main part of V_{in} appears across L_1, while the voltage across J_m is significantly lower due to its low ON-state resistance (fourth waveform in Figure 5). For simplicity, however, it is assumed that V_{in} completely appears across L_1.
- t_1–t_2: When u_{CDC} reaches its steady-state value at $t = t_1$, the current in the auxiliary winding, L_2 becomes zero. However, a low leakage current i_{L_2} still flows through L_2 in order to compensate for the losses in the circuit (e.g. leakage current in C_{DC} and Zener diodes). The performance of $u_{C_{DC}}$ is shown in the bottom waveform in Figure 5.
- t_2–t_3: At the time instant t_2, the negative supply voltage of the optocoupler and IC-driver, u_{gs}, is sufficiently low and provided that the propagation of the pulse width

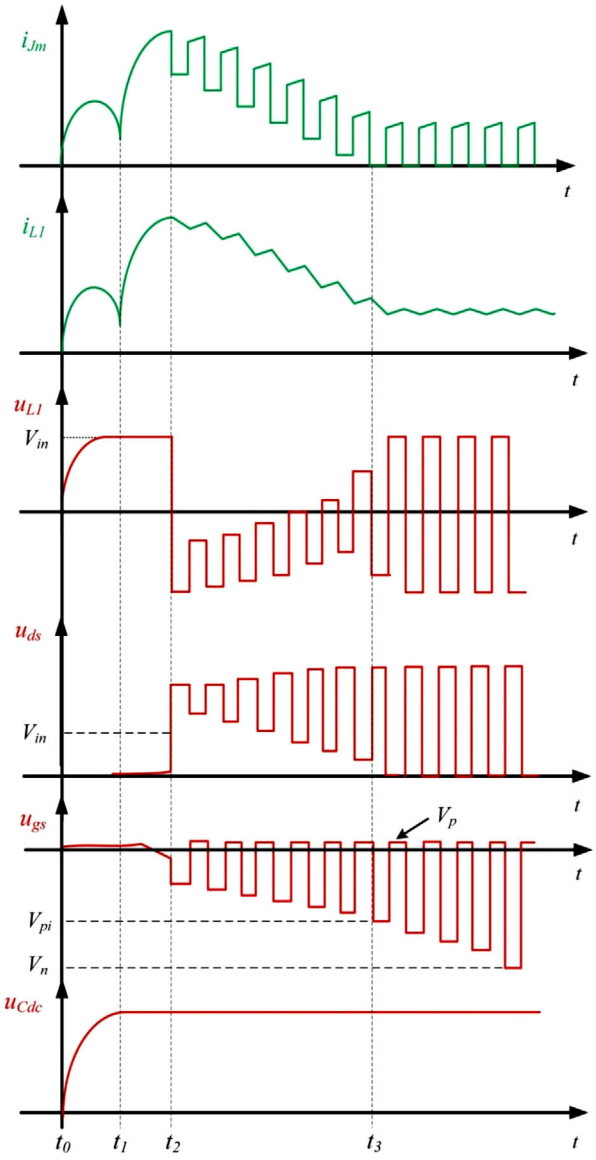

FIGURE 5 Theoretical performance of the UASP circuit employed in the DC/DC boost converter

modulation (PWM) signal to the optocoupler starts at $t = t_0$, J_m is switching. However, J_m is operating in the active region until u_{gs} becomes more negative that the pinch-off voltage of J_m, V_{pi}. During this operating phase the drain-source voltage, u_{ds}, is switching between a high and a low positive voltage level and the SiC JFET might be overheated, unless a proper dimensioning of the UASP and converter is made. As soon as u_{gs} exceeds V_{pi} at $t = t_3$, the SiC JFET is switching normally in the saturation region. Additionally, the voltage across the primary winding of the coupled inductors, u_{L_1} becomes negative and i_{L_1} starts decreasing. This is due to the fact that J_m is turned-OFF (operation in active region) and a high blocking voltage appears across the device. Furthermore, the output voltage of the DC/DC boost converter, V_{out}, equals the envelope of the switching waveform of u_{ds}. Thus, considering that $u_{L_1} = V_{in} - V_{out}$ and that $V_{out} > V_{in}$, a negative voltage appears across L_1. After t_2, u_{L_1} starts to switch between a high negative and a low negative voltage level until $u_{gs} < V_{pi}$.

- $t > t_3$: At $t = t_3$, u_{gs} becomes lower than V_{pi} and hence, the steady-state operation of the converter is reached.

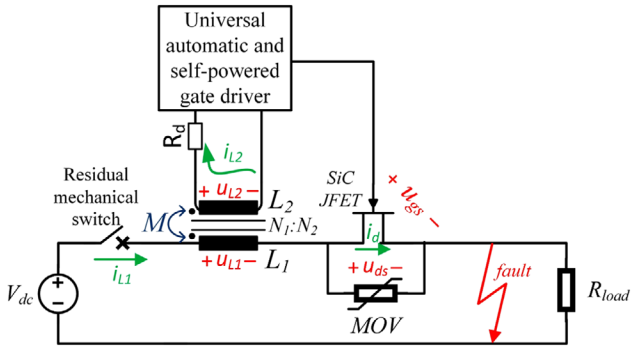

FIGURE 6 Block diagram of the UASP employed in a solid-state DC circuit breaker with a normally-ON SiC JFET

If the turns-ratio between L_1 and L_2 is N_1:N_2, the value of u_{L_2} equals $(N_2/N_1) \cdot u_{L_1}$. This voltage is supplied to the single-phase diode rectifier of the auxiliary circuit and dictates the value of $u_{C_{DC}}$. During steady-state operation of the DC/DC boost converter, the square-wave voltage of L_1 is continuously transformed to u_{L_2} and energises the UASP.

2.2 | UASP in low-voltage solid-state DC breakers

For presenting the operating principle of the UASP when it is employed in a solid-state DC circuit breaker with normally-ON SiC JFETs, the block diagram shown in Figure 6 will be considered. A vital component of a circuit breaker is the series-connected current-limiting inductor, L_1 that limits the rate of rise, as well as the peak value of the fault current. In addition to this, a metal-oxide varistor (MOV) is connected in parallel to the JFET for preventing destructive overvoltage conditions and breakdown. In order to ensure galvanic isolation in the fault line, a residual mechanical switch is also connected in series, which is able to open when the fault current is cleared by the SiC JFET.

Prior to the activation of the UASP, it is assumed that the solid-state circuit breaker conducts the direct line current, $i_{L_1} = I_{nom}$, which flows through L_1 and the normally-ON SiC JFET and it is supplied to the load. When a fault occurs (Figure 6), the line current increases rapidly because the voltage across L_1 equals the direct voltage of the grid, V_{DC}. Similarly to the case of applying the UASP in a switch-mode converter, the voltage across L_1 can be utilised by magnetically-coupling a second inductor L_2. This inductor L_2 feeds power to the UASP and, thus, the low-voltage and low-power circuit components contained in the UASP can be activated. However, in case of a solid-state breaker, there is no need for switching operation and it is only sufficient to supply a negative gate-source

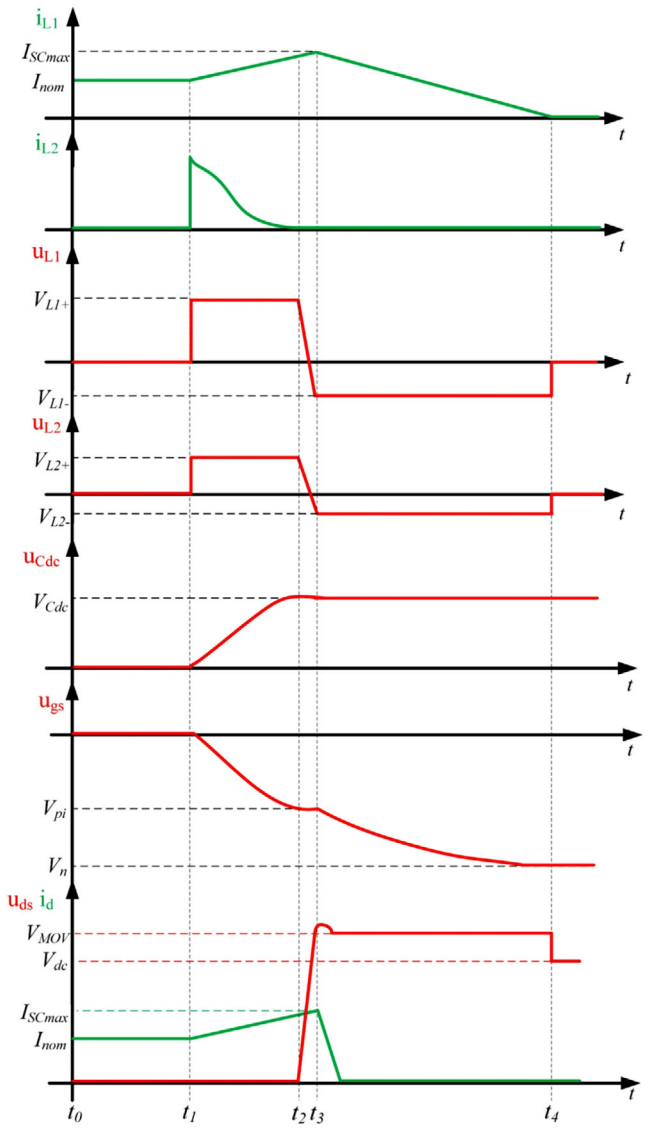

FIGURE 7 Theoretical performance of the UASP circuit employed in a solid-state DC breaker with a normally-ON SiC JFET

voltage for turning-OFF the SiC JFET. It should also be mentioned that a damping resistor, R_{d} connected in series with the second winding of the coupled inductors must be considered in order to dump potential voltage oscillations between L_2 and C_{DC} due to resonance.

The expected theoretical performance of the UASP when employed in a JFET-based solid-state breaker is illustrated in Figure 7. The operation of the UASP in different stages during a short-circuit clearance can be seen in that figure and it is analysed as follows.

- t_0–t_1: Prior to the time instant that the fault occurs ($t < t_1$), a direct line current flows, the voltage across L_1 is zero (i.e. the resistance of L_1 is assumed to be negligible) and the UASP is inactive.
- t_1–t_2: The fault occurs at $t = t_1$, and thus the line current starts rising with a slope determined by the values of V_{DC} and L_1 as shown in the first plot in Figure 7. Beyond t_1, the entire grid voltage V_{DC} appears across L_1 (i.e. $u_{L_1} = V_{L_{1+}} = V_{\mathrm{DC}}$) and a voltage, u_{L_2}, is also induced across L_2 with a magnitude that is determined by the turns ratio $N_1 : N_2$. In particular, $u_{L_2} = V_{L_{2+}} = (N_1/N_2) \cdot V_{\mathrm{DC}}$. Considering the same implementation of the power supply shown in Figure 3, the induced voltage on L_2 is rectified and appears across C_{DC}. As soon as, $u_{C_{\mathrm{DC}}}$ exceeds the sum of the breakdown voltages of the two Zener diodes, the negative and positive voltage supplies to the gate are regulated. However, by utilising the UASP in a JFET employed in a solid-state breaker, the need for a positive gate voltage supply could be omitted, unless conduction power losses are to be further reduced. On the other hand, if the optimisation of the conduction losses is of high design priority, an external positive voltage supply can be used.
- t_2–t_3: At $t = t_2$ and after the voltage across the C_{DC} has been stabilised at $V_{C_{\mathrm{DC}}}$, the u_{gs} becomes equal to the pinch-off voltage, V_{pi}, and therefore, the voltage across the JFET, u_{ds} starts rising as illustrated in the bottom waveform with red line in Figure 7.
- t_3–t_4: At $t = t_3$, the u_{ds} becomes higher than the clamping voltage of the MOV, V_{MOV} and therefore, the u_{gs} becomes less negative than the V_{pi} of the JFET and the SiC JFET starts to turn-OFF, as shown in the bottom plot in Figure 7. At this point, the line short-circuit current reaches the maximum value $I_{\mathrm{SC_{max}}}$, and it commutates from JFET to the MOV. Beyond the time instant t_3, the voltage across L_1 becomes negative and equals the difference between the clamping voltage of the MOV and the grid direct voltage, $u_{L_1} = V_{L_{1-}} = V_{\mathrm{DC}}$. This is also the reason that i_{L_1} starts decreasing at $t = t_3$. During the time period required for i_{L_1} to drop to zero, the voltage across the SiC JFET is clamped to the breakdown voltage of the MOV, V_{MOV}.
- $t > t_4$: The residual energy of the line is dissipated in the varistor and, thus, the line current becomes zero at the time instant t_4. Under the zero-current condition in the line, the residual mechanical switch can open and galvanically isolate the fault grid.

The solid-state breaker employing a normally-ON SiC JFET can be designed to be either self-controlled or externally-triggered. Self-controlled design means that the overall UASP design and dimensioning of the components are such, that when the fault current exceeds a predefined current threshold, the gate-source voltage becomes less negative than V_{pi}, and thus, the JFET turns-OFF. In the externally-triggered design, a positive gate voltage can be supplied by an external voltage source, while the negative gate voltage can be generated by the UASP. However, in this case, an external signal to the opto-coupler is needed for controlling the turn-OFF of the JFET. This is crucial when such a solid-state DC breaker operates in a multi-terminal grid, where selective protection might be required.

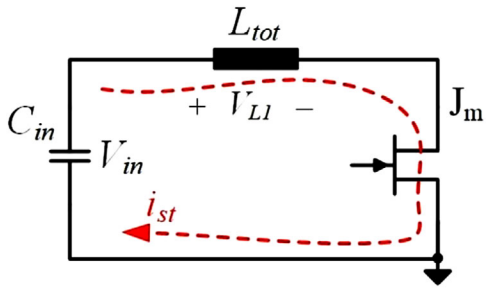

FIGURE 8 Schematic diagram showing the path for the shoot-through current during the start-up process

3 | DESIGN CONSIDERATIONS OF THE AUTOMATIC START-UP CIRCUIT

3.1 | High-input-impedance converter case

During the start-up process in the high-input-impedance converter, the design of UASP must be such that will not cause an extensive discharge of C_{in}. This means that along with the proper selection of L_1, C_{in} must also be selected with respect to the allowed input voltage drop during the activation of the UASP. If V_{in} drops to very low values or zero (fully discharging of C_{in}), the voltage across L_2 will also be either low or zero, and the UASP might not be activated.

A generic schematic diagram showing the path of the shoot-through current in a converter is shown in Figure 8. In this figure, L_{tot} is the total inductance seen from the shoot-through current (i.e. combination of the mutually coupled inductors L_1 and L_2). It is also assumed that the normally-ON SiC JFET J_m has an on-state resistance r_{on}. Based on Figure 8, Equation (1) gives the shoot-through current, i_{st}, as a function of the time t during the start-up phase.

$$\frac{d^2 i_{st}}{dt^2} + \frac{r_{on}}{L_{tot}} \cdot \frac{di_{st}}{dt} - \frac{1}{L_{tot} \cdot C_{in}} \cdot i_{st} = 0 \tag{1}$$

By solving this equation, the analytical expression for i_{st} can be derived. Thus, the energy released from C_{in} and dissipated in J_m can also be calculated using Equation (2). In this equation, I_{st} is the peak value of the shoot-through current and t_{su} is the time needed for J_m to start its switching process in a converter. Equation (3) gives the energy, ΔE_{in}, released from the capacitor during the start-up phase. In this equation, V_{in} and V'_{in} are the voltages across C_{in} before the start-up process is initialised and when J_m is turned-OFF, respectively.

$$E_{J_m} = I_{st}^2 \cdot r_{on} \cdot t_{su} \tag{2}$$

$$\Delta E_{in} = \frac{1}{2} \cdot C_{in} \cdot \left[V_{in}^2 - V_{in}'^2\right] \tag{3}$$

In case of dissipation of the entire energy stored in C_{in}, the voltage V'_{in} will drop to zero, which prevents the proper activation of the UASP. It is, therefore, necessary to set a criterion for the maximum allowed energy $\Delta E_{in,allowed}$ that can be released from C_{in}, as shown in Equation (4). This criterion dictates that $\Delta E_{in,allowed}$ must be significantly higher than the expected energy dissipation in the normally-ON SiC JFET. Thus, the anticipated voltage drop in C_{in} will also be kept low, which results in proper activation of the UASP.

$$\Delta E_{in,allowed} >> E_{J_m} \tag{4}$$

The criterion shown in Equation (4) can also be expressed in terms of the peak shoot-through current, I_{st}, as shown in Equation (5).

$$I_{st} < \sqrt{\frac{1}{2} \cdot \frac{C_{in} \cdot \left[V_{in}^2 - V_{in}'^2\right]}{r_{on} \cdot t_{su}}} \tag{5}$$

In the calculation of I_{st} the required turn-OFF time, t_{su}, must also be taken into account. However, the various combinations of I_{st} and t_{su} are, to some extent, directly associated with the value of L_{tot}. On the other hand, t_{su} is also related with the activation time of the auxiliary gate driver power supply. In particular, a specific time is also necessary in order the gate driver to supply an adequately negative gate voltage which turns-OFF J_m. This time is associated with the activation of the voltage regulators for V_p and V_n, optocoupler and IC-driver.

If the input voltage V_{in} drops more than the value set by the design limits, the voltage across the Zener diodes will not be adequately high to reverse-bias them. Consequently, the design of the coupled inductors L_1 and L_2 must also be done with respect to the range of the input voltage.

The voltage at which the C_{DC}, will be stabilised, $V_{C_{DC}}$, must be at least higher than the sum of the reverse breakdown voltages of the Zener diodes, for operating as voltage regulators. During the startup phase, $V_{C_{DC}}$ depends on the input voltage V_{in} and the turns-ratio of the coupled inductors, N_2/N_1. On the other hand, in case the UASP is employed in a boost converter operating in CCM, during steady-state operation, the voltage $V_{C_{DC}}$ depends on the input voltage, V_{in}, output voltage, V_{out}, and the duty ratio of the converter, D:

$$\begin{aligned} V_{C_{DC}} &= \frac{N_2}{N_1} \cdot [(2 \cdot D - 1) \cdot V_{in} + (1 - D) \cdot V_{out}] \\ &= \frac{N_2}{N_1} \cdot 2 \cdot D \cdot V_{in} \end{aligned} \tag{6}$$

The voltage given by Equation (6) must fulfil the following criterion:

$$V_{C_{DC}} > \left(V_n + V_p + V_{R_{leak}}\right) \tag{7}$$

where V_n and V_p are the absolute values of the negative and positive voltage supplied by the Zener regulators and $V_{R_{leak}}$ the voltage drop across R_{leak}.

3.2 | Solid-state DC circuit breaker case

The design of the UASP in the fault-clearing process in a SiC-JFET-based breaker faces different challenges. In particular, the grid voltages are usually higher than the input voltage of a DC/DC boost converter and hence, the discharge of C_{in} is not likely to occur under high input voltages V_{DC}. Therefore, the design of the proposed circuit will not take into consideration the input capacitance of the DC grid. On the other hand, the high grid voltage leads to the use of a different turns-ratio of the coupled inductors compared to the design of the UASP for the case of a switch-mode converter. The voltage in the UASP circuitry and particularly in C_{DC} should be kept at much lower levels than the grid voltage leading to the need for more turns in the primary inductor compared to the secondary side. In addition to that, the importance of the rate of rise of short-circuit current, $\mathrm{d}i_{L_1}/\mathrm{d}t$ should be emphasised since this may lead to high peak currents, which might heat up the JFET die excessively. The fault current rise in the circuit shown in Figure 6, is governed not only by the L_1, but also by the mutual inductance between L_1 and L_2, and it is given by the following equation.

$$\frac{\mathrm{d}i_{L_1}}{\mathrm{d}t} = \frac{\frac{V_{DC}}{L_1} - \frac{M}{L_1 \cdot L_2} u_{C_{DC}}}{1 - \frac{M^2}{L_1 \cdot L_2}} \tag{8}$$

where M is the mutual inductance given by:

$$M = c\sqrt{L_1 \cdot L_2} \tag{9}$$

In this expression, c is the coupling coefficient of the coupled inductors. Additionally, as mentioned above, a damping resistor, R_d must be considered. The possible oscillations between L_2 and C_{DC} should be damped and thus, the following criterion must be set.

$$R_d > 2\sqrt{\frac{L_2}{C_{DC}}} \tag{10}$$

Finally yet importantly, the charging time of the C_{DC}, t_{ch}, given by approximately $5 \cdot R_d C_{DC}$, should be set in such a way, that the peak short-circuit current will be within an acceptable limit. The t_{ch} indicates the start of the JFET turn-OFF and hence the peak short-circuit current. Therefore, the following criterion must be set.

$$t_{ch} < \frac{(I_{SC_{max}} - I_{nom})\left(1 - \frac{M^2}{L_1 \cdot L_2}\right)}{\frac{V_{DC}}{L_1} - \frac{M}{L_1 \cdot L_2} u_{C_{DC}}} \tag{11}$$

where, I_{nom} and $I_{SC_{max}}$ are the nominal line current and the maximum allowable fault current respectively. It should also be mentioned that the capacitor voltage when the last is fully charged, $V_{C_{DC}}$ will be lower than $N2/N1 \cdot V_{DC}$, due to the voltage drop in the damping resistor R_d. At the same time, Equation (7) must hold true. Therefore, the choice of C_{DC}, R_d and L_2 which will set the $N1/N2$ are of great importance and they must be defined precisely.

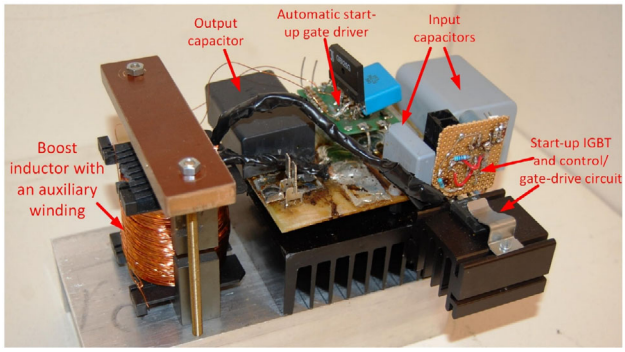

FIGURE 9 Photograph of the experimental DC/DC boost converter prototype employing the automatic start-up circuit

4 | EXPERIMENTAL RESULTS FOR OPERATION IN A SWITCH-MODE POWER CONVERTER

The performance of the proposed UASP power supply for normally-ON SiC JFET operating in switch-mode converters has been validated experimentally using a DC/DC boost converter rated at 6 kW. The lab prototype was designed using a 1200-V SiC JFET with an ON-state resistance of 45 mΩ at room temperature, a pinch-off voltage of -5 V and a chip area of approximately 9 mm^2. A photograph of the experimental DC/DC boost converter prototype is shown in Figure 9.

In order to emulate the start-up process of the circuit, a circuit activation switch employing a silicon IGBT (IXYS IXA55I1200HJ) was connected between the pre-charged C_{in} and L_1. However, in a realistic converter, the start-up switch might consist of a relay or a mechanical switch. In this paper, however, the main target is to demonstrate the operating principle of the proposed universal automatic and self-powered circuit, and thus, the investigations are not expanded to the design and performance of the circuit activation switch.

The design of the coupled inductors, L_1 and L_2, is very crucial for the proper operation of the uasp circuit. Assuming the range of the input voltage to be 50–150 V, the steady-state peak-peak ripple on the inductor current to be kept lower than 8 A, and continuous conduction mode (CCM) for the converter, L_1 was calculated to be 125 μH.

Moreover, given that the voltages supplied by the Zener regulators equal $V_n = -30$ V and $V_p = 2.5$ V and by taking into account a minimum input voltage of $V_{in,min} = 50$ V, the turns-ratio must be equal to $N_1/N_2 = 1{:}1$. Thus, even if the lowest boundary of the input voltage ($V_{in,min} = 50$ V) is fed to the converter, the Zener voltage regulators will be activated properly. Table 1 shows the design parameters of the coupled inductors, which prevent magnetic saturation of L_1. The parameters of the experimental setup are summarised in

TABLE 1 Parameters of the inductor

Parameter/component	Value
Core type	2xE80/38/20
Core material	Ferrite N87
Saturation induction of the core, B_{sat}	0.35 T
Number of turns, N_1	40
Air-gap, l_g	16 mm
Relative permeability, μ_r	1680
Cross-section area of the core A_c	387 mm^2

TABLE 2 Parameters of the experimental setup (power circuit and gate driver)

Parameter/component	Value
Input voltage, V_{in}	50–150 V
Nominal output voltage, V_{out}	600 V
Switching frequency	50 kHz
Maximum duty ratio, D	0.92
C_{in}	80 μF
C_{out}	30 μF
L_1	125 μH
Turns-ratio, N_1/N_2	1:1
SiC Schottky diode parameters	1200 V/30 A
Start-up IGBT	IXYS, IXA55I1200HJ
Diode rectifier, D_b	Vishay GSIB2540 (400 V/25 A)
C_{DC}	2.2 μF (400 V)
V_n	−30 V
V_p	2.5 V
R_{leak}	2.2 kΩ
IC-driver	Ixys IXDD614
Optocoupler	TLP 250
R_g	10 Ω
R_p	12 kΩ
C_g	22 nF
D_g	SMA 40 V/1 A SK14

Table 2. In addition, the PWM signal and the turn-ON signal to the IGBT are provided by a digital signal processor (DSP) (Texas Instruments TMS320F28335).

This set of experiments has been performed by setting the input voltage to V_{in}=50 V. The complete start-up process of the DC/DC boost converter is shown in Figure 10. In this figure, the measured gate-source and drain-source voltages, as well as the drain current of J_m and the current flowing through L_1 are illustrated. As expected, when the start-up process is initialised, the shoot-through current (either I_{L_1} or I_{J_m}) starts rising. The first current peak, due to the charging of C_{DC}, appears approximately 100 μs after the initialisation of the start-up process. After this, the shoot-through current continues rising until the auxiliary gate driver supply is activated. The term "activation"

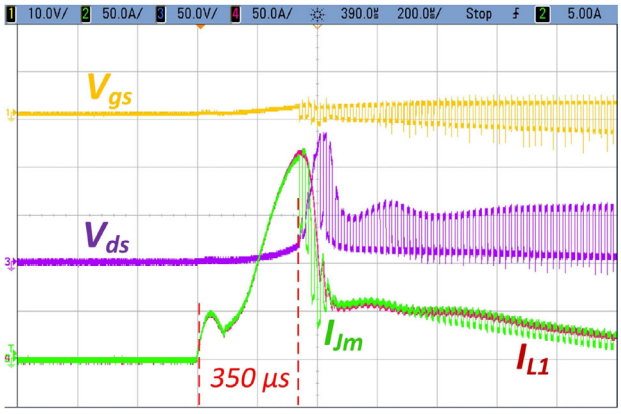

FIGURE 10 Measured gate-source voltage of J_m (yellow line, 10 V/div), drain-source voltage of J_m (purple colour, 50 V/div), drain current I_{J_m} (green line, 50 A/div), and inductor current I_{L1} (red colour, 50 A/div), (time base 200 μs/div) during the start-up process of the converter

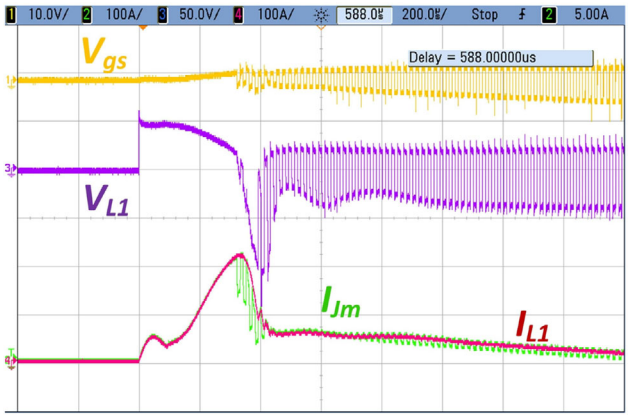

FIGURE 11 Measured gate-source voltage of J_m (yellow line, 10 V/div), voltage across L_1 (purple colour, 50 V/div), drain current I_{J_m} (green line, 100 A/div), and inductor current I_{L_1} (red colour, 100 A/div), (time base 200 μs/div) during the start-up process of the converter

refers to the time point where the IC-driver is able to supply an adequately negative output voltage V_g, which is able to turn-OFF the JFET.

Considering that the PWM signal starts simultaneously with the activation of the converter, the switching process of J_m also starts as soon as the IC-driver is activated. This can be seen in Figure 10 approximately 350 μs after the initialisation of the start-up process. It must be noted that, in order to prevent large overvoltages on the output of the converter, the duty-ratio is slowly increasing from zero up to the steady-state value. Moreover, from Figure 10 it is clear that J_m is switching in the active region, because V_{gs} is lower than zero and less negative that the pinch-off voltage of the device (V_{pi}=–5 V). The switching operation in the active region can also be seen from the simultaneous stress of J_m with high values of blocking voltage (purple line in Figure 10) and current I_{J_m} (green line in Figure 10).

The voltage across the inductor L_1 is shown with the purple line in Figure 11. When the start-up process starts, this voltage is positive and causes a rising current that flows through

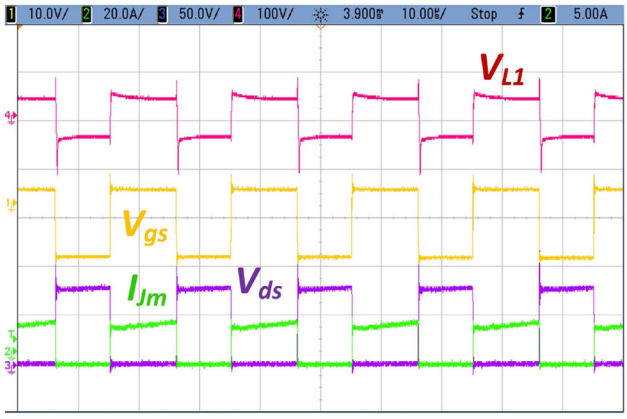

FIGURE 12 Steady-state operation of the DC/DC boost converter. Measured gate-source voltage of J_m (yellow line, 10 V/div), inductor L_1 voltage (red colour, 100 V/div), drain current I_{J_m} (green line, 20 A/div), and drain-source voltage of J_m (purple colour, 50 V/div), (time base 10 μs/div)

L_1 and J_m (red and green waveforms in Figure 11, respectively). When the PWM switching process starts, the voltage across L_1 becomes negative and I_{L_1} starts to decrease. This is due to the fact that when the switching operation starts, J_m conducts a high current and the device operates in the active region. Moreover, during the start-up process and before the switching process starts, the output voltage of the DC/DC boost converter, V_{out}, equals zero. As soon as V_{ds} starts rising, the output voltage of the DC/DC boost converter, V_{out}, also starts increasing and equals the envelope of the switching waveform of V_{ds}. Thus, $V_{L_1} = V_{in} - V_{out}$, which is a negative voltage and I_{L_1} is decreasing.

The steady-state operation of the DC/DC boost converter is reached a few milliseconds after the time instant that the start-up process is initialised. This time interval depends on the values of the passive components of the power converter and the design of the UASP. A caption shown the normal switching operation of J_m at steady-state is presented in Figure 12. From this figure, it is obvious that the converter is operating in CCM at a switching frequency of 50 kHz and a duty ratio slightly higher than 0.5.

5 | OPERATION OF THE UASP CIRCUIT IN LOW-VOLTAGE SOLID-STATE DC BREAKERS WITH NORMALLY-ON SIC JFETS

5.1 | Simulation results

The application and performance of the proposed UASP in a solid-state DC breaker employing a normally-ON SiC JFET has been investigated using simulations. For this purpose a low-voltage DC breaker consisting of a 1200-V SiC JFET that is connected in a DC line has been modeled using LTspice. The SiC JFET is rated at 63 A and has an on-state resistance of 35 mΩ at room temperature. Since the focus of these investigations is to validate the operation of the UASP at device level, a Spice software is the most suitable tool for this purpose. The utilised LTspice device model for the normally-ON SiC JFET (United-SiC, UJ3N120035K3S)) was provided by the manufacturer [40]. Table 3 summarises the design and modelling parameters for the breaker and the DC line.

TABLE 3 Modelling parameters of the solid-state breaker with normally-ON SiC JFET

Parameter/component	Value
DC grid voltage, V_{DC}	700 V
Inductance of the primary winding, L_1	400 μH
Inductance of the secondary winding, L_2	4 μH
Coupling coefficient, c	0.95
Turns-ratio, $N1/N2$	10:1
DC capacitance in UASP, C_{DC}	1 μF
Zener diode, V_n	−30 V
Zener diode, V_p	2 V
Clamping voltage of MOV, V_{MOV}	900 V
Damping resistance, R_d	4 Ω
Load resistance, R_{load}	20 Ω
Nominal line current, I_{line}	35 A
Maximum allowable fault current, $I_{SC_{max}}$	70 A

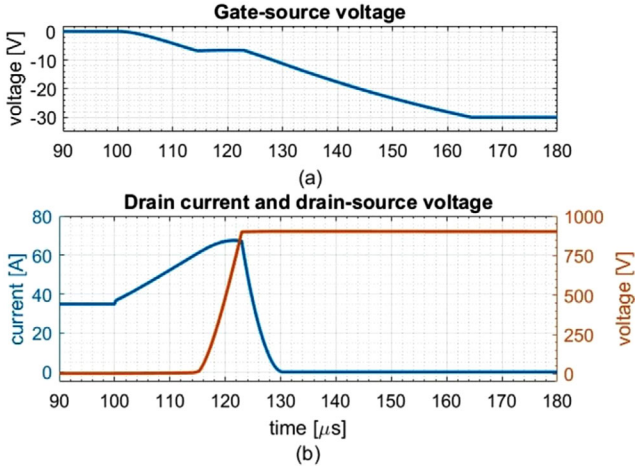

FIGURE 13 Simulation results showing (a) the gate-source voltage and (b) drain current and drain-source voltage under a fault condition

It is assumed that during normal operation of the solid-state DC CB, the SiC JFET conducts a line current of 35 A as shown in Figure 13 prior to t=100 μs. At this time instant t=100 μs a pole-pole fault occurs and, thus, the line current starts rising due to the positive voltage of V_{DC} across L_1. The induced voltage across L_2 is rectified and the gate-source voltage, u_{gs} starts to develop as shown in Figure 13(a). Based on this figure, u_{gs} reaches the steady-state value of −30 V within approximately 60 μs. However, the current through the SiC JFET, i_d, is turned-OFF approximately 23 μs after the fault occurrence as shown in Figure 13. This happens the time instant when u_{gs} drops below the pinch-off voltage of the JFET ($V_{pi} = -6$ V). The drain-source voltage of J_m which has started rising 14 μs after the

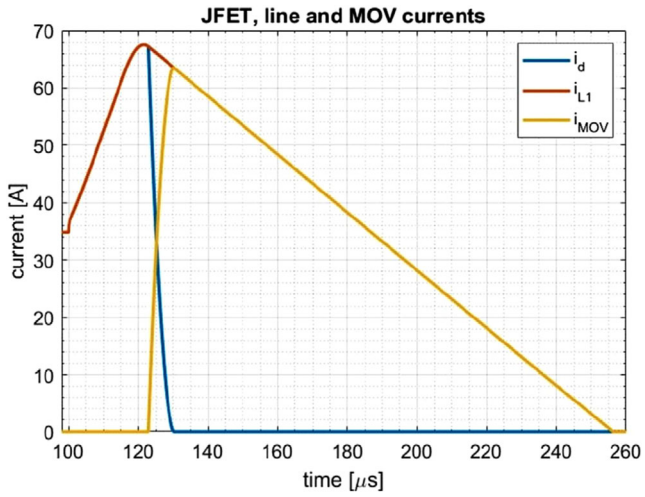

FIGURE 14 Simulation results showing the currents through the SiC JFET, the line current and the MOV under a fault condition

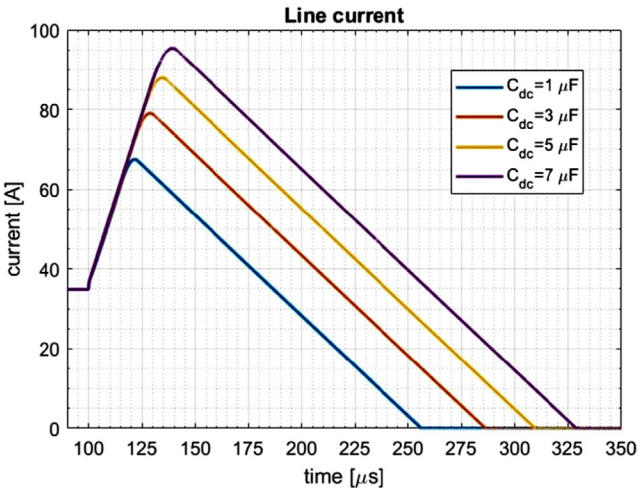

FIGURE 16 Simulation results showing the impact of the choice of C_{DC} on the anticipated line current under a fault condition

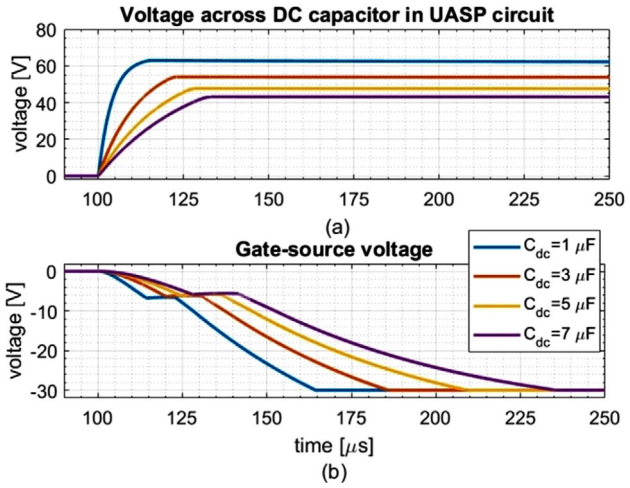

FIGURE 15 Simulation results showing the impact of the choice of C_{DC} on the anticipated (a) voltage across the C_{DC} and (b) gate-source voltage of the SiC JFET under a fault condition

fault occurrence, is clamped at the breakdown voltage of the MOV, which has been set to 900 V as shown in Figure 13(b). As long as the residual energy from the line is dissipated in the MOV, the SiC JFET is blocking 900 V, whereas when the energy dissipation is complete, u_{ds} drops to the nominal grid voltage of V_{DC}.

The performance of the various currents during a fault clearing process is illustrated in Figure 14. From this plot, it is obvious that the line current, i_{L_1} is equal to the sum of the JFET current, i_d and the MOV current, i_{MOV}. When the SiC JFET is turned-OFF, the fault current commutates to the MOV, which dissipates the residual magnetic energy of the DC grid. The residual energy dissipation lasts for approximately 135 μs. In addition to that, the peak short-circuit current reaches approximately 68 A, which is within the limit set.

A further observation relates to the choice of C_{DC} and its impact on the peak fault current. Figures 15 and 16 show the voltage across the C_{DC}, the gate-source voltage and the anticipated line current for various values of C_{DC}. Two issues must be highlighted regarding these figures. Firstly, the C_{DC} is charged at higher voltage level by decreasing the capacitance as illustrated in Figure 15(a). This holds true due to the shorter charging time, t_{ch} at lower capacitances along with the voltage drop across the damping resistor, R_d. Secondly, the peak short-circuit current increases by increasing C_{DC} as shown in Figure 16, because as the value of this capacitor becomes higher, a longer time interval is required for the u_{gs} to reach V_{pi} and turn-OFF J_m, as illustrated in Figure 15(b). High currents through the SiC JFET might result in extensive thermal stress and eventually thermal destruction of the device, unless its chip area is sufficiently large to withstand such high surge currents. On the contrary, a very low value of C_{DC} will trip the CB at very low values of fault current. This might cause breaker tripping under load variations, which is undesired in practical applications.

Furthermore, the importance of the design of the secondary inductor, L_2 can be seen in Figures 17 and 18. In particular, Figure 17 shows the voltage across the C_{DC}, $u_{C_{DC}}$ for three values of L_2. Higher inductance of the secondary inductor leads to smaller turn-ratio and thus the voltage $u_{C_{DC}}$ becomes higher. Therefore, the gate-source voltage reaches sooner the pinch-off voltage, V_{pi} and as a result, the short-circuit current is interrupted at lower peak value, $I_{SC_{max}}$ as depicted in Figure 18. However, significantly high inductance might cause high current in UASP circuitry, as well as, breaker tripping under load variations, similar to the C_{DC} case.

All in all, the choice of both C_{DC} and L_2, as well the overall design of the UASP must be made based on the design and operating constraints of the specific application. More specifically, if the protected DC line feeds power to very critical and sensitive loads or supplied by sensitive power sources, it is inevitable to tune the breaker and UASP such that the fault is cleared as fast as possible. On the other hand, for not very critical source and loads and especially for those exhibiting variations during normal operation, the tuning of UASP could be more flexible.

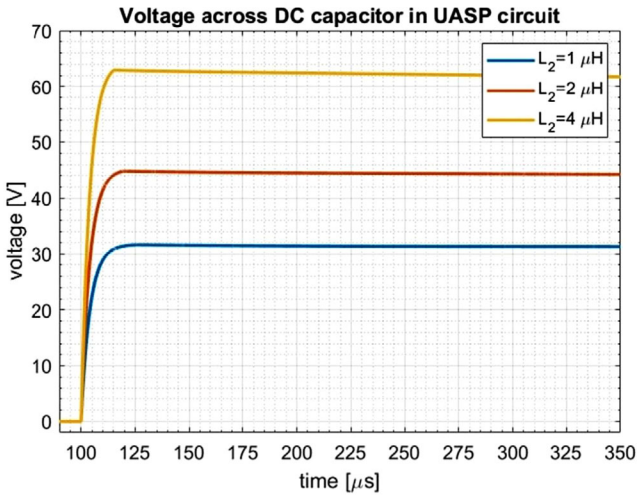

FIGURE 17 Simulation results showing the impact of the choice of C_{DC} on the anticipated voltage across the C_{DC} under a fault condition

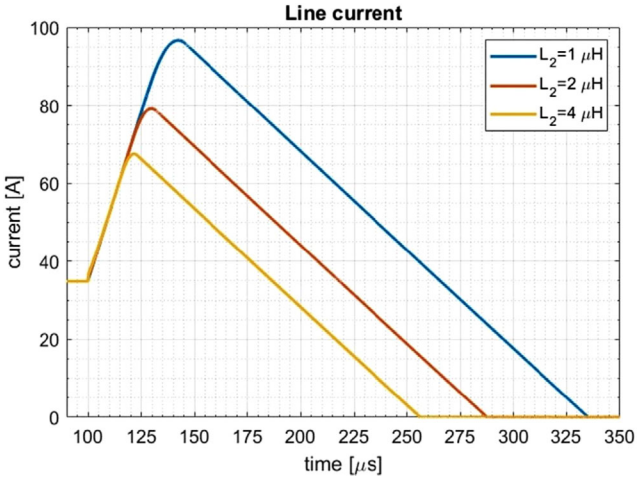

FIGURE 18 Simulation results showing the impact of the choice of C_{DC} on the anticipated line current under a fault condition

5.2 | Experimental results

The performance of the UASP circuit in a solid-state breaker has also been assessed experimentally using the test circuit illustrated in Figure 19. Similar to the simulations presented in Section 5.1, a 1200-V, 63A normally-ON SiC JFET with an ON-state resistance of 35 mΩ at room temperature from UnitedSiC (UJ3N120035K3S) has been used as the main breaker switch. Besides that, a 3.6 kV and 50A IGBT (IXYS IXBX50N360HV) has been considered as an auxiliary switch S_1, which is used to initiate the fault condition. In particular, when S_1 turns-on, a fault line current is flowing through the solid-state breaker. A single pulse test was performed as Figure 19 shows. A photograph of the DC breaker prototype along with the UASP circuit is depicted in Figure 20. Tables 4 and 5 summarise the design parameters for the coupled inductors and the test circuit, respectively.

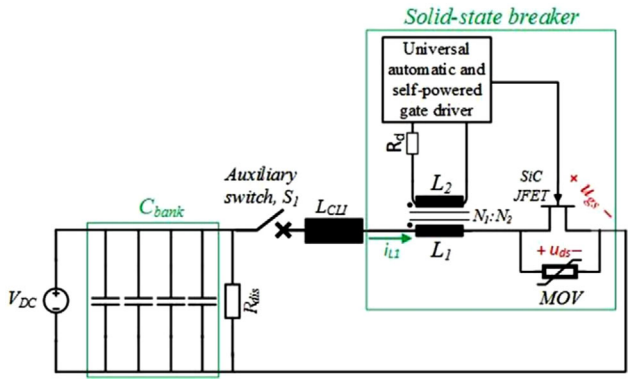

FIGURE 19 Schematic diagram of the test circuit

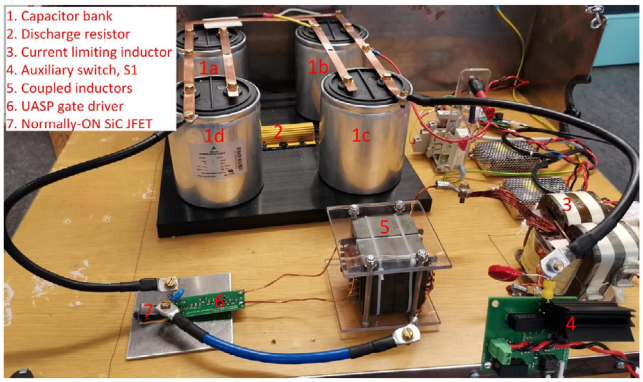

FIGURE 20 Photograph of the experimental solid-state DC circuit breaker prototype employing the UASP circuit

Figure 21 shows the experimental results in case of C_{DC} = 0.1 μF. The line current reaches 23.8 A before the proposed breaker starts the interruption process. The fault clearance time instant occurs at approximately 255 μs. The drain-source voltage of the SiC JFET reaches 848 V, while the voltage across the C_{DC} reaches 35 V in 5 μs and then it stabilises at 28.5 V. On the other hand, Figure 22 shows similar results but in case of C_{DC} = 1 μF. The increase of the capacitance prolongs the turn-off process of the normally-ON SiC JFET and hence, the line current increases accordingly. As a result, the peak current in that case reaches 33 A and the fault is cleared within 330 μs. The capacitor, C_{DC}, is charged in 20 μs reaching a steady-state value of 27.5 V. The last case with C_{DC} = 1 μF corresponds well

TABLE 4 Parameters of the coupled inductors

Parameter/component	Value
Core type	4xE71/33/32
Core material	Ferrite N87
Saturation induction of the core, B_{sat}	0.32 T
Number of turns, N_1	9
Air-gap, l_g	3.15 mm
Relative permeability, μ_r	1680
Cross-section area of the core A_c	1366 mm^2

TABLE 5 Parameters of the experimental setup (power circuit and gate driver)

Parameter/component	Value
Input voltage, V_{DC}	700 V
Main switch SiC JFET	UnitedSiC, UJ3N120035K3S
Auxiliary switch, S_1	IXYS, IXBX50N360HV
Capacitor bank, C_{bank}	EPCOS/TDK, 4 × B25620B1217K983
Discharge resistor, R_{dis}	47 kΩ
Current limiting inductor L_{CLI}	660 μH
Metal-oxide varistor MOV	Bourns MOV-14D621K
L_1, L_2	36 μH
Turns-ratio, N_1/N_2	1:1
Diode rectifier, D_b	ON Semiconductor DF06M
C_{DC}	0.1–1 μF
V_n	−30 V
V_p	5 V
R_{leak}	3 kΩ
IC-driver	Ixys IXDN614PI
R_g	50 Ω

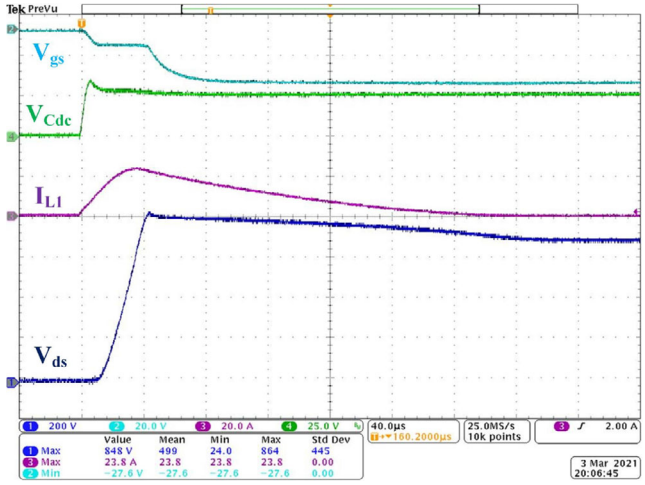

FIGURE 21 Experimental results for the solid-state DC breaker with $C_{DC} = 0.1\ \mu F$. Measured line current (purple line, 20 A/div), C_{DC} voltage (green line, 25 V/div), SiC JFET gate-source voltage (light blue line, 20 V/div), and SiC JFET drain-source voltage (blue line, 200 V/div), (time base 40 μs/div)

with the simulation results shown in Figure 14, where the fault current starts at 35 A and reaches a peak value of 68 A.

6 | CONCLUSION

A universal automatic and self-powered circuit for normally-ON SiC JFET employed in high-input impedance circuits was proposed. The main concept of the proposed circuit is to supply an adequately negative gate voltage using the voltage across

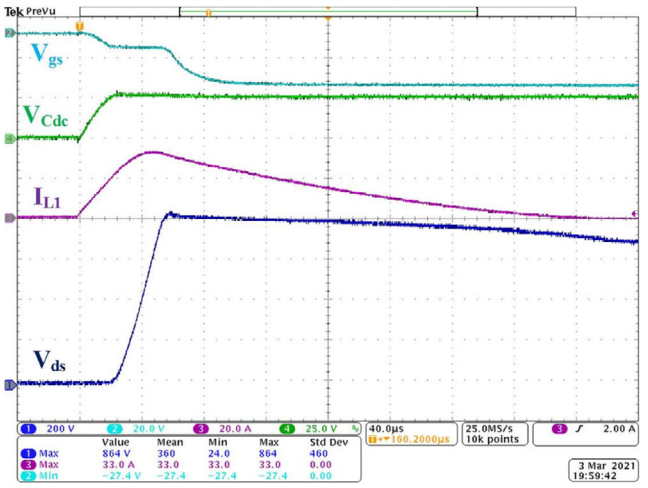

FIGURE 22 Experimental results for the solid-state DC breaker with $C_{DC} = 1\ \mu F$. Measured line current (purple line, 20 A/div), C_{DC} voltage (green line, 25 V/div), SiC JFET gate-source voltage (light blue line, 20 V/div), and SiC JFET drain-source voltage (blue line, 200 V/div), (time base 40 μs/div)

the high-impedance component and an auxiliary coupled winding during both the start-up process and steady-state operation. Apart from its applicability to switch-mode converters, the proposed UASP concept can also be utilised in a low-voltage solid-state circuit breaker.

It has experimentally been shown that applying the UASP in a switch-mode converter, the normally-ON SiC JFET starts switching approximately 350 μs after the start-up process is initialised. However, this time depends on the design of the gate driver supply circuit and the converter. In addition, the steady-state operation of the converter using the UASP circuit is also experimentally shown. Based on these experimental results, a normal switching operation of the normally-ON SiC JFET at 50 kHz during steady-state is observed.

The performance of the proposed UASP concept has also been validated in a low-voltage solid-state DC breaker employing a normally-ON SiC JFET by means of both simulations and experiments. From simulations, it has been shown that the SiC JFET clears a fault current of 68 A within approximately 155 μs, while in experiments, the solid-state breaker interrupts a 33 A short-circuit current in 330 μs. However, a proper and application-oriented tuning procedure is necessary in order to set the tripping current level for the UASP, as well as the expected peak fault currents and thermal stress of the SiC JFET.

It is clear that the design complexity of the proposed UASP gate driver is higher compared to a conventional voltage-source gate driver with external power supply. However, normally-ON SiC JFETs exhibit a better power loss performance in power converters compared to the normally-OFF counterparts. Not only the lower specific on-state resistance and the lower temperature coefficient, but also the voltage-controlled gate-source junction contribute to lower losses.

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