Master's thesis

NTNU
Norwegian University of Science and Technology
Faculty of Information Technology and Electrical Engineering
Department of Electric Power Engineering

Evangelia Rigati

Electrothermal design of medium-voltage, high-power DC/DC converters

Master's thesis in Electric Power Engineering (Master's Programme)
Supervisor: Assoc. Prof. Dimosthenis Peftitsis
June 2020

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Summary

The ever-increasing demand for electrical energy globally and simultaneously the need for clean energy have played an important role in the penetration of renewable energy sources to the electric power distribution grid. As a result, a rapid shift from medium voltage alternating current (MVAC) to medium voltage direct current (MVDC) grids is observed and high power DC-DC converters would play a crucial role in the systems. Dual active bridge DC-DC converter is a quite promising topology to integrate renewables and battery energy storage systems to the MVDC grid. In order to meet the voltage and current requirements of the networks, modularized DAB converters can be developed from the fundamental block and Silicon Carbide (SiC) MOSFET switching devices can be deployed to allow operation of the converters at high switching frequencies, high temperatures and high voltage levels. These properties make them a desirable technology for the bidirectional DAB converter. During the long-term operation of the switching devices, though, failures due to temperature swings in the encapsulation of the chips in different packaging technologies are observed. As a result, there are reliability challenges that need to be tackled for an optimal operation of the MOSFETs in the converters.

This thesis deals with the electrical and thermal design and modelling of a 60 kW modularized DAB DC-DC converter employing SiC MOSFETs. The main purpose is to interconnect photovoltaics and batteries to the MVDC distribution grid. Therefore, two different system configurations have been developed, a centralized and a distributed topology. For an optimal design and operation of the system model, a control scheme has been properly developed, combining a maximum power point (MPP) controller, to track the maximum power from the PV arrays, a single phase shift controller to enable the maximum power flow through the converter and a PI controller to regulate the power flowing from and to the batteries. In order to validate the systems' performance a load profile and variations in solar radiation have been considered for both cases. The results of the system operation have been reported and discussed in terms of reliability and optimal system operation.

Preface

This thesis is the conclusion to my master's degree in Electric Power Engineering at Norwegian University of Science and Technology (NTNU). It is the continuation of the specialization project that was completed in fall 2019, in cooperation with Equinor AS company. The initial scope of the project was to design and control a modularized DAB converter to interconnect photovoltaics and batteries to the MVDC grid with the perspective to construct and test the converter in the lab and carry out studies for enhanced reliability. Due to the unexpected situation of the Covid-19 outbreak, the scope of the thesis was redefined, excluding the part of the experimental analysis, as the lab access was not allowed during the spring semester.

This thesis wouldn't be completed without the academic support and guidance of my supervisor. Therefore, I would like to thank Assoc. Prof. Dimosthenis Peftitsis for supervising and structuring my thesis. I also wish to sincerely thank my co-supervisor at Equinor AS, Dr. Ing. Kamran Sharifabadi, for his guidance and support and for always being available for questions. Furthermore, I would like to express my heartfelt thanks to my parents, Matthaios and Moschoula, as well as my sister, Athanasia, for their unconditional love and support during these two years of my master studies. Last but not least, I would like to thank all my friends and fellow students for the joyful time we spent together and our fruitful collaboration throughout these years.

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Abbreviations

RES	=	Renewable Energy Sources
MVAC	=	Medium Voltage Alternating Current
MVDC	=	Medium Voltage Direct Current
PV	=	Photovoltaic
RES	=	Renewable Energy Sources
BESS	=	Battery Energy Storage Systems
MMC	=	Modular Multilevel Converter
DAB	=	Dual Active Bridge
VSC	=	Voltage Source Converter
ISOS	=	Input-Series Output-Series
IPOP	=	Input-Parallel Output-Parallel
ISOP	=	Input-Series Output-Parallel
IPOS	=	Input-Parallel Output-Series
BJT	=	Bipolar Junction transistor
IGBT	=	Insulated Gate Bipolar transistor
MOSFET	=	Metal Oxide Semiconductor Field Effect Transistor
JFET	=	Junction Gate Field Effect Transistor
ZVS	=	Zero Voltage Switching
DCB	=	Direct Copper Bonded
CTE	=	Coefficients of Thermal Expansion
PCT	=	Power Cycling Test
DUT	=	Device Under Test
TSEP	=	Thermo-Sensitive Electrical Parameter
SOC	=	State of Charge
MPPT	=	Maximum Power Point Tracker
P&O	=	Perturb and Observe
INC	=	Incremental Conductance
PSM	=	Phase Shift Modulation
SPSM	=	Single Phase Shift Modulation
SISO	=	Single Input Single Output
KVL	=	Kirchhoff's Voltage Law
PI	=	Proportional-Integral
PID	=	Proportional-Integral-Derivative
DSP	=	Digital Signal Processors
LPF	=	Low Pass Filter
ADC	=	Analog-to-Digital Converter
ZOH	=	Zero Order Hold
PSSW	=	Phase Shifted Square Wave
EV	=	Electric Vehicle

Chapter 1

Introduction

The ceaseless demand for electrical energy necessitates the increase in power generation worldwide. It has been foreseen that the generated power capacity will be increased by 100 % until 2030, while the global primary energy demand by 55 % [1, 2]. Simultaneously, the reduction of the CO_2-emissions in the utility grid due to massive use of fossil fuels is of primary importance during the last years [2]. The penetration of renewable energy sources (RES) to the utility grid is an attractive solution, as they would provide clean energy generation and distribution to the power system [2, 3]. The European Commission is aiming at decarbonizing the grids by 20 % until 2020 and by 80 % to 95 % until 2050 compared to 1990 situation [4, 5, 6, 7]

So far the electrical energy distribution is achieved by utilizing the MVAC infrastructure [8, 9]. However, the increasing power demand, the electrification of the transportation sector and the increased interest towards the interface between RES, energy storage systems and the existing grid resulted in the investigation of more complex networks [8, 10, 11, 12]. The remarkable progress in the field of power electronics and the lower cost of the DC technology nowadays compared to previous decades played a crucial role to the evolution of MVDC distribution grids [8, 12, 13].

Up till now, though, there have been no real-life installations of MVDC networks and there is still limited knowledge of MVDC specific structure and operating principles [12, 13]. Generally, the design of MVDC grid enables the connection of RES, energy storage systems and loads through different components. These are power electronic converters, transformers, DC transmission lines and proper protection equipment and control strategies for an optimal operation of the systems [14, 15]. Figure 1.1 illustrates a general DC distribution grid. In order to achieve a broad utilization of MVDC networks it is necessary to develop regulations and standards that are not exist whatsoever. The current legislation on MVDC systems only concerns ship and railway applications and the existing standardization refers to DC systems generally. As a result, these may not be applied to MVDC technology [8, 12, 13].

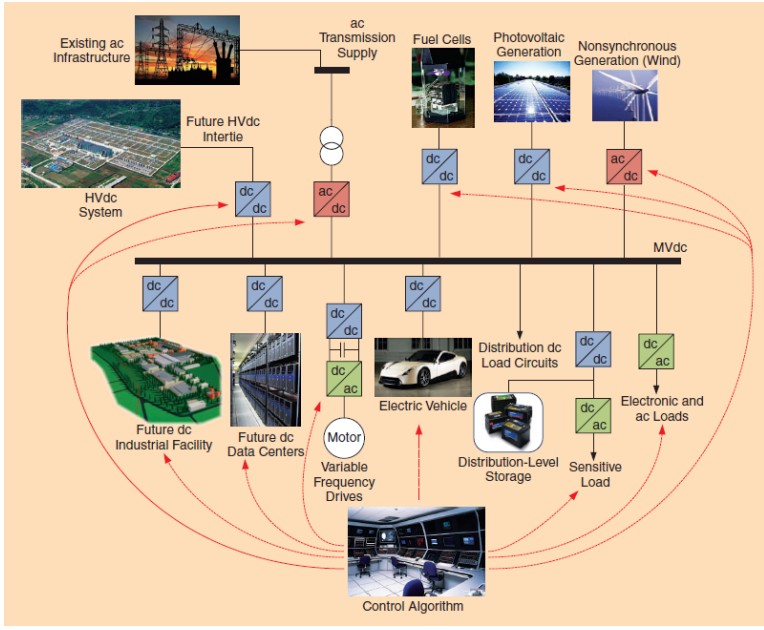


Figure 1.1: General MVDC configuration [13]

Figure 1.2 shows various onshore and offshore applications of MVDC distribution grids. It is clear that these networks enable the interconnection of RES, especially wind farms and photovoltaics (PVs), along with energy storage systems to supply residential and industrial loads. MVDC grid is considered a promising solution as it offers higher stability during synchronization, higher efficiency and better control of active and reactive power compared to MVAC network [2, 8, 16].

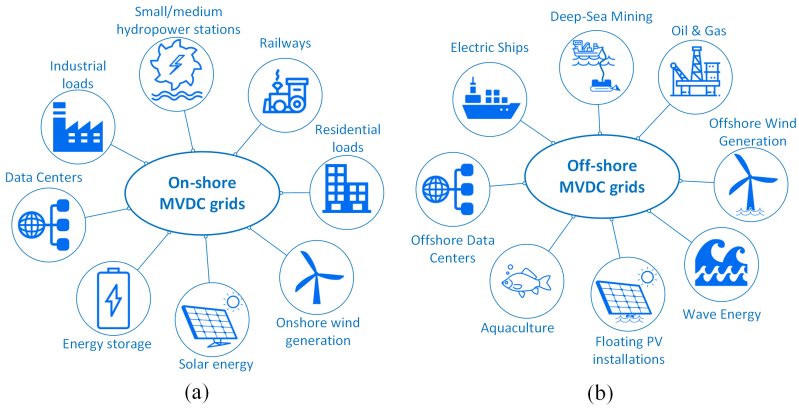


Figure 1.2: (a) Onshore and (b) offshore applications of MVDC grids [8]

Solar and wind energy sources are mainly used in power systems to supply different loads for various purposes. In order to ensure a stable operation of the systems battery energy storage systems (BESS) are utilized.

Generally, battery systems are used in different applications, such as in the transportation sector for vehicles and trains, in backup power systems and for energy storage in stationary applications. As a result, their design is related to charging/discharging power and energy capacity [17]. BESS, in particular, are mainly used in combination with renewable energy sources, for example photovoltaic and wind turbine systems. This is due to the fast response, high efficiency and high energy capacity batteries have, that make them appropriate to balance the instability caused by renewables to the grid [17, 18].

Figure 1.3 shows different topologies of power electronics to integrate PVs and BESS to the AC grid. This architecture can also be used to connect PVs and batteries to the DC grid. As shown in (a) there is a parallel connection of the PVs and batteries to the AC grid through DC-DC and DC-AC converters. In (b) the photovoltaics and batteries are connected in parallel to a common DC bus through DC-DC converters and then to the AC grid through DC-AC inverter. In (c) there is in-line integration topology where the batteries are connected directly to the DC bus and in (d) an AC series connection through DC-AC inverters. Therefore, power electronic converters play a crucial role in order to integrate RES and batteries into the DC and AC grid [8, 19, 20].

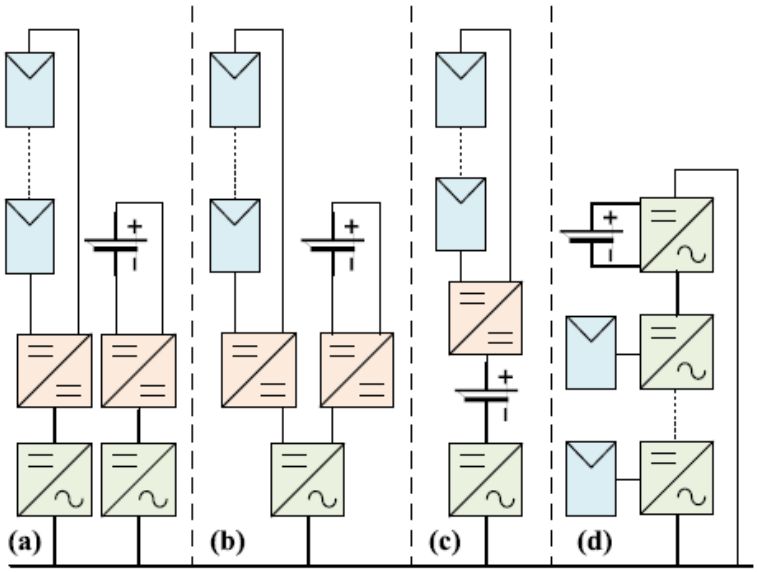


Figure 1.3: State-of-the-art PV-BESS grid connection cases; (a) AC parallel connection (b) DC parallel connection (c) in-line connection and (d) AC series connection [21]

The DC-DC converter [8, 22] is the most promising candidate for DC grids, suitable for high power applications. Particularly, the Modular Multilevel converter (MMC) and the Single- and Three-phase Dual Active Bridge (DAB) converter are of great interest

in research of MVDC distribution grids [22]. Due to its complex design, protection and control schemes, its higher cost and lower efficiency at high voltage ratios, the MMC is less preferable compared to DAB DC-DC converter [23]. The latter, on the other hand has a less complex structure, has shown an impressive efficiency of approximately 99 % and by allowing bidirectional power flow and galvanic isolation between the input and output seems to be the front runner between these two DC-DC converter topologies [8, 22]. In the following chapters a detailed analysis of the DAB configurations and its operating principles is presented. Apart from DC-DC converters, AC-DC converting systems are also necessary in MVDC configurations, but their investigation is out of the scope of this thesis.

The scope of this thesis is to investigate the basic block and modularized DAB DC-DC converter in terms of structure, operating principles and control strategies. Modularized DAB converters have been developed and employed to interconnect PVs and batteries to the MVDC distribution grid. Two different configurations of the hybrid PV-BESS system have been designed, a centralized and a distributed power system. The electrical and thermal performance of the converter switching devices have been investigated under source and load variations in order to assess the reliability of the converters. More specifically, the fundamental research objectives of the thesis are:

- The electrical and thermal design of the fundamental block and modularized DAB DC-DC converter to interconnect PVs and batteries to the MVDC network.
- The development of the dynamic model of the DAB DC-DC converter.
- The development of the MPP controller to track the maximum power generated from the PV arrays.
- The development of the appropriate control scheme based on the dynamic model of the converter to regulate the performance of the converter connected to PVs.
- The development of the proper control scheme to regulate the power flow for the battery-converter system.
- Verification of the overall electrical and thermal performance of the system considering variations in solar radiation and load power demand.
- To present design considerations for enhanced reliability of the converters.

The content of the thesis is organized as follows:

Chapter 1 (the present chapter) introduces the content of the work and briefly describes the objectives that this thesis addresses. At the end of the chapter an outline of the thesis structure is presented (this part).

Chapter 2 is a literature review-based chapter on the DAB DC-DC converter. Particularly, the structure of the fundamental block is analyzed and follow the different topologies of the modularized DAB converters. The semiconductor devices utilized in such a converter are also described and reliability challenges of them are investigated. The application of modularized DAB converters in hybrid PV-BESS systems with various configurations are presented at the end of the chapter.

Chapter 3 introduces the study cases that are modelled and simulated and the development of the PV and converter models is presented. An insight into the operating principles of the DAB converter is given at first for a deeper understanding of its performance. The electrical and thermal analysis has been conducted for a single block DAB converter and the development of the control schemes to regulate the PV, the converter and the battery models is analytically presented.

Chapter 4 comprises captures of the electrical and thermal models and the controllers developed in PLECS simulation software for the two different scenarios that have been considered. Parameters of the systems are also given at this chapter.

Chapter 5 delivers the simulation electrical and thermal results of the under study systems, considering source and load variations to verify the effective operation of the models and control schemes. The reliability results after the implementation of the appropriate algorithm in Matlab are presented at the same chapter for one out of two scenarios.

Chapter 6 summarizes the main points of the thesis work and suggests paths for further investigation in this area of research in the future.

Chapter 2

The modularized DAB DC-DC converter; design aspects, applications and challenges

This chapter presents the modularized DAB DC-DC converter. Different topologies are analysed as found on literature, as well as applications of those converters in PV-BESS hybrid systems. A thorough analysis has been presented on the semiconductor devices implemented on these converters, with emphasis on the challenges and reliability issues of the devices. Two reliability test methods have also been investigated and presented in the following sections.

2.1 The modularized Dual Active Bridge DC-DC converter

The state of art and related work were reviewed, and an identification of the relevant background material were carried out in the project preceding this thesis [24]. No relevant new material was found during the work on the thesis. The presentation from the project report is included below.

The DAB DC-DC converter was firstly introduced in the 1990s by Kheraluwala et.al [25, 26] and since then has gained remarkable attention among a wide number of research groups. What was of great interest in many studies, particularly, was the combination of two single or three phase full bridge voltage source converters (VSCs) with a single or three phase transformer to construct the isolated bidirectional DC-DC converter [27].

Figure 2.1 depicts the basic DAB circuit topology. It is a symmetrical circuit and consists of two full bridges, one on the primary side and one on the secondary side of a high frequency transformer [26, 27]. The H-bridges utilize four semiconductor switches with their anti-parallel diodes. The first bridge operates in an inverter mode, converting the DC voltage into AC and the second as a rectifier, converting the AC into DC voltage in case of positive power flow. The opposite occurs in case of negative power flow. Seeing

that two active converters are utilized in the DAB configuration, bidirectional power flow is enabled [23]. The high frequency transformer is used for galvanic isolation between the two H-bridges, which enhances the efficiency of the converter [22, 28]. The leakage inductance, L_s, is used as an energy storage component. Due to a phase shift between the voltages at the primary and secondary side of the transformer, a voltage difference appears on the stray inductance of the transformer and, therefore, power is transferred across the DAB [23]. A large DC capacitor is used at the input and output of the DAB converter ($C_{dc,1}$ and $C_{dc,2}$) for DC voltage stability and power balance [25].

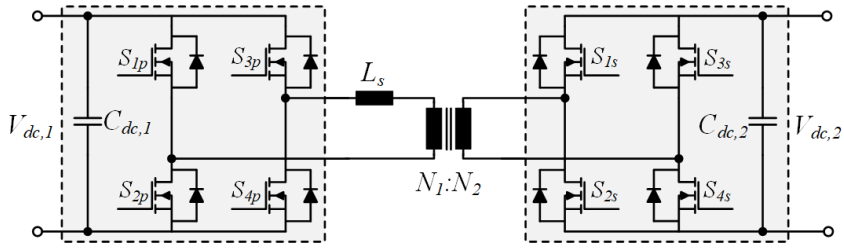


Figure 2.1: Schematic diagram of bidirectional isolated DAB DC-DC converter

A modularized DAB DC-DC converter system can be designed by connecting two or more fundamental blocks in series and/or in parallel owing to galvanic isolation between the input and output terminals of the single-block DAB converter [27]. This modular configuration enables the converter's operation at higher voltage and/or current ratings and an easier adaption of the system power [23].

Figures 2.2 to 2.4 show four possible modularized configurations [29]. The number of the fundamental blocks connected in series and/or in parallel are specified by the voltage and current requirements at the converter terminals. Figure 2.2 illustrates the schematic diagram of the configuration where both the input and output terminals are connected in series (Input-Series Output-Series, ISOS). In this case special attention is paid to balance the voltage sharing at the input and output of the converters with no interest to current balancing.

In Figure 2.3 the modularized DAB converter is designed with both the input and output terminals connected in parallel (Input-Parallel Output Parallel, IPOP). With this configuration the current sharing between the converter terminals is balanced so as to avoid circulating current between the converters.

Figure 2.4 shows the modularized DAB DC-DC converter system, where a series connection of the input terminals is made, while the output terminals are connected in parallel (Input-Series Output-Parallel, ISOP). This configuration enables current sharing balance at the output and the DC output voltage can be stepped down.

Figure 2.5 illustrates the case where the DAB converters are connected in parallel at the input and in series at the output (Input-Parallel Output-Series, IPOS). This configuration is of great importance since the output voltage can be stepped up, while there is input current sharing balance and output voltage sharing balance between the converters.

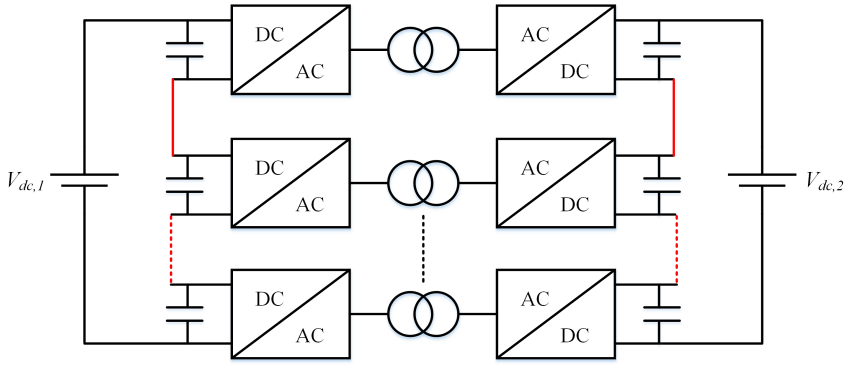


Figure 2.2: Schematic block diagram of the input-series output-series isolated DC-DC converter

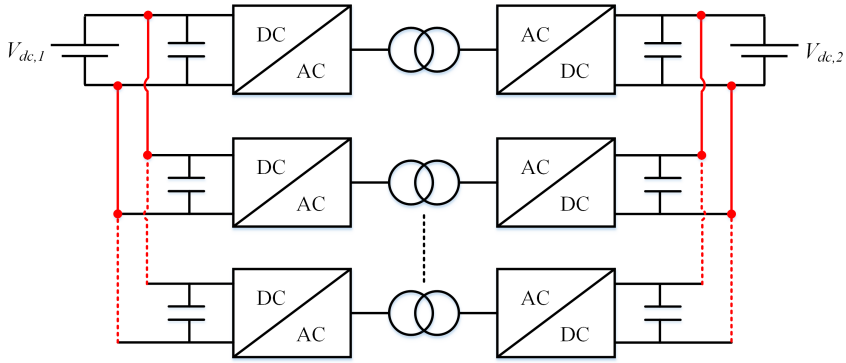


Figure 2.3: Schematic block diagram of the input-parallel output-parallel isolated DC-DC converter

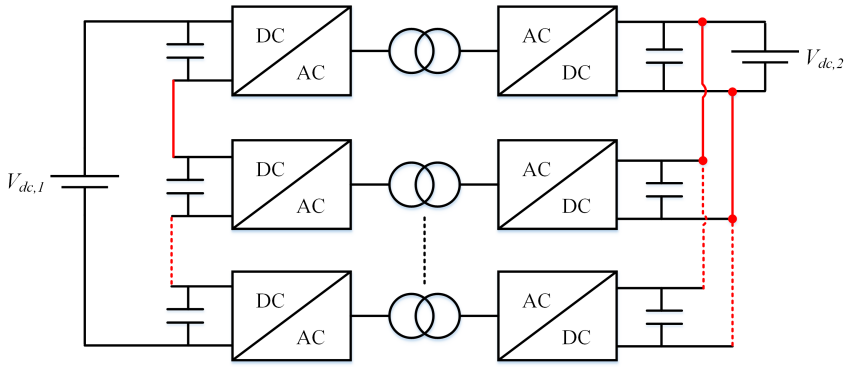


Figure 2.4: Schematic block diagram of the input-series output-parallel isolated DC-DC converter

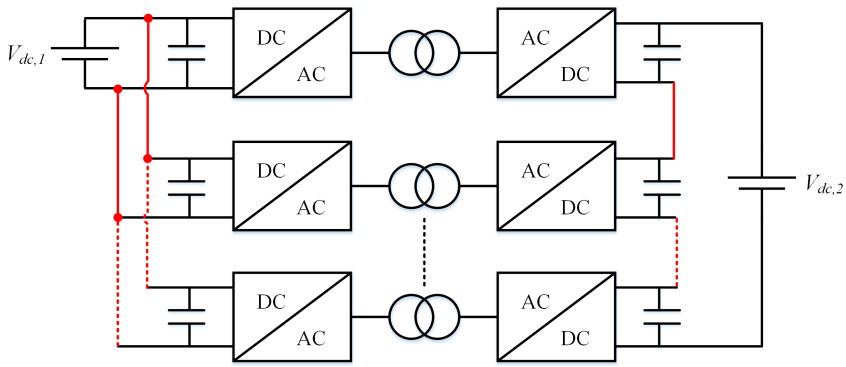


Figure 2.5: Schematic block diagram of the input-parallel output-series isolated DC-DC converter

Modular approach of DAB DC-DC converters has been thoroughly investigated the last years to achieve higher voltage and/or current levels, higher efficiency along with reduced cost. In [30, 31] the authors analyse the ISOP configuration of three DAB DC-DC converters and focus mainly on the design of proper control schemes to ensure the optimal distribution of the input voltages between the converters. In [32] the ISOP connection of three DAB converters is investigated experimentally to assess the behaviour of this modular configuration and validate the theoretical models. Last but not least, the authors in [33] analyse the application of modular DAB converters to an offshore wind farm. The wind generators are separately connected to the DAB converters, which are connected in parallel at the input and in series at the output (IPOS). An appropriate control strategy is presented to balance the current and voltage sharing at the converters' terminals.

2.2 Power semiconductor devices utilized in a DAB DC-DC converter

Power semiconductor devices operate mainly in switching mode when used in most of the power electronic applications [34]. Some of the widely used devices in modern power electronics are the bipolar junction transistors (BJTs), schottky diodes, insulated gate bipolar transistors (IGBTs), metal-oxide-semiconductor field effect transistors (MOSFETs) and junction gate field-effect transistors (JFETs) [34, 35, 36, 37]. So far silicon (Si) has been the dominant material for semiconductors of all types of power devices. This is because silicon allows the fabrication of products with well-suited parameters and at reasonable costs [38, 39, 40]. However, the evolution of the existing power semiconductors was necessary in order to meet the higher system efficiency and higher power density demand in different applications [41, 42, 43]. This resulted in the research of other wide bandgap materials, such as silicon carbide (SiC) or gallium nitride (GaN) as an alternative to Si devices [39, 41, 42, 43, 44, 45].

2.2.1 Advantages of SiC devices

SiC devices are attracting more and more the interest of many research groups and various manufacturers globally [46, 47, 48]. The wide bandgap semiconductors allow operation at higher temperatures, that can exceed 200 ^0C and with their higher thermal conductivity the heat can be easily dissipated [38, 43, 46, 49, 50]. Furthermore, due to the higher breakdown electric field of the SiC material the devices can operate at higher voltage levels compared to Si-based devices, while due to their lower on-state resistance they can operate with lower conduction losses [38, 39, 42, 43, 44, 47, 51]. Another advantage of the SiC semiconductors is the lower switching losses at a given switching frequency compared to Si counterparts. This is due to the high switching speed they have, that is, the turn-on and turn-off time instants are significantly reduced. Last but not least, SiC devices can operate at higher switching frequencies, which is desired since the size of system components, such as inductors and capacitors is reduced and at the same time a smooth power flow and a low system cost is achieved [38, 46, 48]. Figure 2.6 summarizes the Si and SiC properties that are related to various applications [46].

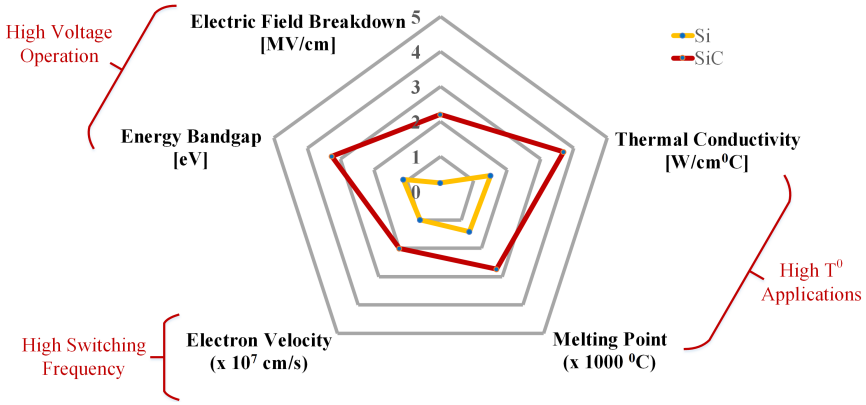


Figure 2.6: Radar chart of the Si and SiC relevant material properties

2.2.2 SiC MOSFETs

SiC MOSFETs are considered a milestone in the evolution of power semiconductors and they can be used in most of the applications [52]. Figure 2.7 illustrates the vertical structure of a MOSFET. It is a unipolar, voltage-driven device where a positive voltage must be supplied to the drain-source junction for the current to flow through the switch. Due to the lower equivalent output capacitance of these devices compared to that of the IGBTs, there is no need for external snubber capacitance, while the ZVS transition time is considerably shorter. Furthermore, their intrinsic body diode can replace the external anti-parallel diode which is another advantage over the IGBT devices. As a result, the converter size can be reduced and the high frequency switching becomes more feasible with considerably lower losses [53].

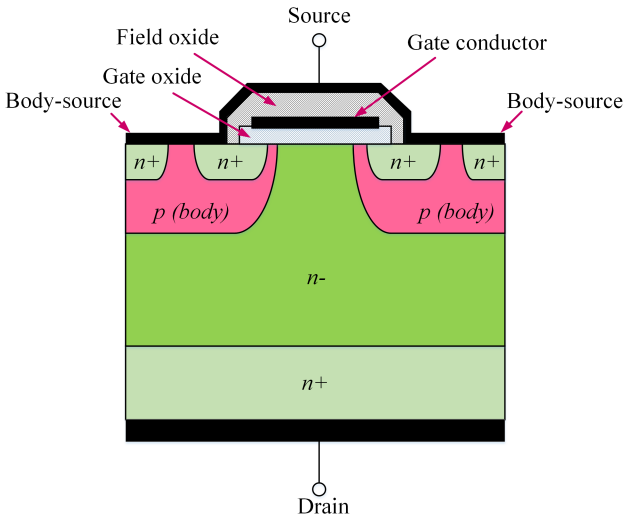
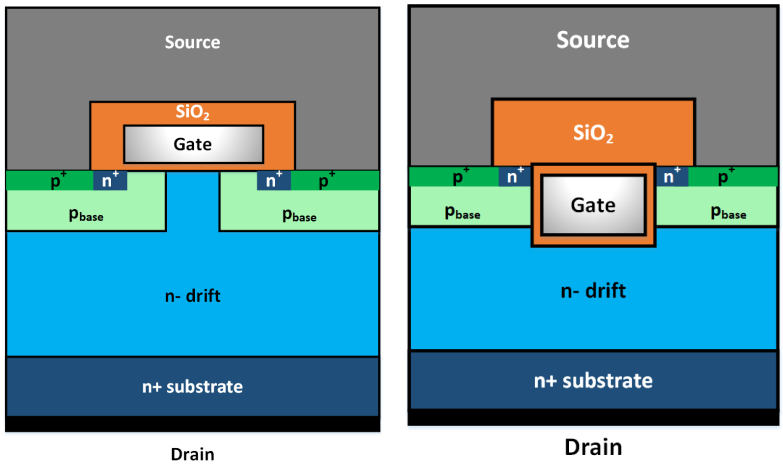


Figure 2.7: Vertical structure of a MOSFET

Currently in the market there are two main designs of SiC MOSFETs, the planar DMOSFET and the trench UMOSFET. The cross sections of these two structures are illustrated in Figure 2.8. The main difference between them is the position of the gate. In the trench technology, the gate is placed at the JFET area and, therefore, the corresponding resistance is excluded. This enhanced design results in a lower on resistance and accordingly lower losses under normal operation in comparison with the DMOSFET [54, 55].



(a) Planar DMOSFET **(b)** Trench UMOSFET

Figure 2.8: Cross section of the planar DMOSFET and trench UMOSFET

One of the challenges when designing SiC MOSFETs is the gate oxide layer, which

proved to be very sensitive at high temperatures and long-term stress [40, 44, 48, 56]. The trench structure, particularly, is rather complicated to fabricate. Another important aspect is the threshold voltage instability, where there is still room for improvement. That is, the mechanisms that are responsible for these voltage variations need to be further investigated [57]. SiC MOSFETs allow the converter operation at higher frequencies with significant low switching losses compared to Si counterparts. However, the challenging part of the high switching frequencies is the higher current overshoot and that more oscillations (ringings) are observed due to the parasitic elements. The oscillations cause a higher EMI spectrum level, which is not desirable [58]. Therefore, a trade-off is necessary between the switching frequency, the losses and the EMI level.

2.2.3 SiC Power Modules

The simple and compact design of the main circuits with SiC switches applied in high power converters necessitate the development of power modules [40]. The latter allow the electrical connection between several chips and circuits and can dissipate the heat to cooling systems, protecting the chips during operation from overheating and harmful ambient influences [59, 60].

To date considerable attempts have been made to construct power modules with high current and temperature ratings. Wolfspeed has presented a half bridge module which is rated at 1200 V/ 450 A maximum current and a 1700 V/ 225 A maximum blocking voltage module implementing SiC planar MOSFETs [61]. Mitsubishi has developed a full SiC power module with 1200 V/ 800 A maximum ratings [62]. Last but not least, Rohm has designed and fabricated a half bridge module applying SiC trench MOSFETs, which is rated at 1200 V/ 576 A maximum drain current and a 1700 V/ 250 A maximum blocking voltage module [63].

2.2.4 Packaging of SiC devices

In practical applications, power devices, either discrete or modules, are encapsulated in packages, as shown in Figure 2.9. The latter illustrates a typical structure of a semiconductor device mounted on a heatsink. The layers between the semiconductor device (chip) and the ambient provide voltage isolation and enables heat dissipation.

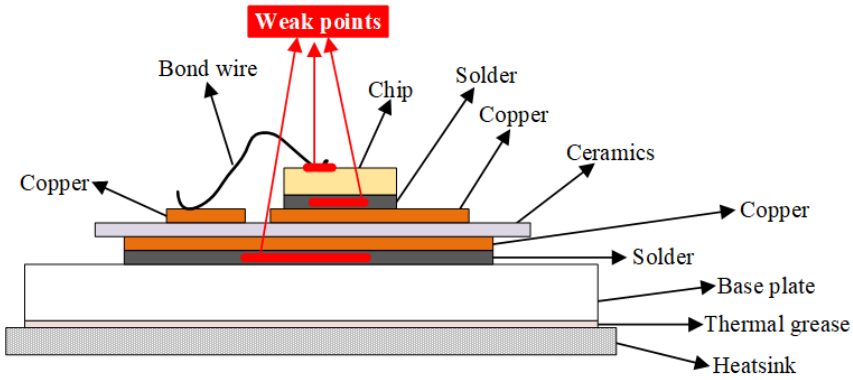


Figure 2.9: Structure of power semiconductor devices mounted on a heatsink

Inside the package, the major technologies implemented so far are the soldering, the wire bonding and utilization of base plate. More specifically, the soldering allows the connection of two metal materials through liquid metal or liquid alloy, while the wire bonding is used for connection of the chip with several other chips or elements. In order to achieve high current levels, multiple aluminium (Al) wires are connected in parallel, while multiple bonding of one wire on a surface (stitching) is also feasible for a better distribution of the current on the chip [60]. Figure 2.10 shows the stitching and parallel connection of bond wires. Due to its flexibility and cost-effectiveness, the wire-bonding technology remains the most dominant connection method for chip surfaces [60].

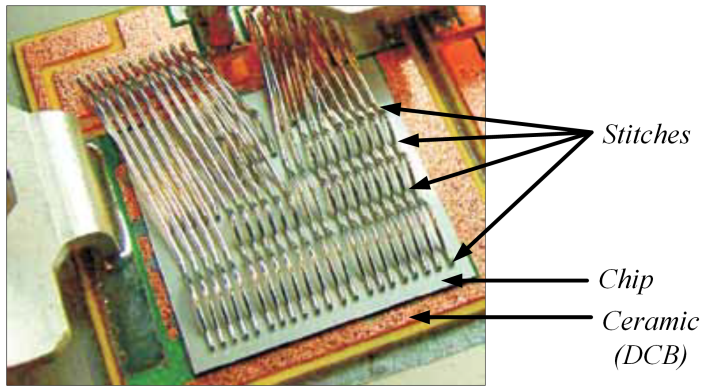


Figure 2.10: Multi-stitched bond wires connected in parallel on a chip [60]

Another important technology is the utilization of the base plate, as shown in Figure 2.9. A direct copper bonded (DCB) substrate, consisting of copper-ceramics-copper layers, is soldered to a base plate. The latter is mainly used in medium and high power ranges and it is not so frequently used in lower power applications [59]. The base plate provides thermal capacity and enables the heat spreading easily while the modules show higher mechanical robustness during transport and assembly [59, 60].

2.2.5 Reliability challenges of SiC devices

Apart from the sensitivity of SiC MOSFET's gate oxide layer, another challenge that needs to be tackled is the high temperature variations (swings) during the operation of the converter [64]. The temperature swings is the result of the heat generated from power losses in the device, as well as the ambient temperature variations. When the devices are stressed under high temperature swings, two main failure mechanisms are observed, the *bond wire lift-off* and the *solder delamination* [64, 65].

Each device package consists of various materials, which have different coefficients of thermal expansion (CTE). The CTE mismatch when the temperature varies applies thermo mechanical stress to the materials and fatigues are observed in the device. Either the bond wire lift-off due to the thermal mismatch between the Al bond wire and the SiC chip or the solder delamination. More specifically, two solder layers are formed in a package, the chip solder layer and the solder layer between the DCB substrate and the base plate, according to Figure 2.9. Under temperature variations the different material layers have a relevant movement due to contraction and expansion and cracks appear in the solder layers [59, 65, 66].

Another weak point that is to be considered is the thermal grease layer between the base plate and the heatsink. It has been observed no connection between the device and the heatsink after the removal of the module. This is due to the bad thermal conductivity of the thermal grease layer [65]. The higher the temperature the SiC MOSFETs operate, the higher the temperature swings are, which can be more harmful to the packaging and lifetime of the devices. Therefore, maximum temperature stress must be avoided in order to expand the lifetime of the devices and modules.

Other issues that need to be considered when utilizing the SiC devices are the bipolar degradation, which can affect the body diode of a SiC device, the power cycling capability and its sensitivity to humid environment. Thus, reliability tests are to be done to be able to estimate the remaining lifetime of the devices and, thus, replace or maintain them before a catastrophic failure occurs [64, 66].

2.2.5.1 Reliability tests of power devices

The power cycling test (PCT) is a commonly used method to assess the lifetime of the semiconductors and the reliability of packaging [59, 65, 66]. The device under test (DUT) is cycled until either the on-state voltage increases by 5 % before the device is turned off or the thermal resistance of the device increases by 20 % [57]. The test circuit along with the switching signals and temperature profile are illustrated in Figure 2.11.

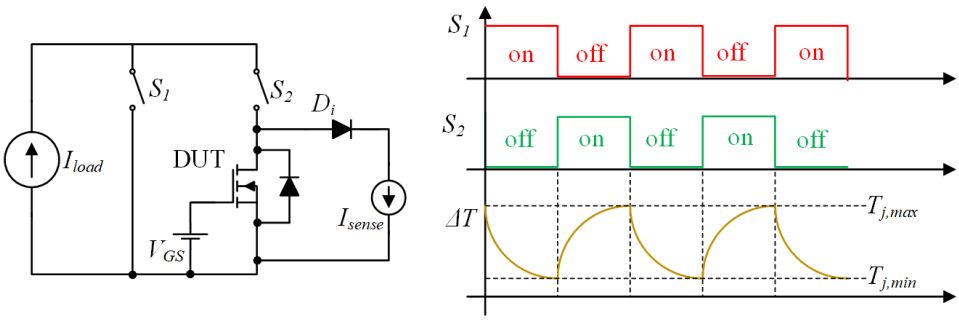


Figure 2.11: Schematic diagram of the power cycling test circuit for SiC MOSFETs with the corresponding control signals of the switches and temperature profile

The switches S_1 and S_2 operate in a complimentary way to avoid power cycling of the source I_{load}. The junction temperature of the device is measured indirectly by measuring a thermo-sensitive electrical parameter (TSEP). A small constant sensing current, I_{sense} is injected to the DUT, which is conducted through the body diode when S_2 is off. In SiC MOSFETs the source-to-drain voltage is utilized as a TSEP, while in Si IGBTs the on-state voltage drop of the switch [57].

However, the temperature stress in a device under operation do not follow any particular pattern, i.e. the ΔT in Figure 2.11 takes random values, which are difficult to predict [66]. This random stress is due to different factors, such as the load variations, the ageing of the devices, the ambient temperature etc. In order to analyse and assess the randomly varying stress waveforms rainflow-counting method can be implemented. This method was firstly introduced in 1968 [67] and is currently used for fatigue analysis of mechanical components.

The original algorithm to identify the rainflow cycles within a sequence is the Pagoda Roof Method, which is summarized in the following steps [66]:

- Identifies the reversal points (peaks and valleys) from the stress or temperature signal history (Figure 2.12 (a)).
- Simplifies the original signal by keeping the amplitudes and the sequence of the reversal points, which are stored in memory, as shown in Figure 2.12 (b).
- This waveform is turned 90^0 clockwise, as illustrated in Figure 2.12 (c).
- Each peak and valley is assumed to be a source from which water flows down the pagoda roof-shape of the rotated waveform (Figure 2.12 (c)).
- The terminations in flow occur either when it meets a new water source that is "deeper" or when it merges with the flow from a previous and "deeper" source.
- A *range* value is assigned to the flow that terminates. Its magnitude is the stress or temperature difference between the source and the termination point. Each flow that terminates corresponds to a half cycle of stress.

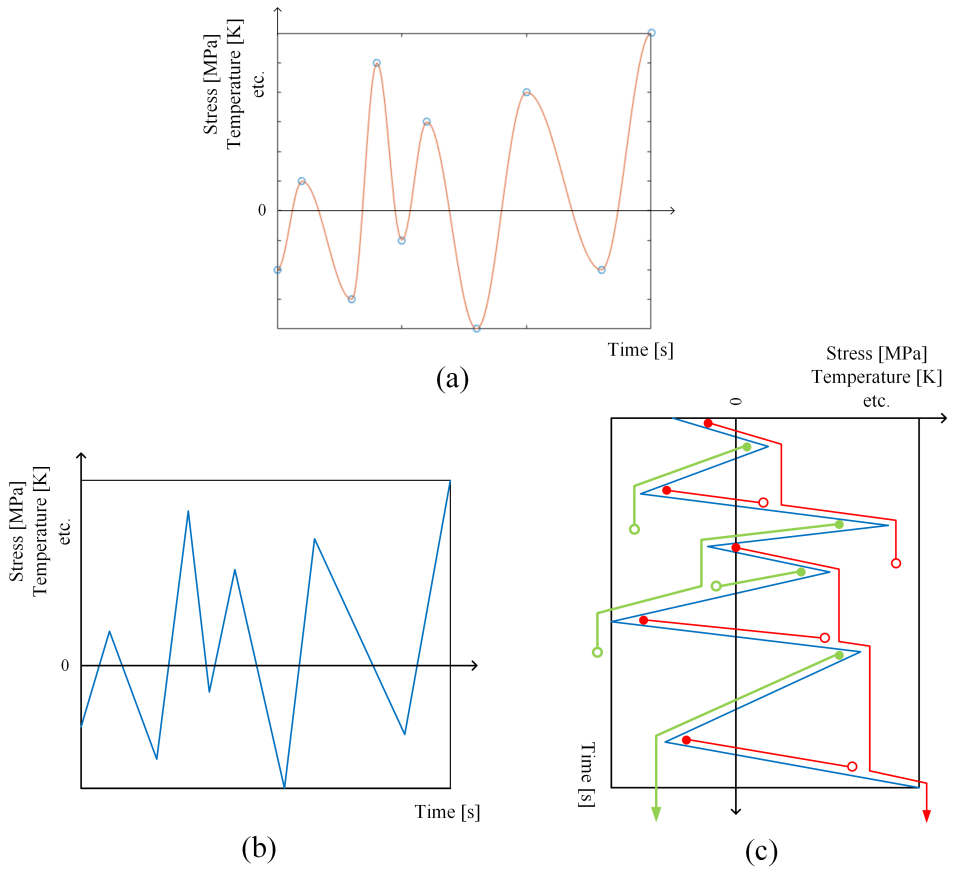


Figure 2.12: (a) Random signal to be evaluated, (b) simplified signal with amplitudes and reversal points and (c) waterflow according to pagoda roof algorithm

2.3 Application of modularized DAB converter in PV-BESS hybrid systems

In recent years there has been a clear orientation of research towards the integration of renewable energy sources, such as photovoltaics to the grid. However, the fluctuations of PV output power due to the unpredictable weather conditions and changes in power demand results in grid instability and, therefore, the PV integration is more challenging [68, 69, 70]. The utilization of battery energy storage systems along with the photovoltaics can compensate the intermittency of the PV generation and ensure a smoother and more stable power flow to the grid. Therefore, the power network stability and reliability is increased [71, 72, 73].

Figure 2.13 illustrates the different modes of operation of the hybrid PV-BESS system, when a load is considered to be connected to the MVDC grid. When the PV power gener-

ation is higher than the load demand ($P_{PV} > P_{loaddemand}$), the PVs supply the load and the charge the battery. In the case when the solar power in not sufficient to supply the load ($P_{PV} < P_{loaddemand}$), the additional power is supplied by the battery and the latter is in discharging mode. When the power produced by the photovoltaics equals the load demand ($P_{PV} = P_{loaddemand}$) only the PVs supply power to the load and the battery is in ideal mode. In the final case that there is no solar PV production ($P_{PV} = 0$) the load demand is covered by the battery, which is in discharging mode.

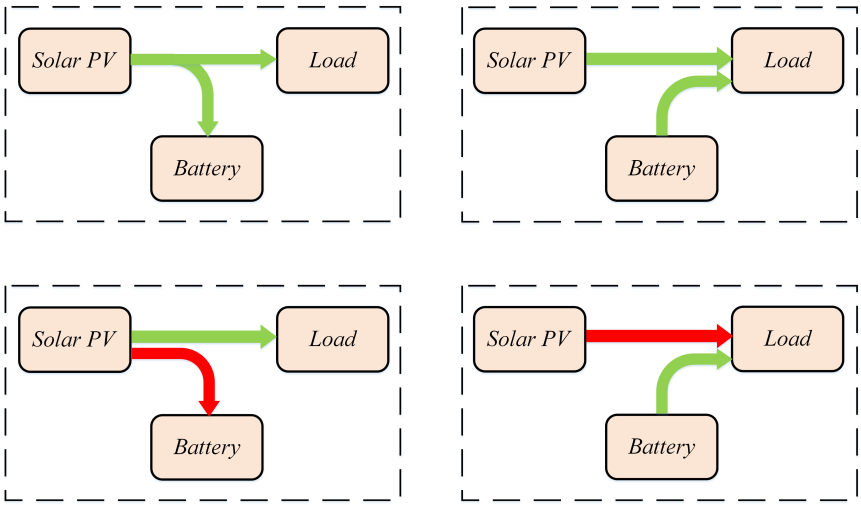


Figure 2.13: Modes of operation of a hybrid PV-BESS system

The variations in solar radiation, the load demand and the state of charge (SOC) of batteries determine the implementation of appropriate converters to handle the power flow and control the DC bus voltage [73]. The most efficient solution is the application of bidirectional modularized DAB converters to allow high power transfer and regulate the bus voltage at the MVDC side.

So far various topologies of hybrid PV-BESS with converting systems have been proposed in the literature implementing DAB DC-DC converters. In [74] a series connection of DAB DC-DC converters is proposed for integration of PVs and BESSs to the MVDC grid. At the input of each converter, batteries are connected in parallel to photovoltaics through a DAB DC-DC converter, as shown in Figure 2.14. The main disadvantage of this configuration is its complicated structure. Each BESS is connected to two DAB converters, which results in an increased number of conversion stages. This increases both the complexity of the control and the amount of losses during the operation of the converters. The authors of [71] propose the series connected DAB converters to interface BESSs to the MVDC grid, while in [75] a multi-input modularized DAB DC-DC converter is presented to integrate multiple battery systems to the DC grid. Such a distributed configuration of batteries and PVs is illustrated in Figure 2.15. The PVs and BESSs are separately connected to DAB DC-DC converters to a common DC bus. There is a series connection of the DAB converters to interface the PVs and batteries with the MVDC grid. The bidi-

rectional capability of the converter enables the charging and discharging of the batteries, whereas there is a unidirectional power flow from the photovoltaics. Another possible topology is shown in Figure 2.16. The modularized DAB converters for interconnection of batteries and PVs to the MVDC grid are connected in parallel at the input with the PVs and batteries respectively and in series at the output. With this centralized configuration high current values are achieved at the input and high voltage values at the output. However, the reliability of the system is low in case of a fault either in batteries or photovoltaics operation.

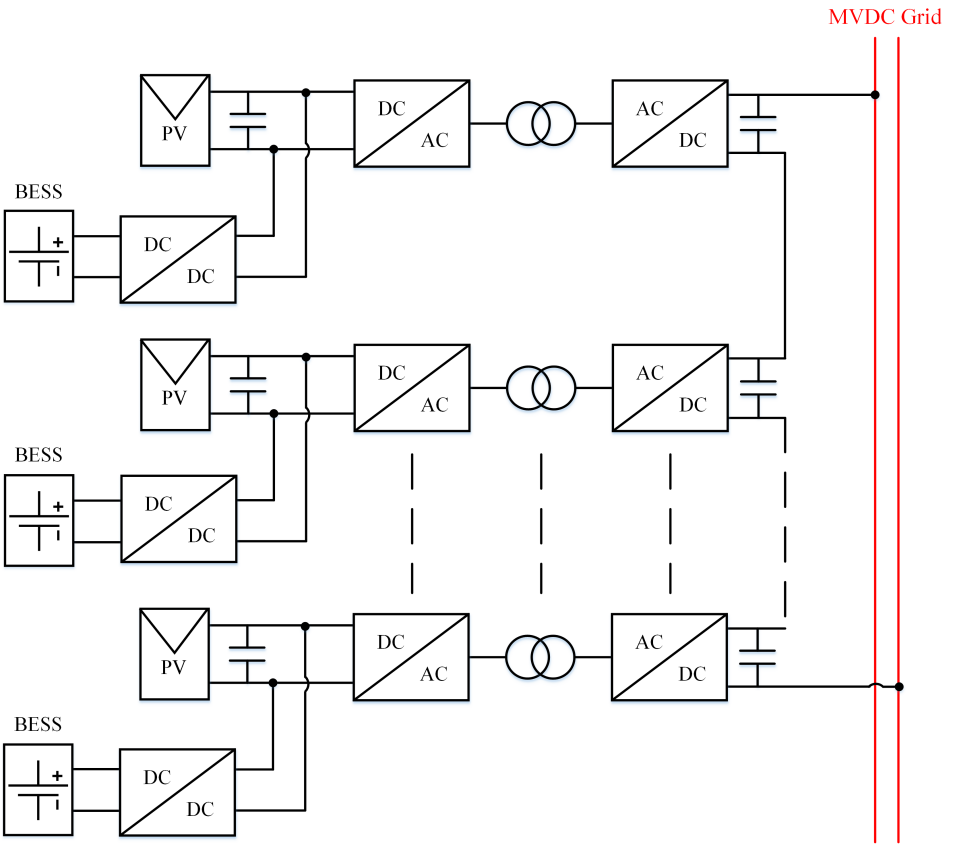


Figure 2.14: Connection of BESS at the output of PVs through a DAB DC-DC converter

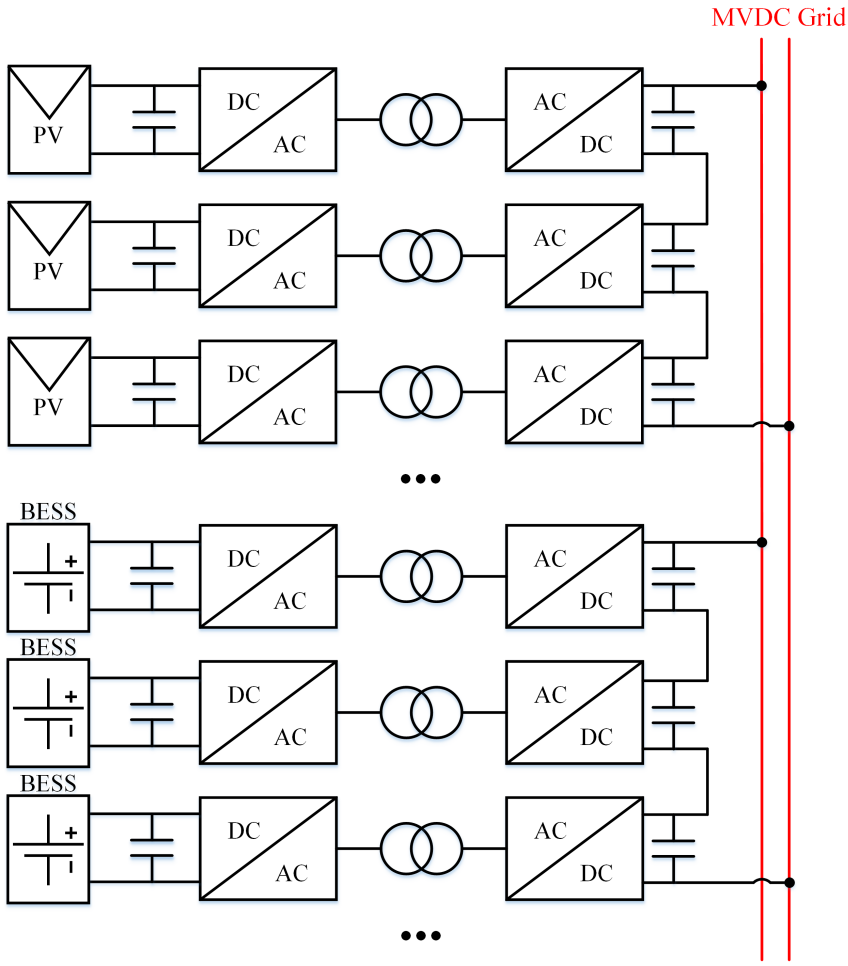


Figure 2.15: Distributed configuration where PV and BESS are connected to the same DC link through DAB DC-DC converters

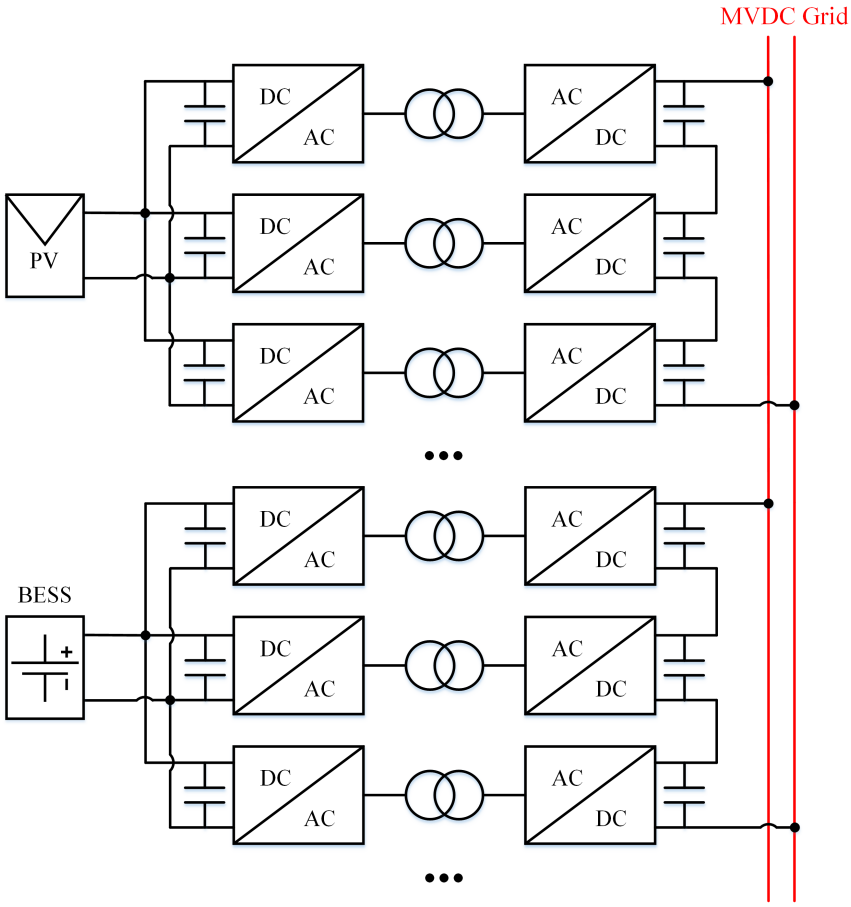


Figure 2.16: Centralized configuration with IPOS connection of DAB converters. PV and BESS are connected to a common DC bus trough the DAB converters

Chapter 3

Design and Control of Hybrid PV-BESS System and DAB DC-DC Converter

The aim of this chapter is to design various configurations of the hybrid PV-BESS system for interconnection to the MVDC distribution grid through DC-DC converters. Two different scenarios, in particular, have been investigated and modularized DAB DC-DC converters have been employed to the systems. Moreover, proper control schemes have been developed in order to track the maximum power point from the photovoltaics, regulate the power transferred through the converters and control the battery system operation. Appropriate switching devices have also been selected to enhance the overall performance of the converters in each case study. In the following sections a thorough analysis of the system components have been conducted for the optimal design of the proposed system configurations.

3.1 Case Studies

Figures 3.1 and 3.2 illustrate the different structures that have been investigated in the present work to integrate PVs along with BESS to the MVDC grid. In the first scenario three DAB converters are connected in parallel with the PV arrays at the input to achieve high current level and in series at the output to obtain high voltage level for the MVDC connection. The same centralized configuration has been considered for the batteries, which are connected to the MVDC grid through three IPOS DAB converters. In the second scenario there is an output series connection of the same converters to meet the requirements of the MVDC grid. In this decentralized structure the DAB converters are separately connected to the PV arrays and BESS. With this structure the system will be able to operate even if a number of the photovoltaics or batteries will fail to operate and therefore the reliability of the system is increased.

An optimal design of the system is based on developing an improved model of the photovoltaics, the proper selection and thermal management of the switching devices utilized in the converters and the optimal sizing of the energy transfer inductances to enable maximum power flow. The filters at the input and output of the converters have been properly selected to handle the current and voltage ripple. Last but not least, the appropriate control schemes for the PV arrays, DAB converters and batteries are of the utmost importance to ensure the optimal operation of the systems.

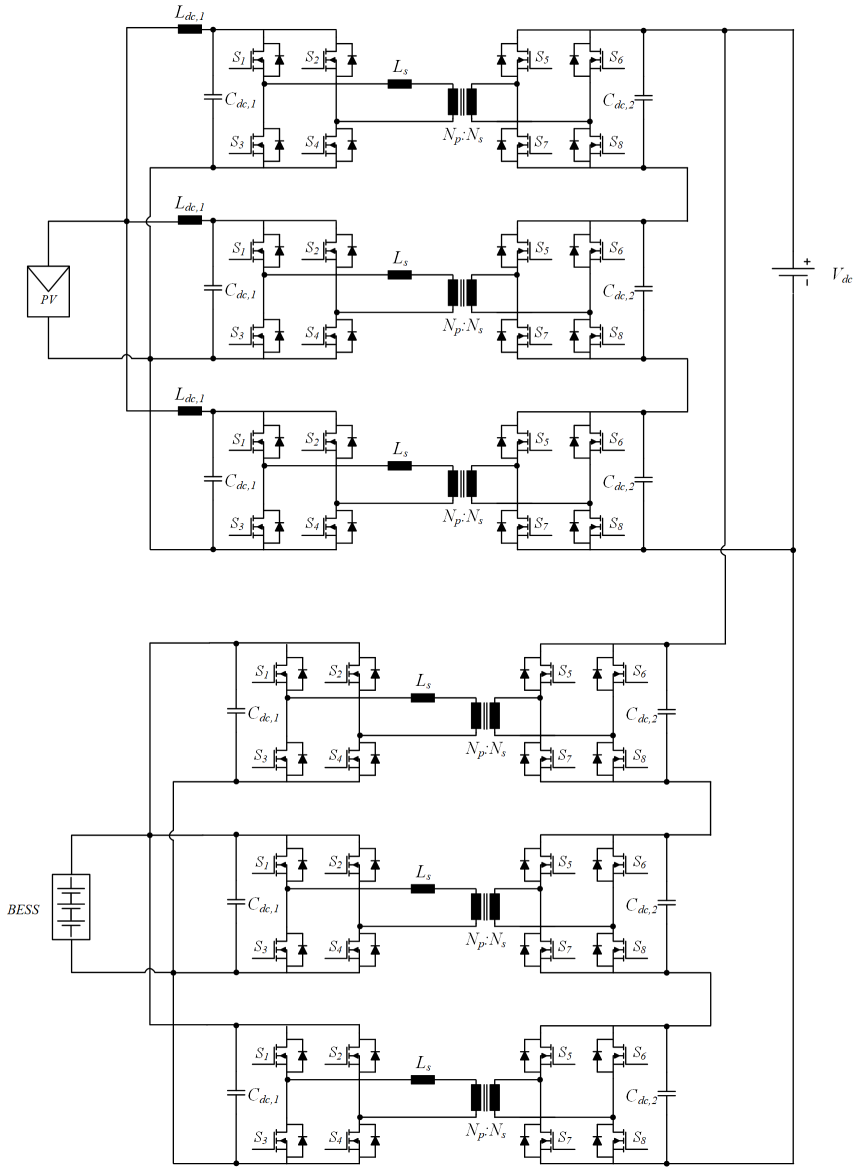


Figure 3.1: Schematic diagram of the proposed centralized PV-battery hybrid system

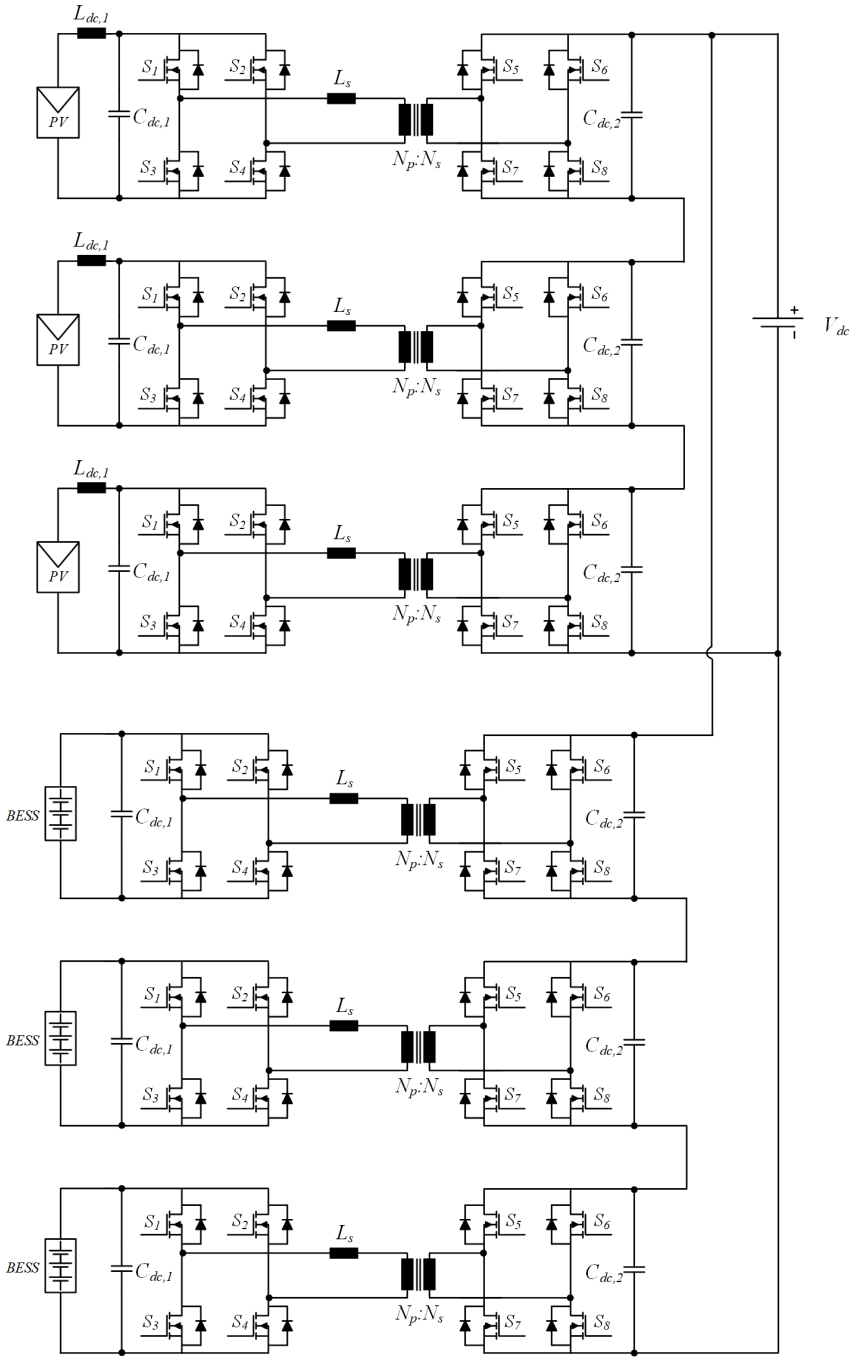


Figure 3.2: Schematic diagram of the proposed decentralized PV-battery hybrid system

3.1.1 Photovoltaic system model

The state of art and related work were reviewed, and an identification of the relevant background material were carried out in the project preceding this thesis [24]. No relevant new material was found during the work on the thesis. The presentation from the project report is included below.

The single diode model developed in [76] has been considered for simulations in the present work. Figures 3.3a and 3.3b depict the equivalent circuit of a practical PV device and the I-V characteristic curve respectively.

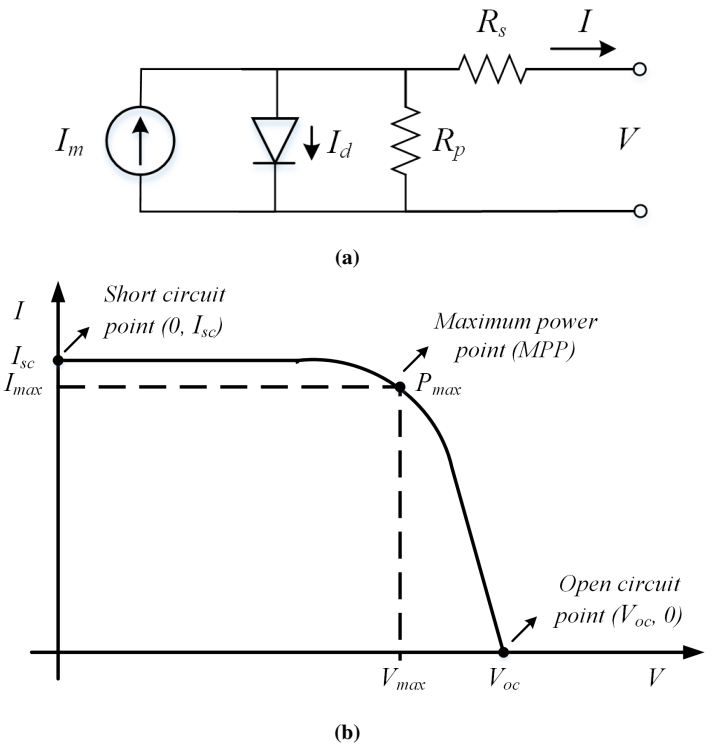


Figure 3.3: (a) The equivalent circuit of the practical PV array and (b) the I-V characteristic curve

This model is described by Equation 3.1 [76] which gives the I-V characteristic curve of a practical PV array:

$$I_m = I_{PV} - I_0 \left[exp\left(\frac{V + R_s I}{\alpha V_t} \right) - 1 \right] \tag{3.1}$$

where $I_{PV} = I_{PV,cell} * N_p$ is the photovoltaic current, $I_0 = I_{0,cell} * N_p$ is the saturation current of the PV array, with N_p the number of the parallel connected cells and R_s and R_p are the equivalent series and parallel resistances of the array. The thermal voltage is calculated by $V_t = N_s kT/q$, where N_s is the series-connected number of cells,

$q = 1.60217662e^{-19}C$ is the electron charge, $k = 1.3806503e^{-23}J/K$ is the Boltzmann constant and T is the temperature [in Kelvin]. The parameter α is the ideality constant of the diode, which takes an arbitrary value usually in the range from 1 to 1.5, depending upon the the parameters of the I-V model.

The generated current from a PV cell is given by Equation 3.2:

$$I_{PV,cell} = (I_{PV,n} + K_I \Delta T)\frac{G}{G_n} \tag{3.2}$$

where $I_{PV,n}$ is the photovoltaic current at standard test conditions (STC, $25^0C, 1000W/m^2$), K_I is the short circuit current/temperature coefficient, $\Delta T = T - T_n$ is the temperature difference between the actual and nominal temperatures [in Kelvin] and G and G_n are the actual and nominal solar irradiation [in W/m^2] respectively.

The diode saturation current can be calculated by the simplified Equation 3.3, as follows:

$$I_{0,cell} = \frac{I_{sc,n} + K_I \Delta T}{exp((V_{oc,n} + K_V \Delta T)/\alpha V_t) - 1} \tag{3.3}$$

Finally, the nominal value of the PV current ($I_{PV,n}$) differentiates from the nominal short circuit current ($I_{sc,n}$) according to Equation 3.4:

$$I_{PV,n} = \frac{R_p + R_s}{R_p} I_{sc,n} \tag{3.4}$$

3.1.2 Dual Active Bridge DC-DC converter

The state of art and related work were reviewed, and an identification of the relevant background material were carried out in the project preceding this thesis [24]. No relevant new material was found during the work on the thesis. The presentation from the project report is included below.

In order to investigate the modularized DAB converter it is of great importance to analyze the structure and operation of the fundamental block. The schematic diagram of a single-block DAB converter is shown in Figure 3.4. This can be expanded and built modularized DAB converters with higher voltage ratings. However, in this thesis, the main focus is on the design, control and performance evaluation of the fundamental block, which are crucial for the optimal design of modularized counterparts.

Each of the two H-bridges consists of four switching devices, operating in pairs, complimentary to each other. The bridges are connected back-to-back via an AC link, which comprises a transformer for galvanic isolation and a leakage inductance, L_s.

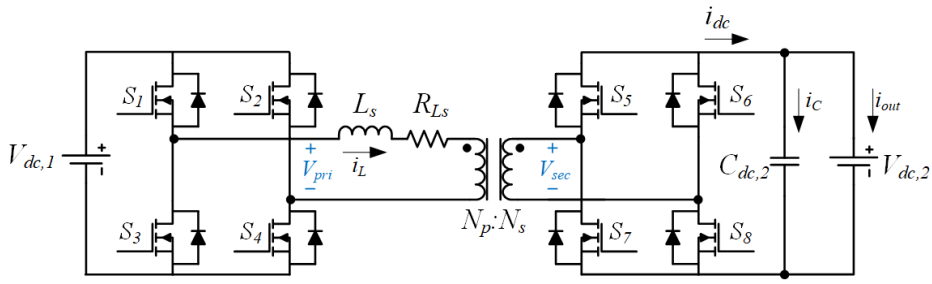


Figure 3.4: Schematic diagram of the bidirectional isolated DAB DC-DC converter

3.1.2.1 Operating principles

Power flow in a DAB converter can be obtained by phase shifting the voltage pulses of the bridges with respect to each other. At high frequencies the magnetizing inductance of the transformer is negligible and, thus, the transformer can be modelled by its leakage inductance. The equivalent circuit of the DAB converter at high frequency ratings is shown in Figure 3.5.

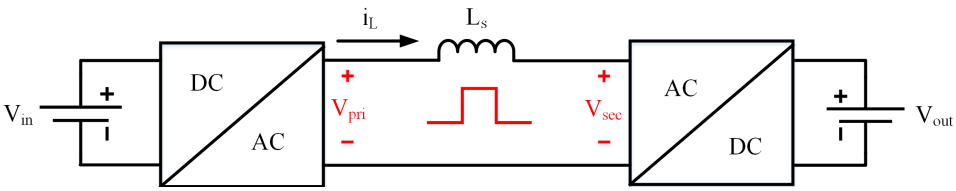


Figure 3.5: Block diagram of the simplified circuit of the DAB converter at high frequencies

The two bridges invert the DC voltages in both sides and AC square waves are produced (V_{pri}, V_{sec}) to feed the transformer. These voltage waves are phase shifted properly by an angle δ and, thus, a voltage difference is appeared across the inductor, resulting in a current i_L to flow.

This operating principle is properly illustrated in Figure 3.6. It is assumed that initially S_1 and S_4 of the primary bridge are conducting. Due to phase shift, switches S_5 and S_8 are delayed by a phase angle δ and therefore the current is flowing through S_6 and S_7 at the secondary side. After angle δ, a control signal triggers the switching pair S_5 and S_8, as shown in Figure 3.6a. Phase-shifted voltage square waves are produced at the output of the H-bridges, according to Figure 3.6b and their difference appears across the inductor. Assuming the case with source variations (e.g. output of PV arrays) this voltage difference is non-zero, i.e. $V_{pri} \neq V_{sec}$. This results in a current i_L flowing as shown in Figure 3.6c.

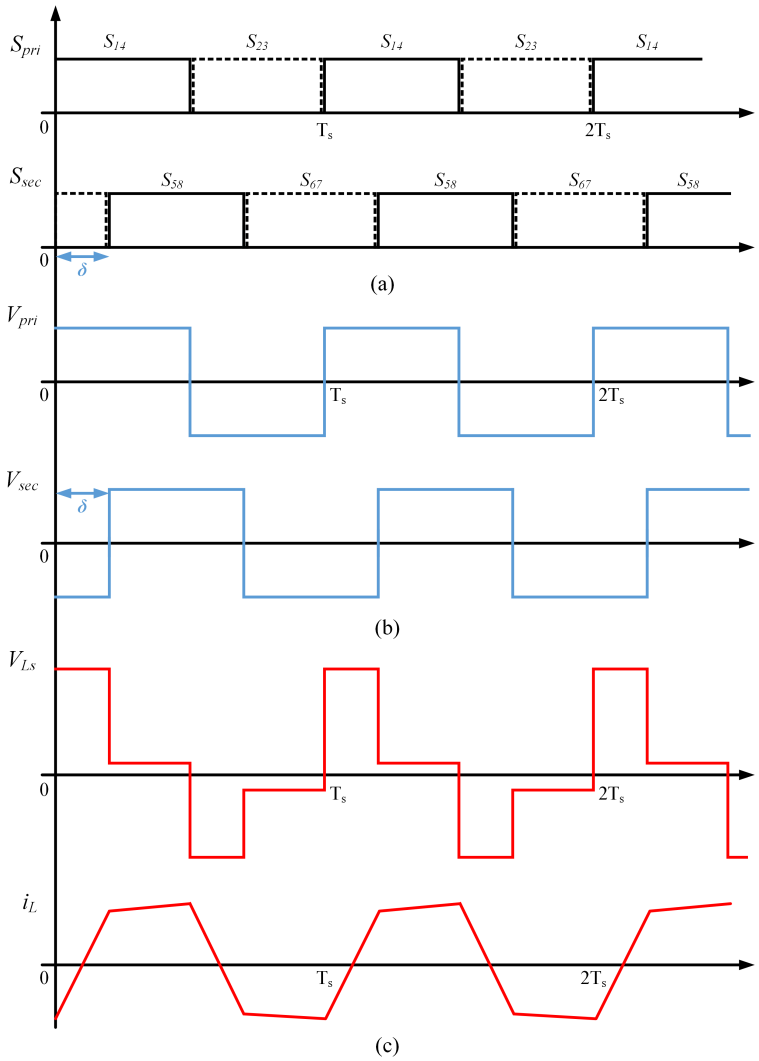


Figure 3.6: (a) Control signals that trigger the switching pairs, (b) Voltage square waves produced by each bridge and (c) Voltage and current across the inductor

This principle can be explained further with the development of equivalent circuits for each switch state during one switching period, as illustrated in Figure 3.7. It is assumed that the power flow is directed from the primary to the secondary bridge and the current is initially flowing through S_1 and S_4 switches. Due to the signal delay by the angle δ, the current is flowing through switches S_6 and S_7 at the secondary bridge. When a control signal is given at switches S_5 and S_8 the current commutates to the latter pair, as shown in Figure 3.7b. The same operating principle is repeated for the other half switching period when S_2 and S_3 are conducting, as illustrated in Figures 3.7c and 3.7d.

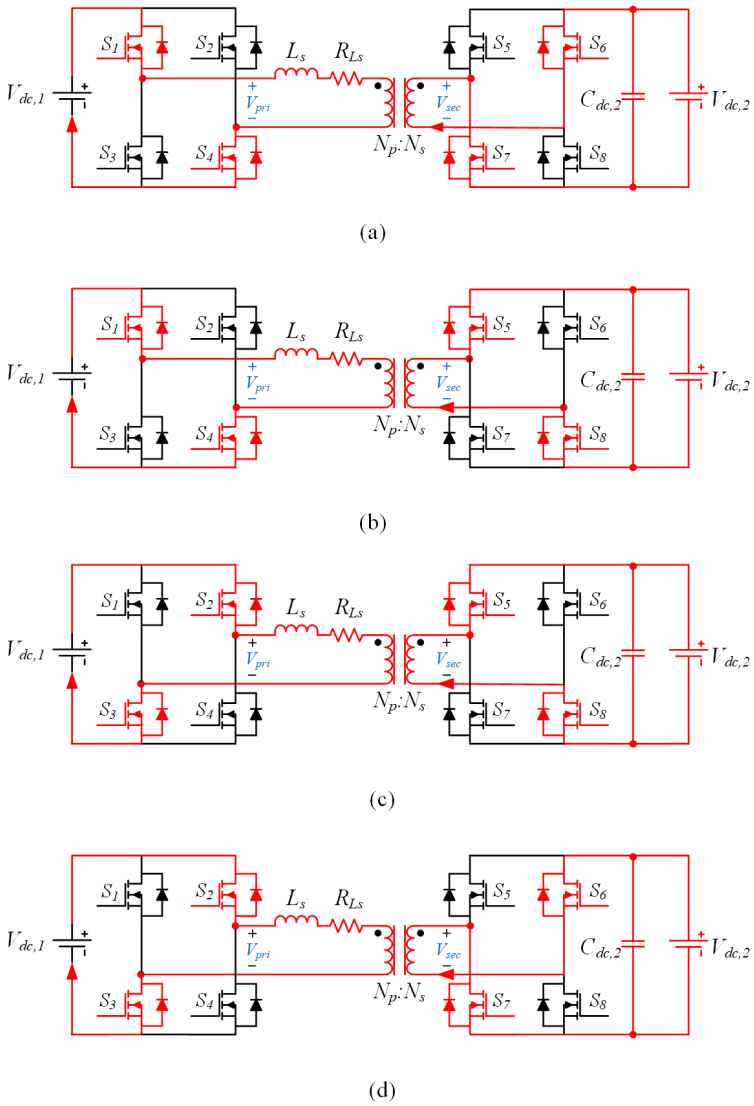


Figure 3.7: Equivalent circuits when (a) S_5 and S_8 are delayed to trigger, (b) S_5 and S_8 are triggered after the phase shift, (c) S_6 and S_7 are delayed to trigger and (d) S_6 and S_7 are triggered after the phase shift

According to the aforementioned analysis, the DC output power of the DAB converter and the phase shift angle are strongly correlated. Considering only the fundamental harmonic of the primary and secondary voltage square waves, the average output power is given by Equation 3.5 [27, 77]:

$$P = \frac{V_1 n V_2}{\omega L_{lk}} \delta (1 - \frac{\mid \delta \mid}{\pi}) \tag{3.5}$$

where, V_1 and V_2 are the primary and secondary voltages respectively, n is the transformer ratio, $\omega = 2\pi f_s$ is the angular frequency and f_s is the switching frequency of the converter, L is the leakage inductance and δ is the phase shift angle in the range of -90 to 90 degrees.

When δ takes a positive value the power flows from the primary to the secondary bridge, otherwise the power flow has the opposite direction [27]. Maximum power transfer can be obtained when the phase shift angle equals ± 90 degrees, while minimum output power is achieved when δ is equal to zero. It should be noted that even though the output power may be zero the current is not zero. Instead it is circulating in the circuit, increasing the losses of the devices [26].

3.1.2.2 Inductor and transformer selection

The size of the inductor depends on the phase shift angle, assuming that the DC bus voltages have fix values and the most suitable switching frequency has been determined 20 kHz. Considering Equation 3.6, L_s can be calculated for maximum power transfer, as follows:

$$L_{s,max} = \frac{V_1 n V_2 \delta_{P_{max}} (1 - \frac{|\delta_{P_{max}}|}{\pi})}{\omega P_{max}} \tag{3.6}$$

A suggested size of the transfer inductance is $0.75...0.85 L_{s,max}$ for an effective control operation [78]. In the present work, $L_s = 0.75 L_{s,max}$ has been considered a sufficient margin for the leakage inductance sizing.

Figure 3.8 shows the relationship between the transfer inductance and angle δ. Assuming $V_1 = V_2 = 700V$ and P_{max} =20 kW, the inductance equals 0.115 mH considering the selected margin mentioned above. This value corresponds to a phase shift angle of 90 degrees or 1.57 rad, where maximum power is transferred.

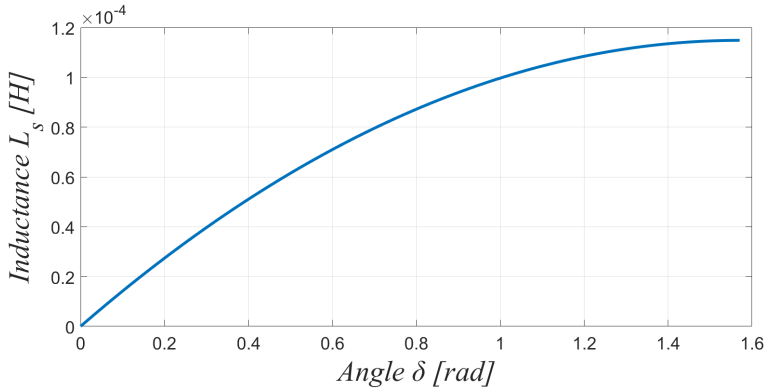


Figure 3.8: Relationship between the transfer inductance and the angle δ

The design of the transformer is out of the scope of this analysis. Therefore, an ideal transformer with turns ratio $n = 1$ has been taken into account for the design and simulation analysis of the converter.

3.1.2.3 Switching devices

The switching devices placed in the two bridges are of the utmost importance when designing the DAB converter. According to the aforementioned, the converter operates at high switching frequency (20 kHz), which results in a lower size of the inductor. In Chapter 2 a comparison between the Si and SiC materials has been considered and the characteristics of different semiconductor devices have been introduced. The SiC MOSFET seems to be the most suitable candidate for the design of the converter, due to its high frequency and voltage capability and reduced amount of losses. Therefore, it is a promising power device for an improved overall performance of the converter.

3.1.2.4 Loss analysis

The total losses in a DAB converter is a combination of the losses on different components. More specifically, the switching and conduction losses of the semiconductor devices along with the transformer and inductor losses need to be taken into account in order to obtain a precise amount of losses. In the present work, though, where the transformer has been considered as an ideal component, and the inductor design is omitted, only the switching and conduction losses have been calculated.

Due to ZVS during the turn-on time, no energy is considered to be lost ($E_{on} = 0$). So, only E_{off} during turn-off time contributes to the switching losses. As a result, the switching losses are the product of the switching energy loss during turn-off and the switching frequency, as follows:

$$P_{sw} = E_{off} f_s \tag{3.7}$$

where $f_s = 1/T_s$

The conduction losses are obtained during the on-state of the device. Calculating the maximum rms on-state current and obtaining the maximum drain-to-source on-resistance from the datasheet the conduction losses per device are given by:

$$P_{cond} = I_{on,rms}^2 R_{DS,on} \tag{3.8}$$

The total losses per MOSFET are, therefore given by:

$$P_{tot} = P_{sw} + P_{cond} \tag{3.9}$$

and the total losses per bridge (four MOSFETs) are equal to:

$$P_{tot,bridge} = 4P_{tot} = 4(P_{sw} + P_{cond}) \tag{3.10}$$

In real applications, the diode is only used during a small fraction of the overall switching cycle (during dead-times). In diodeless operation the reverse current is possible to flow through the MOSFET channel and not through the body diode [41]. In order to calculate the efficiency of the DAB converter in the diodeless operation case the losses of the two bridges are considered as follows:

$$
\begin{aligned}
n(\%) &= \frac{P_{out} - P_{tot,2bridges}}{P_{out}} * 100\% \\
&= \frac{P_{out} - 8(P_{sw} + P_{cond})}{P_{out}} * 100\%
\end{aligned}
\tag{3.11}
$$

3.1.2.5 Thermal equivalent circuit design

When designing the DAB converter it is necessary to regulate the internal temperature (junction temperature) of the switching devices to avoid undesirable effects on the circuit components [36]. Heat must flow through different material layers from the semiconductor to the ambient, as shown in Figure 3.9. An appropriate heatsink is utilized for cooling of the devices and the package is mounted on it.

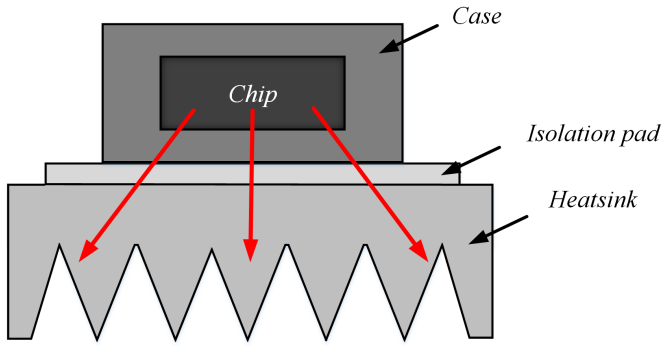


Figure 3.9: Power dissipation in a multilayer structure of one power MOSFET mounted on a heatsink

The power flow per unit time is given by [36]:

$$
P_{cond} = \frac{\lambda A \Delta T}{d} \tag{3.12}
$$

where λ [in W/m^0C] is the thermal conductivity, A [in m^2] is the cross section area, $\Delta T = T_2 - T_1$ is the temperature difference [in ^0C] and d is the length [in m].

Opposing to the flow of heat, the thermal resistance is determined as follows:

$$
R_{\theta,cond} = \frac{\Delta T}{P_{cond}} \tag{3.13}
$$

or considering Equation 3.14:

$$
R_{\theta,cond} = \frac{d}{\lambda A} \tag{3.14}
$$

Considering the thermal resistances of each layer the total thermal resistance from the junction to the ambient (ja) for one semiconductor device is calculated by:

$$R_{\theta,ja} = R_{\theta,jc} + R_{\theta,cs} + R_{\theta,sa} \tag{3.15}$$

where $R_{\theta,jc}, R_{\theta,cs}, R_{\theta,sa}$ are the thermal resistances of the junction-to-case, case-to-heatsink and heatsink-to-ambient respectively.

The resulting junction temperature (T_j) is given by:

$$T_j = P_d(R_{\theta,jc} + R_{\theta,cs} + R_{\theta,sa}) + T_a \tag{3.16}$$

Having calculated the total losses (P_{loss}) of the circuit the junction-to-ambient thermal resistance equals:

$$R_{\theta,ja} = \frac{T_{j,max} - T_{a,max}}{P_{loss}} \tag{3.17}$$

The $R_{\theta,cs}$ can be calculated from the manufacturer's datasheet and, thus, knowing the $R_{\theta,jc}$ and $R_{\theta,cs}$ the $R_{\theta,sa}$ can be determined by Equations 3.15 and 3.17.

In the case of the DAB converter, where eight switching devices are placed in the two bridges, two heatsinks have been considered, one for each bridge. The thermal equivalent circuit for one bridge is then constructed according to the aforementioned assumption, as illustrated in Figure 3.10. The same circuit is considered for the secondary bridge as well.

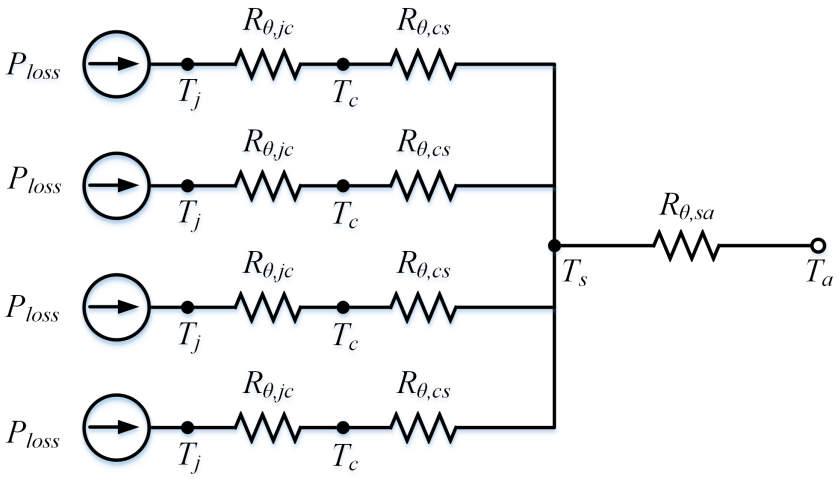


Figure 3.10: Thermal equivalent circuit for the switching devices of one bridge

The thermal resistances of Figure 3.10 can be determined, following a similar process as the aforementioned.

3.2 Control system design

The design of the proper control system for the proposed hybrid system topologies is one of the most challenging parts to deal with. Three different control schemes have been

developed, an MPPT controller to track the MPPT from the photovoltaic system, a phase shift controller for the DAB DC-DC converter and a PI controller for the battery control as shown in Figure 3.11. The MPPT controller gives a voltage reference at the output, which is the V_{max}. This is then compared with the voltage from the PV arrays to give the input to the phase shift controller. The latter generates the gate pulses, necessary to turn on the switching devices. Concerning the battery control, the difference between the reference and actual battery power is the input to a PI controller. A phase shift controller generates the gate pulses for the operation of the switches in DAB converter. The controller models are thoroughly analysed in the following sections.

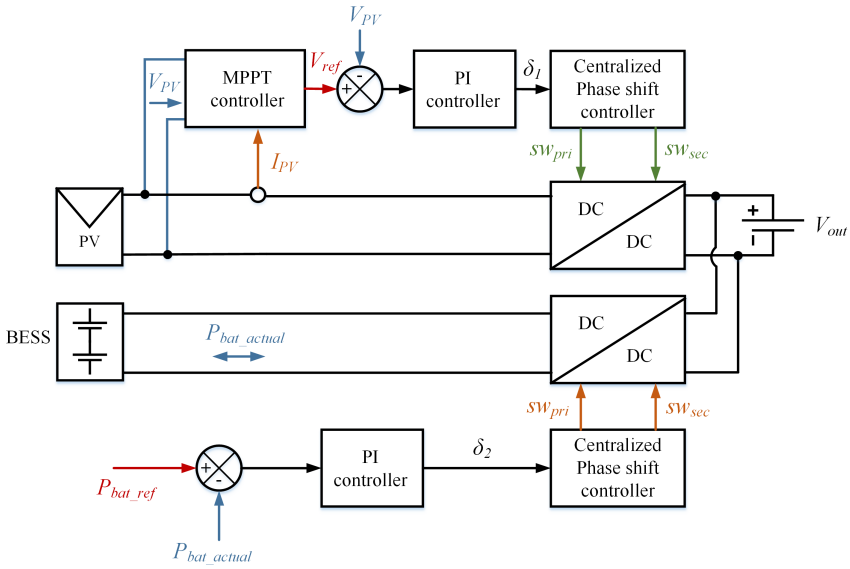


Figure 3.11: System model with the MPPT and phase shift controllers

3.2.1 MPPT controller

The state of art and related work were reviewed, and an identification of the relevant background material were carried out in the project preceding this thesis [24]. No relevant new material was found during the work on the thesis. The presentation from the project report is included below.

One of the major aspects when designing a photovoltaic system is to develop a control algorithm to maximize the power generation of the PV array. The MPPT controller enables the tracking of the Maximum Power Point (MPPT) under various atmospheric and operating conditions. Among the so far proposed PV control schemes [79, 80, 81], two maximum power point tracking algorithms have been mainly implemented; the Perturb and Observe (P&O) and the Incremental Conductance (INC) algorithms [82, 83, 84]. These are widely used control methods due to their accuracy and simplicity when employed in a system compared to the other developed algorithms.

A widely used method due to its simplicity is the P&O algorithm [81, 84]. The operation of this is based on the concept of varying the operating voltage of the photovoltaic device and observing and measuring the results on the PV output power [80, 83]. When $dP/dV > 0$ the operating point is moving towards the maximum power point on the left side and the perturbation remains at the same direction to obtain the MPP, as illustrated in the P-V characteristic of Figure 3.12. On the other hand, when $dP/dV < 0$ the operating point is moving far from the maximum power point on the right side and the perturbation is reversed to obtain the MPP. Finally, when $dP/dV = 0$ the MPP is extracted.

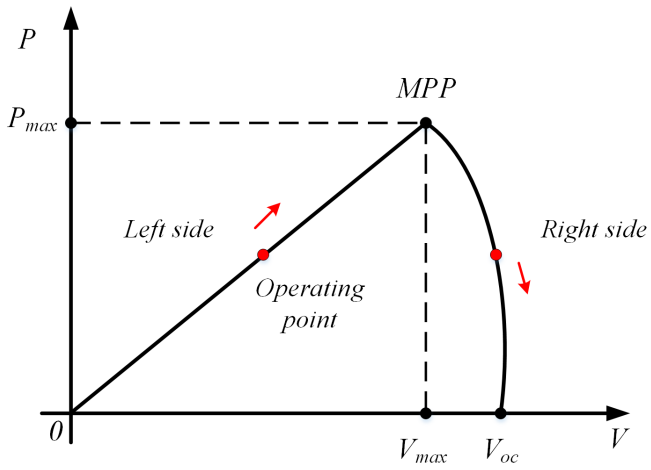


Figure 3.12: P-V characteristic of the photovoltaic array

The INC algorithm is the second commonly used method to control the output of the PV array, due to the fact that it is highly efficient and can be easily implemented [82]. In this concept, the instantaneous conductance ($G_s = I/V$) and incremental conductance ($G_d = dI/dV$) are taken into consideration to obtain the MPP. The two parameters are compared to extract the MPP. When $G_d > G_s$ the operating point is moving towards the MPP, so the perturbation is kept at the same direction. When $G_d < G_s$ the operating point is moving away from the MPP and, therefore, the perturbation is reversed, as shown in Figure 3.12. When $G_d = G_s$ the MPP is obtained [81, 82, 83].

Both algorithms have many inherent advantages compared to other control strategies. However, comparing the two methods, some considerable drawbacks have been found. As far as the P&O algorithm is concerned, defects in the tracking method have been observed. That is, the algorithm is not efficient enough when rabid changes in atmospheric conditions occur and, thus, the MPP tracking is not achieved. More power losses have also been observed. On the other hand, the INC is a more stable and efficient algorithm and is able to track the MPP under various conditions. The probability of obtaining the MPP is very low, though, since almost never $G_d = G_s$ due to oscillations around the MPP. Another important factor is the fact that the INC algorithm is more complex compared to P&O, which increases considerably the computational time [81, 83].

Considering all the aforementioned aspects of the two algorithms, the P&O seems to

be a more efficient method to be implemented, because it is less time consuming and more simple to implement. Therefore, it will be employed in the present work to perform the necessary simulations.

3.2.2 Control of DAB converter

The state of art and related work were reviewed, and an identification of the relevant background material were carried out in the project preceding this thesis [24]. No relevant new material was found during the work on the thesis. The presentation from the project report is included below.

Control strategy for the DAB DC-DC converter is one of the most challenging parts of the converter design. Extensive research has been conducted towards the most suitable control method and, thus, a variety of control schemes has been proposed so far. Among these, the phase shift modulation (PSM) is the commonly used method, and, in particular, the single phase shift modulation (SPSM) scheme [53, 85, 86], due to its simplicity, low inertia and high dynamic [85].

In this control scheme, only the phase shift angle between the primary and secondary voltages is necessary to be controlled [87]. The switch pairs of the two bridges that are cross-connected are switched in turn to produce square waves with constant duty cycle of 50 % at the transformer's terminals. These waves can be appropriately phase-shifted to control the power that is delivered from the leading to the lagging bridge. More specifically, by regulating the phase shift angle between the primary and secondary voltages of the transformer the voltage across the leakage inductance changes and, thus, the amplitude and the direction of power flow is controlled.

Although SPSM method is widely used to control the DAB converter, there are challenges that are to be faced. Seeing that the power flow control depends on the leakage inductance, large power circulating currents can be developed in the converter when the primary and secondary voltage magnitudes are not matched [85, 86]. Furthermore, there has been observed a inrush current at the beginning of the converter operation due to zero voltage at the secondary side. Thus, at turn-on, the entire input voltage appears on the inductor causing this inrush current to flow [88]. Another challenge that is to be tackled is the ZVS maintenance during the operation of the converter under the whole power range [85, 86]. Due to these disadvantages of the SPSM scheme, other control strategies have been proposed, such as the dual phase shift, triple phase shift and hybrid phase shift modulation scheme [53, 85, 86, 87, 89]. These control schemes are typically improved methods of the SPSM and are more beneficial compared to the latter. The sophisticated design of the controller, though, impedes the broad implementation of these control schemes. In the present work, the SPSM has been utilized for the control of DAB DC-DC converter, which is analysed in the following sections.

3.2.2.1 Dynamic modelling

Dynamic modelling of the DAB converter has been thoroughly investigated [53, 77] in order to obtain accurate transfer functions of the converter in a simple way. The proposed strategy, called harmonic modelling, develops an accurate model of the converter's dynamics based on Fourier analysis of the switching functions in the time domain. To do

this, the output voltage waveforms of the primary and secondary bridge (V_{pri}, V_{sec}) and the output current are derived in terms of the switching functions, as shown below.

Assuming one H-bridge, e.g. the primary bridge, the behaviour of the switches is investigated to obtain the output voltage. The switches of each leg operate complimentary to each other, as illustrated in Figure 3.13 and a truth table can be formed to summarize the four states of the H-bridge (Table 3.1).

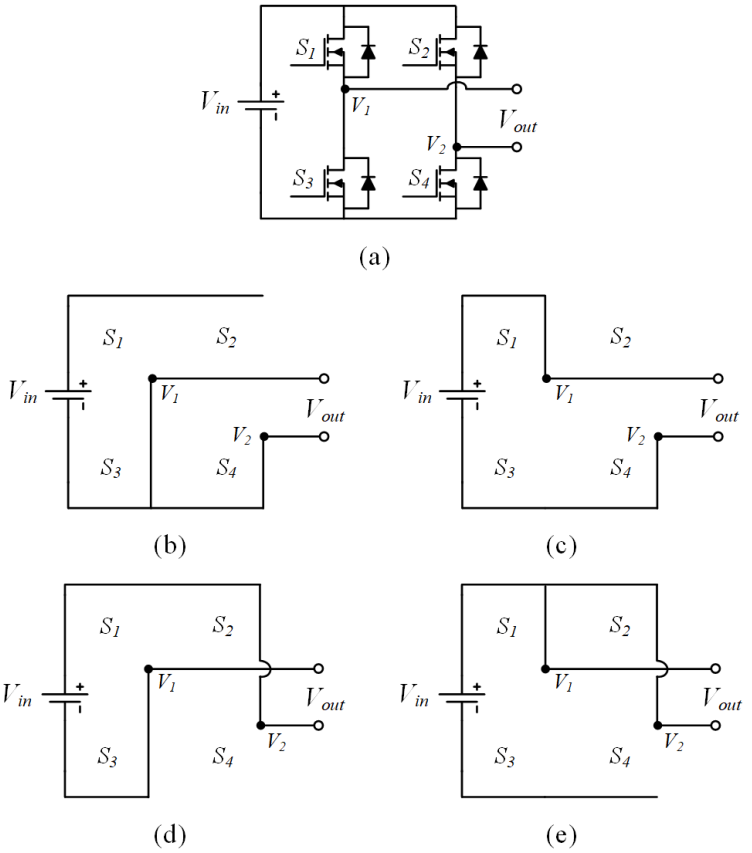


Figure 3.13: Switch states of the primary H-bridge

Table 3.1: Truth table of the primary H-bridge

Switch State		Output Voltage		
S_1	S_2	V_1	V_2	V_{out}
0	0	0	0	0
1	0	V_{in}	0	V_{in}
0	1	0	V_{in}	-V_{in}
1	1	V_{in}	V_{in}	0

It can be observed that the output voltage is the difference between the voltages at V_1 and V_2 points and, depending on the switch state, the output voltage of the bridge equals V_{in}, -V_{in} or zero. The same analysis can be carried out for the secondary bridge as well and the primary and secondary voltages are derived in the time domain by Equations 3.18 and 3.19.

$$V_{pri}(t) = V_{in}(t) * \{S_1(t) - S_2(t)\} \tag{3.18}$$

$$V_{sec}(t) = V_{out}(t) * \{S_5(t) - S_6(t)\} \tag{3.19}$$

The dynamics of the output voltage at the capacitor are of the utmost importance. Considering the schematic diagram of Figure 3.14, KCL (Kirchhoff's Current Law) can be applied at the secondary bridge and, thus, Equation 3.20 is derived:

$$i_C(t) = i_{dc}(t) - i_{out}(t) \tag{3.20}$$

where $i_C(t) = C * \frac{dV_{out}(t)}{dt}$ is the current that flows through the capacitor, $i_{dc}(t)$ is the current at the output of the secondary bridge and $i_{out}(t)$ is the load current that can be obtained by measurement. The injected current from the secondary bridge, though, depends on the state of S_5 and S_6 switches and the current through the inductor, i_L. By forming the truth Table 3.2, the $i_{dc}(t)$ current is obtained and is given in Equation 3.21:

$$i_{dc}(t) = i_L(t) * \{S_5(t) - S_6(t)\} \tag{3.21}$$

Table 3.2: Truth table to obtain i_{dc} current

Switch State		Output Current
S_5	S_6	i_{dc}
0	0	0
1	0	i_L
0	1	-i_L
1	1	0

By applying the Kirchhoff's Voltage Law (KVL) at the inner loop of the converter, as shown in Figure 3.14, the inductor current can be determined in the time domain. Equation 3.22 describes the time dependent voltages at the inner loop.

$$V_{pri}(t) - Ls * \frac{di_L(t)}{dt} - i_L(t) * R_{Ls} - \frac{N_p}{N_s} * V_{sec} = 0 \tag{3.22}$$

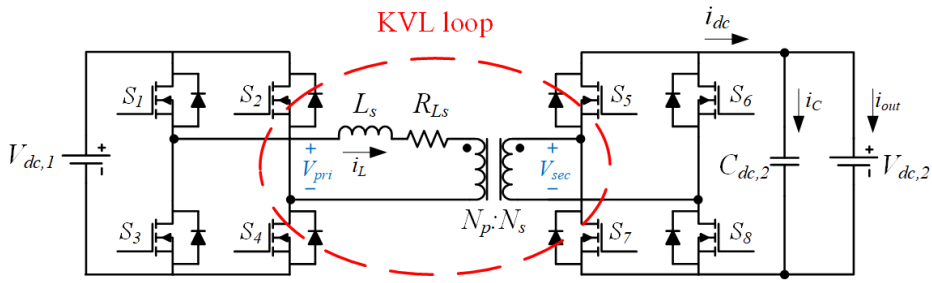


Figure 3.14: The KVL inner loop of the converter

Inserting Equations 3.18 and 3.19 into Equation 3.22 and rearranging, an expression of the output voltage in terms of the switching states and the leakage inductance is given by Equation 3.23.

$$\begin{aligned} Ls * \frac{di_L(t)}{dt} + i_L(t) * R_{Ls} = V_{in}(t) * \{S_1(t) - S_2(t)\} \\ - \frac{N_p}{N_s} * V_{out}(t) * \{S_5(t) - S_6(t)\} \end{aligned} \tag{3.23}$$

This non-linear dynamic equation of the DAB converter can be solved by Fourier analysis of the switching functions. That is, the initially binary-valued square-wave switching signals can be represented by a series of sinusoids [36, 90], according to Equation 3.24 [90], and these continuous time functions can be implemented to the dynamic equations of the converter.

$$S_k(t) = \frac{1}{2} + \frac{2}{\pi} \sum_{n=0}^{N} \frac{sin([2n+1]\{\omega_s t - \alpha_k\})}{[2n+1]}, \; N \geq 0, \; k = 1, 2, 3, ... \tag{3.24}$$

where ω_s=2πf_s is the angular switching frequency, α_k is the phase angle delay of the square wave and N is the number of harmonics of the switching functions. Figure 3.15 illustrates the square wave, considering the 1^{st}, 3^{rd}, 5^{th} and 7^{th} harmonics. If a higher number of harmonics is taken into account in the summation, the square wave would be represented in a better way.

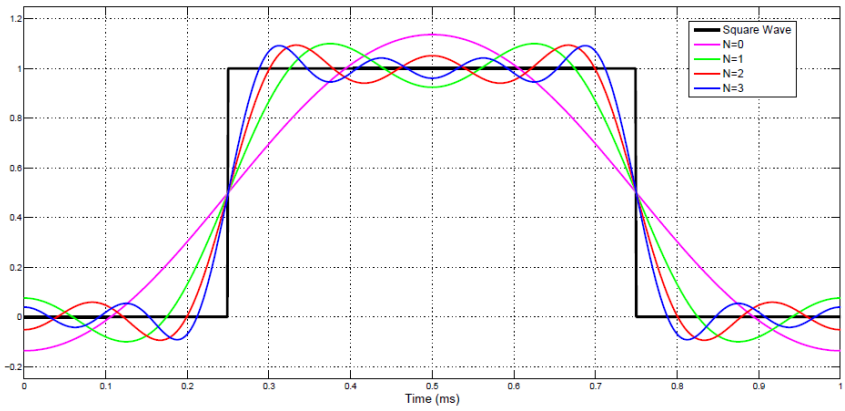


Figure 3.15: Square wave considering the fundamental, 3rd, 5th and 7th order harmonics [77]

Based on Equation 3.24 and assuming that S_1 is the reference phasor the switching functions for S_1, S_2, S_5 and S_6 switches are given by the following equations:

$$S_1(t) = \frac{1}{2} + \frac{2}{\pi}\sum_{n=0}^{N}\frac{sin([2n+1]\{\omega_s t\})}{[2n+1]},\ N \geq 0,\ k = 1,2,3,... \tag{3.25}$$

$$S_2(t) = \frac{1}{2} + \frac{2}{\pi}\sum_{n=0}^{N}\frac{sin([2n+1]\{\omega_s t - \pi\})}{[2n+1]},\ N \geq 0,\ k = 1,2,3,... \tag{3.26}$$

$$S_5(t) = \frac{1}{2} + \frac{2}{\pi}\sum_{n=0}^{N}\frac{sin([2n+1]\{\omega_s t - \delta\})}{[2n+1]},\ N \geq 0,\ k = 1,2,3,... \tag{3.27}$$

$$S_6(t) = \frac{1}{2} + \frac{2}{\pi}\sum_{n=0}^{N}\frac{sin([2n+1]\{\omega_s t - \delta - \pi\})}{[2n+1]},\ N \geq 0,\ k = 1,2,3,... \tag{3.28}$$

Substituting the switching functions into Equation 3.23 the inductor current is given in Equation 3.29:

$$i_L(t) = \frac{4}{\pi}\sum_{n=0}^{N}\left\{\frac{1}{[2n+1]}\left[\frac{V_{in}(t)}{\mid z_n \mid}sin([2n+1]\omega_s t - \phi)\right.\right. \tag{3.29}$$
$$\left.\left. - \frac{N_p}{N_s}\frac{V_{out}(t)}{\mid z_n \mid}sin([2n+1](\omega_s t - \delta) - \phi)\right]\right\}$$

where $\mid z_n \mid = \sqrt{R_{Ls}^2 + ([2n+1]\omega_s L_s)^2}$ is the magnitude and $\phi = tan^{-1}(\frac{[2n+1]\omega_s L_s}{R_{Ls}})$ is the angle of the series impedance.

By inserting $i_L(t)$ into Equation 3.21, the $i_{dc}(t)$ current can be calculated, which then gives the simplified expression of $i_C(t)$ from Equation 3.20, as follows:

$$i_C(t) = \frac{8}{\pi^2}\frac{N_p}{N_s}\sum_{n=0}^{N}\left\{\frac{1}{[2n+1]^2}\left[\frac{V_{in}(t)}{\mid z_n \mid}cos([2n+1]\delta-\phi)\right.\right. \\ \left.\left. - \frac{N_p}{N_s}\frac{V_{out}(t)}{\mid z_n \mid}cos(\phi)\right]\right\} - i_{out}(t) \tag{3.30}$$

Therefore, the non-linear model of the output voltage dynamics is given by:

$$\frac{dV_{out}(t)}{dt} = \frac{i_C(t)}{C} = \frac{8}{C\pi^2}\frac{N_p}{N_s}\sum_{n=0}^{N}\left\{\frac{1}{[2n+1]^2}\left[\frac{V_{in}(t)}{\mid z_n \mid}cos([2n+1]\delta-\phi)\right.\right. \\ \left.\left. - \frac{N_p}{N_s}\frac{V_{out}(t)}{\mid z_n \mid}cos(\phi)\right]\right\} - \frac{i_{out}(t)}{C} \tag{3.31}$$

Linearization of this model is the next step. Based on small-signal analysis [91], a steady-state operating point is specified (V_{out_0}, δ_0, i_{out_0}) and partial differential equations are developed to describe the converter output voltage response under small variations in phase shift (approximately 5%) and output current around this operating point. Therefore, Equation 3.32 is derived:

$$\frac{d(V_{out_0}+\Delta V_{out_0}(t))}{dt} \approx f(V_{out_0},\delta_0,i_{out_0}) \\ + \frac{\theta f}{\theta V_{out}}\bigg|_0 \Delta V_{out}(t) + \frac{\theta f}{\theta i_{out}}\bigg|_0 \Delta i_{out}(t) + \frac{\theta f}{\theta \delta}\bigg|_0 \Delta\delta \tag{3.32}$$

A linearized model for the output voltage rate of change can eventually be developed, as follows:

$$\frac{d\Delta V_{out}(t)}{dt} = A\Delta V_{out} + B_\delta \Delta\delta + B_I \Delta i_{out} \tag{3.33a}$$

$$A = -\frac{8}{C\pi^2}\left(\frac{N_p}{N_s}\right)^2 \sum_{n=0}^{N}\frac{cos\phi}{[2n+1]^2 \mid z_n \mid} \tag{3.33b}$$

$$B_\delta = \frac{8V_{in}}{C\pi^2}\frac{N_p}{N_s}\sum_{n=0}^{N}\left\{\frac{sin(\phi-[2n+1]\delta_0)}{[2n+1] \mid z_n \mid}\right\} \tag{3.33c}$$

$$B_I = -\frac{1}{C} \tag{3.33d}$$

where A and B_I are constants of the model, while B_δ changes with the input phase shift.

3.2.2.2 Closed loop control

Closed loop control is necessary in power converters to ensure a stable operation of the system under load or reference variations. Two main closed loop strategies have been identified, the non-linear and linear, with the latter being the most popular when regulating DC-DC bidirectional converters [77]. In linear controllers, the variable that needs to be controlled is selected at first, then the appropriate control loop is designed and, finally, the regulator part is structured.

In DAB DC-DC converter the output voltage of the system is to be controlled to be able to track the reference voltage under various operating conditions. As for the control loop, a single-loop feedback controller is the most attractive candidate to be employed in the converter. This is because this control system is utilized mainly in Single Input Single Output (SISO) systems, like the DAB converter, which has one input state (angle δ) and one output state (V_{out}). A schematic diagram of the closed loop control system is shown in Figure 3.16. This simple loop design consists of a plant or converter model ($G(s)$) that needs to be controlled and the controller ($C(s)$), which varies the phase shift angle δ in a way that the plant output voltage will be able to track the reference voltage (V_{ref}). The output voltage sample is compared to V_{ref} and an error signal is generated which feeds the controller. The design of the regulator aims at eliminating the error between the compared voltages, ideally to zero.

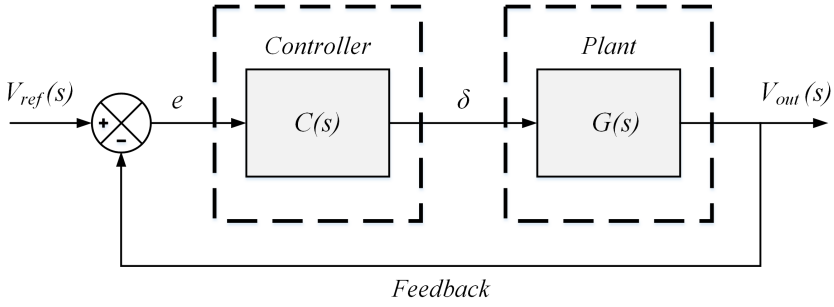


Figure 3.16: Closed loop block diagram of the converter

The simplest and commonly used regulators in bidirectional DC-DC converters are the Proportional-Integral (PI) controllers because they produce zero steady state error [26, 92]. They are characterized by a proportional gain (K_p), which regulates the speed of the controller and an integral gain (K_i) to eliminate the error. The transfer function of the PI controller is given by the following equation:

$$C(s) = K_p + \frac{K_i}{s} \tag{3.34}$$

In order to obtain the transfer function of the converter model, Equation 3.33 is considered. Initially, the output current disturbance is assumed negligible and, after using Laplace transformation, Equation 3.35 arises:

$$\Delta V_{out}(s - A) = B_\delta \Delta\delta \tag{3.35}$$

The transfer function of the plant is then equal to:

$$G(s) = \frac{B_\delta}{s - A} \tag{3.36}$$

Having derived the controller and plant transfer functions, the function of the closed loop system can now be determined as follows:

$$F(s) = C(s)G(s) = \left(K_p + \frac{K_i}{s}\right)\left(\frac{B_\delta}{s - A}\right) \tag{3.37}$$

3.2.2.3 Digital controller

Modern power electronics require the implementation of digital closed loop controllers using microprocessors, such as Digital Signal Processors (DSP). The PI controller described in the previous section cannot be implemented unless it is represented as a discrete time controller. The connection between the continuous time domain (plant) and the discrete time domain (digital controller) can be done by the employment of Analog-to-Digital Converter (ADC). Its main operation is to take samples of the continuous time plant and create a discrete time model. A commonly used sampling method is the Zero Order Hold (ZOH) approximation, which holds a sample for one interval until the next sample is obtained [93].

In order to derive the discrete PI controller, the conversion is first performed on the Proportional-Integral-Derivative (PID) controller and then it is simplified to the PI. The transfer function of the PID controller is given by:

$$PID(s) = K_p + \frac{K_i}{s} + K_d s \tag{3.38}$$

where K_d is the derivative gain. The derivative term is commonly modified to a low pass filter (LPF) of order N to reduce the noise and, thus, Equation 3.39 arises:

$$PID(s) = K_p + \frac{K_i}{s} + \frac{NK_d}{1 + \frac{N}{s}} \tag{3.39}$$

Both the integral and derivative terms are converted to their discrete counterparts by Z-transform. Applying the backward Euler method [93] and for a given sampling time, T_s, the discrete form of integral and derivative terms are respectively:

$$\frac{K_i}{s} \longleftrightarrow \frac{K_i T_s z}{z - 1} \tag{3.40a}$$

$$\frac{NK_d}{1 + \frac{N}{s}} \longleftrightarrow \frac{NK_d(z - 1)}{(1 + NT_s)z - 1} \tag{3.40b}$$

Equation 3.39 is now equal to:

$$PID(z) = K_p + \frac{K_i T_s z}{z - 1} + \frac{NK_d(z - 1)}{(1 + NT_s)z - 1} \tag{3.41}$$

Although a discrete time PID controller is obtained in 3.29, further modification is necessary to derive the difference equation in order to implement it in the DSP code. Therefore, another format of the transfer function is introduced in Equation 3.42 and after mathematical calculations [90, 94] the PID error-to-control variable transfer function is given by:

$$PID(z) = \frac{\delta(z)}{e(z)} = \frac{b_0 + b_1 z^{-1} + b_2 z^{-2}}{a_0 + a_1 z^{-1} + a_2 z^{-2}}, \tag{3.42a}$$

$$b_0 = K_p(1 + NTs) + K_i T_s(1 + NTs) + NK_d \tag{3.42b}$$

$$b_1 = -[K_p(2 + NTs) + K_i T_s + 2NK_d] \tag{3.42c}$$

$$b_2 = K_p + NK_d \tag{3.42d}$$

$$a_0 = 1 + NT_s \tag{3.42e}$$

$$a_1 = -(2 + NT_s) \tag{3.42f}$$

$$a_2 = 1 \tag{3.42g}$$

Rearrangement of 3.42 gives:

$$\begin{aligned}\delta(z) = &-\frac{\alpha_1}{\alpha_0}\delta(z)z^{-1} - \frac{\alpha_2}{\alpha_0}\delta(z)z^{-2} + \frac{b_0}{\alpha_0}e(z) \\ &+ \frac{b_1}{\alpha_0}e(z)z^{-1} + \frac{b_2}{\alpha_0}e(z)z^{-2}\end{aligned} \tag{3.43}$$

Finally, the expression of the required difference equation is given by 3.44, according to [90]:

$$\begin{aligned}\delta[k] = &-\frac{\alpha_1}{\alpha_0}\delta[k-1] - \frac{\alpha_2}{\alpha_0}\delta[k-2] + \frac{b_0}{\alpha_0}e[k] \\ &+ \frac{b_1}{\alpha_0}e[k-1] + \frac{b_2}{\alpha_0}e[k-2]\end{aligned} \tag{3.44}$$

The control signal of the PI controller is the input reference to a digital modulator. The latter is responsible for producing the signals for the turn-on and turn-off states of the converter switches. In the present work a two-level phase-shifted square wave (PSSW) block modulation strategy has been applied to the converter. This scheme comprises pulses of high frequency and 50 % duty ratio that are applied to each phase leg of one bridge and the difference between them appears on the output voltage of the bridge. Each reference signal is compared to a triangular carrier waveform to produce the gate signals. These are generated at the crossing points of the two waveforms (carrier and reference), as shown in Figure 3.17.

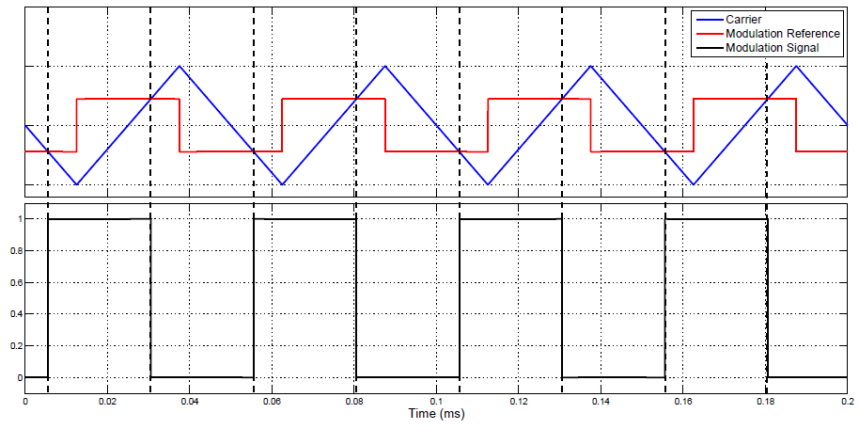


Figure 3.17: The PSSW modulator [77]

3.2.3 Control of BESS

Battery energy storage systems play a crucial role in the optimal operation of the photovoltaics. It is, therefore, necessary to develop a power management control strategy that enables the efficient charging and discharging of the batteries along with the PVs and the continuous power supply to the dc loads. For that reason, a dc load connected to the MVDC grid has been considered in all the aforementioned scenarios to validate the performance of the hybrid systems. When the PV power is higher that the load demand, the solar power is transferred to the load and the excess of power is utilized to charge the battery. In the case that the load requires more power than that produced by the PVs, the battery provides the extra power needed and, therefore, it is discharged.

The control strategy for the battery-DAB converter operation is shown in Figure 3.18. The battery power reference, $P_{bat,ref}$, is determined by the difference between the load demand and the solar power. This signal is compared with the actual battery power, $P_{bat,actual}$, and the error passes through a PI controller to obtain the phase shift angle φ in high precision. The phase shift controller varies the angle such that the output power is able to track the reference value. The same single phase shift modulation strategy analysed in the previous subsection has been applied to control the battery DAB converter.

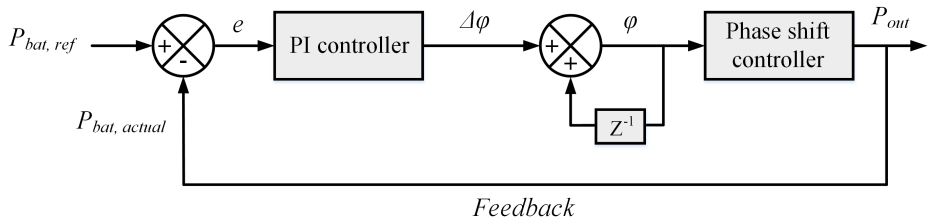


Figure 3.18: Schematic diagram of the battery-DAB converter control model

Chapter 4

Modelling of the Systems

All the system models have been developed in PLECS simulation software and are represented in the present chapter. Both the electrical and thermal models of the converters have been investigated and developed for the centralized scenario. Each full bridge of the converters consists of four 1.2-kV class, 90 A current rating SiC MOSFETs (Wolfspeed C2M0025120D, TO-247-3 package) [95], which are mounted on the same heatsink. The manufacturer's datasheet can be found in the Appendix. The most proper selection of heatsink was found to be the LAM 5 D K 100 24 by Fischer Elektronik [96]. The transformers are considered ideal with transformation ratio 1:1. Finally, the selected PV module in both cases is the multicrystal KC200GT Kyocera model [97], whose datasheet is found in the Appendix. The models are thoroughly analysed in the following sections.

4.1 Modelling of the centralized scenario

Figure 4.1 illustrates the electrical model of the under study system. Three identical DAB converters, have been developed, parallel connected at the input and in series at the output. The same structure has been considered both for the PV and the battery integration to the MVDC grid. The BESS system and the MVDC network are modelled with a constant voltage source.

Table 4.1 summarizes the design and operating parameters of the under-study system. Each modularized converter is designed with a nominal power of 60 kW. The MVDC grid is assumed to have a voltage level of 2.1 kV.

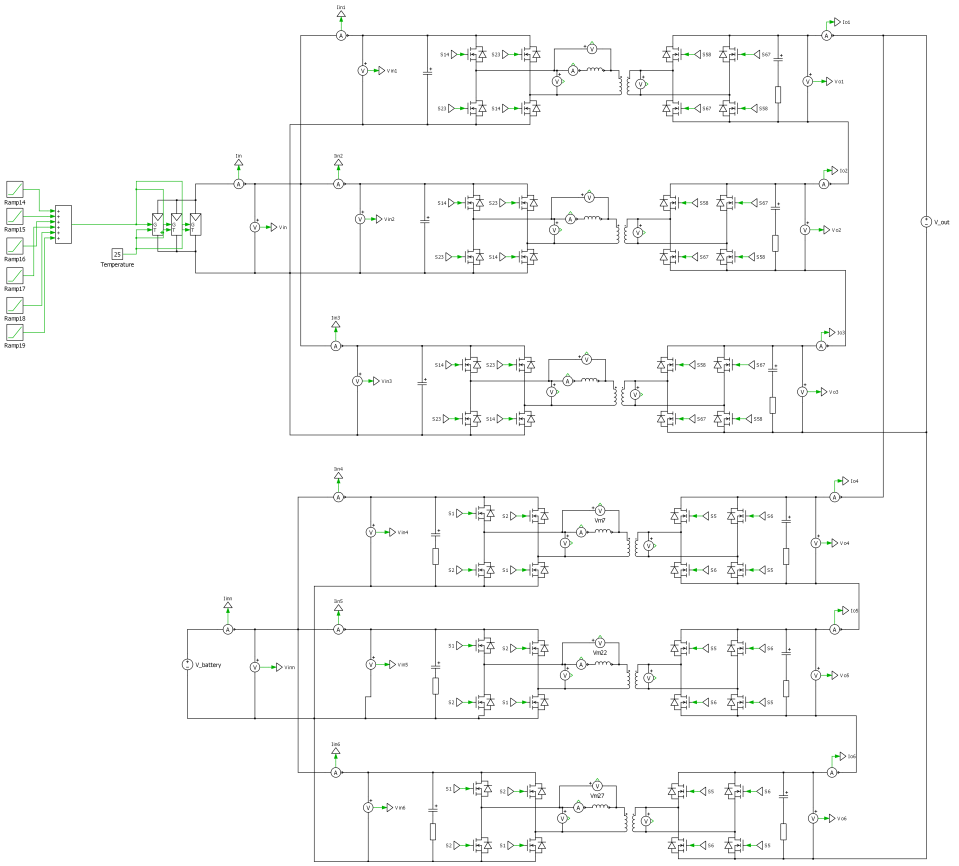


Figure 4.1: Electrical model for the centralized scenario developed in PLECS

Table 4.1: Parameters of the simulation model

Circuit parameters	
Number of PV modules in series	27
Number of PV module strings in parallel	12
Maximum PV module voltage	26.3 V
Maximum PV module power	200 W
Power rating per DAB block, P	20 kW
Input/output voltage rating per converter, V_{dc1}, V_{dc2}	700 V_{dc}
Switching frequency, f_s	20 kHz
Leakage inductance per converter, L_s	0.115 mH
Transformer turns ratio	1:1
Input filter capacitor per converter, C_{dc1}	300 μF
Input filter inductance per converter, L_{dc1}	3 μH
Output filter capacitor per converter, C_{dc2}	300 μF

As analyzed in Chapter 3, three different control schemes have been implemented to the system to ensure the optimal operation of the PVs, batteries and DAB converters. Figures 4.2 and 4.3 illustrate the MPPT controller and the phase shift controller implemented for the modularized DAB converter connected to the PV system. For the digital controller, in particular, the calculation of the controller gains (K_p, K_i) is out of the scope of this work and, thus, the optimal selection of the gains is based on trial and error method.

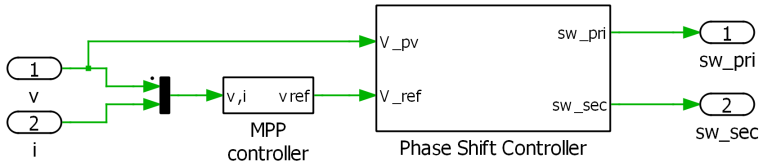


Figure 4.2: MPPT and phase shift controller

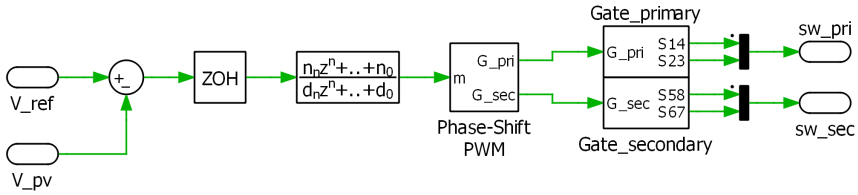


Figure 4.3: The phase shift controller of PV converter system

The output of the PI controller is the reference to the digital modulator in order to produce the gate signals. A detailed model of the PSSW modulation scheme has been developed in PLECS and is shown in Figure 4.4.

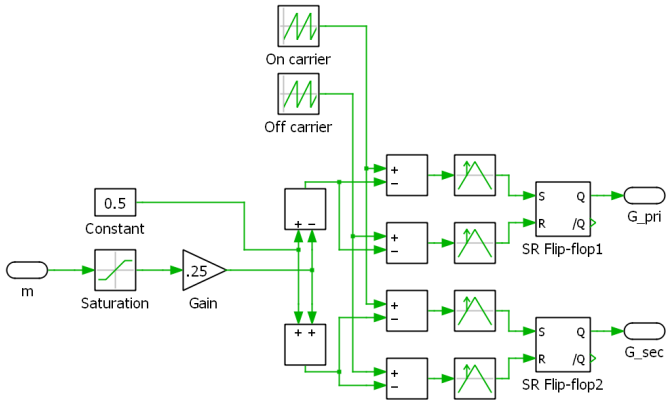


Figure 4.4: The PSSW modulation scheme developed in PLECS

Figures 4.5 and 4.6 show the BESS converter control scheme. In order to verify the

performance of the system a stochastic daily load profile is considered, which is simulated with a number of ramps in PLECS. More details about the load profile are mentioned in Chapter 5. The reference power to the BESS control scheme is the difference between the power demand at the output and the PV power generation. A comparison between the reference and actual battery power is made and through a PI controller the delay angle is obtained. This in the input to the phase shift modulator of Figure 4.4 to generate the gate signals of the switches.

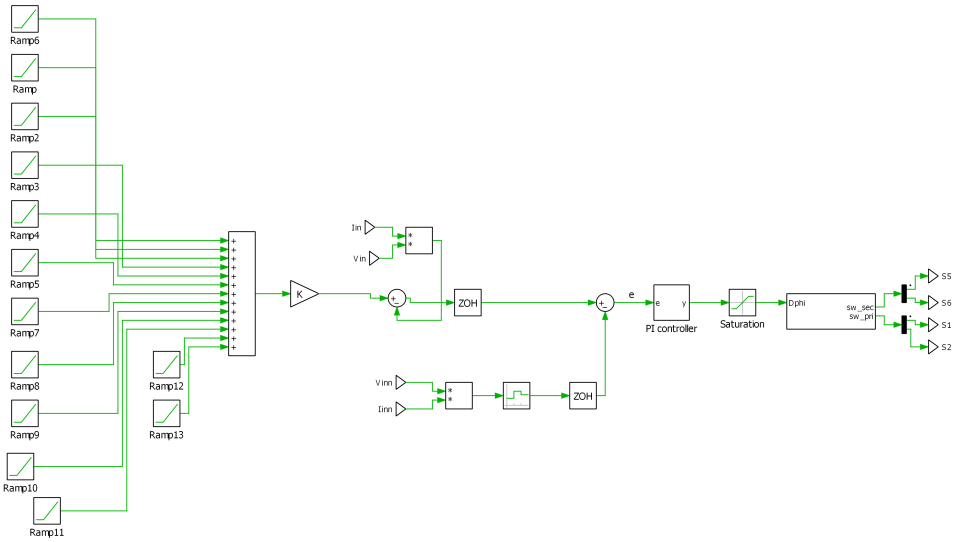


Figure 4.5: The battery control scheme as developed in PLECS

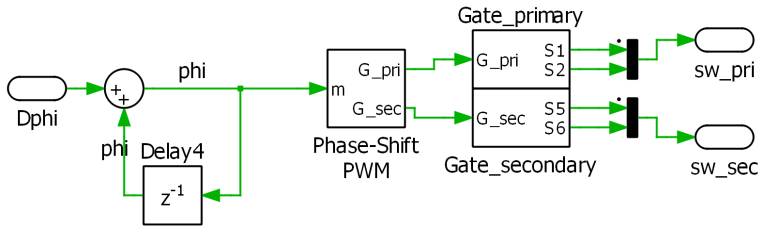


Figure 4.6: The phase shift controller of battery converter system

The thermal model of the converter has been developed based on the assumption that the four MOSFETs of each bridge are mounted on the same heatsink as mentioned above. The thermal specifications of the MOSFETs were available on the PLECS, according to manufacturer's datasheet and were loaded onto the electrical model. Figure 4.7 shows the thermal model that was initially developed. However, due to the large amount of data loaded with this method, the simulations ran very slow and, therefore, a different thermal design was necessary.

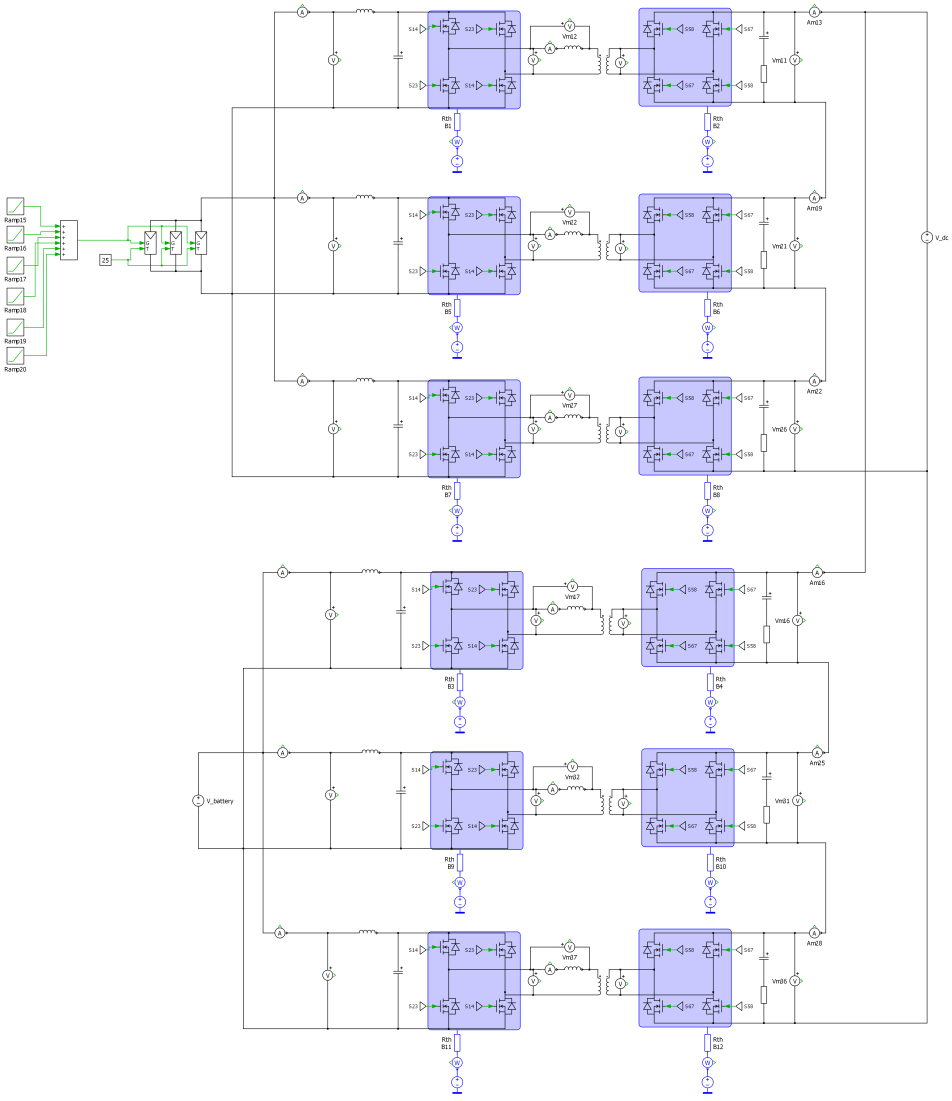


Figure 4.7: Initial thermal model of the modularized converters applied to PV-BESS hybrid system

The analysis in Chapter 3 about the thermal equivalent design of a MOSFET was taken into consideration in order to develop the thermal model in PLECS. More specifically, at steady state each MOSFET can be represented as a circuit consisting of a heat source and a series connection of thermal resistances. Considering that four MOSFETs are mounted on the same cooling device, the dynamic thermal models with thermal resistances, R_{th}, and thermal capacitances, C_{th}, to obtain the temperature variations (ΔTs) have been developed, as shown in Figures 4.8 and 4.9. Seeing that all the switching devices are identical, the thermal design of one converter has been considered (one converter connected to the PVs and one connected to the BESS).

According to these figures, the heat source corresponds to the total losses in a MOSFET, i.e. the conduction and switching losses. The RMS current is given by the electrical simulations, as indicated in Figure 4.10 for one MOSFET, and the on resistance is given from the datasheet for a maximum junction temperature of 100^0C. Therefore, the conduction losses are determined, according to Figure 4.12b. More specifically, a look-up table with the rms current and time values is used and then the square of the current is calculated. A second look-up table is considered with the on resistance and junction temperature values. The outputs of them are multiplied and the conduction losses are determined.

As for the switching losses, the current that flows through the MOSFETs is given by the electrical simulations. This waveform is plotted in Matlab in order to extract the upper envelope of the waveform, i.e. the maximum current values, as shown in Figure 4.11. A look-up table with these data and the time data is formed, according to Figure 4.12a, and is further used to obtain the turn-off energy (E_{off}) from the datasheet. These values correspond to the maximum current, while the turn-on energy (E_{on}) is considered zero due to the ZVS condition. Another look-up table with these data is formed and its output is multiplied with the 20 kHz switching frequency (Table 4.1) to calculate the switching losses for one MOSFET. The same process is followed for all the switching devices of the bridges.

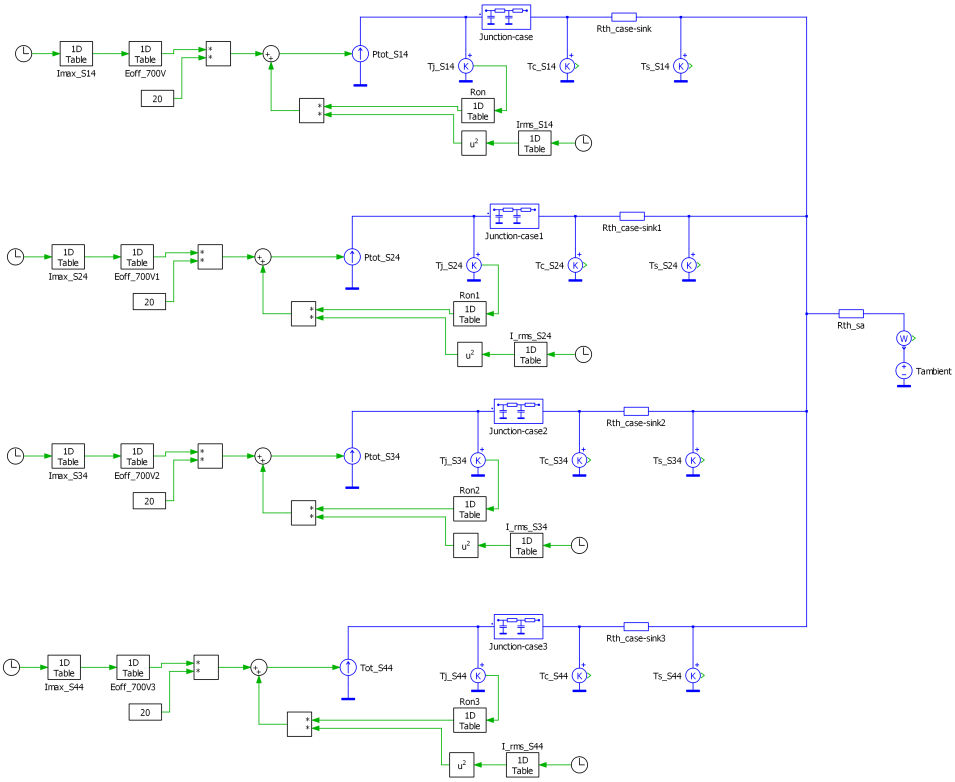


Figure 4.8: Thermal equivalent of one full bridge circuit employed in the PV-DAB converter MOSFETs

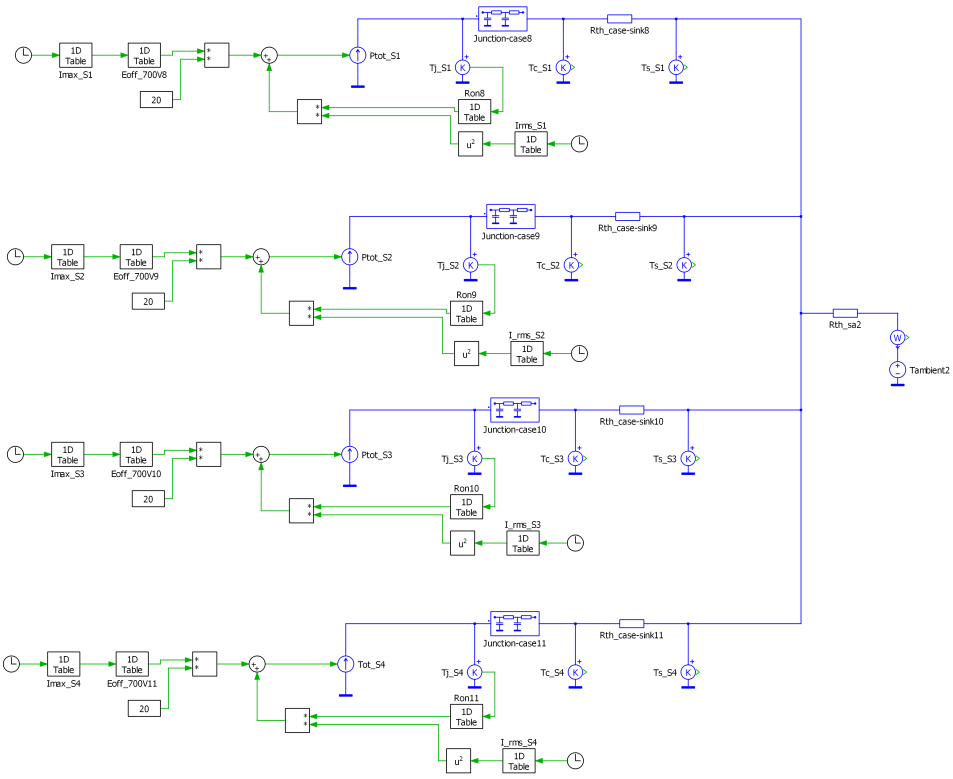


Figure 4.9: Thermal equivalent of one full bridge circuit employed in the BESS-DAB converter MOSFETs

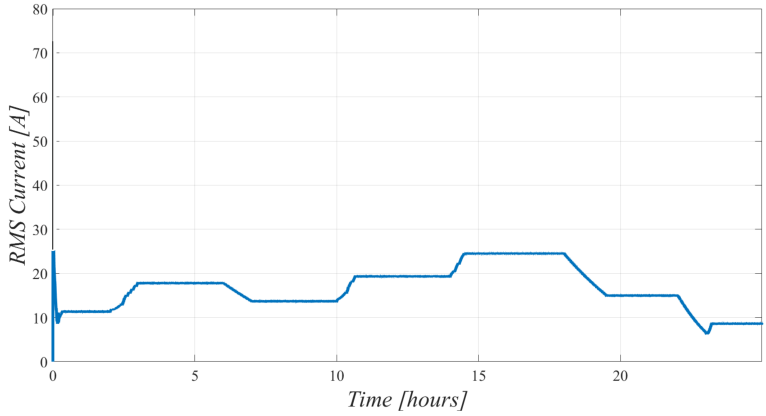


Figure 4.10: The RMS value of the current flowing through one MOSFET. These values are used to calculate the conduction losses

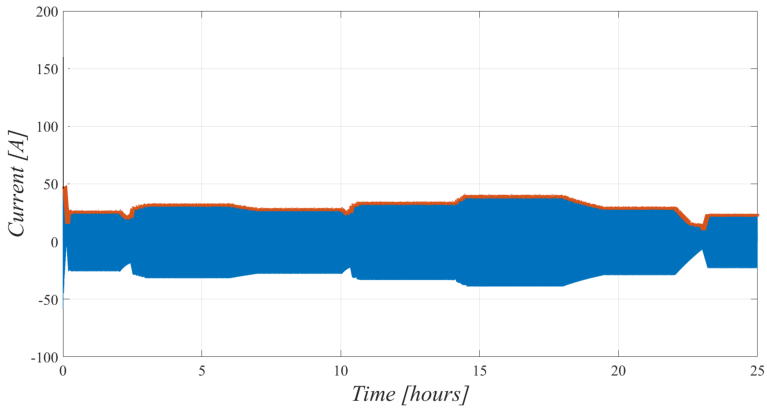
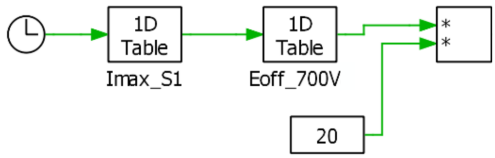
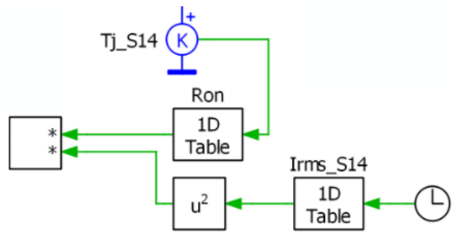


Figure 4.11: The current flowing through one MOSFET with the extracted upper envelope. The maximum values are used to calculate the switching losses



(a) Switching losses of one MOSFET



(b) Conduction losses of one MOSFET

Figure 4.12: Simulation of (a) the switching losses and (b) the conduction losses in PLECS for one MOSFET

The thermal resistances are specified by the datasheet and some additional calculations as already presented in Chapter 3. The junction-to-case thermal resistance, in particular, is a combination of resistances and capacitances, i.e. the thermal equivalent network, as shown in Figure 4.13 [98]. These values are given by the MOSFET datasheet [95]. The case-to-sink thermal resistance is calculated by the thermal impedance of the insulation ($0.13^0 Cin^2/W$) [99], as found in the Appendix, and the MOSFET area ($A = 0.5277in^2$). Finally, the sink-to-ambient thermal resistance is calculated for the proper selection of the

heatsinks. The calculated values of the thermal resistances and temperatures per MOSFET are given in Table 4.2 for the PV and BESS converter switching devices. The appropriate cooling device was found to be the LAM 5 D K 100 24 by Fischer Elektronik [96]. The dimensions and thermal resistance of the heatsink are illustrated in Figure 4.14.

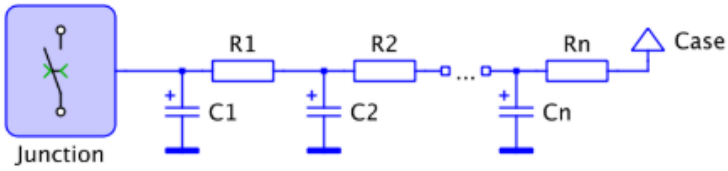


Figure 4.13: The junction-to-case thermal resistances and capacitances [98]

Table 4.2: Heatsink design specifications

Heatsink Specifications		
Parameters	**PV connection**	**BESS connection**
P_{tot} $[W]$ per MOSFET @ rated power (20 kW)	33.88	30.29
R_{jc} $[^0C/W]$ per MOSFET	0.27	0.27
R_{cs} $[^0C/W]$ per MOSFET	0.246	0.246
R_{sa} $[^0C/W]$ total	0.314	0.366
Junction temperature, T_j $[^0C]$	100	100
Case temperature, T_c $[^0C]$	90.85	91.82
Heatsink temperature, T_s $[^0C]$	82.5	84.36
Ambient temperature, T_a $[^0C]$	40	40

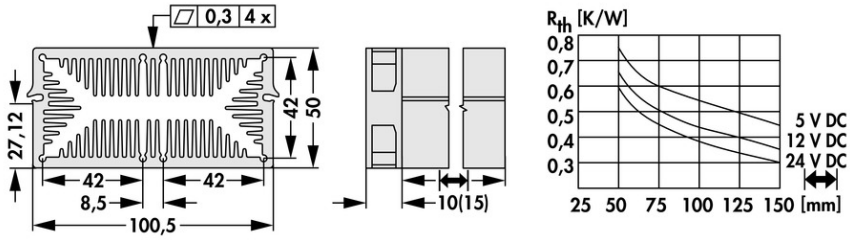


Figure 4.14: Dimensions and thermal resistance of the heatsink with the operating voltage of the fan motor

4.2 Modelling of the distributed scenario

Figure 4.15 illustrates the distributed electrical model of the PV-BESS hybrid system, as developed in PLECS software. Three identical DAB DC-DC converters have been

separately connected to the PV arrays at the input, while the outputs are series-connected to reach the medium voltage levels (2.1 kV). The same structure has been considered for the battery integration to the MVDC grid.

The same controller schemes of Figures 4.2 to 4.6, developed for the centralized model, have also been implemented to the distributed configuration. The main difference is that separate identical controllers are used to control the power flow of each PV-DAB and BESS-DAB subsystem. It should be mentioned that the thermal model of this configuration has not been investigated, as for the centralized case. However, a similar procedure can be followed as for the centralized scenario to obtain the thermal performance.

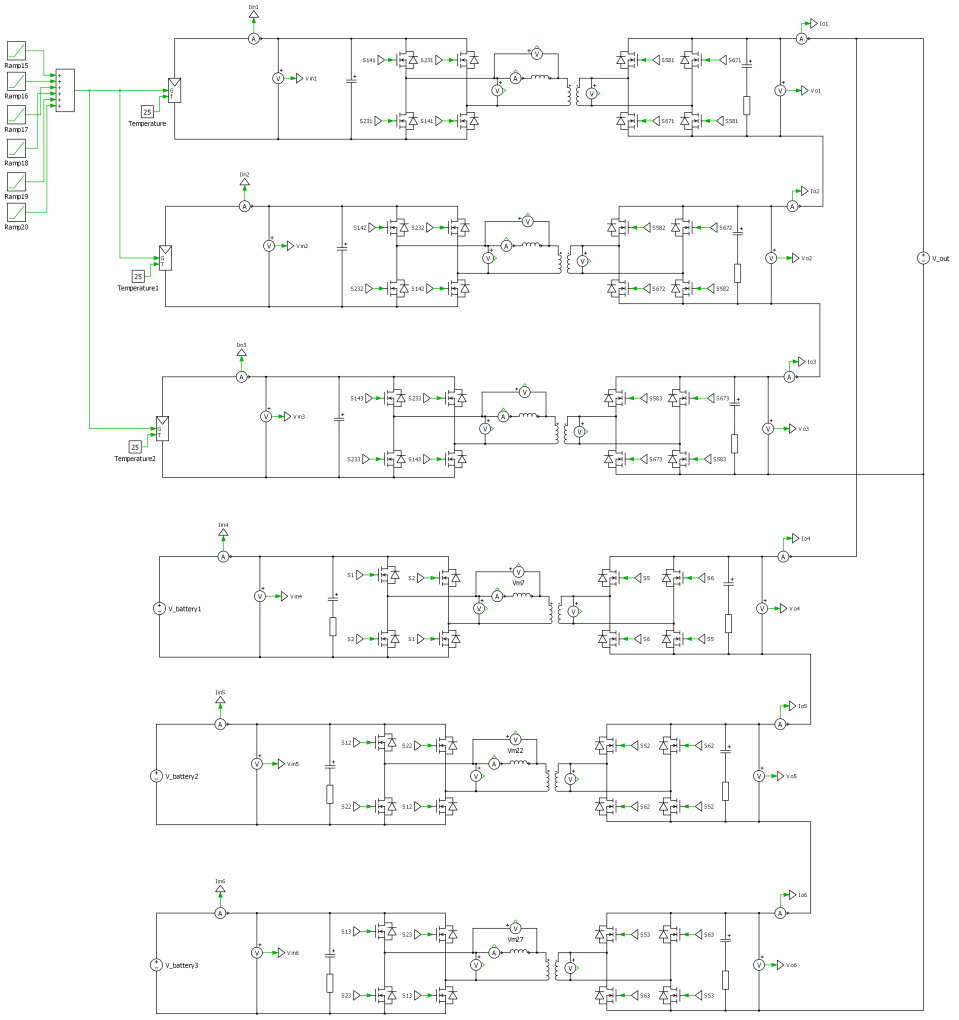


Figure 4.15: Electrical model for the distributed scenario developed in PLECS

Chapter 5

Simulation Results

This chapter delivers the simulation results of the electrical and thermal models developed in PLECS. The electrical simulations, particularly, have been carried out for both scenarios, the centralized and distributed, whereas the thermal simulations only for the centralized system configuration.

The first stage in the system operation is the collection of forecasting data. That is, the solar radiation, which impacts directly the PV power generation and the load power demand. Figure 5.1 illustrates the daily solar radiation profile [100], which refers to $63^0 26' 48.5772''$ N and $10^0 25' 18.8616''$ E for the 139^{th} day of the year. In order to verify the hybrid system operation the stochastic load profile of Figure 5.2 has been considered. According to [101], the forecasted load profile for one day of operation is assumed to be a fast electric vehicle (EV) charging station.

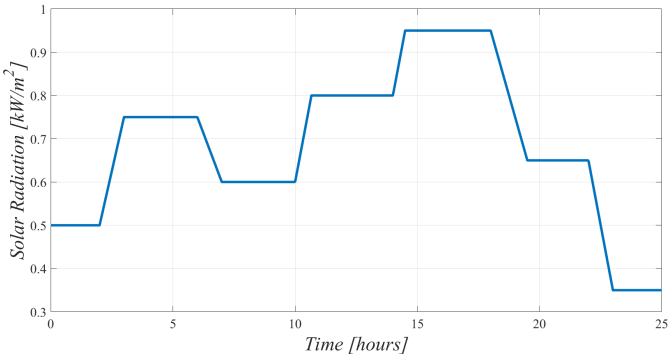


Figure 5.1: The solar radiation profile for the 139^{th} day of the year, referring to $63^0 26' 48.5772''$ N and $10^0 25' 18.8616''$ E

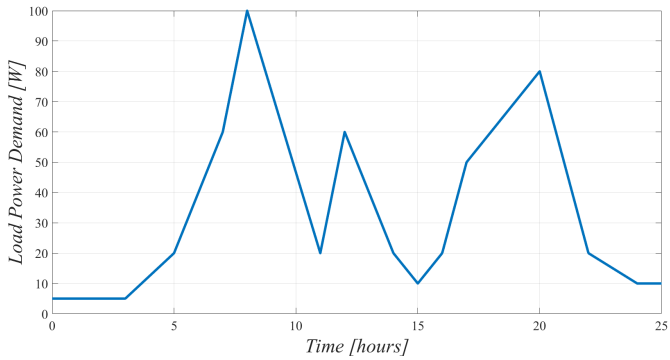


Figure 5.2: Stochastic load power demand profile for a typical day of the year

5.1 Centralized scenario

Considering the electrical model in Chapter 4 for the centralized configuration of the hybrid system and the solar and load profiles of Figures 5.1 and 5.2, the performance of PVs and batteries is captured in Figure 5.3. When the power generated from the PVs is sufficient to supply the load demand the batteries are in charging mode and, thus, the battery power (P_{bat}) is negative. Similarly, when the PV power is not sufficient to feed the load the batteries supply the additional necessary power and, therefore, they are in discharging mode with a positive power value, P_{bat}.

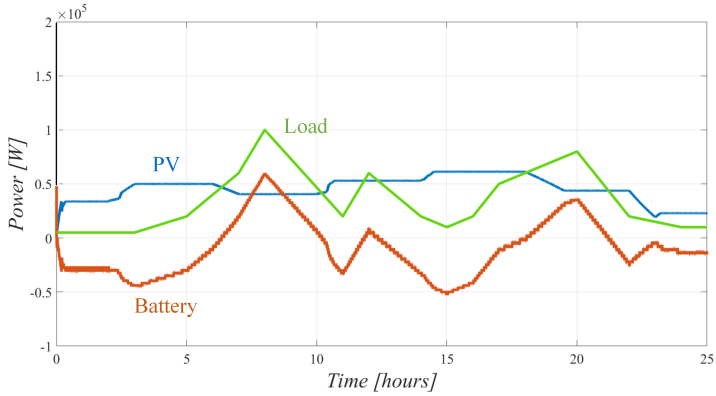


Figure 5.3: PV, battery and load power profiles at a given solar radiation

The devices' current has also been captured from the electrical simulations. More specifically, Figure 5.4 illustrates the current flowing through S_{14} MOSFET, which is placed in the modularized DAB converter connected to photovoltaics. This is the instantaneous value of the current that is captured around 3 PM, when the solar radiation has its maximum value. At this time instant, the maximum MOSFET current is around 40 A, which is within acceptable design limits.

The waveforms of the primary and secondary voltage of one block, as well as the inductor voltage have been captured for the same time instant and they are illustrated in Figure 5.5. The phase shift angle δ results in a voltage difference on the inductor, as shown in the figure. The results verify the correct performance of the modularized converter connected to PVs and the phase shift controller.

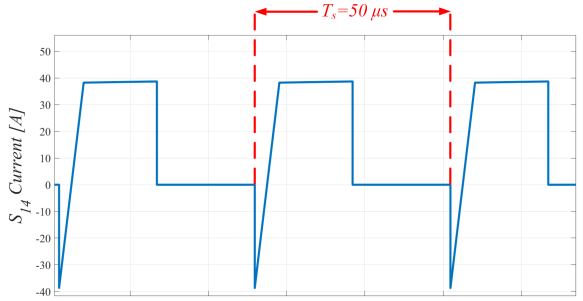


Figure 5.4: Capture of current flowing through one MOSFET of the modularized DAB converter connected to PVs under maximum solar radiation

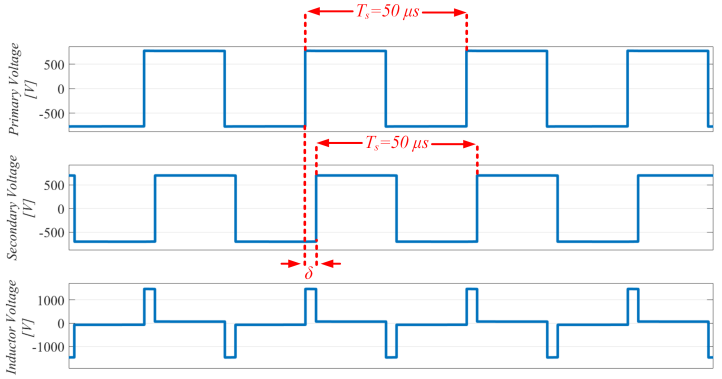


Figure 5.5: Capture of the primary, secondary and inductor voltages for the first block of the modularized DAB converter connected to PVs

Figure 5.6 shows the instantaneous value of the current flowing through the S_1 MOSFET operating in the DAB converter connected to batteries. This capture is taken around 8 AM, when the battery output power has its maximum value, as shown in Figure 5.3. During this time instant the MOSFET current is approximately 40 A, which is an acceptable value as already mentioned. It is worth mentioning that the reverse current flows through the MOSFET channel and not through the body diode due to diodeless operation. This results in both a lower cost and size of the converter and lower conduction losses, as only the MOSFET channel is used for the negative current to flow and not the body diode [41].

Figure 5.7 illustrates the primary, secondary and inductor voltage waveforms, which have been captured for the same time instant. It is observed that the converter connected

to batteries and the phase shift controller operates in an effective way to allow the power flow in both directions.

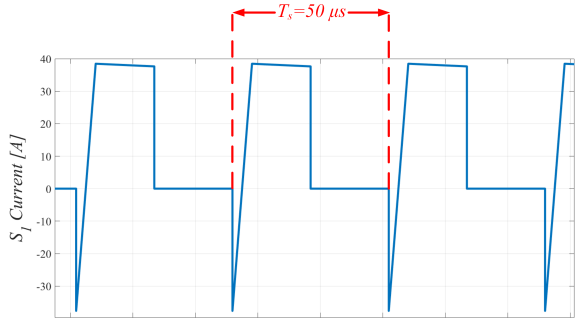


Figure 5.6: Capture of current flowing through one MOSFET of the modularized DAB converter connected to batteries under maximum solar radiation

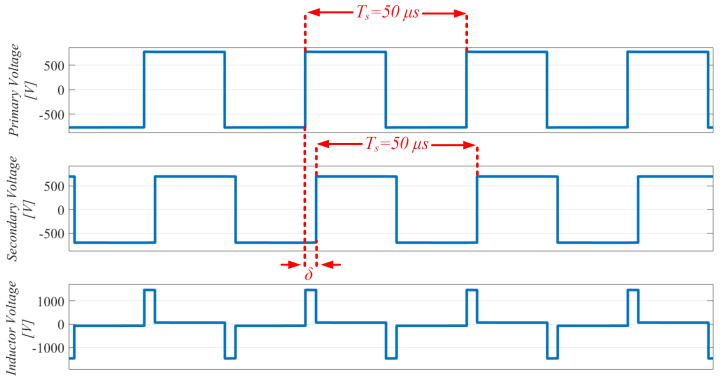


Figure 5.7: Capture of the primary, secondary and inductor voltages for the first block of the modularized DAB converter connected to batteries

Figure 5.8 illustrates the response of the PI controller for the daily solar radiation profile described above. The results show that the control variable does not saturate (< 1), which is a considerable advantage of the controller. Saturation would limit the speed of the closed loop performance and might lead to instability if there was no compensation [102]. The same can be observed in Figure 5.9, where the control variable reaches the maximum value of $0.25 < 1$ and does not saturate. Therefore the BESS-DAB controller operates in an optimal way during the whole day.

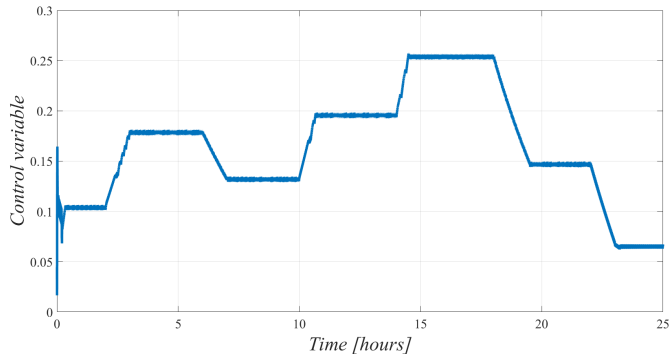


Figure 5.8: Response of the digital PI controller of the DAB converter connected to PVs

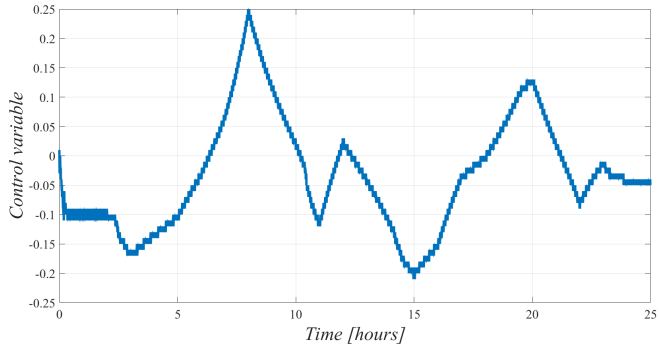


Figure 5.9: Response of the PI controller of the DAB converter connected to batteries

Considering the thermal simulations for one block of each modularized DAB converter, as analysed in Chapter 4, the anticipated junction temperature variations ($T_{junction}$) of one MOSFET has been captured for the whole day. Figure 5.10 shows these temperature swings for one MOSFET of the DAB connected to PVs. The switching device is stressed at various temperature cycles in the range of $\Delta T = 15 - 30^0 C$. Considering the solar radiation profile and the power generated from the PVs, the current flowing through each MOSFET increases when the solar radiation and, thus the PV power increases. During the hours that the solar radiation is low, the generated power is reduced and, therefore, the MOSFET current is lower. The decrease and increase of current result in temperature variations inside the MOSFET, i.e. the temperature is higher for a higher current and lower for a lower flowing current. This stress introduces reliability issues, as it is responsible for the reduction of the expected operating lifetime of the MOSFET.

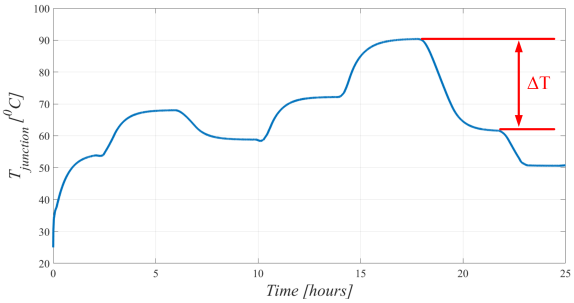


Figure 5.10: Junction temperature variations of one MOSFET of the modularized DAB converter connected to PVs due to variations in solar radiation

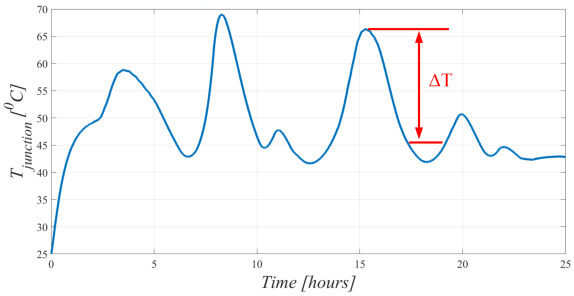


Figure 5.11: Junction temperature variations of one MOSFET of the modularized DAB converter connected to batteries due to variations in solar radiation

Figure 5.11 shows the temperature swings of one MOSFET operating in the DAB block connected to the batteries. These variations are also related to the generated PV power and load power-demand profiles. The current flowing through the MOSFETs increases when the power flow from the batteries also increases to supply additional power to the load when the PV power is not sufficient enough. Therefore, the MOSFET temperature increases. On the other hand, the MOSFET current and, thus, its temperature decreases when the battery power is low and the load is supplied only by the PVs. This temperature stress of the MOSFET is of great importance to investigate for this case. Since the temperature cycles are not constant and take load-demand dependent values during the whole operation of the MOSFETs, PCT reliability test cannot give an accurate lifetime estimation due to the ΔT variations. Instead the rainflow algorithm that has been presented in Chapter 2 can be implemented.

Figure 5.12 shows the temperature cycles as a function of cycle average and cycle range, which is plotted in Matlab for the case of battery-DAB converter MOSFET. Initially, the algorithm turns the temperature history into a sequence of reversals. These are the local maxima and minima where there is a change in sign, as shown in the upper part of the image. At the end a histogram of cycles is produced according to the lower part of the figure. For this case, there are 5.5 stress cycles in the range of $\Delta T = 5 - 50^0C$, as shown in the histogram. More specifically, there is 1 cycle of 5^0C, 2 cycles of 10^0C, 2

cycles of 30^0C and half cycle of 50^0C. The number of cycles and the cycle amplitude are responsible to trigger a failure in the MOSFET. However, for $\Delta T = 5^0C$, for example, the contribution to failure is not considered because the stress is within the elastic limit and the material resumes its original shape and size without a permanent deformation.

In order to estimate the operating lifetime of the MOSFETs, the simulations need to run for a longer time under a repetitive stress and a lifetime model needs to be implemented. The damage of the device due to variable stress can also be determined using Miner's rule [66]. However, this is out of the scope of this work and won't be further analyzed.

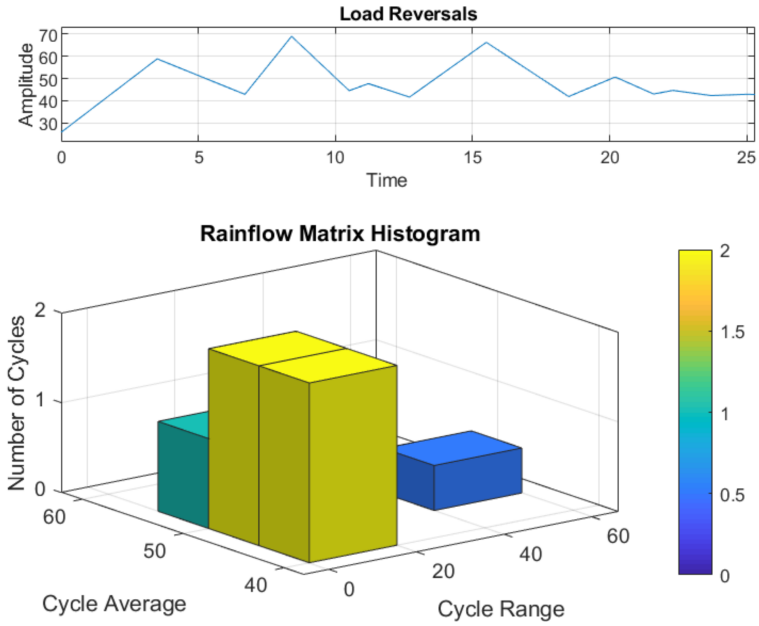


Figure 5.12: Rainflow histogram of temperature cycles as a function of cycle average and cycle range for the case of battery-DAB converter MOSFET

5.2 Distributed scenario

This scenario has been investigated considering the distributed model as analyzed in Chapter 4 only for electrical simulations. The load demand profile of Figure 5.2 has been considered and two different solar radiation profiles have been plotted as inputs to the PV arrays. Figure 5.13 illustrates the initial solar radiation (Solar 1) for the 139^{th} day of the year, referring to $63^0 26' 48.5772''$ N and $10^0 25' 18.8616''$ E and a stochastic solar profile (Solar 2) in order to verify the simulations. Two out of three PV-converter blocks have the "Solar 1" input and the third has the "Solar 2" input. The reason behind this approach is to verify the independent operation of the converters when a change in solar radiation occurs.

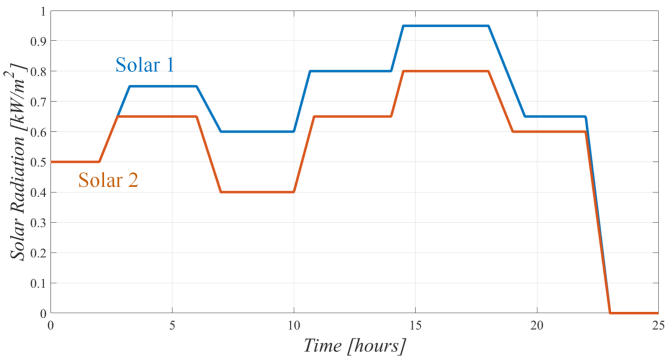


Figure 5.13: Solar 1: The solar radiation profile for the 139^{th} day of the year, referring to $63^0 26' 48.5772''$ N and $10^0 25' 18.8616''$ E. Solar 2: A stochastic solar radiation to verify the simulations

Figure 5.14 shows the power profiles of the PVs and batteries for the given load demand. It can be observed that when the load demand is higher that the power generated from the photovoltaics, the batteries are discharging by supplying the additional necessary power to the load. During the night, in particular, that the PV power drops to zero the batteries supply power to meet the load demand. Similarly, when PV is sufficient ot feed the load the batteries are charging either from the grid or the PVs. Therefore, the system operation is verified also in this scenario.

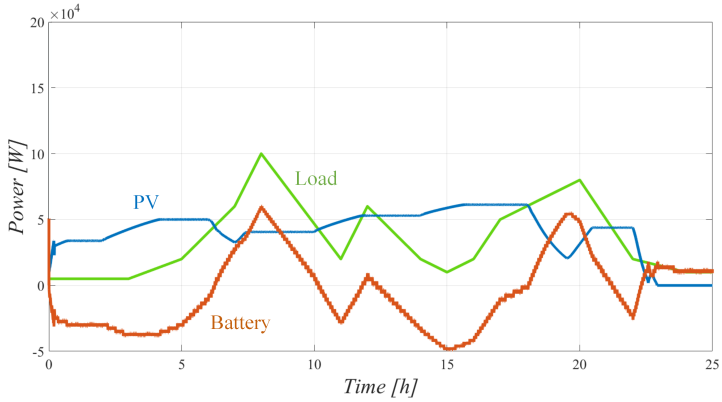


Figure 5.14: PV, battery and load power profiles under the given different solar radiations

The instantaneous values of the MOSFET currents have also been captured and are presented below. Figure 5.15 illustrates the S_{141}, S_{142} and S_{143} MOSFET currents, each operating in a separate PV-DAB converter. The waveforms are captured at approximately 3 PM, when the solar radiations have a maximum value. It is observed that the peak current value is around 40 A, which is within acceptable design limits.

At the same time instant the voltage waveforms of the primary and secondary bridges of one block have been captured and are presented in Figure 5.16. The converter and the

phase shift controller operates effectively allowing the power to flow from the PVs to the load. The difference between the primary and secondary voltages appears on the inductor and, as a result, the power flows from the leading to the lagging bridge.

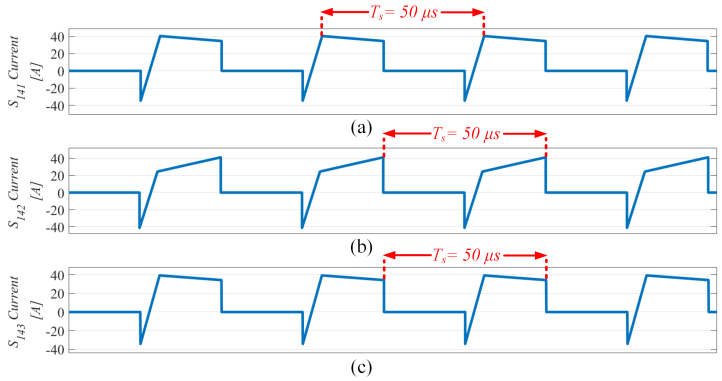


Figure 5.15: Instantaneous values of currents flowing through the MOSFETs operating in PV-DAB converters under maximum solar radiation. (a) S_{141} MOSFET current of PV-DAB block 1, (b) S_{142} MOSFET current of PV-DAB block 2 and (c) S_{143} MOSFET current of PV-DAB block 3

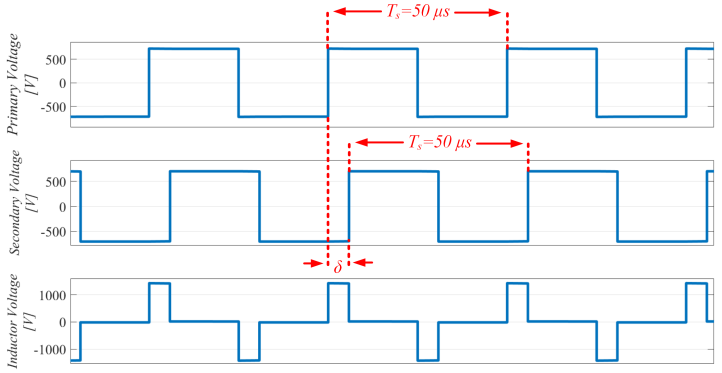


Figure 5.16: Capture of the primary, secondary and inductor voltages for the first block of the modularized DAB converter connected to photovoltaics

Figure 5.17 shows the corresponding MOSFET currents, for MOSFETs S_1, S_{12} and S_{13} each operating in BESS-DAB converter blocks. The instantaneous current waveforms are taken at 8 AM, when the power supplied by the battery is at its maximum. The current of the switching devices reaches 40 A, which is also an acceptable value. For this case also the primary, secondary and inductor voltages have been taken into consideration at 8 AM and they are shown in Figure 5.18. It can be observed that the power flows from the batteries to supply the load, as the PV power is not sufficient. The voltage difference between the primary and secondary bridge of the block appears on the inductor allowing the current to flow.

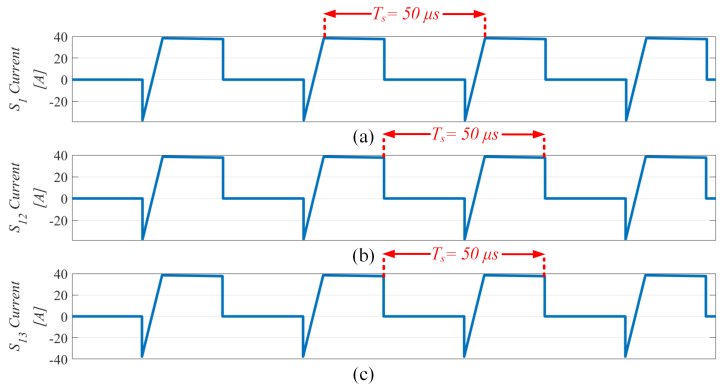


Figure 5.17: Instantaneous values of currents flowing through the MOSFETs operating in BESS-DAB converters under maximum battery power flow. (a) S_1 MOSFET current of BESS-DAB block 1, (b) S_{12} MOSFET current of BESS-DAB block 2 and (c) S_{13} MOSFET current of BESS-DAB block 3

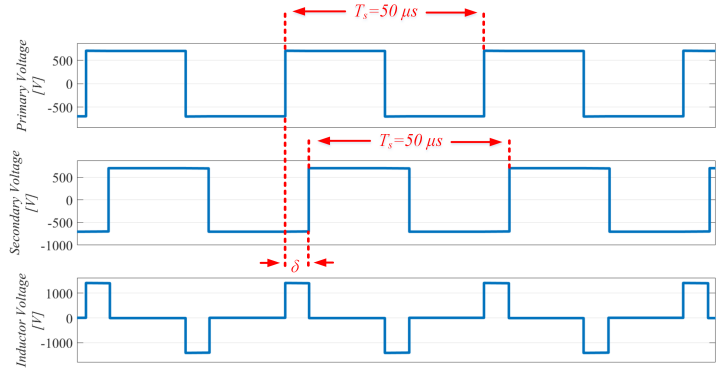


Figure 5.18: Capture of the primary and secondary bridge voltages as well as the inductor voltage for one block of the converter connected to batteries

Figures 5.19 and 5.20 illustrate the control variable of the PI controller for the control of PV and battery power flow respectively. Also for this scenario the variable reaches a maximum value of $0.25 < 1$ during the daily operation, which is within acceptable limits and it does not saturate.

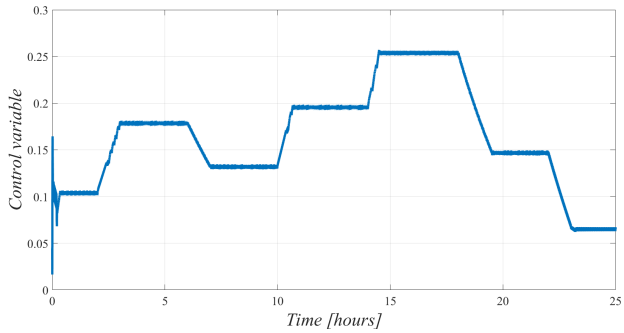


Figure 5.19: Response of the digital PI controller of the DAB converter connected to photovoltaics

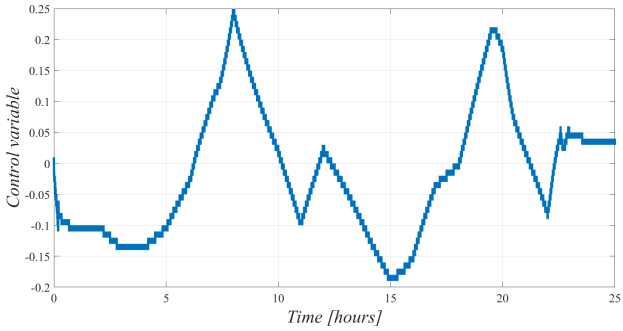


Figure 5.20: Response of the PI controller of the DAB converter connected to the battery system

From the aforementioned analysis it can be concluded that although both scenarios are designed and operate in an optimal way the distributed configuration is more reliable. This is because the converters can operate and can be controlled irrespective of each other. Therefore, in case of a change in solar power or a fault in PVs or batteries, the system will not collapse but will be able to operate unaffected by the faults and changes however at a limited power flow capability.

Chapter 6

Conclusion and Future Work

In the present work a dual active bridge DC-DC converter is utilized to develop modularized systems in order to interconnect photovoltaics and batteries to the MVDC distribution grid. An overview of the different modularized converter topologies is presented and possible connections of PV-BESS systems to the MVDC grid are discussed. In order to understand the operation of such a converter, thorough analysis has been conducted on the principles of design and operation, dynamic characteristics and bidirectional power flow capability of the DAB fundamental block. The converter modeling and control strategy are also developed based on a single phase shift modulation scheme. In order to interconnect PVs and batteries to the MVDC grid through the modularized DAB converters the PV model and MPPT control scheme are investigated and a PI controller is implemented to regulate the power flow from the battery system.

Two different system configurations, in particular, have been developed in PLECS simulation software. The first is a centralized PV-BESS hybrid system utilizing two 60 kW IPOS modularized DAB converters, each connected to PVs and batteries respectively, where identical SiC MOSFETs are employed to the converters. In order to verify the system operation, a stochastic load profile of a fast EV charging station and variations in solar radiation have been considered. Both the electrical and thermal models have been developed for the 139^{th} day of the year, referring to $63^0 26' 48.5772''$ N and $10^0 25' 18.8616''$ E coordinates. The electrical results show that the system operates in an optimal way. The PVs supply the necessary power to the load and the batteries are in charging mode and, when this is not sufficient, the batteries are in discharging mode, supplying the additional power to the load. The MOSFETs' current has also been observed and reaches the value of 40 A, which is within acceptable design limits. At the same time instant the voltage waveforms of the primary and secondary bridge of one block as well as the inductor voltage have been captured from PLECS. The results verify the efficient performance of the converter and the phase shift controller. Moreover, the response of the PI controllers for the control of power from the PVs and batteries during the daily solar radiation profile have been taken into consideration. The results show that the control variable does not saturate in both controllers, as the maximum value they reach is 0.25 (< 1). This veri-

fies the good performance of the controllers within stability design limits. The thermal results indicate that the MOSFETs are stressed at various temperature cycles in the range of $\Delta T = 15 - 30^0 C$ for those connected to PVs and $\Delta T = 5 - 50^0 C$ for those connected to batteries. To obtain particularly the latter temperature range, the rainflow algorithm has been implemented using Matlab.

The second scenario is a distributed system configuration, where the same converters are utilized and they are separately connected to PVs and batteries at the input and in series at the output. The operation of the system has been investigated considering the same load profile and two different solar radiations as inputs to PV arrays at the same time. The reason is to verify the irrelevant operation of the converters when a change in solar radiation occurs, as they can be controlled irrespective of each other. For this configuration only the electrical model has been developed and the results have shown an optimal operation of the system as in the first topology. The current flowing through the MOSFETs under maximum solar radiation and maximum battery power reaches 40 A, which is an acceptable value. Also the primary and secondary bridge voltages of one block of the converters connected to PVs and batteries as well as the inductor voltage have been captured. The results verify the operation of the converters and their controllers. The response of the PI controllers have also been considered and they show good performance, as they do not saturate during the daily operation of the system. It is worth mentioning that although the two topologies are designed and operate in an optimal way, the distributed configuration is more reliable. This is because in case of a change in solar radiation or a fault in PVs and/or batteries the system will keep operating, supplying power (lower than the rated), and will not collapse.

The system models developed in the present thesis require further work to improve the overall operation of the converters. Firstly, a different control scheme is to be investigated, for example a dual phase shift control strategy, to avoid the high circulating currents appeared in the converter. Also, the inrush current issue at the start-up of the converter can be tackled and the ZVS during the whole operation can be maintained.

It is interesting to develop the thermal model for the distributed scenario, based on the model presented for the centralized system configuration. The rainflow algorithm can be then used to obtain the temperature cycles and a lifetime model can be implemented to estimate the lifetime of the MOSFETs under a repetitive stress. The results from the rainflow algorithm along with the use of lifetime models, such as those in [103] or [104] can be used to estimate the operating lifetime of the switching devices also for the centralized scenario.

Another aspect that can be further investigated is to examine these system configurations when a fault occurs in the batteries. The employment of the proper protection scheme in the system will isolate the fault part and it is interesting to see the impact the fault has on the whole operation of the system.

Last but not least, a construction of the converter in the lab and experimental investigation of the system operation is of great importance. Also reliability tests of the MOSFETs can be carried out in the lab to obtain experimental results.

Bibliography

[1] P. K. Steimer and O. Apeldoorn. Medium voltage power conversion technology for efficient windpark power collection grids. In *The 2nd International Symposium on Power Electronics for Distributed Generation Systems*, pages 12–18, June 2010.

[2] W. Chen, A. Q. Huang, C. Li, G. Wang, and W. Gu. Analysis and comparison of medium voltage high power dc/dc converters for offshore wind energy systems. *IEEE Transactions on Power Electronics*, 28(4):2014–2023, April 2013.

[3] Matt Golden, Adam Scheer, and Carmen Best. Decarbonization of electricity requires market-based demand flexibility. *The Electricity Journal*, 32(7):106621, 2019. Special Issue: Energy Optimization is the Key to Affordable, Reliable Decarbonization.

[4] Y. Zhang, X. Wang, W. Zhang, F. Hou, and Z. Wu. Analysis of technical strategies towards a low carbon electricity system in europe. In *2015 5th International Conference on Electric Utility Deregulation and Restructuring and Power Technologies (DRPT)*, pages 2561–2565, Nov 2015.

[5] L. K. Panwar, K. S. Reddy, and R. Kumar. Productive use of distributed renewable generation source with electric vehicle in smart grid. In *2014 6th IEEE Power India International Conference (PIICON)*, pages 1–6, Dec 2014.

[6] Matt Golden, Adam Scheer, and Carmen Best. Decarbonization of electricity requires market-based demand flexibility. *The Electricity Journal*, 32(7):106621, 2019. Special Issue: Energy Optimization is the Key to Affordable, Reliable Decarbonization.

[7] European Commission. Energy roadmap 2050; impact assessment and scenario analysis. 2011.

[8] A. Giannakis and D. Peftitsis. Mvdc distribution grids and potential applications: Future trends and protection challenges. In *2018 20th European Conference on Power Electronics and Applications (EPE'18 ECCE Europe)*, pages P.1–P.9, Sep. 2018.

[9] J. Priebe, N. Wehbring, and A. Moser. Design of medium voltage dc grids– impact of power flow control on grid structure. In *2018 53rd International Universities Power Engineering Conference (UPEC)*, pages 1–6, Sep. 2018.

[10] M. Stieneker and R. W. De Doncker. Medium-voltage dc distribution grids in urban areas. In *2016 IEEE 7th International Symposium on Power Electronics for Distributed Generation Systems (PEDG)*, pages 1–7, June 2016.

[11] S. Patrobers, X. Ai, B. G. Teshager, and W. Kunyu. Modelling and control of a vsc medium-voltage dc distribution network with dfig wind farm. *The Journal of Engineering*, 2017(13):2502–2507, 2017.

[12] J. Priebe, N. Wehbring, and A. Moser. Planning and design of medium voltage dc grids– an overview. In *2018 53rd International Universities Power Engineering Conference (UPEC)*, pages 1–6, Sep. 2018.

[13] G. F. Reed, B. M. Grainger, A. R. Sparacino, and Z. Mao. Ship to grid: Medium-voltage dc concepts in theory and practice. *IEEE Power and Energy Magazine*, 10(6):70–79, Nov 2012.

[14] G. F. Reed, B. M. Grainger, M. J. Korytowski, and E. J. Taylor. Modeling, analysis, and validation of a preliminary design for a 20 kv medium voltage dc substation. In *IEEE 2011 EnergyTech*, pages 1–8, May 2011.

[15] M. Yang, D. Xie, H. Zhu, and Y. Lou. Architectures and control for multi-terminal dc (mtdc) distribution network-a review. In *11th IET International Conference on AC and DC Power Transmission*, pages 1–7, Feb 2015.

[16] M. S. Carmeli, F. Castelli-Dezza, D. Rosati, G. Marchegiani, and M. Mauri. Mvdc connection of offshore wind farms to the transmission system. In *SPEEDAM 2010*, pages 1201–1206, June 2010.

[17] K. Takeda, C. Takahashi, H. Arita, N. Kusumi, M. Amano, and A. Emori. Design of hybrid energy storage system using dual batteries for renewable applications. In *2014 IEEE PES General Meeting — Conference Exposition*, pages 1–5, 2014.

[18] J. D. Boles, Y. Ma, J. Wang, D. Osipov, L. M. Tolbert, and F. Wang. Converter-based emulation of battery energy storage systems (bess) for grid applications. *IEEE Transactions on Industry Applications*, 55(4):4020–4032, 2019.

[19] K. Sharifabadi, L. Harnefors, H.-P. Nee, S. Norrga, and R. Teodorescu. *Design, Control, and Application of Modular Multilevel Converters for HVDC Transmission Systems*. John Wiley Sons, Ltd, 2016.

[20] S. Patil, S. Vemuru, V. Devabhaktuni, and K. Al-Olimat. Comparison of multi-level dc-dc converter topologies. In *IEEE International Conference on Electro-Information Technology , EIT 2013*, pages 1–5, May 2013.

[21] N. Kim and B. Parkhideh. Pv-battery series inverter architecture: A solar inverter for seamless battery integration with partial-power dc–dc optimizer. *IEEE Transactions on Energy Conversion*, 34(1):478–485, 2019.

[22] N. Soltau, R. U. Lenke, and R. W. De Doncker. *High-Power DC-DC Converter*. E.ON Energy Research Center series, 2014 & 2016.

[23] S. P. Engel, M. Stieneker, N. Soltau, S. Rabiee, H. Stagge, and R. W. De Doncker. Comparison of the modular multilevel dc converter and the dual-active bridge converter for power conversion in hvdc and mvdc grids. *IEEE Transactions on Power Electronics*, 30(1):124–137, Jan 2015.

[24] E. Rigati. Design and control of sic-based dual active bridge dc/dc converter for interconnection of pvs to the dc grid. Project report in TET5500, Department of Electric Power Engineering, NTNU – Norwegian University of Science and Technology, Dec. 2019.

[25] J. Hong, D. M. Vilathgamuwa, N. Ghasemi, T. Ishrat, and J. You. A single phase dc-ac dual active bridge series resonant converter for photovoltaic applications. In *2017 IEEE 12th International Conference on Power Electronics and Drive Systems (PEDS)*, pages 881–886, Dec 2017.

[26] G. D. Demetriades. *On Small-Signal Analysis and Control of the Single and the Dual-Active Bridge Topologies*. PhD thesis, KTH, Royal Institute of Technology, 2005.

[27] H. Akagi, S. Kinouchi, and Y. Miyazaki. Bidirectional isolated dual-active-bridge (dab) dc-dc converters using 1.2-kv 400-a sic-mosfet dual modules. *CPSS Transactions on Power Electronics and Applications*, 1(1):33–40, Dec 2016.

[28] M. Kim, M. Rosekeit, S. Sul, and R. W. A. A. De Doncker. A dual-phase-shift control strategy for dual-active-bridge dc-dc converter in wide voltage range. In *8th International Conference on Power Electronics - ECCE Asia*, pages 364–371, May 2011.

[29] P. Grzejszczak, R. Barlik, M. Nowak, and K. Wolski. Bidirectional modular dc/dc converter for directcurrent microgrids. In *2017 Progress in Applied Electrical Engineering (PAEE)*, pages 1–7, 2017.

[30] P. Zumel, L. Ortega, A. Lázaro, C. Fernández, A. Barrado, A. Rodríguez, and M. M. Hernando. Modular dual-active bridge converter architecture. *IEEE Transactions on Industry Applications*, 52(3):2444–2455, 2016.

[31] P. Zumel, L. Ortega, A. Lazaro, C. Fernandez, and A. Barrado. Control strategy for modular dual active bridge input series output parallel. In *2013 IEEE 14th Workshop on Control and Modeling for Power Electronics (COMPEL)*, pages 1–7, 2013.

[32] P. Zumel, L. Ortega, A. Lázaro, C. Fernández, A. Barrado, A. Rodríguez, and M. M. Hernando. Modular dual-active bridge converter architecture. *IEEE Transactions on Industry Applications*, 52(3):2444–2455, 2016.

[33] M. Guan. A series-connected offshore wind farm based on modular dual-active-bridge (dab) isolated dc–dc converter. *IEEE Transactions on Energy Conversion*, 34(3):1422–1431, 2019.

[34] M. Trivedi and K. Shenai. Power semiconductor devices. In W.-K. Chen, editor, *The Electrical Engineering Handbook*, chapter 7, pages 163–176. Academic Press, 2005.

[35] B. J. Baliga. *Fundamentals of Power Semiconductor Devices*. Springer, 2008.

[36] Undeland T. M. Mohan, N. and W. P. Robbins. *Power Electronics: Converters, Applications, and Design, 3rd Edition*. John Wiley Sons, Inc., 2003.

[37] M. G. Simoes. Power bipolar transistors. In H. M. Rashid, editor, *Power Electronics Handbook Third Edition*, chapter 3, pages 29–41. Butterworth-Heinemann, 2011.

[38] A. Elasser and T. P. Chow. Silicon carbide benefits and advantages for power electronics circuits and systems. *Proceedings of the IEEE*, 90(6):969–986, June 2002.

[39] M. G. H. Aghdam and T. Thiringer. Comparison of sic and si power semiconductor devices to be used in 2.5 kw dc/dc converter. In *2009 International Conference on Power Electronics and Drive Systems (PEDS)*, pages 1035–1040, Nov 2009.

[40] Peftitsis D. Rabkowski, J. and H.-P. Nee. Recent advances in power semiconductor technology. In Malinowski M. Abu-Rub, H. and K. Al-Haddad, editors, *Power Electronics for Renewable Energy Systems, Transportation, and Industrial Applications, First Edition*, chapter 4, pages 69–106. John Wiley Sons, Ltd., 2014.

[41] D. Peftitsis, G. Tolstoy, A. Antonopoulos, J. Rabkowski, J. Lim, M. Bakowski, L. Angquist, and H. Nee. High-power modular multilevel converters with sic jfets. In *2010 IEEE Energy Conversion Congress and Exposition*, pages 2148–2155, Sep. 2010.

[42] J. Biela, M. Schweizer, S. Waffler, and J. W. Kolar. Sic versus si—evaluation of potentials for performance improvement of inverter and dc–dc converter systems by sic power semiconductors. *IEEE Transactions on Industrial Electronics*, 58(7):2872–2882, July 2011.

[43] H. Qin, B. Zhao, X. Nie, J. Wen, and Y. Yan. Overview of sic power devices and its applications in power electronic converters. In *2013 IEEE 8th Conference on Industrial Electronics and Applications (ICIEA)*, pages 466–471, June 2013.

[44] M. Östling, R. Ghandi, and C. Zetterling. Sic power devices — present status, applications and future perspective. In *2011 IEEE 23rd International Symposium on Power Semiconductor Devices and ICs*, pages 10–15, May 2011.

[45] J. Millán, P. Godignon, X. Perpiñà, A. Pérez-Tomás, and J. Rebollo. A survey of wide bandgap power semiconductor devices. *IEEE Transactions on Power Electronics*, 29(5):2155–2163, May 2014.

[46] R. R. Lamichhane, N. Ericsson, S. Frank, C. Britton, L. Marlino, A. Mantooth, M. Francis, P. Shepherd, M. Glover, S. Perez, T. McNutt, B. Whitaker, and Z. Cole. A wide bandgap silicon carbide (sic) gate driver for high-temperature and high-voltage applications. In *2014 IEEE 26th International Symposium on Power Semiconductor Devices IC's (ISPSD)*, pages 414–417, June 2014.

[47] P. Friedrichs and R. Rupp. Silicon carbide power devices - current developments and potential applications. In *2005 European Conference on Power Electronics and Applications*, pages 11 pp.–P.11, Sep. 2005.

[48] J. Rabkowski, D. Peftitsis, and H. Nee. Silicon carbide power transistors: A new era in power electronics is initiated. *IEEE Industrial Electronics Magazine*, 6(2):17–26, June 2012.

[49] M. A. Huque, L. M. Tolbert, B. J. Blalock, and S. K. Islam. Silicon-on-insulator-based high-voltage, high-temperature integrated circuit gate driver for silicon carbide-based power field effect transistors. *IET Power Electronics*, 3(6):1001–1009, Nov 2010.

[50] P. G. Neudeck and J. A. Powell. Performance limiting micropipe defects in silicon carbide wafers. *IEEE Electron Device Letters*, 15(2):63–65, Feb 1994.

[51] D. Peftitsis, G. Tolstoy, A. Antonopoulos, J. Rabkowski, J. Lim, M. Bakowski, L. Angquist, and H. Nee. High-power modular multilevel converters with sic jfets. In *2010 IEEE Energy Conversion Congress and Exposition*, pages 2148–2155, Sep. 2010.

[52] M. Rahimo. Performance evaluation and expected challenges of silicon carbide power mosfets for high voltage applications. *Materials Science Forum*, 897:649–654, May 2017.

[53] G. Kenny. Design and control of a bidirectional dual active bridge dc-dc converter to interface solar, battery storage, and grid-tied inverters. Master's thesis, University of Arkansas, Fayetteville, 2015.

[54] N. Iwamuro. Recent progress of sic mosfet devices. *Materials Science Forum*, 954:90–98, May 2019.

[55] B. Kakarla et al. Planar to trench: Short circuit capability analysis of 1.2 kv sic mosfets. *Materials Science Forum*, 924:782–785, June 2018.

[56] J. Rabkowski, G. Tolstoy, D. Peftitsis, and H. Nee. Low-loss high-performance base-drive unit for sic bjts. *IEEE Transactions on Power Electronics*, 27(5):2633–2643, May 2012.

[57] F. Gothner, O. C. Spro, M. Hernes, and D. Peftitsis. Challenges of sic mosfet power cycling methodology. In *2018 20th European Conference on Power Electronics and Applications (EPE'18 ECCE Europe)*, pages P.1–P.8, Sep. 2018.

[58] X. Yuan. Application of silicon carbide (sic) power devices: Opportunities, challenges and potential solutions. In *IECON 2017 - 43rd Annual Conference of the IEEE Industrial Electronics Society*, pages 893–900, Oct 2017.

[59] U. Choi, F. Blaabjerg, and S. Jørgensen. Power cycling test methods for reliability assessment of power device modules in respect to temperature stress. *IEEE Transactions on Power Electronics*, 33(3):2531–2551, 2018.

[60] A. Wintrich, U. Nicolai, W. Tursky, and T. Reimann. Application manual power semiconductors. *Nuremberg, Germany: SEMIKRON International GmbH*, 2011.

[61] Wolfspeed website. Power products.

[62] Mitsubishi Electric website. Semiconductors & devices.

[63] Rohm semiconductor website. Products.

[64] N. Kaminski. Reliability challenges for sic power devices in systems and the impact on reliability testing. *Materials Science Forum*, 924:805–810, June 2018.

[65] J. Lutz. Packaging and reliability of power modules. *IEEE Conference Integrated Power Systems (CIPS)*, pages 1–8, 01 2014.

[66] A. Antonopoulos, S. D'Arco, M. Hernes, and D. Peftitsis. Challenges and strategies for a real-time implementation of a rainflow-counting algorithm for fatigue assessment of power modules. In *2019 IEEE Applied Power Electronics Conference and Exposition (APEC)*, pages 2708–2713, 2019.

[67] M. Matsuishi and T. Endo. Fatigue of metals subjected to varying stress. *Japan Society of Mechanical Engineers*, 68(2):37–40, 1968.

[68] D. Meneghel, E. d. C. Bortoni, and A. Karimi. Boosting dc/ac ratio of pv plant for bess integration on dc side. In *2018 IEEE Conference on Technologies for Sustainability (SusTech)*, pages 1–4, 2018.

[69] Y. Khawaja, D. Giaouris, H. Patsios, and M. Dahidah. Optimal cost-based model for sizing grid-connected pv and battery energy system. In *2017 IEEE Jordan Conference on Applied Electrical Engineering and Computing Technologies (AEECT)*, pages 1–6, 2017.

[70] K. Tytelmaier, O. Husev, O. Veligorskyi, and R. Yershov. A review of non-isolated bidirectional dc-dc converters for energy storage systems. In *2016 II International Young Scientists Forum on Applied Physics and Engineering (YSF)*, pages 22–28, 2016.

[71] S. Thomas, M. Stieneker, and R. W. De Doncker. Development of a modular high-power converter system for battery energy storage systems. In *Proceedings of the 2011 14th European Conference on Power Electronics and Applications*, pages 1–10, 2011.

[72] X. Li, D. Hui, and X. Lai. Battery energy storage station (bess)-based smoothing control of photovoltaic (pv) and wind power generation fluctuations. *IEEE Transactions on Sustainable Energy*, 4(2):464–473, 2013.

[73] C. S. Nalamati and R. Gupta. Isolated bidirectional battery converter control for standalone solar pv applications. In *2018 IEEMA Engineer Infinite Conference (eTechNxT)*, pages 1–5, 2018.

[74] A. Azidehak, R. Chattopadhyay, S. Acharya, A. K. Tripathi, M. G. Kashani, G. Chavan, and S. Bhattacharya. Control of modular dual active bridge dc/dc converter for photovoltaic integration. In *2015 IEEE Energy Conversion Congress and Exposition (ECCE)*, pages 3400–3406, 2015.

[75] C. S. Nalamati, A. Agrawa, and R. Gupta. Integration of multiple energy storage sections in solar pv based hmgs using multi-input dab. In *2018 IEEE International Conference on Power Electronics, Drives and Energy Systems (PEDES)*, pages 1–6, 2018.

[76] M. G. Villalva, J. R. Gazoli, and E. R. Filho. Comprehensive approach to modeling and simulation of photovoltaic arrays. *IEEE Transactions on Power Electronics*, 24(5):1198–1208, May 2009.

[77] S. D. Segaran. *Dynamic modelling and control of dual active bridge bi-directional DC DC converters for smart grid applications*. PhD thesis, School of Electrical and Computer Engineering (SECE), RMIT University, 2013.

[78] J. Everts. Design and optimization of an efficient (96.1%) and compact (2 kw/dm3) bidirectional isolated single-phase dual active bridge ac-dc converter. *Energies*, 9:799, 2016.

[79] T. Esram and P. L. Chapman. Comparison of photovoltaic array maximum power point tracking techniques. *IEEE Transactions on Energy Conversion*, 22(2):439–449, June 2007.

[80] A. Trivedi, A. Gupta, R. K. Pachauri, and Y. K. Chauhan. Comparison of perturb observe and ripple correlation control mppt algorithms for pv array. In *2016 IEEE 1st International Conference on Power Electronics, Intelligent Control and Energy Systems (ICPEICES)*, pages 1–5, July 2016.

[81] K. Jain, M. Gupta, and A. Kumar Bohre. Implementation and comparative analysis of po and inc mppt method for pv system. In *2018 8th IEEE India International Conference on Power Electronics (IICPE)*, pages 1–6, Dec 2018.

[82] B. Liu, S. Duan, F. Liu, and P. Xu. Analysis and improvement of maximum power point tracking algorithm based on incremental conductance method for photovoltaic array. In *2007 7th International Conference on Power Electronics and Drive Systems*, pages 637–641, Nov 2007.

[83] A. S. Ahmed, B. A. Abdullah, and W. G. A. Abdelaal. Mppt algorithms: Performance and evaluation. In *2016 11th International Conference on Computer Engineering Systems (ICCES)*, pages 461–467, Dec 2016.

[84] J. Hu, P. Joebges, and R. W. De Doncker. Maximum power point tracking control of a high power dc-dc converter for pv integration in mvdc distribution grids. In *2017 IEEE Applied Power Electronics Conference and Exposition (APEC)*, pages 1259–1266, March 2017.

[85] B. Zhao, Q. Song, W. Liu, and Y. Sun. Overview of dual-active-bridge isolated bidirectional dc–dc converter for high-frequency-link power-conversion system. *IEEE Transactions on Power Electronics*, 29(8):4091–4106, Aug 2014.

[86] R. Piveta, H. C. Sartori, L. Roggia, and J. R. Pinheiro. Circulating current mitigation in dual active bridge converter. In *2015 IEEE 13th Brazilian Power Electronics Conference and 1st Southern Power Electronics Conference (COBEP/SPEC)*, pages 1–6, Nov 2015.

[87] C. Calderon, A. Barrado, A. Rodriguez, P. Alou, A. Lazaro, C. Fernandez, and P. Zumel. General analysis of switching modes in a dual active bridge with triple phase shift modulation. *Energies*, 11(9):2419, Sep 2018.

[88] X. Fei, Z. Feng, N. PuQi, and W. Xuhui. Analyzing zvs soft switching using single phase shift control strategy of dual active bridge isolated dc-dc converters. In *2018 21st International Conference on Electrical Machines and Systems (ICEMS)*, pages 2378–2381, 2018.

[89] M. Kim, M. Rosekeit, S. Sul, and R. W. A. A. De Doncker. A dual-phase-shift control strategy for dual-active-bridge dc-dc converter in wide voltage range. In *8th International Conference on Power Electronics - ECCE Asia*, pages 364–371, May 2011.

[90] D Burley, R R Clements, P Dyke, D J G James, J Searl, N Steele, and Jerry H G Wright. *Advanced Modern Engineering Mathematics*. Prentice Hall, 4th edition, 2011.

[91] G. C. Goodwin, S. F. Graebe, and M. E. Salgado. *Control System Design*. Prentice Hall PTR, 1st edition, 2000.

[92] C. R. Dorf and H. R. Bishop. *Modern Control Systems*. Prentice Hall, 12th edition, 2001.

[93] F. Haugen. Article: Discretization of simulator, filter, and pid controller. *Modeling, Identification and Control, MIC*, May 2010.

[94] I. A. El- sharif, F. O. Hareb, and A. R. Zerek. Design of discrete-time pid controller. In *2nd International Conference on Control Engineering Information Technology (CEIT-2014)*, volume 8, pages 110–115, May 2014.

[95] Wolfspeed, Cree. *Silicon Carbide Power MOSFET, C3M0075120D Datasheet*.

[96] Fischer Elektronik. *LAM 5 D K 100 24 Datasheet*.

[97] Kyocera. *High efficiency multicrystal photovoltaic module, KC200GT Datasheet*.

[98] Plexim website. Thermal simulation.

[99] Henkel BERGQUIST. *Thermal Management Materials, Hi-Flow 300P Datasheet*.

[100] D. Peftitsis, G. Adamidis, P. Bakas, and A. Balouktsis. Photovoltaic system mpp-tracker investigation and implementation using dsp engine and buck - boost dc-dc converter. In *2008 13th International Power Electronics and Motion Control Conference*, pages 1840–1846, Sep. 2008.

[101] M. O. Badawy and Y. Sozer. Power flow management of a grid tied pv-battery system for electric vehicles charging. *IEEE Transactions on Industry Applications*, 53(2):1347–1357, 2017.

[102] Claudio Scali, G. Nardi, A. Landi, and A. Balestrino. Variable structure pi controllers in the presence of uncertainty and saturation. *IFAC Proceedings Volumes*, 26:637–642, 07 1993.

[103] R. Bayerer, T. Herrmann, T. Licht, J. Lutz, and M. Feller. Model for power cycling lifetime of igbt modules - various factors influencing lifetime. In *5th International Conference on Integrated Power Electronics Systems*, pages 1–6, 2008.

[104] M. Held, P. Jacob, G. Nicoletti, P. Scacco, and M. . Poech. Fast power cycling test of igbt modules in traction application. In *Proceedings of Second International Conference on Power Electronics and Drive Systems*, volume 1, pages 425–430 vol.1, 1997.

Appendix

V_{DS}	1200 V
$I_{D\ @\ 25°C}$	90 A
$R_{DS(on)}$	25 mΩ

C2M0025120D

Silicon Carbide Power MOSFET
C2M™ MOSFET Technology

N-Channel Enhancement Mode

Features

- High Blocking Voltage with Low On-Resistance
- High Speed Switching with Low Capacitances
- Easy to Parallel and Simple to Drive
- Avalanche Ruggedness
- Resistant to Latch-Up
- Halogen Free, RoHS Compliant

Benefits

- Higher System Efficiency
- Reduced Cooling Requirements
- Increased Power Density
- Increased System Switching Frequency

Applications

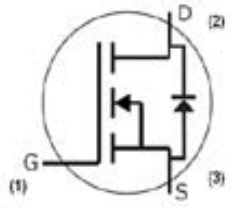
- Solar Inverters
- Switch Mode Power Supplies
- High Voltage DC/DC converters
- Battery Chargers
- Motor Drive
- Pulsed Power Applications

Package

TO-247-3

Halogen-Free

RoHS



Part Number	Package
C2M0025120D	TO-247-3

Maximum Ratings (T_C = 25 ˚C unless otherwise specified)

Symbol	Parameter	Value	Unit	Test Conditions	Note
V_{DSmax}	Drain - Source Voltage	1200	V	V_{GS} = 0 V, I_D = 100 µA	
V_{GSmax}	Gate - Source Voltage	-10/+25	V	Absolute maximum values	
V_{GSop}	Gate - Source Voltage	-5/+20	V	Recommended operational values	
I_D	Continuous Drain Current	90	A	V_{GS} =20 V, T_C = 25˚C	Fig. 19
		60		V_{GS} =20 V, T_C = 100˚C	
$I_{D(pulse)}$	Pulsed Drain Current	250	A	Pulse width t_P limited by T_{jmax}	Fig. 22
P_D	Power Dissipation	463	W	T_C=25˚C, T_J = 150 ˚C	Fig. 20
T_J , T_{stg}	Operating Junction and Storage Temperature	-55 to +150	˚C		
T_L	Solder Temperature	260	˚C	1.6mm (0.063") from case for 10s	
M_d	Mounting Torque	1 8.8	Nm lbf-in	M3 or 6-32 screw	

Electrical Characteristics (T_C = 25˚C unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions	Note
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	1200			V	V_{GS} = 0 V, I_D = 100 µA	
$V_{GS(th)}$	Gate Threshold Voltage	2.0	2.6	4	V	V_{DS} = V_{GS}, I_D = 15mA	Fig. 11
			2.1		V	V_{DS} = V_{GS}, I_D = 15mA, T_J = 150 °C	
I_{DSS}	Zero Gate Voltage Drain Current		2	100	µA	V_{DS} = 1200 V, V_{GS} = 0 V	
I_{GSS}	Gate-Source Leakage Current			600	nA	V_{GS} = 20 V, V_{DS} = 0 V	
$R_{DS(on)}$	Drain-Source On-State Resistance		25	34	mΩ	V_{GS} = 20 V, I_D = 50 A	Fig. 4,5,6
			43			V_{GS} = 20 V, I_D = 50 A, T_J = 150 °C	
g_{fs}	Transconductance		23.6		S	V_{DS}= 20 V, I_{DS}= 50 A	Fig. 7
			21.7			V_{DS}= 20 V, I_{DS}= 50 A, T_J = 150 °C	
C_{iss}	Input Capacitance		2788		pF	V_{GS} = 0 V V_{DS} = 1000 V f = 1 MHz V_{AC} = 25 mV	Fig. 17,18
C_{oss}	Output Capacitance		220				
C_{rss}	Reverse Transfer Capacitance		15				
E_{oss}	C_{oss} Stored Energy		121		µJ		Fig 16
E_{AS}	Avalanche Energy, Single Pluse		3.5		J	I_D = 50A, V_{DD} = 50V	Fig. 29
E_{ON}	Turn-On Switching Energy		1.4		mJ	V_{DS} = 800 V, V_{GS} = -5/20 V, I_D = 50A, $R_{G(ext)}$ = 2.5Ω,L= 412 µH	Fig. 25
E_{OFF}	Turn Off Switching Energy		0.3				
$t_{d(on)}$	Turn-On Delay Time		14		ns	V_{DD} = 800 V, V_{GS} = -5/20 V I_D = 50 A, $R_{G(ext)}$ = 2.5 Ω, R_L = 16 Ω Timing relative to V_{DS} Per IEC60747-8-4 pg 83	Fig. 27
t_r	Rise Time		32				
$t_{d(off)}$	Turn-Off Delay Time		29				
t_f	Fall Time		28				
$R_{G(int)}$	Internal Gate Resistance		1.1		Ω	f = 1 MHz, V_{AC} = 25 mV, ESR of C_{ISS}	
Q_{gs}	Gate to Source Charge		46		nC	V_{DS} = 800 V, V_{GS} = -5/20 V I_D = 50 A Per IEC60747-8-4 pg 83	Fig. 12
Q_{gd}	Gate to Drain Charge		50				
Q_g	Total Gate Charge		161				

Reverse Diode Characteristics

Symbol	Parameter	Typ.	Max.	Unit	Test Conditions	Note
V_{SD}	Diode Forward Voltage	3.3		V	V_{GS} = - 5 V, I_{SD} = 25 A	Fig. 8, 9, 10
		3.1		V	V_{GS} = - 5 V, I_{SD} = 25 A, T_J = 150 °C	
I_S	Continuous Diode Forward Current		90		T_C= 25 °C	Note 1
t_{rr}	Reverse Recovery Time	45		ns	V_{GS} = - 5 V, I_{SD} = 50 A ,T_J = 25 °C VR = 800 V dif/dt = 1000 A/µs	Note 1
Q_{rr}	Reverse Recovery Charge	406		nC		
I_{rrm}	Peak Reverse Recovery Current	13.5		A		

Note (1): When using SiC Body Diode the maximum recommended V_{GS} = -5V

Thermal Characteristics

Symbol	Parameter	Typ.	Max.	Unit	Test Conditions	Note
$R_{\theta JC}$	Thermal Resistance from Junction to Case	0.24	0.27	°C/W		Fig. 21
$R_{\theta JC}$	Thermal Resistance from Junction to Ambient		40			

Typical Performance

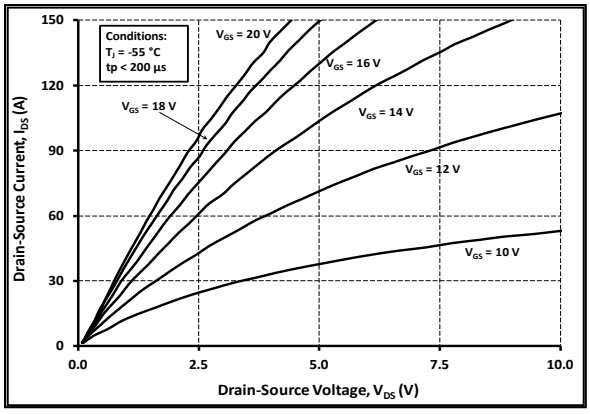


Figure 1. Output Characteristics T_J = -55 °C

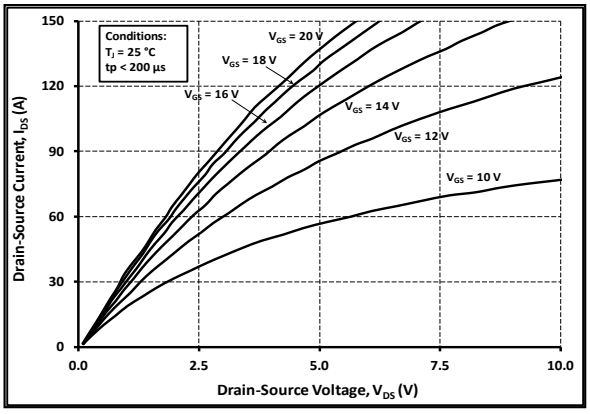


Figure 2. Output Characteristics T_J = 25 °C

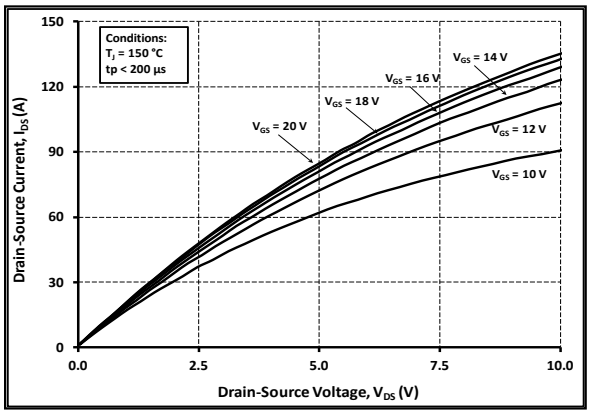


Figure 3. Output Characteristics T_J = 150 °C

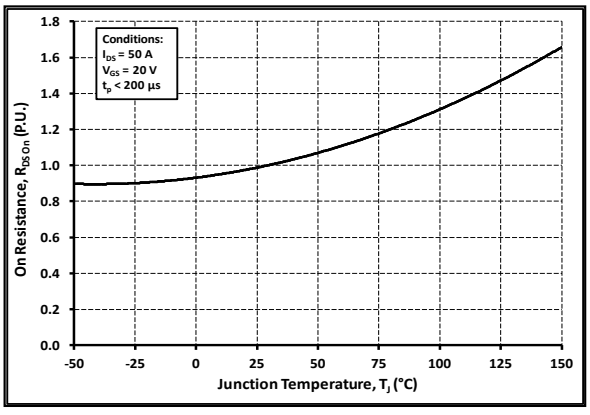


Figure 4. Normalized On-Resistance vs. Temperature

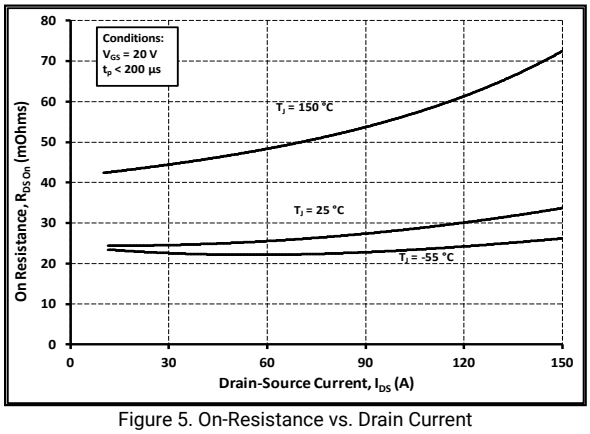


Figure 5. On-Resistance vs. Drain Current
For Various Temperatures

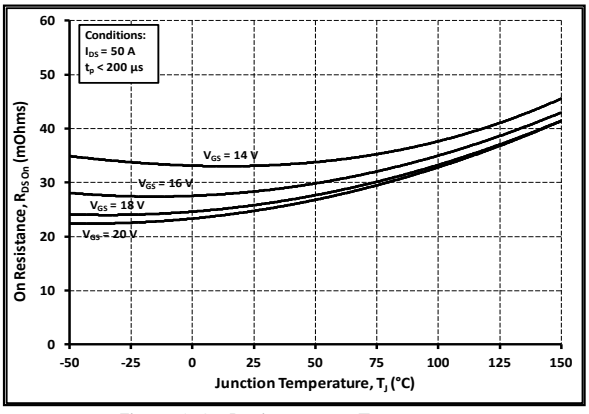


Figure 6. On-Resistance vs. Temperature
For Various Gate Voltage

Typical Performance

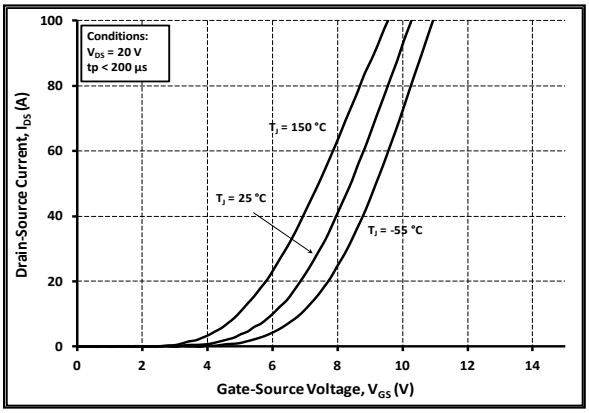


Figure 7. Transfer Characteristic For Various Junction Temperatures

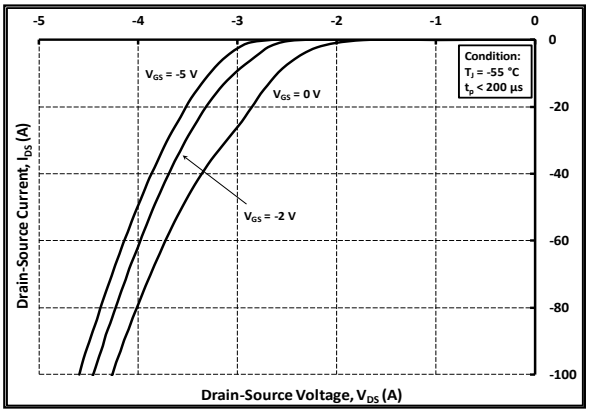


Figure 8. Body Diode Characteristic at -55 ºC

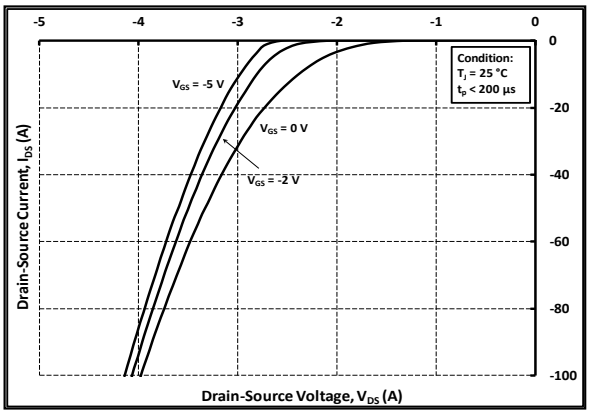


Figure 9. Body Diode Characteristic at 25 ºC

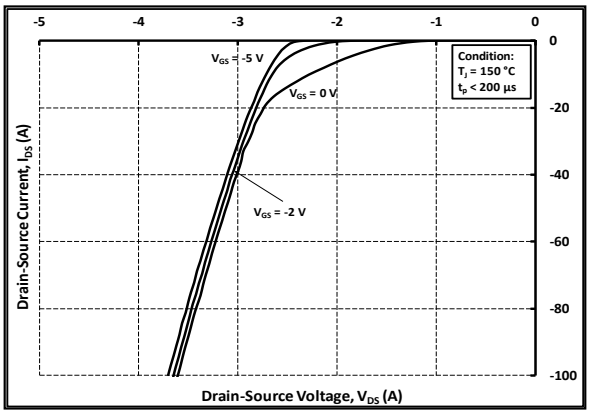


Figure 10. Body Diode Characteristic at 150 ºC

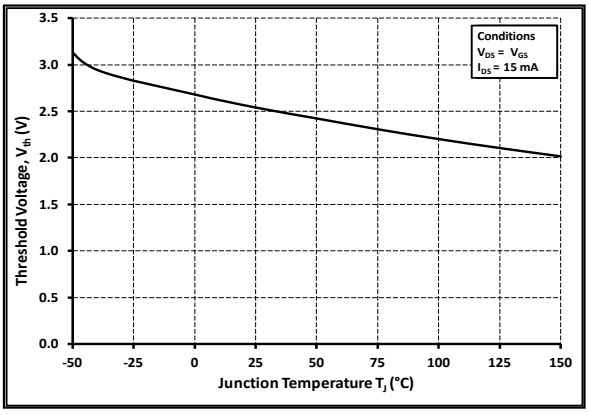


Figure 11. Threshold Voltage vs. Temperature

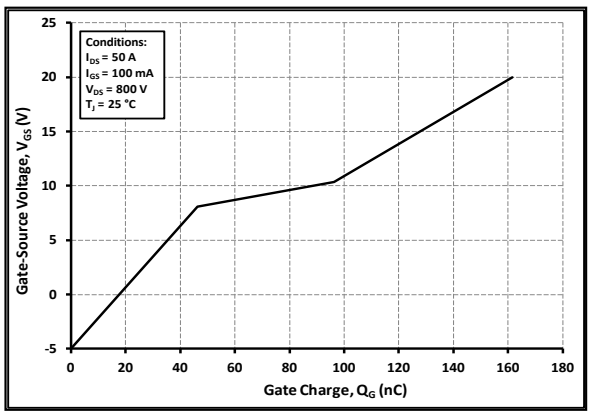


Figure 12. Gate Charge Characteristic

Typical Performance

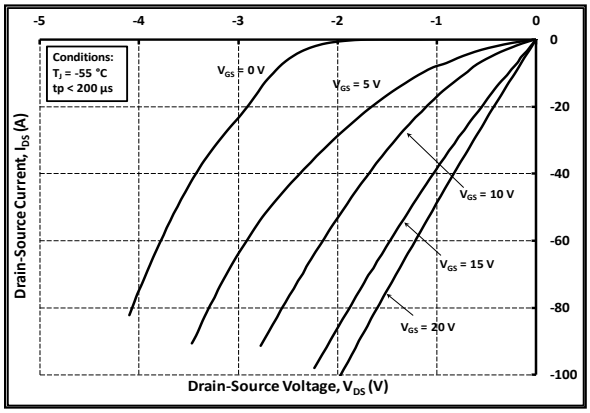


Figure 13. 3rd Quadrant Characteristic at -55 °C

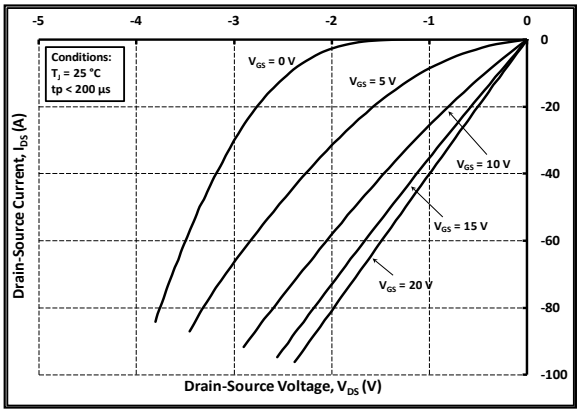


Figure 14. 3rd Quadrant Characteristic at 25 °C

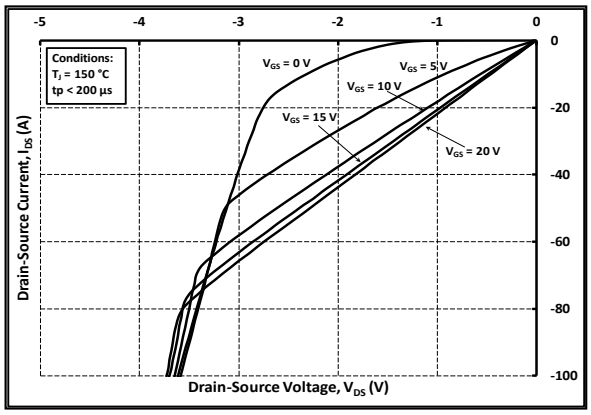


Figure 15. 3rd Quadrant Characteristic at 150 °C

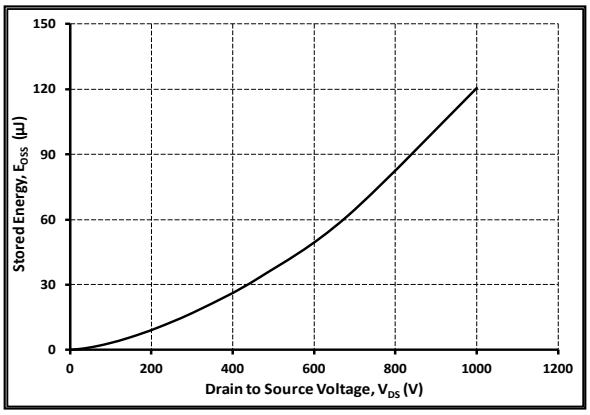


Figure 16. Output Capacitor Stored Energy

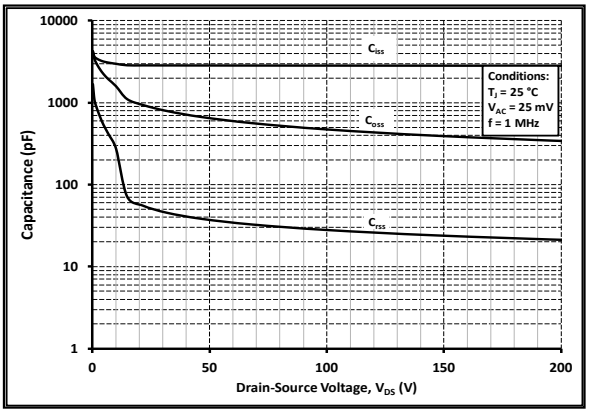


Figure 17. Capacitances vs. Drain-Source Voltage (0-200 V)

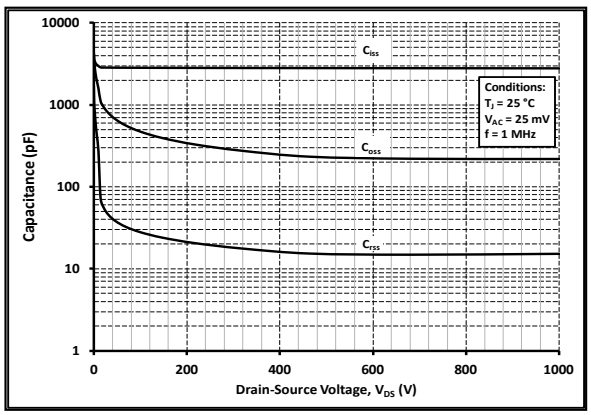


Figure 18. Capacitances vs. Drain-Source Voltage (0-1000 V)

Typical Performance

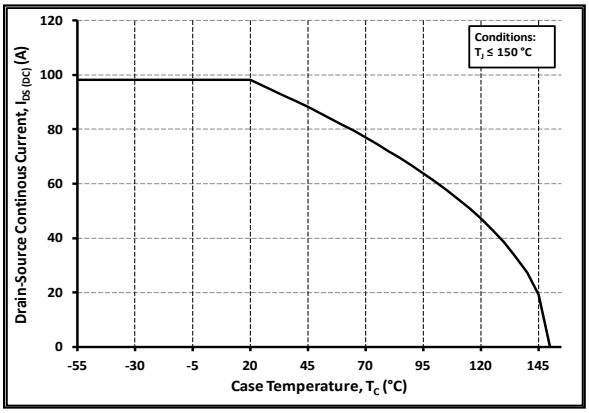


Figure 19. Continuous Drain Current Derating vs. Case Temperature

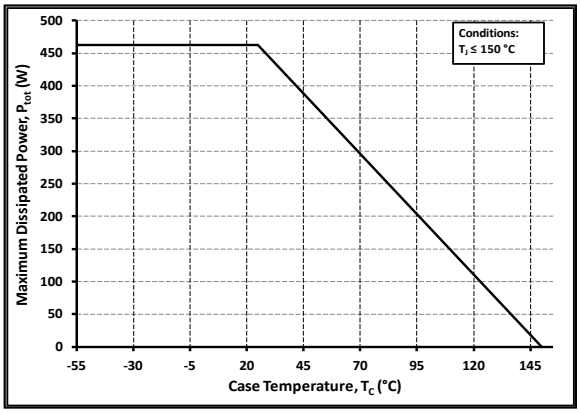


Figure 20. Maximum Power Dissipation Derating vs. Case Temperature

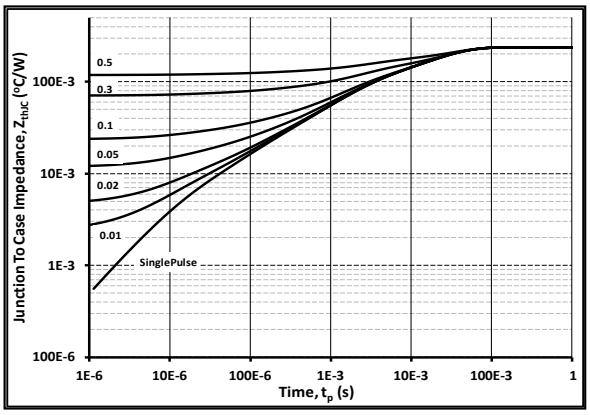


Figure 21. Transient Thermal Impedance (Junction - Case)

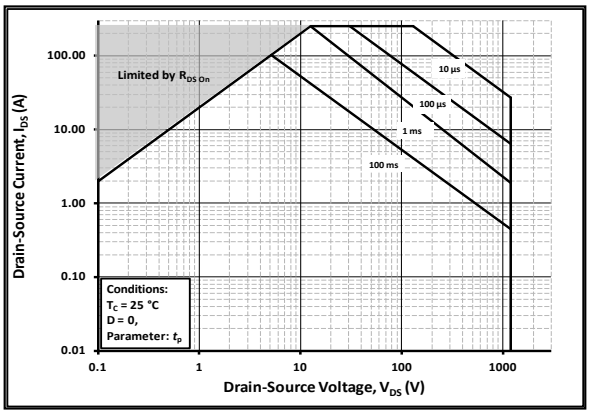


Figure 22. Safe Operating Area

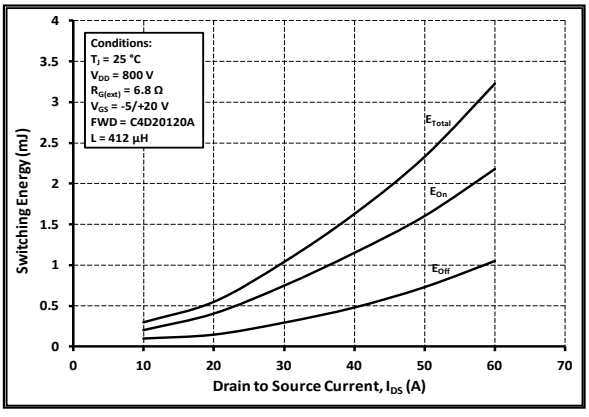


Figure 23. Clamped Inductive Switching Energy vs. Drain Current (V_{DD} = 800V)

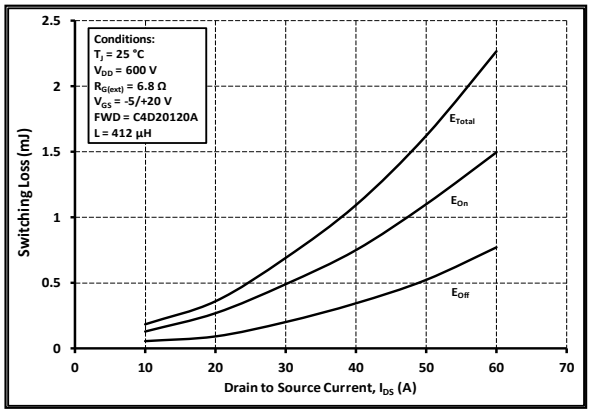


Figure 24. Clamped Inductive Switching Energy vs. Drain Current (V_{DD} = 600V)

Typical Performance

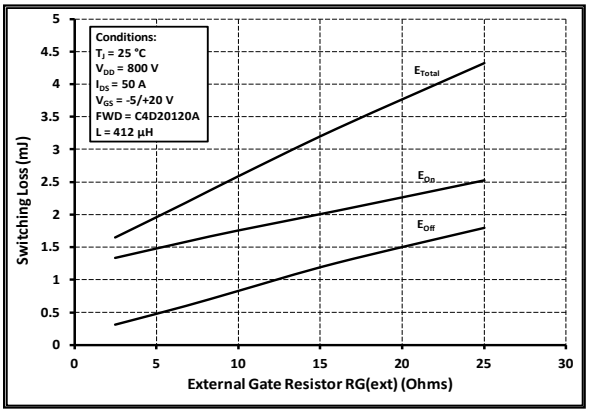


Figure 25. Clamped Inductive Switching Energy vs. $R_{G(ext)}$

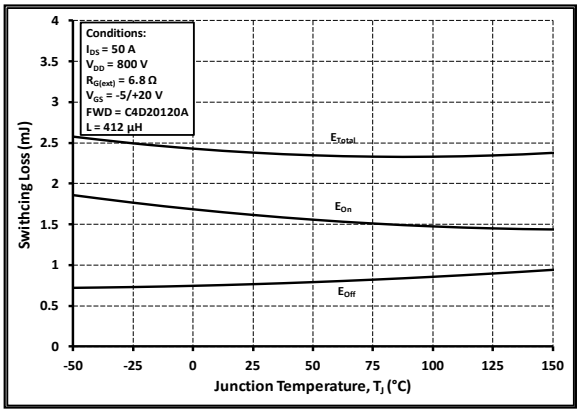


Figure 26. Clamped Inductive Switching Energy vs. Temperature

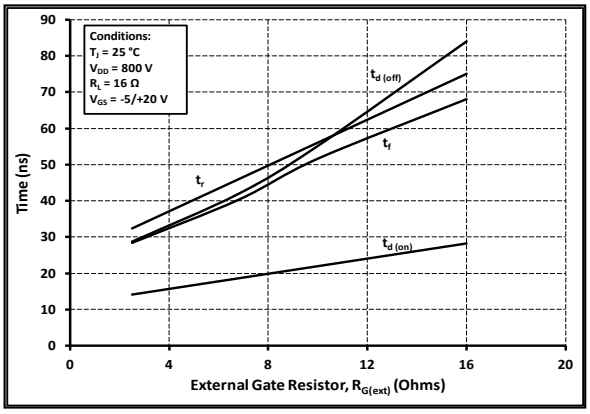


Figure 27. Switching Times vs. $R_{G(ext)}$

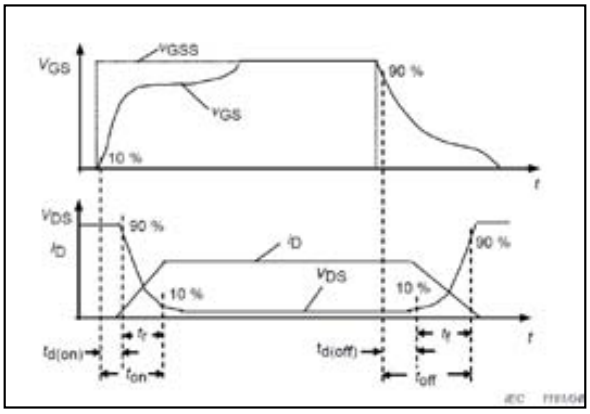


Figure 28. Switching Times Definition

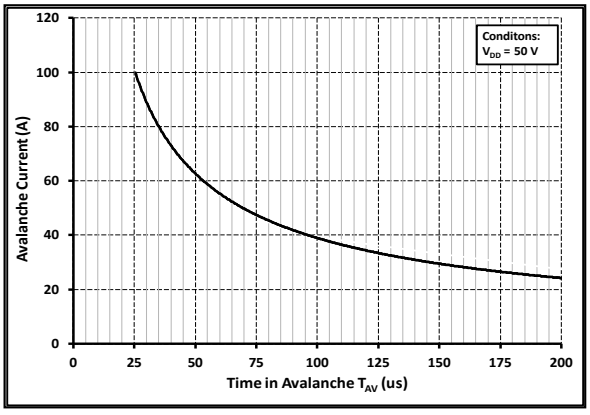


Figure 29. Single Avalanche SOA curve

Test Circuit Schematic

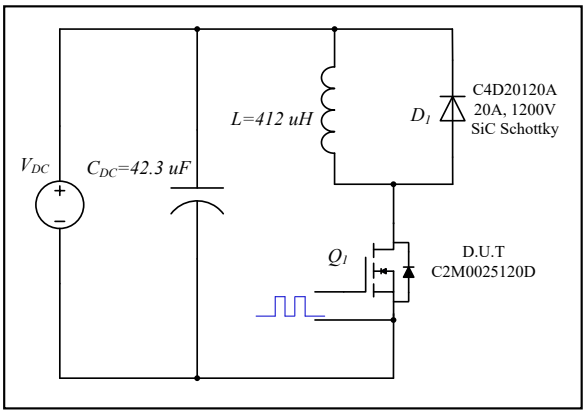


Figure 30. Clamped Inductive Switching Waveform Test Circuit

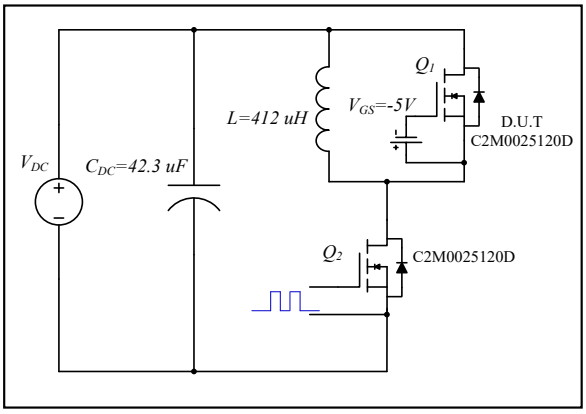


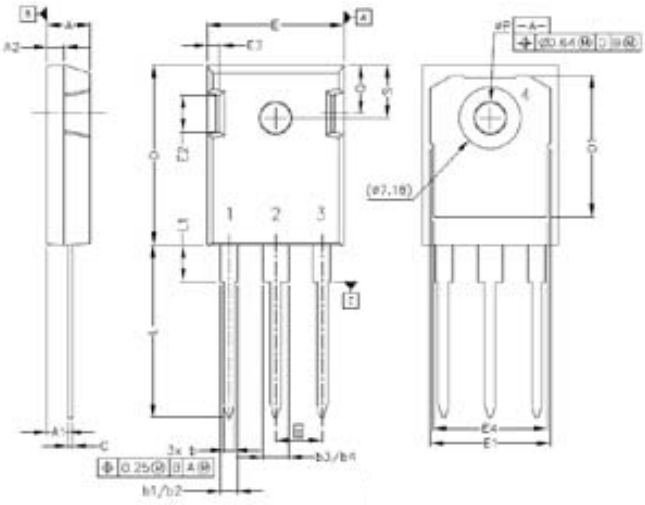
Figure 31. Body Diode Recovery Test Circuit

ESD Ratings

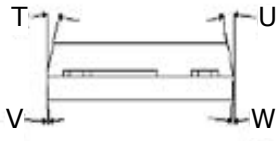
ESD Test	Total Devices Sampled	Resulting Classification
ESD-HBM	All Devices Passed 1000V	2 (>2000V)
ESD-MM	All Devices Passed 400V	C (>400V)
ESD-CDM	All Devices Passed 1000V	IV (>1000V)

Package Dimensions

Package TO-247-3



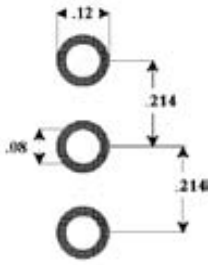
POS	Inches		Millimeters	
	Min	Max	Min	Max
A	.190	.205	4.83	5.21
A1	.090	.100	2.29	2.54
A2	.075	.085	1.91	2.16
b	.042	.052	1.07	1.33
b1	.075	.095	1.91	2.41
b2	.075	.085	1.91	2.16
b3	.113	.133	2.87	3.38
b4	.113	.123	2.87	3.13
c	.022	.027	0.55	0.68
D	.819	.831	20.80	21.10
D1	.640	.695	16.25	17.65
D2	.037	.049	0.95	1.25
E	.620	.635	15.75	16.13
E1	.516	.557	13.10	14.15
E2	.145	.201	3.68	5.10
E3	.039	.075	1.00	1.90
E4	.487	.529	12.38	13.43
e	.214 BSC		5.44 BSC	
N	3		3	
L	.780	.800	19.81	20.32
L1	.161	.173	4.10	4.40
ØP	.138	.144	3.51	3.65
Q	.216	.236	5.49	6.00
S	.238	.248	6.04	6.30
T	9°	11°	9°	11°
U	9°	11°	9°	11°
V	2°	8°	2°	8°
W	2°	8°	2°	8°



Pinout Information:

- Pin 1 = Gate
- Pin 2, 4 = Drain
- Pin 3 = Source

Recommended Solder Pad Layout



TO-247-3

Part Number	Package	Marking
C2M0025120D	TO-247-3	C2M0025120

Notes

- **RoHS Compliance**
  The levels of RoHS restricted materials in this product are below the maximum concentration values (also referred to as the threshold limits) permitted for such substances, or are used in an exempted application, in accordance with EU Directive 2011/65/EC (RoHS2), as implemented January 2, 2013. RoHS Declarations for this product can be obtained from your Cree representative or from the Product Documentation sections of www.cree.com.

- **REACh Compliance**
  REACh substances of high concern (SVHCs) information is available for this product. Since the European Chemical Agency (ECHA) has published notice of their intent to frequently revise the SVHC listing for the foreseeable future,please contact a Cree representative to insure you get the most up-to-date REACh SVHC Declaration. REACh banned substance information (REACh Article 67) is also available upon request.

- This product has not been designed or tested for use in, and is not intended for use in, applications implanted into the human body nor in applications in which failure of the product could lead to death, personal injury or property damage, including but not limited to equipment used in the operation of nuclear facilities, life-support machines, cardiac defibrillators or similar emergency medical equipment, aircraft navigation or communication or control systems, air traffic control systems.

Related Links

- **C2M PSPICE Models: http://wolfspeed.com/power/tools-and-support**
- **SiC MOSFET Isolated Gate Driver reference design: http://wolfspeed.com/power/tools-and-support**
- **SiC MOSFET Evaluation Board: http://wolfspeed.com/power/tools-and-support**

Cree, Inc.
4600 Silicon Drive
Durham, NC 27703
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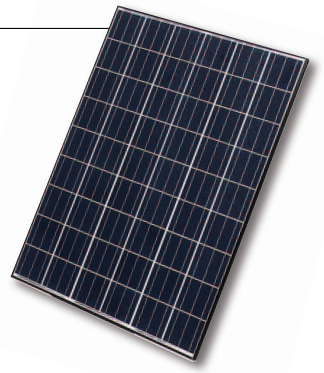
Fax: +1.919.313.5451
www.cree.com/power

THE NEW VALUE FRONTIER

KYOCERA

KC200GT

HIGH EFFICIENCY MULTICRYSTAL
PHOTOVOLTAIC MODULE



LISTED

HIGHLIGHTS OF KYOCERA PHOTOVOLTAIC MODULES

Kyocera's advanced cell processing technology and automated production facilities produce a highly efficient multicrystal photovoltaic module.
The conversion efficiency of the Kyocera solar cell is over 16%.
These cells are encapsulated between a tempered glass cover and a pottant with back sheet to provide efficient protection from the severest environmental conditions.
The entire laminate is installed in an anodized aluminum frame to provide structural strength and ease of installation.
Equipped with plug-in connectors.

APPLICATIONS

KC200GT is ideal for grid tie system applications.

- Residential roof top systems
- Large commercial grid tie systems
- Water Pumping systems
- High Voltage stand alone systems
- etc.

QUALIFICATIONS

- **MODULE** : UL1703 certified
- **FACTORY** : ISO9001 and ISO 14001

QUALITY ASSURANCE

Kyocera multicrystal photovoltaic modules have passed the following tests.

- Thermal cycling test
- Thermal shock test
- Thermal / Freezing and high humidity cycling test
- Electrical isolation test
- Hail impact test
- Mechanical, wind and twist loading test
- Salt mist test
- Light and water-exposure test
- Field exposure test

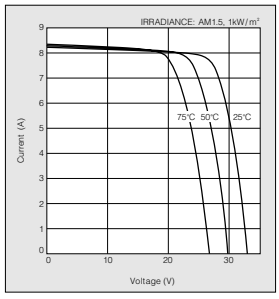
LIMITED WARRANTY

※1 year limited warranty on material and workmanship
※20 years limited warranty on power output: For detail, please refer to "category IV" in Warranty issued by Kyocera

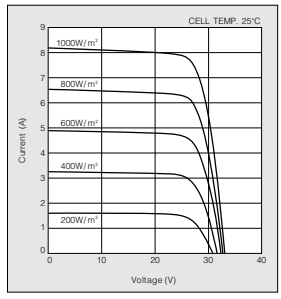
(Long term output warranty shall warrant if PV Module(s) exhibits power output of less than 90% of the original minimum rated power specified at the time of sale within 10 years and less than 80% within 20 years after the date of sale to the Customer. The power output values shall be those measured under Kyocera's standard measurement conditions. Regarding the warranty conditions in detail, please refer to Warranty issued by Kyocera)

ELECTRICAL CHARACTERISTICS

Current-Voltage characteristics of Photovoltaic Module KC200GT at various cell temperatures



Current-Voltage characteristics of Photovoltaic Module KC200GT at various irradiance levels

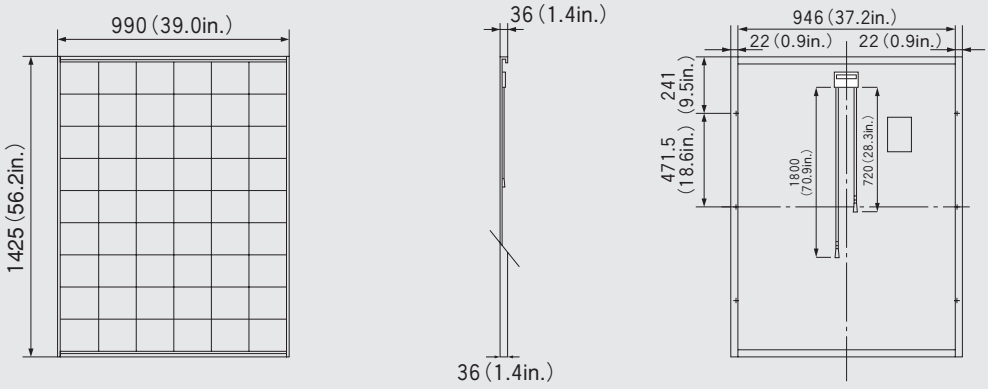


SPECIFICATIONS

KC200GT

Physical Specifications

Unit : mm (in.)



Specifications

Electrical Performance under Standard Test Conditions (*STC)	
Maximum Power (Pmax)	200W (+10%/−5%)
Maximum Power Voltage (Vmpp)	26.3V
Maximum Power Current (Impp)	7.61A
Open Circuit Voltage (Voc)	32.9V
Short Circuit Current (Isc)	8.21A
Max System Voltage	600V
Temperature Coefficient of Voc	-1.23×10^{-1} V/℃
Temperature Coefficient of Isc	3.18×10^{-3} A/℃

*STC : Irradiance 1000W/m², AM1.5 spectrum, module temperture 25℃

Electrical Performance at 800W/m², NOCT, AM1.5	
Maximum Power (Pmax)	142W
Maximum Power Voltage (Vmpp)	23.2V
Maximum Power Current (Impp)	6.13A
Open Circuit Voltage (Voc)	29.9V
Short Circuit Current (Isc)	6.62A

NOCT (Nominal Operating Cell Temperature) : 47℃

Cells	
Number per Module	54

Module Characteristics	
Length × Width × Depth	1425mm(56.2in)×990mm(39.0in)×36mm(1.4in)
Weight	18.5kg(40.7lbs.)
Cable	(+)720mm(28.3in),(-)1800mm(70.9in)

Junction Box Characteristics	
Length × Width × Depth	113.6mm(4.5in)×76mm(3.0in)×9mm(0.4in)
IP Code	IP65

Reduction of Efficiency under Low Irradiance	
Reduction	7.8%

Reduction of efficiency from an irrandiance of 1000W/m² to 200W/m² (module temperature 25℃)

Please contact our office for further information

KYOCERA

KYOCERA Corporation

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http://www.kyocera.com

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http://www.kyocerasolar.com

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http://www.kyocerasolar.com.au/

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● KYOCERA Asia Pacific Ltd.
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Tsimshatsui East, Kowloon, Hong Kong
TEL:(852)2-7237183 FAX:(852)2-7244501

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● KYOCERA(Tianjin) Sales & Trading Corporation
19F, Tower C HeQiao Building 8A GuangHua Rd.,
Chao Yang District, Beijing 100026, China
TEL:(86)10-6583-2270 FAX:(86)10-6583-2250

BERGQUIST

Technical Data Sheet

Hi-Flow® 300P

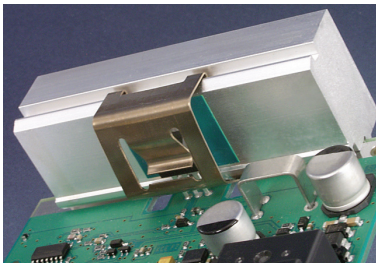
November 2013

PRODUCT DESCRIPTION

Electrically Insulating,Thermally Conductive Phase Change Material

FEATURES AND BENEFITS

- Thermal impedance: 0.13°C-in2/W (@25 psi)
- Field-proven polyimide film
  - excellent dielectric performance
  - excellent cut-through resistance
- Outstanding thermal performance in an insulated pad



Hi-Flow® 300P consists of a thermally conductive 55°C phase change compound coated on a thermally conductive polyimide film.The polyimide reinforcement makes the material easy to handle and the 55°C phase change temperature minimizes shipping and handling problems.

Hi-Flow® 300P achieves superior values in voltage breakdown and thermal performance when compared to its competition.The product is supplied on an easy release liner for exceptional handling in high volume manual assemblies. Hi-Flow 300P is designed for use as a thermal interface material between electronic power devices requiring electrical isolation to the heat sink.

Bergquist suggests the use of spring clips to assure constant pressure with the interface and power source. Please refer to thermal performance data to determine nominal spring pressure for your application.

Note: To build a part number, visit our website at www.bergquistcompany.com.

TYPICAL PROPERTIES OF HI-FLOW 300P

PROPERTY	IMPERIAL VALUE	METRIC VALUE	TEST METHOD
Color	Green	Green	Visual
Reinforcement Carrier	Polyimide	Polyimide	—
Thickness (inch) / (mm)	0.004 - 0.005	0.102 - 0.127	ASTM D374
Film Thickness (inch) / (mm)	0.001 - 0.002	0.025 - 0.050	ASTM D374
Elongation (%)	40	40	ASTM D882A
Tensile Strength (psi) / (MPa)	7000	48	ASTM D882A
Continuous Use Temp (°F) / (°C)	302	150	—
Phase Change Temp (°F) / (°C)	131	55	ASTM D3418
ELECTRICAL			
Dielectric Breakdown Voltage (Vac)	5000	5000	ASTM D149
Dielectric Constant (1000 Hz)	4.5	4.5	ASTM D150
Volume Resistivity (Ohm-meter)	10^{12}	10^{12}	ASTM D257
Flame Rating	V-O	V-O	U.L. 94
THERMAL			
Thermal Conductivity (W/m-K) (1)	1.6	1.6	ASTM D5470

THERMAL PERFORMANCE vs PRESSURE					
Pressure (psi)	10	25	50	100	200
TO-220 Thermal Performance (°C/W) 0.0010"	0.95	0.94	0.92	0.91	0.90
TO-220 Thermal Performance (°C/W) 0.0015"	1.19	1.17	1.16	1.14	1.12
TO-220 Thermal Performance (°C/W) 0.0020"	1.38	1.37	1.35	1.33	1.32
Thermal Impedance (°C-in²/W) 0.0010" (2)	0.13	0.13	0.12	0.12	0.12
Thermal Impedance (°C-in²/W) 0.0015" (2)	0.17	0.16	0.16	0.16	0.15
Thermal Impedance (°C-in²/W) 0.0020" (2)	0.19	0.19	0.19	0.18	0.18

1) This is the measured thermal conductivity of the Hi-Flow coating. It represents one conducting layer in a three-layer laminate. The Hi-Flow coatings are phase change compounds. These layers will respond to heat and pressure induced stresses. The overall conductivity of the material in post-phase change, thin film products is highly dependent upon the heat and pressure applied. This characteristic is not accounted for in ASTM D5470. Please contact Bergquist Product Management if additional specifications are required.
2) The ASTM D5470 test fixture was used and the test sample was conditioned at 70°C prior to test. The recorded value includes interfacial thermal resistance. These values are provided for reference only. Actual application performance is directly related to the surface roughness, flatness and pressure applied.

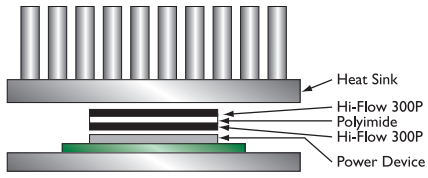
TYPICAL APPLICATIONS INCLUDE

- Spring / clip mounted
- Discrete power semiconductors and modules

CONFIGURATIONS AVAILABLE

- Roll form, die-cut parts and sheet form, dry both sides

We produce thousands of specials. Tooling charges vary depending on tolerances and complexity of the part.



Henkel

Disclaimer

Note:

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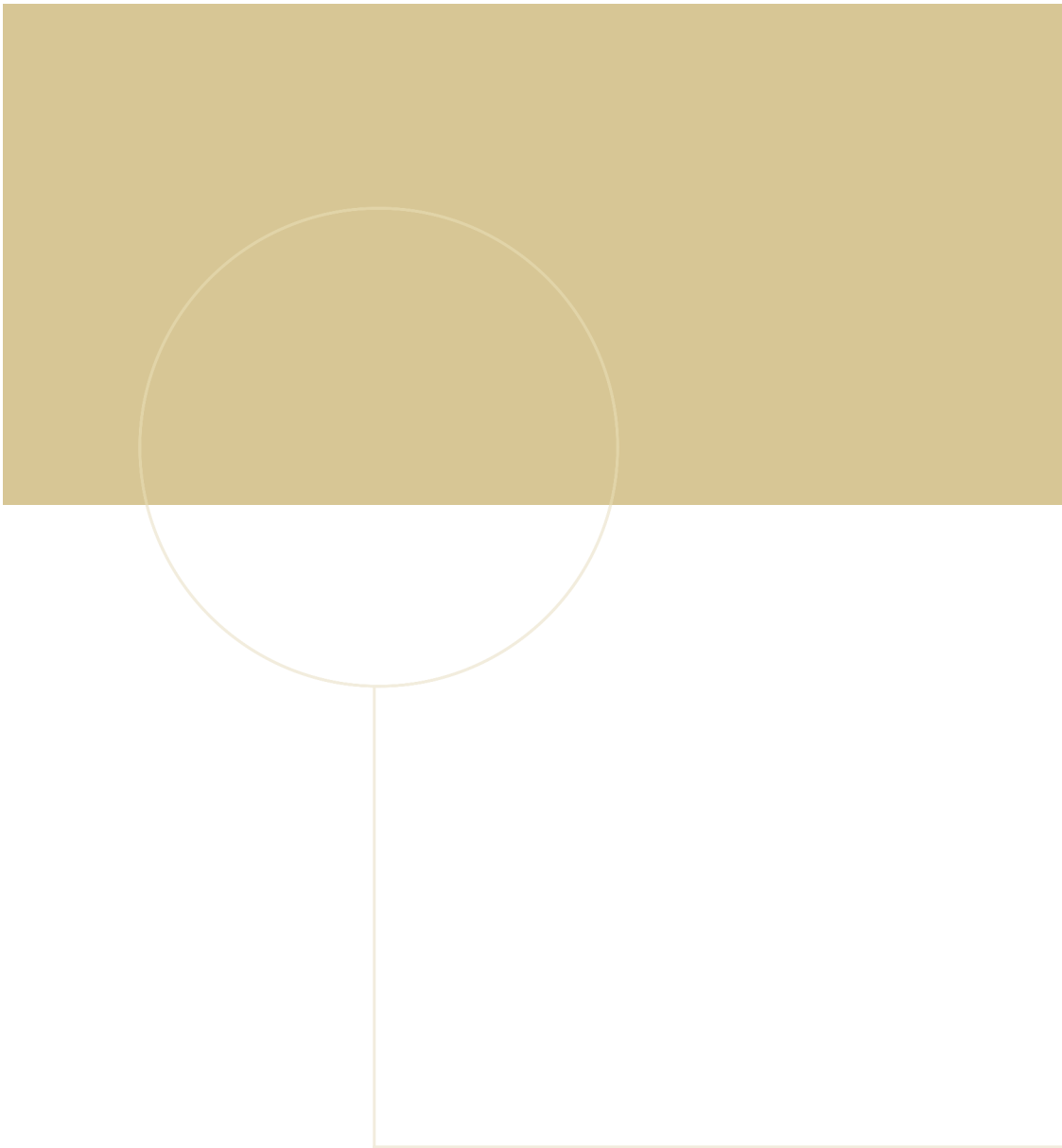

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