Master's thesis

NTNU
Norwegian University of Science and Technology
Faculty of Information Technology and Electrical Engineering
Department of Electric Power Engineering

Tobias Nieckula Ubostad

Investigation of parasitics and thermal performance of a SiC MOSFET power module using FEM and LTSpice

Master's thesis in Energy and Environmental Engineering
Supervisor: Dimosthenis Peftitsis
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Sammendrag

I denne masteroppgaven analyseres ytelsen til SiC halvbro-modulen CAS300M12BM2 fra Cree gjennom datasimuleringsverktøy. De viktigste bidragsyterne til parasittisk induktans i modulen har blitt identifisert og deres innvirkning på svitsjekarakteristikken blir studert. Videre utføres en termisk analyse for å studere temperaturfordelingen i modulen.

En modell av modulen er utviklet i ANSYS slik at den kan etterligne den kommersielt tilgjengelige modulen fra Cree. Q3D Extractor ble brukt til å trekke ut de parasittiske induktansene og motstandene til modulen. Dobbel-puls tester i LTSpice ble gjennomført for å vurdere modulens svitsje-ytelse og effekten av parasittisk induktans. Videre ble en forbedret utforming av modulens kraftterminaler undersøkt.

Studien fant at modulen ikke er egnet for drift under høy temperatur på grunn av den spesifikke plasseringen av SiC MOSFET chippene. FEM-simuleringene avslørte også at de store kraftterminalene er hovedkilden til parasittisk induktans i modulen. Analysen i LTSpice viste at disse induktansene fører til overspenninger og oscillasjoner i strøm- og spenningsbølgene.

Videre ble tre forbedrede utforminger av hovedterminalene til modulen foreslått og undersøkt, slik at overspenningene og oscillasjonene kan reduseres. De foreslåtte terminalene tar større nytte av magnetiske fluksannulerende effekter, og reduserer effektivt den totale strømsløyfeinduktansen til modulen. Simuleringer av de nye terminalene i LTSpice viste at overspenningene blir redusert og svitsjeenergien ble redusert derav.

Abstract

In this thesis, the performance of the half-bridge SiC power module CAS300M12BM2 from Cree is analyzed through computer simulation tools. The largest contributors to the parasitic inductance internal to the module are identified and their impact on switching performance is studied. Furthermore, a thermal analysis is performed to study the temperature distribution in the module.

A model of the module has been developed in ANSYS so that it can emulate the commercially available module from Cree. Q3D Extractor was used to extract the parasitic inductances and resistances of the module. Double-pulse tests in LTSpice were used to assess the switching performance and the effect of stray inductance. Moreover, an improved design for the power terminals of the module was investigated.

Through the investigation is was found that the module is not properly fit for high-temperature operation due the specific placement of SiC MOSFET dies. The FEM simulations did also reveal that the large power terminals are the main source of stray inductance in the module. The analysis in LTSpice showed that these stray inductance lead to voltage overshoots and ringing in the current and voltage waveforms.

Consequently, a three improved new power terminal designs were suggested and investigated so that the voltage overshoots and oscillations could be reduced. The suggested terminals take a larger advantage of magnetic flux cancelling effects, which effectively reduce the total power loop inductance in the module. Simulations of the new design in LTSpice showed that the voltage overshoots were reduced and there was an improvement to the switching energy.

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List of acronyms

AC	Alternating Current
AlN	Aluminium Nitride
BJT	Bipolar Junction Transistor
CFD	Computational Fluid Dynamics
Cu	Copper
DBC	Direct Bonded Copper
DC	Direct Current
DPT	Double-Pulse Test
DUT	Device Under Test
FEM	Finite Element Method
FRD	Fast Recovery Diode
HV	High Voltage
IGBT	Insulated-Gate Bipolar Transistor
LC	Inductor-Capacitor
MoM	Method of Moments
MOSFET	Metal-Oxide-Semiconductor Field-Effect-Transistor
Pb	Lead
PCB	Printed Circuit Board
RLC	Resistance-Inductance-Capacitance
SBD	Schottky Barrier Diode
Si	Silicon
SiC	Silicon Carbide
Sn	Tin
SPICE	Simulation Program with Integrated Circuit Emphasis
WBG	Wide Bandgap

1 Introduction

This section will present the scope and motivation of the thesis and briefly explain the outline of the report.

1.1 Background

The strong focus on renewable energy sources and environmental considerations have made power electronic solutions in the transportation and energy sector increasingly popular, as these sectors are responsible for a large percentage of the greenhouse gas emissions. However, for the electrification of the these sectors to succeed, existing solutions have to be improved to that they can meet the specific requirements of the applications. For instance, in the transportation section there strict demand for compact and reliable solutions. In order to achieve this, it is desirable to reduce the losses of the power electronics systems, which would reduce the size of the cooling solution. In addition, the size of the passive components can also be reduced by increasing the operating frequency of the converters [1].

However, the existing power semiconductor technology based on Si is reaching its theoretical limit in terms of switching and conduction performance, as well as voltage ratings [2]. They have relatively high losses and limited switching speed, which limits any improvements to the power density, as the passive and cooling components must be larger.

SiC semiconductors have become increasingly popular in last decade as a replacement for Si. MOSFETs based on SiC material are able to attain very high switching speeds and higher junction temperatures. Hence, SiC MOSFETs can be solution to the previously mentioned challenges and open up for development of power modules with power densities that are currently not attainable with existing Si technology. However, commercially available power modules today are still based on designs similar to existing Si IGBT modules, which limits both the switching speed and thermal performance of the module.

SiC MOSFETs are especially sensitive to parasitic inductance that are present internally in power modules, as they induce overvoltages and oscillations due to the fast switching of SiC. Therefore, the superior characteristics of SiC are not utilized fully. The main contributors to this parasitic inductance must be identified and understood, so that proper steps can be taken to improve SiC power modules. In this thesis a commercially available SiC MOSFET half-bridge power module will be investigated to understand how the different parts of the module contribute to the stray inductance and how it affects the switching characteristics. Additionally, the thermal performance of the module will be investigated.

1.2 Objective and scope of work

In this thesis the aim is to recreate and simulate a conventional SiC MOSFET power module in FEM software. The selected module is the CAS300M12BM2 half-bridge power module from Cree, and it is rated for 1.2 kV, 300 A and 150 °C. The geometry of the power

module will be realized in 3D modelling software ANSYS Electronics, which contain several other modules for electrical and thermal analysis. The parasitic components of the module will be investigated and extracted by using Q3D Extractor. The extracted values will be used to create a model of the electrical circuit layout for analysis in the circuit simulator LTSpice so that the switching behavior can be evaluated.

In addition to this, the thermal performance of the module will be evaluated by using Icepak, to showcase how the thermal design of the module is not properly fit to take advantage of the superior thermal characteristics of SiC MOSFETs.

Thus, the entire thesis will be based on using computer simulations tools to conduct the investigation. As the computer simulation tools are becoming more accurate, the use of them has become a standard among researchers and manufacturers. Experimentation and testing through computer tools have become a vital part of the design process for power electronic components, as several different variations of the components can be investigated through simulation before a physical prototype can be built and tested.

1.3 Layout of the thesis

This thesis is structured into seven chapters, where Chapter 1 is an introduction of the problem and objective. In Chapter 2, the properties of SiC is presented, as well as theory required to understand how state-of-the-art SiC semiconductors work and are limited by parasitic components.

Chapter 3 gives a brief literature review of power module packaging approaches and trends. Some industry standard layouts are presented and few new state-of-the-art designs are shown. Furthermore, the inductive design of power modules is discussed thoroughly.

In Chapter 4 the CAS300M12BM2 power module is implemented in the FEM software ANSYS Q3D Extractor. The creation of 3D design is presented and the parasitic components are extracted through FEM simulations. Relevant theory to understand how the parasitic components interact with each other and how the software algorithm works is given as well. Furthermore, a thermal analysis of the power module is also conducted and different methods of modelling the heatsink are presented to show how they affect the results from the FEM simulations.

In Chapter 5 the inductive design of the power module is realized in LTSpice and double-pulse testing is done to evaluate the switching behavior of the module. The switching energy losses, voltage overshoots and oscillations in the main waveforms are discussed and compared with the physical module.

In Chapter 6 an improved design of the main power terminal geometry is presented. It results in significantly lower power loop inductance, which leads to better switching characteristics. The new design is implemented in LTSpice to assess the new switching waveforms and the results and challenges with the design are discussed.

Finally, in Chapter 7 conclusions are drawn from the entire thesis and suggestions for further work are laid out.

2 High power semiconductor devices based on Silicon Carbide

In this chapter the properties of the SiC material will be presented and compared to Si material. After that, some state-of-the-art SiC devices will be presented together with a detailed analysis of the operation of the devices.

2.1 The properties of SiC material

SiC is wide bandgap material, that is: a material with significantly higher bandgap than Si and it is measured in electronvolt (eV). The definition of bandgap is the energy difference between the valence band and the conduction band of a solid material and it is given together with other important material properties of SiC and Si in Table 2.1.

Table 2.1: Key material properties of Si and SiC [3].

Property	Si	4H-SiC
Bandgap energy (eV)	1.1	3.2
Critical electric field (MV/cm)	0.3	3.5
Electron saturation velocity (cm/s) x10^7	1.0	2.2
Electron mobility (cm^2/Vs)	1350	720
Thermal conductivity (W/(cm·K))	1.5	5
Dielectric constant	11.3	10

These properties are well suited to explain why SiC can make power converters more compact and efficient. The higher bandgap energy reduces the leakage current in the blocking state of the device and allows operation at higher junction temperatures. Additionally, the thermal conductivity of SiC is about three times higher than for Si, which means that more heat can be removed from the junction and thus enhancing the thermal capability if the device.

The breakdown strength (critical electric field) of SiC is also about ten times higher than that of Si. Thus, theoretically, a SiC device with the same thickness as a Si device, will be able to block a voltage ten times as high as the Si device. This means that the SiC device also can be made ten times thinner to obtain the same blocking capability a corresponding Si device, which also means lower on-state resistance. The reduced thickness yields lower junction capacitance, which allows for higher operating frequencies.

Higher saturation velocity means that electrons can move faster in SiC devices than in Si devices, making is possible to have a higher switching frequency as well. However, the lower electron mobility of SiC will cause higher on-state resistance of the drift region [4].

All these properties allow creating more compact power converters, as the higher operating frequency will reduce the size of passive components such as transformers. Lower losses also means that the size of the device heatsink can be reduced, while still maintaining the same operating temperature.

2.2 State-of-the-art SiC devices

This section will describe and analyze the operation of the SiC MOSFET and SBDs, which are currently the most used SiC devices in power electronics.

2.2.1 SiC MOSFET

The SiC MOSFET is a majority carrier device and has no minority carrier injection during operation, as opposed to IGBTs and BJTs. This is advantageous, as there is no minority charge that have to be removed from the junction during turn-off, which means that there is no tail current and power loss due to minority carrier extraction. Even though the MOSFET has this advantage, the IGBT has dominated the market for power semiconductor devices, as the Si MOSFET is not suitable for voltages higher than 900 V due to high on-state losses [5]. However, the SiC MOSFET, which has established itself quite well in the power semiconductor market in the last decade, is able sustain higher blocking voltages with lower on-state resistance, as explained in Section 2.1. For instance Cree is currently manufacturing SiC MOSFETs with voltage ratings up to 1700 V and current rating up to 72 A at that voltage. Additionally, with increasing junction temperature, the on-state resistance for SiC MOSFETs increase at a much slower rate than for Si MOSFETs, providing lower on-state resistance at higher temperatures [5].

2.2.1.1 The structure of the MOSFET

The structure of a MOSFET is shown in Figure 2.1. It has three external terminals: drain, source and gate, and the alternating doping levels ensure that the current flowing from drain to source is controlled by the applied voltage between gate and source.

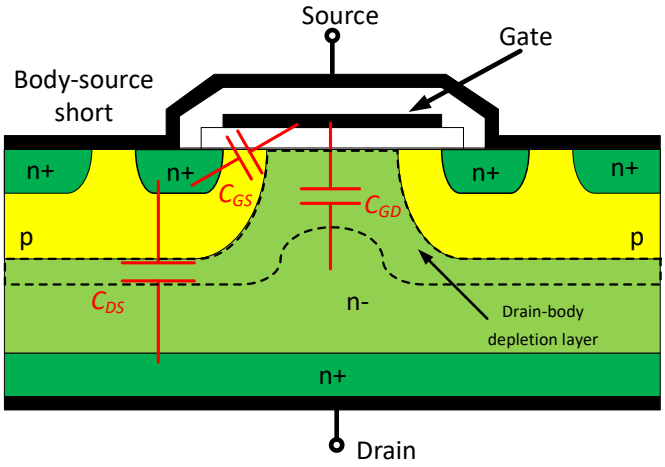


Figure 2.1: Structure of a n-channel MOSFET [6].

By applying a positive voltage to the gate, negative charge will start to accumulate on the surface of the pn+ junction, creating a depletion layer. This process is illustrated in Figure 2.2. As the gate-source voltage rise from $V_{GS,1}$ to $V_{GS,2}$, more and more holes are repelled from the area beneath the gate electrode, effectively thickening the depletion layer.

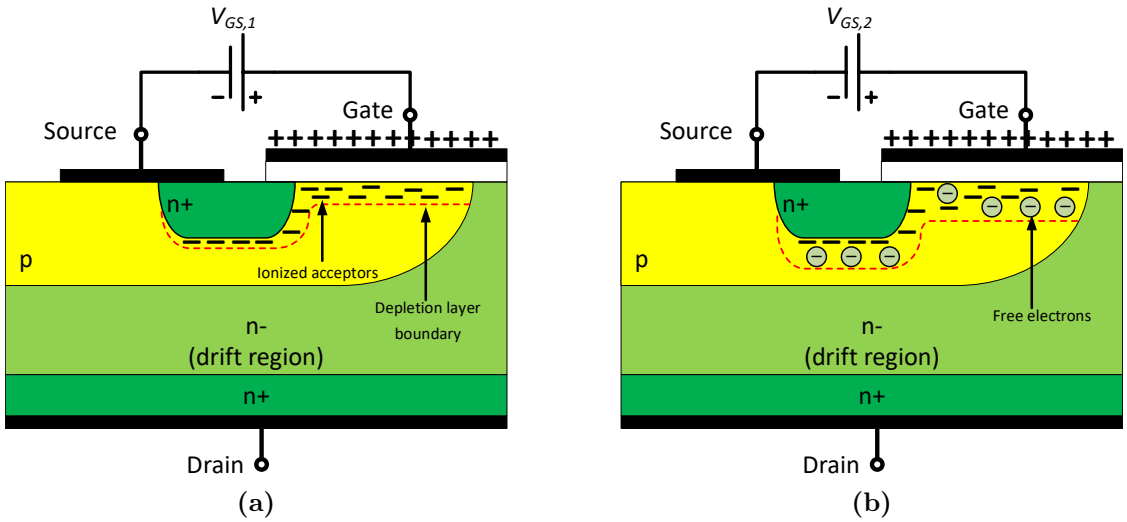


Figure 2.2: (a) Depletion starts forming when a voltage $V_{GS,1}$ is applied between gate and source, (b) and by increasing the voltage to $V_{GS,2}$ the depletion layer becomes thicker [6].

As this process continues, the negative charge density eventually becomes larger than the density of positive holes in the p-layer. This creates an inversion layer, as the p-doped semiconductor layer is effectively inverted to a n-layer. This is shown in Figure 2.3. The voltage at this point, $V_{GS,3}$, is the threshold voltage of the MOSFET. This inversion layer contains a high density of free electrons, which effectively shorts the drain and source terminals and makes it possible for a current to flow between drain and source. The gate-source voltage in increased further, so that the inversion layer becomes larger, allowing higher currents to pass through and the on-state resistance of the MOSFET is decreased.

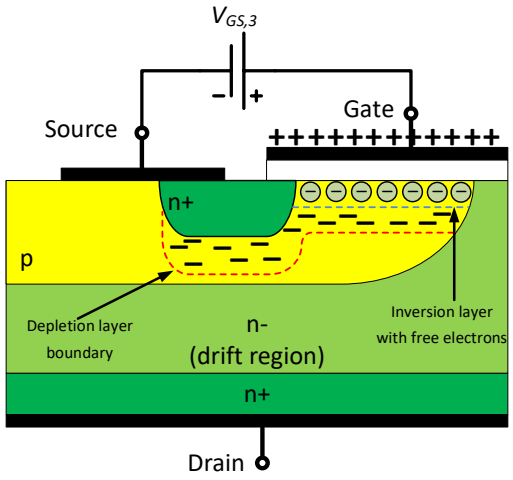


Figure 2.3: Creation of the inversion layer [6].

2.2.1.2 Intristic capacitance in the MOSFET structure

The capacitances shown in Figure 2.1 illustrate the parasitic capacitances of the MOSFET structure and can be used to create a capacitor model of the MOSFET, as shown in Figure 2.4.

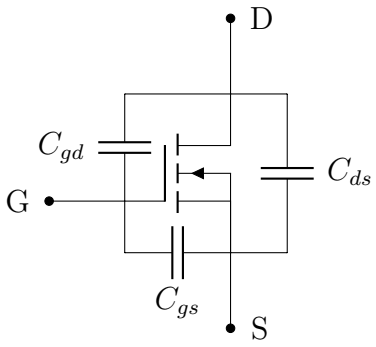


Figure 2.4: Capacitor model of MOSFET.

The value of these capacitances are dependent on several factors. The drain-source capacitance C_{ds} depends on the size of the drift region, whereas the gate-source C_{gs} and gate-drain C_{gd} capacitances are dependent on the gate-oxide layer and depletion layer, which means that they vary with applied voltage. The manufacturer usually presents the values of the capacitances in form of a graph, as shown in Figure 2.5, where:

$$\begin{aligned} C_{iss} &= C_{gs} + C_{gd} \\ C_{oss} &= C_{ds} + C_{gd} \\ C_{rss} &= C_{gd} \end{aligned} \tag{2.2.1}$$

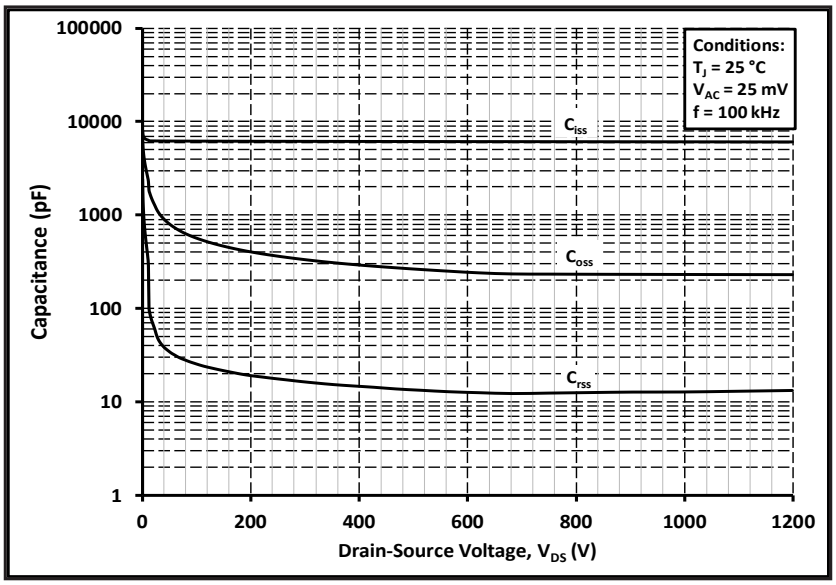


Figure 2.5: MOSFET capacitances as a function of drain-source voltage [7].

The input capacitance C_{iss} is the capacitance that has to be charged at turn-on and discharged at turn-off, which means that it affects the switching performance directly. The output capacitance C_{oss} is useful to know as the it can resonate with the stray inductance of the circuit, forming a LC circuit, which can be problematic. The reverse transfer capacitance C_{rss} often just referred to as the Miller capacitance, and has a direct effect on the rise and fall times of the voltage during the turn-off and turn-on transients.

2.2.1.3 I-V characteristics of the MOSFET

The I-V characteristics of a MOSFET are illustrated in Figure 2.6. The MOSFET will traverse these I-V characteristics from cutoff through the active region to the ohmic region as the device turns on and reversely when it turns off. When the gate-source voltage is below the threshold voltage, the MOSFET is in cutoff and there is no current flowing through it. In the active region, the drain current is dependent on the gate-source voltage, and can be increased by increasing the gate-source voltage. This is basically the transition from on to off-state and reversely, and a lot of power is consumed in this stage since there is an overlap in current and voltage across the device. The goal is to reach the ohmic region, which is eventually reached when the gate-source voltage is increased to a large value. In the ohmic region, the power dissipation is determined by the on-state resistance and drain current, and this region becomes wider with higher gate-source voltage.

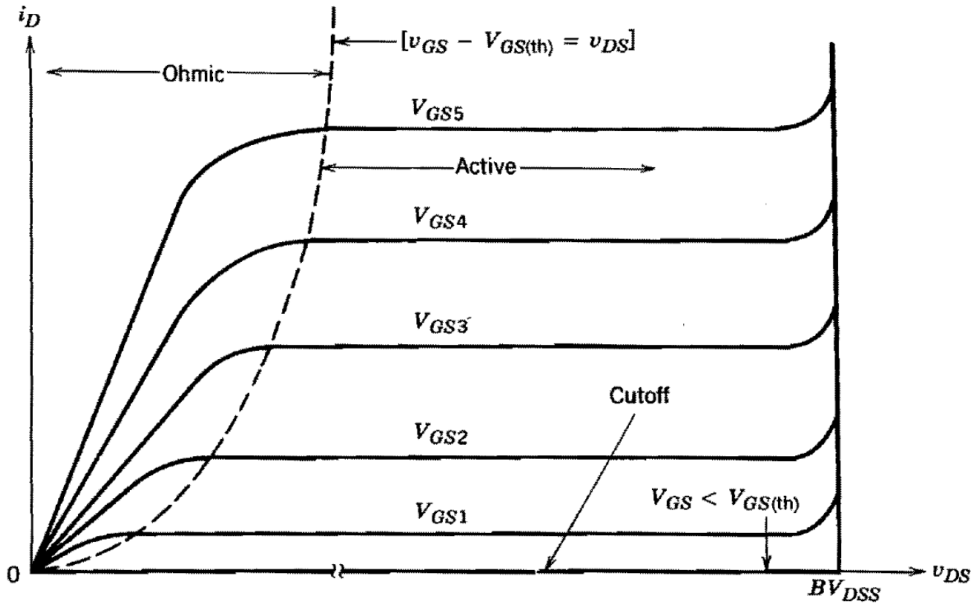


Figure 2.6: I-V characteristics of a MOSFET, where $V_{GS5} > V_{GS4}$ etc. [1].

2.2.1.4 MOSFET switching characteristics

In order to turn on a MOSFET, the gate capacitors have to be charged by applying a positive gate voltage. The turn-on waveforms of the gate-source and drain-source voltages and drain current are shown in Figure 2.7a.

At t_0 the gate voltage is stepped from zero to V_{gg}. Consequently, the gate-source voltage starts increasing to $V_{gs(th)}$ at t_1 and the MOSFET is in cutoff. t_1 is defined as the turn-on delay time $t_{d(on)}$ and at that time the drain current starts flowing as the inversion layer is formed. Between t_1 and t_2 the drain current will continue to rise until it reaches the load current I_0 and the MOSFET is in the active region. When I_0 is reached, the gate-source voltage cannot increase more until the voltage across the MOSFET has decreased significantly. Hence, between t_2 and t_3, the drain-source voltage is falling to the on-state voltage. This time interval is also referred to as the Miller plateau, due to the "plateau" appearing in the V_{gs} waveform. This is due to the gate current mostly charging C_{gd} and keeping the gate-source voltage constant. During this time C_{gd} will increase in value and reduce the rate at which the gate-drain capacitance in charged. Once this interval has ended, the MOSFET has moved along the constant gate-source voltage lines of Figure 2.6 into the ohmic region. During the last stage of the turn-on transient, from t_3 to t_4, the gate-source voltage increases until it has reached the applied reference, V_{GG}, from the drive circuit. During this interval, the on-state resistance of the MOSFET is is reduced even further.

Figure 2.7b illustrates the turn-off transient for the MOSFET. This switching event is alike the turn-on event, but in reverse order and instead of charging the input capacitance of the MOSFET, it is discharged. At t_5 the applied gate voltage is stepped down to zero or a negative value, leading to a current flowing from the gate capacitors through the gate resistor back to the drive and the MOSFET moves through the ohmic and active region, until it finally reaches the cutoff region and is completely turned off.

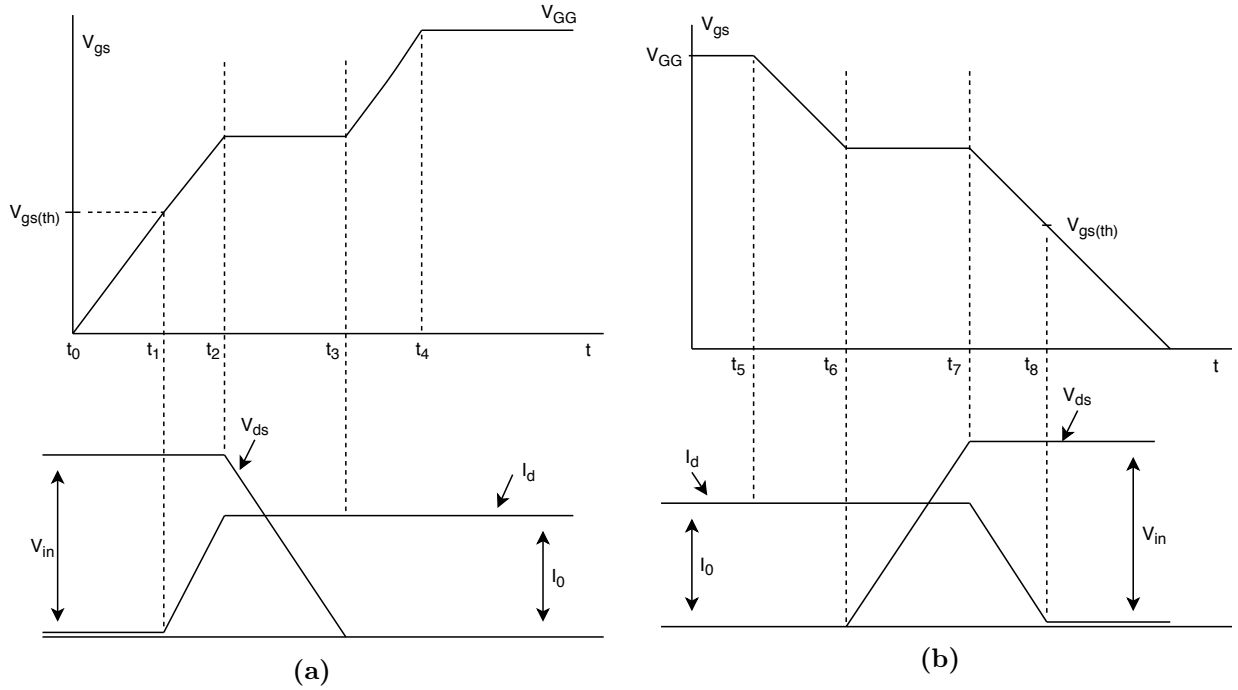


Figure 2.7: (a) Turn-on and (b) turn-off switching transients.

2.2.2 SiC Schottky barrier diodes

Compared to regular Si FRDs, the SBD is a faster diode with lower on-state voltage. Figure 2.8 illustrates the cross section of a SBD. SBDs can be either made out of Si or SiC.

In a SBD, the electrodes are covered by a thin metal film, which directly is in contact with the semiconductor material. This creates the main basis for the principle of operation in a SBD, as this junction created by the metal and semiconductor consists two materials with different electron potential energy. The result is that the electrons will diffuse from the area with high potential energy (semiconductor) to the area with lower potential energy (metal). Thus, the metal will become negatively charged and the semiconductor will form a depletion layer with positive charge. This will eventually form a large enough potential barrier to stop current from flowing through the device. However, when a positive voltage is applied between the anode and cathode terminals, the depletion layer will be reduced, leading to a lower barrier potential and current starts flowing.

Figure 2.9 shows the I-V characteristic of a SBD, which is similar to the I-V characteristics of a regular Si diode. R_{on} is the on-state resistance of the SBD and BV_{BD} is the reverse breakdown voltage. The threshold voltage is usually around 1 V, but will vary from device to device and is dependent on temperature [5].

Since electrons are the only carriers taking part in the operation, the SBD is a majority carrier device. Hence, the device can switch faster compared to regular Si FRD, as there is no minority carrier storage in the junction. However, there is still a reverse recovery current which discharges the junction capacitance, but the switching loss of due to this current is much lower than for Si FRDs and is almost independent of the forward current and temperature, leading to fast recovery across the whole operation range [5].

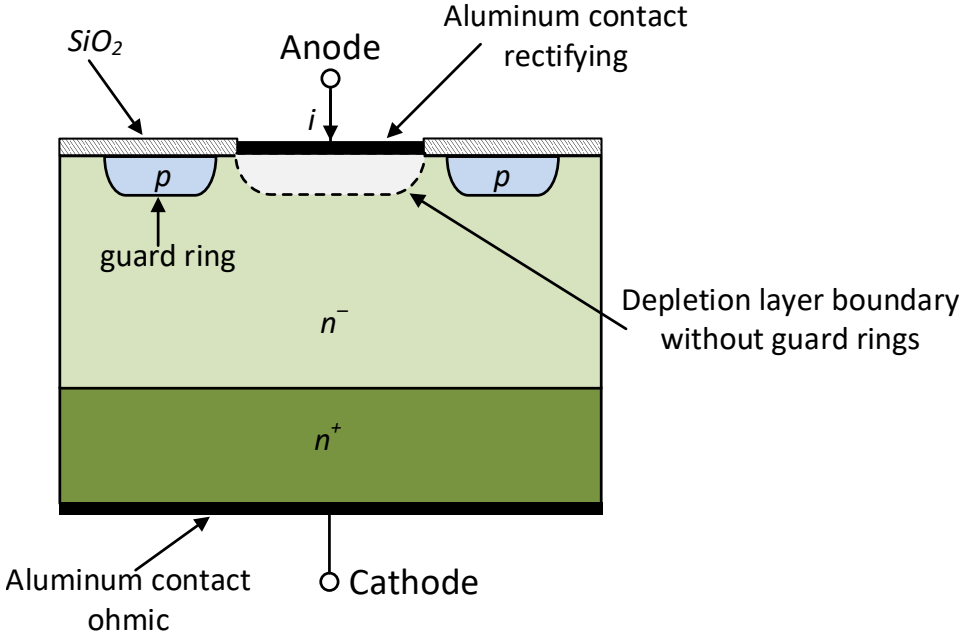


Figure 2.8: Structure of a SBD [6].

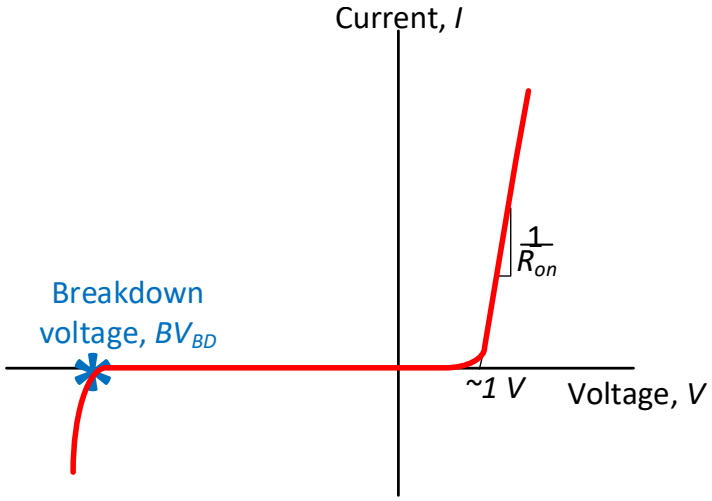


Figure 2.9: I-V characteristics of a SBD [6].

Si SBDs are restricted to breakdown voltages of 200 V, due to the limiting properties of Si, but the emergence of SiC as a power semiconductor material changed this. Currently, SiC SBD with voltage ratings up to 1700 V are on the market. Additionally, SiC SBD have much better thermal performance than Si SBDs and FRDs, with lower losses, leading to more compact and efficient power devices.

2.3 Impact of stray inductance on the switching performance of SiC MOSFETs

The switching performance of SiC MOSFETs is heavily influenced by the presence of stray inductance in the circuit layout. This will lead to voltage overshoots and current sharing imbalances during operation of the device, which in turn may cause some of the devices to fail prematurely due to excessive or non-uniform heating and electrical stress. This can be prevented by de-rating the device, but the semiconductors will not be fully utilized.

The presence of parasitics is more problematic for SiC devices than it is for the well-matured Si devices, and the main reason for this is that the SiC devices are capable of much higher switching frequencies and much faster transients with very high derivatives, and are thus more susceptible for voltage overshoots [8].

Figure 2.10 shows the main parasitics that are involved in the switching; the parasitic capacitances of the MOSFETs and the lumped parasitic inductances present in the circuit. The stray inductances can be classified into three different values: power loop inductance L_p, gate loop inductance L_{gs} and common source inductance L_{cm}.

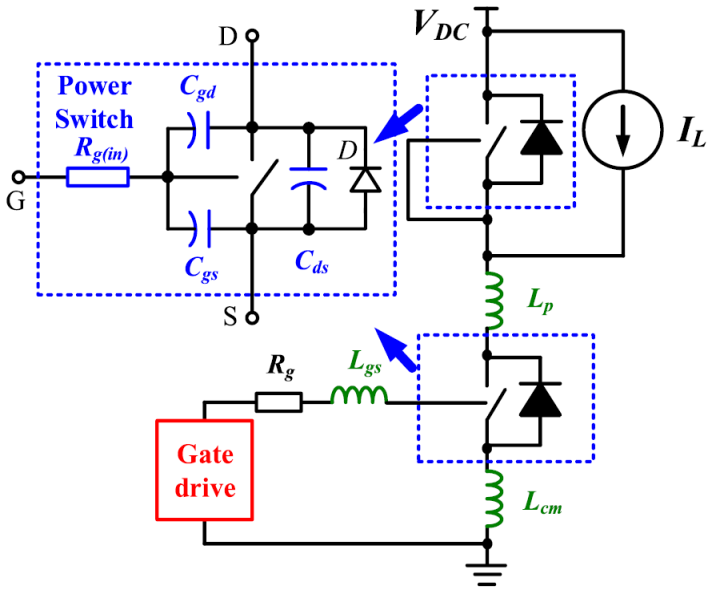


Figure 2.10: Parasitics involved in the switching of semiconductors [8].

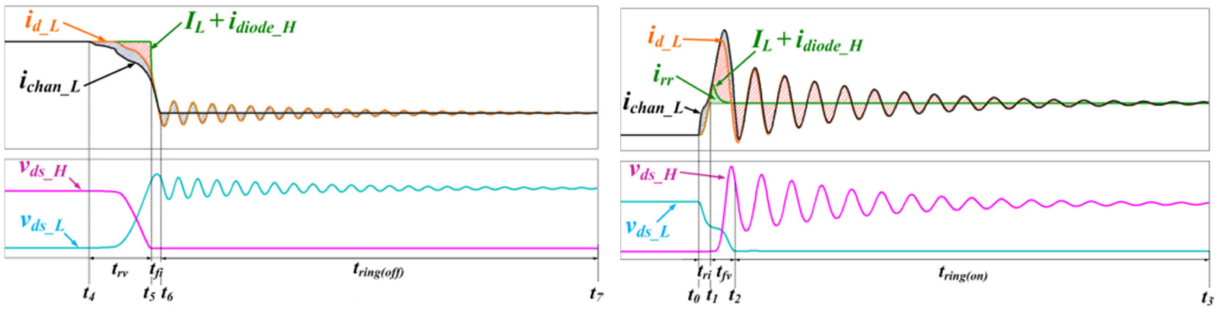
The power loop inductance, also called the commutation inductance is made out of the power current path, that is the bondwires, DBC and terminals. It has generally the most significant effect on the switching transition by causing overvoltages at turn-off and high-frequency underdamped ringing as it resonates with the output capacitance of the MOSFET and diode capacitance. This ringing will affect the performance of the device, and might offset the benefits faster switching speed provides.

The common source inductance is the inductance shared by both the gate and power loop, and will appear if the source bondwires for the gate loop are not separated from the power loop. This inductance will work as negative feedback from the power loop to the gate loop, leading to slower switching speed and higher losses. However, if a Kelvin connection is employed, L_{cm} will be negligible.

The gate inductance is due to the gate and source bondwires, DBC and terminals. Generally, this inductance can be quite high due to the more slender and compact design of the gate-source circuit. This inductance will slow down the gate drive current, as well as it might oscillate with the input capacitance of the MOSFET and trigger parasitic turn-on. This is risk is often negated by adding extra damping in the gate loop in form of resistors, but at the cost of increased time for the switching transition to complete as the gate current will be limited.

The typical switching transient waveforms of SiC devices in a phase leg configuration are shown in Figure 2.11. It shows significant overshoot in the voltage waveforms at turn-off and long lasting ringing, due to the fast switching transients. The energy stored in the capacitances of the devices and the stray inductance will continue to alternate between these parasitics and show itself as underdamped oscillations. The overshoots and ringing will become more severe with higher derivatives during the transients and larger inductance in the switching loop. Thus, new designs should strive towards low-inductive power module designs, so that the switching speed SiC devices are capable of can be taken advantage of to a greater extent.

At turn-on there is reverse recovery of the diode, which superimpose itself upon the switching current, leading to a larger current overshoot and ringing.



(a) **(b)**

Figure 2.11: Typical switching waveforms of SiC devices in a phase-leg. (a) Turn-off switching transient and (b) turn-on switching transient of lower switch [8].

3 Review of power module packaging for SiC devices

As mentioned, the main benefits of SiC devices lays in the fact that they support much higher temperatures and frequencies than the matured Si devices. They are also able provide higher power density and lower losses. However, the power device packaging technology has not followed the development of the semiconductor devices, and has become a bottleneck in the application of SiC. The packaging technology in the future has to consider the temperature SiC devices can withstand, that is at least 175 °C, and the inductive design of the module has to be properly fit to take full advantage of the excellent characteristics SiC offer as they are more sensitive to stray inductance than Si counterparts. These challenges have triggered an increased amount of research into SiC power module packaging technology and this chapter will investigate the ongoing research for the next generation SiC power module design.

3.1 The traditional power module

The most widely used power module structure is shown in Figure 3.1. It is estimated that this structure is implemented in between 70 and 80 % of all power modules [9]. This structure is the most widely used due to the ease of implementation, maturity with regard to production and quality, and low costs. The bondwires are easily connected to the power dies and copper tracks and provide the flexibility other packaging methods might lack, as they are easily paralleled to increase the current capability.

The assembly usually starts with a baseplate at the bottom which provide mechanical support and usually has a heatsink mounted to it so that the power losses generated in the module may be dissipated. A DBC substrate is soldered onto the baseplate, which is a sandwich-like structure, consisting of a ceramic with copper on both sides. The ceramic acts as an insulator to electrically isolate the top and bottom layers and has also good thermal conductivity so that it can conduct the heat generated in the power devices to the base plate. The top copper layer of the DBC has tracks that create the electrical structure of the power module and the power dies are soldered to this layer. The bottom of the die is usually either

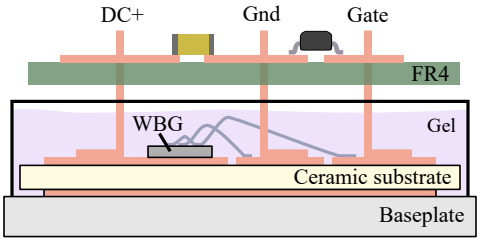


Figure 3.1: Structure of a conventional power module [10].

the drain of the MOSFET or the cathode of the diode and is connected through soldering to the top copper layer of the DBC, while the source and gate and the diodes anode terminal are on the top of the device. The top side of the die is then interconnected to the DBC via bond wires which are usually connected through ultrasonic welding and soldering is not required. The DBC and bond wires are generally immersed in epoxy or silicone gel, to ensure mechanical stability of the bond wires in application where there is typically a lot of vibrations and is also protecting the devices from contaminants and humidity. This gel has also higher dielectric constant than air, allowing a more compact power module and reducing the risk of flashover [11]. This is then encapsulated in a larger plastic case to protect the internal parts from external forces and make it easier to handle the device. Other electrical components are then connected to the power terminals of the module, such as gate drivers and DC-link capacitors.

The internal layout of the DBC in the power module, that is the structure of the copper tracks and the location and amount of bondwires is essential for the performance of the power module. The geometry and current loops will determine the stray inductances that are present in the circuit, which will be both from the copper tracks and the bondwires. Therefore it is important to seek designs minimizing the parasitic inductance without penalizing the other parameters of the module.

The internal layout of a power module, namely the 62 mm CAS300M12BM2 half-bridge module is illustrated in Figure 3.2. The module consists of four DBC pads and each pad has three paralleled SiC MOSFETS in parallel with three SBDs. Two pads in parallel essentially form the upper and lower switch of the power module. According to the manufacturer, the total stray inductance is 15 nH between terminals 3 and 2 [13]. This is the power loop inductance and is the sum of the stray inductances present in each conduction path of the module. The equivalent circuit of the lower switch is shown in Figure 3.3. It shows the location of each inductance within the power module, but do not show their values, which will vary due to different length of the conduction paths for each device. However, in this module the layout is quite symmetrical and evenly distributed parasitics are expected. There are some small variations, as the dies are placed with slightly different distances from the power terminals and some variation in mutual coupling will be present.

There might be room for improved stray inductance in this module. For instance, the commutation loop may be made smaller if the diodes could be replaced by the internal SiC MOSFET diode and the geometry of the power terminals can be improved. Furthermore, the gate loop consists of very long and thin DBC traces and very high inductance in the gate loop is expected. A limitation of this module will also be the tight placement of the dies, which will lead higher temperatures as there will be more thermal coupling between the dies. Hence, the power module is limited to 150 °C [13]. All this will be investigated in the next chapters.

In Figure 3.4 the internal layout a half-bridge power module manufactured by ROHM is depicted. The total stray inductance of this module is 25 nH [14], which is rather high when comparing with the half-bridge module from Cree. It is noted from the figure that the current paths in the ROHM module are slightly larger and there are fewer bondwires that are paralleled, thus adding more stray inductance. In addition, this layout is not symmetrical, and due to this the inductance each MOSFET sees will be different, and might lead to unbalanced current sharing. However, this might not be a big issue during operation if the

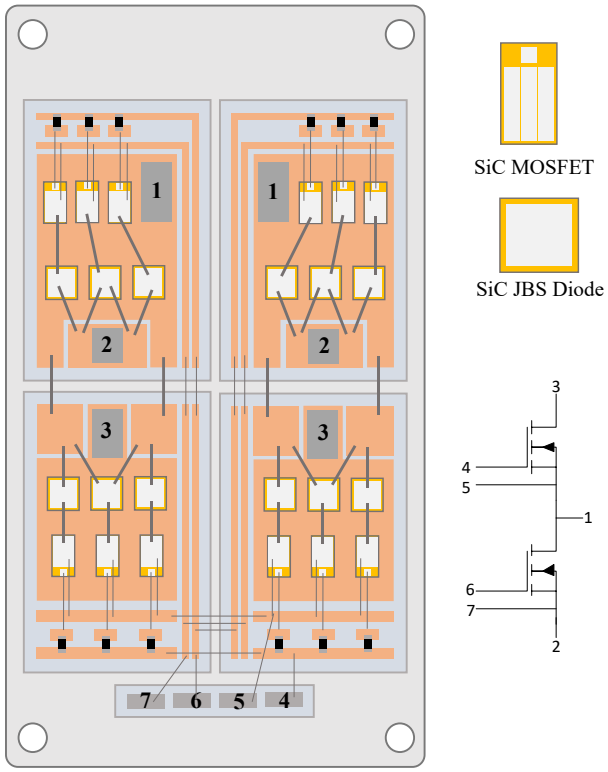


Figure 3.2: The internal layout of a 1.2 kV/300 A Cree CAS300M12BM2 half-bridge power module [12].

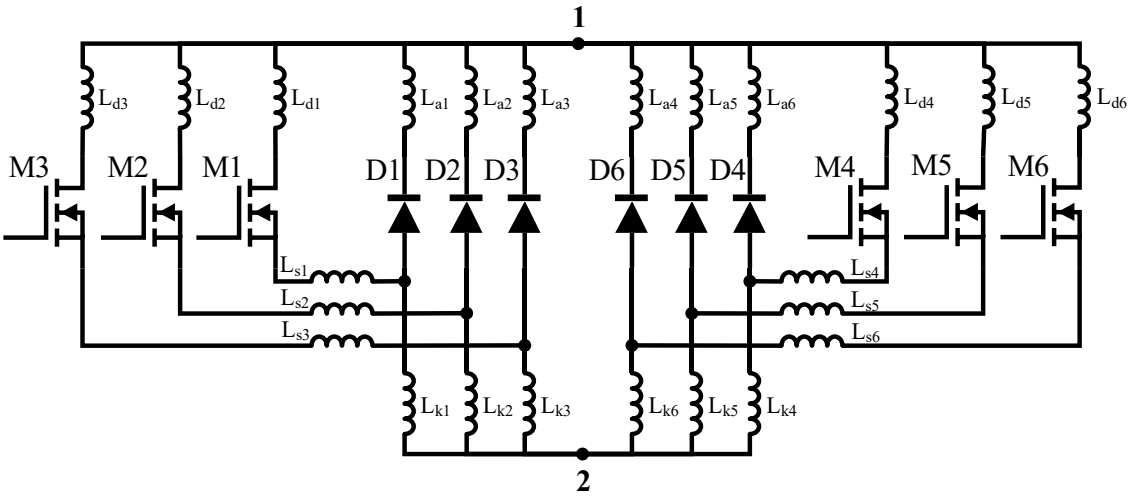


Figure 3.3: The equivalent circuit of the lower side of the half-bridge module from Figure 3.2 [12]

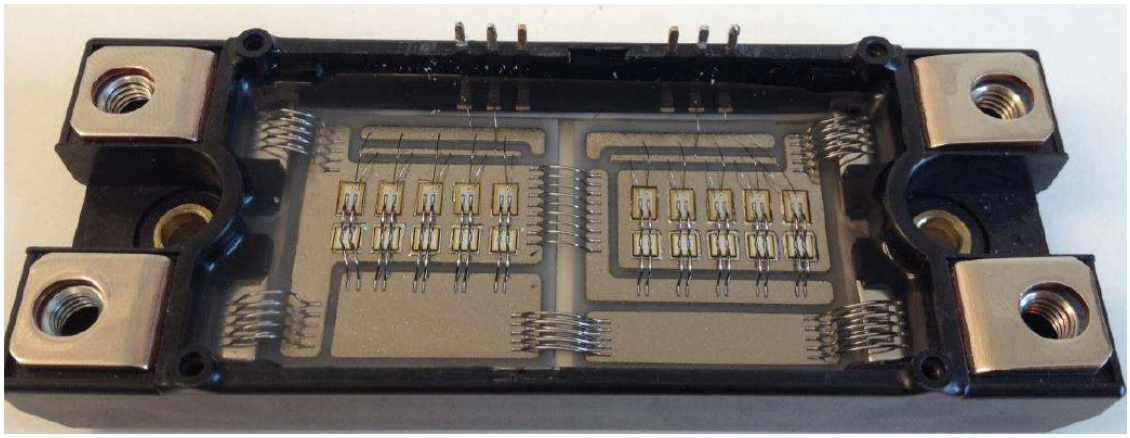


Figure 3.4: The internal layout of an 1.2 kV/134 A ROHM BSM120D12P2C005 half-bridge power module [15].

device is de-rated and the SiC MOSFETs will have a self-balancing effect due to temperature dependent $R_{ds(on)}$.

3.2 New packaging technologies

To fully take advantage of SiC devices new packaging technology is required. The development has been centered around high-temperature operation and reduction of parasitic elements of the power module. Thus, several new methods for interconnections in the power module have been developed, allowing higher temperatures and faster switching operation. New packaging layouts applying three-dimensional placement of dies and interconnections are very promising, as it effectively reduces the loop inductances compared to the conventional 2D-layout of existing DBC technology and makes it possible to implement double sided cooling.

Figure 3.5 shows the SKiN structure developed by SEMIKRON [16]. It uses a two-sided flexible printed circuit board, where the top-side is the logic side for the control signals and the bottom-side is the power side. The flexible PCB has openings, or "vias" to allow the gate signals reach the correct contact and the solders are replaced with sinters (a new die-attachment method). The result is a power module with about 1 nH of stray inductance in the commutation loop. The thick aluminium bondwires in present day power modules add a significant amount of stray inductance, whereas in the SKiN design the bondwires are replaced by wide and flexible copper leads that have a larger cross section and cover a larger area of the top-side of the power semiconductors.

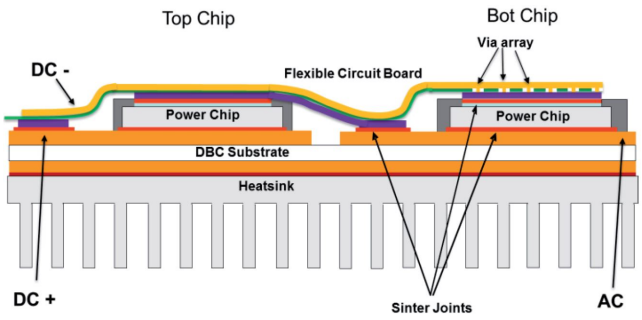


Figure 3.5: SKiN technology used for a SiC power module [16].

Figure 3.6 illustrates a two sided DBC planar bonding structure. It a press-pack like struture, where two SiC MOSFETs are connected in parallel. The upper substrate contains several layers, where the source contacts are connected to the copper top plate and provides separate gate and source terminals for the gate driver. This layout allows the mounting of two heatsinks for better thermal management, but as the heatsinks are directly mounted on the powered copper plate, they have to be properly accounted for, in both the parasitic design and the ability to carry current.

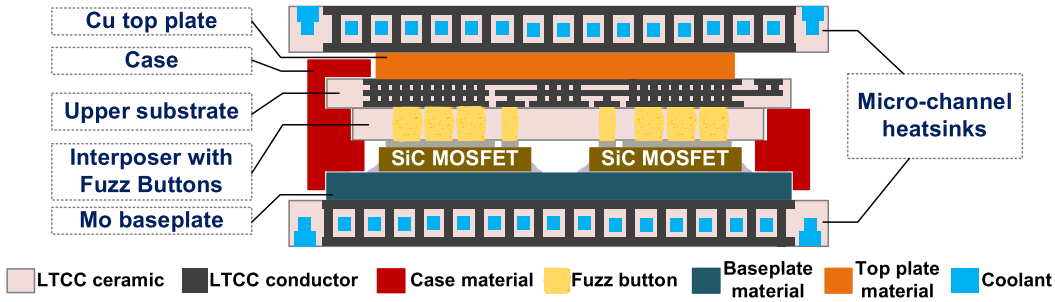


Figure 3.6: Press-pack SiC MOSFET structure [17].

Several other packaging structures have been suggested, such as Siemens Planar Interconnect Echnology (SiPLIT), where relevant areas of the DBC are laminated for insulation and then coated with copper to connect the different parts of the power module together [18]. Chip-on-chip structures are also very promising, such as the one developed in [19]. The power dies are embedded inside a dielectric layer, with direct connection between each others source and drain and separate source and gate connections. This module has extremely low stray inductance, down to 0.25 nH.

By moving from bond wired structures to structures that utilize wider conduction paths and by changing the commutation loop from 2D to 3D, the loop area is reduced and magnetic field-cancelling has a larger effect, cutting down on the stray inductance. This also opens up for double sided cooling and higher power density and current rating. However, manufacturing of such structures is difficult, as the power dies are required to have proper joining capabilities on both sides and the manufacturing process is much more intense compared to the existing bond wired sturctures, which are still more viable today.

4 | Design and simulation of a power module in FEM software

In this chapter the process of creating the power module in ANSYS will be presented and the parasitic components of the module will be extracted through simulations. Furthermore, a thermal analysis of the module will be performed, and the theoretical background for both investigations will be laid out.

4.1 Theory for extraction of parasitics

Parasitic elements in circuits are unavoidable, and all conductors possess inductance and resistance, as well as capacitance. These elements cannot be eliminated, but they can be reduced by streamlining the geometry of the conductors and by knowing how the various parts of the electrical network interact with each other. Determining these values can be difficult, especially for complex geometries such as power modules. Thus, to find these inductances, powerful numerical tools have to be used, such as ANSYS Electronics Suite or COMSOL Multiphysics, as finding these values by hand is difficult, time consuming and much less accurate. Moreover, to validate the simulation results, experimental measurements have to be conducted to determine the accuracy of the simulations.

This section will for the most part cover stray inductance as well as parasitic resistance, and compare the usage of FEM software with theoretical calculations.

4.1.1 Theoretical calculations of stray inductance

There are several formulas for the calculation of stray inductance for different geometries; round or rectangular conductors, with varying degree of accuracy [20]. Similarly, there are formulas for the mutual inductance, which depends on the way the conductors are located with respect to one another. The equation for calculating the partial inductance of a round conductor is given by (4.1.1). l and r_w is the length and radius of the conductor respectively and μ_0 is the magnetic constant. It is assumed that $l \gg r_w$, which often is the case [21].

$$L_p = \frac{\mu_0}{2\pi} \cdot l \left(\ln \frac{2l}{r_w} - 1 \right) \tag{4.1.1}$$

However, this equation only considers the self-inductance created due to the external magnetic fields. It assumes that the frequency is so high that all the current has crowded towards the surface of the wire. In this case the current will flow in an annulus with the thickness defined as the skin depth [1]:

$$\delta = \frac{1}{\sqrt{\pi f \mu_0 \sigma}} \tag{4.1.2}$$

σ is the conductivity of the conductor. This means internal self-inductance of the wire, which is sourced by the magnetic flux internal to the wire will decrease as more current concentrates at the surface of the wire. At very high frequencies when the skin effects becomes dominating, the inductance will only consist of the external inductance, that is self-inductance created due to the external magnetic flux of the wire. The internal inductance of a round wire with an uniformly distributed current can be expressed as [21]:

$$L_{internal} = \frac{\mu_0}{8\pi} \cdot l \tag{4.1.3}$$

Hence, the internal inductance of a wire can be given in per-unit-length as 50 nH/m, which usually is quite small when compared to the external inductance and is quite often neglected. Moreover, the current usually has a frequency above zero, so the internal inductance will generally be smaller.

When it comes to the mutual inductance between two wires, the calculation depends on the position of the wires with respect to one another. The mutual inductance of two wires in parallel is given by [21]:

$$M_p = \frac{\mu_0}{2\pi} \cdot l \left[\sinh^{-1} \frac{l}{d} - \sqrt{1 + \left(\frac{d}{l}\right)^2} + \frac{d}{l} \right] \tag{4.1.4}$$

The distance between the centre of the two wires is defined as the parameter d and it is assumed that $d \gg r_w$. A smaller distance between two conductors leads to more flux linkage, and thus higher inductance. However, this depends on the direction of the currents. If the currents are in the opposite directions of each other, some of the flux will cancel, leading to a reduction of inductance. This is a technique quite often used to reduce the inductance of certain components, such as power modules or capacitor terminals.

4.1.2 FEM simulations for extraction of stray inductance

To compare the theory presented in the section above with simulations performed in FEM software, the round conductor in Figure 4.1 was simulated. The length of the wire is 30 mm and its diameter is 0.2 mm.

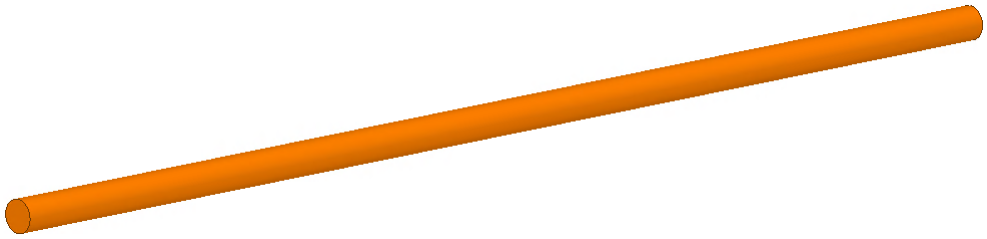


Figure 4.1: Round copper wire in ANSYS Q3D Extractor.

The theoretical calculation and simulation results are presented in Table 4.1. It shows that the simulation values are very close to the theoretical value, and the difference can be almost neglected.

Table 4.1: Simulation and theoretical values for inductance of a 30 mm wire with radius 0.1 mm.

Frequency	Theoretical calculation	Q3D simulation
DC/Low frequency	33.88 nH	33.99 nH
High frequency	32.38 nH	32.46 nH

The reason for the difference in the results might be that the software uses FEM/MoM to calculate the inductance. This means that the wire is divided into several hundred/thousands elements, and Maxwell's equations are solved for each of these elements. This is done until a desired accuracy is achieved. To achieve an exact solution, the number of elements must be increased substantially. Furthermore, the equations presented in the Section 4.1.1 include some simplifications as well.

Similarly, the mutual inductance of between two identical wires of the type shown in Figure 4.1 with distance d equal to 1 mm can be be calculated. Theoretical calculation according to equation (4.1.4) gives an mutual inductance of 18.76 nH, whereas simulation gives 18.77 nH. This shows that there is a significant amount of coupling between the wires, and that simulation provides results that coincide well with theory.

As the geometry of the object becomes more complex, more smaller elements have to be generated to achieve a solution with good accuracy, but this happen at the cost of longer simulation time. However, ANSYS Electronics comes with three environments for electrical analysis: Maxwell, HFSS and Q3D Extractor. Each of these environments are specifically optimized to speed up the the simulations in different areas of power electronics design. ANSYS Maxwell offers very high accuracy up to 10 MHz, but is usually used for low frequency analysis, such as transformers and electrical machines, where precise modelling of the electrical and magnetic fields is required. HFSS is used for very high frequency analysis, that is from 10 MHz to several GHz. The last environment, Q3D Extractor, is specifically optimized with regard to quickly classify the electrical parasitics that are present in interconnects, busbars, PCBs. etc. at frequencies ranging from DC to 1.5 GHz. Compared to Maxwell, the model is easier to set up in Q3D Extractor with faster solving and includes adaptive meshing [10].

Q3D Extractor uses two methods to calculate self and mutual parasitics of a structure: FEM and MoM. Which method to be used is determined by which values that are to be calculated. Q3D has divided these entities into three parts: capacitance and conductance, DC inductance and resistance, and AC inductance and resistance. FEM is only used in the DC analysis, as the current is distributed over a volume, whereas MoM is used in simulations where the surface charge is approximated. This means that at very high frequencies only the surface of a conductor is modelled as that is where the current is concentrated, and MoM is used to solve the electromagnetic equations [22]. Thus, Q3D Extractor solves the DC and high frequency asymptotes of the of model and the behavior in between these regions, called the transition region, is estimated using a blended algorithm. This is illustrated in Figure 4.2. It shows the how the inductance of the wire from Figure 4.1 varies with frequency, and the DC and AC asymptotes which are given in Table 4.1 are shown to illustrate the relation.

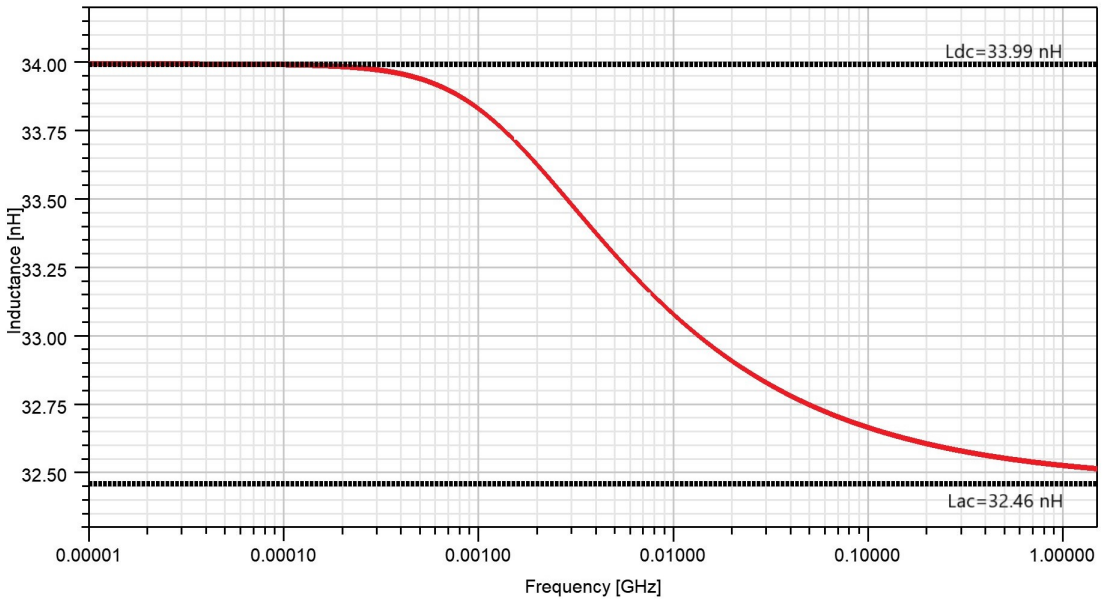


Figure 4.2: Plot of inductance of a round copper wire with length 30 mm and radius 0.1 mm versus frequency.

The graph does not reach the AC asymptote, which might due to the how Q3D calculates the values in the transition region, but it does certainly converge towards it. Furthermore, the values in the transition region are only an estimation, due to the simplified nature of the blended algorithm implemented in Q3D Extractor, so the results will lack accuracy. ANSYS Maxwell can be used to get more accurate results in the transition region, as it is a pure FEM software and can model the skin depth better, but this will increase the simulation time significantly [22]. In addition to all this, Q3D Extractor will also model the mutual coupling between conductors inside the module.

The resistance of the wire will also vary with frequency. In fact, the resistance of the copper wire will increase proportionally with the square root of frequency, as skin depth gets smaller and more current crowds towards the surface of the conductor (eq. (4.1.2)). This is illustrated in Figure 4.3. The resistance at DC and low frequency is constant and as the frequency increases the resistance starts increasing and will continue increase proportionally with $\sqrt{f}$.

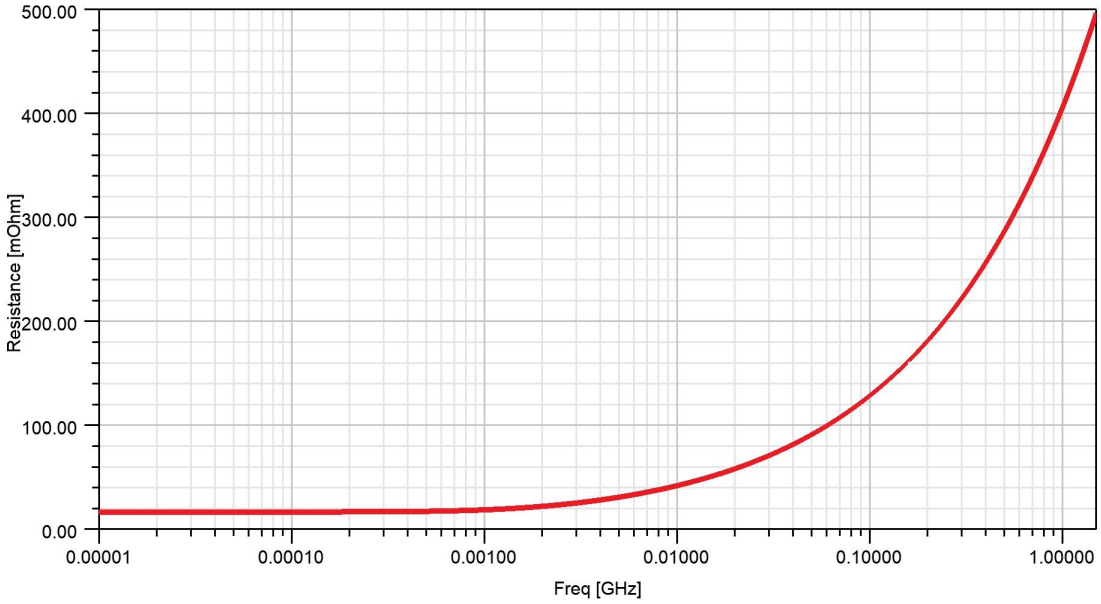


Figure 4.3: Plot of resistance of a round copper wire with length 30 mm and radius 0.1 mm versus frequency.

4.2 Design of the power module in ANSYS

The module selected to be created in the simulation software is the CAS300M12BM2 SiC MOSFET half-bridge module manufactured by Cree. It is based on the standard 62 mm package, which is a standard used by several manufacturers.

To create the module in the software, it is essential to know both the precise inner and outer dimensions and geometries of the module. This is unfortunately not readily available from the manufacturer. However, a picture of the inner layout of the CAS300M12BM2 power module can be found in [15] and is shown in Figure 4.4.

Figure 4.4: Picture of the layout inside a CAS300M12BM2 half-bridge power module [15].

This figure in correlation with Figure 3.2 and the datasheet from the manufacturer [13] is assumed to provide accurate enough readings to recreate the internal geometry of the module in ANSYS, even though there will be some inaccuracies involved. Moreover, the thickness of the different layers and the materials are given in [23].

4.2.1 The geometry of the power module

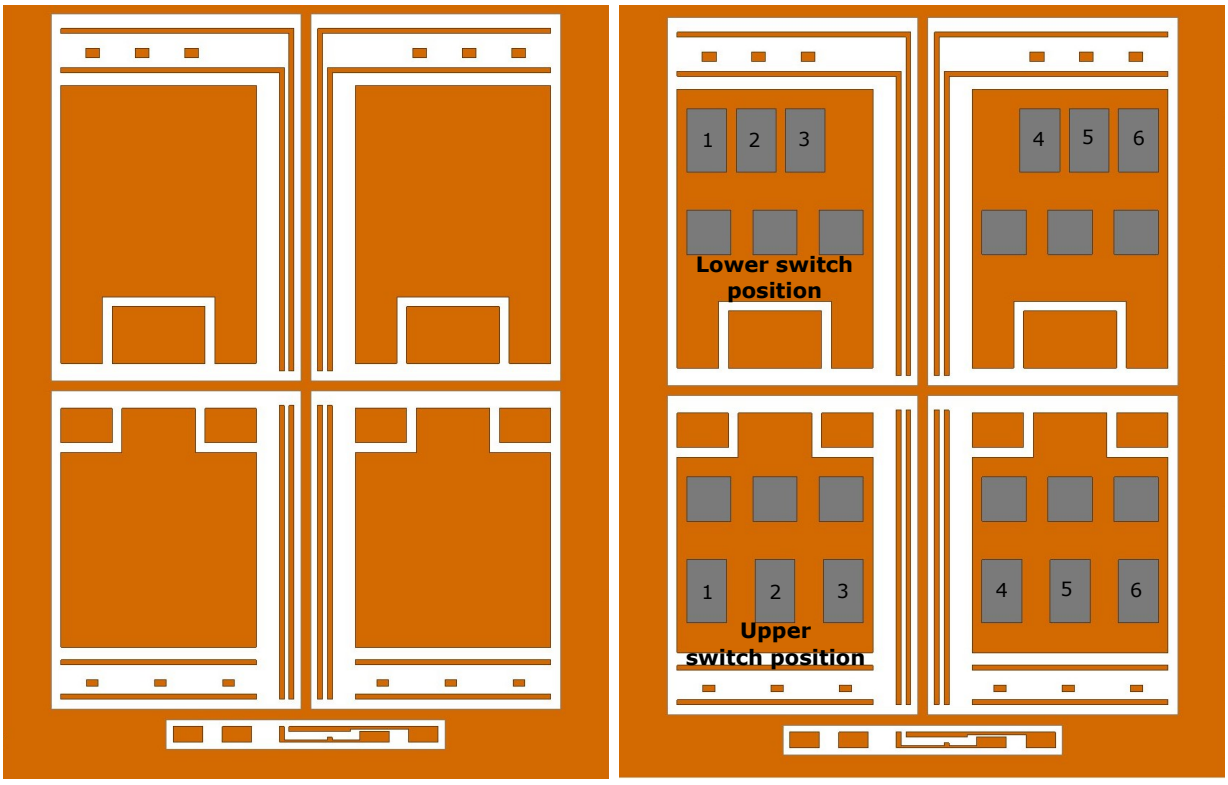
The creation of the module was done sequentially. First off the outer dimensions of the module were extracted from the datasheet. The width and length of the bottom of the module are given as 62 and 106 mm respectively. The height is 30 mm and will be used later. This is used to create the baseplate of the module. The width and length of the layers on top of the baseplate are obtained through careful examination of Figure 3.2 together with the package dimensions given in the datasheet. Even though the drawing in Figure 3.2 probably is not to scale, it does quite accurately shape of the different geometries and how they approximately scale to one another. Thus, together with the other gathered information, it is deemed that the geometry obtained will be quite close to the actual geometry of the physical module. Afterwards, the different layers have to be determined, that is the material and the thicknesses. The thicknesses of the the different layers are given in Table 4.1 and are used for the 3D model in ANSYS.

Table 4.1: The thicknesses of the different layers inside the power module [23].

Layer	Material	Thickness (μm)
SiC MOSFET/SBD	SiC	180/350
Chip solder	Sn_5Pb_{95}	80
Copper layer	Cu	300
DBC ceramic	AlN	355
Copper layer	Cu	280
System solder	Sn_5Pb_{95}	40
Baseplate	Cu	3000

Most of the information in this table seems to be accurate, but the SiC power chips have metallization on both sides (cathode/anode and drain/source) with thickness of a couple μm which has been chosen to be omitted in this model. This is due to the fact that these layers are so thin, so they will not affect the parasitic elements.

The finalized form of the DBC is shown in Figure 4.5a. The topside of the DBC yields the paths for conduction and placement of chips, terminals and bondwires. The lower pads are slightly smaller than the upper pads, so that the gate and source circuits could fit on the limited space, as there has to be space for the casing and mounting points on the 62 mm baseplate. Furthermore, the pads symmetrical from left to right, and at least 0.5 mm of width is kept between distinct copper tracks.



(a) **(b)**

Figure 4.5: CAS300M12BM2 half-bridge power module with (a) only substrate pattern and (b) with placed and numbered SiC MOSFETs and SBDs.

The next step is to place the SiC MOSFETs and SBDs together with their solder on the copper pads of the DBC. To do this, the size of the SiC chips has to be known and this information is not provided. The power rating of the module is 1200 V/ 300 A, and by browsing the bare power dies in the Cree catalogue and matching the power ratings, the proper bare power dies are found. There are 6 SiC MOSFETs and 6 SiC SBDs in each switch position, which means that each die should be rated for at least 50 A. The SiC MOSFET die that fits the requirements is CPM2-1200-0025B, which is rated for 98 A and its dimensions also fits with the size given in [24] where the same module was investigated. The model of SiC SBD is CPW5-1200-Z050B and is rated for 50 A. This is summed up in Table 4.2.

The placement of the bare dies is done in accordance with Figure 4.4. Each switch position consists of two DBC substrates or pads and each pad has three MOSFETs and three SBDs. The bare MOSFET dies are placed tightly on the upper pad to accommodate space for the output terminal, whereas the lower pads have no such restriction. Additionally, symmetry is kept when placing the chips, so that the parasitics for each conduction path are as equal to one another as possible. The final layout of the chips is shown in Figure 4.5b.

Table 4.2: Data for the bare SiC MOSFET and SBD dies [25], [26].

Part	Rating	Die size (mm x mm)	No. of dies in switch
CPM2-1200-0025B MOSFET	1200 V/ 98 A	4.04x6.44	6
CPW5-1200-Z050B SBD	1200 V/ 50 A	4.9x4.9	6

Placing the bond wires that interconnect the different conduction paths inside the module is the next step in designing the module in the software. Unfortunately, there is little information to be found about the bondwires inside the CAS300M12BM2 module. However, it can be assumed that the bondwires are made out of heavy aluminium, as aluminium is usually what is used for high power modules [11]. Next, the diameter of the bondwires has to be selected, and there are two types of bondwires used in this module: gate/source wires and power wires. The bondwires on the power side are thick, as they carry the load current, whereas the gate/source bonds can be thinner since they only convey the low power signal to the gate of the switch.

The power side bondwires are usually made out of heavy aluminium wires, with diameters from 0.2 mm to 0.5 mm, whereas the gate interconnections are made out of thinner aluminium wires, for instance wires with diameter of 0.05 mm as they do not experience a lot of current going through them. A 0.2 mm heavy aluminium wirebond can carry 15 A [11], and each MOSFET die will carry a maximum continuous drain current of 50 A. This means that at least four 0.2 mm bondwires must be paralleled, but instead five 0.2 mm bondwires are used for each interconnection to keep a safer margin. This can also be seen from Figure 4.4, which shows that interconnections in the real module are made out of five bondwires as well. Moreover, by increasing the amount of bondwires, the stray inductance of the layout is decreased. The bondwires for the gate-source circuit are selected as fine 0.05 mm aluminium wires.

The terminals are also modelled, but there is less information to go on here, especially for the gate and source terminals. The positive, negative and output terminals are carefully created by studying Figure 4.4 and by using the technical drawing the the datasheet. Same goes for the gate and source terminals. The thickness of the power terminals is set to 1 mm as that is assumed to be a reasonable value, while the cross section of the control terminals is given in the datasheet to be 2.8x0.5 mm. Furthermore, it is assumed that the control and power terminals are created from copper alloy. The final module is shown from the side in Figure 4.6.

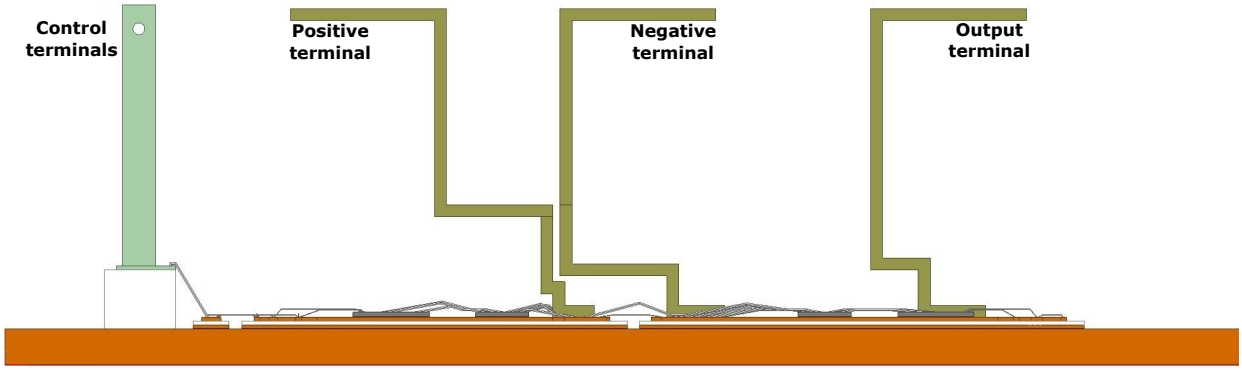


Figure 4.6: 3D model of the module shown from the side.

The 3D model of the entire module is shown in Figure 4.7. One thing to note is that there are internal resistors in the gate path of each SiC MOSFET inside the power module, which can be seen in Figure 3.2 and Figure 4.4. These have been omitted in the ANSYS model, and are simply shorted. The semiconductors and bondwires are also usually immersed in a silicone encapsulant so that the power chips and interconnections are protected from the outside environment. The silicone gel has not been included in this model, as it will not affect the distribution of the parasitics in the module. However, the encapsulant can work as a heat-spreading medium, which might affect the thermal performance of the module, leading to different junction temperatures, but this is not in the scope of this thesis.

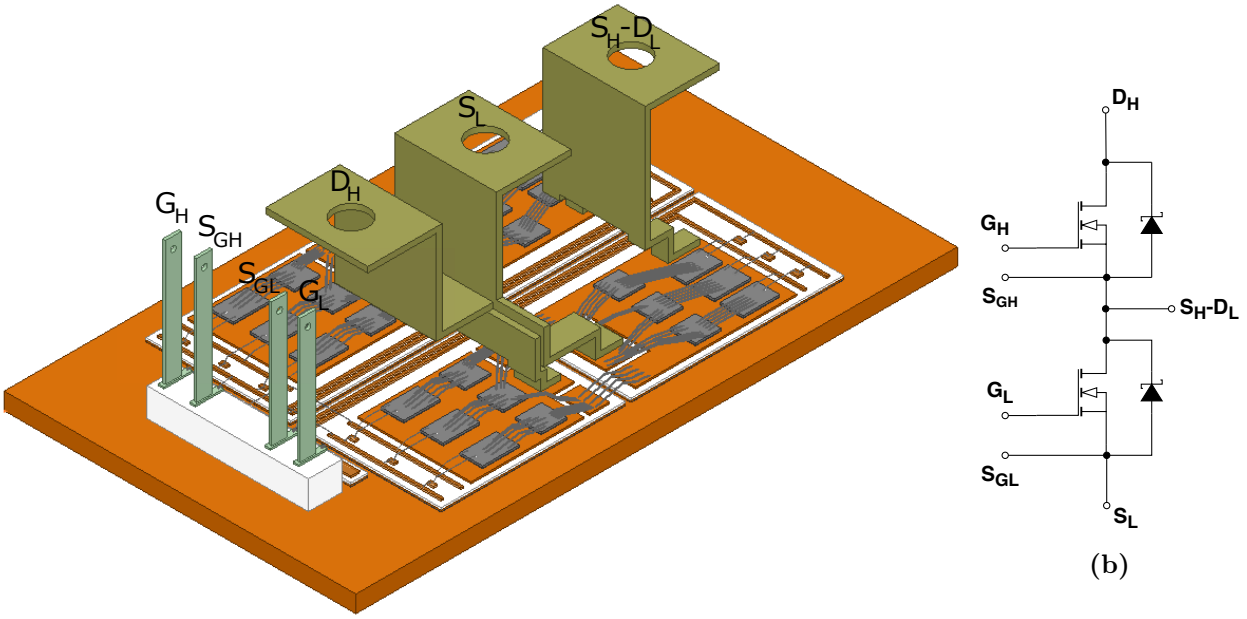


Figure 4.7: (a) Full view of the 3D module and (b) explanation of the terminals.

By studying the figures in this section, one can see that the module is very symmetrical. This is of course done on purpose, as by carefully placing the semiconductors in such a way

makes the parasitic components each chip sees approximately equal between all the chips in one switch. This ensures that the current among the paralleled MOSFETs and SBDs is close to evenly distributed.

4.3 Parasitic extraction

The extraction of the power module RLC parasitics will be done by using ANSYS Q3D Extractor. The solver calculates the electromagnetic field equations and will extract the parasitic components through pre-defined current paths and are identified by using nets. A net is defined as a collection of touching conductor objects separated by non-conducting materials. The nets are created and modified by assigning conducting material to elements which are supposed to be conducting (i.e. copper) or insulating material if the element is not supposed to conduct (i.e. SiC). For instance, if a SiC MOSFET is in its on-state, it is attributed copper material, but when it is in its off-state it is assigned SiC material. Thus, several simulations have to be performed to get a complete overview of the parasitics inside the power module.

When the nets are identified by the software, the sources and sinks can be assigned, which will determine for what parts of the module the software will extract the parasitic components as well as whether the inductive coupling terms inside the module are positive or negative. When this is taken care of, the simulation can be started.

4.3.1 Extraction of total commutation inductance

The total stray inductance is given in the data sheet of the CAS300M12BM2 module to be 15 nH and is measured between the positive and negative terminals of the module [13]. It is not given for what frequency this value is for.

Simulations were performed to extract the corresponding value from the 3D model of the module. Both upper and lower MOSFETs are then in on-state, so they are modelled as copper, whereas the SBDs are blocking and are therefore modeled as SiC. This creates a single net, and the positive terminal is assigned source and the negative terminal is sink. The results are given in Table 4.1. These values are the asymptotes of the frequency dependent inductance, as explained in Section 4.1.2, and assume either pure DC operation or infinitely high frequency. The inductance during real operation will be somewhere in between these values, probably closer to the AC value depending on the rise and fall times during switching transients, as during those periods the module will experience higher derivatives and the current will concentrate more towards the surface of the conducting parts of the module. These values include do also include the magnetic coupling between the different conducting elements of the module.

Table 4.1: Values of power loop inductance at DC and AC.

	DC [nH]	AC [nH]
L_{loop}	13.65	9.83

Furthermore, the total simulated value does differ a bit from the datasheet value of 15 nH. This might be due to disparities between the 3D model and the physical module, as they are not identical. The simulation might also not be able to model very accurately all the electromagnetic interactions and the manufacturer may also include some margin of safety in the given datasheet value. However, it might be sensible to believe that the inductance given by the manufacturer is the worst case inductance, that is at DC, since that is when the inductance is at its largest value. Thus, the simulated value of 13.65 nH at DC is not that far off. Anyhow, real measurements on the power module have to be performed to get a better overview.

4.3.2 Extraction of partial inductances in the power loop

In this section the different conducting paths in the module will be analyzed and their RL-parasitics extracted. This is to prepare a comprehensive model for further analysis in LTSpice and see how much the different parts contribute to the total inductance, that is the terminals, DBC and bondwires.

First off, the partial inductances of the power circuit are found. The partial inductances that are to be extracted are shown by the markers in Figure 4.8.

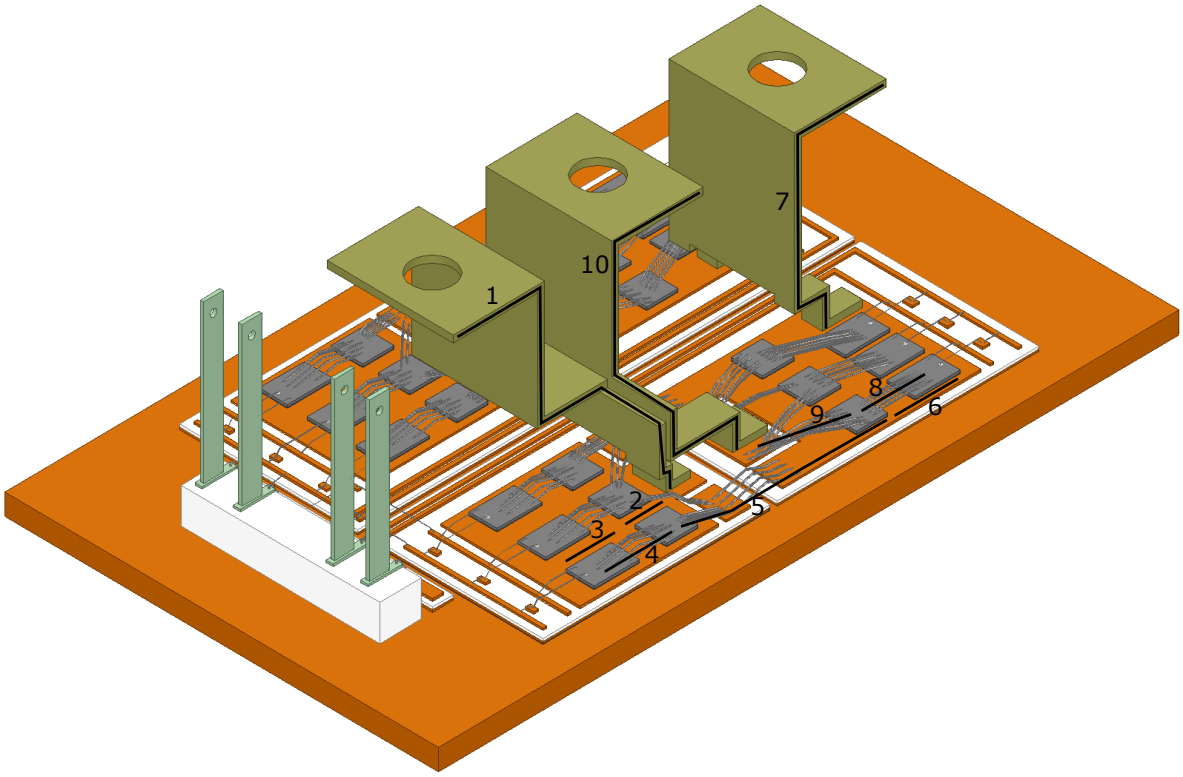


Figure 4.8: The power module with markers that indicate the paths to be analyzed.

Table 4.2 explains the different conduction paths marked in the figure. However, the paths are a bit different for each device, due to them being placed in different locations on the pads which will lead to differences in the extracted self-inductances. This has been

accounted for in the simulations and only one side of the module has been simulated, except for the terminals, as the pads are symmetrical from left to right.

Table 4.2: Explanation of the different conduction paths shown in Figure 4.8.

Marker no.	Explanation
1	Positive terminal
2	Between foot of positive terminal and upper diode cathode.
3	Between upper diode cathode and upper MOSFET drain.
4	Between upper MOSFET source and upper diode anode.
5	Between upper diode anode and lower diode cathode.
6	Between lower diode cathode and lower MOSFET drain.
7	Output terminal.
8	Between lower MOSFET drain and lower diode anode.
9	Between lower diode anode and foot of negative terminal.
10	Negative terminal.

This analysis only considers the partial self inductances, which means that coupling effects due to current flow in parallel are not modelled. Q3D Extractor has a function that allows creating lumped SPICE models that can easily be exported to a circuit simulator such as LTSpice. This function is very handy when there is a case with several nets, such as here, as the coupling between the nets is significant, but difficult to keep a good overview of. For instance, having a model with ten nets would create a 10x10 SPICE matrix with self-inductances along the diagonal, while the off-diagonal elements would be the coupling between the nets. In this thesis, it was attempted to create such a SPICE model, but it proved to be difficult to get it to work. However, the most significant coupling inside the module is included for the LTSpice model, that is the coupling between the main power terminals.

The partial inductance terms are calculated for a frequency of 3 MHz, and the same goes for the parasitic resistance inside the module. The parasitic model of the module is illustrated in Figure 4.9, together with the values of the stray inductances.

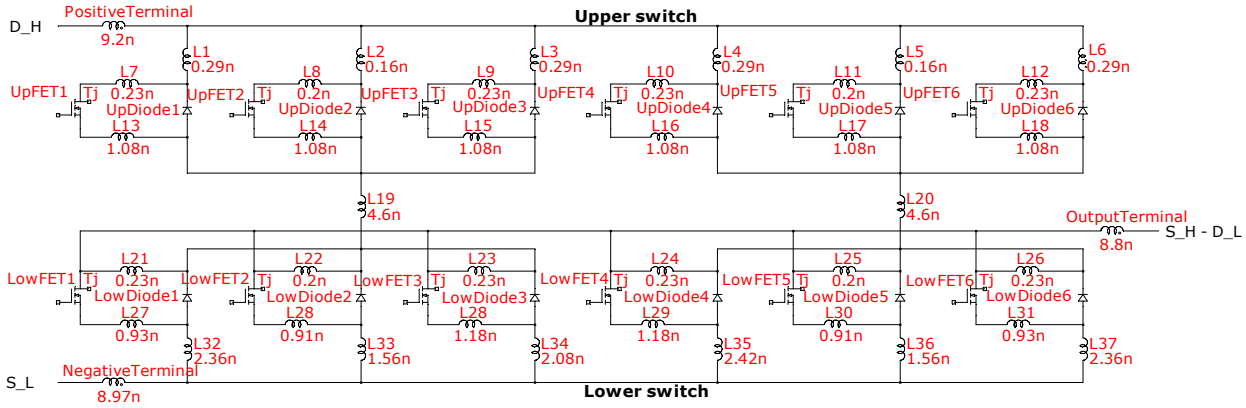


Figure 4.9: Parasitic model of the power module.

In this figure, the inductances are given in nH and the parasitic resistances are included in the stray inductance components. The stray resistances are for the most part no higher than 2 mΩ. From the figure, inductances L1 to L6 represent marker 2 in Figure 4.8 for each of the six MOSFETs. L7 to L12 represent marker 3 and so on. As can be seen from the figure, the power terminals bring in a lot of stray inductance. More than fifty percent of the inductance is due to the power terminals, and the rest is distributed between the bondwires and DBC. The high value of the terminals is due their thickness and tall structure, whereas the bondwires are paralleled, leading to a lower share in the total inductance. The DBC has a low share as well, due to its width and its capability to distribute the current across a larger cross section.

4.3.3 Extraction of partial inductances in the gate-source loop

The analysis done in Section 4.3.2 for the inductances in the power path of the module, is also performed for the gate-source loops in the module. It is assumed that there is no common source inductance shared between the power and gate loop, which is true, as the source connection is realized through a Kelvin connection. However, there will be magnetic coupling between these loops, but they have been left out as the coupling terms would be difficult to keep good track of. The paths subjected to analysis are marked in Figure 4.10.

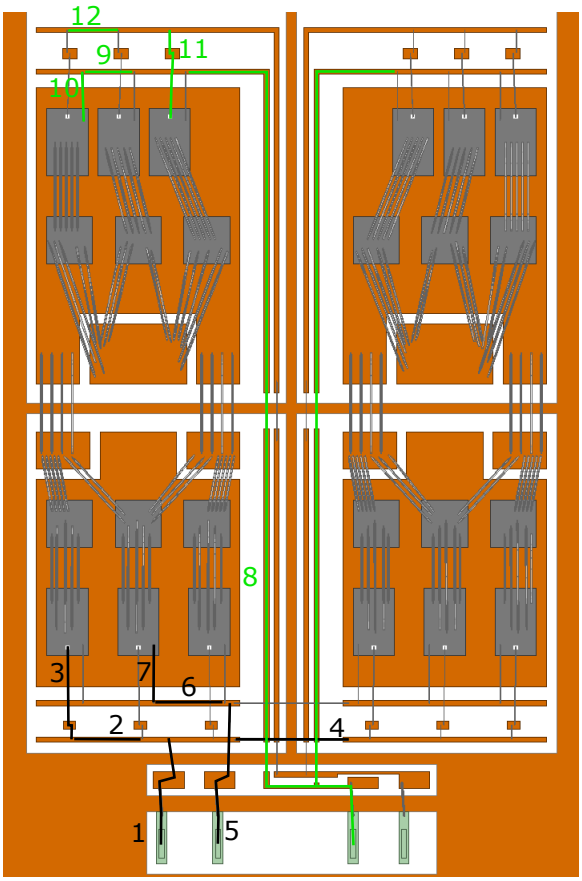


Figure 4.10: The power module with markers that indicate the paths to be analyzed in the gate-source loop.

The black markers are for the upper switch and the green markers are for the lower switch. Marker number 8 is for the equivalent inductance of the DBC trace for the lower source, which is common for all the six lower MOSFETs. This is done due to nearly perfect symmetry between the source connections of the left and right lower MOSFETs, and the gate traces of the lower MOSFETs are also analyzed in the same way.

Table 4.3: Explanation of the different conduction paths shown in Figure 4.10.

Marker no.	Explanation
1	Upper gate terminal and connection to DBC.
2	Copper trace between two upper MOSFET gate connections.
3	Upper MOSFET gate bondwire connection.
4	Bondwire traverse between upper left and right pads.
5	Upper source terminal and connection to DBC.
6	Copper trace between two upper MOSFET source connections.
7	Upper MOSFET source bondwire connection.
8	Common equivalent gate/source path for lower MOSFETs.
9	Copper trace between two lower MOSFET source connections.
10	Lower MOSFET source bondwire connection.
11	Lower MOSFET gate bondwire connection.
12	Copper trace between two lower MOSFET gate connections.

The extracted values and the gate-source circuit is shown in Figure 4.11. The partial inductances are extracted for a frequency of 3 MHz, and are numbered accordingly to the marker numbers given in Table 4.3. No inductive coupling between different conduction paths is modelled for simplicity, as the coupling would make the model very complex. At a later stage, when this circuit will be implemented in LTSpice, the most significant coupling will be accounted for, that is the coupling between L1 and L5 and between L8_1 and L8_2.

One can see from this figure that the stray inductances in the gate loop are much higher than the ones in the power loop. This is due to the thin and slender DBC traces for the gate and source paths, as well as the thinner bondwires. In the power loop the conducting parts are wide and several bondwires are connected in parallel to keep the inductance as low as possible and have higher current capacity. This has not been done in the gate-source circuit, maybe due to limited space or that it is not needed. In fact, the slew rate of the current in the gate loop is much lower than for the power loop during operation, which means that eventual overvoltages in the gate loop will be far lower than those experienced in the power loop [8]. Even though this is usually the case, the high inductance of the lower MOSFET control signal paths might be problematic and might lead to excessive ringing. This is also the reason for having an internal gate resistor for each of the MOSFETs inside the power module, as it will add damping to the circuit.

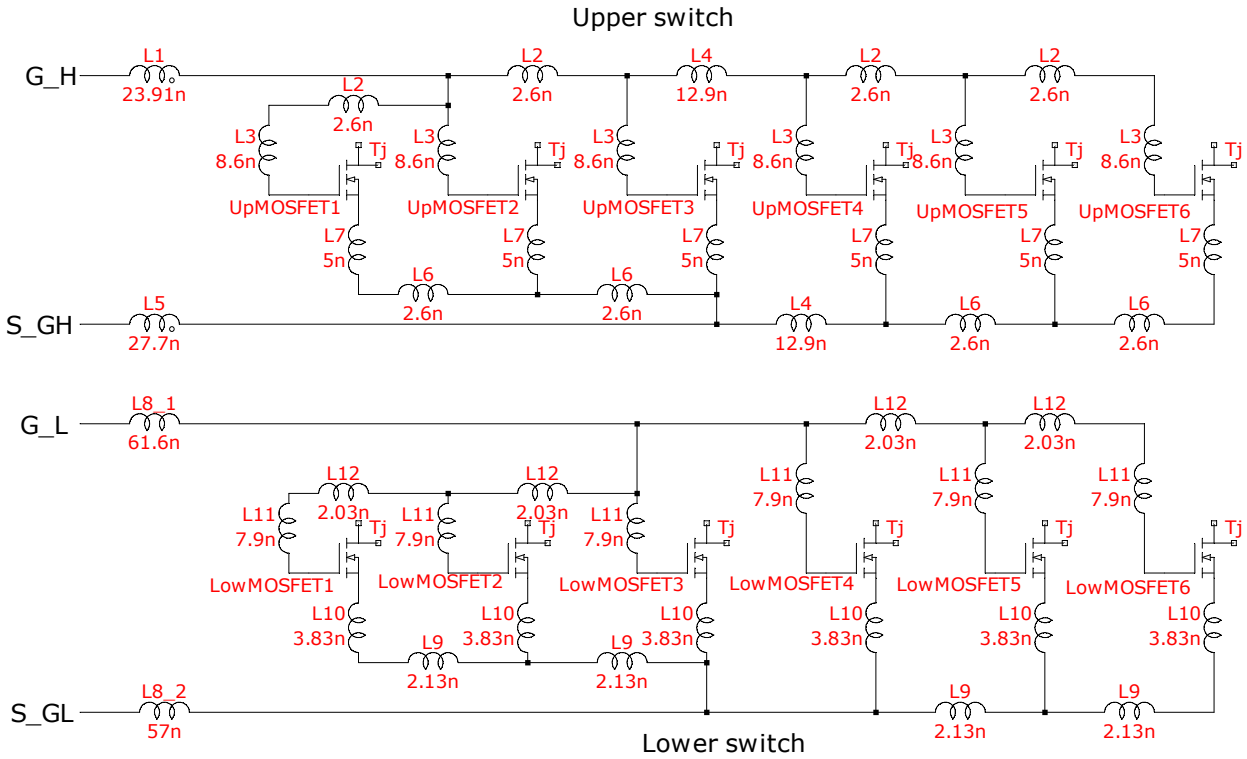


Figure 4.11: Parasitic model of gate-source circuit in the module.

4.4 Theory for thermal analysis

One of the most important aspects in power module design and application is the thermal management. The module has to be able to dissipate the generated heat without surpassing the allowable junction temperature. This has to be determined for different operating conditions, i.e. different power dissipation levels. The lower the temperature is, the better the package, as lower thermal resistance between the chip junction and heatsink means that the module can operate at higher power density with the same temperature increase as a package with a more thermally resistive structure. This section will present the relevant theory for a thermal analysis of power module package.

4.4.1 Characterization of the thermal layers in the power module

In heat transfer by conduction the temperature difference across of a structure is determined by the by the heat flow rate, P, and the thermal resistance, R_{th} [1]:

$$\Delta T = P \cdot R_{th} \tag{4.4.1}$$

The thermal resistance is defined as:

$$R_{th} = \frac{d}{\lambda A} \tag{4.4.2}$$

Where d is the thickness of the layer, λ is the thermal conductivity of the material and A is the cross-sectional area over which the heat is conducted. λ of a material is given in the

unit of watt per centigrade-meter, and depends on the material. Generally, λ, is a function of temperature and will decrease with increased temperature. For instance, λ of SiC is 400 W/(m·K) at 25 °C, while at 100 °C it is 260 W/(m·K) [27]. However, in this thesis λ is assumed to be constant in the region of operation.

If a structure is consists of several layers, such as the power module, the total thermal resistance is the sum of the thermal resistances of the individual layers:

$$R_{th} = \sum_i \frac{d_i}{\lambda_i A_i} \tag{4.4.3}$$

d_i, λ_i, A_i are the thickness, thermal conductivity and cross-sectional area of the i-th layer. This equation will also consider heat spreading within the module, as the heat moves towards the case surface. This is usually done by assuming a constant spreading angle, which is generally chosen to be 45°. Such a structure with indicated heat spreading angle is illustrated in Figure 4.12.

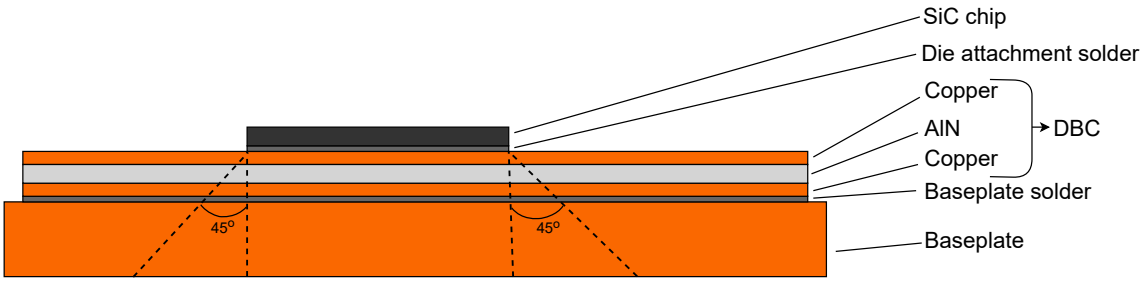


Figure 4.12: Model of the layered structure in a power module with heat spreading.

This is a simple approach for determining the thermal performance of a power module, but is has several flaws which affect the accuracy of the results. The model assumes that the heat will spread homogeneously across the area of each layer, which is often not the case. The model also assumes that the interface between two layers is perfectly isotherm and that is also almost never the case. This is illustrated through a simulation performed in ANSYS Icepak in Figure 4.13 where 100 W of power is applied to the power MOSFET shown in Figure 4.12. It shows that the isothermals are non-planar, and that the heat does not spread homogeneously across each layer.

Furthermore, the heat spreading angle will vary between the layers and will also not be constant within a layer [28]. This model omits the thermal coupling between different chips placed on the same DBC as well. This interaction is difficult to model theoretically, and FEM simulations or real measurements have to be conducted to get reliable results.

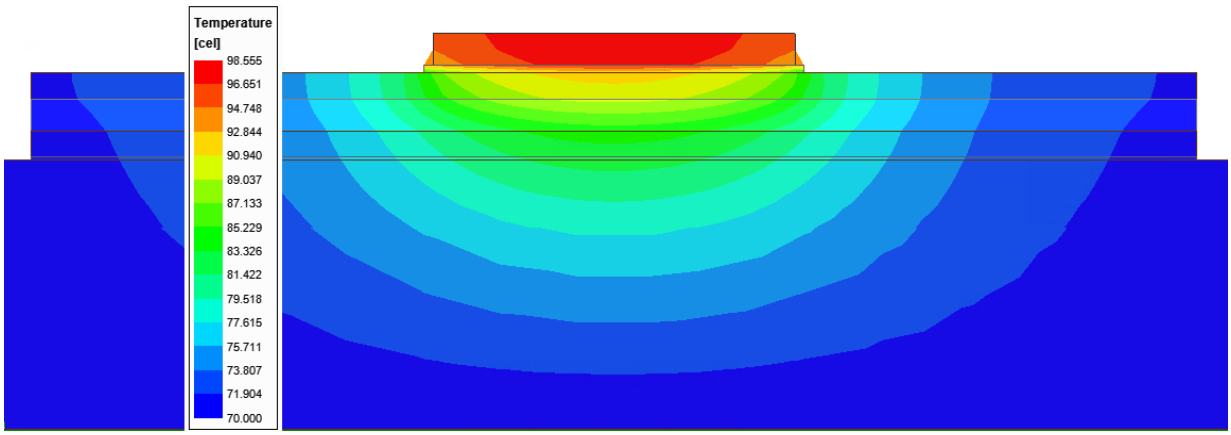


Figure 4.13: Heat spreading for a single MOSFET with T_{case} = 70 °C and P_{loss} =100 W.

4.4.2 Characterization and modelling of the boundary conditions

The boundary condition on the case surface of the power module has a great effect on the thermal performance of a module. The heat transfer across this interface will depend on the cooling system. For simulations this boundary condition has to be defined, so that it can emulate the real cooling solution. There are two main ways of doing this: isothermal case or a case surface with equivalent heat transfer coefficient, *htc*. One may also use the real geometry of the heatsink and mount it on the case, but this was not done in this thesis as implementing a real heatsink geometry would take more more time and increase the simulation time.

By assigning a isothermal boundary, that is a fixed case temperature, the whole case surface is forced to have one temperature, as illustrated in Figure 4.13. This is hardly ever the case, as the heat will be more concentrated just below the heat source, i.e. chip. This together with heat spreading, will lead to varying temperature over the whole case surface [29].

The second method is realized by applying a *htc* to the case and it is defined to be the amount of heat transferred by convection between a solid and fluid [30]:

$$htc = \frac{q}{\Delta T} \tag{4.4.4}$$

q is the heat flux, that is the heat transfer between the solid and fluid and is defined as the power loss in the module per unit area W/m^2. ΔT is the temperature difference between fluid and solid surface. This can be extended into:

$$R_{th} = \frac{1}{htc \cdot A} \tag{4.4.5}$$

Here R_{th} and A are the thermal resistance and the effective area for heat dissipation of the heatsink. One can see that the thermal resistance of the heatsink will decrease with higher *htc*. Thus, by selecting a suitable *htc* for the case surface, the heatsink can be emulated. The *htc* will depend on the cooling solution, and will vary from 10 W/(m^2·K) for natural convection to 100 000 W/(m^2·K) for solutions with phase change. Generally, forced convection with air will yield a *htc* up to 200 W/(m^2·K) and for water cooled solutions the

htc can be as high as 10 000 W/(m^2·K) [30]. Figure 4.14 shows simulated values of the same configuration as in Figure 4.13, but with a *htc* of 4500 W/(m^2·K) applied to the case boundary.

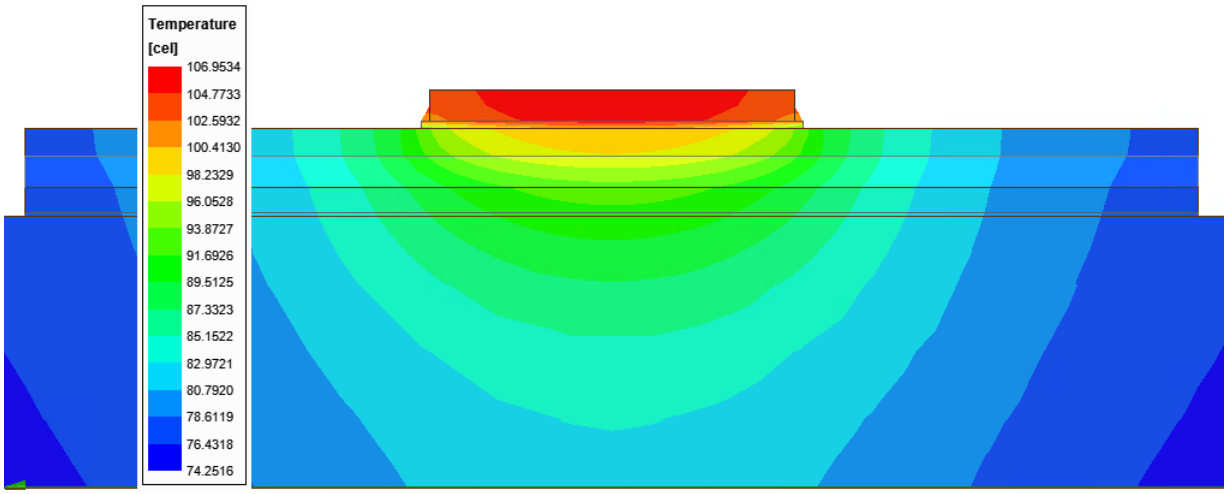


Figure 4.14: Heat spreading for a single MOSFET with *htc* =4500 W/(m^2·K) and P_{loss} =100 W.

The figure reveal that the case temperature is far from isothermal and the case temperature below the MOSFET is much higher than any other points on the case. Moreover, increasing the *htc* further will make the heat more concentrated below the MOSFET. This will decrease the heat spreading and thus not take as much advantage of the large area of the baseplate.

R_{th} of the structure with a single MOSFET was calculated for different boundary conditions and the results are given in Table 4.1. One can see that they vary a bit. This is due to the fact that the heat spreads less in the model with fixed T_{case}, and hence R_{th} will be higher. The reason for this is that the heat will meet more resistance when it spreads and thus the heat flux is more concentrated below the MOSFET. In fact, fixing T_{case} means that the *htc* of the case surface is infinitely high and is thus just a special case of *htc* [28]. Even though R_{th} is higher for the fixed case temperature boundary, T_j will be lower as the cooling solution is more effective.

The theoretically calculated thermal resistance is based on the 45° heat spreading model, which introduces some inaccuracy due to the several simplifications the model is based on. Hence, there is a difference between the FEM results and the theoretical value.

Table 4.1: Thermal resistance of the structure shown in Figure 4.13.

Condition	R_{th} [°C/W]
Theoretical calculation	0.3045
FEM isothermal boundary	0.2886
FEM *htc* boundary	0.2467

4.5 Thermal analysis

In this section the thermal performance of the created power module will be assessed. However, to do this, the power losses have to be calculated for the module, so that the specific temperature distribution can be related back to a specific current. When this is done, the power losses can be applied in the FEM software ANSYS Icepak.

4.5.1 Calculation of power losses

The power losses are calculated using a purely resistive load. That means there is no inductance in the load, and the diodes will not conduct. Generally, there will be inductance in any real load, but in this case it is neglected. The conduction losses were calculated using the circuit shown in Figure 4.15.

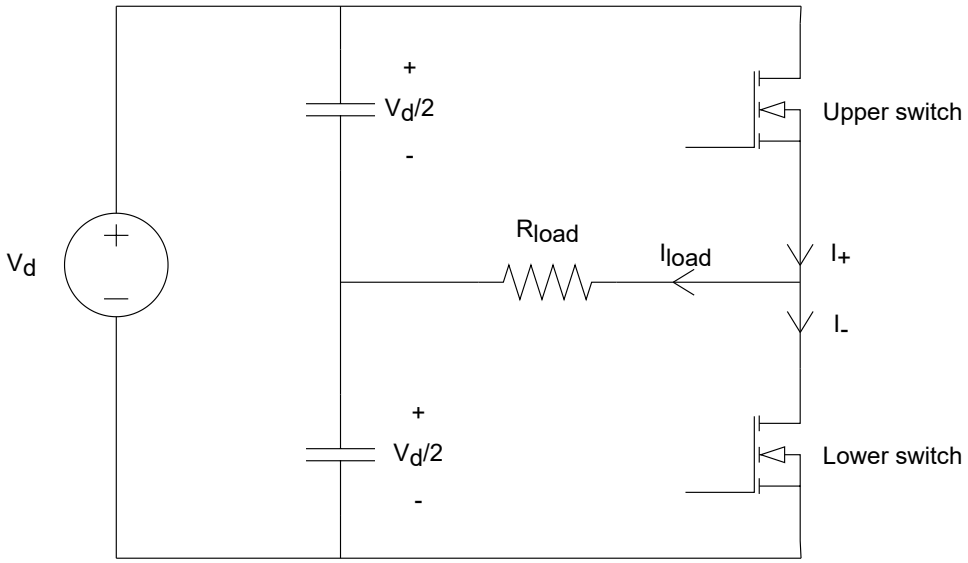


Figure 4.15: Simple circuit for calculating losses in a half-bridge configuration.

There are two ways to calculate the losses; the first way is to vary the duty cycles D of the upper and lower devices between 0 and 1 and the second method is to use a fixed duty cycle. The RMS current I_{RMS} through the upper and lower switch can be derived from Figure 4.15:

$$I^{+}_{RMS} = \frac{V_d}{2 \cdot R_{load}} \sqrt{D} = I_{load} \sqrt{D} \tag{4.5.1}$$

$$I^{-}_{RMS} = \frac{V_d}{2 \cdot R_{load}} \sqrt{1 - D} = I_{load} \sqrt{1 - D} \tag{4.5.2}$$

V_d and R_{load} are the bus voltage and load resistance respectively. By fixing R_{load}, the load current I_{load} can be fixed and thus D can be varied to achieve different I^{+}_{RMS} and I^{-}_{RMS}. However, at low and high D, the current will be very low in one switch and very high in the other switch, and thus will not give a good representation of the worst case scenario.
The second method, fixing D to a given value, usually 0.5, is a good way to simulate the

worst case power dissipation as the current is even in both switches, and can be increased or decreased by adjusting R_{load}. From here the conduction losses of one switch are calculated according to:

$$P_{cond} = R_{ds(on)} \cdot I_{RMS}^2 \tag{4.5.3}$$

$R_{ds(on)}$ is the on-state resistance of the MOSFET. The switching losses are calculated by using:

$$P_{sw} = f_{sw} \cdot (E_{sw,on} + E_{sw,off}) \tag{4.5.4}$$

Where f_{sw}, $E_{sw,on}$ and $E_{sw,off}$ are the switching frequency, turn-on energy and turn-off energy respectively. The total P_{loss} consist of both these terms and are evenly distributed between the six MOSFET dies that form each switch position, under the assumption that the current is evenly distributed among them.

For the thermal analysis the $R_{ds(on)}$ has been selected to be worst case value, according to the datasheet for the CAS300M12BM2 power module, that is 7.7 mΩ for $T_j = 150$ °C [13]. The switching energies are estimated by assuming a DC-link voltage of 800 V and by fitting a curve to the corresponding total switching energy graph in the datasheet. The equation for the total switching energy is:

$$E_{tot} = 3 \cdot 10^{-5} \cdot I_{ds}^2 + 0.0441 \cdot I_{ds} + 1.5387 \tag{4.5.5}$$

The equation is valid for I_{ds} between 100 and 400 A and yields values in the unit mJ. The switching losses are calculated using (4.5.4) and assuming f_{sw} =10 kHz. However, for the following analysis, the drain current is limited to 300 A.

4.5.2 Preparing the module for thermal FEM simulations

The simulation are done in ANSYS Icepak, which solves the heat equations using the ANSYS CFD numerical solver, Fluent [31]. It is based on the same principle as ANSYS Maxwell; the model is divided into several smaller volumes through a meshing process and then the heat transfer equations are solved for each of these volumes.

For the thermal simulations, the 3D model has been stripped of all interconnections and terminals, as they will have a negligible effect on the temperature distribution [32]. That means that only the chips and the layered DBC/baseplate structure will be simulated, which will improve the simulation speed. The simulated module is shown in Figure 4.16. Furthermore, an ambient temperature of 20 °C is used, and it is assumed that all the heat generated in the chips is only dissipated through the case surface, so there is no heat dissipating through the silicon gel over the top or through the sides of the module. Furthermore, the thermal conductivity of the materials are assumed to be independent of temperature, i.e. constant and are given in Table 4.1.

Table 4.1: Thermal conductivities of the materials used in ANSYS Icepak [11].

Material	Thermal conductivity [W/(m·K)]
SiC	490
Solder ($Pb_{95}Sn_5$)	32
Cu	400
AlN	120

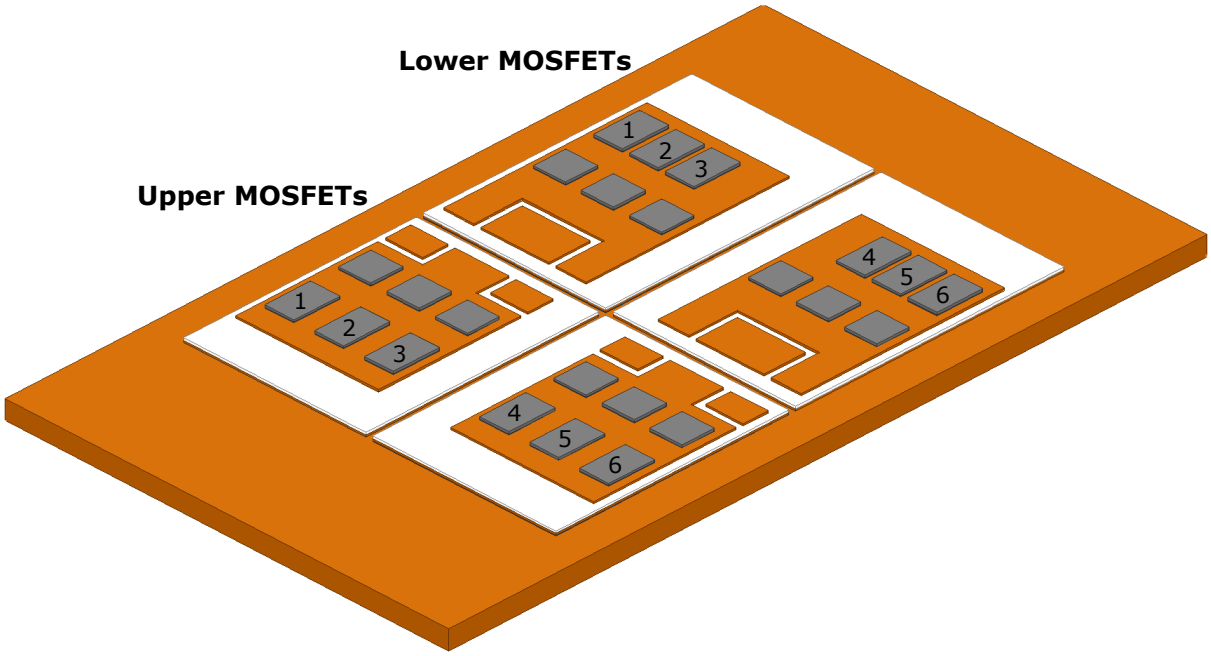
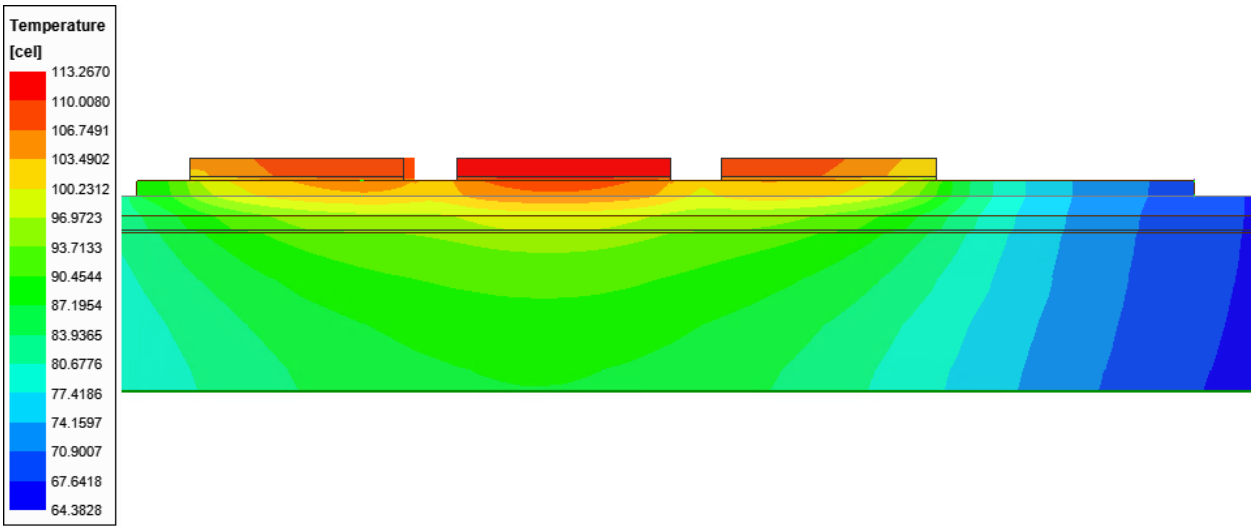


Figure 4.16: 3D model of the power module prepared for thermal analysis with numbered MOSFETs.

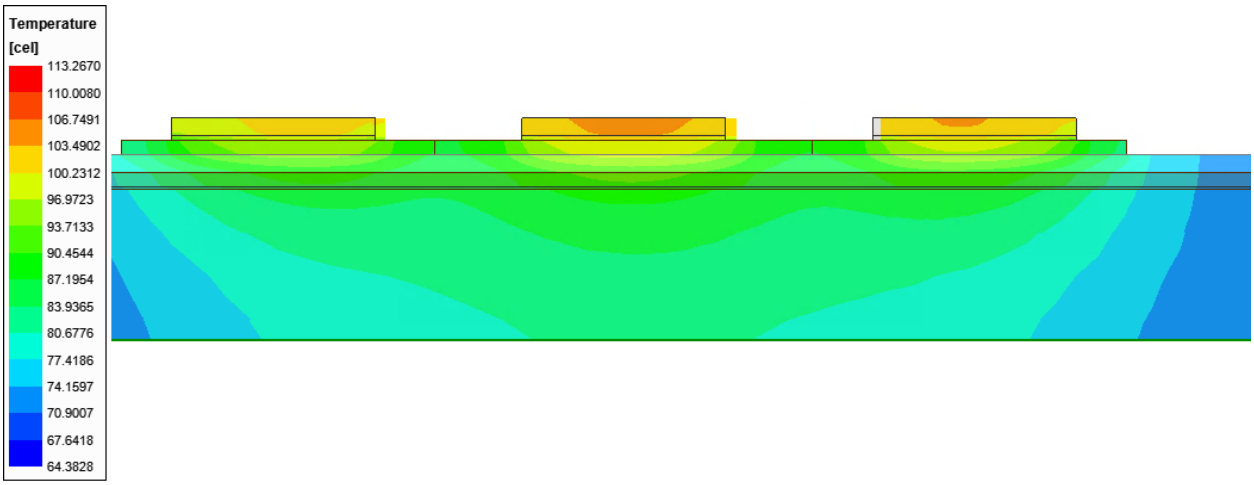
The power losses are calculated for currents between 50 A and 300 A in steps of 25 A with a fixed duty cycle of 0.5. They are applied to the MOSFET as a heat source and are evenly distributed over the chip volume. The SBD are assumed to not conduct at all, since the load is purely resistive. T_j is defined as the temperature on the middle of the top chip surface, and the T_{case} is the temperature of the point below the MOSFET on the case surface.

4.5.3 Simulations with *htc* case boundary

In this analysis different values of *htc* are applied to see how the different T_j and R_{th}. Figure 4.17 show the temperature distribution over the cross-section for the lower and upper switch with $htc = 4000$ W/(m^2·K) and $I_d = 225$ A. By looking at the isotherms in the lower switch, one can see that they connect much more between the chips, leading to higher T_j and T_{case}. This phenomenon is not as prominent in the upper switch, as there is more space between the chips and more of the substrate and baseplate is used to spread the heat. This leads to lower T_j and T_{case} and can be seen out of the coloring in the plots.



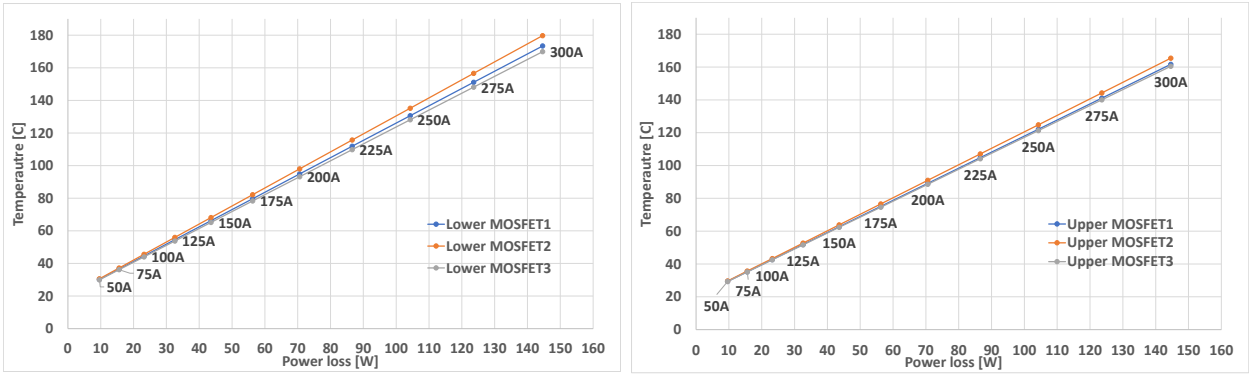
(a)



(b)

Figure 4.17: Temperature distribution over the cross-section of (a) lower switch and (b) upper switch. $htc = 4000$ W/(m^2·K) and $I_d = 225$ A (86.6 W per chip).

T_j of the lower and upper MOSFETs at varying I_d are shown by the graphs in Figure 4.18 for $htc = 4000$ W/(m^2·K). The pads and the arrangement of the MOSFETs on a pad are symmetrical to one another, as illustrated in Figure 4.16, which means that the temperature distribution will be symmetrical under the assumption that the same power is applied to each MOSFET in the corresponding pad. Thus, only the temperatures of the chips on a single pad are shown.



(a) **(b)**

Figure 4.18: Temperature of (a) lower and (b) upper MOSFETs 1, 2 and 3 with power applied. The heat transfer boundary is selected to be modelled with $htc = 4000$ W/(m^2·K)

Several things can be observed from these graphs; the temperatures of the upper chips are generally lower than for the chips in the lower switch and there is a higher temperature difference between the lower chips than for the upper chips. This coincide well with the findings from Figure 4.17, from which it was concluded that there is more coupling between the chips in the lower position. Thus, the middle die in the lower pads experience the T_j.

However, the FEM simulation is not able to consider the fact there will be a self-balancing effect between the paralleled chips since $R_{th(on)}$ is a function of T_j. When the temperature of a single die is higher, its $R_{th(on)}$ will be higher as well, which means that more current will flow through the other dies. These dies will be heated more and their resistance will increase again and this will go on until a balance is reached. Thus, this might not be a big issue during operation.

Furthermore, the graphs show that the maximum $T_j = 150$ °C of the power module is exceeded, which means that a higher htc is required to limit the temperature. In fact, according to the FEM simulations, the htc has to be increased to 7000 W/(m^2·K) for the junction temperature of each MOSFET to be below 150 °C at $I_d = 300$ A. The simulations results for several different htc values are given in Table 4.2.

Table 4.2: Junction temperatures of upper and lower MOSFETs for $I_d = 300$ A (144.6 W per chip) and different htc.

htc	Upper MOSFET temperature [°C]			Lower MOSFET temperature [°C]		
[W/(m^2·K)]	1	2	3	1	2	3
5000	144.1	147.8	142.9	154.9	161.3	151.6
6000	134.6	138.1	133.3	144.7	151.1	141.6
7000	127.5	131.0	126.2	137.3	143.7	134.3

The table shows that the lower switch is the limiting factor of the power module with consistently about 10 °C higher T_j. That is expected, as the dies are more tightly packed but with higher htc this difference will decrease. Moreover, the middle chip is the limiting factor as it is thermally coupled to both chips beside it and it will decide the maximum T_j of

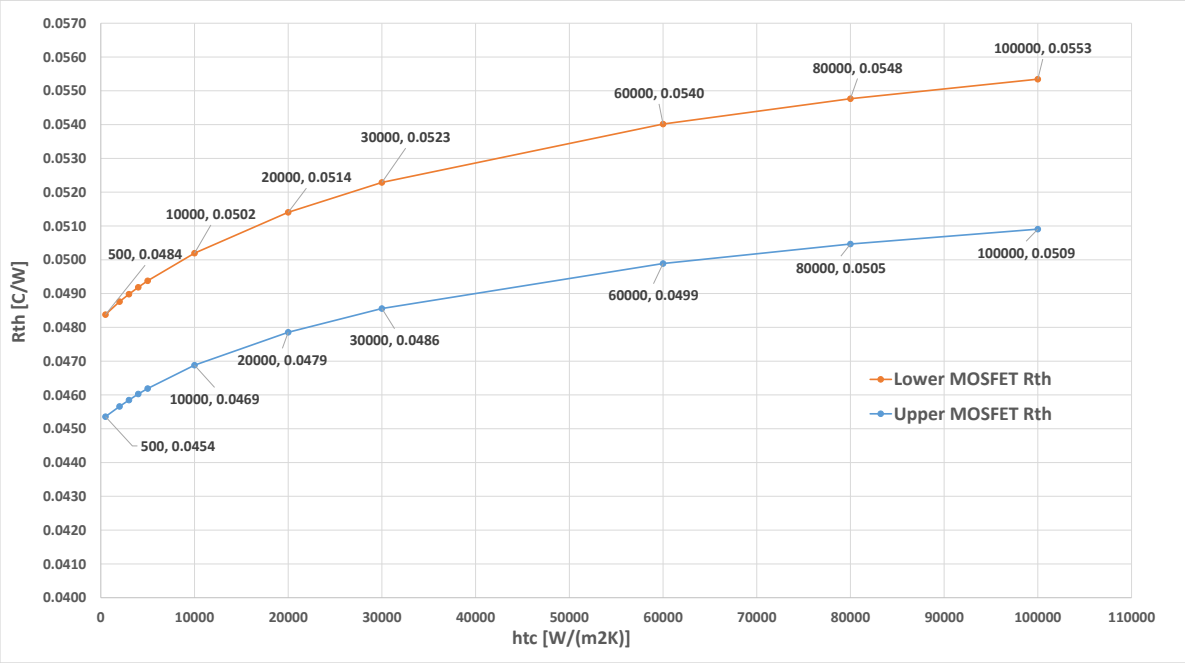


Figure 4.19: $R_{th(eq)}$ of upper and lower switch versus *htc* from FEM simulations.

the module. This is reflected by the datasheet of the single bare MOSFET die, which gives a maximum $T_j = 175$ °C [25], whereas the power module is limited to 150 °C [13]. Hence, the MOSFETs cannot be utilized to their greatest potential.

Figure 4.19 shows how the equivalent $R_{th(eq)}$ of the module develops with increasing *htc*. The R_{th} for one die is calculated using (4.4.1), where ΔT is the temperature difference between chip junction and the point of the case placed under the corresponding die. $R_{th(eq)}$ is calculated as a parallel connection of R_{th} for all the six chips forming a switch. Looking at the figure there is clear trend for $R_{th(eq)}$ to increase with higher *htc*, which is expected from the theory in Section 4.4.

There are some drawbacks by modelling the case with a *htc*. For instance, using the *htc* is only viable for simulations, as the case temperature will vary across the whole surface, making it difficult to estimate T_j by hand if the precise case temperature below the MOSFET die is not known and thus the given R_{th} will be rendered somewhat useless.

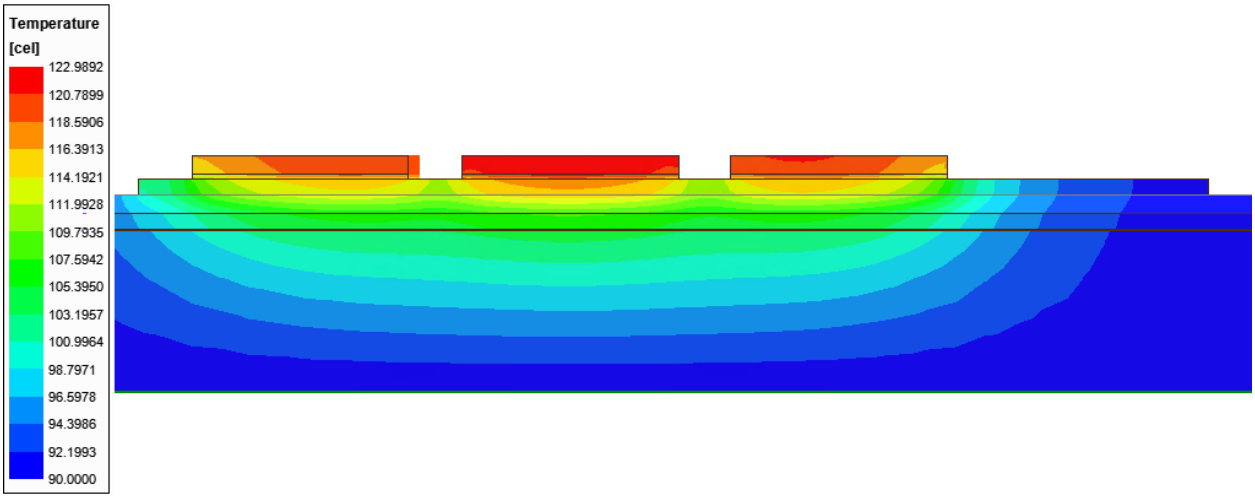
The *htc* does also not represent the heatsink quite well, as A in equation (4.4.5) is the effective heat dissipation area of the heatsink, that is the surface area over which the forced convection take place and this area is larger than the case surface. This means that the *htc* used in this analysis will only represent the heat transfer between the case and the heatsink. Hence, it must be a larger value so that the heatsink can be represented as the heat transfer is a function of area and the case surface is smaller compared to the effective heatsink area.

The geometry of the heatsink will also affect how the heat transfers over the interface and how it spreads over in the volume. All things considered, modelling the heatsink with a real geometry and fluid flow would provide more accurate simulation results, but at the cost of much longer simulation time.

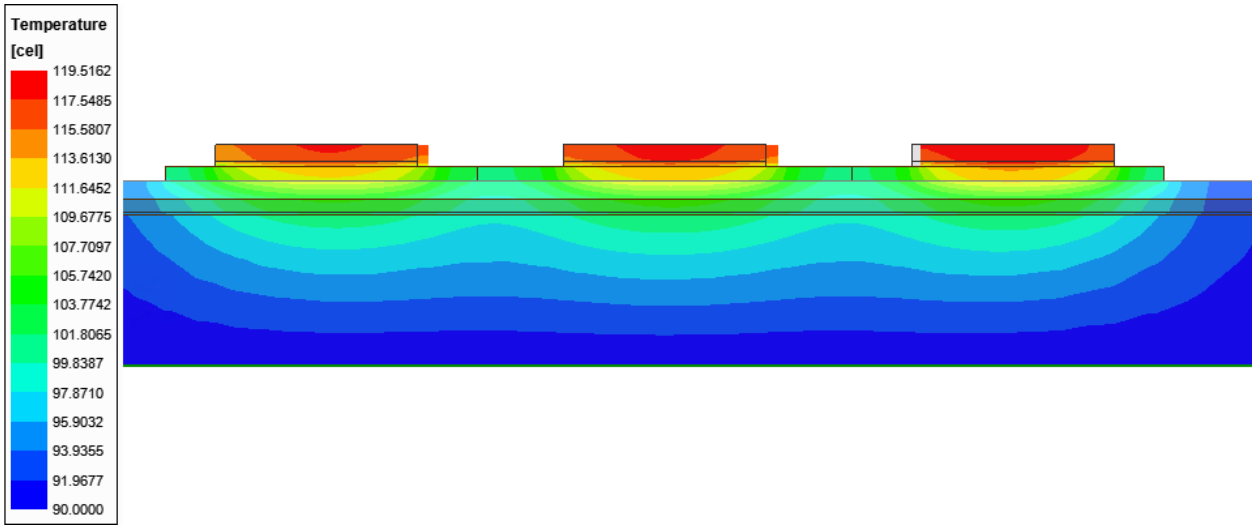
4.5.4 Simulations with isothermal case boundary

FEM simulations were also done for the power module with the case temperature fixed. Different values for T_{case} were tried and it was found that varying it will not affect R_{th} of the module. This is due to the fact that the heat transfer across the case surface is infinitely high, so decreasing or increasing the temperature will not affect the thermal resistance, but only increase or decrease the chip temperatures by the changed amount. Moreover, since the *htc* of a isothermal case is infinitely high, the R_{th} from the analysis will represent the upper asymptotes for the two graphs in Figure 4.19 as the *htc* goes towards infinity.

Figure 4.20 shows the temperature distribution over the cross section with $T_{case} = 90$ °C. Similar observations can be made here: there is less coupling in the upper switch position resulting in lower T_j compared to the lower switch.



(a)



(b)

Figure 4.20: Temperature distribution over the cross-section of (a) lower switch and (b) upper switch. $T_{case} = 90$ °C and $I_d = 225$ A (86.6 W per chip).

Table 4.3 gives the temperatures of the chips for $I_d = 300$ A, and all the temperatures are well below the limit of 150 °C. The temperature difference between the chips will is much lower than in Section 4.5.3, and that is due to isothermal case, as it emulates a much stronger cooling solution.

Table 4.3: T_j of upper and lower MOSFETs for $I_d = 300$ A (144.6 W per chip) and $T_{case} = 90$ °C.

Upper MOSFET temperature [°C]			Lower MOSFET temperature [°C]		
1	2	3	1	2	3
118.9	118.5	117.8	120.8	122.8	120.7

Table 4.4 gives the $R_{th(eq)}$ of upper and lower switch. The thermal resistance is higher compared to the *htc* method.

Table 4.4: $R_{th(eq)}$ of upper and lower switch with $T_{case} = 90$ °C.

Upper MOSFET $R_{th(eq)}$	Lower MOSFET $R_{th(eq)}$
0.0547 °C/W	0.0603 °C/W

According to this, T_{case} can be maximum 97.7 °C to maintain a junction temperature below 150 °C at $I_d = 300$ A (144.6 W per chip). The datasheet of the physical module states that the equivalent thermal resistance junction-to-case for the MOSFET is typically 0.070 °C/W, and was measured at $T_{case} = 90$ °C and 150 W power dissipation [13].

The difference between the FEM simulations and datasheet may be explained by the fact that the FEM software will not always give the most precise values, as it is not able to capture all the interactions within the real module. The thermal conductivity of the materials are also temperature dependent, some more than other, which will make a difference for the junction-to-case resistance. The thermal conductivity of materials will usually decrease with higher temperature, and thus contribute to a higher thermal resistance [28], and has not been implemented in these simulations. The thicknesses of the different layers and the materials from Table 4.1 might also involve some inaccuracies which will affect the thermal resistance. Furthermore, the chips in each switch position might heat differently due to mismatches in the characteristics of each chip and the parasitic layout of the module, and there will be heating the copper traces and bondwires as well. All of this will contribute to differences between the FEM model and the physical module.

Also, if the temperature of the case below the die is selected according to a real cooling solution and T_j is theoretically calculated by using R_{th} from an isothermal case analysis, then the temperature will be overestimated, which is reasonable as it will add a margin of safety.

However, conclusions can be drawn from this analysis. The figures show how the temperatures are unevenly distributed among the paralleled chips, especially for the dies placed in the middle. Thus, the power module has to be de-rated so that the dies can be kept in a safe operating range and the full potential of SiC cannot be realized.

5 Simulation of switching performance in LTSpice

This chapter will investigate the switching characteristics of the module by creating and simulating the parasitic circuit in LTSpice. The required theoretical background will be laid out first.

5.1 Double-Pulse test

After extraction of parasitic components in ANSYS Q3D Extractor, the electrical layout of the module will be implemented in LTSpice, with all the relevant models for MOSFET and SBD provided by the manufacturer. The simulation will be a DPT, which will provide the switching characteristics of the DUT. DUT in this case will be one of the switch positions in the power module. The circuit for a DPT is shown in Figure 5.1.

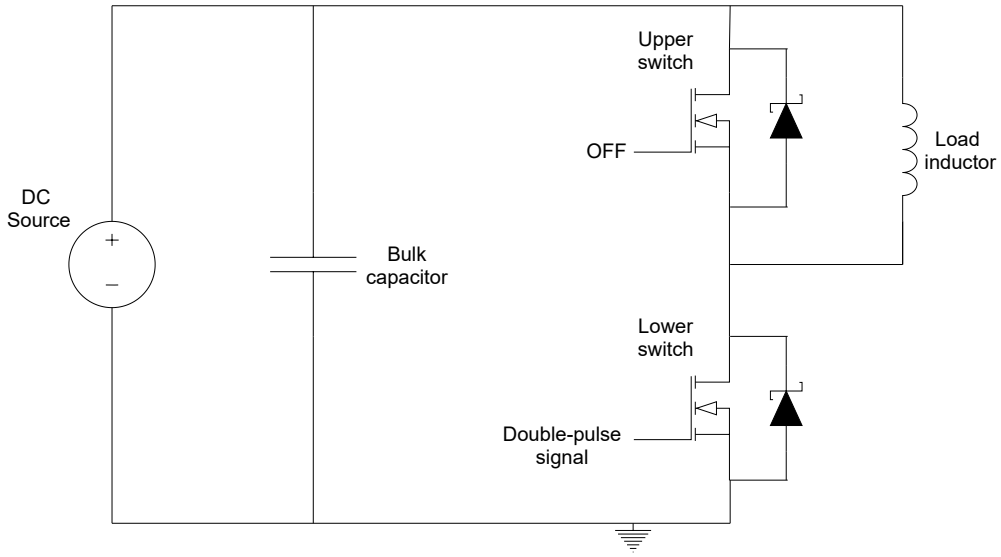


Figure 5.1: The circuit for DPT with an inductive load.

Usually a pure inductive load is used to build up the load current to a value at which the test is performed. The time required to build up a desired current I_d can be calculated by:

$$V_{DC} = L\frac{di}{di} \quad \rightarrow \quad \Delta t = L\frac{\Delta I}{V_{DC}} \tag{5.1.1}$$

The lower MOSFET will be turned on during the first pulse, and a current is charged through the inductor. When the I_d that is to be analyzed is achieved, the MOSFET is turned off, and the current commutates to the upper SBD. During this stage I_d is circulating through the upper SBD and load inductor for a short break. Next, the second pulse is applied

to the lower MOSFET and the current commutates back to the lower MOSFET. Thus, the hard-switching transients at turn-on and turn-off of the DUT can be analyzed at exact load currents. The general waveform of a double-pulse signal is shown in Figure 5.2.

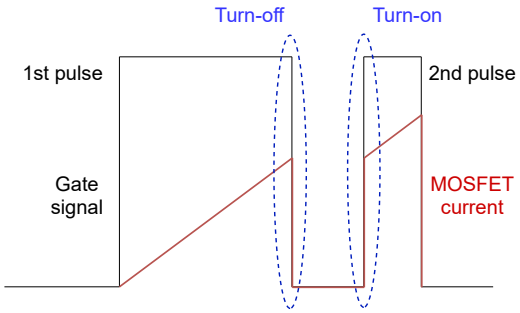


Figure 5.2: Double-pulse signal.

This pulse is usually applied to the gate with a low frequency (1 Hz), so that the DUT will be able remove the generated heat from the junction.

5.1.1 MOSFET switching transients

The transients that will be analyzed are shown in Figure 5.3. It shows the turn-on and turn-off waveforms of the drain current I_d, and drain-source voltage V_{ds}, as well as the gate-source voltage V_{gs}. The figure is not completely to scale, as the Miller plateau is omitted.

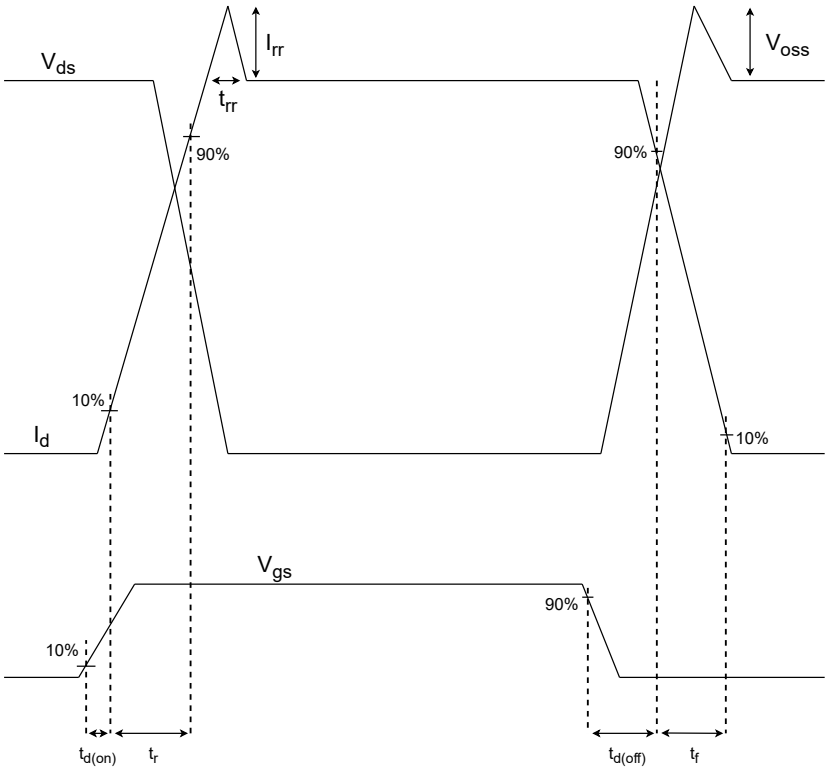


Figure 5.3: Switching times during transients.

The most important switching time parameters are illustrated in the figure. $t_{d(on)}$ is the turn-on delay time, and is the time from V_{gs} has risen to 10 % of its on-state values to the time I_d has risen to 10 % of its on-state value. t_r is the current rise time, and the time period for I_d to rise from 10 % to 90 % of its on-state value. The same goes for the turn-off times. $t_{d(off)}$ is the turn-off delay time, and is the time from 90 % V_{gs} to 90 % I_d. t_f is the current fall time and is the time from 90 % I_d to 10 % I_d. t_{rr} is the diode reverse recovery time and is the time it takes for the diode to remove the stored junction charge. The fall and rise times can also be defined for the voltage waveform. t_{rv} is the voltage rise time, and is the time for V_{ds} to rise from 10 % to 90 % of final blocking voltage, whereas t_{fv} is the voltage fall time and is the time it takes V_{ds} to fall from 90 % to 10 % of blocking voltage. The voltage derivative at turn-off and current derivative at turn-on can be calculated by:

$$\frac{dv}{dt} = \frac{0.9 \cdot V_{ds} - 0.1 \cdot V_{ds}}{t_{rv}} = \frac{0.8 \cdot V_{ds}}{t_{rv}} \tag{5.1.2}$$

$$\frac{di}{dt} = \frac{0.9 \cdot I_d - 0.1 \cdot I_d}{t_r} = \frac{0.8 \cdot I_d}{t_r} \tag{5.1.3}$$

As the switching transients of SiC MOSFETs are very fast and the derivatives of the current and voltage are very high, there will be overshoots and ringing in the waveforms due to the parasitics in the circuit, which can be seen to a degree in Figure 5.3. V_{oss} is the turn-off voltage overshoot, and there is turn-on current overshoot as well, which is created mainly due to the reverse recovery of the diode. This is more notable in simulated switching transients shown in Figure 5.4. The oscillations contain energy that circulate between the LC components in the device, where the inductance is due to circuit layout and the capacitance is mostly due to the capacitance of the transistors and diodes. This is an underdamped system and it takes a while for the oscillations to reach steady state, which depends on the damping provided by stray resistance in the module and $R_{ds(on)}$ of the MOSFET.

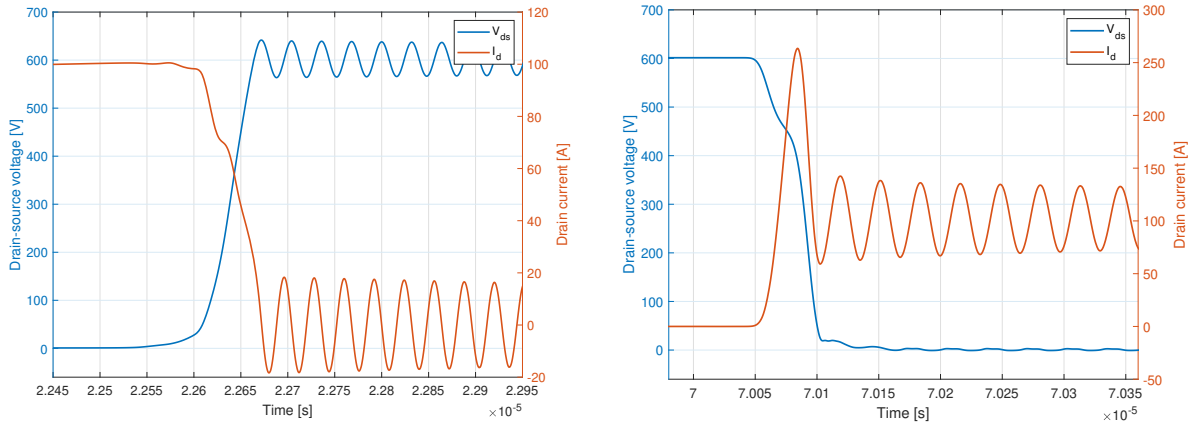


Figure 5.4: Simulated switching transients for (a) turn-off and (b) turn-on.

5.1.2 Switching losses in MOSFETs

The switching losses of power MOSFETs can be determined through DPTs at different V_{ds} and I_d. It is important to investigate these losses as they will contribute significantly to the total power losses of a module. The total power loss in a MOSFET is given as:

$$p_{loss}(t) = v_{ds}(t) \cdot i_d(t) \tag{5.1.4}$$

This equation contains both the on-state losses and conduction losses. When the MOSFET is in its off-state, there will be a small leakage current, but the generated losses are negligible. However, in the on-state of the MOSFET, power will be dissipated in the MOSFET due to the on-state resistance $R_{ds(on)}$. Anyhow, a DPT is not well suited for determining the conduction losses, as the drain current is strictly increasing due to the purely inductive load. It is better suited for determining the switching losses generated during the turn-on and turn-off transients as specific values of I_d. This is shown in Figure 5.5.

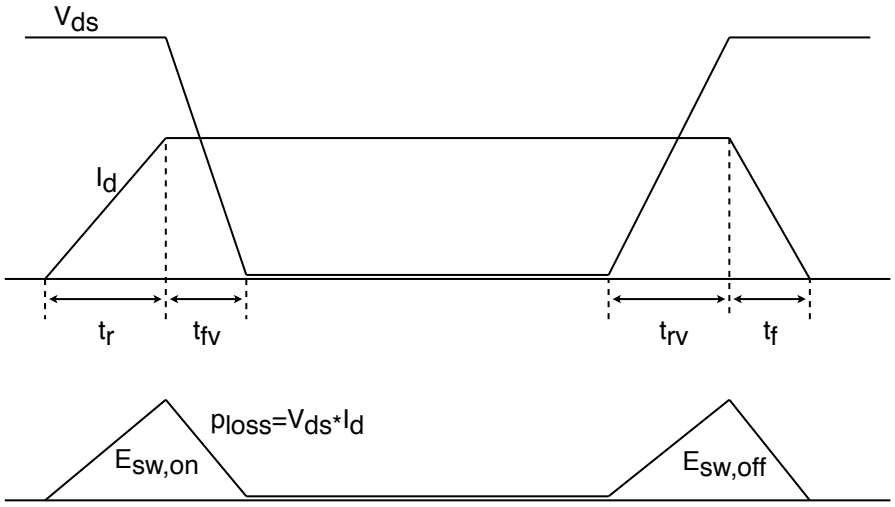


Figure 5.5: Switching losses in MOSFET.

The product of V_{ds} and I_d can be integrated to obtain the power losses during the switching transient:

$$E_{sw,on} = \int_0^{t_r+t_{fv}} p_{loss}(t)dt = \int_0^{t_r+t_{fv}} v_{ds}(t) \cdot i_d(t)dt \tag{5.1.5}$$

$$E_{sw,off} = \int_0^{t_f+t_{rv}} p_{loss}(t)dt = \int_0^{t_f+t_{rv}} v_{ds}(t) \cdot i_d(t)dt \tag{5.1.6}$$

The SBD will generate losses in the DPT as well due to the reverse recovery and conduction losses during freewheeling. The switching losses in the SBD are mostly generated during turn-off of the SBD, as the junction capacitance charge is removed. This turn-off reverse recovery current will affect $E_{sw,on}$, as it adds onto the transient drain current creating a large peak and leads to higher $E_{sw,on}$. The turn-on power losses of a SBD are negligible [5].

5.2 The circuit in LTSpice

The circuits shown in Figure 4.9 and Figure 4.10 were merged to form the entire electrical circuit of the module. This entire circuit in a DPT configuration is shown in Figure 5.6, where the lower switch is the DUT.

The layout also includes the internal gate resistors of the module. According to the datasheet of the power module, the equivalent internal resistance is 3 Ω, and since there are six dies in each switch, the gate resistor on each die is 18 Ω. However, the bare die by itself provides an internal gate resistance of 1.1 Ω, which makes the actual internal gate resistor equal to approximately 17 Ω [13], [25].

As mentioned in the previous chapter the most significant inductive coupling has been included in the LTSpice model. The coupling coefficients are given in Table 5.1. The reason for only modelling these coupling terms are that the model will become extremely complex with more coupling, since there will be coupling between all paths. Furthermore, the gate and source coupling terms do not only include the coupling between the terminals, but also between some of the DBC traces. It is assumed no coupling between the gate and power loops, even though Q3D Extractor simulations show some coupling between them and that might lead to noise from the power loop entering the gate loop.

Table 5.1: Most significant coupling terms in the power module.

Coupling between	Coupling coefficient
Positive terminal and negative terminal	-0.56
Negative terminal and output terminal	-0.26
Positive terminal and output terminal	-0.2
Lower gate and source path	-0.57
Upper gate and source path	-0.34

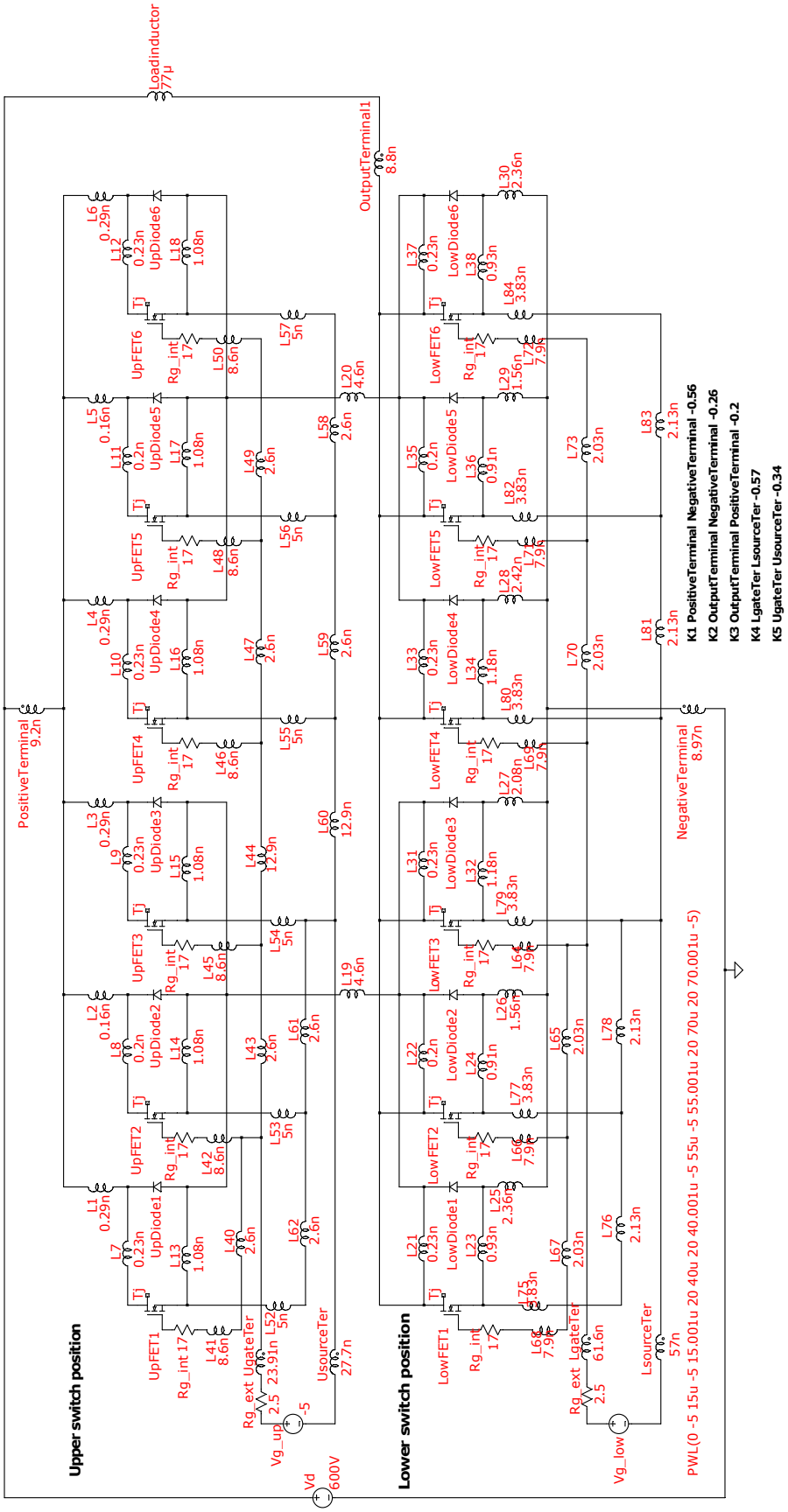


Figure 5.6: Parasitic model of the entire power module in a DPT configuration.

The DPT was performed using the same specifications as in the datasheet of the power module. That is, the load inductor is set as 77 µH, the gate voltage is switched between -5 and 20 V, the external gate resistor $R_{g(ext)}$ is fixed to 2.5 Ω and the T_j is 25 °C. T_j is fixed by putting a 25 V voltage source on the junction temperature terminal of the MOSFET. LTSpice models of the SiC MOSFET and SBD dies are provided by Cree and the gate drive circuit selected to be a single gate resistor with the same turn-on and turn-off path.

The load inductor is connected across the upper switch and this switch is always off as the voltage bias is always negative at -5 V. The lower switch is the DUT and is given the double pulse signal. An example of a double pulse test is given in Figure 5.7. The test is performed at V_{ds} = 600 A and I_d = 150 A.

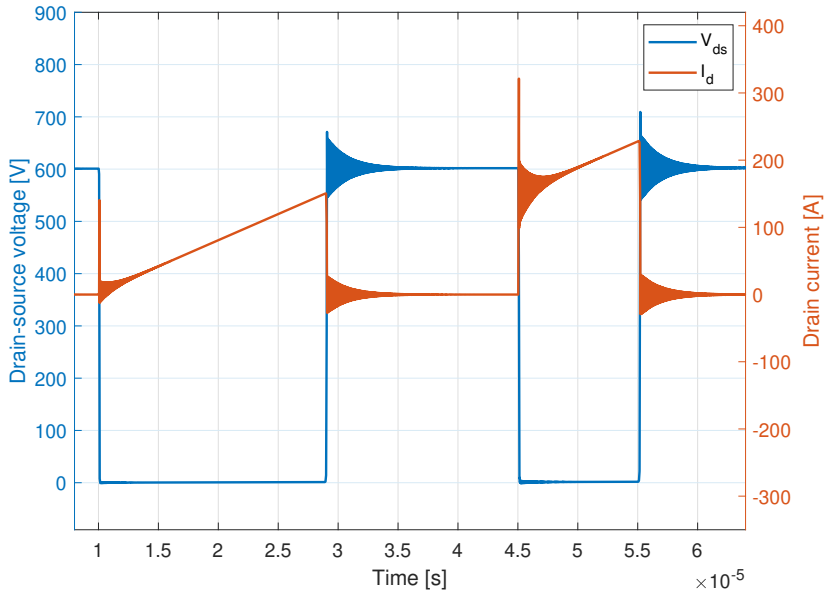


Figure 5.7: Double pulse test simulation.

5.3 Switching characteristics and losses

This section will present the results obtained from LTSpice simulations. The DPT will be performed for V_{ds} = 600 V and I_d varying from 50 to 400 A.

5.3.1 Turn-off switching characteristics

An example of turn-off switching characteristics at I_d = 150 A drain current is shown in Figure 5.8. It shows a overshoot in the voltage and ringing in both current and voltage waveforms. Table 5.1 gives the voltage rise time t_{rv}, current fall time t_f, voltage derivative dv/dt and voltage overshoot V_{osc} at different drain currents so that the switching transients can be compared. These values are determined using the theory presented in Section 5.1.

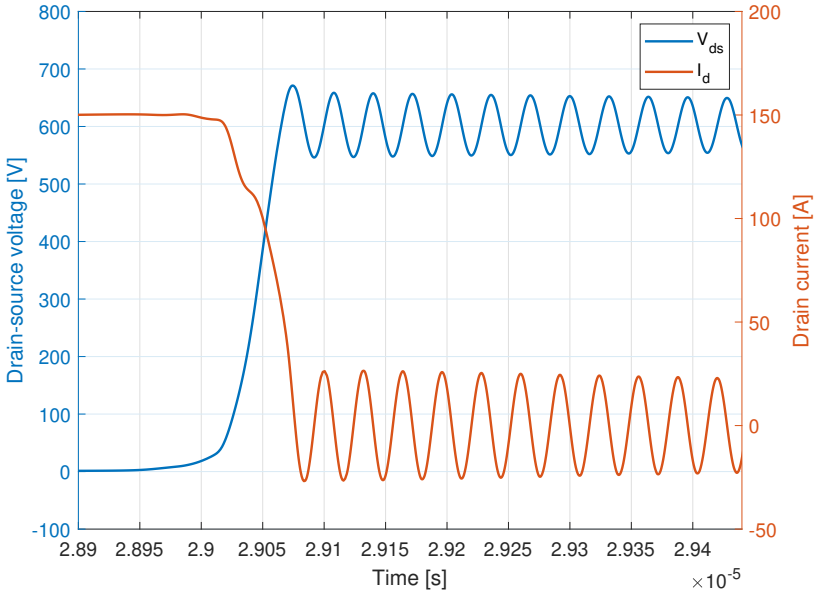


Figure 5.8: DPT turn-off characteristics at 600 V and 150 A.

One can see V_{osc} increases with I_d. This is due to the fact that the current fall time decreases, leading to higher drain current derivative and larger induced voltage overshoot. Furthermore, the t_{rv} also decreases with larger I_d and lead to higher voltage derivative. There is also a larger difference between the measurements at 50 A and 100 A than between any other measurements. This is due to the oscillations becoming more significant at 50 A, making it difficult to get good measurements of the rise and fall times.

Table 5.1: Switching characteristics at turn-off.

I_d [A]	t_{rv} [ns]	t_f [ns]	dv/dt [V/ns]	V_{osc} [V]
50	71.7	89.3	6.7	14
100	46.4	56.0	10.3	42
150	39.7	49.0	12.1	72
200	36.0	46.6	13.3	96
250	34.2	45.1	14.0	118
300	33.1	44.9	14.5	137
350	32.4	44.9	14.8	151
400	32.0	44.4	15.0	165

5.3.2 Turn-on switching characteristics

The same way, the turn-on characteristics are examined for I_d between 50 A and 400 A. An example of turn-on switching characteristics is shown in Figure 5.9. The current transient has a large current overshoot with long lasting ringing. The ringing is almost negligible in the voltage waveform. Similarly, Table 5.2 gives the turn-on parameters so that the switching

transients can be compared for different drain currents. The values given are the voltage fall time t_{fv}, current rise time t_r, current derivative di/dt and current overshoot I_{osc}.

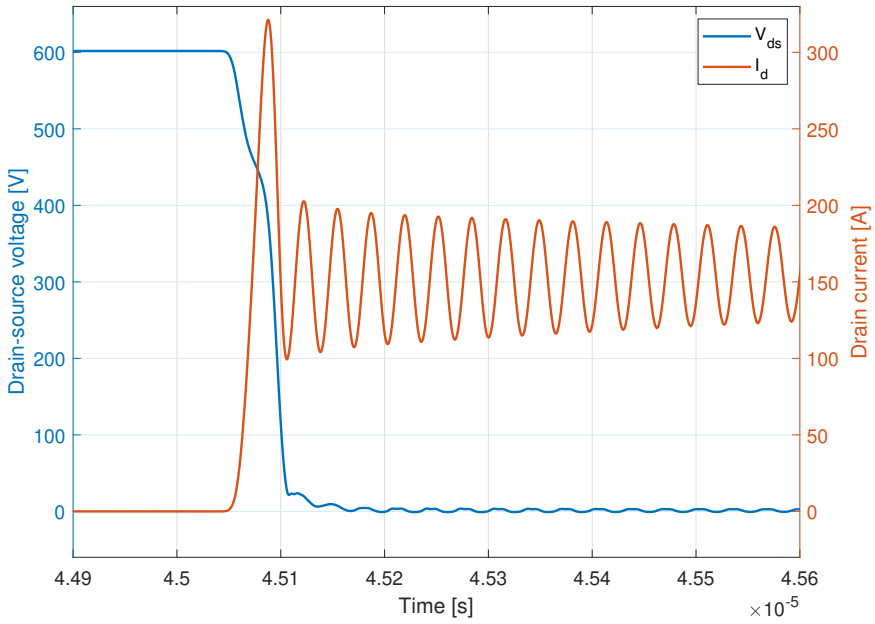


Figure 5.9: DPT turn-off characteristics at 600 V and 150 A.

Table 5.2: Switching characteristics at turn-on.

I_d [A]	t_{fv} [ns]	t_r [ns]	di/dt [A/ns]	I_{osc} [A]
50	36.0	8.8	4.5	154
100	39.6	11.3	7.1	164
150	44.7	13.8	8.7	170
200	46.3	15.9	10.1	177
250	49.5	18.2	11.0	182
300	54.5	20.4	11.8	187
350	55.7	22.4	12.5	191
400	58.4	24.7	13.0	196

The table shows that the switching times are increasing with drain current, as it takes longer time for the MOSFET to traverse the different regions of the I-V characteristic to reach the desired current. There is a current overshoot at turn-on, as the reverse-recovery current of the SBD is discharging its junction capacitance. This overshoot value is not as dependent on drain current as the voltage overshoot, since the junction capacitance is nearly independent of drain current. This leads to a reverse-recovery current also less independent of drain current and relates well with the theory presented in Section 2.2.2. However, some variation is observed.

5.3.3 Switching energy

The turn-off and turn-on switching powers are calculated by multiplying the drain-source voltage and drain current. The switching power at 150 A and 600 V is shown in Figure 5.10. By integrating these waveforms, the switching losses are obtained. At turn-off there is much more ringing in the switching energy, which is due both the current and voltage oscillating together at turn-off, whereas at turn-on there is almost no ringing in the voltage. For turn-off only the initial peak is integrated and the energy contained in the oscillations is ignored. The reason for this is that is was found that the energy contained in the oscillations was usually below 0.1 mJ.

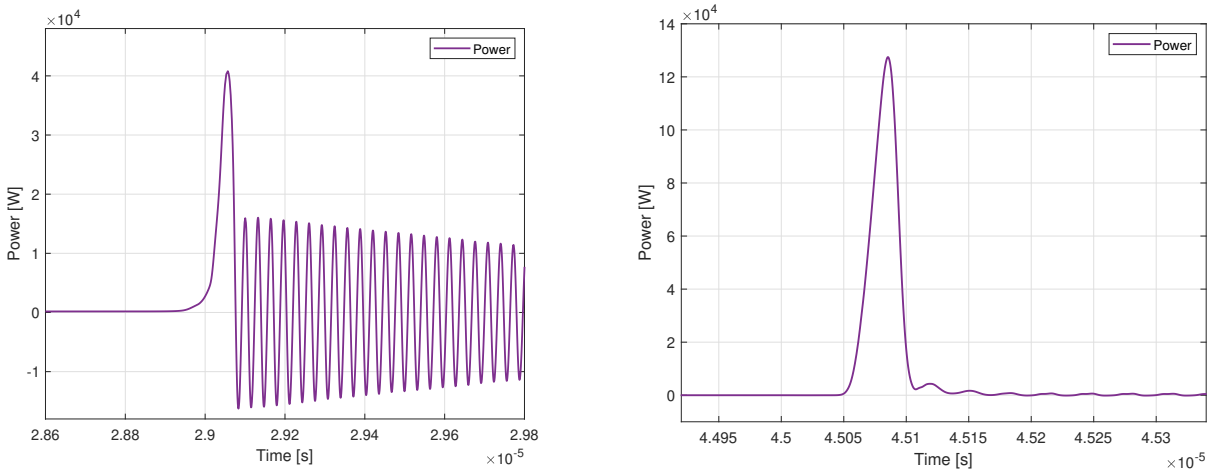


Figure 5.10: Switching power at (a) turn-off and (b) turn-on.

The simulated switching losses at 600 V V_{ds} are shown in Figure 5.11. It shows turn-on energy E_{on}, turn-off energy E_{off} and total energy E_{tot}. The figure also shows the experimental switching loss graphs provided by Cree for comparison.

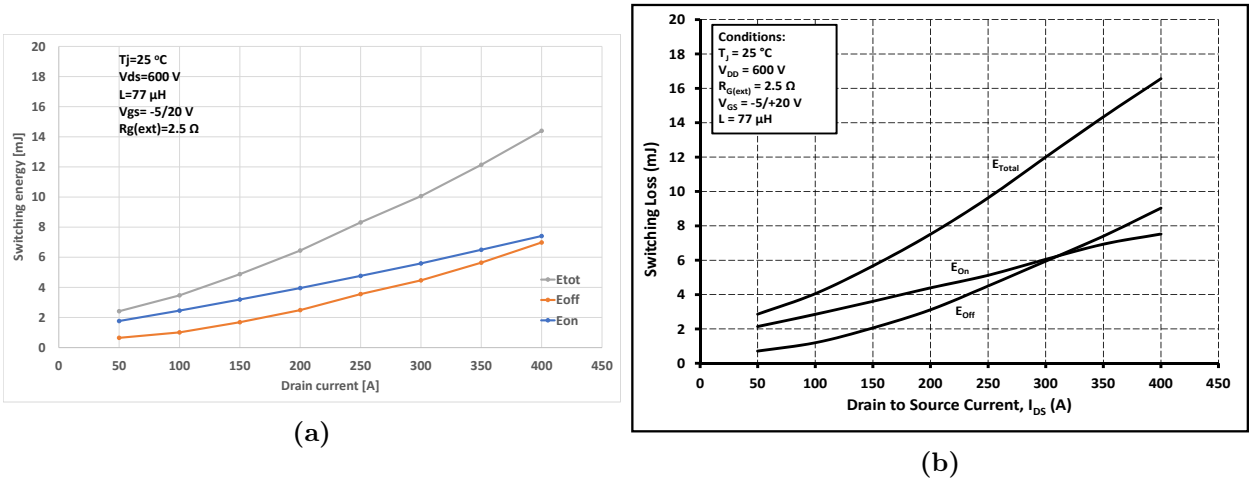
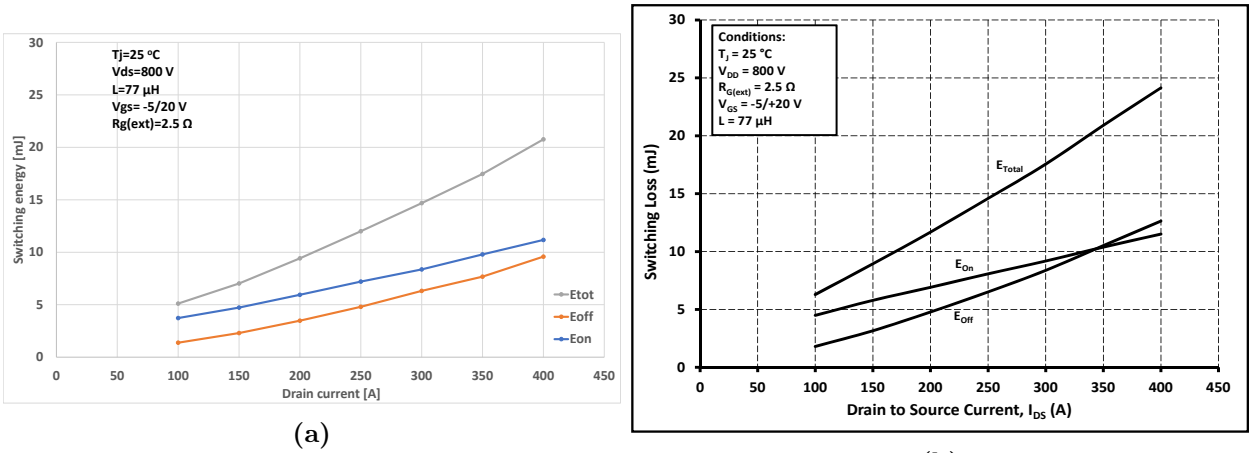


Figure 5.11: (a) Simulated and (b) datasheet switching losses at 600 V drain-source voltage [13].

Both the turn-off and turn-on losses increase with drain current, as expected. The simulated switching losses follow the same trend as the experimental losses provided by Cree. However, they are lower than the values from Cree and do also not cross each other. There might be several reasons for this different behavior. The LTSpice model do not consider the self-heating of the device, and the junction temperature is fixed to 25 °C. This does not a realistic behavior, and as pulses are applied to the MOSFET, the junction temperature will increase with the width of the pulse. Due to this, the experimental double-pulses are applied at a low frequency, so that the device can cool between the pulses. The MOSFET SPICE models are also based on linearized capacitance equations, which is not the real case, as parasitic capacitances of a MOSFET are strongly non-linear. The capacitances decide how the switching transients develop and this may lead to inaccuracies between simulations and experiments [33]. Additionally, due to convergence problems in LTSpice, the tolerances had to be increased and the cost of that is reduced accuracy.

The switching losses have also been simulated at $V_{ds} = 800$ V. The simulation results and the graph from the datasheet for comparison is shown in Figure 5.12. Similar observations are made here: the simulation losses are lower than the experimental losses, but they do follow the same trend.

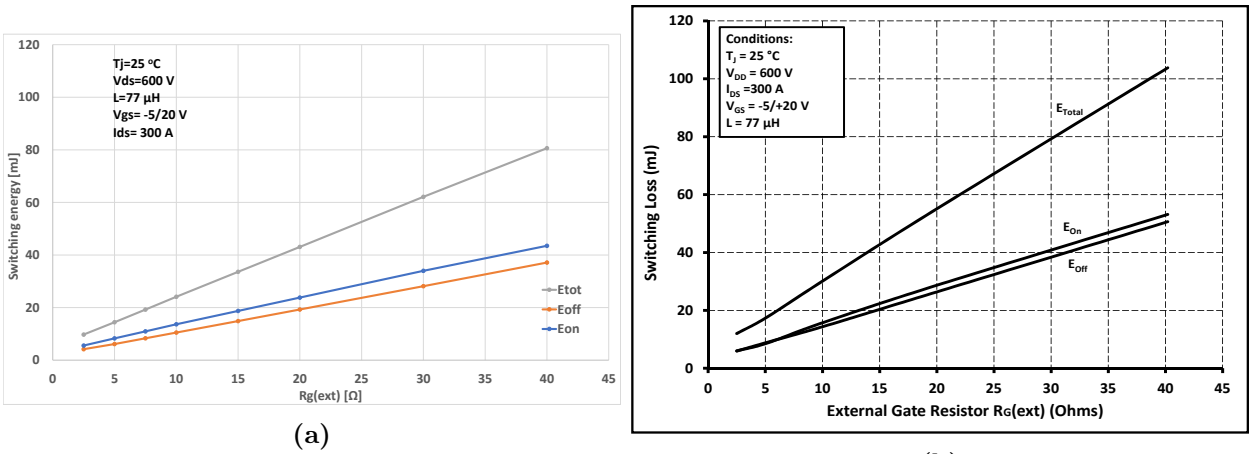


(a) (b)

Figure 5.12: (a) Simulated and (b) datasheet switching losses at 800 V drain-source voltage [13].

5.3.4 Gate resistor influence on switching energy and switching times

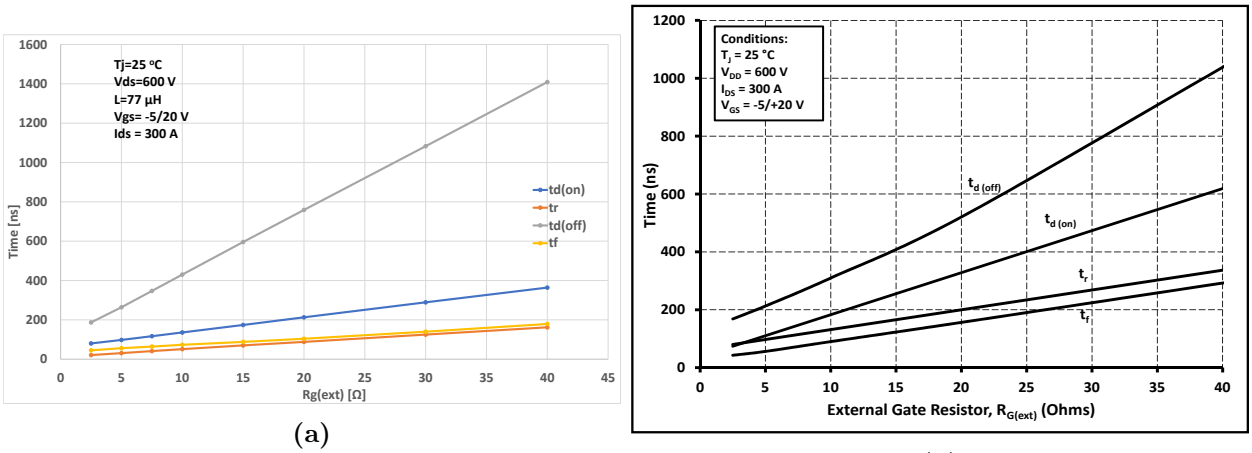
The switching performance has also been investigated by varying the external gate resistor $R_{g(ext)}$ between 2.5 Ω and 40 Ω. The simulation results and datasheet values are illustrated in Figure 5.13. It is clear that the switching losses increase with increasing gate resistance, and this is due to the switching transients slowing down as it takes more time to charge and discharge the MOSFET capacitances. Hence, there will be a larger overlap between the current and voltage during the switching transient and the losses will be larger. The simulated values are lower compared to the datasheet values and the sources for these differences were discussed in Section 5.3.3.



(a) **(b)**

Figure 5.13: (a) Simulated switching losses and (b) datasheet switching losses for different $R_{g(ext)}$ [13].

Secondly, the switching times are found as a function of $R_{g(ext)}$ and these results are shown in Figure 5.14. It shows the turn-on delay $t_{d(on)}$, turn-off delay $t_{d(off)}$, current rise time t_r and current fall time t_f. These are measured by using the definitions from Section 5.1. The switching times increase with larger $R_{g(ext)}$, and hence the switching transients are slowed down. This leads the higher switching losses which is also shown in Figure 5.13. Here as well, there is a large difference between the simulated values and datasheet. In addition to the previously mentioned reasons for differences between the simulations and datasheet, there might be differences in how the switching times are defined. That is, the definition of the switching times given in Section 5.1 might be different from the definitions Cree uses to measure the values given in the datasheet.



(a) **(b)**

Figure 5.14: (a) Simulated switching times and (b) datasheet switching times for different $R_{g(ext)}$ [13].

5.3.5 Current sharing capability of the module and oscillations

As the layout of module is very symmetrical, it is expected that the currents will be shared very evenly between the MOSFET dies. This is shown in Figure 5.15, where the currents going through lower MOSFET 1, 2 and 3 from a LTSpice simulation are shown. It is not necessary to plot the currents going through MOSFETs 4, 5 and 6, as they are pretty much a mirror image of the the three first dies.

MOSFET 2, that is the middle switch of each pad, conducts more current compared to the other two before the turn-off happens and that is due to lower inductance in the conduction path of the middle die on each pad, as shown in Figure 4.9. At 150 A, the difference is 1 A, and becomes more noticeable at higher drain currents. However, when the current is in steady-state, there will be a balancing effect between the MOSFETs in each switch and this might not be a big issue during operation. However, during the turn-on transient, there is a larger difference between the currents (6 A at $I_d = 150$ A), as there is a larger current that has to be shared due to reverse recovery of the SBD. The current through MOSFET 1 and 3 is almost identical, as they have approximately equal inductances in their paths.

Furthermore, in LTSpice the MOSFET models are identical, but in a real device there will be some mismatches between the dies for $R_{ds(on)}$, V_{th} and so on, which will lead to uneven current sharing during the transients and also steady state.

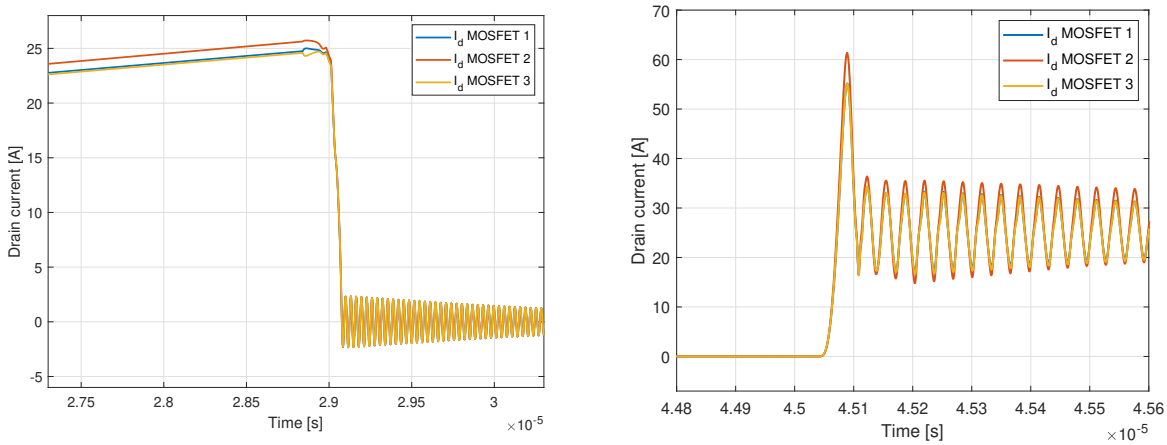
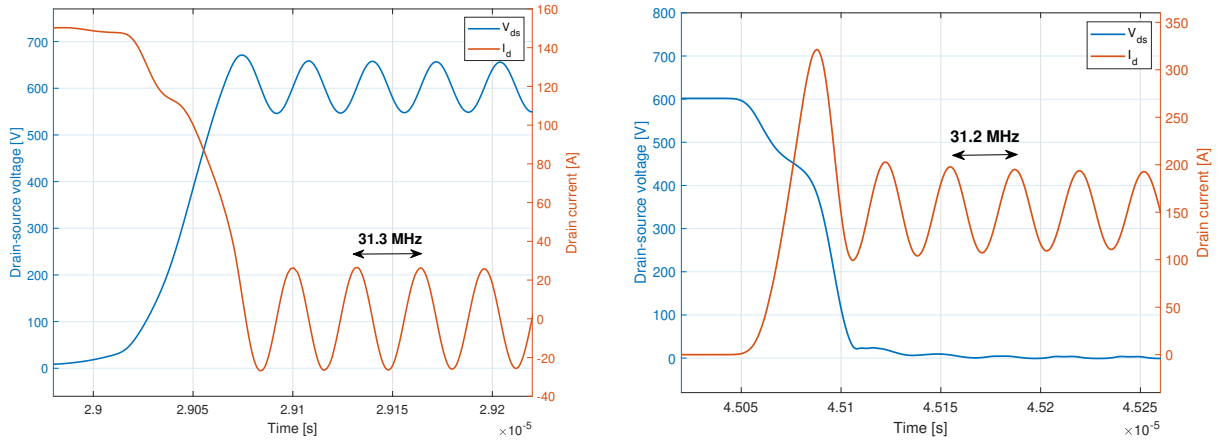


Figure 5.15: Current sharing between lower MOSFET dies on one pad for (a) turn-off and (b) turn-on. $V_{ds} = 600$ V, $I_d = 100$ A.

After finishing the turn-off and turn-on processes there is a lot ringing that appear in the voltage and current waveforms. These appear due to the very high derivatives in combination with parasitic capacitance and inductance present in the circuit. After the switch state transition is completed, there is still energy left stored in the C_{oss} of the switches and L_{loop}. This energy will continue to alternate between the parasitic components leading to underdamped ringing. After a while the current and voltage will approach steady-state due to the damping provided by $R_{ds(on)}$ and parasitic resistance in the layout.

The frequency of the ringing is measured as shown in Figure 5.16. At turn-on the load



(a) **(b)**

Figure 5.16: Measurement of (a) turn-off ringing frequency and (b) turn-on ringing frequency.

current commutate from the freewheeling SBDs in the upper switch to the lower switch (DUT). Once this process is completed, the C_{oss} of the DUT starts discharging and the voltage across it falls to the on-state voltage while the voltage across the upper diode/switch will rise to approximately the DC-link voltage. The energy discharged from the output capacitance will circulate in the LC-circuit formed by the parasitic commutation inductance L_{loop} and the output capacitance of the upper switch/diode. The same process will take place during the turn-off, as the upper switch/diode will discharge and the DUT voltage will rise to approximately DC-link voltage. Hence, the ringing frequency measured and shown in Figure 5.16 is close to equal for both turn-on and turn-off, since C_{oss} is equal for the DUT and upper switch/diode. The ringing frequency can be controlled by calculating the theoretical value using:

$$f_{ringing} = \frac{1}{2\pi\sqrt{L_{stray}C_{oss}}} \tag{5.3.1}$$

The C_{oss} of each switch is 2.57 nF at 600 V according to the datasheet [13] and the stray commutation inductance is 9.83 nH. This yields a ringing frequency of 31.7 MHz, which correspond very well with the simulation.

6 Investigation of the power terminal geometry for improved switching performance

Some adjustments can be made to the module so that the stray inductance can be reduced, which will lead to better switching performance. The power terminals contribute with the most stray inductance in the power loop, which can be seen from Figure 4.9. By changing their geometry the stray inductance of the module can be significantly reduced.

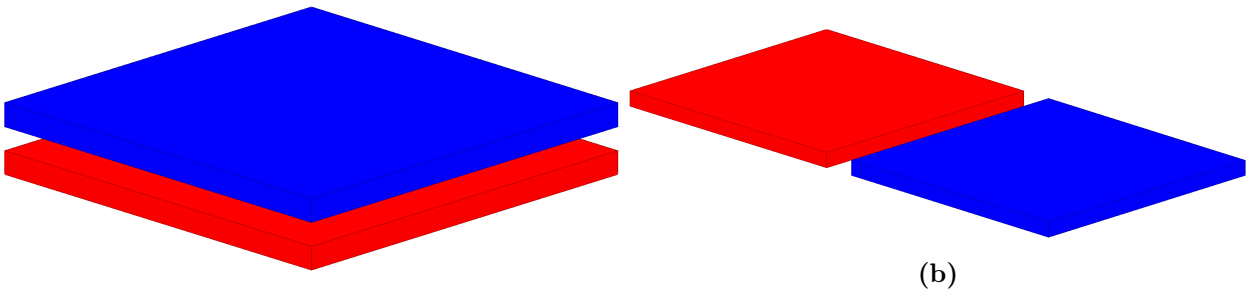
6.1 Busbar and terminal design

In literature several different bus bar designs have been developed, so that the impedance of the busbar can be reduced and the full potential of SiC can be extracted. Generally, when designing a busbar, the goal is to achieve the lowest busbar impedance Z [34]:

$$Z = \sqrt{\frac{L_{stray}}{C_{dis}}} \tag{6.1.1}$$

L_{stray} is the stray inductance and C_{dis} is the distributed capacitance of the busbar. Thus, the aim should be to decrease L_{stray} and increase C_{dis}.

Generally, there are two ways of arranging a pair of conductors to form a busbar. The first method is to vertically stack the conductors, so that they form a parallel plate and the second way is to place them side by side. Such layouts are called planar and coplanar plates and are illustrated in Figure 6.1.



(a) **(b)**

Figure 6.1: (a) Planar and (b) coplanar structures.

C_{dis} and L_{stray} are associated with the width w, length l and distance between the plates h (planar) and t (coplanar) [35]:

$$C_{dis} = \epsilon_0 \cdot \epsilon_r \cdot \frac{w \cdot l}{h} \tag{6.1.2}$$

$$L_{stray,planar} = \mu_0 \cdot \mu_r \cdot \frac{l \cdot h}{w} \tag{6.1.3}$$

$$L_{stray,coplanar} = \frac{\mu_0 \cdot \mu_r}{\pi} \cdot \cosh^{-1}\left(\frac{w+t}{w}\right) \tag{6.1.4}$$

ϵ_0, ϵ_r and μ_r are the permittivity of free space, relative permittivity and relative permeability respectively.

Both methods provide magnetic field cancelling, as the two conductors are in close proximity to one another with currents in reverse directions, and hence the effective L_{stray} is lower. However, the planar structure is much better at cancelling the fields, as there is substantially more overlap between the magnetic flux lines. This was shown in [34], where the termination of a capacitor was either coplanar and planar, and the planar termination gave a lower value of L_{stray}. More overlap in the magnetic flux lines will lead to larger mutual inductance or coupling between the elements, and if the current is carried in opposite direction the effective inductance can be given as:

$$L_{loop} = L_{11} + L_{22} - 2M_{12} \tag{6.1.5}$$

L_{11} and L_{22} are the self-inductances and M_{12} is the mutual inductance between the two elements. Thus by increasing M_{12}, L_{loop} can be decreased.

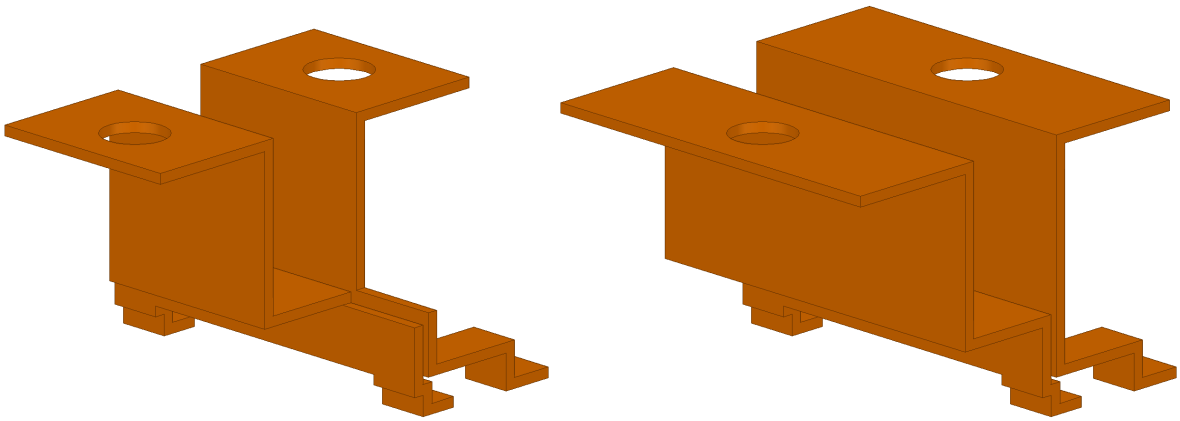
C_{dis} is due to the fact that two conductors with different voltage levels and in close proximity to one another will store charge in the space between them. This is especially noticeable in the planar structure, as it basically forms a parallel plate capacitor. An increased value of this capacitor will lead to lower busbar impedance, and hence it would be beneficial to make this capacitance as large as possible. This can be achieved by keeping the distance between the two conductors as low as possible and by using dielectric materials with high ϵ_r between the plates [34]. However, if the conductors are closely spaced they are also subjected a higher breakdown risk of the insulation. Also, a complete planar design can be difficult to realize in places where the terminations and clearances are required.

6.2 Improving the power terminal design

Some of the points presented in the previous section can be used to improve the inductive layout of the power module created in this thesis. Figure 4.6 and Figure 4.7 show that the positive and negative power terminals of the designed module are placed in an almost planar-like structure. However, some improvements can be made. The terminals can be made wider, as that will increase the cross section of the terminals, leading to lower L_{stray}. Furthermore, the positive terminal can also be made totally straight, so that there is no bend and that will result in more coupling between the terminals. This will also increase C_{dis} between the terminals.

The first modification to the terminals is shown in Figure 6.2b. The width of both positive and negative terminals is increased to 34.8 mm, and that is as wide that they can be due to the restrictions of space. The results of the parasitic extraction from Q3D Extractor are given in Table 6.1 for both the normal terminals and the widened version. The stray inductance decreases when the terminals are widened and the coupling coefficient becomes larger, which will result in lower effective L_{stray}. As the terminals are widened, C_{dis} increases

from 4.34 pF to 4.92 pF, which is not a very large increase. C_{dis} and the coupling coefficient are common for both terminals.



(a) **(b)**

Figure 6.2: Positive and negative power terminals with (a) normal layout and (b) width increased to 34.8 mm.

Table 6.1: Stray inductance, inductive coupling and capacitance for the designs in Figure 6.2.

Case	L_{dc} [nH]	L_{ac} [nH]	Coupling coeff.	C_{dis} [pF]
Normal terminals				
Positive	11.18	9.2	-0.565	4.34
Negative	10.84	8.97	-	-
Wide terminals				
Positive	8.32	6.88	-0.61	4.92
Negative	8.56	7.13	-	-

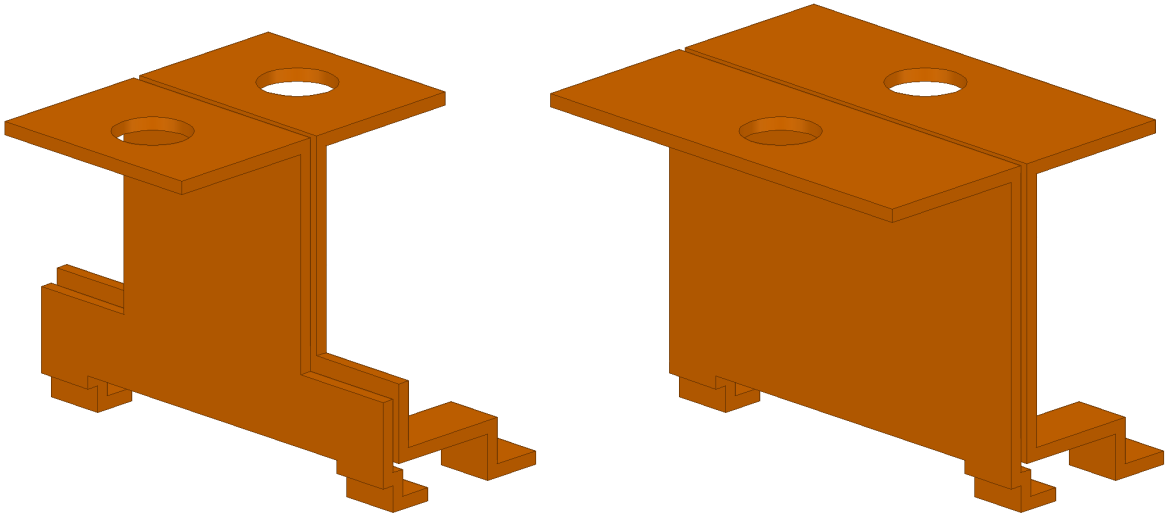
The second modification to the terminals is shown in Figure 6.3. Here the bend of the positive terminal is removed and it is made entirely straight. The results of the parasitic extraction from Q3D Extractor are given in Table 6.2 for both versions of the straight terminal. The inductance of the straight negative terminal remains unchanged from Table 6.1, as this terminal is not changed. However, there is a large decrease in L_{stray} of the positive terminal and coupling coefficient has increased significantly. The same goes for C_{dis}. In this 3D designed module the clearance between the terminals is very low, about 1 mm, while in reality the clearance will be larger, which would result in lower coupling coefficients and C_{dis}.

However, a clearance of 1 mm might be realistic if proper care is taken so that no flashover can occur. For instance an insulating dielectric material can be placed in between the terminals so that the breakdown voltage will increase. For instance Kapton material can be used. Kapton has a breakdown voltage of 5 kV/mil (197 kV/mm) [34] and could be a suitable candidate for this. However, placing sheets of dielectric material between

Table 6.2: Stray inductance, inductive coupling and capacitance for the designs in Figure 6.3.

Case	L_{dc} [nH]	L_{ac} [nH]	Coupling coeff.	C_{dis} [pF]
Straight terminals				
Positive	9.6	8.06	-0.834	8.51
Negative	10.87	8.97	-	-
Straight and wide terminals				
Positive	7.09	6.16	-0.831	12.83
Negative	8.56	7.13	-	-

the terminals might increase the risk for breakdown in some applications, for example in automotive converters, where there is a lot of vibrations which might tear on the insulation.



(a) **(b)**

Figure 6.3: Straight positive and negative terminals with (a) normal width and (b) width increased to 34.8 mm.

Table 6.3 gives the total power loop inductance for the entire module with the different terminal designs. Compared to the value of L_{loop} extracted from the normal 3D model of the physical module in Table 4.1 there is a reduction of about 50 % in L_{loop} if the design from Figure 6.3b would be implemented. However, there might be some reasons for not implementing such a design. There is a larger risk of short-circuiting the the power terminals as they are in such a close proximity to one another. Even with a dielectric between them, there will be a risk as it can deteriorate with time and subjection to vibrations. Furthermore, there is limited space in the module, so there might not be enough room to realize the wide design and the manufacturer may consider such a design unnecessary, as it is more costly and intense in fabrication.

Table 6.3: Total power loop inductance for the different terminal designs.

Case	L_{dc} [nH]	L_{ac} [nH]
Wide normal terminals	10.4	7.2
Straight terminals	7.6	4.3
Straight wide terminals	6.6	3.8

6.2.1 LTSpice simulations with improved power terminal design

The new designs are put into the previously used LTSpice model. Only the inductance of the positive and negative terminals is changed, as well as the coupling coefficient. The DPT were performed for a DC-link voltage of 600 V and the drain current is varied between 50 A and 400 A. The reduction of L_{stray} has the most significant impact on the turn-off waveforms, and some of those are shown in Figure 6.4. The overvoltage is reduced from 737 V to 700 V when the design with straight and wide terminals is used, and the oscillations are damped more quickly.

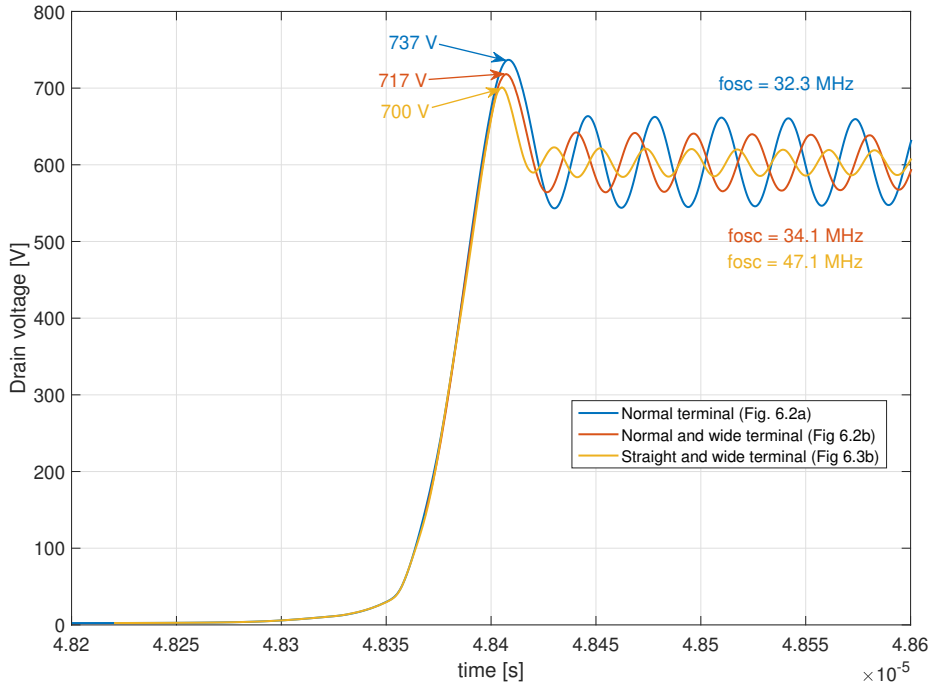


Figure 6.4: Turn-off voltage waveform for three terminal designs at V_{ds} =600 V and I_d =300 A.

A few selected results from the LTSpice analysis of the terminals in Figure 6.2 are given in Table 6.4. The overshoot voltage V_{oss} has been reduced with the new design, and due to

this the turn-off energy E_{off} has been decreased. E_{on} remains approximately the same, as the turn-on is not that affected by L_{stray}.

Table 6.4: Switching energy and overshoot voltage for different I_d for the terminal designs in Figure 6.2.

Case	E_{off} [mJ]	E_{on} [mJ]	V_{oss} [V]
Normal terminals			
100 A	0.89	2.46	42
300 A	4.06	5.59	137
400 A	6.24	7.41	165
Wide terminals			
100 A	0.87	2.46	32
300 A	3.89	5.60	117
400 A	5.93	7.37	141

The same simulations are done for the terminals in Figure 6.3 and the results are given in Table 6.5. The overshoot voltage is decreased even further with this terminal design and results in a decreased E_{off}. However, E_{on} seems to increase slightly, even though it should not be affected that much by L_{stray}. The reason for the increase might be that the switching energy was difficult to measure in the LTSpice due to more damped oscillations. However, it quite clear that the design with straight and wide terminals gives the best results, as it has the least overvoltage and hence reduced switching losses.

Table 6.5: Switching energy and overshoot voltage for different I_d for the terminal designs in Figure 6.3.

Case	E_{off} [mJ]	E_{on} [mJ]	V_{oss} [V]
Straight terminals			
100 A	0.87	2.53	30
300 A	3.73	5.76	111
400A	5.66	7.58	132
Straight and wide terminals			
100 A	0.86	2.53	28
300 A	3.68	5.77	100
400 A	5.51	7.61	121

7 | Conclusion and further work

This section will draw the main conclusions from the work done in this thesis and some suggestions for further study are presented.

7.1 Conclusion

In this thesis the geometry of a conventional SiC half-bridge 1200 V 300 A power module from Cree has been realized and simulated in FEM software and LTSpice.

The thermal analysis revealed that the layout of the bare MOSFET dies is not well fit for high temperature operation, as the dies in the lower switch position experience much higher junction temperatures due to them being to more tightly placed. The middle MOSFET on each pad does also experience elevated temperatures due to the thermal coupling to the dies on both sides, and is found to be the bottleneck for operation at higher temperatures as it limits the power module to 150 °C. Furthermore, it was found that the different methods of modelling the case boundary will affect the temperature distribution and makes the thermal analysis more challenging to do. Fixing the case to a given temperature is the easiest method for analyzing the thermal performance of the module, but does not represent a real cooling solution at all, since the temperature distribution over the case surface will be far from isothermal in reality and will affect the results significantly. Thus, the method that might represent the real case better is to model the case boundary with a *htc*, which has to be selected with the heatsink in mind.

The parasitic inductances were extracted in Q3D and it was found that the main power terminals contributed by more than 50 % to the total power loop inductance of the module. Furthermore, the simulations also showed large values of gate-loop inductance due to the long and slender gate-source traces.

These extracted values, together with stray resistances also extracted with Q3D, were incorporated into double-pulse test circuit in LTSpice. The simulated tests showed significant voltage overshoots and ringing due to the power loop inductance resonating with the output capacitance of the MOSFET and SBD capacitance. It was found that the simulated switching losses followed the same trend as the datasheet values, but with some discrepancies as the simulated model has its limitations in how the LTSpice models of the SiC MOSFETs and SBDs work and that the junction temperature was fixed.

The simulations showed that the module has good current sharing capability, as the parasitic inductances in each conduction path is close to equal. Only during the turn-on transients was there a noticeable larger difference due to the large reverse recovery current of the SBD superimposing itself on the load current.

Strip-line arrangement of the power terminals showed that the stray inductance of the power terminals can be reduced significantly, as the magnetic cancelling effects were taken advantage of to a larger degree and the width of the terminals was increased. The terminal design with straight and wide terminals showed the best performance, with a reduction in voltage overshoot from 137 V to 100 V at 150 A load current. Consequently, a reduction

in the turn-off energy was observed. However, this design may be the most difficult one to realize in a physical module due to space restriction and low margins when it comes to distance between the positive and negative terminals.

7.2 Suggestions for further work

The work in this thesis has shown that there is room for improvement in conventional bondwire power modules.

- The next step will be to continue with the work done in this thesis. It would be interesting to implement the new power terminal design in a real physical module to see the improvements through real experiments and how they compare with the simulation results.

- This thesis was for the most part concentrated on the parasitics in the power loop. However, extraction of the gate loop parasitics was done and it was shown that their values are quite high. Thus, it would be interesting to investigate their effect on the switching performance. The gate inductance of each die is uneven, and it may affect each die differently. More attention could also be paid to the gate driver and how to fine tune it for better switching performance.

- Diodeless operation of the module is also an interesting solution to investigate. The SBDs in the module could be removed and replaced entirely by the internal diodes of the SiC MOSFETs. This would possibly free up space on the DBC, making it possible to arrange the MOSFET dies differently for better performance. For instance the thermal performance could be improved as the space of the DBC could be utilized better. It would also be interesting to see how the internal MOSFET diode performs compared to the SBD.

- The thermal performance of the module could be investigated in ANSYS Icepak with a real heatsink. It would be interesting to see how this would compare to modelling the case surface with a fixed temperature or *htc*. In addition, it would be beneficial to include thermal properties of the materials as a function of temperature for more accurate results.

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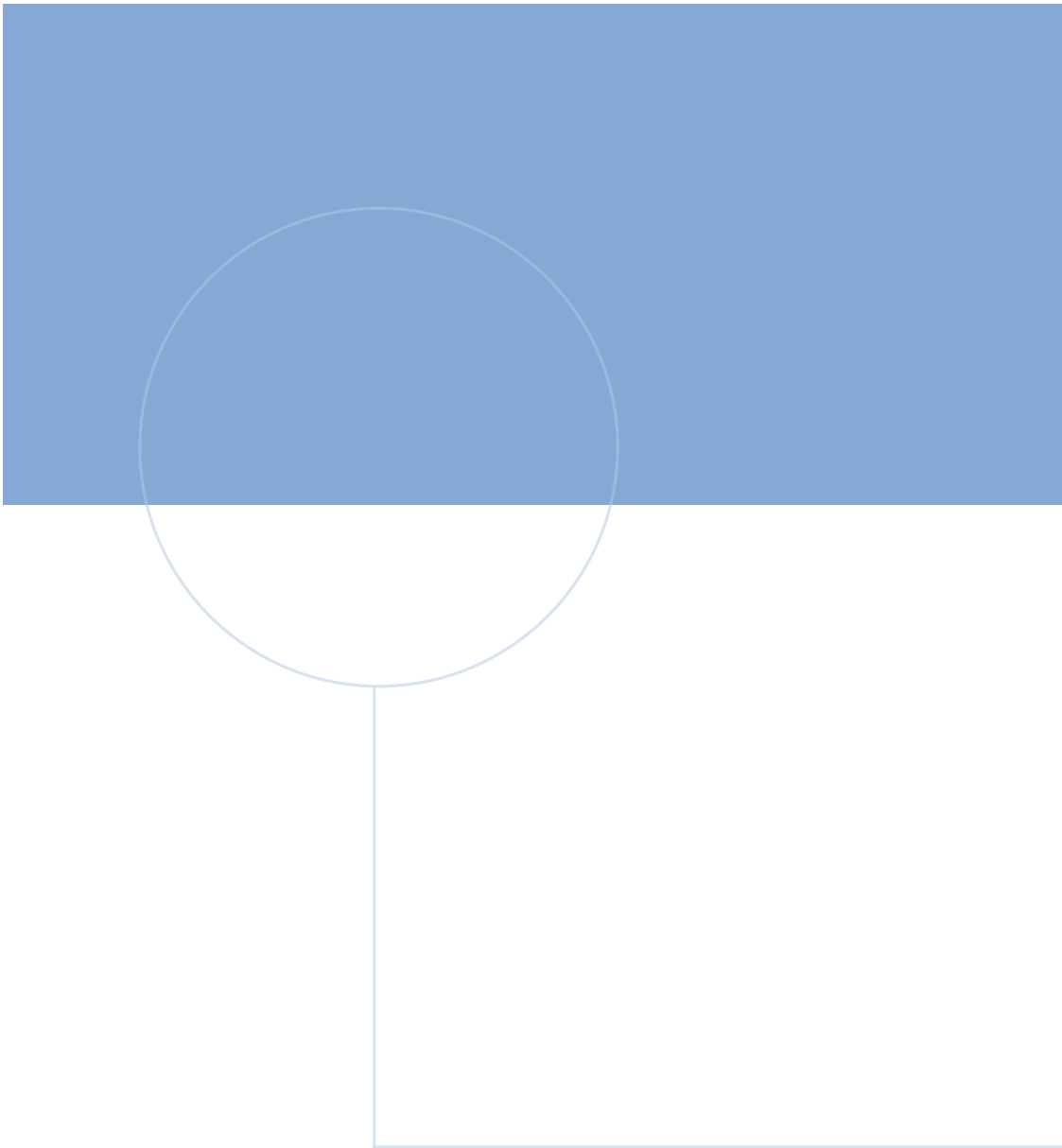

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