Master's thesis

NTNU
Norwegian University of Science and Technology
Faculty of Information Technology and Electrical Engineering
Department of Electric Power Engineering

Dan Godhei

Understanding the Subsynchronous Oscillation Occurring in Offshore Wind Farm Converters Connected via HVDC

Master's thesis in Electrical Power Engineering
Supervisor: Mohammad Amin
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Kunnskap for en bedre verden

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Summary

The need for renewable energy has lead to substantial investment in offshore wind energy technology. One technology considered to be a viable option for the future is high-voltage direct current (HVDC) transmission. HVDC transmission revolves around transmitting power as direct current(dc). Commercial wind turbines (WT) today generate alienating current(ac). To send ac power as dc power the current must first be converted from ac to dc. To convert the power from ac to dc a multi modular converter (MMC) can be used. One advantage of ac power is that the current-voltage(IV) can be changed with a transformer. Transformers are connected between the MMC and the WTs to reduce the voltage across the WT terminal. To control the power produced by a WT can be a complicated task. To simplify the power production, the WT can be represented as a constant dc source. To control how much power the WT delivers to the grid, a 2-level voltage source converter (VSC) is connected to the dc source. The VSC is connected to the WT terminal. Dc power from the turbine is now sent through the converter, where it is converted from dc to ac. The ac power is sent through transformers where the IV ratio changes. The ac power is then converted to dc in the MMC and delivered to the grid. This is a master thesis that will describe this operation in detail and show how the power quality varies when power delivered by the WT to the grid change.

In this thesis show how that a VSC converter can be designed to control the power output and synchronise to the grid by using a PLL. By analyzing the VSC in a time domain, it is observed harmonic distortion (HD) in the controller, when delivering 50MW and 10MW to the grid. It is also found that the magnitude of these oscillation are not dependent on the power output as they remain almost the same for 50MW and 10MW. The thesis shows a way to control an MMC with and without circulating current control. Tests performed in both frequency and time domain show that by excluding internal dynamics by removing the circulating current control is the controller unable to operate in steady state for 50MW. By considering internal dynamics with a circulating current controller is the MMC capable of setting the ac voltage at the WT terminal. This conclusion is drawn after testing the MMC for 50MW and 10MW, connected and disconnected to the VSC. Also, the MMC experience HD which influences stability. The HDs can be located when the MMC connected and disconnected to the VSC. By testing the MMC without connecting it to the VSC, it is proven that some of the HD originates at either the MMC control system or from the switching components. When the MMC and VSC become interconnected, the THD for the whole system increase, it is therefore likely that the controllers influence each other and make one another more unstable. Passive components in the transformer and the transmission line can be designed to filter out some HDs.

Preface

This is a master thesis written by Dan Godhei. The thesis is submitted to the Department of Electrical Power Engineering at the Norwegian University of Science and Technology. It is the final requirement of a two-year master program in power electronics. Associate Professor Mohammad Amin has contributed with his time and knowledge and is the supervisor for this project. To test an analytical model in a close to realistic environment has Matlab Simulink been used to build and simulate the model. The master project started in January of 2020 and ended on June 10. 2020. A prerequisite study on VSC in HVDC systems were conducted in the fall of 2019 as groundwork for this thesis.

Acknowledgements

You should never take for granted the time and effort other people spend on helping you. From the fall of 2019 to the summer of 2020, Mohammad Amin has shared with me his knowledge, been patient, and kind. I would, therefore, sincerely thank him for his contribution to this thesis. He has pushed me to set higher standards for myself and spent numerous hours in meeting in person and on Skype. He has been an excellent representative of the higher academic community, and I would not hesitate to say yes if I get an opportunity to work with him again.

Dan Godhei
Trondheim, 10.06.2020

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Chapter 1

Introduction

This chapter will present specific background knowledge for this thesis, like Per Unit system, Phase-Phase to Phase-Ground transformation, harmonics and general stability. It also specify that renewable energy investment has made wind energy technology popular.

1.1 Background

Significant investments in the renewable energy sector have led to rapid growth of technology. [1] As much of the potential land-based energy sources are either being used, or in places already inhabited by people, many researchers look to the ocean for answers. Installations located on the open sea are often far away from where the power is consumed. Additionally are the demand for power increasing as installations are becoming more abundant. Longer distances and more power being transferred are two main reasons that power equipment efficiency is essential for the future. [1]

One way of transferring ac power very long distances is to send it as High Voltage DC (HVDC) power. The advantage of DC power is that it does not produce reactive power, it does not require three phases of cable, and it does not need to be synchronized to the grid. [2] This lowers the cost and material usage and is why HVDC is a viable option, and is why this thesis will present the possibility of using HVDC to transfer power.

According to [3] wind energy provides 4.8% of the global power production. In 2018, wind energy production grew by 10%, reaching a capacity of 564 GW. In Denmark, more than 46% of power produced come from the wind energy sector. In Europe, 5047 offshore wind turbines (WT) are connected to the grid across 12 countries. [4] Of these 5047, 502 of them were installed from 2018 to 2019. Norway alone were responsible for installing approximately 10 GW capacity for this period.[4] The market is clearly expanding, and offshore WTs are one way of extracting these marine energy resources. This is why this report will take a look at an offshore wind farm (WF).

1.2 Per Unit System

There are a lot of values and notations when dealing with complex power systems. Just by looking at a graph, can it be challenging to compare International system of units (SI) units to the reference value. To simplify the analysis of power systems, one can create a set of scalar parameters which are connected and can be used when presenting results. These parameters are called base values. Typical base parameters are apparent power S_b, peak phase to ground voltage V_b, peak current I_b and impedance Z_b, where the subscript b indicates that it is a base parameter. What value these parameters have is up to the person performing calculations. The base values are reliant on each other, meaning that if two parameters are decided, then the rest of the parameters are set. It can be recommended to set the base values equal to rated values and first to decide apparent power and voltage is most common in literature. The relationship between the mentioned ac base values are

$$I_b = \frac{2}{3}\frac{S_b}{V_b} \tag{1.1}$$

$$Z_b = \frac{V_b}{I_b} \tag{1.2}$$

Other base parameters often presented in literature are angular frequency ω_b, resistance R_b, inductance L_b and capacitance C_b, which can be calculated accordingly

$$Z_b = R_b = \omega_b L_b = \frac{1}{\omega_b C_b} \tag{1.3}$$

where angular frequency is independent on other values. When an impedance Z is presented in its original SI unit, one can use the base value Z_b to generate the result in per unit Z_{pu} like this

$$Z_{pu} = \frac{Z}{Z_b} \tag{1.4}$$

A per unit value, in this thesis, is presented with the unit ”pu”. Dc base calculations are presented in [5]. Voltage is often presented in literature as the RMS line to line voltage V_{LL} and can be transferred to its phase to ground peak base value as follows

$$V_b = \sqrt{\frac{2}{3}} V_{LL} \tag{1.5}$$

1.3 Phase-Phase to Phase-Ground

When presenting a result most values are presented in per unit unless SI units will help illustrate a point. Per unit is used as it makes it is easier for the reader to compare the result to reference values. Furthermore, it is simpler for someone else to recreate the experiment and compare their results to this thesis. This system operates with two sets of base values, WF Inverter base and HVDC base, separated by two transformers. The Simulink model is built as an isolated network. This will prevent the possibility of measuring from phase to

ground. Voltages, therefore, have to be measured between phases, so-called phase-phase. Phase-phase voltage can be transformed into phase-ground accordingly [6]

$$V_{an} = \frac{V_{AB} - V_{CA}}{3} \tag{1.6}$$

$$V_{bn} = \frac{V_{BC} - V_{AB}}{3} \tag{1.7}$$

$$V_{cn} = \frac{V_{CA} - V_{BC}}{3} \tag{1.8}$$

Where V_{an}, V_{bn} and V_{cn} are the phase-ground voltage and V_{AB}, V_{BC} and V_{CA} are the phase-phase voltages.

1.4 Harmonics

Ac voltage and current waveforms consist of harmonics, which are those frequencies which are integer multiples of a fundamental grid frequency. [7] Harmonic distortion is the effect non-sinusoidal fundamental or higher frequency current and voltage waveforms have on the fundamental sinusoidal waveform, caused by electrical equipment or mechanical faults. In power electronics are common sources of harmonic distortion, according to [7], inverters, industrial motor drives, light dimmers and personal computers. Also, insulation failure may cause overheating in transformers and motor drives which are a common cause of harmonic distortion. Voltage and current can have waveforms with many frequencies. When found, the magnitude of these other frequencies can be compared to the magnitude of the fundamental frequency. This will allow us to represent harmonic distortion as percent, where 100% are the energy of the fundamental frequency. [8]

$$HD_n = \frac{|V_n|}{|V_1|} \tag{1.9}$$

where n is the harmonic integer, HD_n is the nth harmonic distortion in percent, $|V_1|$ is the fundamental frequency voltage magnitude and $|V_n|$ in the nth harmonic voltage magnitude. Another common way of expressing harmonic distortion in literature [7], is to present the sum of all harmonic distortion as total harmonic distortion (THD). A high total harmonic distortion is bad. A popular way of calculating THD is to use Fast Fourier transform (FFT) analysis. Fourier analysis makes it possible to extract each frequency waveform component. These frequency components can be expressed as sine and cosine waveforms.

$$v(t) = \frac{a_0}{2} + \sum_{n=1}^{\infty} \left(a_n cos \frac{n\pi t}{F} + b_n sin \frac{n\pi t}{F} \right) \tag{1.10}$$

where v(t) is the voltage waveform, n = 1 is as that is the fundamental frequency component, F is a half period of the fundamental frequency and a_n and b_n are

$$a_n = \frac{1}{F} \int_0^{2F} v(t) cos \frac{n\pi t}{F} dt \tag{1.11}$$

$$b_n = \frac{1}{F}\int_0^{2F} v(t) sin\frac{n\pi t}{F} dt \tag{1.12}$$

If it is assumed that the ac voltage does not contain a dc component, then a_0 = 0. 1.1 show an arbitrary harmonic distortion. There it can be seen the first order harmonic is a lot higher compared to the other harmonics. It is also clear that odd harmonics, also called third order harmonics, often are higher than even harmonics. The figure shows that as the harmonic number increase, the magnitude of the frequency component decreases. This can be seen mathematically performing the integration in 1.11 and 1.12, which will result in the whole term being divided by the frequency number term n and is why lower order harmonics are more impactful than high order harmonics. This can be described physically with ohm's law for reactance X

$$X = 2\pi f L \tag{1.13}$$

where X is resistance, f is frequency and L is inductance. As reactance changes proportional to frequency, higher frequencies will have a higher reactance component, which will give a lower magnitude.

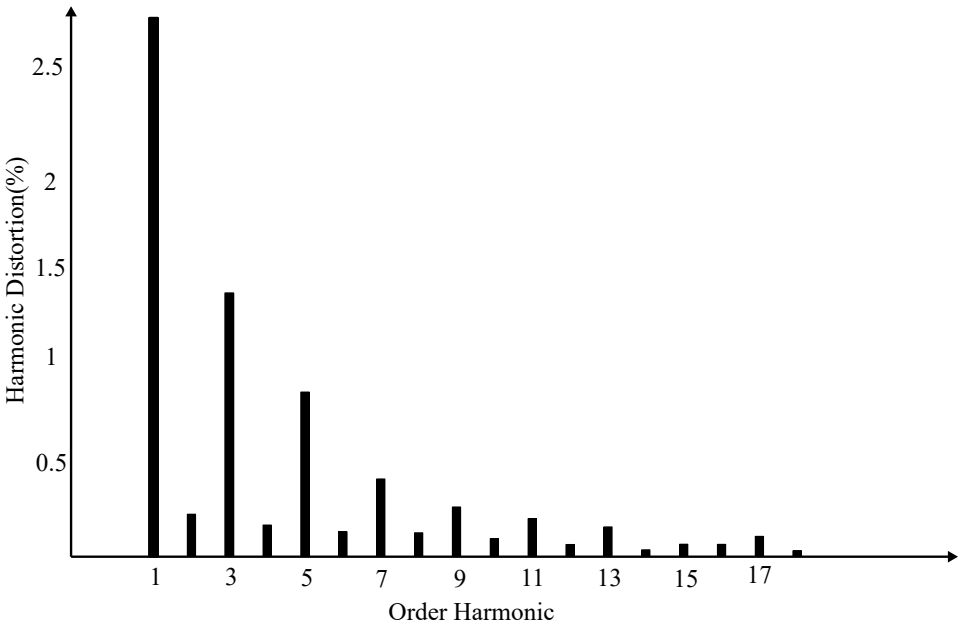


Figure 1.1: Arbitrary harmonic distortion

1.5 Filters

All ac voltages and currents contain some sort of harmonic distortion. Therefore, filters are regularly used to reduce these harmonics and make waveforms more sinusoidal. An ac

filter consists of impedances in series and parallel. A good filter will reduce higher order frequency components without influencing the fundamental frequency. 1.2 show a typical filter for reducing harmonics in an ac circuit.

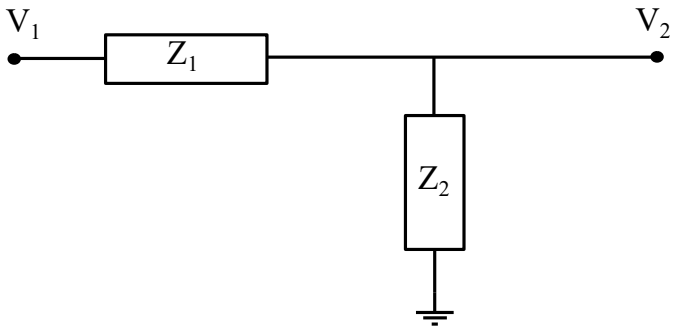


Figure 1.2: Ac filter where Z_1 and Z_2 are impedances

The filter capacitance and inductance directly influence what type of harmonics the filter is going to reduce. According to [7] are higher frequencies filtered with smaller components. High switching frequencies are better for system stability for systems controlled by transistors. This is because high switching reduces impactful low order harmonics, but increases high order harmonics. This means that by carefully choosing components, switching frequency can be used to remove lower harmonics, and filters can be implemented to remover higher ones. Filter components should not be too large as Ohm's law state that higher impedance results in higher losses P.

$$P = IZ^2 \tag{1.14}$$

where I is current.

1.6 General Stability

According to [9] can a system either be asymptotically stable, stable or unstable. Figure 1.3 illustrate the difference between these terms. x_o is the condition where the system starts. x_1 is the equilibrium point where the system will remain constant if not affected by a disturbance, x=constant gives dx/dt=0.

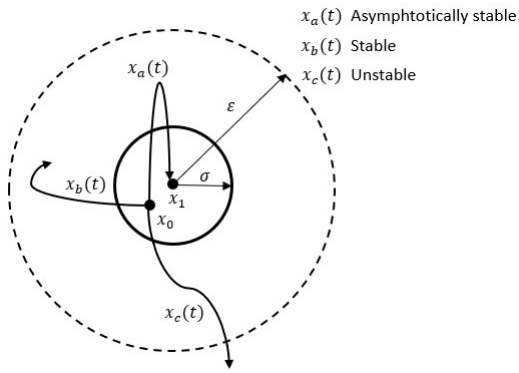


Figure 1.3: Definition of system that is asymptotically stable, stable and unstable

If the system over time ends up reaching the equilibrium point, like x_a in figure 1.3, the system is defined as Asymptotically stable.

$$\lim_{t\to\infty} x_a(t) = x_1 \tag{1.15}$$

If the system over time does not leave the area defined by the number ε, like x_b in figure 1.3, the system is considered stable.

$$\lim_{t\to\infty} x_b(t) < \varepsilon \tag{1.16}$$

If the system, over time, does leave the area defined by the number ε, like x_c in figure 1.3, the system can be considered unstable

$$\lim_{t\to\infty} x_c(t) > \varepsilon \tag{1.17}$$

1.7 State Space Representation

In [9] a *system* is defined as *"a set of physical elements acting together and realizing a common goal"*. These physical elements are all components necessary to predict how a system will react. To make these predictions we need, input variables, representing the force acting on the system, output variables, representing the output from the system and state variables, describing what conditions the system is operating under. State variables will have to be linearly independent, meaning they can not be a linear combination of another state variable[10]. These system states may be static, i.e. time-invariant, x_1, or dynamic i.e. time-dependent, $x_1(t)$ [9]. The input, output and states are what makes up the nonlinear system

$$\dot{x} = F(x, u) \tag{1.18}$$

$$\dot{y} = G(x, u) \tag{1.19}$$

Where $\dot{x}$ is the state equation, $\dot{y}$ is the output equation, F(x,u) and G(x,u) are vectors of a nonlinear equations. For a linear system, the state and output equations will be as follows

$$\dot{x} = Ax + Bu \tag{1.20}$$

$$\dot{y} = Cx + Du \tag{1.21}$$

Where A, B, C and D are matrices derived by derivating F and G with respect to x and u. In other words, 1.18 and 1.19 can be represented as linear equations by approximation [9]

$$\Delta\dot{x} = A\Delta x + B\Delta u \tag{1.22}$$

$$\Delta\dot{y} = C\Delta x + D\Delta u \tag{1.23}$$

For a system to be linear, it has to deliver within the constraints of superposition and homogeneity. Superposition means that a change in input, u, will result in the same change for the output, y. I.e., is u increased by 10 then y is increased by 10. Homogeneity means that if the input is multiplied by a scalar, the output will yield a response multiplied by the same scalar. Some systems are linear at a specific range, as an electronic amplifier, but will become nonlinear at very high voltage inputs due to saturation. Other systems, like an electrical motor, will have a dead zone, where it does not start to accelerate due to friction, even though it is supplied by a voltage source. [10] Linearization is necessary to study the stability of a dynamic system for small signal stability purposes.

Systems can be affected by external forces, called disturbances (z(t)), which can make a stable system unstable. A representation of a standard feedback system is illustrated in figure1.4

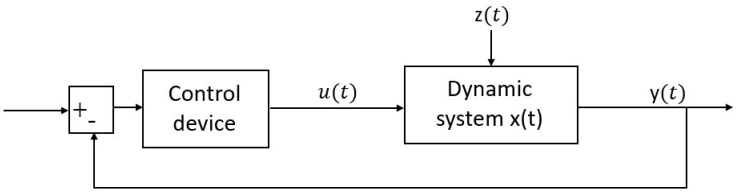


Figure 1.4: Feedback control system with disturbance z(t)

1.8 Impedance Modeling

Ohm's law specifies that some components, like a purely resistive element, depend only on the amount of current I flowing through it, to decide what the losses R of the resistor will be.

$$R = UI \tag{1.24}$$

Where U is voltage. While other components, like inductors and capacitors, are influenced by the frequency of the current to decide on how well the component conducts current.

$$X = wL \tag{1.25}$$

$$X = \frac{1}{wC} \tag{1.26}$$

Where X is the reactance, ω is the frequency times 2π, L is the inductance and C is the capacitance. Losses are not the only parameter that are influenced by the frequency of a circuit. When studying the impedance Z of the system, where an imaginary j component is included, it is possible to tell the phase shift ϕ of the current relative to the voltage.

$$I\angle\phi = \frac{U\angle 0}{Z} \tag{1.27}$$

$$Z = R + j\omega L + \frac{1}{j\omega C} \tag{1.28}$$

By testing a system for a broad frequency specter, it will be possible to say how much frequency influences loss and phase shift. Table 1.1 shows how the impedance provided by a resistor, inductor and capacitor change as a function of frequency. For a very high frequency, an inductor operates as an open circuit and a capacitor as a short circuit. For low frequencies, as for example dc, an inductor will operate as a short and a capacitor as an open circuit.

Table 1.1: How impedance change for a passive component as a function of frequency

	Zero freq.	Low freq.	High freq.	Infinity freq.
Resistance	R	R	R	R
Inductance	Zero	Low	High	Infinity
Capacitance	Infinity	High	Low	Zero

1.9 Nyquist Stability Criterion

A closed loop system in Laplace domain can be represented accordingly

$$L_N(s) = \frac{Y_N(s)}{U_N(s)} = \frac{G_N(s)}{1 + G_N(s)H_N(s)} \tag{1.29}$$

where L_N is the transfer function, Y_N is the output, U_N is the input, G_N is the system being controlled and H_N is the feedback function. This system is stable if the roots of the denominator lie in the left-hand side plane, in the s-domain, as this would prevent zero division. But to find all the roots of a transfer function can be time consuming work. Therefore there are alternative ways to evaluate stability that do not require to find all roots. One way to study stability is to evaluate the Nyquist plot. The Nyquist plot is a contour C_N, which encircles all of the right half plane in the s-domain. All zeros Z_N and poles P_N of the function $G_N(s)H_N(s)$ in the right half side are now encircled. While moving along the contour C_N, one can calculate the magnitude and angle from where you are on the contour to each pole and zero. The sum of magnitude and angle, where zeros are negative and poles are positive, generates a new contour in the ω-plane. The number of times this new contour for $G_N(j\omega)H_N(j\omega)$ encircles the critical point (-1 + j0) in the

clockwise direction is given by M_N, which is equal to Z_N - P_N. The system is stable if the number of zeros in the right half plane is equal to zero and if M encircles the critical point the same number of times in the counter clockwise directions as there are poles in the right half plane. [11], [12], [13]

The Nyquist plot can also be used to evaluate stability margins of the system. 1.5 show a figure of a Nyquist diagram. The point where the contour crosses the real axis is called the Phase crossover. The distance from the Phase crossover to the critical point is the gain margin, which is how much the system can increase in magnitude before it becomes unstable. The point where the contour crosses the unit circle is called the Gain crossover. The angle of the line from origo to the Gain crossover is called Phase margin, which is how much the system can be shifted before it reaches the critical point. If the contour does not cross the real axis or the unity circle, gain margin and phase margin are infinite. [13]

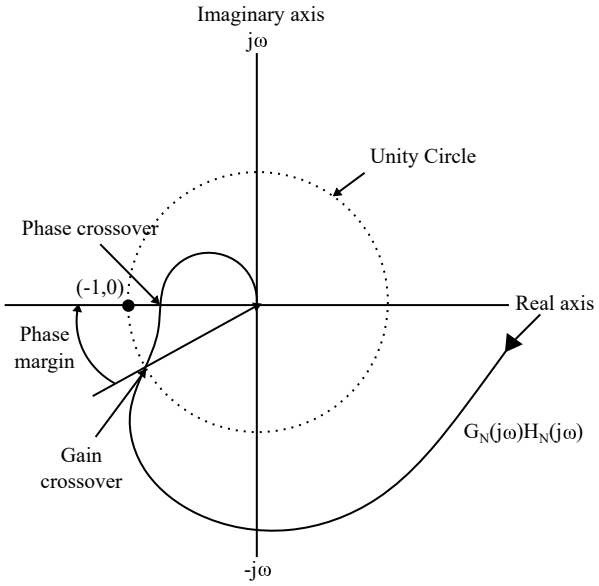


Figure 1.5: Nyquist diagram

Chapter 2

Wind Energy Conversion System

This chapter will describe the operation principle and control technique of a WF Inverter. The inverter is controlled with a current controller and a PLL. This chapter also include parameters that can be used to design a 2-level VSC and the frequency response for a control system with those parameters.

2.1 show a WECS with both rectifier and inverter present. To simplify this system the power produced by the WF and converted in the rectifier is represented by the voltage V_{dc} across the capacitor.

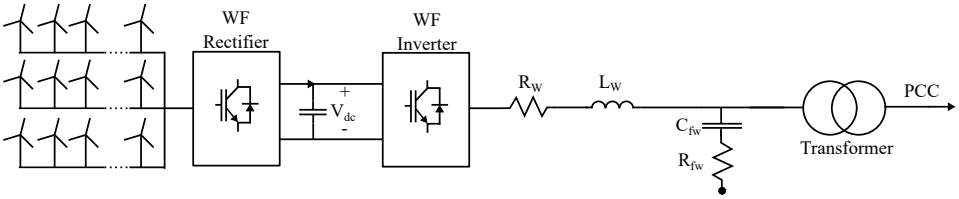


Figure 2.1: Wind energy conversion system

2.1 Voltage Source Converter Theory

A power converter is a device that converts power from dc to ac or ac to dc. A converter consists of transistors which are controlled to generate desired voltage and current waveforms. [14] VSCs are very common for high power systems as dc power does not produce the reactive power when transferred over long distances, contrary to ac power, according to [15]. Another reason for VSCs popularity is their outstanding performance and their ability to control real and reactive power, ac and dc voltage, as well as current.[1] [16] One drawback of VSCs are that they are very vulnerable to dc faults. Faults which can produce over currents many times the rated current to flow across the transistors.[17] A standard two-level voltage source converter is illustrated in figure 2.2.

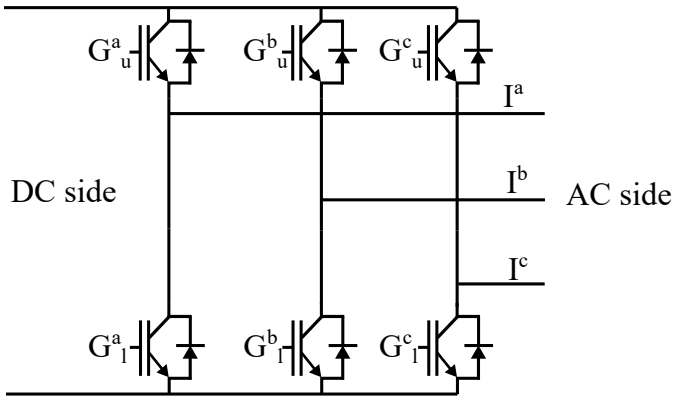


Figure 2.2: Two-level voltage source converter

As can be seen on 2.2, are each transistor in parallel with a diode. This is a bypass diode, and it is there to lead overcurrents past the switch to prevent the switch from getting destroyed. A control system sends a six pulse binary signal to the transistor gates, which controls if the switch conduct or blocks current. Later on, this thesis will explain how to generate and control this type of signal. Two popular choices as transistors are the Isolated gate bipolar transistor and Metal Oxide Semiconductor Field Effect Transistor, or IGBT and MOSFET as they are commonly known. [18] MOSFETS are generally designed for faster switching and IGBT for higher voltage ratings. [18]

2.1.1 Voltage Source Converter System Equation

To decide on the parameter values for the VSC is it necessary to know the voltage across the converter. Kirchhoff's current law say that the current from the dc side is equal to the sum of the currents on the ac side. The full equivalent circuit for the VSC connected to a voltage source on the ac side is presented in 2.3.

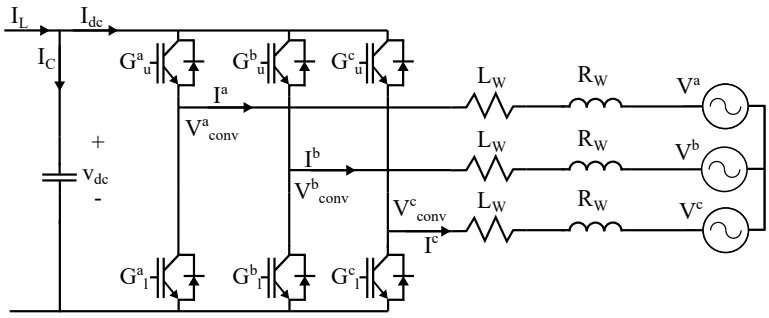


Figure 2.3: Two-level voltage source converter connected between an ac and dc grid.

where V^k_{conv} is the voltage on the ac side of the converter, superscript k indicates the phases (k = a, b and c), R_W and L_W are the line resistance and inductance and V^k are the

grid voltage. This is expressed in the following equation where the voltage drop across the passive components are impedance times current I^k

$$V^k = R_W I^k + L_W \frac{d}{dt} I^k + V^k_{conv} \tag{2.1}$$

This equation is used to control the VSC. But when a controller is implemented, the controller often takes values in a rotating reference frame as input variables. [1] [19] Variables expressed in the rotating reference frame is noted with d and q superscript. The process of transforming variables from synchronous to rotating reference frame is called *Park's transformation*, and is presented in 2.2. [20]

$$\begin{bmatrix} x^d \\ x^q \end{bmatrix} = \frac{2}{3} \begin{bmatrix} sin(\theta_t) & sin(\theta_t - \frac{2\pi}{3}) & sin(\theta_t - \frac{4\pi}{3}) \\ cos(\theta_t) & cos(\theta_t - \frac{2\pi}{3}) & cos(\theta_t - \frac{4\pi}{3}) \end{bmatrix} \begin{bmatrix} x^a \\ x^b \\ x^c \end{bmatrix} \tag{2.2}$$

where *x* represent the parameter which goes through the transformation, and θ_t is the angle of the rotating reference frame. Why it becomes beneficial to express values in this form will be described at a later stage. When 2.1 is represented in a dq frame, the derivative term for the voltage drop across the inductor will make for an additional term, due to the chain rule.[21]

$$\begin{bmatrix} V^d \\ V^q \end{bmatrix} = R_W \begin{bmatrix} I^d \\ I^q \end{bmatrix} + L_W \frac{d}{dt} \begin{bmatrix} I^d \\ I^q \end{bmatrix} + L \begin{bmatrix} 0 & -\omega \\ \omega & 0 \end{bmatrix} \begin{bmatrix} I^d \\ I^q \end{bmatrix} + \begin{bmatrix} V^d_{conv} \\ V^q_{conv} \end{bmatrix} \tag{2.3}$$

A step by step calculation of how this additional term is included is presented in Appendix.

2.2 Voltage Source Converter Control

A typical way to control a VSC is with a DC voltage controller, a current controller and a phase locked loop (PLL) control system. [1] How this control can be implemented is illustrated in 2.4. In addition to the control system, the model contains an LC filter with an inductance L_w and capacitance C_{fw}. The inductive and capacitive components both contain some parasitic resistive elements R_w and R_{fw}, respectively. There is also a transformer connected to the inverter side. The inverter delivers current to the low voltage side and the transformer steps up the voltage which is sent to the grid. The voltage and current measurements are taken after the inductor, to let the inductor straighten out the converter voltage curve. Both the voltage and the current are sent to a component that transfers the three-phase signals in a stationary reference frame, into a two-phase signal in a rotating reference frame. Subsequently, the voltage signal is sent to the PLL control system to generate a signal synchronized to the grid voltage signal. This signal is used to perform dq transformation of the voltage and current vectors. The dq transformed current and voltage signal is then sent into the current controller to generate a converter voltage signal, which will be explained more in the next subsection. The dc voltage controller controls the voltage across the dc side capacitor. To simplify the control system, dc voltage control will not be included, and the dc voltage is represented as a constant dc voltage source.

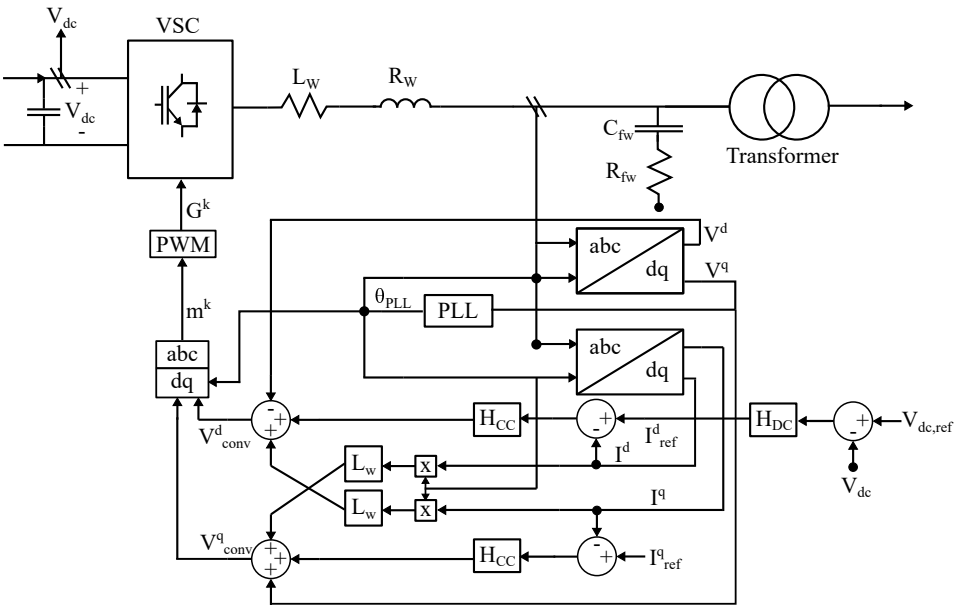


Figure 2.4: Wind energy conversion system with current controller and PLL

2.2.1 Current Controller

Current controller is a technology for controlling VSC and is very common. [1], [22]-[23] The controller design used in this paper is presented by M.Amin in [1]. This controller measures the input current and compares it to a reference signal, which is used to decide on what voltage the converter should produce. By looking closely at 2.1 it becomes clear that if the grid voltage and passive components remain constant, the current delivered from the converter to the grid is only dependent on the converter voltage.

Figure 2.5 shows what operations the current signal is sent through to generate the current reference signal. This block diagram takes in dq reference signals. In steady state dq signals are constant, which is beneficial for PI controllers. [24]

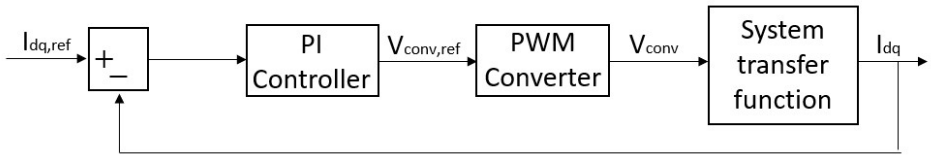


Figure 2.5: Current controller control system with Pules width modulator

2.2.2 PI Controller

The current and voltage signals are sent into the current controller after transformation from abc to dq. There the dq current I^{dq} are compared to the current reference values

I_{ref}^{dq} to find a current error. This error signal is sent through a PI controller block with proportional and integral parameters $K_{p,cc}$ and $K_{i,cc}$, respectively. A third parameter, $T_{i,cc}$ is the time constant of the PI controller, and is calculated accordingly, $T_{i,cc}$ = $K_{p,cc}/K_{i,cc}$. The transfer function of the PI controller is

$$H_{cc}(s) = K_{p,cc} + \frac{K_{i,cc}}{s} = K_{p,cc}\frac{1 + T_{i,cc}s}{T_{i,cc}s} \tag{2.4}$$

The output voltage $V_{conv}^{\prime dq}$ of the PI controller then becomes

$$V_{conv}^{\prime} = (I_{ref}^{dq} - I^{dq})(K_{p,cc} + \frac{K_{i,cc}}{s}) \tag{2.5}$$

2.2.3 PWM

As can be seen on 2.5 is the converter voltage marked with an apostrophe then put through a pulse width modulator(PWM). This is a triangular wave modulator, which compares the voltage waveform to a three-phase triangular signal. This is a popular method for generating bipolar signals for many types of switching devices.[25] The output of the modulator is the converter signal. The PWM can be expressed as a time delay. [26]

$$V_{conv}^{dq} = V_{conv}^{\prime dq}\frac{1}{1 + sT_a} \tag{2.6}$$

Where T_a is average time delay of the converter

$$Ta = \frac{T_{sw}}{2} = \frac{1}{2f_{sw}} \tag{2.7}$$

Where T_{sw} is the switching time in seconds and f_{sw} is the switching frequency in hertz.

2.2.4 System Transfer Function

The purpose of the VSC current controller is to control the output current of the controller. This is done by controlling the converter voltage, which is explained in 2.1. To simplify the controller, the waveforms are converted to a synchronous reference frame. Dq transformation presented in 2.2 introduces a cross-coupling term, $\omega l I^{dq}$ calculated in Appendix. This cross-coupling term can be compensated for by introducing a feed forward term. This will allow for independent dq control. [5]

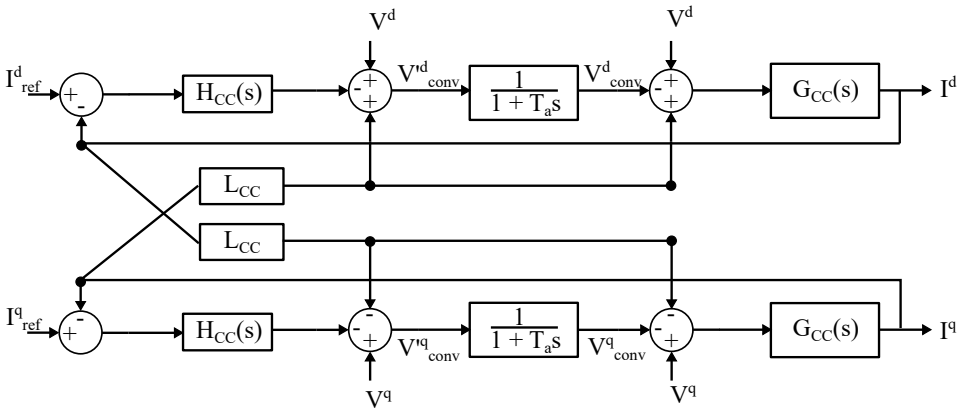


Figure 2.6: How to exterminate the cross coupling terms for the current controller

Where L_{CC} is the cross coupling term $\omega_g L_W$, and G_{CC} is the system transfer function

$$G_{CC} = \frac{1}{R_W} \frac{1}{1 + s\tau} \tag{2.8}$$

where τ is defined as inductance over resistance $\frac{L_W}{R_W}$.

2.2.5 Phase Locked Loop

The technique known as phase locked loop was first presented by Appleton in 1923. [27] But was not wildly used in the industry before the 1970s, due to difficulty when implementing it into real systems. At that time, it was first introduced by control engineers to control synchronous motors and has been used ever since. [28] The purpose of a PLL is to make one signal trace another. A PLL makes it possible to generate an output signal which contains the same phase angle and frequency as a desirable reference signal. The general requirements for a standard PLL are, according to [28] and [29], a phase detector, loop filter and a voltage control oscillator. The phase detector compares each phase of the measured input signal. Then generates an error signal which the voltage control oscillator uses to make the output frequency equal to the input frequency. PLLs have three operating states, frequency running, capture and locked state, which are explained in [29]. PLLs operate in a feedback loop to reduce error and be able to change in case the system frequency should change. [30]

The PLL presented in this paper is connected to the WF Inverter. The reason for this is that the WF Inverter delivers current to the grid, and to do so will the current phase angle decide on what type of power the converter delivers. The reference frequency for the converter is the grid voltage. The grid voltage is measured on and sent to the PLL. Because the WF Inverter operates in a synchronous reference frame are the three-phase grid voltage signals transformed into a dq signal with an initial phase angle zero. The purpose of this PLL is to set the phase angle of the synchronous reference frame equal to the grid phase angle. When synchronization is achieved, the dq voltage signal will be constants. The angle between the direct and quadrature axis is always 90°. They will

always rotate at the same speed, and the direct axis voltage V^d can, therefore, be neglected. After the transformation is the quadrature voltage signal V^q filtered to remove high order frequencies.

$$G_{PLL}(s) = \frac{1}{T_{f,PLL}s + 1} \tag{2.9}$$

Where G_{PLL} is the filter transfer function in the Laplace domain and $T_{f,PLL}$ is the filter break frequency. The reference quadrature voltage signal is set to zero as this will make the direct voltage signal equal to the three-phase voltage peak phase signal V_g.

$$V^d = V_g \quad and \quad V^q = 0 \tag{2.10}$$

The quadrature reference voltage and real voltage are compared which generated an error. This error is sent through a PI controller with transfer function H_{PLL}

$$H_{PLL} = K_{p,PLL} + \frac{K_{i,PLL}}{s} \tag{2.11}$$

where $K_{p,PLL}$ and $K_{i,PLL}$ are the proportional and integral terms of the PLL PI controller, respectively. The PI controller generates ω_{error}, which is the angular frequency difference between the synchronous reference frame ω_{PLL} and the base angular frequency ω_b. The rotation speed of the synchronous reference frame can be calculated accordingly

$$\omega_{PLL} = \omega_b + \omega_{error} \tag{2.12}$$

The real phase angle θ_{PLL} can thereby be calculated by integrating the synchronous reference frame speed.

$$\theta_{PLL} = \frac{\omega_{PLL}}{s} \tag{2.13}$$

This reference frame angle is sent back to the beginning of the PLL loop to transform the three-phase signal into the dq reference frame. The loop is then restarted to produce an even smaller phase angle error. The PLL process is illustrated under

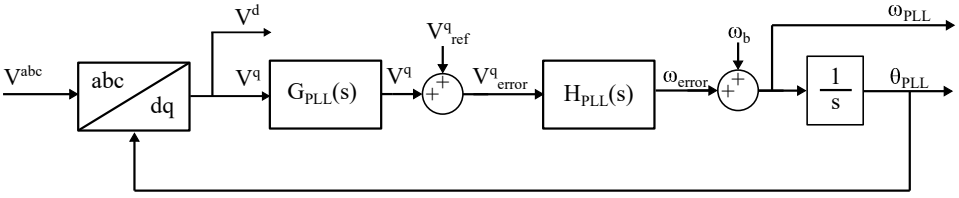


Figure 2.7: PLL block diagram

2.3 Voltage Source Converter Tuning

The VSC is controlled by a current controller presented in [1]. The current controller gets its reference values from the PLL controller. For weak grids can one power supply, like

the wind turbine system presented in this thesis, influence the grid voltage substantially. This can make the input of the PLL oscillating, which can, if not tuned correctly, make the PLL use a long time to synchronize with a higher margin of error. Which can make the power output of the inverter oscillate and, in the worst case, make the whole system unstable. That is why it is important to design a system with substantial transient response and margins. This section will present a technique on how to tune the PI parameters of the current controller and PLL controller. The WF Inverter parameters are

Table 2.1: WF Inverter parameters

Parameter	Value
Rated power S_w	50e6 VA
Rated ac voltage V_w	690 V
Rated dc power $V_{w,dc}$	1500 V
Rated frequency f_w	50 Hz
Inverter Resistance R_w	0.003 pu
Inverter Inductance L_w	0.15 pu
Inverter Capacitance C_{fw}	0.0344 pu

The system parameters of the current controller and the PLL are

Table 2.2: VSC and PLL PI parameters

Parameter	Value
VSC CC gain $K_{p,cc}$	0.0455
VSC CC integral term $K_{i,cc}$	4.5487
PLL gain $K_{p,PLL}$	1
PLL integral term $K_{i,PLL}$	16.42

2.3.1 VSC Tuning Techniques

The open loop transfer function of the controller is a low order plant. The system transfer function is the product of the current controller, PWM and the PLL. [31]

$$G_{cc,ol}(s) = K_{p,cc}(\frac{1+T_{cc}s}{T_{cc}})\frac{1}{1+sT_a}\frac{1}{R_W}\frac{1}{1+s\tau} \tag{2.14}$$

There are two ways to tune the parameters of the current controller. The first is modulus optimum. Modulus optimum is a way to simplify the system transfer function and, in that way, tune the current controller. According to [32], is modulus optimum common when tuning analog controllers with low order control plants, that does not contain any time delays. This controller has a dominant time constant, and additional, but less significant, time constants. With modulus optimum, it will be possible to cancel out these lesser constants, which gives fewer poles and a less complicated system. The poles are canceled when the PI parameters are equal to the current controller parameters, accordingly

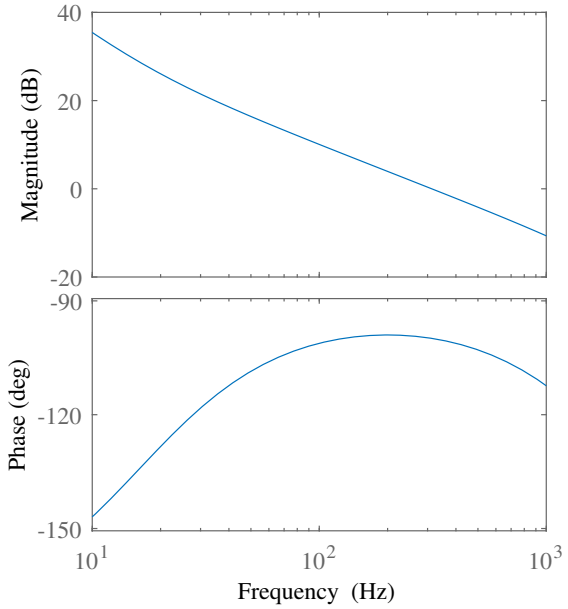


Figure 2.8: Current controller bode

$$T_{cc} = \tau \tag{2.15}$$

$$K_{p,cc} = \frac{\tau R_W}{2T_a} \tag{2.16}$$

When the PI parameters are set to these values the new open loop current controller transfer function becomes

$$G_{cc,ol}(s) = \frac{1}{2}\frac{1}{T_a^2 s^2 + T_a s} \tag{2.17}$$

The second way to tune the parameters is according to symmetrical optimum. Symmetrical optimum is presented in [31]. The main objective of symmetrical optimum is to maximize phase margin for low frequencies. This will make the system more tolerant to delay. 2.8 shows the frequency response of the current controller. The figure shows that the system operates with phase margin of 70° around the operating point(50Hz). The peak phase margin is 80°, which occurs where the magnitude plot crosses 0dB. According to the bode plot is the current controller stable, with good stability margins.

Next is to analyze the step response of the current controller, which can be found in figure 2.9. The step response can be calculated according to [33]. Rise time is defined as how long it takes for the system to go from 5% to 95% of its final value. Peak time is at what time the first peak value of the response occurs. Maximum overshoot is how high

above unity the maximum peak goes; for this case, it is presented in percent. Settling time is how long time it takes for the system response to reach 98% of unity value, without it deviate outside of 2% of unity value.

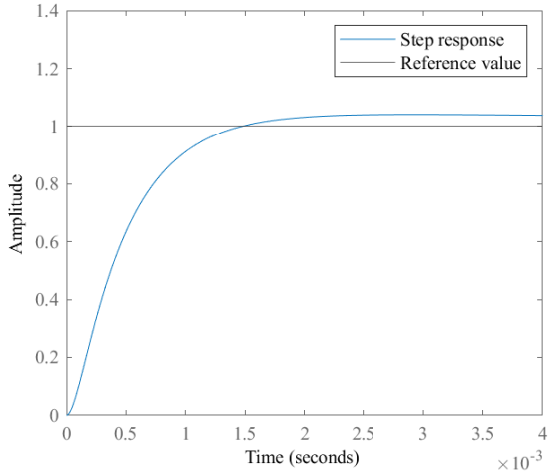


Figure 2.9: Current controller step response

It can be seen that the system transient response is
Rise time = 1.15e-3 sec (5% to 95%)
Peak time = 2.9e-3sec
Maximum overshoot = 4%
Settling time = 4e-3 sec

2.3.2 PLL Response

As discussed previously is quadrature voltage filtered and then sent into a PI controller. The output of the PI controller of the PLL is the angular frequency of the rotating reference frame. This angular frequency is integrated to find the angle of the rotating reference frame. These calculations are what generates the system transfer function. [34]

$$G_{PLL} = (K_{p,PLL} + \frac{K_{i,PLL}}{s})\frac{1}{s}\frac{1}{T_{f,PLL}s + 1} \tag{2.18}$$

The frequency response for the PLL is presented in the 2.10. The figure shows that the cross over point occurs at very low frequency. And if the magnitude of the converter is to be shifted, the PLL will still operate with decent stability margins around 50Hz.

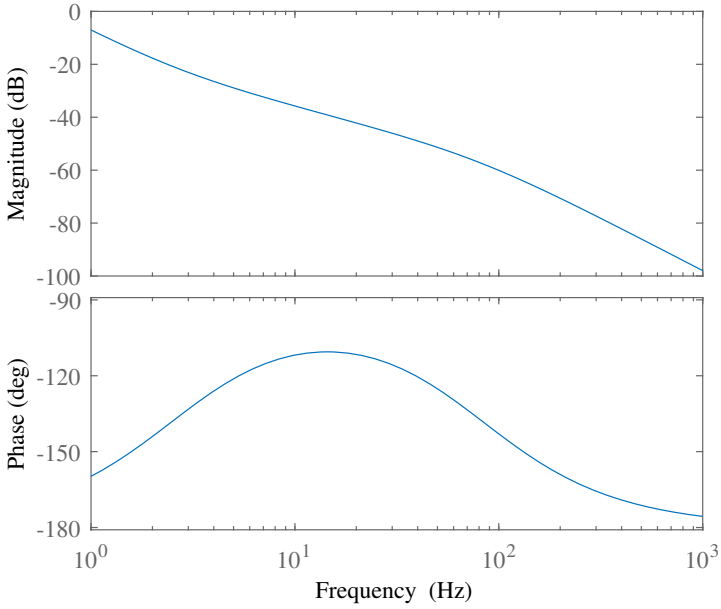


Figure 2.10: PLL bode plot

Chapter 3

High-Voltage DC Rectifier

This chapter describes the operating principle and tuning technique of a MMC rectifier in a HVDC system. This chapter will also present the parameters used to control the MMC and the system frequency response this generates. The MMC is controlled according to three principles, Compensated modulation and Direct modulation with and without circulating current control. 3.1 show where in a HVDC conversion system the MMC rectifier is located. In this thesis, when the HVDC system is mentioned it talks about the MMC rectifier.

Modular multilevel converters (MMC) have been accepted in the industry as they are able to produce excellent voltage quality for medium and high voltage. When compared to a 2-level voltage source converter, an MMC requires less filtering and has lower power semiconductor losses. [35] Compared to other types of multilevel converters, like a neutral point clamped converter (NPC), the MMC is beneficial, as many cells allow it to produce voltages of different levels. [36] Even though it has a large number of cells that require a more complex controller, the simple design of each cell result in a simple structure. This, together with lower filtering requirements, lowers production costs and makes the MMC highly competitive. A type of multilevel converter capable of reaching high voltage levels is the H-bridge converter. According to [36], do each H-bridge usually require an isolated dc-source, which is often supplied by a multi pulse transformer. MMCs does not require an input transformer [37] which makes scaleability simple for medium and high power levels. [38], [39]

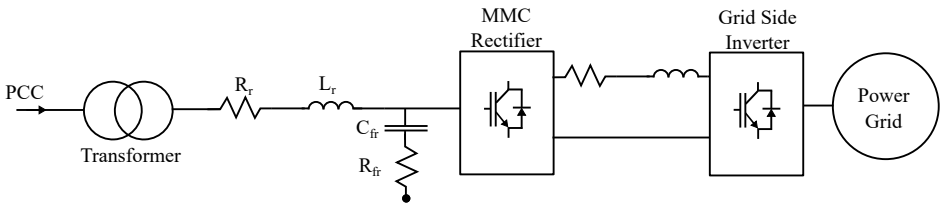


Figure 3.1: HVDC converter system

3.1 Modular Multi Level Converter Topology

An MMC is a converter consisting of a large number of power cells, connected in series. Each of these power cells, or submodules (SM), consists of some kind of switching system. [40] Typical switching systems are full-bridge converter, half-bridge converter, unidirectional cells, multilevel NPC cell, multilevel flyback capacitor cell, and some other converters described by M.A.Perez in [35]. Among these, are full-bridge and half-bridge most common. A half-bridge SM is only able to generate positive and zero voltage, and will, therefore, require the power system to be connected to a dc system. The full-bridge converter is, on the other hand, able to also generate negative voltage and can, therefore, be used when connected to both full ac and dc systems. The disadvantage of the full-bridge converter is that it demands more physical components then a half-bridge cell. A unidirectional modular multilevel converter (uMMC) for HVDC subsea system is proposed by G.J.M.de Sousa in [41]. It can be advantageous to other MMCs as it requires only one switching device per SM, which can lower cost and increase reliability. The disadvantage of the uMMC is that current can only flow one direction. This prevents the converter from being applicable for some popular generator types for wind turbines, like the doubly fed induction generator, which requires reactive power to induce a magnetic field to produce power. Most of the literature found for this thesis, [35], [36], [38], [41], are on 2-level arm converters (2L), but in [42] E. Solas explains the working principles of 3-level arm converters (3L). For example, can, according to [42], a 3L-NPC converter do approximately the same job as a 2L converter, with half the SMs, which can make the 3L-NPC more compact than a 2L converter. But, the 3L NPC and flyback converter will require voltage balancing control for all capacitors of each SM. These extensive measurement requirements, of all capacitor voltages, increase computational costs, which can be a determining factor when deciding what type of converter to use.

A half-bridge MMC is illustrated in 3.2. The SM contains two switches and is therefor capable of operating in three modes.[40]

- *Inserted:* S1 is open and S2 is closed, the capacitor is charges and discharges.
- *Bypassed:* S1 is closed and S2 is open, the voltage in the capacitor remains constant.
- *Blocked:* Both gates are in an open state blocking current from flowing. The voltage from the dc voltage source may still charge up the capacitor, but the capacitor may not discharge.

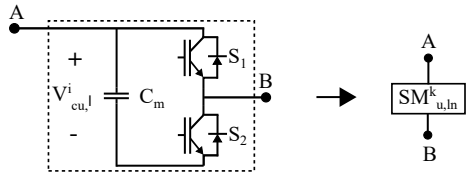


Figure 3.2: Half-bridge cell for MMC SM

An MMC can convert power from single phase to single phase, three phase to single phase, single phase to three phase and three phase to three phase as illustrated in 3.3 [35]

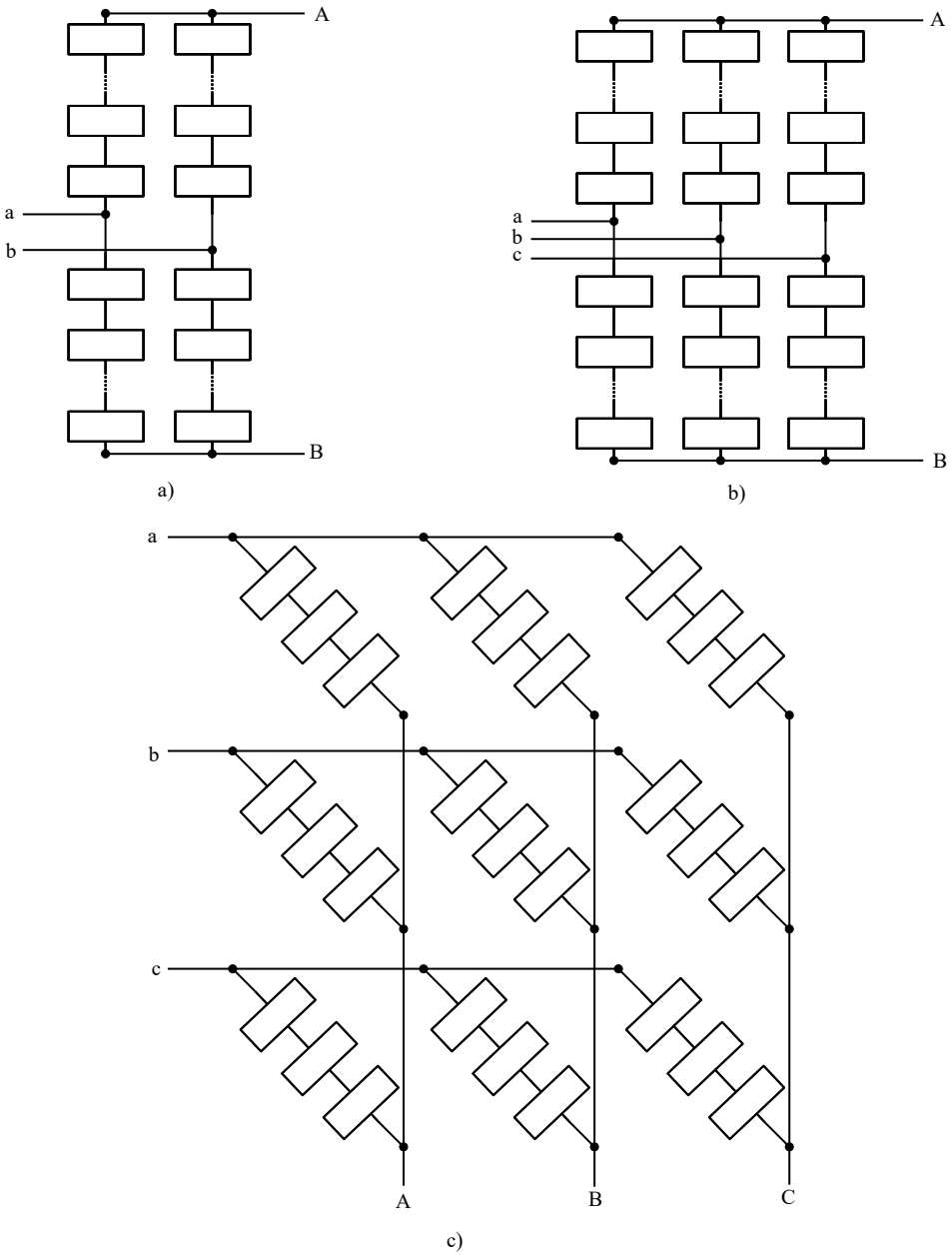


Figure 3.3: Modular multilevel converter. a) single phase to single phase b) three phase to single phase, single phase to three phase and c) three phase to three phase

The power cells are divided into subgroups called arms, which are connected between two phases(example dc phase and ac phase). For a single-phase to three-phase converters, an arm can be connected in two ways, either to the positive or negative part of the single

phase. If the arm is connected to the positive part of the single-phase, it is an upper arm and is noted with the subscript *u*, if an arm is connected to the negative phase of the single line, it is a lower arm, and is noted with the subscript *l*. An example of a MMC connected between a dc and a three-phase ac grid is presented in 3.4, where V_{dc} and V_g are the dc and ac grid voltages, respectively, and L_{dc}, L_m and L_s are the dc side, arm and ac side inductances, respectively.

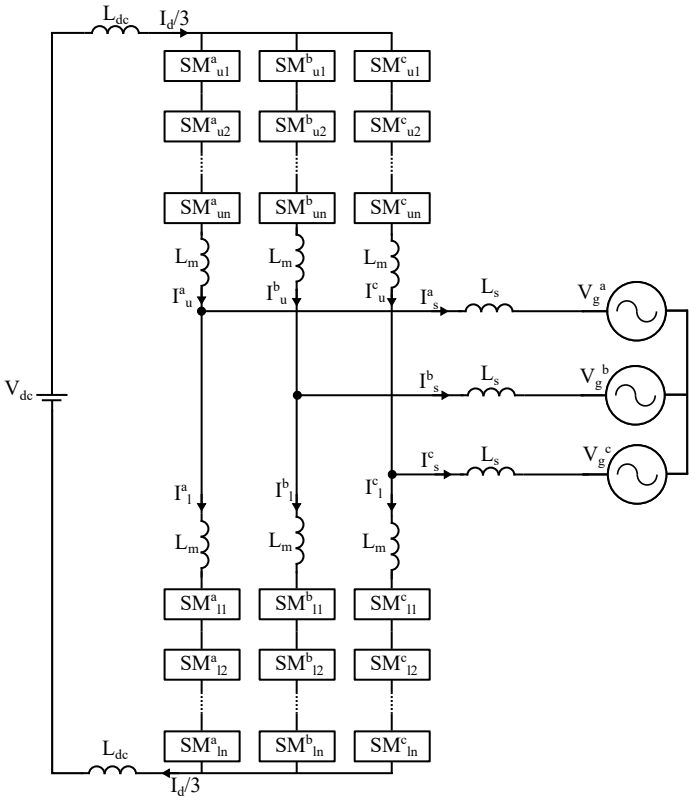


Figure 3.4: Modular multilevel converter. Single phase to three phase

3.2 Dynamic Relations of MMC

The common way of controlling an MMC is to control the voltage or current at its terminal. There must be implemented a control strategy that controls the voltage levels in the energy storage elements of the MMC. There can also be a secondary control objective, some of which are explained under this section.

Arm current control is used to decide the arm current and is presented in [43]. It can be used to control ac side current, dc-bus current and circulating current. Arm current is set by controlling the arm voltages. [25] The modulation signals can be calculated directly from the input and output reference set for the desired operating value. An open-loop

case is presented in [44] where a compensation term is included to eliminate steady state error. This strategy is able to produce a stable output in steady state. For the closed loop case presented in [45] the feedback loop eliminates the steady-state error. These closed loop systems can vary in difficulty, from simple PI controllers to more advanced linear-quadratic regulator controllers.

Capacitor voltage control operates with the purpose of maintaining a set average voltage reference level. To simplify the calculations for this technique, all SMs are considered to be a single equivalent capacitance. From [25] the power equation describing the relationship of the capacitance power P_{cap}, input power P_{in}, output power P_{out} and power loss P_{loss} across the MMC in steady state is

$$P_{cap} = P_{in} - P_{out} - P_{loss} \tag{3.1}$$

Power across the capacitor is

$$P_{cap} = \frac{C_{eq}}{2} \frac{dV_{avg}^2}{dt} \tag{3.2}$$

Where C_{eq} is the equivalent capacitance and V_{avg} is the average voltage. This means that for the energy to stay constant across the equivalent capacitor, the power sent into the system must equal the power out plus any losses in the converter, while operating at steady state.

To study the dynamics of an MMC it can be beneficial to study it as an equivalent circuit, where the SMs are modeled as a constant voltage source. This allows us to simplify each phase of the model substantially, as illustrated in the following figure. [38]

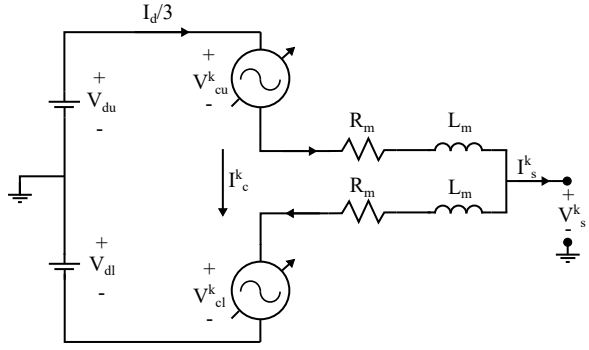


Figure 3.5: Modular multilevel converter. Single phase equivalent circuit.

As for the VSC are each phase expressed by *k* for a three phase MMC. Where V_{du} and V_{dl} are the positive and negative dc voltages, respectively. Where in the case of figure 3.5 they will be half of the real dc voltage, presented in 3.3

$$V_{du} = V_{dl} = \frac{V_{dc}}{2} \tag{3.3}$$

The voltages $V_{cu,l}^k$ are the voltage representing the capacitors and is where the control signal is sent to control the MMC. [38] The resistance R_m are parasitic arm resistance and

converter losses, which is often very small and can vary with operating conditions. The inductance L_m is the arm inductance, which is there to lower the fault current and current harmonics of each arm. [40] The inductance is also necessary to limit the current that flows when a switch turns on/off due to the instantaneous difference in voltage across the arm. [35] There are three different currents flowing in the MMC. We assume power flow from the dc to the ac side. The current from the dc side is divided equally in each of the three phases. Therefore, is the current in the upper leg equal to $I_d^k/3$. The output current flowing on the ac side of the MMC is I_s^k. At first sight, it can be natural to think that the dc current is equal to the ac current of the MMC. But an important characteristic for the MMC is the upper and lower circulating current $I_{u,l}^k$ controls the output current.

$$I_s^k = I_u^k - I_l^k \tag{3.4}$$

Where the circulating currents I_c^k is defined as

$$I_c^k = \frac{I_u^k + I_l^k}{2} \tag{3.5}$$

Kirchhoff's voltage law can be used to find the dynamic of the equivalent circuit by summing the voltages across all the components.

$$V_{du} = V_g^k + V_{cu}^k + R_m I_u^k + L_m \frac{dI_u^k}{dt} \tag{3.6}$$

$$V_{dl} = -V_g^k + V_{cl}^k + R_m I_l^k + L_m \frac{dI_l^k}{dt} \tag{3.7}$$

Where V_g^k is the voltage on the ac grid side of the converter. According to [40] is the sum of all the capacitor voltages equal $V_{cu,l}^k$

$$V_{cu}^k = n_u^k V_{cu}^{\sum k} \tag{3.8}$$

$$V_{cl}^k = n_l^k V_{cl}^{\sum k} \tag{3.9}$$

Where $n_{u,l}^k$ are the insertion indices in phase k when u and l are upper and lower arm, respectively. And $V_{cu,l}^{\sum k}$ are the sum of voltages across all capacitors in phase k, for upper and lower arm. [38] represent two techniques for controlling the MMC, *compensated modulation* and *direct modulation*.

3.2.1 Compensated Modulation

Compensated modulation makes it possible to disregard the internal dynamics of the MMC. [38] [40] This makes way for the assumption that the arm voltages are equal to the voltage control references. This type of control is very difficult to implement in reality as time delays from the voltage measurements will lead to problems.

For compensated modulation the insertion index calculated accordingly

$$n_u^k = \frac{V_{du} - V_s^{refk}}{V_{cu}^{\sum k}} \tag{3.10}$$

$$n_l^k = \frac{V_{dl} + V_s^{refk}}{V_{cl}^{\sum k}} \tag{3.11}$$

Where V_s^{refk} is the desired output voltage in phase k. Subtracting 3.6 and 3.7 gives

$$L_m \frac{d}{dt}(I_u^k + I_l^k) + R_m(I_u^k + I_l^k) + (v_{cu}^k + v_{cl}^k) = V_{dc} \tag{3.12}$$

substituting in 3.5, 3.8-3.11, 3.13 show that the circulating current naturally drops to zero at steady state. This means, that its not necessary to actively suppress the circulating current. [38]

$$L_m \frac{dI_c^k}{dt} + R_m I_c^k = 0 \tag{3.13}$$

Adding 3.6 and 3.7 gives

$$L_m \frac{d}{dt}(I_u^k - I_l^k) + R_m(I_u^k - I_l^k) + (V_{cu}^k - V_{cl}^k) = V_{dc}^{\Delta} \tag{3.14}$$

where $V_{dc}^{\Delta k}$ is the imbalanced dc bus voltage in phase k

$$V_{dc}^{\Delta k} = V_{du}^k - V_{dl}^k \tag{3.15}$$

which for a three phase system is equal to zero. [38] Substituting 3.4, 3.8-3.11, 3.13 into 3.14 gives the dynamic equation describing the output current from the MMC for compensated modulation mode.

$$\frac{L_m}{2}\frac{dI_s^k}{dt} = V_s^k - V_g^k - \frac{R_m}{2} I_s^k \tag{3.16}$$

3.2.2 Direct Modulation

For direct modulation mode will the internal dynamics of the MMC have to be considered. By assuming that the capacitance is high enough to maintain a constant voltage across each arm, the sum of the capacitor voltages is equal to the dc side voltage. The insertion index from 3.10 and 3.11 are used to find the new insertion index n_{ul}^k for the direct modulation controller by taking the circulating current voltage reference V_c^{refk} into consideration

$$n_u^k \approx \frac{V_{du} - V_s^{refk} - V_c^{refk}}{V_d} \tag{3.17}$$

$$n_l^k \approx \frac{V_{dl} + V_s^{refk} - V_c^{refk}}{V_d} \tag{3.18}$$

The general formula for energy stored in a capacitor is used to find the sum of the energy in each arm of the converter.

$$W_{ul}^k = \frac{C_m}{2} \sum_{i=1}^{N} (V_{c,ul}^{ik})^2 \tag{3.19}$$

Where W_{ul} is the stored up energy in the capacitor, N is the number of SMs, C_m and V_c^i is the individual capacitance and capacitor voltage, respectively. It is known that the input power of an arm at one instant is equal to the time derivative of stored up energy.

$$\frac{dW_{ul}^k}{dt} = C_m \sum_{i=1}^{N} V_{c,ul}^{ik} \frac{dV_{c,ul}^{ik}}{dt} = V_{c,ul}^k I_{c,ul}^k \tag{3.20}$$

Due to the large capacitance of the converter is the change in energy minor, which allows for the assumption that the individual arm capacitor voltage $V_{c,ul}^{ik}$ is equal to the sum of the capacitor voltages in either upper or lower arm $V_{c,ul}^{\sum k}$, divided by the number of SM in that arm. Or in other words, the arm capacitor voltage is equal to the mean capacitor voltage.

$$\frac{dW_{ul}^k}{dt} = C_m \sum_{i=1}^{N} V_{c,ul}^{ik} \frac{dV_{c,ul}^{ik}}{dt} \approx \frac{C_m}{N} V_{c,ul}^{\sum k} \sum_{i=1}^{N} \frac{dV_{c,ul}^{ik}}{dt} = \frac{C_m}{2N} \frac{d(V_{c,ul}^{\sum k})^2}{dt} \tag{3.21}$$

This assumption makes for a new expression for the energy stored per arm

$$W_{ul}^k = \frac{C_m}{2N} (V_{c,ul}^{\sum k})^2 \tag{3.22}$$

The dynamic equation of the sum of the capacitor voltage can now be derived by substituting 3.21 and

$$V_{c,ul}^k = n_{ul}^k V_{c,ul}^{\sum k} \tag{3.23}$$

into 3.20. Resulting in

$$\frac{C_m}{N} \frac{dV_{c,ul}^{\sum k}}{dt} = n_{ul}^k I_{ul}^k \tag{3.24}$$

The converter voltage can be found by substituting upper and lower arm voltage from the dc side voltage.

$$V_c = \frac{V_d - n_u^k V_{cu}^{\sum k} - n_l^k V_{cl}^{\sum k}}{2} \tag{3.25}$$

Where the sum of the upper and lower converter voltages are, of course, equal to the total of the capacitor voltages

$$V_c^{\sum k} = V_{cu}^{\sum k} + V_{cl}^{\sum k} \tag{3.26}$$

By substituting 3.17, 3.18, 3.25 and 3.26 into 3.24, the first equation describing the internal dynamics of the MMC is obtained in 3.27.

$$\frac{C_m}{N} \frac{dV_c^{\sum k}}{dt} = -\frac{V_s^{refk} I_s^k}{V_d} + (1 - \frac{2V_c^{refk}}{V_d}) I_c^k \tag{3.27}$$

The unbalanced capacitor voltage per phase $V_c^{\Delta k}$ is the difference between the sum of the upper and lower capacitor voltages

$$V_c^{\Delta k} = V_{cu}^{\sum k} - V_{cl}^{\sum k} \tag{3.28}$$

By deviating 3.28 and then substituting in 3.3 - 3.5, 3.17, 3.18, 3.24, the dynamic state equation for unbalanced capacitor voltage is derived to be

$$\frac{C_m}{N}\frac{dV_c^{\Delta k}}{dt} = (1 - \frac{2V_c^{refk}}{V_d})\frac{I_s^k}{2} - \frac{2V_s^{refk}}{V_d}I_c^k \tag{3.29}$$

3.16 describes how the circulating current decays for compensated modulation control. This will not be the case for direct modulation as the circulating current does not equal zero. From subtracting 3.8 and 3.9 the new expression for circulating current is derived

$$L_m\frac{dI_c^k}{dt} = V_c^k - R_m I_c^k \tag{3.30}$$

Now, by substituting in 3.3 - 3.5, 3.17, 3.18, 3.25, 3.26 and 3.28 for 3.30 the dynamic circulating state equation is derived

$$L\frac{dI_c^k}{dt} = \frac{1}{2}(V_d - \frac{V_c^{\sum k}}{2} + \frac{V_c^{refk}V_c^{\sum k}}{V_d} + \frac{V_s^{refk}V_c^{\Delta k}}{V_d}) - R_m I_c^k \tag{3.31}$$

3.3 Control Structure

3.3.1 Phase Shift and Level Shifted Modulation

Phase shifted and level shifted triangular waveforms are often compared with the reference signal to generate a switching signal, as illustrated in 3.6a and 3.6b. These techniques have, even though they are good, high switching losses compared to other techniques, like fundamental frequency modulation. [25] Level shifted modulation is presented in [46], there it is specified that this technique is very simple, even for a large number of SM per arm. This is not the case for phase shifted modulation as this technique becomes complex as the number of SM per arm increases. [25]

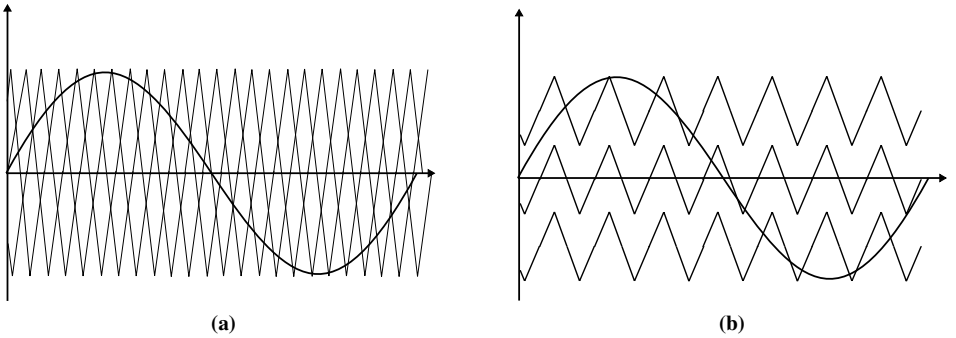


Figure 3.6: Pulse width modulation: a) Phase shifted modulation b) Level shifted modulation

3.3.2 Proportional Resonant Controller

There are two popular ways to control converters presented in this report. The first one is dq-control and the second phase control. Phase control takes, in this case, in three sinusoidal signals, a, b and c, and compare these signals to oscillating reference signals. Two compare the reference and measured signals, a proportional-resonant (PR) controller is implemented in [38]. The PR controller has three parameters, the proportional term K_p, a resonant term K_r and a frequency term ω. The transfer function $H_v(s)$ of the PR controller controlling the ac voltage is

$$H_v(s) = K_{pv} + \frac{K_{rv}s}{s^2 + \omega_v^2} \tag{3.32}$$

Where the subscript v is indicating that the parameter is a part of the ac voltage controller. The goal of the PR controller is to make the MMC operate in steady state, with as low error as possible. A model of how the controller is implemented for the system is illustrated in 3.7

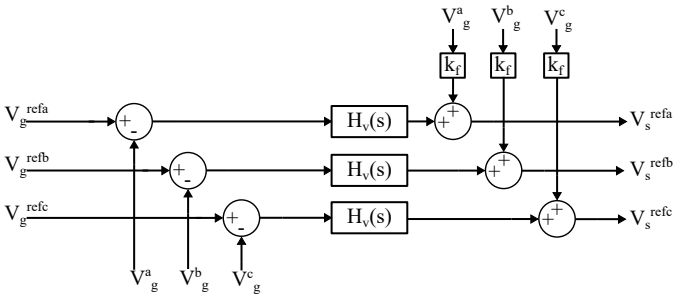


Figure 3.7: PR controller with feed forward gain

To improve the dynamic response, a feed forward gain k_f is included in the controller. The reference output voltage of the MMC in the frequency domain $V_s^{refk}(s)$ is

$$V_s^{refk}(s) = H_v(s)[V_g^{refk}(s) - V_g^k(s)] + k_f V_g^k(s) \tag{3.33}$$

Where V_g^{refk} is the fundamental frequency voltage.

In the direct modulation case, as discussed previously, circulating current control has to be considered, as circulating current is not suppressed naturally for this case. The circulating current is controlled by controlling the circulating current voltage. The circulating current voltage is controlled with a PR controller, accordingly

$$H_c(s) = K_{pc} + \frac{K_{rc}}{s^2 + \omega_c^2} \tag{3.34}$$

Where $H_c(s)$ is the transfer function of the controller, K_{pc}, and K_{rc} is the controller proportional and resonance parameters, respectively, and ω_2 is twice the angular frequency. The PR controller takes in circulating current reference and measures circulating current, which is calculated according to 3.5. The circulating current voltage is given by

$$V_c^{refk}(s) = H_c(s)[I_c^{refk}(s) - I_c^k(s)] + RI_c^{refk}(s) \tag{3.35}$$

Where the reference circulating current I_c^{ref} is equal to the steady state current I_{c0}^k, and resistance times reference current compensates for the voltage drop that occurs due to the resistive parasitic element in the converter.

3.4 HVDC Tuning

A frequency and time dependent scenario has to be performed to test the potential stability of these components. In order to do so, the parameters have to have some value. Each value for the MMC and its controller is presented in 3.1 and 3.2.

Table 3.1: HVDC parameters

Parameter	Value
Rated power S_r	50e6 VA
Rated ac voltage V_r	166e3 V
Rated dc power $V_{r,dc}$	400e3 V
Rated frequency f_r	50 Hz
Arm resistance R_m	1.81e-6 pu
Arm inductance L_m	0.057 pu
SM capacitance C_m	96.95 pu
Rectifier Resistance R_r	0.0011 pu
Rectifier Inductance L_r	0.054 pu
Rectifier Capacitance C_{fr}	0.2038 pu

Table 3.2: MMC PR controller parameters

Parameter	Value
Ac voltage PR, proportional K_{pv}	0.5
Ac voltage PR K_{rv}	50
Circulating current PR controller K_{pc}	20
Circulating current PR controller K_{rc}	1000

3.32 represent the ac voltage controller in open loop. This function can be turned into closed loop with 3.36.

$$H_{v,cl}(s) = \frac{H_v(s)}{1 + H_v(s)} \tag{3.36}$$

The result of the previous equation is presented in 3.37

$$H_{c,cl}(s) = \frac{K_{pv}(1 + T_{pv})}{T_{pv} + K_{pv}(1 + T_{pv})} \tag{3.37}$$

Where T_{pv} is the resonant time constant given by

$$T_{pv} = \frac{K_{pv}}{K_{rv}} \tag{3.38}$$

To evaluate stability is it of interest to study the response of the PR ac voltage controller. 3.8 show the controller response in a bode plot. The result from the bode plot show that the controller delivers stable output for normal frequency range.

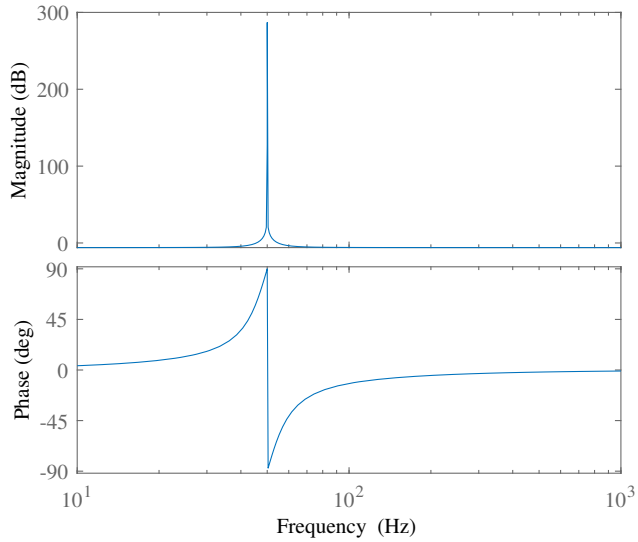


Figure 3.8: PR ac voltage controller bode

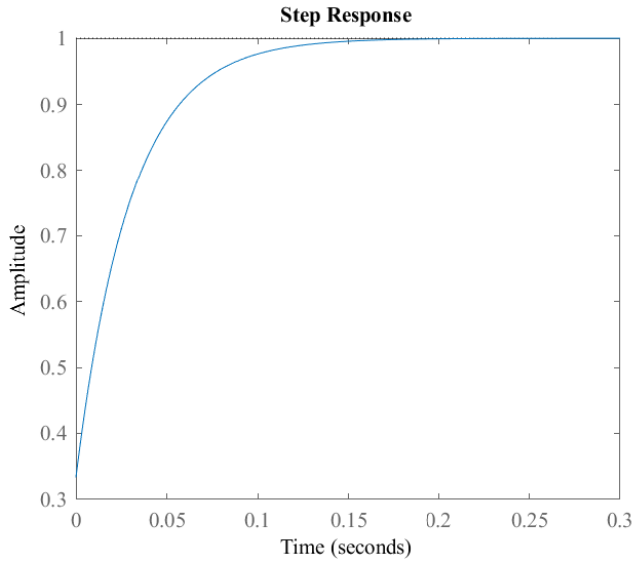


Figure 3.9: PR ac voltage controller step response

The voltage controller step response is presented in 3.9, and is used to evaluate how long time the controller will use to produce a stable output.

The figure shows that the settling time is fast with a critically damped response, meaning that the system reaches the reference value without any overshoot. The step response gives the following transient response Rise time = 100e-3 sec (5% to 95%)
Settling time = 110e-3 sec

Chapter 4

Stability Analysis of Wind Farm-HVDC System

This chapter show how to calculate various stability models of a VSC and a MMC. It show how stable the converters should be according to parameters presented in 2.1, 2.2, 3.1 and 3.2.

Small-signal stability methods test system stability by injecting a small perturbation current, also called disturbance, into a system. A small perturbation current is in this case a current that still allows the system equations to be linearized for analysis purposes. [47] A system is considered unstable if, by injecting a small disturbance, the system goes from synchronized to unsynchronized. In power systems today, lack of system stability is often due to insufficient damping of system oscillations. [47] To perform small-signal stability analysis the system has to be linearized, which was explained in 1.7.

4.1 State Space Representation

4.1.1 Wind Energy Conversion State Space

This section will present a description of how to generate equations describing all operating conditions for a VSC with current control connected to a grid. 4.1 show the location of all parameters for the system, except for the controller. To generate the equations to analyzing the system, fairly simple circuit analysis can be performed. [48]

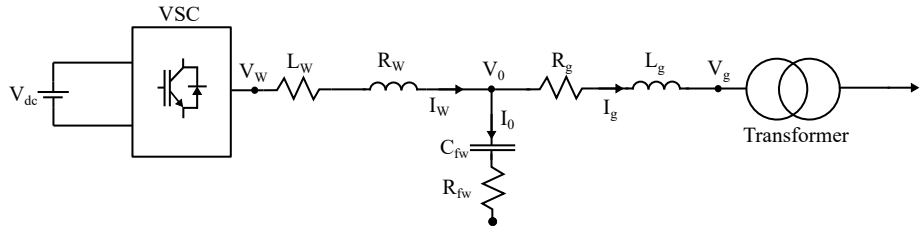


Figure 4.1: Voltage source inverter wind conversion system

The dynamic equation of current flowing from the converter I_W is decided by the voltage difference between the converter V_W and V_0, and the voltage drop across the converter resistor R_W and inductor L_W. The function for the current is presented in 4.1, take note that the current is transferred to the dq domain, which introduces an additional term calculated in Appendix.

$$\frac{dI_W^{dq}}{dt} = \frac{V_W^{dq} - V_0^{dq} - I_W^{dq} R_W}{L_W} \pm \omega_g I_W^{qd} \tag{4.1}$$

Where ω_g is the grid frequency. Another dynamic equation of grid current I_g is decided by the the voltage difference between V_0 and the grid V_g, and grid resistance R_g and inductance L_g, in 4.2.

$$\frac{dI_g^{dq}}{dt} = \frac{V_0^{dq} - V_g^{dq} - I_g^{dq} R_g}{L_g} \pm \omega_g I_g^{qd} \tag{4.2}$$

4.3 describes V_0. It specifies that V_0 is equal to the voltage drop across the grounded capacitor C_{fw}. It is calculated by analysing the sum of the currents flowing through V_0

$$\frac{dV_0^{dq}}{dt} = \frac{I_W^{dq} - I_g^{dq}}{C_{fw}} \pm \omega_g V_0^{qd} \tag{4.3}$$

Current Controller

The VSC dynamics are also dependent on the controller parameters. This means that the current controller with the PLL generate reference signals which are used for the VSC. The block diagram of the current controller with a PLL is represented in chapter 2. The block diagram is built to emulate 4.4 to calculate the converter voltage V_{conv}

$$V_{conv}^{dq} = V_o^{dq} + H_{cc}(I_{cc,ref}^{dq} - I_{cc}^{dq}) \mp I_{cc}^{qd} \omega_{PLL} L_W \tag{4.4}$$

Where H_{cc} is the PI regulator with proportional and integral terms $K_{cc,p}$ and $K_{cc,i}$, respectively. Now, auxiliary variables γ can represent the dynamic performance of the integral term of the PI controller in 4.5.

$$\frac{d\gamma^{dq}}{dt} = (I_{cc,ref}^{dq} - I_{cc}^{dq}) \tag{4.5}$$

PLL

The PLL can be expressed with three dynamic equations describing its operating conditions. 4.7 is included do to the low pass filter containing an integral component. The standard equation for a signal going through a low pass filter is presented in 4.6

$$V_{PLL}^{q} = V^{q} \frac{\omega_{LP}}{s + \omega_{LP}} \tag{4.6}$$

Where V_{PLL}^{q} is the voltage running through the PLL, ω_{LP} is the cut-off frequency of the filter. The dynamic equation of 4.6 is

$$\frac{dV_{PLL}^{q}}{dt} = V^{q}\omega_{LP} - V_{PLL}^{q}\omega_{LP} \tag{4.7}$$

For steady-state operating conditions, the q component of the converter voltage should be zero. As the q-axis voltage signal is sent through the PLL-PI controller, a new auxiliary variable ϵ_{PLL} is introduced do to the integral term of the PI controller.

$$\frac{d\epsilon_{PLL}}{dt} = V^{q} \tag{4.8}$$

At last, the phase angle $\delta\theta_{PLL}$ of the PLL is calculated as V^q is used to calculate ω_{PLL} through a PI controller. The integral of ω_{PLL} is then taken which gives

$$\frac{d\delta\theta_{PLL}}{dt} = \delta\omega_{PLL} = Kp_{PLL}V^{q} + KI_{PLL}\epsilon_{PLL} \tag{4.9}$$

Where $\delta\omega_{PLL}$ also can be expressed as

$$\delta\omega_{PLL} = \omega_{PLL} - \omega_{g} \tag{4.10}$$

4.1.2 Modular Multi Level Converter State Space

The dynamic equations describing the operating conditions for the MMC are expressed in 3.24, 3.29 and 3.16. To use these equations to analyze the stability of the system, they first have to be linearized at a steady state. It may be assumed that the steady state conditions for the state variables are

$$V_{c0}^{\sum k} = 2V_{d} \tag{4.11}$$

$$V_{c0}^{\Delta k} = 0 \tag{4.12}$$

$$I_{c0}^{k} = \frac{P}{3V_{d}} \tag{4.13}$$

Where the subscript 0 notes the steady-state value and P is transferred power. [38]

4.2 Impedance Modeling

The system is tested for impedance response in a bode plot to evaluate the stability of the converters. When testing the frequency response of the ac equivalent impedance models the system can be split up into three parts, WF inverter, LC filter and HVDC MMC. Each impedance frequency response is also analyzed and compared to one another, by moving the equivalent impedances across the transformers. This chapter will also derive a way to represent the three impedances as one equivalent impedance model, shown in figure 4.2.

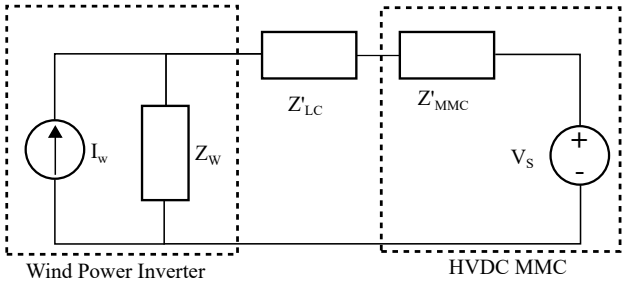


Figure 4.2: System impedance model

4.2.1 Voltage Source Converter Impedance

Impedance based stability analysis are in [49] superior to state space modeling as it overcome limitations that can occur for state space modeling. Additionally, impedance modeling will require the impedance of a system at the input and output terminal. The most common way to represent a VSC current controller is in the dq-domain, but it is also possible to represent a current VSC controller in the phase domain. [50] What type of controller will influence how complicated the stability analysis will become. In litterateur, impedance can be in either dq or sequence domain. [51] This thesis will prioritize sequence impedance as the MMC is controlled by a phase controller. Impedance modeling can be represented in for both dc and ac power. This thesis will present ac impedance modeling.

[49] presents an ac sequence impedance method for a VSC with dc voltage control, current control and PLL. When a constant dc voltage is assumed, the dc voltage control loop can be neglected for bandwidths above the voltage controller, which is 10Hz. For a system only containing a current controller, correct results may be assumed for bandwidths above the voltage controller, which is usually frequencies above 10Hz. The transfer function for the current controller is presented in 2.4. The synchronous reference frame angle θ_{PLL} is generated by integrating the angular frequency ω_{PLL}, which is generated from the PLL PI converter. This makes the PLL compensation function

$$H_{PLL2}(s) = (K_{p,PLL} + \frac{K_{i,PLL}}{s})\frac{1}{s} \tag{4.14}$$

The loop gain of the PLL them becomes

$$T_{PLL}(s) = \frac{V_w H_{PLL2}(s)}{2(1 + V_w H_{PLL2}(s))} \tag{4.15}$$

where V_w is the per unit phase to ground peak ac side voltage magnitude. The relationship between the phase voltages abc and the sequence voltages int the time domain can be written as

$$V_{wk}(t) = V_w cos(2\pi f_1 t) + V_p cos(2\pi f_p t + \phi_{vp}) + V_n cos(2\pi f_n t + \phi_{vn}) \tag{4.16}$$

where k is the phase, f_b is the fundamental or in this case the base frequency, V_p is the positive sequence voltage magnitude with a phase ϕ_{vp} and frequency f_p, and V_n is the negative sequence voltage magnitude with a phase ϕ_{vn} and frequency f_n. This can be written in the frequency domain as

$$V_a[f] = \begin{cases} V_1 & f = f_b \\ V_p & f = (f_p - f_b) \\ V_n & f = (f_n + f_b) \end{cases} \tag{4.17}$$

With these functions [49] calculate the positive Z_{wp} and negative Z_{wn} sequence impedance to be

$$Z_{wp} = \frac{H_{cc}(s - j\omega_b)V_0 + (s - j\omega_b)L_W}{1 - T_{PLL}(s - j\omega_b)[1 + H_{cc}(s - j\omega_b)\frac{I_w V_0}{V_w}])} \tag{4.18}$$

$$Z_{wn} = \frac{H_{cc}(s + j\omega_b)V_0 + (s + j\omega_b)L_W}{1 - T_{PLL}(s + j\omega_b)[1 + H_{cc}(s + j\omega_b)\frac{I_w V_0}{V_w}])} \tag{4.19}$$

where I_w is the ac side peak current. The input impedances include the output impedance of the inverter but is excluding the capacitor. Therefore, the capacitor impedance is calculated separately later in this chapter. The following figure shows where on the circuit the ac impedance is calculated from

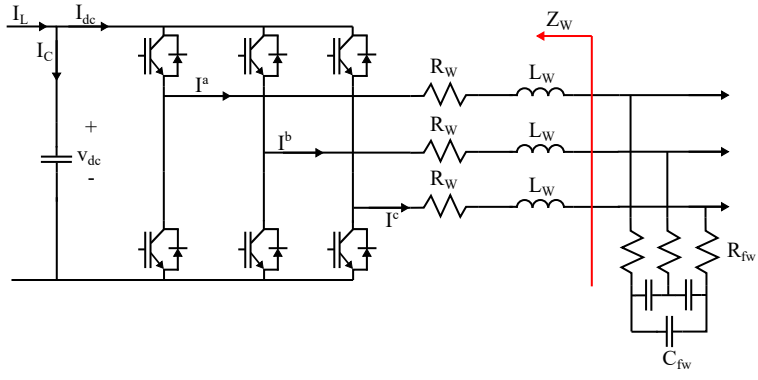


Figure 4.3: VSC impedance model

The frequency response of Z_W, which is equal to Z_{wp}, is presented in 4.4. There, it can be seen that the impedance margins are really high, which indicates that the VSC is stable for the operating conditions presented in 2.1 and 2.2

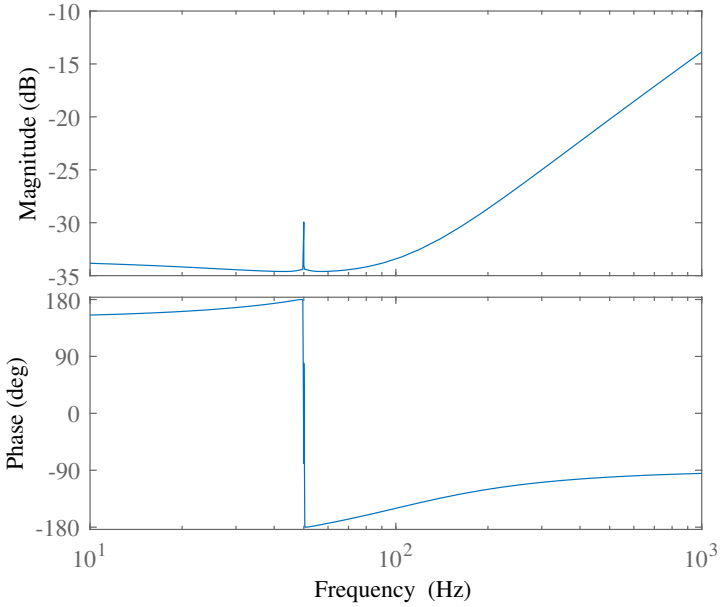


Figure 4.4: VSC frequency response

4.2.2 Modular Multi Level Converter Impedance

The MMC impedance is calculated as ac impedance from the grid side across the converters. The output impedance as well as the leg impedance is included, which can be seen in the following figure

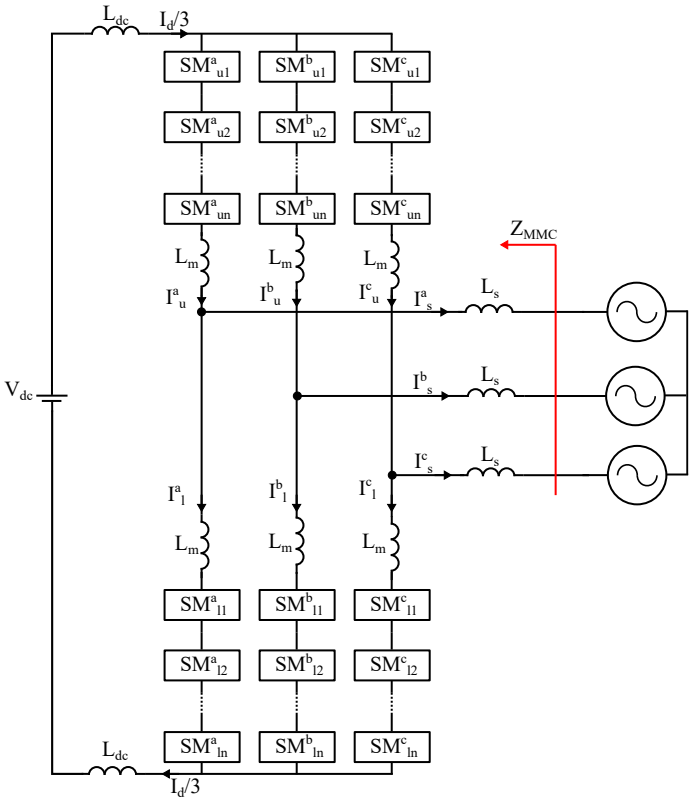


Figure 4.5: MMC ac impedance

Compensated modulation case

To study the stability for the compensated modulation controller, it is necessary to extract the impedance model of the MMC when the circulating current decays to become zero as time progress. The impedance is found by taking 3.33 and putting it into 3.16, then applying linearization. The result is

$$\frac{1}{2}(L_m s + R_m)\tilde{I}_s^k(s) = (k_f - H_v(s) - 1)\tilde{V}_g^k(s) \tag{4.20}$$

where the tilde is indicating that the variable is linearized. The impedance Z_{MMC} is given by $\tilde{V}_g^k$ over $-\tilde{I}_s^k$, accordingly

$$Z_{MMC}(s) = -\frac{\tilde{V}_g^k}{\tilde{I}_s^k} = \frac{L_m s + R_m}{2(1 - k_f + H_v(s))} \tag{4.21}$$

To evaluate the stability of the compensated modulation controller the bode plot and the Nyquist plot in 4.6 and 4.7, respectively. The bode plot shows that the converter is stable, but with a small impedance phase margin, 5.46dB at 50.3Hz. As there is no crossing of the -180° line, the impedance gain margin is assumed infinite. The Nyquist plot also indicates that the system is stable as there are no rotations around the critical point.

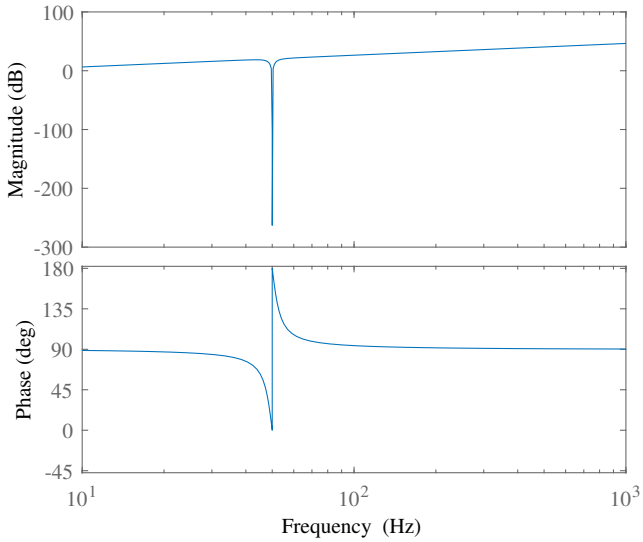


Figure 4.6: MMC with compensated modulation control bode plot

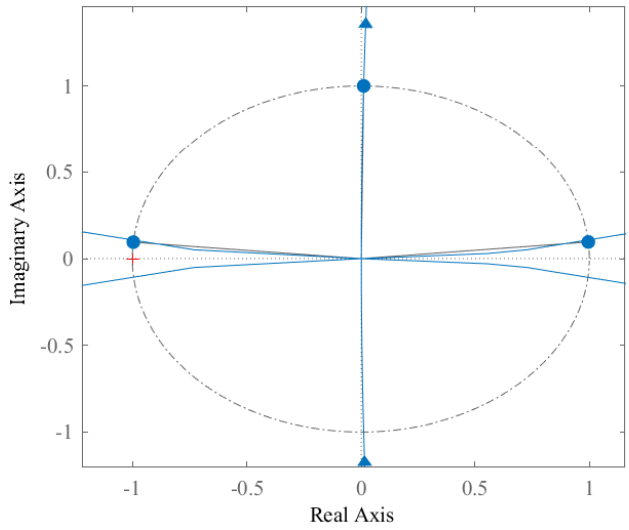


Figure 4.7: MMC with compensated modulation control Nyquist plot

Direct Modulation Without Circulating Current Control

To extract the impedance of the MMC ac voltage controller 3.14 is used as the equation describing the system. By substituting 3.5, 3.8, 3.9, 3.17 and 3.18 into 3.14 a new equation for system response is

$$2V_g^k + L\frac{dI_s^k}{dt} + R_m I_s^k + \frac{1}{2}V_c^{\Delta k} - \frac{V_c^{refk}}{V_d}V_c^{\Delta k} - \frac{V_s^{refk}}{V_d}V_c^{\sum k} \tag{4.22}$$

Without the circulating current controller it can be assumed that the circulating current voltage reference is equal to zero, V_c^{refk} = 0. With this assumption 4.22 can be simplified accordingly

$$2V_g^k + L\frac{dI_s^k}{dt} + R_m I_s^k + \frac{1}{2}V_c^{\Delta k} - \frac{V_s^{refk}}{V_d}V_c^{\sum k} \tag{4.23}$$

Then, by merging 3.33 and 4.23 with two of the state equations 3.27 and 3.29, then this new equation can be linearized in the frequency domain with the assumptions from 4.11, 4.12 and 4.13, giving

$$A_{vc}\tilde{V}_g^k(s) + A_{ic}\tilde{I}_s^k(s) - A_{cc}\tilde{I}_c^k(s) = 0 \tag{4.24}$$

where A_{vc}, A_{ic} and A_{cc} is given by

$$A_{vc} = 2 - \frac{N[k_f - H_v(s)]I_c^{ref}}{C_m V_d s} + \frac{Nm[k_f - H_v(s)]I_{s0}e^{j\phi}}{2C_m V_d s} - 2[k_f - H_v(s)] \tag{4.25}$$

$$A_{ic} = sL_m + R_m + \frac{N}{4C_m s} + \frac{Nm^2}{4C_m s} \tag{4.26}$$

$$A_{cc} = \frac{Nm}{C_m s} \tag{4.27}$$

Where m is the modulation index which is

$$m = 2\frac{\hat{V}_g}{V_{dc}} \tag{4.28}$$

where the hat on $\hat{V}_g$ indicates peak value, I_{s0} and ϕ is the amplitude and the initial angle of the output current I_s. According to [38], can the perturbation circulating current be represented by the perturbation circulating current second order harmonic component $\tilde{I}_{c2}^k$ if the perturbation dc current is ignored.

$$\tilde{I}_c^k(s) \approx \tilde{I}_{c2}^k(s) \tag{4.29}$$

And by modeling the the dc side capacitor as a constant dc source the second order circulating current can be calculated accordingly

$$\tilde{I}^k_{c2}(s) \approx A_{cc2}\tilde{I}^k_c(s) \approx \frac{\frac{3m}{8(s-j\omega)}}{\frac{4C_m}{N}(2L_m(s-j\omega)+R_m)+\frac{6+4m^2}{12(s-j\omega)}}\tilde{I}^k_c(s) \tag{4.30}$$

By substituting the 4.30 into 4.24 the ac side impedance of the HVDC side MMC can be obtained as

$$Z_{MMCc}(s) = \frac{A_{ic} - A_{cc}A_{cc2}}{A_v c} \tag{4.31}$$

To evaluate the stability of the MMC without circulating current control is the impedance model evaluated in a bode plot in 4.8. What is worth noting for this response is that there are two resonant peaks at 23.8Hz and 76.4Hz. When finding the impedance model phase margin and gain margin, it is observed that they are located at almost the same frequency, which is the fundamental. And that they are relatively small, 19dB and 19°. It is also noted 0dB is crossed several times around where the bode phase plot crosses the 180°-line. This indicates that the MMC without circulating current controller is unstable.

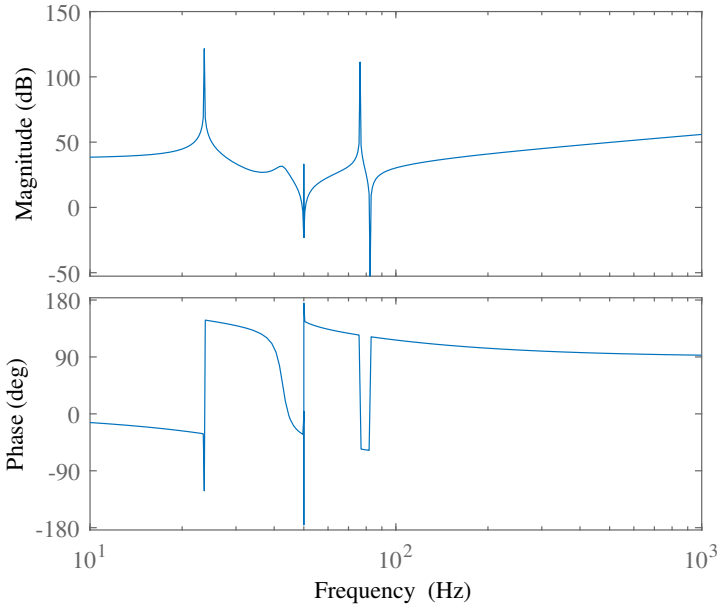


Figure 4.8: MMC without circulating current control bode plot

Direct Modulation With Circulating Current Control

By substituting 3.27, 3.29, 3.33 and 3.35 into 4.22 for then to apply linearization in the frequency domain, the result is

$$A_v\tilde{V}_g^k(s) + A_i\tilde{I}_s^k(s) + A_c\tilde{I}_c^k(s) = 0 \tag{4.32}$$

where,

$$A_v = 2 - \frac{2N[k_f - H_v(s)]I_c^{ref}}{C_m V_d s}\left(\frac{1}{2} - \frac{R_m I_c^{ref}}{V_d}\right) + \frac{Nm[k_f - H_v(s)]I_{s0}e^{j\phi}}{2C_m V_d s} - 2[k_f - H_v(s)] \tag{4.33}$$

$$A_i = sL_m + R_m + \frac{N}{C_m s}\left(\frac{1}{2} - \frac{RI_c^{ref}}{V_d}\right)^2 + \frac{Nm^2}{4C_m s} \tag{4.34}$$

$$A_c = \frac{N}{C_m s}\left(\left(\frac{[H_c(s) - R_m]I_{s0}e^{j\phi}}{V_d} - 2m\right)\left(\frac{1}{2} - \frac{R_m I_c^{ref}}{V_d}\right) - m\frac{H_c(s)I_c^{ref}}{V_d}\right) \tag{4.35}$$

The purpose of the circulating current controller is to suppress the circulating current during steady state. [38] Therefore, can the MMC impedance model be expressed as

$$Z_{MMC}(s) = -\frac{\tilde{V}_g^k(s)}{\tilde{I}_s^k} = \frac{A_i}{A_v} \tag{4.36}$$

in the frequency domain. The system impedance response is presented in 4.9. By comparing the bode plot of the MMC with circulating current control to the bode plot in 4.8, of the MMC without circulating current control, it is clear that the resonant peaks at 20 and 70Hz are suppressed due to internal damping provided by the circulating current controller. As this system response does not cross the -180° line, the MMC with current control is considered stable, but with a low impedance phase margin of 6.3°.

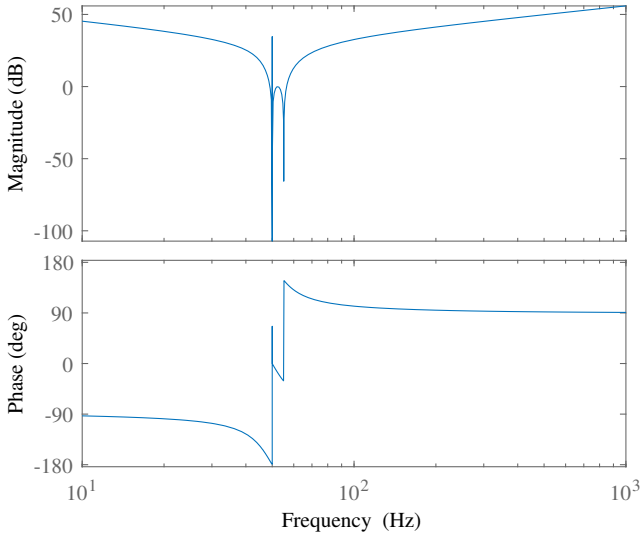


Figure 4.9: MMC with circulating current control bode plot

4.2.3 Cable and Transformer Impedance

As a large amount of ac power is transferred from the WF Inverter to the HVDC side will passive components influence the power. A model of these components is illustrated in 4.10. As can be seen, the model is constructed with two transformers. The first transformer T_1 increase the voltage from V_w 690V to V_c 50kV and the second T_2 from 50kV to V_r 166kV. Both of these transformers are implemented with a resistance $R_{Tnp,s}$ of 0.005pu and inductance $L_{Tnp,s}$ of 0.001pu on primary p and secondary s side, where n indicates which transformer. These transformer parameters have to be considered when calculating the impedance of the system.

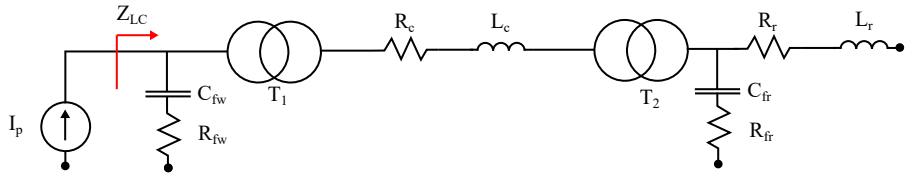


Figure 4.10: Single line diagram of cable passive components with transformers

A small perturbation current is sent from the WF Inverter side. The ac parameters that influence this current are all moved to the low voltage side of the transformers. Transformer 1 and two turns ratio T_{a1} and T_{a2}, respectively are

$$T_{a1} = \frac{V_c}{V_w} \tag{4.37}$$

$$T_{a2} = \frac{V_r}{V_c} \tag{4.38}$$

The mid voltage impedance Z_c can be transferred to the low voltage side in the frequency domain accordingly

$$Z_c' = \frac{R_{T1p} + sL_{T1p} + R_c + L_c + R_{T2s} + sL_{T2s}}{(T_{a1})^2} \tag{4.39}$$

Where apostrophe $'$ specifies that the impedance is shifted to the secondary side. The HVDC side impedance Z_r of the LC filter becomes

$$Z_r' = \frac{R_{T2p} + sL_{T2p} + (\frac{(R_r+sL_r)^{-1}+(R_{fr}+\frac{1}{sC_{fr}})^{-1}}{})^{-1}}{(T_{a1} + T_{a2})^2} \tag{4.40}$$

Where the filter impedance is marked with an f. Where the denominator is both transformer 1 and 2 turns ratio, as the impedance has to be moved across both transformers. The ac impedance on the WF Inverter side Z_{LC} then becomes

$$Z_{LC}' = \left((R_{fw} + \frac{1}{sC_{fw}})^{-1} + (R_{T1s} + sL_{T1s} + Z_c' + Z_r')^{-1}\right)^{-1} \tag{4.41}$$

The frequency response of the filter is

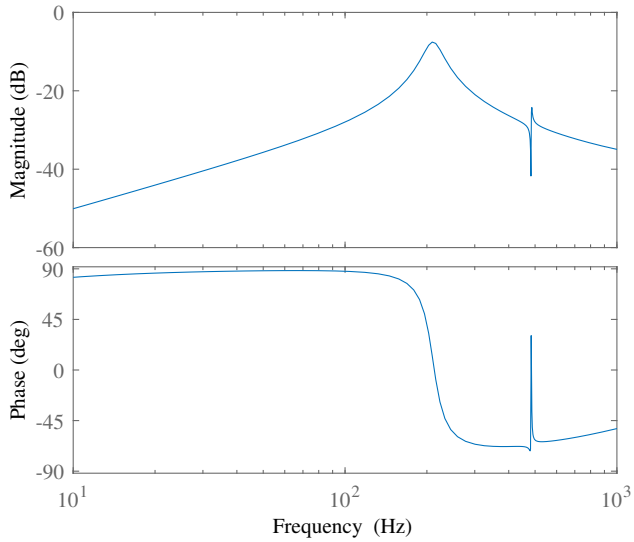


Figure 4.11: The frequency response of the passive components.

The frequency response show that the passive components are stable for all suspected power outputs.

4.2.4 Full System Impedance Stability

To analyze if the WF Inverter and HVDC system is stable when connected together, they are evaluated in an open loop. As there are transformers separating the WF Inverter and HVDC systems, it will be necessary to do a transformation, so the systems operate on the same side of the transformers. As the resistive components are transferred to the low voltage side in the previous section, it is less complicated to also transfer the HVDC to the low voltage side. This is done by dividing the impedance of the MMC by the turns ratio squared, accordingly

$$Z'_{MMC} = \frac{Z_{MMC}}{(T_{a1} + T_{a2})^2} \tag{4.42}$$

The bode plot of an interconnected WF Inverter-HVDC system is presented in 4.12. The frequency response of the MMC is a little different than the frequency response in 4.9, due to the change in impedance across transformers. [38] presents the criterion that the interconnected system is stable if the WF MMC is always smaller then the VSC impedance. The bode plot confirms that this is the case, which means that for normal operating conditions, this interconnected system is stable.

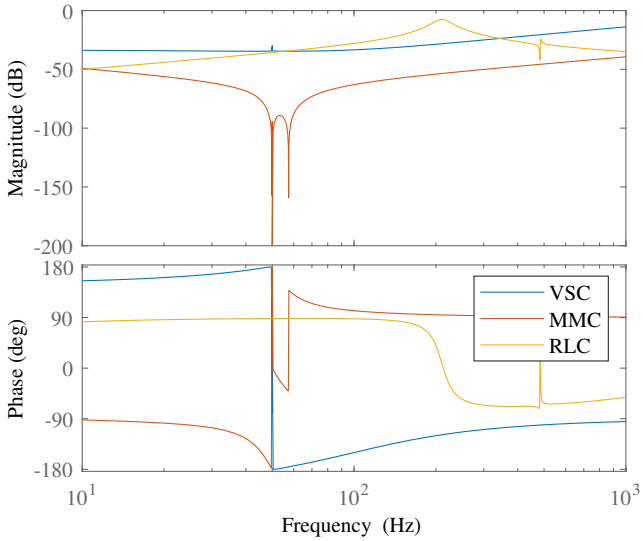


Figure 4.12: The frequency response comparison of the VSC, MMC and the passive RLC components in the ac system for 50MW

The total system impedance Z_{tot} is found by combining 4.18, 4.36, 4.37, 4.38 and 4.41 in 4.2. Then the total system impedance becomes

$$Z_{tot} = \frac{Z'_{MMC}}{Z_W + Z'_{LC}} \tag{4.43}$$

To evaluate how well the system operates, it has also been tested for 10MW. First frequency response has been tested in 4.13. By comparing the frequency response to the test for 50 MW in 4.12 show that none of the components are very much influenced by this change. The bode plot also proves according to the assumption from [38], that interconnected system is stable for 10MW. The WF Inverter-HVDC system will be tested in the time domain to make sure that the results found in this section are accurate.

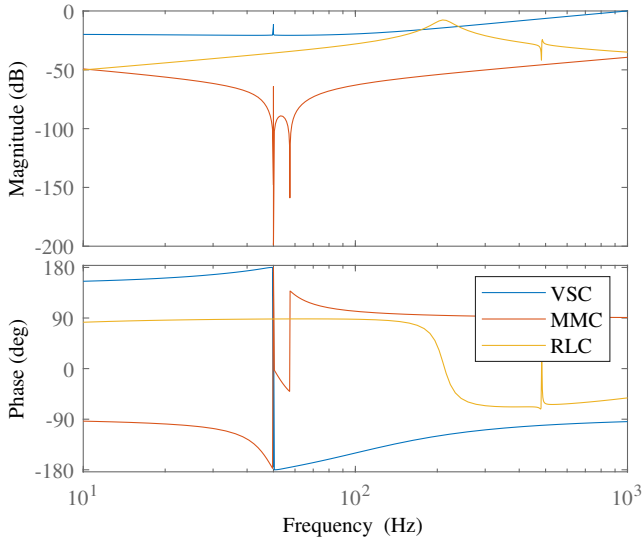


Figure 4.13: The frequency response comparison of the VSC, MMC and the passive RLC components in the ac system for 10MW

Chapter 5

Simulation Result of Interconnected Wind Farm-HVDC System

This chapter will present the results obtained from Matlab Simulink. The model is, of course, based on theory and values presented in Chapters 2 and 3. The Simulink model will be tested for a total of four cases. In the first case, the WF Inverter-HVDC system is tested to see if its capable of producing 50MW and 10MW when the MMC does not contain a circulating current controller. In the second case, the system is tested for the same thing, but this time will the MMC contain a circulating current controller. To establish what is the source of harmonic oscillations in the system, the third and fourth case are that each converter will be connected in an isolated grid. What this means is, that the WF Inverter will be connected directly to a strong grid, that is not influenced by a single power source, as presented in 2.3. This can be done simply in Simulink by connecting the converter to an ”ac voltage source”-block. Then the converter will be set to deliver 50MW and 10MW. The HVDC system does the job of setting the ac side voltage. Therefore, the MMC is connected to a load that draws 50MW and 10MW. This means that the power flow happens in the opposite direction, but as discussed in 3 should this not be a problem for a half-bridge MMC.

The VSC is simulated with the parameters from 2.1 and 2.2. The MMC with and without circulating current control is simulated with the parameters from 3.1 and 3.2 The tests are performed accordingly:

For the first 0.15 seconds, the MMC is turned on alone to generate a stable ac power throughout the system. At 0.15 is the PLL turned on to synchronize to the MMC ac voltage without the VSC influencing the system. At this time, none of the VSC switches are conducting current, and the inverter only delivers power through its diodes. That means that the converter operates as a diode inverter, and there is no active control over the current delivered by the WF side. After 0.3 seconds, the VSC current controller is turned on. This is done by the synchronous reference direct current component being set to 1pu,

which makes the VSC deliver 50MW to the grid. 0.1 seconds after the current controller is turned on, and the inverter delivers a stable output to the grid. The first measurements of the WF Inverter and HVDC voltage and currents are taken to analyze the result. At 0.6 seconds after the MMC is turned on for the first time, and the direct current reference is changed to 0.2pu. This makes the VSC deliver 10MW to the grid. 0.2 seconds later the output is considered stable, and the second measurement is taken to analyze power quality and stability.

The isolated cases are also set to the same references at the same time to best compare the connected and isolated cases.

5.1 Case 1: WF Inverter-HVDC Without Circulating Current Control

The global graph in 5.1a show that the MMC without circulating current control is unable to set a stable ac voltage for zero, 10MW and 50MW. This will not allow the PLL to synchronize to anything which will make the power flow unstable, which can be seen in the current flow presented in 5.1b.

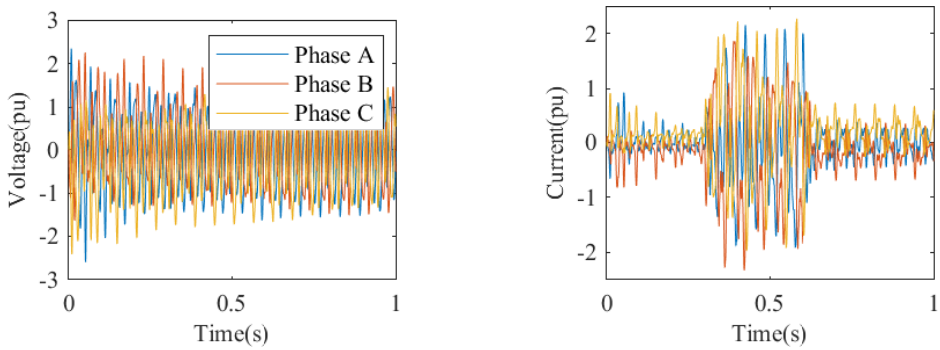


Figure 5.1: Three Phase HVDC side voltage and current in pu for MMC without Circulating Current Control. a) Voltage and b) Current

5.2 Case 2: WF Inverter-HVDC With Circulating Current Control

The time domain response of both the 10MW and 50MW simulation are presented in the following figures. 5.2a and 5.2b show the global voltage and current waveforms on the HVDC side. Just by looking at these figures, it becomes clear that stability has improved significantly. Later, figures will show that the converter system is able to operate in steady

state, which agrees with the conclusion from the previous chapter that the system would be stable for both 50MW and 10MW.

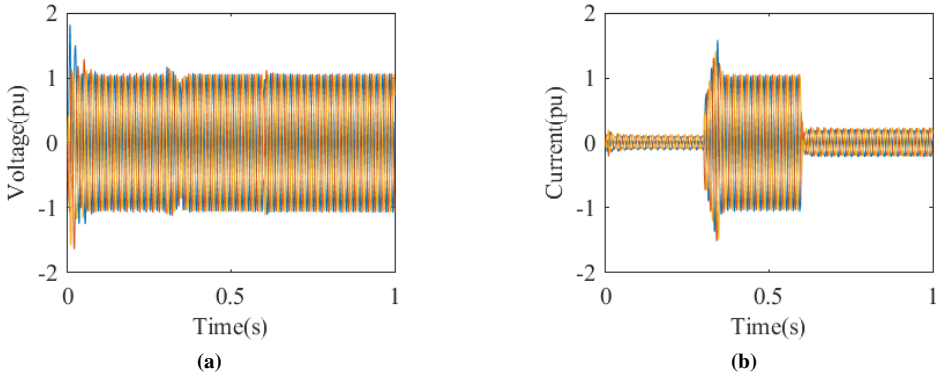


Figure 5.2: Three phase HVDC side voltage and current in pu for MMC with Circulating Current Control. a) Voltage and b) Current

5.2.1 Case 2: 50MW Case

The active and reactive power output of the WF Inverter is shown compared to the reference values in 5.3. The figure shows that the converters are able to deliver the desired output after a couple of milliseconds. As the control systems settle, there is some overshoot of both active and reactive power. The figure shows that the system delivers a stable power output after 0.4 seconds, which is why future voltage and current measurements are taken after 0.4 seconds.

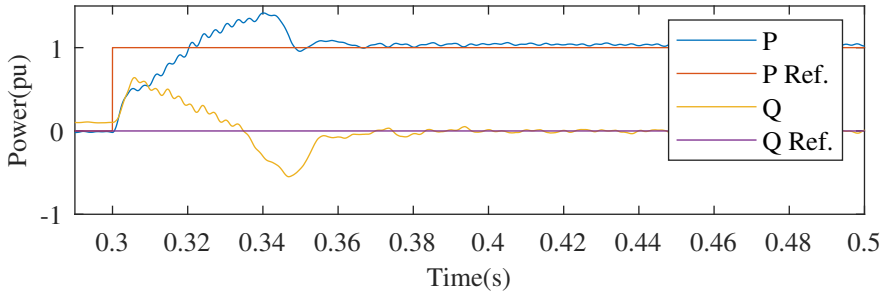
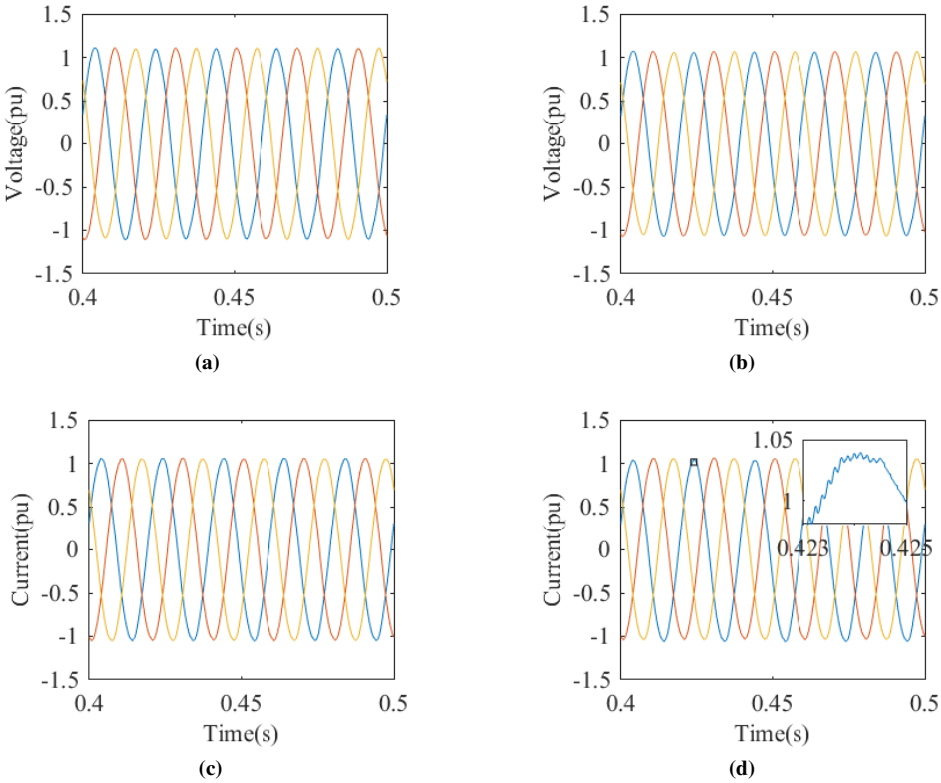


Figure 5.3: Active and reactive output power for 50MW case

5.4a to 5.4d shows the voltage and current waveforms on the ac side of the two converters. 5.4a and 5.4b show that the ac voltage is a little more than 1pu. The current from the WF Inverter to the HVDC side is presented in 5.4c and 5.4d. The second figure shows that there are some small-signal subsynchronous oscillations in the current. These ripples are very well documented in the literature and have been observed in real life. [1],[38],

[52] According to [1] one reason for these harmonics are interactions between the WF Inverter and HVDC controllers and interconnected system impedance. But both [1] and [52] clearly states that the root cause of these oscillations is not clearly understood. It becomes clear when studying the power output in 5.3 that there are some oscillations influencing the power quality. Another way of evaluating power quality, than by looking at the waveforms, is to do an FFT analysis. FFT analysis will generate the THD of a waveform. FFT analysis is easily applied in Simulink by using the integrated FFT analysis in the ”powergui”-block. The result of the FFT analysis for the HVDC side current and voltage waveform is presented in 5.4e and 5.4f. The figures show what type of HDs that are influencing the waveforms.



(a) **(b)** **(c)** **(d)**

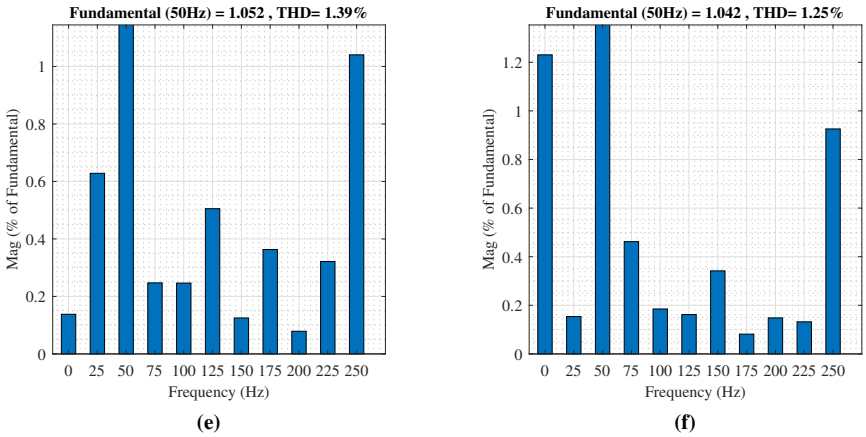


Figure 5.4: For 50MW case. a) WF Inverter voltage b) HVDC voltage c) WF Inverter current d) HVDC current e) THD HVDC Voltage f) THD HVDC Current

5.2.2 Case 2: 10MW Case

D-reference value is changed to make the VSC deliver less power to the grid. The power output result is presented in 5.5. As the figure shows is there an instantaneous drop to 10MW output. 5.6a and 5.6b illustrates that the voltage do not change as the power output drops. This means that the MMC, which controls the voltage, is able to set the ac voltage at a node for a large variety of power ratings. 5.6c and 5.6d show that the current output decreases to 0.2pu, which means that the output power is controlled only by the current controller. The current controller is more influences by harmonics for "smaller" power outputs ($<$ 10MW). The harmonic distortion in 5.6e and 5.6f shows an increase in THD for both voltage and current. Of course, it is the current that experiences the biggest increase, with a new THD of more than 4.5%. It is likely that the large amounts of THDs are the reason why the voltage also experiences harmonic increase. Because the MMC control system is dependent on the circulating current control. For a case where the output current is unstable, can this influence the circulating current. 5.6f also show that the current contains a large amount of dc harmonics.

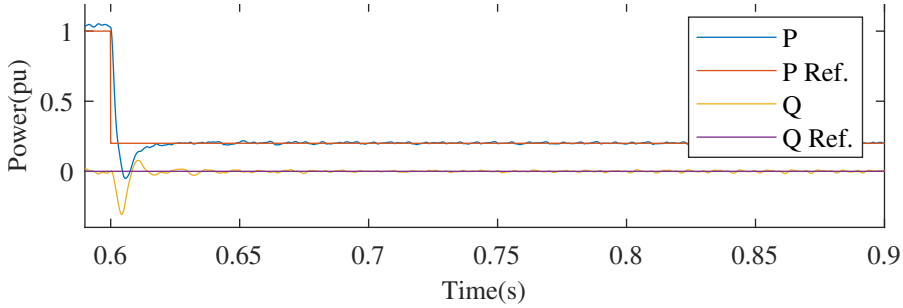
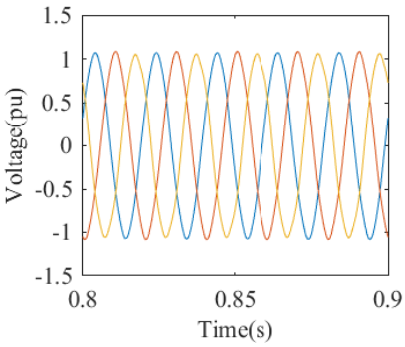
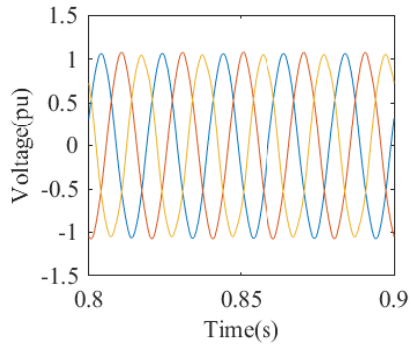


Figure 5.5: Active and reactive output power for 10MW case



(a)



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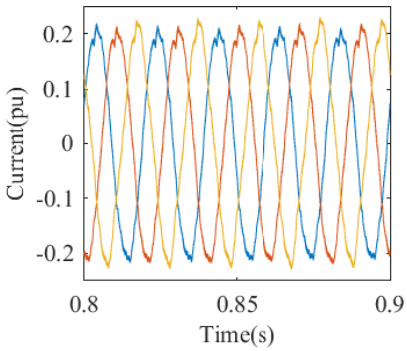
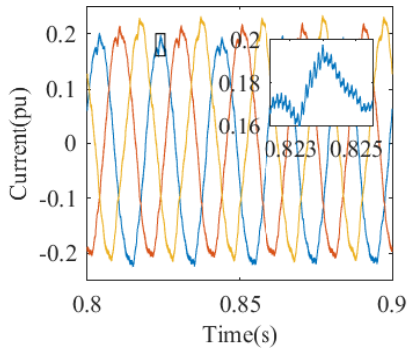


(c)



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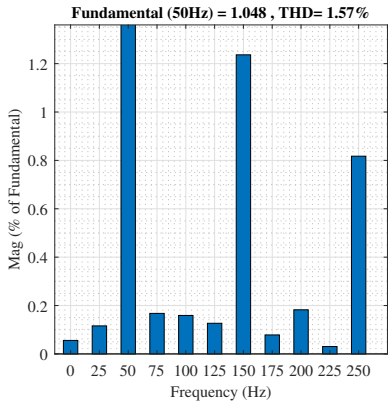
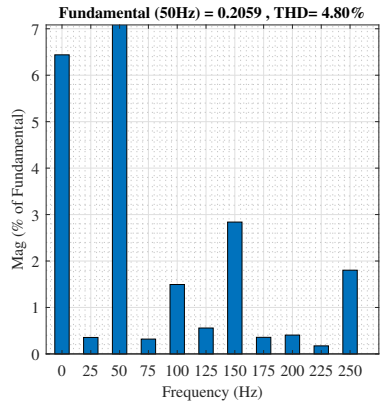


(e)

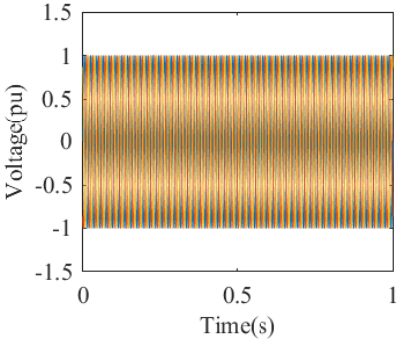


(f)

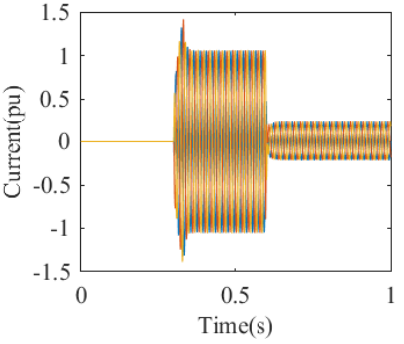
Figure 5.6: For 10MW case. a) WF Inverter voltage b) HVDC voltage c) WF Inverter current d) HVDC current e) THD HVDC Voltage f) THD HVDC Current

5.3 Case 3: WF Inverter Isolated Case

For the WF Inverter isolated case, the ac side voltage is set by a constant ac voltage source. This case will show how the VSC operates when it is connected to a stiff grid, which could be the case for some wind farms. The figures in 5.7a and 5.7b show the voltage and current for the WF Inverter. These figures show that the VSC is capable of delivering a stable current flow to the grid, but to evaluate if the power quality has improved it is necessary to look closer at the current.



(a)



(b)

Figure 5.7: Three phase isolated WF Inverter side voltage and current in pu for VSC. a) Voltage and b) Current

5.3.1 Case 3: 50MW Case

5.8 show the power flow from the WF Inverter to the grid. The result shows that the current controller reaches steady state after approximately 0.06 seconds. The figure also shows that the active power output is uncompensated, which, according to [10], can be improved by changing the PI parameters.

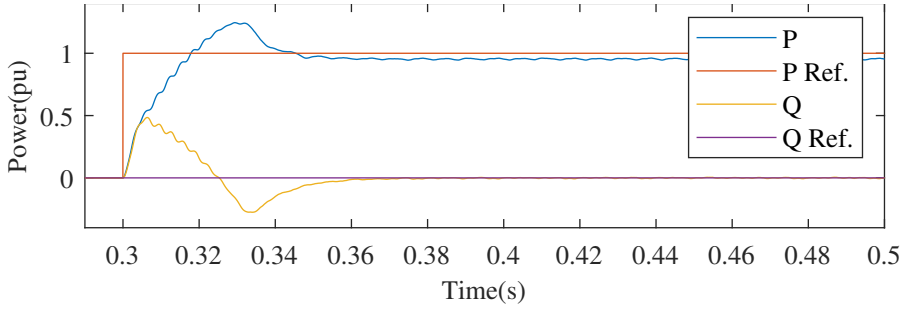
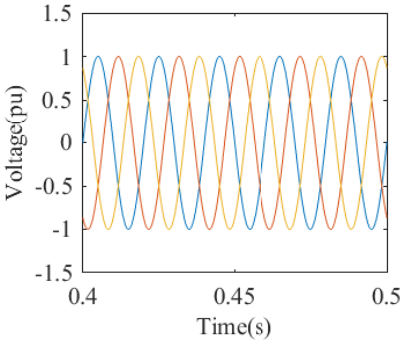
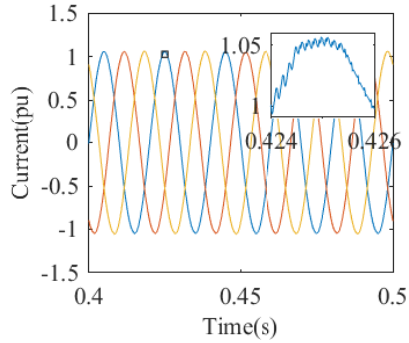


Figure 5.8: Active and reactive output power for 50MW isolated case

5.9a and 5.9c show that the voltage from the ac voltage source is perfectly sinusoidal without any harmonics. 5.9b show the current from the delivered to the grid by the VSC. The figure shows that the current delivered is more than what is expected. The current waveform also has higher order harmonics, which can be studied closely in the HD figure in 5.9d.



(a)



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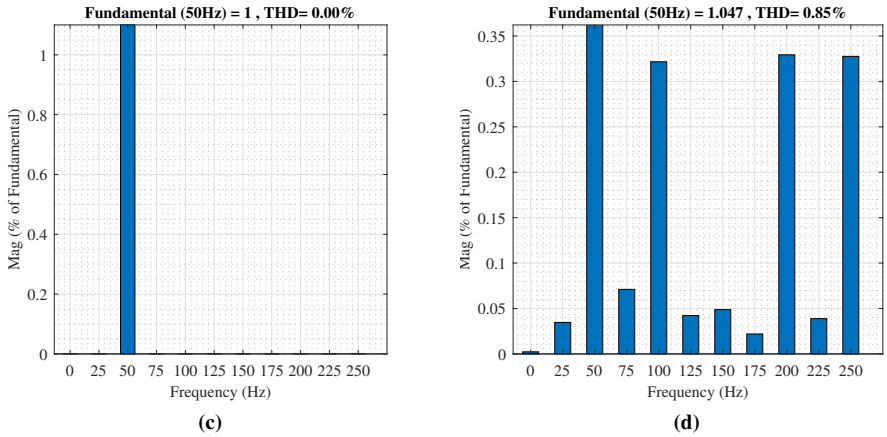


Figure 5.9: For isolated 50MW case. a) WF Inverter voltage b) WF Inverter current c) THD WF Inverter Voltage d) THD WF Inverter Current

5.3.2 Case 3: 10MW Case

Now the reference current has been lowered, and the power output presented in 5.10 changes immediately. The converter is able to deliver the required power to the grid without much steady state error.

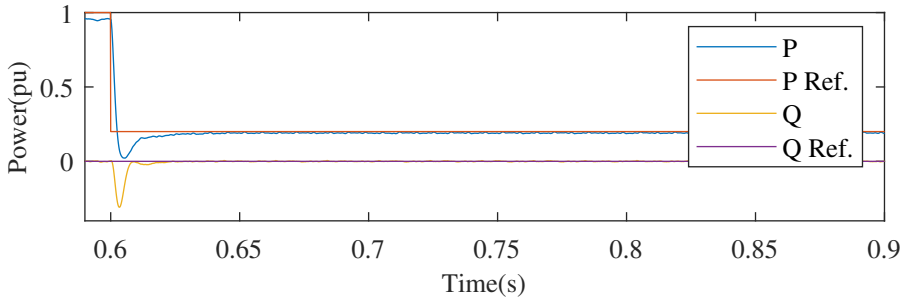


Figure 5.10: Active and reactive output power for 10MW isolated case

5.11a and 5.11c again show stable grid voltage. 5.11b show that the

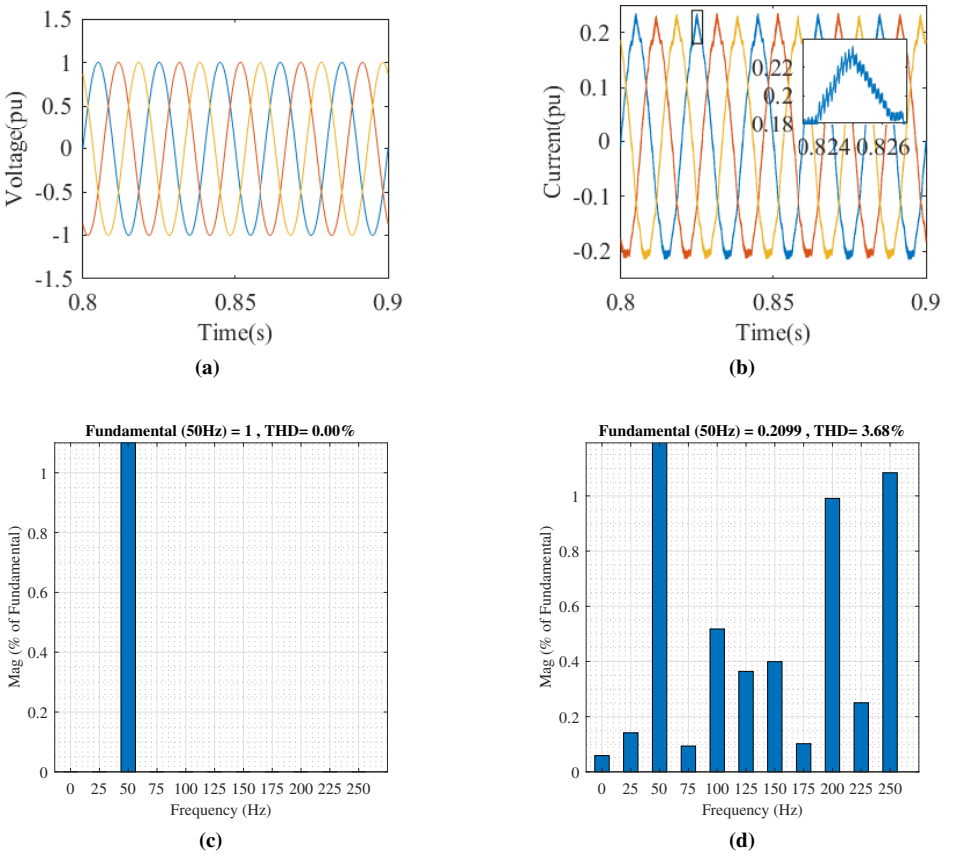


Figure 5.11: For isolated 10MW case. a) WF Inverter voltage b) WF Inverter current c) THD WF Inverter Voltage d) THD WF Inverter Current

From the previous cases, it seems as if HD increase as the power output for the VSC decreases. In 5.12, the fundamental current waveform for 50Hz is subtracted from the output current. This is done, so the only frequencies left is that of the HD. What is made clear during this operation is that the amount of HD in the current waveform almost remains constant. And that the HD increase only because of the magnitude of the fundamental frequency decrease.

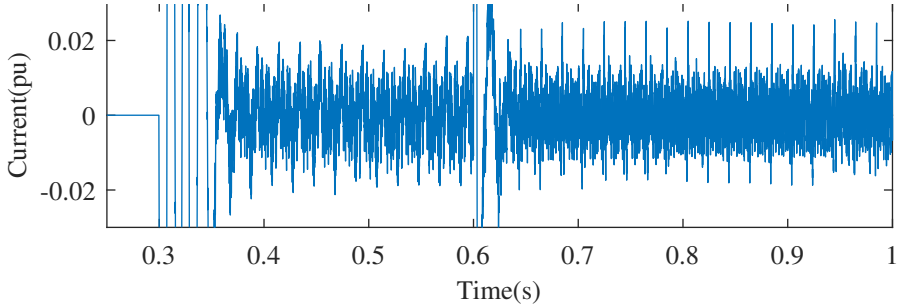


Figure 5.12: WF Inverter current noise for 50MW and 10MW in phase a

5.4 Case 4: HVDC Isolated Case

5.13a and 5.13b show the HVDC side voltage and current, respectively when the HVDC system operates as an isolated network. The MMC ac voltage controller decides the ac voltage. A changing load decides the ac current, and its waveform is dependent on the ac voltage. This section will show how the HVDC system operates independently from the WF Inverter.

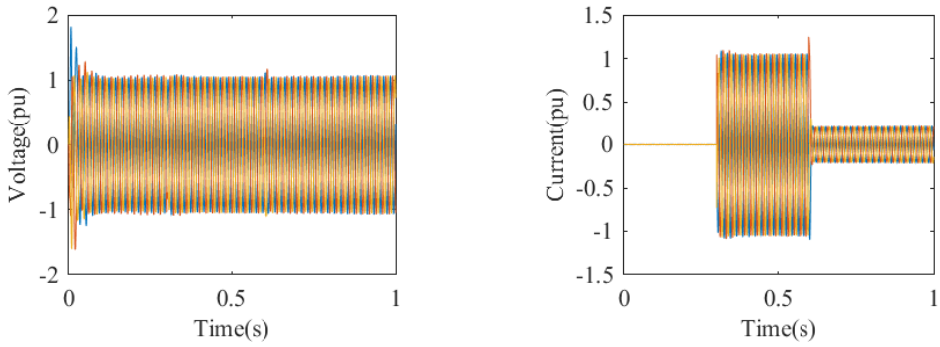


Figure 5.13: Three phase isolated HVDC side voltage and current in pu for MMC. a) Voltage and b) Current

5.4.1 Case 4: 50MW Case

For the 50MW case power is drawn from the dc side to the ac side. Power flow is shown in 5.14 which illustrate that the power is flowing opposite to the other cases. The power flow figure show that the power delivered to the load has lower overshoot than the other cases and stabilize after 0.05 seconds.

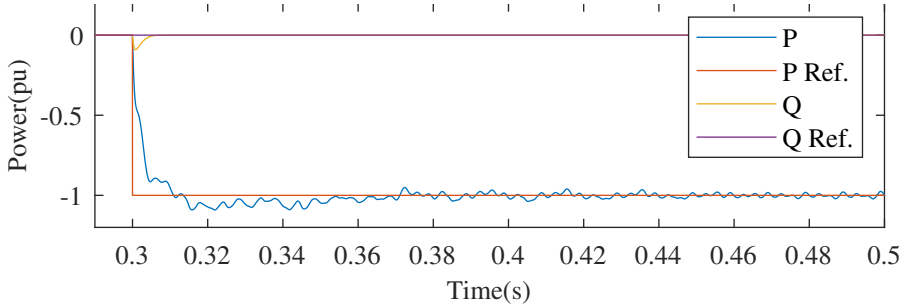
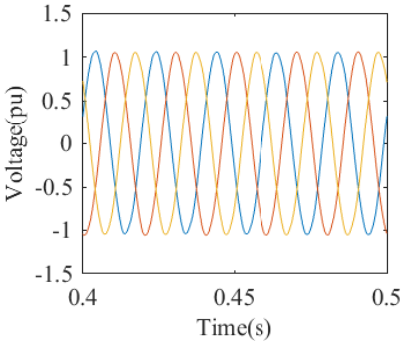
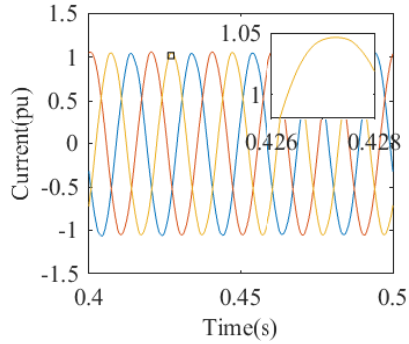


Figure 5.14: Active and reactive output power for 50MW isolated case

5.15a and 5.15b show the HVDC voltage and current, respectively for the isolated 50MW case. The figures show what looks like almost perfectly sinusoidal waves with low HD. 5.15c and 5.15d reveal that the HD is identical for the voltage and current waveforms. This is as expected as the load is considered to not produce any noise to the system, with a magnitude set by the load impedance and ac voltage and a waveform that follows the ac voltage.



(a)



(b)

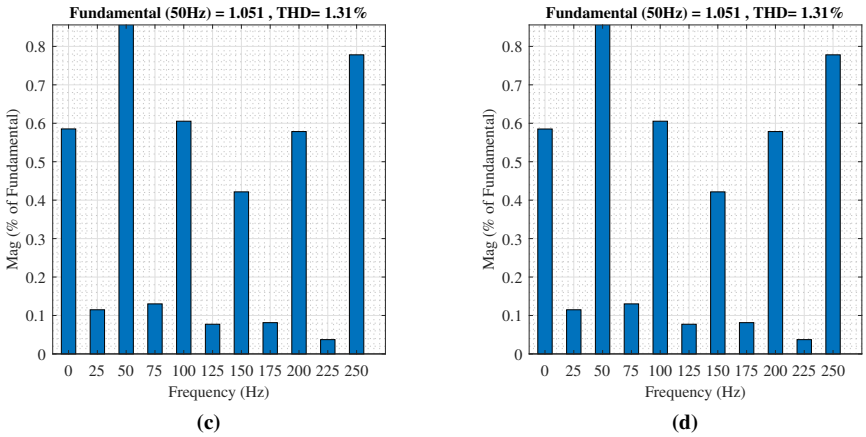


Figure 5.15: For isolated 50MW case. a) HVDC voltage b) HVDC current c) THD HVDC Voltage d) THD HVDC Current

5.4.2 Case 4: 10MW Case

The power delivered to the load from the HVDC system is changed by changing the load impedance. The active and reactive power result of changing the load impedance is presented in 5.16. It is observed the load draws stable power from the dc side after approximately 0.2 seconds.

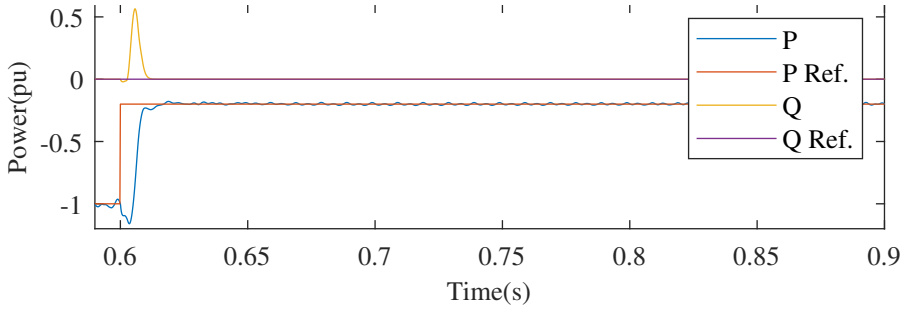


Figure 5.16: Active and reactive output power for 10MW isolated case

5.17a and 5.17b show the HVDC voltage and current, respectively for the isolated 10MW case. Again it can be seen in 5.17c and 5.17d that the noise in the current waveform is fully dependent on the ac voltage.

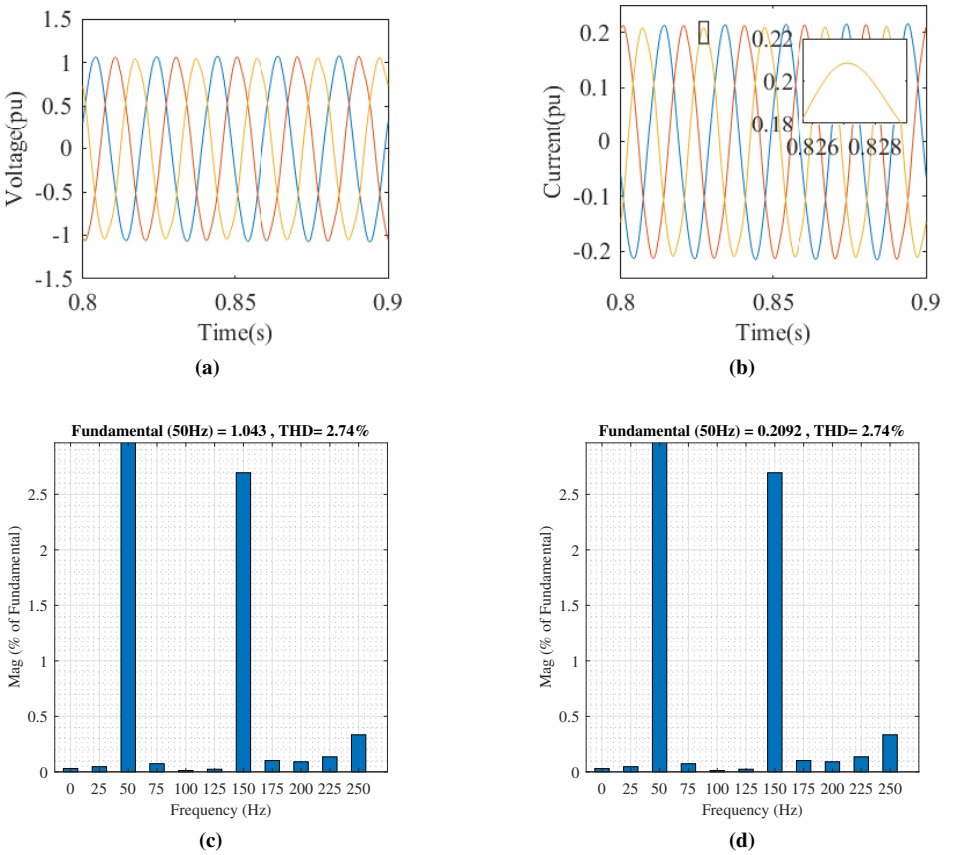


Figure 5.17: For isolated 10MW case. a) HVDC voltage b) HVDC current c) THD HVDC Voltage d) THD HVDC Current

5.5 Wind Farm Inverter controller system analysis

5.5.1 Impact of Phase Locked Loop

The importance of a good PLL can not be overstressed. The point of the PLL is to obtain the synchronous frequency, which is used through the whole VSC. 5.18 shows the system response of the PLL for the interconnected system with circulating current control case (case 2). The PLL is turned on after 0.15 seconds. It can be seen that the PLL has an overshoot of more than 100%. As the simulation result shows that the PLL reaches a steady state after 0.05 seconds. When the current controller gets turned on, there is some uncontrollable ripple. But after 0.1 seconds are this ripple turned into a stable output with 50 ± 1 Hz, as can be seen in the additional square in 5.18. The PLL simulation response shows that the PLL is able to reach within 2% of the reference value after 0.1 seconds. It is likely that some of these ripples occur due to the ac voltage ripple. The first order low pass

filter of the PLL is set to 500 Hz cut of frequency, which will reduce high order harmonics in the system.

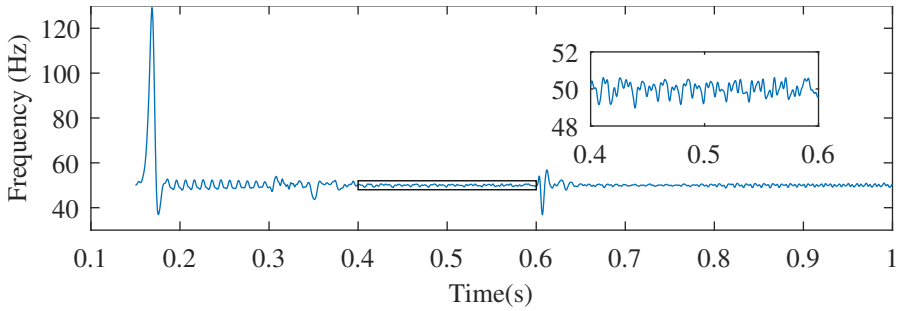


Figure 5.18: PLL time response for interconnected system

5.19 show the PLL time response for the isolated WF Inverter case (case 3). What separates this PLL response from that in case 2 is that the PLL is connected to a stiff grid, that is not influenced by a change in power output. The show that the high overshoot in the start up for the PLL is a result of the PLL tuning. After the PLL reaches steady-state it will produce a stable output with no noticeable ripple. 5.19, therefore, proves that the PLL time response noise is due to the PLL voltage reference noise and no noise produced by the PLL controller. A conclusion can be drawn that the PLL output will improve automatically if the grid voltage becomes stable.

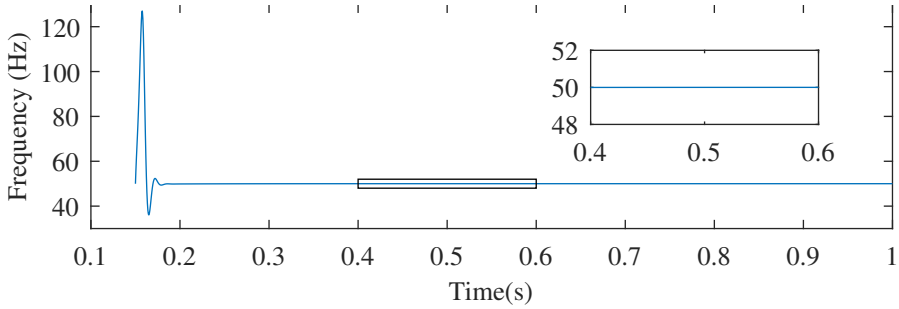


Figure 5.19: PLL time response for isolated case

5.5.2 Impact of VSC Current Controller

To makes sure that the VSC current controller is operating properly, the dq current signal in the control system, for case 2, is measured compared to its reference values. The current component is presented in per unit and is illustrated from the controller is turned on, until one second has passed. The result is presented in 5.20. The figure shows that the controller can generate a fast responding signal with a very small margin of error in steady state. By changing the reference value from first a large value to a smaller output, it is proven that this type of controller can control the power delivered WF Inverter.

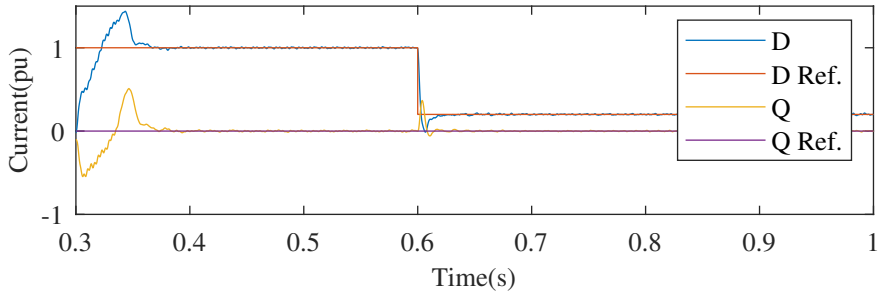


Figure 5.20: DQ current in controller for interconnected system

5.21 show the dq current for the case 3. By comparing the dq current from cases 2 and 3, it is observed that the improvement by having a stiff grid is minimal. The response shows that the 50MW power steady state error is between $\pm 1\%$. This steady state error is close to what we can observe for the interconnected system in case 2.

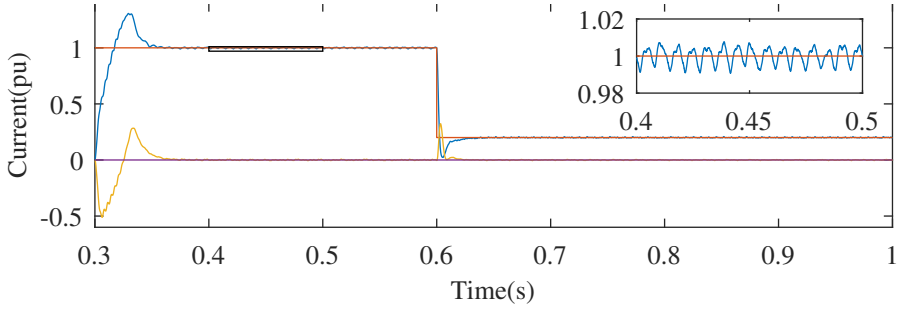


Figure 5.21: DQ current in controller for isolated case

5.6 HVDC Controller System Analysis

5.6.1 AC Voltage Proportional Resonant Controller

The control system consists of two PR controllers, a circulating current controller and an ac voltage controller. The circulating current controller takes in a three-phase sinusoidal signal generated by a Sine Wave block in Simulink. The purpose of the sine waves are to set the reference for the circulating current in each leg. The reference signal is phase shifted by 120 degrees with a frequency of twice the fundamental angular frequency. Upper and lower leg current is measured in each of the three phases, then the currents are summed and divided by two to calculate the phase circulating current. The calculated circulating current is compared to its reference value and the error is sent trough the circulating current PR controller. A feed forward gain is implemented to compensate for the voltage drop across the parasitic resistance. The output of the PR controller and the feed forward gained are summed up to produce the voltage inducing the circulating current.

The circulating current voltage is used to calculate the insertion index in upper and lower leg for each phase.

There are three ac voltage controllers, one for each phase. The purpose of the controller is to generate a voltage output that matches the grid voltage. This is achieved according to 3.32. The reference ac voltage signal is generated the same way as for the circulating current controller. The ac voltage measurements are in Simulink taken after the LC filter has influenced the ripple. Measuring voltage to close to the MMC can result in high order frequency harmonics, which, if not filtered out, can make the controller unstable. As the reference output voltage of the converter becomes close to the reference value, the output of the PR controller becomes small compared to the feed forward therm. 5.22 show the output of the PR controller during steady state. The figure shows that the controller has an output of approximately $\pm 0.25pu$, which indicates that the system has some offset even though the grid voltage curve is similar to its reference value.

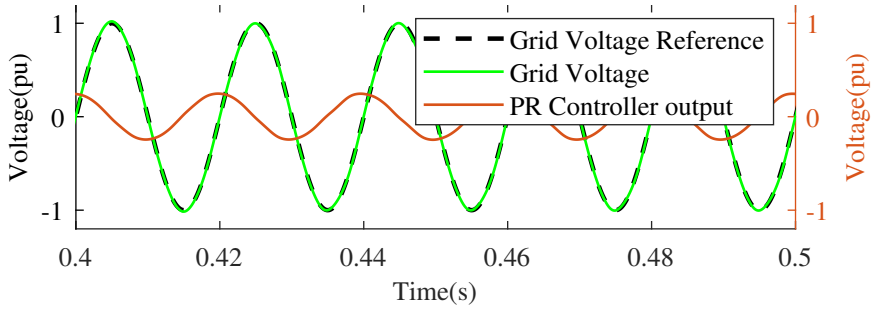


Figure 5.22: Left axis is output voltage reference and output voltage, and right side is PR controller output

5.6.2 Half-bridge Signal and Converter Voltage

3.17 and 3.18 are the two equations used to generate the insertion index for the direct modulation control. For both equations, the numerator are divided by the dc side voltage. The numerators consist of a constant value of upper and lower dc side voltage. According to 3.3 are upper and lower dc voltage half of the total dc voltage. The output voltage and circulating current voltage, are oscillating sine waves, which means that the average insertion index value will be 0.5. Alternatively, in other words, the insertion index will oscillate between 0 and 1. This is very important when deciding on a PWM techniques, as some methods assume average value of zero with oscillations from -1 to 1. [53] 5.23 show the the insertion index and sum of the on signals sent to a phase upper arm SM during full operation mode (i.e. v_s^{ref} = 1pu). This summation of signals is one way to make sure that the PWM is working properly. Note that the insertion index does not reach 0 and 1, which means that the model does not produce at optimal capacity. This also makes so the arm is constantly conducting current. This can, if inaccurate voltage balancing or certain PWM techniques are chosen, mean that the SMs are only bypassed. An example of this is if level shifted PWM is used as, presented in [53], the insertion index will never cross the upper triangular waveform, which generates a constant bypass signal to the SM.

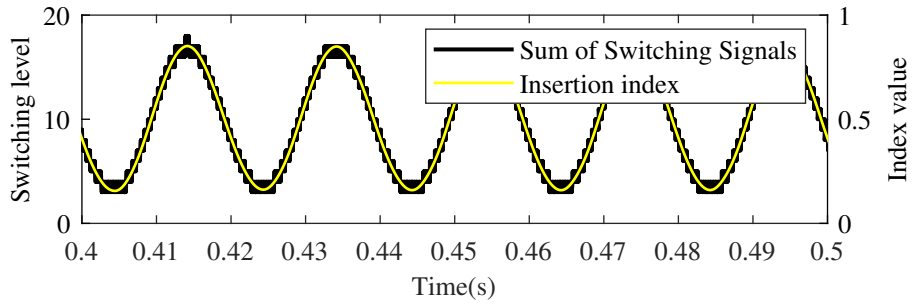


Figure 5.23: Sum of switching signals left hand side and insertion index right hand side in upper arm phase a.

Phase shifted triangular waveforms are for this 20 SM MMC phase shifted by 360/N = 18°. The phase shifted triangular PWM is implemented for this model as it is a technique that divides the on-off time equally among all SM. 5.24 shows that the voltage across the capacitors is approximately equal, which backs up the previous statement. 5.24 also show that the voltage deviation across the capacitors is relatively constant due to the large capacitance of each capacitor. The voltage sum of these capacitors is equal to the dc side voltage.

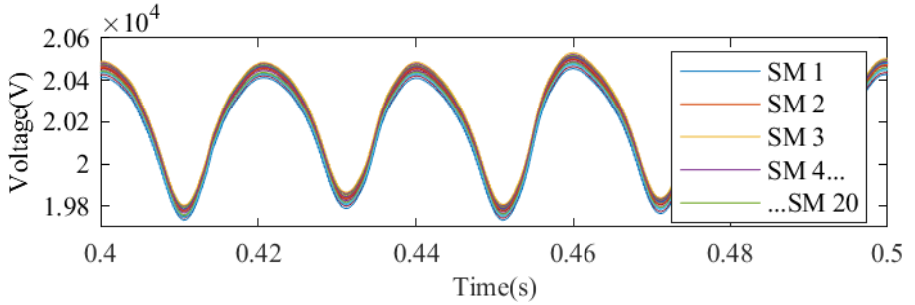


Figure 5.24: Voltage across each of the 20 capacitors in upper arm phase a.

5.6.3 Connecting Wind Farm Inverter and HVDC System

Two transformers are used to change the I-V ratio when transferring power from the WF Inverter to the HVDC system. It is assumed that the distance from one transformer station to the next is 10 kilometers. By increasing voltage and lowering current losses are expected to drop exponentially according to Ohm's law $P = ZI^2$. The WF Inverter side transformer increases the line-line voltage from 575V to 50kV. The HVDC side transformer increases the voltage from 50kV to 166kV.

Chapter 6

Discussion and Conclusion

This chapter will present a discussion around the result, and a final conclusion on WF Inverter-HVDC control strategy and harmonic distortion. The last section will present the authors thought on what can be done to improve the project.

6.1 Discussion

This thesis has presented a way of controlling an HVDC-WF Inverter conversion system, which is very appropriate today and in the future. The WF Inverter in the thesis is controlled with a current controller. It is deemed as unnecessary to us a dc voltage controller as it is possible to replace it with a constant dc voltage source. However, this is not the case if the voltage converter were to be implemented in a larger system where the power was delivered by turbines. So for an expanded system dc voltage control through the VSC is a viable option. Also, active and reactive power control is something that would be attractive to include, as that is presented frequently in literature. [54], [55] Due to time limitations an outer control is not included in the VSC.

There are presented three techniques for controlling an MMC, compensated modulation, direct modulation without circulating current control, and direct modulation with circulating current control. MMC with compensated modulation is, according to [38], very difficult to implement in real life systems, and is therefore only used as an analytical example. 4.7 show that the MMC will be stable with compensated modulation control, but with very small margins. The analytical result shows that an MMC can, in theory, be controlled with a single control loop. Direct modulation without circulating current control is tested for 50MW to see if the MMC can be controlled in direct modulation by a single control loop. The controller is tested both analytical in the frequency domain and simulated in the time domain. The main principle of direct modulation is that the circulating voltage is suppressed. The analytical response for direct modulation without circulating current control is presented in a bode plot in 4.8. In the bode plot, two resonant peaks for approximately 20Hz and 70Hz are observed. These resonant peaks will mean that noise sent through the controller with these frequencies will heavily impact the controller. The phase

margin for this controller is also small and is located at the fundamental frequency. The bode plot indicates that the direct modulation without circulating current control should not be stable at 50MW. To find out if this is indeed true is the MMC simulated in Simulink without circulating current control while connected to the WF Inverter. The time domain simulation gives the same answers, that for 50MW the MMC will not be able to produce a stable output. The time domain test also shows that the interconnected system without circulating current control is not stable for 10MW either.

Analytical and simulation-based tests are performed to study rather or not a circulating current controller can be implemented to improve stability the impedance model of an MMC controlled by direct modulation. The analytical result is presented in a bode plot in 4.9. This bode plot also indicates that the impedance model of MMC with voltage control has a very low phase margin around the fundamental frequency, which could cause instability. When the system is interconnected in 4.12 and 4.13 it is observed that the impedance ration for the MMC has changed. The interconnected system is considered stable for both 50MW and 10MW if each system is stable independently, and if the impedance ration for the MMC is smaller than the impedance ratio for the VSC at all frequencies. [38] The limitations for the analytical analysis in Chapter 4 is that the bode plot does not show stability margins of the interconnected system. To perform a stability margin analysis, the interconnected system could be tested according to the Nyquist criterion. A Nyquist plot would also reveal what HD distortion that could be expected from the converters. To ensure interconnected system stability, the poles of the converters should be mapped and compared to the result obtained from the Nyquist plots.

The WF Inverter and HVDC system is tested in four time domain cases. The first case, interconnected WF Inverter-HVDC system without circulating current controller, shows the importance of the internal dynamic control. The time domain results show that the system is unable to reach a steady state and produce a stable output. This reflects what is found in the analytical model.

Cases 3 and 4 show how the converters can be expected to change when the power output is reduced. 5.9d and 5.11d show that the HD is more influential for lower power output. An interesting observation is found in 5.12, which proves that the magnitude of the noise in the VSC does not increase when the power output is reduced. Rather, it is only the fundamental frequency that is lowered and therefore experiences a higher impact from the harmonics. For future work, it could be interesting to see the controller could be improved substantially by implementing specific harmonic order filtering. Now we have seen what can be expected from the VSC in a best-case scenario, case 4 show the same for the MMC. HD in the MMC shows that the system harmonic is only influenced by the voltage waveform. The 50MW case shows that there are some HD produced by the MMC. It is observed in 5.17c that the converter is especially affected by the 5th order harmonic (150Hz).

The second case shows that by implementing a current controller will the stability margins improve significantly for both 50MW and 10MW. The analytical model indicates that the converters should produce a stable output. The time domain simulation shows that the system indeed produces a stable power output. FFT analysis of the current shows that dc and third order harmonics are the main sources of harmonic distortion in the waveform. The dc HD magnitude is low for cases 3 and 4, and it can, therefore, be concluded that

by connecting the WF Inverter and HVDC dc harmonic increase substantially. When the power output reference is changed from 50MW to 10MW the voltage HD becomes heavily influenced by the 5th order harmonic originating from the MMC ac voltage controller. By comparing cases 2 and 4, it is observed that the THD in the voltage and current is actually reduced. Voltage and current HD reduction when connecting the converters could be a result of filtering due to transformers and line impedance.

The PLL is a vital part of the WF Inverter, as it is the converter that synchronizes the rotating reference frame to the HVDC side's angular frequency. The stability of the PLL is presented with a bode plot in 2.10. The plot shows that the PLL has good stability margins for frequencies in the operating range. That the PLL has good stability margins is proven in a time simulation when the controller is connected to a stiff gird without harmonics in case 3. The time response also shows that the PLL is fast to reach steady state and has almost no steady state error. This indicates that in order to improve the VSC output, the current control has to be improved.

6.2 Conclusion

In this thesis, a VSC and an MMC are connected by transformers to represent a WF Inverter connected to an HVDC system. The VSC converter is controlled with a current controller and PLL controller. The MMC is controlled by an ac voltage controller and circulating current control. Tests performed in frequency and time domain show that an interconnected WF Inverter-HVDC system can be controlled to produce the desired power output. The test in the time domain shows that triangular phase shifted PWM technique will divide the on-off time equally among MMC SMs. The tests in the time domain show that with high MMC SM capacitance can the voltage across each capacitor be considered constant. The test also uncovers that subsynchronous oscillation is of great concern in this high power system. Literature referenced in this paper indicates that sources of these oscillations are interaction between WF Inverter and HVDC controllers. Time domain test indicates that some of the HD originates from the control technique and interaction between the controllers can both increase and decrease subsynchronous oscillations. It is shown that the THD can be reduced for an interconnected system due to passive component impedance. Test results in the frequency domain acknowledge that HD could occur due to low stability margins.

6.3 Future Work

Future work should first aim to analyze the interconnected system in the Nyquist diagram. The goal of this should be to find the stability margins, poles and zeros. It would be especially interesting to see how the stability margins for the VSC current controller would change, as this current controller is considered to be the most significant source of HD for the system as a whole. By locating the poles and zeros it could be an alternative to try to actively cancel out certain harmonic orders with a filter in the control system. By improving the control system instead of improving power quality with power grid impedance and capacitance filters the total efficiency might be higher. During this work

the number of SMs has been changed. The number of SMs decide how many voltage levels the MMC is able to deliver for. Therefore, by increasing the number of SM HD should improve. But, the VSC has been tested with stiff 50Hz grid without that lowering the THD bellow 3% for 10MW. That means, even if one implemented a MMC with an infinite number of SMs this VSC should not be able to produce bellow 3% THD for 10MW, which would require high computing power for relatively high amount of distortion. For this reason is increasing number of SM not considered a significant improvement alone. VSC outer loop control is frequently carried out in litterateur and is more realistic to include for a real control system. This is because it is, for most cases, more useful to control power output or dc voltage across a converter than direct and quadrature current. If the goal is to analyse a more complete and realistic converter system, VSC outer loop control should be considered.

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Appendix

How the cross coupling term is derived in system equation *This extraction is presented in [19] by D.Godhei*

To transfer abc frame to dq frame, inverse Parks(P^{-1}) can be factorized from the abc-frame accordingly

$$X^{abc} = P^{-1}X^{dq0} \tag{6.1}$$

The VSC system equation is as follows

$$V^{abc} = RI^{abc} + L\frac{d}{dt}I^{abc} + V^{abc}_{conv} \tag{6.2}$$

Start off by do the transformation according to equation 6.1

$$P^{-1}V^{dq0} = P^{-1}RI^{dq0} + P^{-1}L\frac{d}{dt}I^{dq0} + P^{-1}V^{dq0}_{conv} \tag{6.3}$$

Multiply the previous equation by a regular park matrix (P)

$$PP^{-1}V^{dq0} = PP^{-1}RI^{dq0} + PL\frac{dP^{-1}}{dt}I^{dq0} + PP^{-1}L\frac{d}{dt}I^{dq0} + PP^{-1}V^{dq0}_{conv} \tag{6.4}$$

The inductor part of the equation gives the following equation, due to product derivation rule

$$PP^{-1}L\frac{d}{dt}I^{dq0} = PL\frac{dP^{-1}}{dt}I^{dq0} + PP^{-1}L\frac{d}{dt}I^{dq0} \tag{6.5}$$

For one part of the equation will the multiplied parks cancel the inverse Parks

$$PP^{-1}L\frac{d}{dt}I^{dq0} = PL\frac{dP^{-1}}{dt}I^{dq0} + L\frac{d}{dt}I^{dq0} \tag{6.6}$$

The second part of equation 6.5 yields

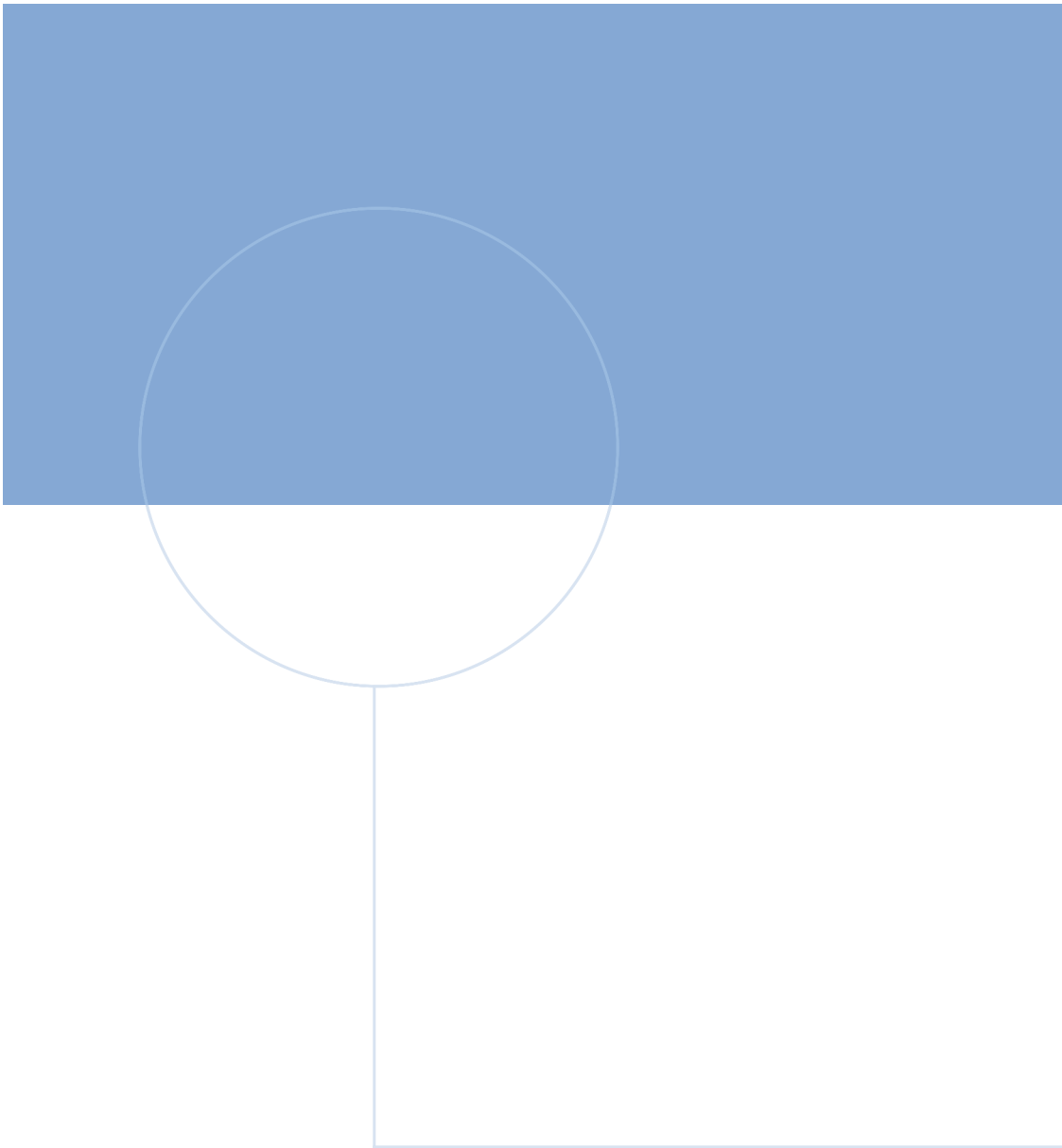
$$PL\frac{dP^{-1}}{dt}I^{dq0} = L\begin{bmatrix}0 & -\omega & 0\\ \omega & 0 & 0\\ 0 & 0 & 0\end{bmatrix}\begin{bmatrix}I^d\\ I^q\\ I^0\end{bmatrix} \tag{6.7}$$

On matrix form equation 6.5 then becomes

$$PP^{-1}L\frac{d}{dt}\begin{bmatrix}I^d\\ I^q\\ I^0\end{bmatrix} = L\begin{bmatrix}-\omega I^q\\ \omega I^d\\ 0\end{bmatrix} + L\frac{d}{dt}\begin{bmatrix}I^d\\ I^q\\ I^0\end{bmatrix} \tag{6.8}$$

When the previous equation is put into 6.4 and i^0 terms are neglected it gives the final equation

$$\begin{bmatrix}V^d\\ V^q\end{bmatrix} = \begin{bmatrix}I^d\\ I^q\end{bmatrix} + L\frac{d}{dt}\begin{bmatrix}I^d\\ I^q\end{bmatrix} + L\begin{bmatrix}-\omega I^q\\ \omega I^d\\ 0\end{bmatrix} + \begin{bmatrix}V^d_{conv}\\ V^q_{conv}\end{bmatrix} \tag{6.9}$$



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